Demonstratives of Patent Owner Greenthread, LLC

Case No: IPR2023-01242, -01243, -01244

USPTO Patent Trial and Appeal Board

Oral Hearing: November 13, 2024

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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Summary

- **“Aid carrier movement”**
  - **“Graded dopant concentration” does not necessarily “aid carrier movement.”**
  - Petitioner has presented no evidence that carriers move from the surface to the substrate.
  - Petitioner introduced a new and incorrect claim construction in its Reply.
  - All of the grounds in all of the petitions must be dismissed for lack of evidence.
- Petitioner cannot rely on inherency for “aid carrier movement”
- Petitioner’s Kawagoe grounds fail
- Petitioner’s Wieczorek grounds fail
- Petitioner’s Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

Claim Construction



"Quite apart from the written description and the prosecution history, **the claims themselves provide substantial guidance as to the meaning of particular claim terms**.

To begin with, the context in which a term is used in the asserted claim can be highly instructive. To take a simple example, the claim in this case refers to 'steel baffles,' which strongly implies that the term 'baffles' **does not inherently** mean objects made of steel."

Phillips v. AWH Corp., 415 F.3d 1303, 1314 (Fed. Cir. 2005) (internal citations omitted)

U.S. Patent 11,121,222, Claim 1

- "Graded" and "aid carrier movement" are separate limitations.
- A graded concentration "does not inherently" aid movement.
- The graded concentration must aid movement from the active region (or surface) to the substrate.


US 11,121,222 B2

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

ONSEMI EXHIBIT 1001, Page 15

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

-01242: PO Resp. [47] at 13-15; PO Sur-Reply [65] at 2-5

"Aid Carrier Movement"

US 11,121,222, Claim 1

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

US 10,510,842, Claim 1

1. A semiconductor device, comprising:
a substrate of a first doping type at a first doping level having first and second surfaces;
a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region; and
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

-01243: Ex. 1001 ('842 pat.) at 4:45-60

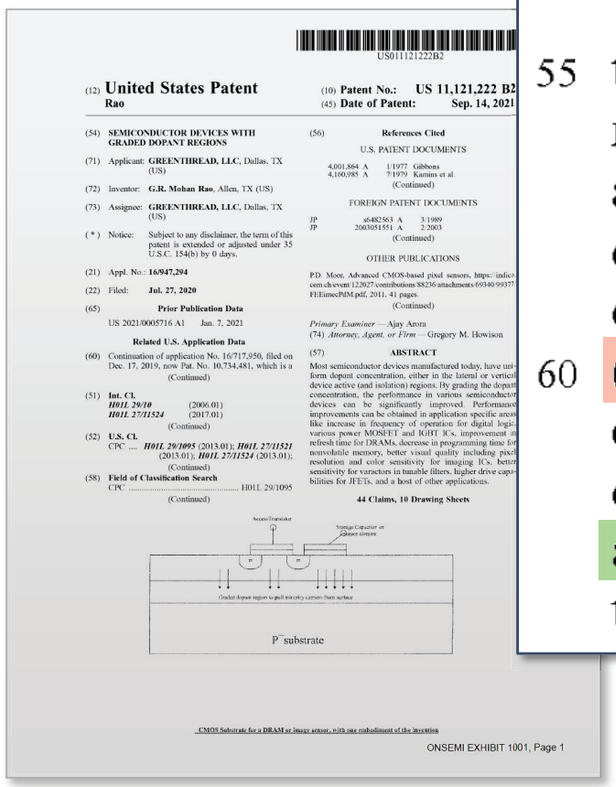
US 11,121,222, Claim 44

44. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of the surface layer;
a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and
at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

-01244: Ex. 1001 ('222 pat.) at 8:21-39

Specification

- The specification confirms that a graded concentration does not necessarily aid carrier movement.
- The "relative slope" determines whether there is a "suitable aiding drift electric field."
- The specification discloses slopes that have a magnitude of 10 to 100.



US011121222B2

(12) **United States Patent**
Rao

(10) **Patent No.: US 11,121,222 B2**
(45) **Date of Patent: Sep. 14, 2021**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

(71) Applicant: **GREENTHREAD, LLC**, Dallas, TX (US)

(72) Inventor: **G.R. Mohan Rao**, Allen, TX (US)

(73) Assignee: **GREENTHREAD, LLC**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/947,294**

(22) Filed: **Jul. 27, 2020**

(65) **Prior Publication Data**

US 2021/0005716 A1 Jan. 7, 2021

Related U.S. Application Data

(60) Continuation of application No. 16/717,950, filed on Dec. 17, 2019, now Pat. No. 10,734,481, which is a (Continued)

(51) **Int. Cl.**
H01L 29/10 (2006.01)
H01L 27/11524 (2017.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/1095*** (2013.01); ***H01L 27/11521*** (2013.01); ***H01L 27/11524*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 29/1095
(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,001,864 A 1/1977 Gibbons
4,160,985 A 7/1979 Kamins et al.
(Continued)

FOREIGN PATENT DOCUMENTS

JP s6482563 A 3/1989
JP 2003051551 A 2/2003
(Continued)

OTHER PUBLICATIONS

P.D. Moor, Advanced CMOS-based pixel sensors, https://indico.cern.ch/event/122027/contributions/88236/attachments/69340/99377/FEElmecPdM.pdf, 2011, 41 pages.
(Continued)

Primary Examiner — Ajay Arora
(74) *Attorney, Agent, or Firm* — Gregory M. Howison

(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

44 Claims, 10 Drawing Sheets

A CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

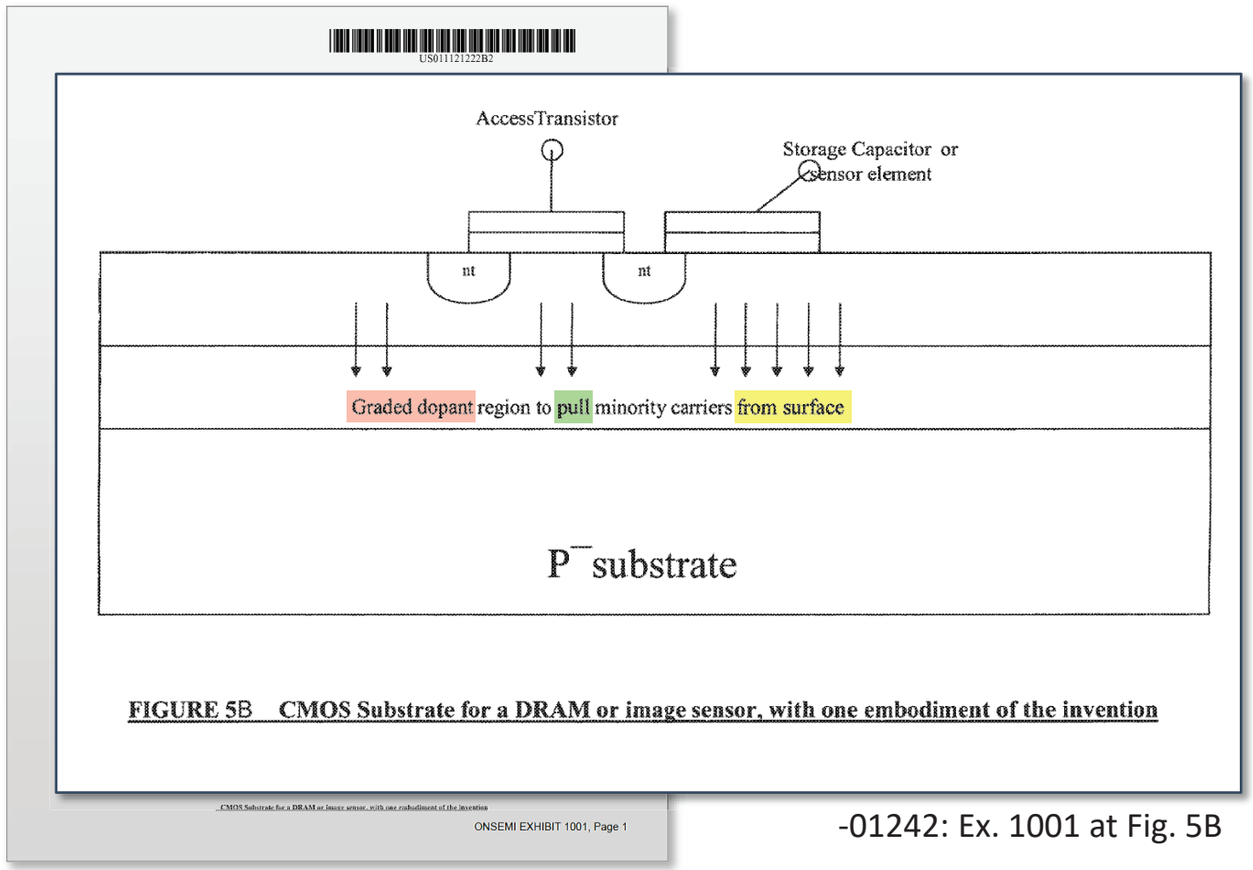
ONSEMI EXHIBIT 1001, Page 1

55 The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/cm^3$, whereas the base region is 10^{14} to $10^{16}/cm^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction
60 (1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift

-01242: Ex. 1001 ('222 pat.) at 2:54-64

Specification

- The specification confirms that the graded concentration “pulls” or “sweeps” carriers from the surface to the substrate.



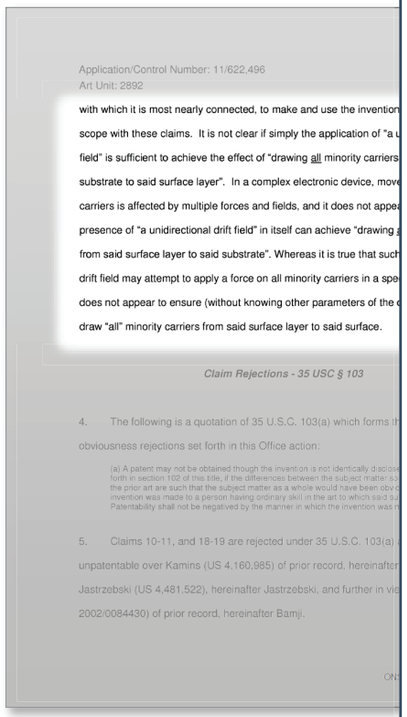
-01242: Ex. 1001 at Fig. 5B

not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n^-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n^-layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^-well and p^-wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in

-01242: Ex. 1001 (’222 pat.) at 3:52-66

Prosecution History

- The Prosecution History confirms that a graded concentration does not necessarily move carriers from the surface to the substrate.


Application/Control Number: 11/622,496
Art Unit: 2892

with which it is most nearly connected, to make and use the invention

scope with these claims. It is not clear if simply the application of "a u

field" is sufficient to achieve the effect of "drawing all minority carriers

substrate to said surface layer". In a complex electronic device, move

carriers is affected by multiple forces and fields, and it does not appe

presence of "a unidirectional drift field" in itself can achieve "drawing

from said surface layer to said substrate". Whereas it is true that such

drift field may attempt to apply a force on all minority carriers in a spe

does not appear to ensure (without knowing other parameters of the

draw "all" minority carriers from said surface layer to said surface.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms th

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclos
forth in section 102 of this title, if the differences between the subject matter s
the prior art are such that the subject matter as a whole would have been obv
invention was made to a person having ordinary skill in the art to which said su
Patentability shall not be negatived by the manner in which the invention was

5. Claims 10-11, and 18-19 are rejected under 35 U.S.C. 103(a)

unpatentable over Kamins (US 4,160,985) of prior record, hereinafter

Jastrzebski (US 4,481,522), hereinafter Jastrzebski, and further in vie

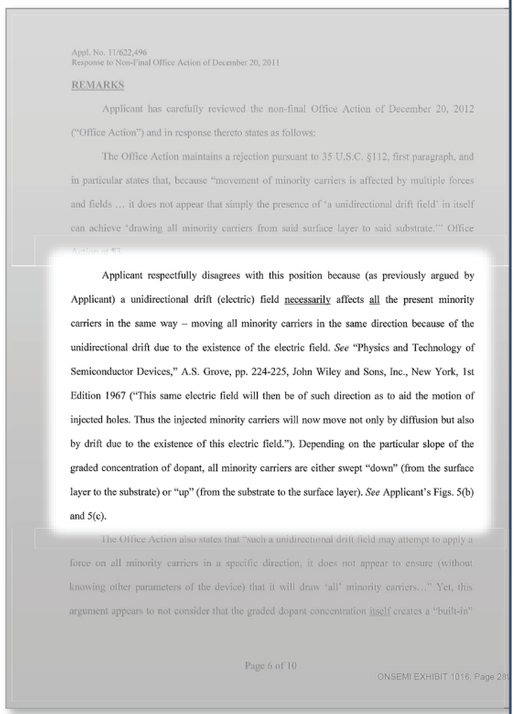
2002/0084430) of prior record, hereinafter Bamji.

with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. It is not clear if simply the application of "a unidirectional drift field" is sufficient to achieve the effect of "drawing all minority carriers from said substrate to said surface layer". In a complex electronic device, movement of minority carriers is affected by multiple forces and fields, and it does not appear that simply the presence of "a unidirectional drift field" in itself can achieve "drawing all minority carriers from said surface layer to said substrate". Whereas it is true that such a unidirectional drift field may attempt to apply a force on all minority carriers in a specific direction, it does not appear to ensure (without knowing other parameters of the device) that it will draw "all" minority carriers from said surface layer to said surface.

'195 Office Action (12/20/2011)
-01242: Ex. 1016 at 270

Prosecution History

- The Prosecution History confirms that carrier movement depends on "the particular slope" of the graded concentration.


Appl. No. 11/622,496
Response to Non-Final Office Action of December 20, 2011

REMARKS

Applicant has carefully reviewed the non-final Office Action of December 20, 2012 ("Office Action") and in response thereto states as follows:

The Office Action maintains a rejection pursuant to 35 U.S.C. §112, first paragraph, and in particular states that, because "movement of minority carriers is affected by multiple forces and fields ... it does not appear that simply the presence of 'a unidirectional drift field' in itself can achieve 'drawing all minority carriers from said surface layer to said substrate.'" Office

Applicant respectfully disagrees with this position because (as previously argued by Applicant) a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way – moving all minority carriers in the same direction because of the unidirectional drift due to the existence of the electric field. *See* "Physics and Technology of Semiconductor Devices," A.S. Grove, pp. 224-225, John Wiley and Sons, Inc., New York, 1st Edition 1967 ("This same electric field will then be of such direction as to aid the motion of injected holes. Thus the injected minority carriers will now move not only by diffusion but also by drift due to the existence of this electric field."). Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept "down" (from the surface layer to the substrate) or "up" (from the substrate to the surface layer). *See* Applicant's Figs. 5(b) and 5(c).

The Office Action also states that "such a unidirectional drift field may attempt to apply a force on all minority carriers in a specific direction, it does not appear to ensure (without knowing other parameters of the device) that it will draw 'all' minority carriers..." Yet, this argument appears to not consider that the graded dopant concentration itself creates a "built-in"

Page 6 of 10

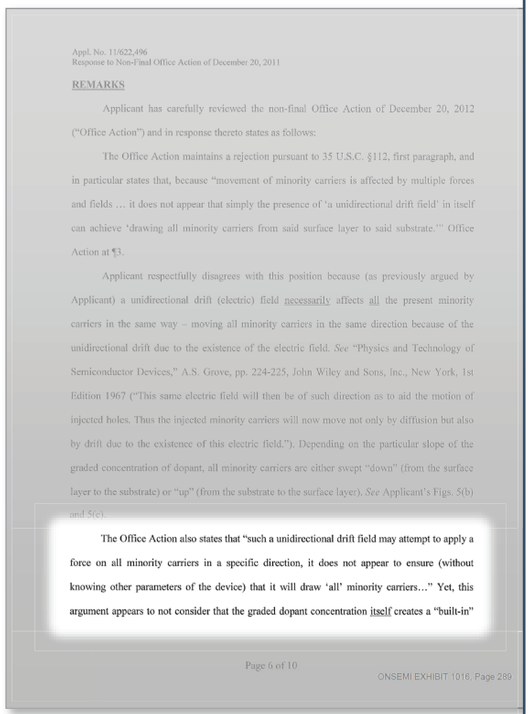
ONSEMI EXHIBIT 1016, Page 289

Applicant respectfully disagrees with this position because (as previously argued by Applicant) a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way – moving all minority carriers in the same direction because of the unidirectional drift due to the existence of the electric field. *See* "Physics and Technology of Semiconductor Devices," A.S. Grove, pp. 224-225, John Wiley and Sons, Inc., New York, 1st Edition 1967 ("This same electric field will then be of such direction as to aid the motion of injected holes. Thus the injected minority carriers will now move not only by diffusion but also by drift due to the existence of this electric field."). Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept "down" (from the surface layer to the substrate) or "up" (from the substrate to the surface layer). *See* Applicant's Figs. 5(b) and 5(c).

'195 Applicant Remarks (4/17/2012)
-01242: Ex. 1016 at 289

Prosecution History

- The Prosecution History confirms that carrier movement depends on the slope of the graded concentration.



Appl. No. 11/622,496
Response to Non-Final Office Action of December 20, 2011

REMARKS

Applicant has carefully reviewed the non-final Office Action of December 20, 2012 ("Office Action") and in response thereto states as follows:

The Office Action maintains a rejection pursuant to 35 U.S.C. §112, first paragraph, and in particular states that, because "movement of minority carriers is affected by multiple forces and fields … it does not appear that simply the presence of 'a unidirectional drift field' in itself can achieve 'drawing all minority carriers from said surface layer to said substrate.'" Office Action at ¶3.

Applicant respectfully disagrees with this position because (as previously argued by Applicant) a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way – moving all minority carriers in the same direction because of the unidirectional drift due to the existence of the electric field. *See* "Physics and Technology of Semiconductor Devices," A.S. Grove, pp. 224-225, John Wiley and Sons, Inc., New York, 1st Edition 1967 ("This same electric field will then be of such direction as to aid the motion of injected holes. Thus the injected minority carriers will now move not only by diffusion but also by drift due to the existence of this electric field."). Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept "down" (from the surface layer to the substrate) or "up" (from the substrate to the surface layer). *See* Applicant's Figs. 5(b) and 5(c).

The Office Action also states that "such a unidirectional drift field may attempt to apply a force on all minority carriers in a specific direction, it does not appear to ensure (without knowing other parameters of the device) that it will draw 'all' minority carriers…" Yet, this argument appears to not consider that the graded dopant concentration itself creates a "built-in"

Page 6 of 10

ONSEMI EXHIBIT 1016, Page 289

The Office Action also states that "such a unidirectional drift field may attempt to apply a force on all minority carriers in a specific direction, it does not appear to ensure (without knowing other parameters of the device) that it will draw 'all' minority carriers…" Yet, this argument appears to not consider that the graded dopant concentration itself creates a "built-in" electrical field that forces the movement of carriers into a particular direction, whereby the "direction" of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant. With regard to the existence of a "built-in" electric field created by a graded dopant density, *see*, e.g., Jastrzebski (US 4,481,522) col. 5, lines 11-13 (cited in Office Action). Applicant respectfully submits that this inherent "built-in" unidirectional electric field is the additional parameter for ensuring that all minority carriers are being moved in one direction and which parameter the Office Action deemed to be missing from the disclosure.

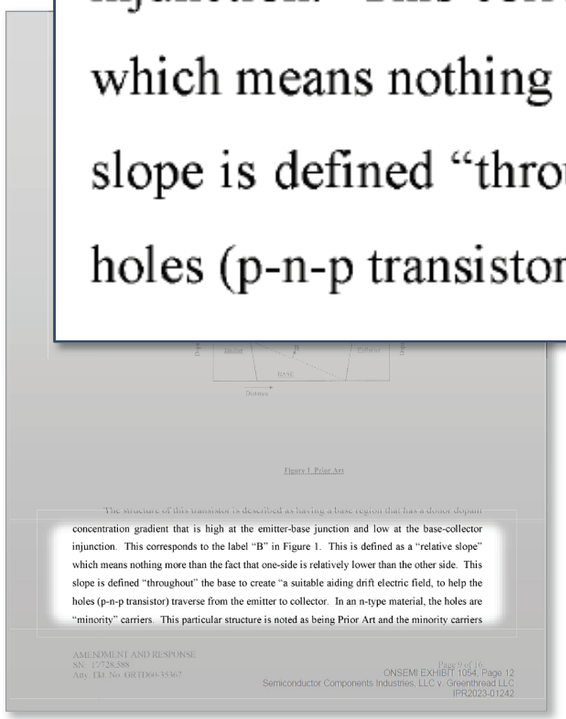
'195 Applicant Remarks (4/17/2012)
-01242: Ex. 1016 at 289-290

-01242: PO Resp. [47] at 15; PO Sur-Reply [65] at 17-19

Prosecution History

- The Prosecution History confirms that the “relative slope” determines whether there is a “suitable aiding drift electric field.”

injunction. This corresponds to the label “B” in Figure 1. This is defined as a “relative slope” which means nothing more than the fact that one-side is relatively lower than the other side. This slope is defined “throughout” the base to create “a suitable aiding drift electric field, to help the holes (p-n-p transistor) traverse from the emitter to collector. In an n-type material, the holes are


Figure 1 Prior Art

The structure of this transistor is described as having a base region that has a donor dopant concentration gradient that is high at the emitter-base junction and low at the base-collector injunction. This corresponds to the label “B” in Figure 1. This is defined as a “relative slope” which means nothing more than the fact that one-side is relatively lower than the other side. This slope is defined “throughout” the base to create “a suitable aiding drift electric field, to help the holes (p-n-p transistor) traverse from the emitter to collector. In an n-type material, the holes are “minority” carriers. This particular structure is noted as being Prior Art and the minority carriers

AMENDMENT AND RESPONSE
SN: 17/728,588
Atty. Dkt. No. GRTD60-35367
Page 9 of 16
ONSEMI EXHIBIT 1054, Page 12
Semiconductor Components Industries, LLC v. Greenthread LLC
IPR2023-01242

17/728,555 Applicant Remarks (8/1/2024)
-01242: Ex. 1054 at 12

Claim Construction



"[B]ecause the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful" in understanding the scope of the patent.

Phillips v. AWH Corp., 415 F.3d 1303, 1317 (Fed. Cir. 2005)

Claim Construction

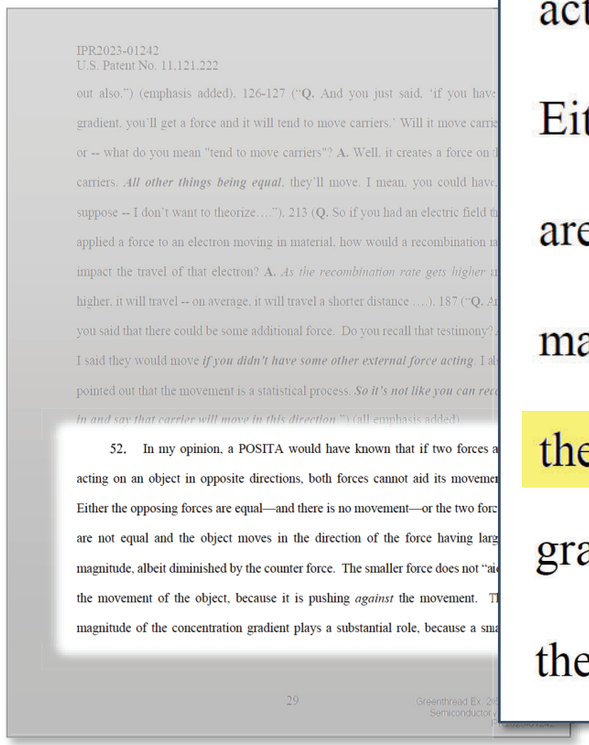


"Any ambiguity" in the prosecution history must be resolved in favor of the plain claim language, because "the claims represent the final product of a sometimes imperfect process. Representations during prosecution cannot enlarge" the claims.

Biogen, Inc. v. Berlex Lab'ys, Inc., 318 F.3d 1132, 1140 (Fed. Cir. 2003)

Dr. Glew Testimony

- Dr. Glew explained that an electric field does not necessarily "aid carrier movement."



52. In my opinion, a POSITA would have known that if two forces are acting on an object in opposite directions, both forces cannot aid its movement. Either the opposing forces are equal—and there is no movement—or the two forces are not equal and the object moves in the direction of the force having larger magnitude, albeit diminished by the counter force. The smaller force does not "aid" the movement of the object, because it is pushing *against* the movement. The gradient may not be sufficient to overcome the resistance of the material in which the gradient exists.

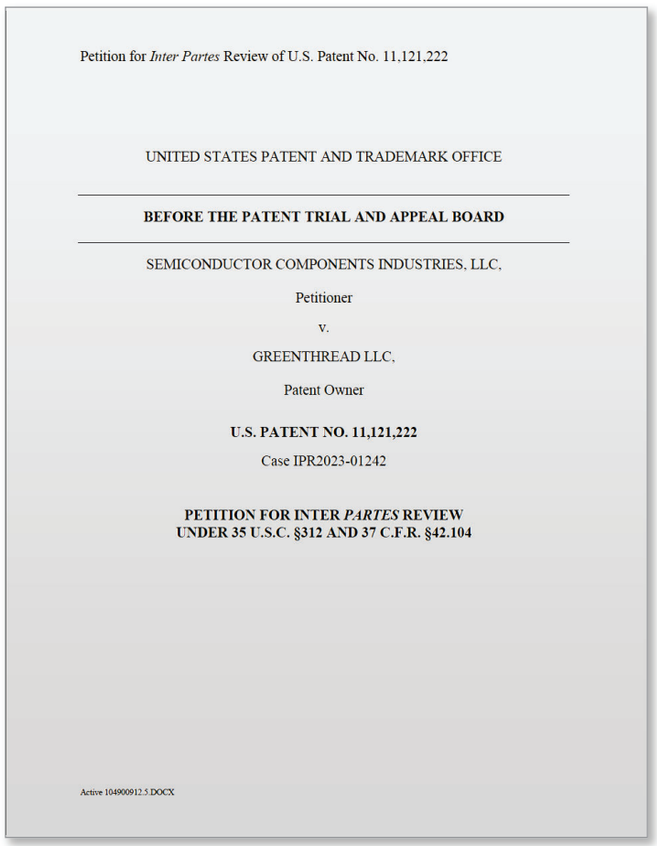
-01242: Ex. 2057 (Glew Decl.) at ¶52

Summary

- **“Aid carrier movement”**
  - **“Graded dopant concentration” does not necessarily “aid carrier movement.”**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- Petitioner cannot rely on inherency for “aid carrier movement”
- Kawagoe’s “graded dopant concentration” and improper claim mapping
- Petitioner’s Wieczorek grounds fail
- Petitioner’s Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

Petition

- Petitioner did not argue in the Petition that "any given electric field will aid electron movement."



Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,

Petitioner

v.

GREENTHREAD LLC,

Patent Owner

U.S. PATENT NO. 11,121,222

Case IPR2023-01242

PETITION FOR INTER *PARTES* REVIEW UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

Active 104900912.5.DOCX

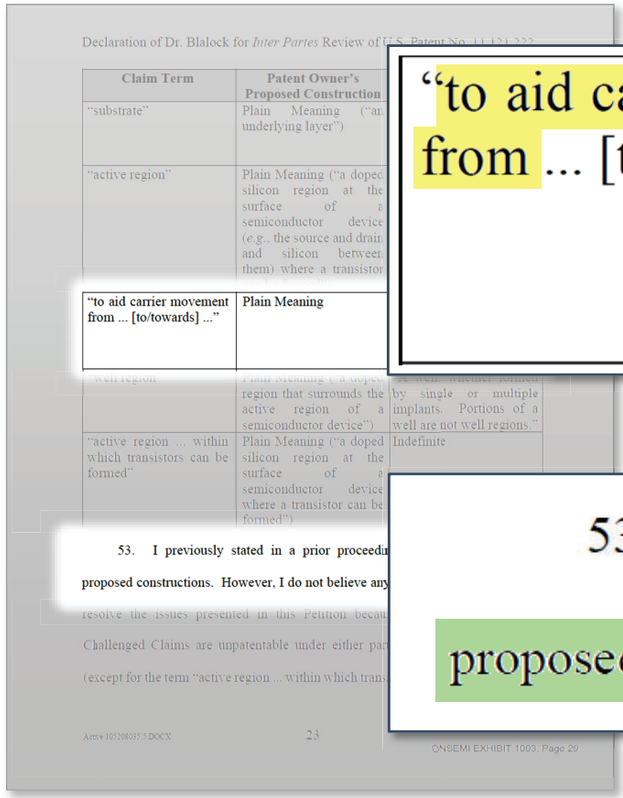
VI. CLAIM CONSTRUCTION

Claims in an IPR are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition. However, Petitioner is aware that Patent Owner and Intel Corporation took positions on the meaning of certain claims. *See* EX1036 (listing constructions in IPR2023-00420). Petitioner takes no position on whether Intel or Patent Owner's proposals are correct, but the Challenged Claims would be unpatentable under either proposal. EX1003 ¶¶52-53.

-01242: Pet. [1] at 6

Petition

- Dr. Blalock testified that "aid carrier movement" means "sweep the carriers from" the surface to the substrate.


Declaration of Dr. Blalock for *Inter Partes* Review of U.S. Patent No. 11,121,222

Claim Term	Patent Owner's Proposed Construction
"substrate"	Plain Meaning ("an underlying layer")
"active region"	Plain Meaning ("a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor
"to aid carrier movement from ... [to/towards] ..."	Plain Meaning
"well region"	Plain Meaning ("a doped region that surrounds the active region of a semiconductor device")
"active region ... within which transistors can be formed"	Plain Meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")

by single or multiple implants. Portions of a well are not well regions."

Indefinite

53. I previously stated in a prior proceedi

proposed constructions. However, I do not believe any

resolve the issues presented in this Petition becau

Challenged Claims are unpatentable under either par

(except for the term "active region ... within which trans

Active 105208035.5.DOCX 23

ONSEMI EXHIBIT 1003, Page 29

"to aid carrier movement from ... [to/towards] ..."	Plain Meaning	Indefinite Alternative Construction: "to sweep the carriers from ... [to/towards] ..."

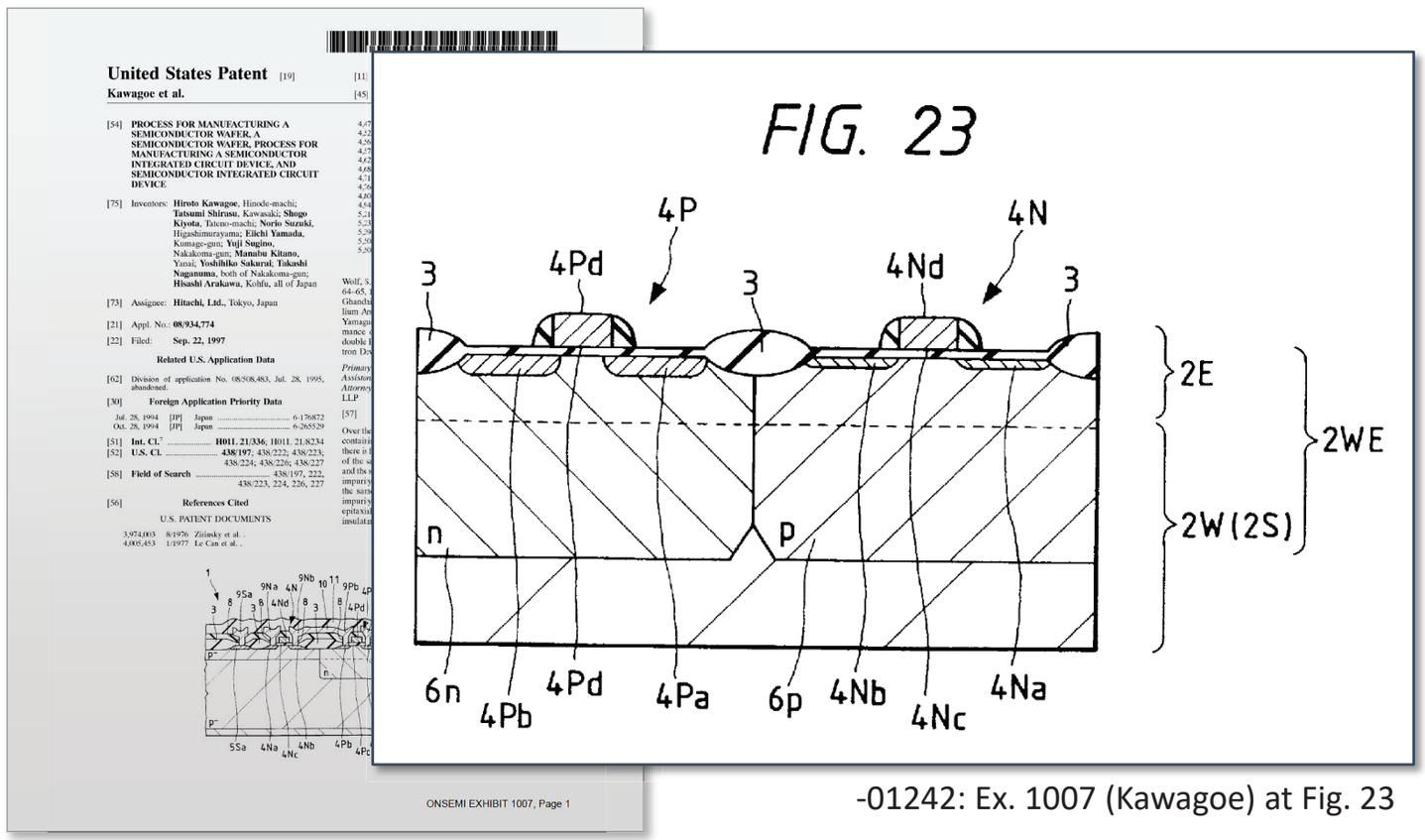
Ex. 1003 at ¶52

53. I previously stated in a prior proceeding that I supported Intel's proposed constructions. However, I do not believe any terms need be construed to

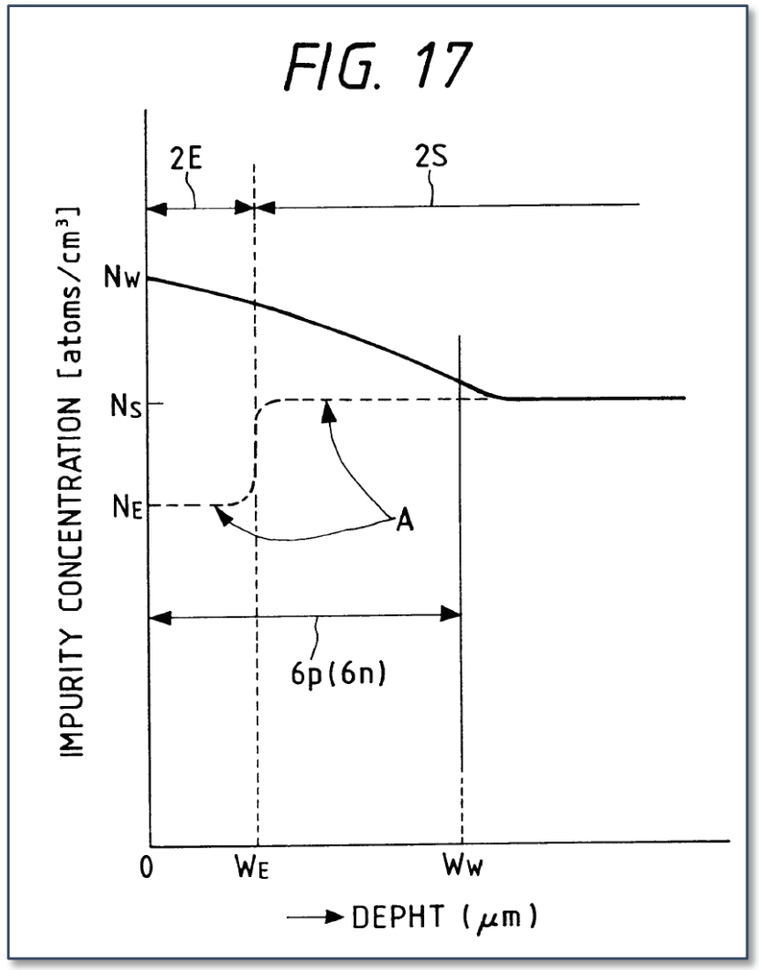
-01242: Ex. 1003 (Blalock Decl.) at ¶53

Petition

- There is <u>no</u> evidence that Kawagoe moves carriers from surface to substrate.



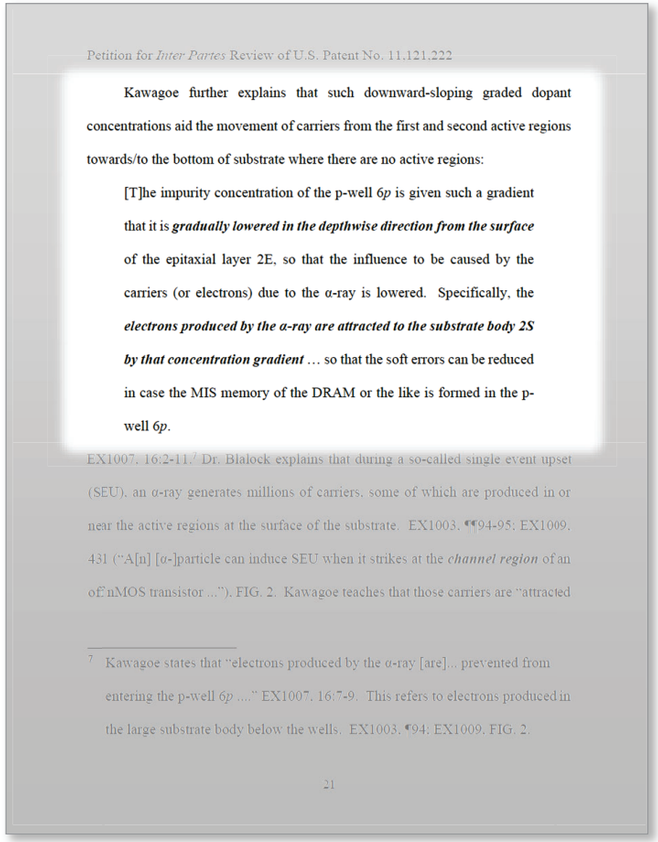
-01242: Ex. 1007 (Kawagoe) at Fig. 23



-01242: Ex. 1007 at Fig. 17

Petition

- Petitioner used ellipsis to hide that Kawagoe does not move carriers from surface to substrate.



Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222

Kawagoe further explains that such downward-sloping graded dopant concentrations aid the movement of carriers from the first and second active regions towards/to the bottom of substrate where there are no active regions:

[T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction from the surface*** of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** … so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

EX1007, 16:2-11.[7] Dr. Blalock explains that during a so-called single event upset (SEU), an α-ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate. EX1003, ¶¶94-95; EX1009, 431 ("A[n] [α-]particle can induce SEU when it strikes at the *channel region* of an of nMOS transistor ..."). FIG. 2. Kawagoe teaches that those carriers are "attracted

[7] Kawagoe states that "electrons produced by the α-ray [are]... prevented from entering the p-well 6*p* ...." EX1007, 16:7-9. This refers to electrons produced in the large substrate body below the wells. EX1003, ¶94; EX1009, FIG. 2.

21

Kawagoe further explains that such downward-sloping graded dopant concentrations aid the movement of carriers from the first and second active regions towards/to the bottom of substrate where there are no active regions:

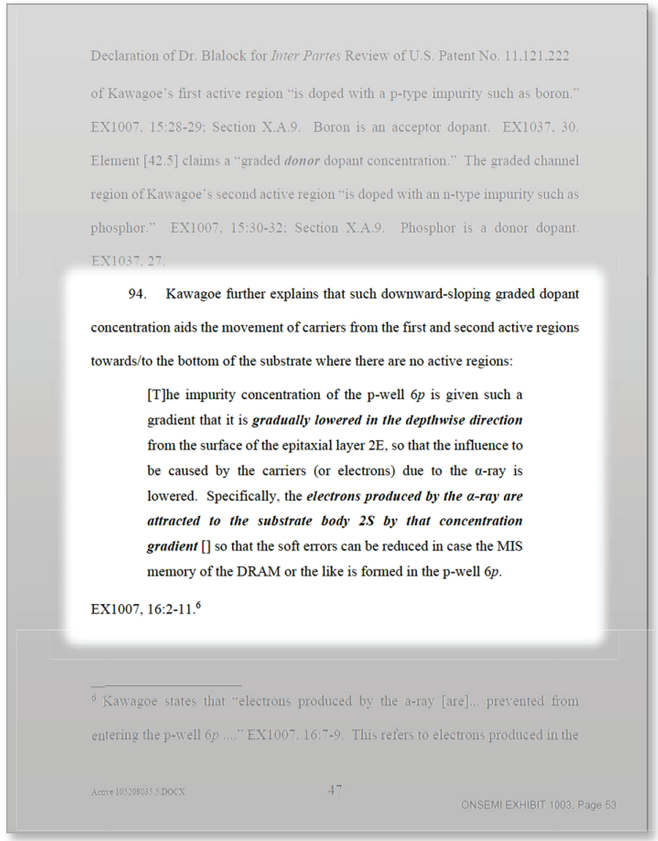
> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction from the surface*** of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** … so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

EX1007, 16:2-11.[7] Dr. Blalock explains that during a so-called single event upset

-01242: Pet. [1] at 21

Petition

- Dr. Blalock used brackets to hide that Kawagoe does not move carriers from surface to substrate.



Declaration of Dr. Blalock for *Inter Partes* Review of U.S. Patent No. 11,121,222

of Kawagoe's first active region "is doped with a p-type impurity such as boron." EX1007, 15:28-29; Section X.A.9. Boron is an acceptor dopant. EX1037, 30. Element [42.5] claims a "graded ***donor*** dopant concentration." The graded channel region of Kawagoe's second active region "is doped with an n-type impurity such as phosphor." EX1007, 15:30-32; Section X.A.9. Phosphor is a donor dopant. EX1037, 27.

94. Kawagoe further explains that such downward-sloping graded dopant concentration aids the movement of carriers from the first and second active regions towards/to the bottom of the substrate where there are no active regions:

> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

EX1007, 16:2-11.[6]

[6] Kawagoe states that "electrons produced by the a-ray [are]... prevented from entering the p-well 6*p* ...." EX1007, 16:7-9. This refers to electrons produced in the

Active 105208035.5.DOCX 47 ONSEMI EXHIBIT 1003, Page 53

94. Kawagoe further explains that such downward-sloping graded dopant concentration aids the movement of carriers from the first and second active regions towards/to the bottom of the substrate where there are no active regions:

> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

EX1007, 16:2-11.[6]

-01242: Ex. 1003 (Blalock Decl.) at ¶94

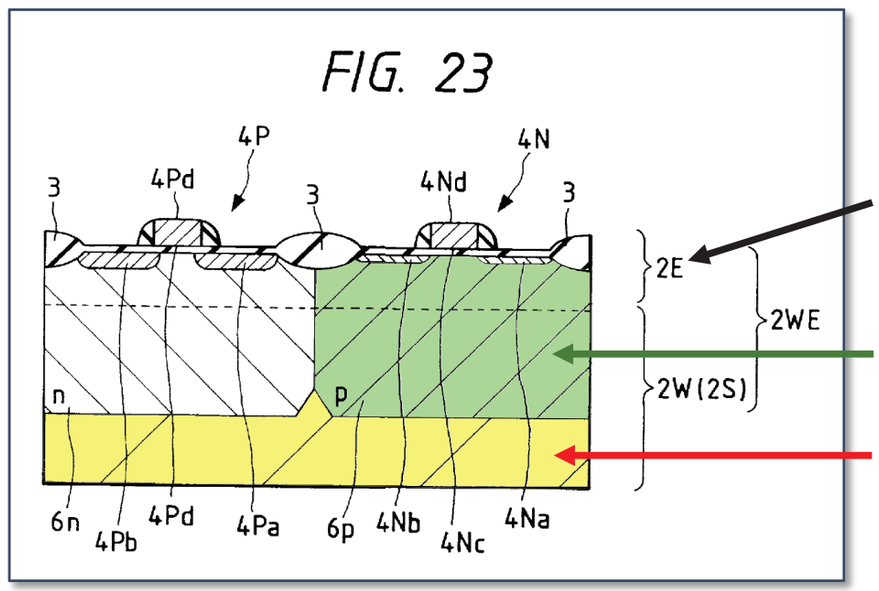
Kawagoe

- Kawagoe actually says it <u>prevents</u> the electrons from entering the p-well.
- Kawagoe does <u>not</u> move electrons from active region (surface) to substrate.

Incidentally, in the present embodiment 4, the aforementioned p-well **6***p* and n-well **6***n* are formed to extend from the surface of the epitaxial layer **2**E to the upper portion of the semiconductor substrate body **2**S, as shown in FIGS. **16** and **17**, and the p-well **6***p* and n-well **6***n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer **2**E. Thus, the impurity concentration of the p-well **6***p* is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer **2**E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body **2**S by that concentration gradient and prevented from entering the p-well **6***p* so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well **6***p*. The impurity

ONSEMI EXHIBIT 1007, Page 1

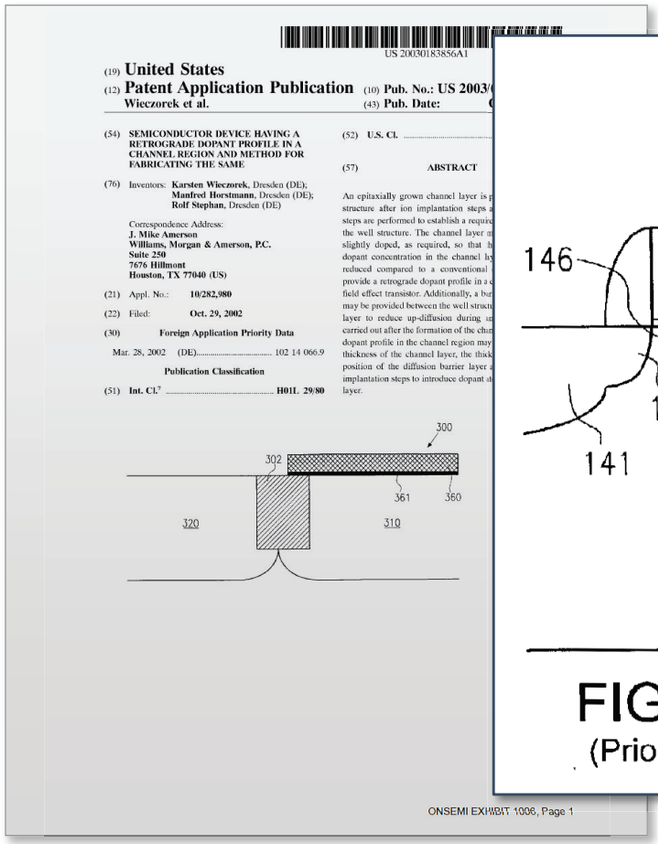
-01242: Ex. 1007 at 15:62-16:11



-01242: Ex. 1007 (Kawagoe) at Fig. 23

Wieczorek

- Petitioner relies entirely on the following two figures.
- There is no evidence that carriers move from the surface to the substrate.



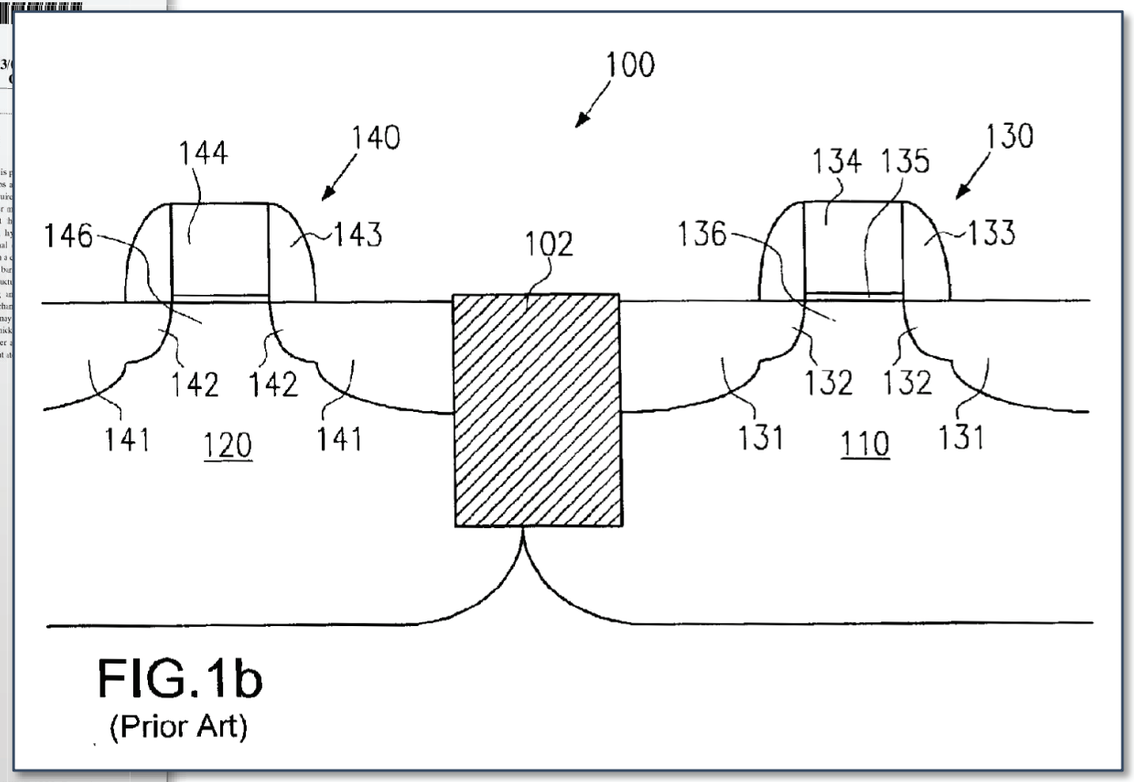


FIG.1b
(Prior Art)

-01242: Ex. 1006 (Wieczorek) at Fig. 1b

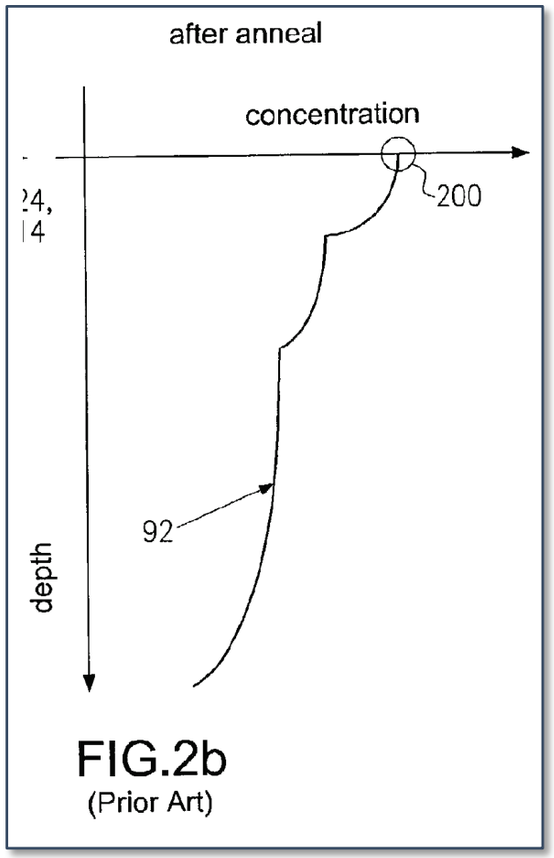
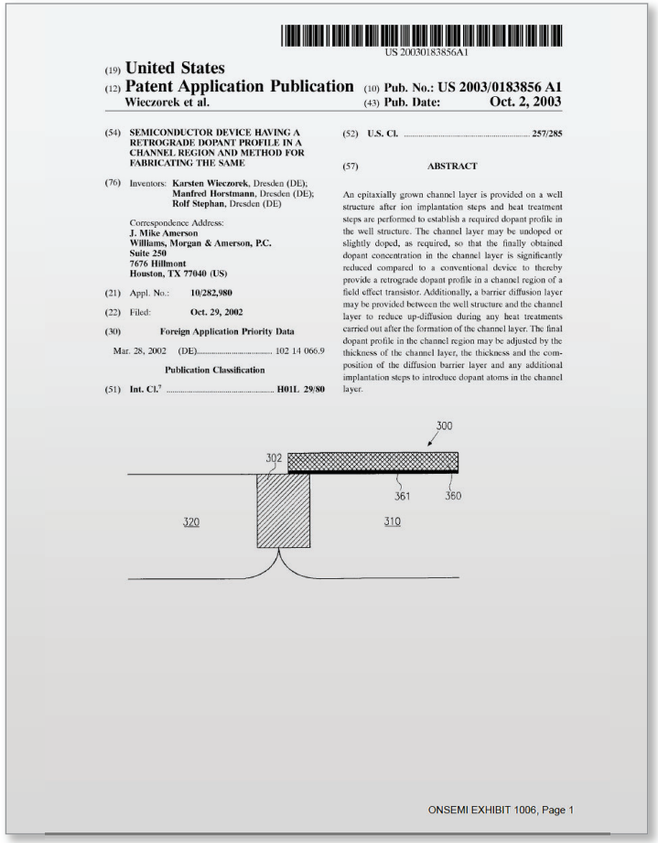


FIG.2b
(Prior Art)

-01242: Ex. 1006 at Fig. 2b

Wieczorek

- Wieczorek never mentions carriers, much less moving carriers from the surface to the substrate.



US 20030183856A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2003/0183856 A1**

Wieczorek et al. (43) **Pub. Date: Oct. 2, 2003**

(54) **SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME**

(76) Inventors: **Karsten Wieczorek**, Dresden (DE); **Manfred Horstmann**, Dresden (DE); **Rolf Stephan**, Dresden (DE)

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(21) Appl. No.: **10/282,980**

(22) Filed: **Oct. 29, 2002**

(30) **Foreign Application Priority Data**

Mar. 28, 2002 (DE)..... 102 14 066.9

Publication Classification

(51) **Int. Cl.**[7] **H01L 29/80**

(52) **U.S. Cl.** **257/285**

(57) **ABSTRACT**

An epitaxially grown channel layer is provided on a well structure after ion implantation steps and heat treatment steps are performed to establish a required dopant profile in the well structure. The channel layer may be undoped or slightly doped, as required, so that the finally obtained dopant concentration in the channel layer is significantly reduced compared to a conventional device to thereby provide a retrograde dopant profile in a channel region of a field effect transistor. Additionally, a barrier diffusion layer may be provided between the well structure and the channel layer to reduce up-diffusion during any heat treatments carried out after the formation of the channel layer. The final dopant profile in the channel region may be adjusted by the thickness of the channel layer, the thickness and the composition of the diffusion barrier layer and any additional implantation steps to introduce dopant atoms in the channel layer.

ONSEMI EXHIBIT 1006, Page 1

[0009] **FIG. 2***a* is a graph, in which the dopant concentration of the N-well structure **120** and the P-well structure **110** is depicted with respect to the depth in the respective well structures. In particular, it is evident from **FIG. 2***a* that the V_T implantation (**114**, **124**), indicated by the same reference number as the respective implantation portions, leads to a dopant concentration that significantly decreases at the vicinity of the surface of the semiconductor device **100**. That is, the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile in the N-well structure **120** and the P-well structure **110** near the surface of the semiconductor device **100**, where, after completion of the device, a channel will form during operation of the device.

-01242: Ex. 1006 at [0009]

[0011] **FIG. 2***b* shows a corresponding graph with a typical dopant profile with respect to the depth of the respective well structure. Due to the up-diffusion of the dopant atoms during the heat treatment, the initially retrograde profile in the vicinity of the surface of the semiconductor device **100**, as indicated by reference number **200**, may have become substantially uniformly distributed.

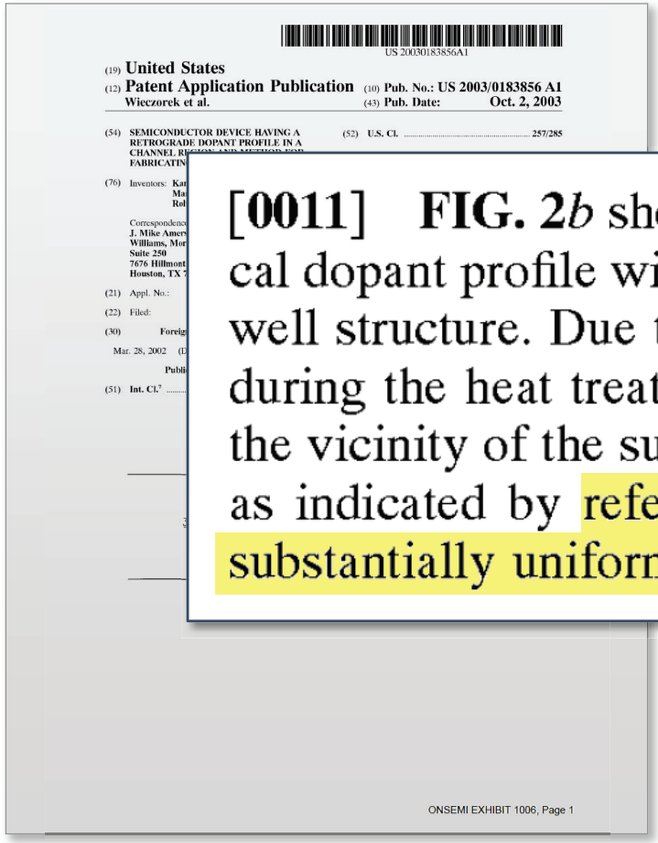
-01242: Ex. 1006 at [0011]

[0013] Typically, the N-channel transistor **130** and the P-channel transistor **140** are formed by the following processes. After the heat treatment, the gate insulation layer **135** is formed, wherein the gate insulation layer may be deposited by chemical vapor deposition (CVD), or, if an oxide layer is used, a rapid thermal furnace process or a conventional furnace oxidation process may be used. Since, commonly, elevated temperatures are involved in fabricating the gate insulation layer **135**, this process also contributes to a further diffusion of the dopants within the P-well structure **110** and the N-well structure **120**. Thereafter, polysilicon is deposited and patterned by sophisticated photolithography techniques to form the gate electrodes **134** and **144**. With a first implantation, the extensions **132** and **142** are defined, and, subsequently, the spacer elements **133**, **143** are formed and serve as an implantation mask during a subsequent implantation process for defining the source and drain regions **131**, **141**. Since a further heat treatment is necessary to activate the dopants within the regions **131**, **132** and **141**, **142** and to cure any crystal damage caused by the preceding implantation steps, the initial dopant concentration, as shown in **FIG. 2***a*, will be even more strongly affected so that, after the plurality of heat treatments, the actual dopant concentration will be represented by the graph shown in **FIG. 2***b*. In particular, it is thus very difficult to obtain or to maintain a retrograde dopant profile in the channel regions **136** and **146**, which would be desirable to achieve an improved carrier mobility therein.

-01242: Ex. 1006 (Wieczorek) at [0013]

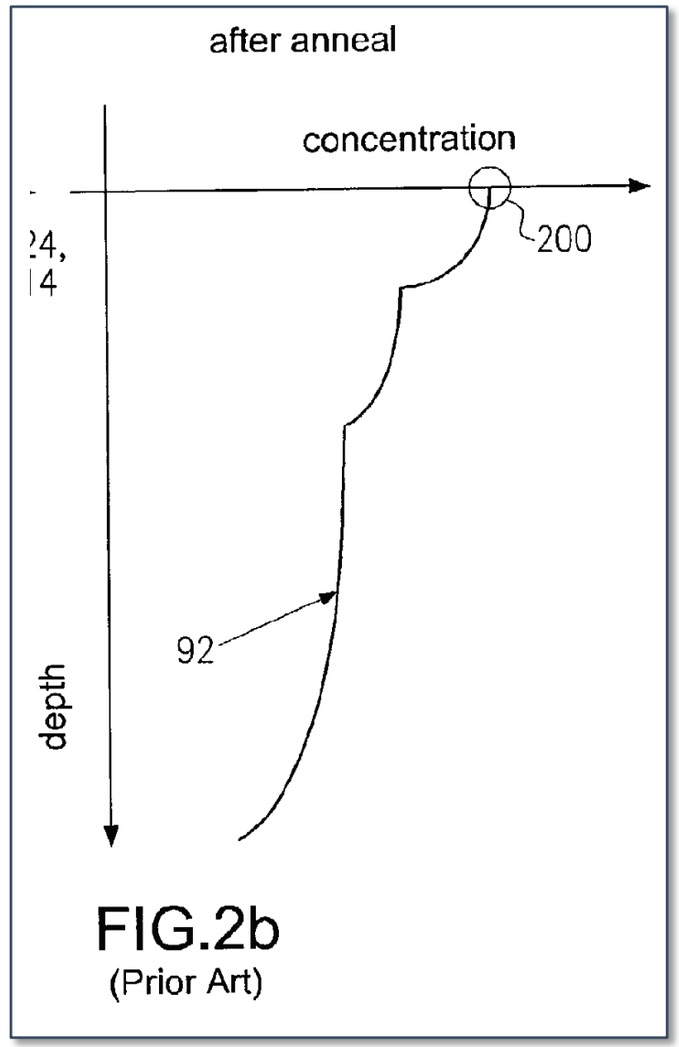
Wieczorek

- Wieczorek says the gradient concentration may be uniform.



[0011] **FIG. 2*b*** shows a corresponding graph with a typical dopant profile with respect to the depth of the respective well structure. Due to the up-diffusion of the dopant atoms during the heat treatment, the initially retrograde profile in the vicinity of the surface of the semiconductor device **100**, as indicated by reference number **200**, may have become substantially uniformly distributed.

-01242: Ex. 1006 (Wieczorek) at [0011]



-01242: Ex. 1006 at Fig. 2b

Wieczorek

- Dr. Blalock admitted the force depends on the slope, and that he did not calculate the slope for any of the references.

Q. How do you know the magnitude of the force a dopant concentration puts on carriers?

A. Well, as the patent owner discussed -- I have references to it, but it's -- I don't know. Anyway, it's related to the -- the steepness of the gradient, the slope of the concentration gradient. And that was also well known by a POSITA as well, which the patent owner pointed out also.

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IPR2023-01242

-01242: Ex. 2058 at 89:3-10

Q. And regarding any of these three references, for the mapping of the claim phrase "aid carrier movement," have you looked at any aspect of the gradient other than its being downward sloping?

MR. SPEEGLE: Objection, form.

THE WITNESS: As I've said, the patent owner tells us that that's sufficient, so that's what I did. I have not done calculations of the slope per se.

-01242: Ex. 2058 (Blalock Dep. Tr.) at 195:8-16

Wieczorek

- There is no way to determine the slope, or whether there is a sufficient force.

60. Dr. Blalock testified that he did not calculate the slope of the concentration gradient that he said Wieczorek discloses. Ex. 2058, 195 ("Q. And regarding any of these three references [including Wieczorek], for the mapping of the claim phrase 'aid carrier movement,' have you looked at any aspect of the gradient other than its being downward sloping? … THE WITNESS: As I've said, the patent owner tells us that that's sufficient, so [t]hat's what I did. I have not done calculations of the slope per se."). It would have been impossible for Dr. Blalock to make such a calculation because the dopant gradient Petitioner points to in Figure 2B (and Wieczorek generally) does not have any values from which one could calculate a slope. In mathematical terms, the slope in each direction (X, Y, and Z) is known formally as the gradient vector. The magnitude of the slope is essential to determine the magnitude of the force the dopant gradient places on the carrier and thus the net force.

-01242: Ex. 2057 (Glew Decl.) at ¶60

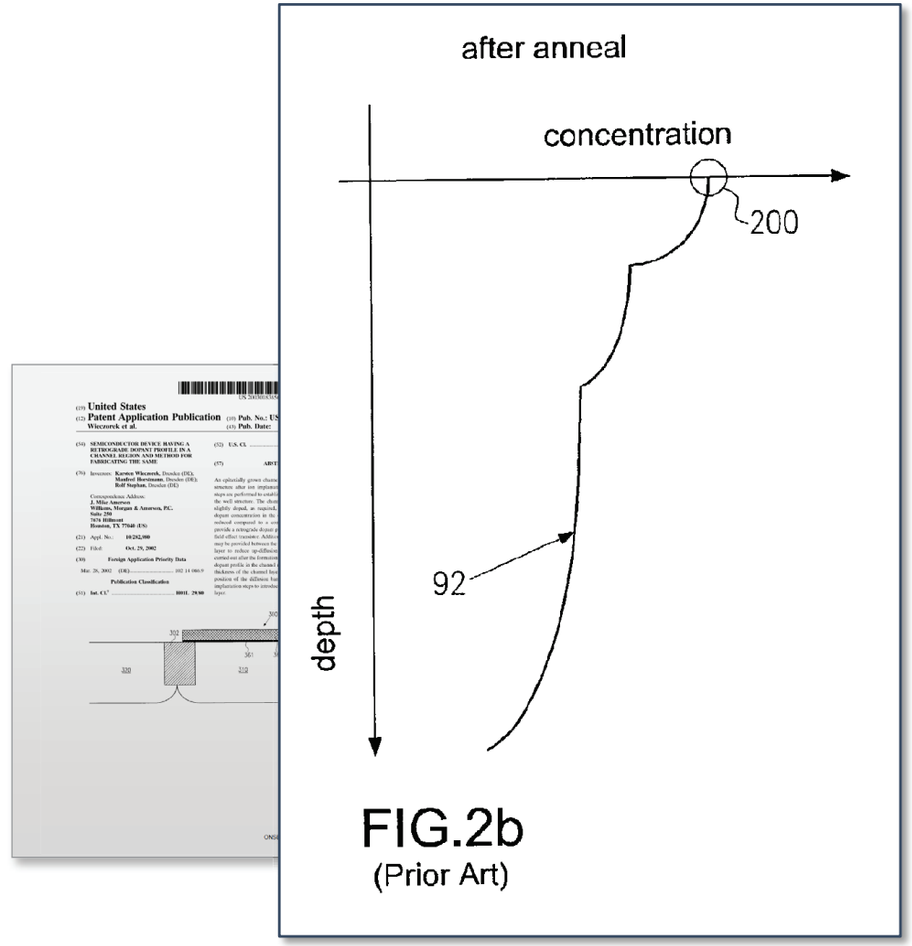
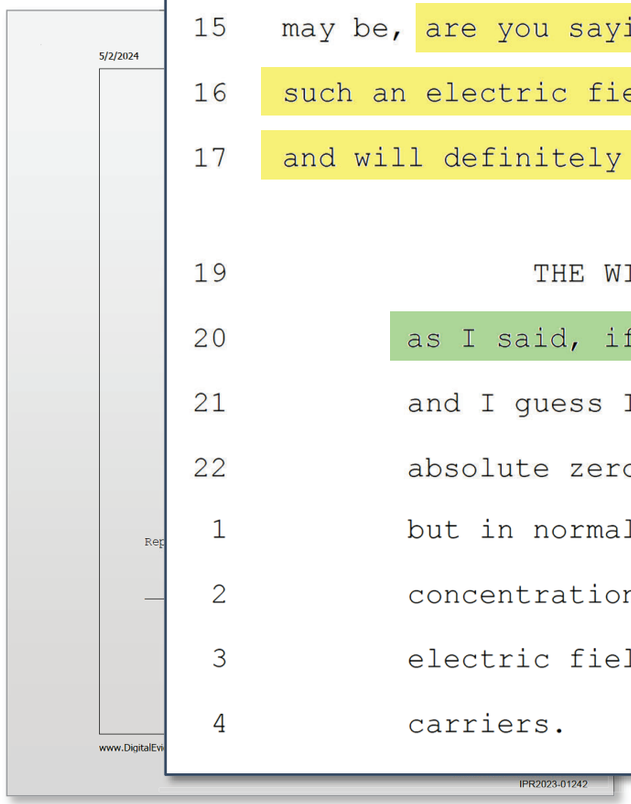


FIG.2b
(Prior Art)

-01242: Ex. 1006 (Wieczorek) at Fig. 2b

Wieczorek

- Dr. Blalock admitted that an electric field does not always move carriers.



Q. I'm saying apart from what the patent owner said and whatever your interpretation of that may be, are you saying that as a matter of physics, such an electric field will definitely be created and will definitely move carriers?

* * *

THE WITNESS: I mean, it depends on -- as I said, if there are no other fields -- and I guess I should qualify for not an absolute zero temperature, all this stuff, but in normal circumstances, if you have a concentration gradient, it will result in an electric field, which will then act on the carriers.

Q. So you mentioned that if there aren't other fields present and the carrier was introduced into that field, you'll move the carrier.

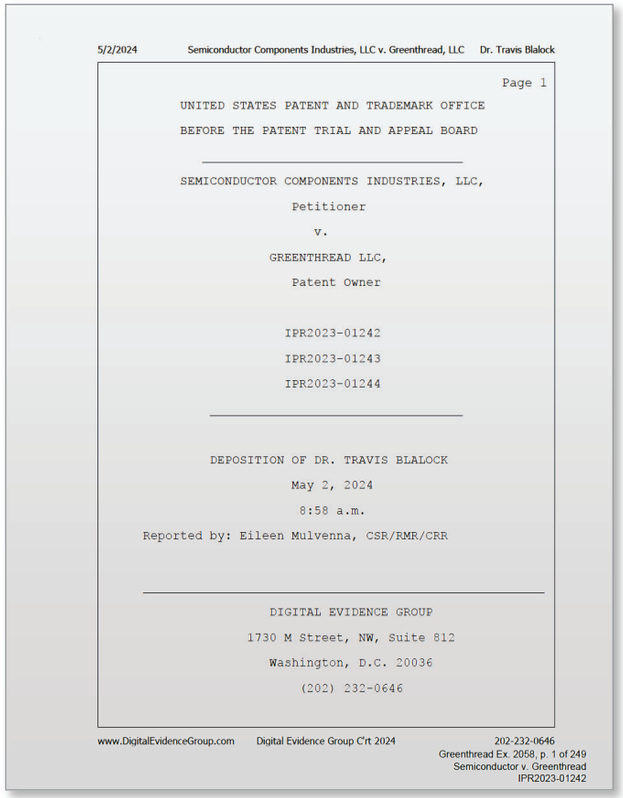
Where could other fields come from?

A. Externally applied voltages from the circuit, if the structure's in a circuit, things like that. Or I suppose some environmental effect. I don't know.

-01242: Ex. 2058 (Blalock Dep. Tr.) at 131:13-132:13

Dr. Blalock Testimony

- Dr. Blalock also admitted that there may be a force that is larger than the gradient force.



5/2/2024 Semiconductor Components Industries, LLC v. Greenthread, LLC Dr. Travis Blalock

Page 1

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,
Petitioner
v.
GREENTHREAD LLC,
Patent Owner

IPR2023-01242
IPR2023-01243
IPR2023-01244

DEPOSITION OF DR. TRAVIS BLALOCK
May 2, 2024
8:58 a.m.
Reported by: Eileen Mulvenna, CSR/RMR/CRR

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Greenthread Ex. 2058, p. 1 of 249
Semiconductor v. Greenthread
IPR2023-01242

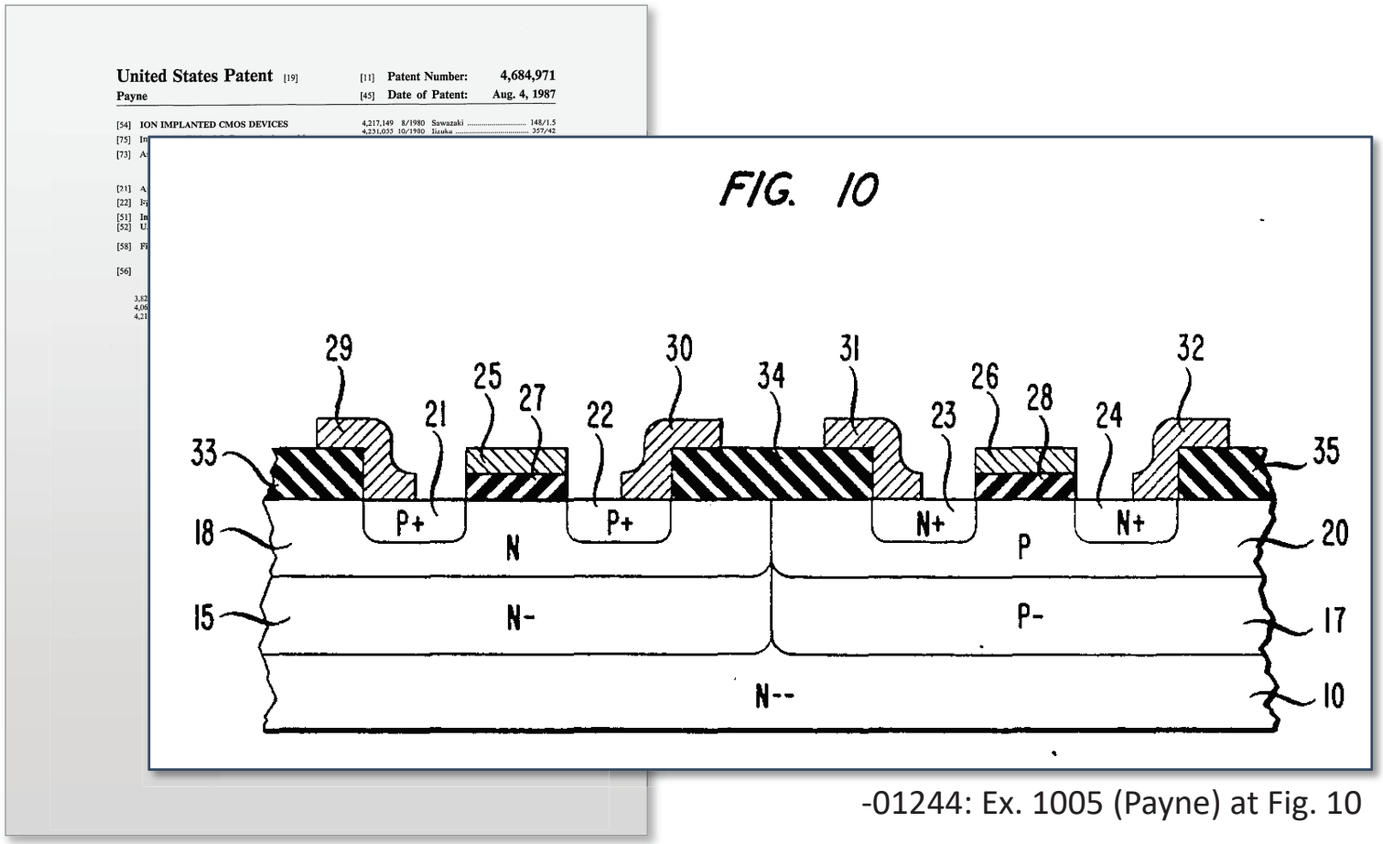
17 Q. Is there a gradient that would be so
18 steep or so shallow, that it would not aid carrier
19 movements?
* * *
22 THE WITNESS: It will create a force.

1 A shallow or a steep one will create a force.
2 As I said a few moments ago, as I've already
3 answered, if there are -- through some other
4 imagined, who knows, means, someone creates
5 an additional force, that might be larger
6 than the force created by the gradient.
7 But there will be a force -- that
8 mechanism, the gradient mechanism which
9 creates the force, which acts in the
10 direction to move the carriers, will be
11 there.

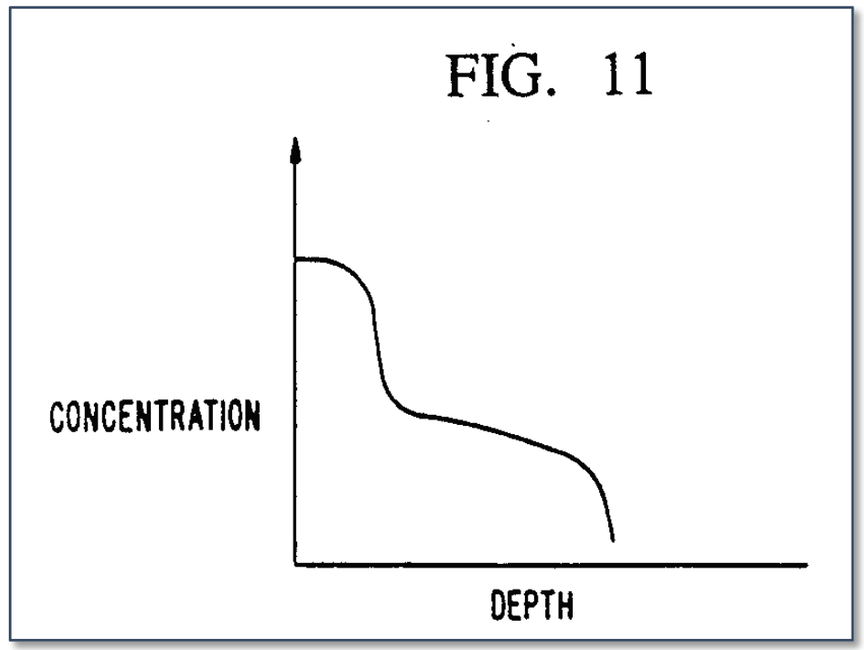
-01242: Ex. 2058 (Blalock Dep. Tr.) at 137:17-138:11

Payne

- Petitioner relies entirely on the following two figures.
- There is no evidence that carriers move from the surface to the substrate.



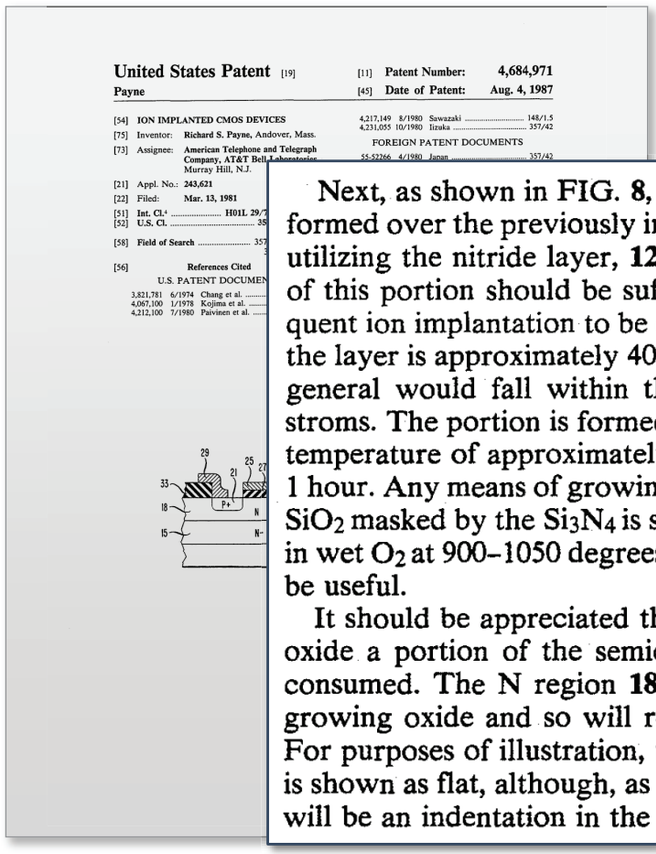
-01244: Ex. 1005 (Payne) at Fig. 10



-01244: Ex. 1005 at Fig. 11

Payne

- Payne <u>never</u> mentions carriers, much less moving carriers from the surface to the substrate.



United States Patent [19]
Payne

[11] Patent Number: 4,684,971
[45] Date of Patent: Aug. 4, 1987

[54] ION IMPLANTED CMOS DEVICES
[75] Inventor: Richard S. Payne, Andover, Mass.
[73] Assignee: American Telephone and Telegraph Company, AT&T Bell Laboratories, Murray Hill, N.J.
[21] Appl. No.: 243,621
[22] Filed: Mar. 13, 1981
[51] Int. Cl.[4] H01L 29/7
[52] U.S. Cl. 35
[58] Field of Search 357
[56] References Cited
U.S. PATENT DOCUMEN
3,821,781 6/1974 Chang et al. .....
4,067,100 1/1978 Kojima et al. .....
4,212,100 7/1980 Paviten et al. .....
4,217,149 8/1980 Sawazaki 148/1.5
4,231,055 10/1980 Iizuka 357/42
FOREIGN PATENT DOCUMENTS
55-52266 4/1980 Japan 357/42

Next, as shown in FIG. **8**, a thick oxide portion **19** is formed over the previously implanted regions **18** and **15** utilizing the nitride layer, **12**, as a mask. The thickness of this portion should be sufficient to block the subsequent ion implantation to be described. In this example, the layer is approximately 4000 Angstroms thick, but in general would fall within the range 3000–4500 Angstroms. The portion is formed by heating in wet O_2 at a temperature of approximately 1000 degrees Celsius for 1 hour. Any means of growing the requisite thickness of SiO_2 masked by the Si_3N_4 is suitable. Typically, heating in wet O_2 at 900–1050 degrees Celsius for 1–4 hours will be useful.

It should be appreciated that in the formation of the oxide a portion of the semiconductor surface will be consumed. The N region **18** will diffuse ahead of the growing oxide and so will remain at the new surface. For purposes of illustration, the semiconductor surface is shown as flat, although, as a result of oxidation, there will be an indentation in the area of the N tub.

-01244: Ex. 1005 (Payne) at 4:38-59

a separate step is not ordinarily needed. The resulting impurity profile in both tubs thereby has the general shape illustrated in FIG. **11**, where the abscissa is depth and the ordinate is impurity concentration.

The oxide layer can then be stripped off, for example, with a solution of dilute HF, and fabrication may proceed in accordance with standard techniques to produce the CMOS device depicted in FIG. **10**. The p-channel device includes source and drain regions, **21** and **22**, respectively, of P^+ conductivity type formed with the N surface region, **18**. Similarly, the n-channel device includes source and drain regions, **23** and **24**, of N^+ conductivity type formed within the P surface region **20**. These source and drain regions would typically have a surface impurity concentration of approximately 10^{19}–10^{20} ions/cm^3 and a depth of 1 μm. It will be noted, therefore, that the n and p surface regions, **18** and **20**, will be present at the surface of their respective devices except for the areas comprising the source and drain. The depth of the surface regions should be at least as great as that of the source and drain regions.

The devices further include gate electrodes, **25** and **26**, typically comprising polycrystalline silicon, formed over gate oxide portions **27** and **28**. Ohmic contacts to source and drain regions are provided by metal portions, **29–32**, typically comprising aluminum, formed over field oxide portions **33–35** and contact windows in said oxide. These features and their method of fabrication are well-known in the art and consequently are not discussed in detail.

It will be appreciated that during the drive-in of the source and drain regions, **21–24**, the regions **18**, and **20** will also be driven somewhat further into the substrate, while the depth of the tubs **15** and **17** is essentially unaffected. In a typical device, the final depth of surface regions **18** and **20** would be approximately 1–2μ and the depth of tub regions **15** and **17** would be typically 3–8μ. The surface impurity concentration of the surface regions is typically $0.5–5 \times 10^{16}$ ions/cm^3 and that of the tub regions is typically 10^{15}–10^{16} ions/cm^3, with the former concentration being at least twice as much as the latter over these ranges.

The major advantage in formation of the high-low implant profile of FIG. **11** is illustrated in FIGS. **12** and

-01244: Ex. 1005 at 5:14-57

device. In a device fabricated in accordance with the present invention, as illustrated in FIG. **13**, the composite profiles remain high and then fall off rapidly at a much closer distance from the boundary. This is due to the high impurity concentration of surface regions **18** and **20** as well as the short diffusion lengths of these regions. On each side of the boundary, therefore, the high impurity concentration of the surface region (e.g., **18**) is compensated for only by the low concentration tub region of the adjacent device (**17**) and substantial overlap is permitted. In a typical device, it is expected

-01244: Ex. 1005 at 6:7-17

Summary

- **“Aid carrier movement”**
  - **“Graded dopant concentration” does not necessarily “aid carrier movement.”**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - All of the grounds in all of the petitions must be dismissed for lack of evidence.
- Petitioner cannot rely on inherency for “aid carrier movement”
- Kawagoe’s “graded dopant concentration” and improper claim mapping
- Petitioner’s Wieczorek grounds fail
- Petitioner’s Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

Petitioner's New Claim Construction

- Petitioner now argues that "any given electric field will aid electron movement."

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC
Petitioner

v.

GREENTHREAD LLC
Patent Owner

Under the strawman guise of arguing about whether "graded" means "aided," PO repeatedly mischaracterizes prior relevant statements about what "aid[ing] carrier movement" requires. To be clear, Petitioner is not arguing that "graded" means "aided," but Petitioner nonetheless disagrees with PO's characterization of the "aid carrier movement" limitation. In particular, PO wrongly suggests that the "aid carrier movement" limitation requires calculating the slope of a dopant concentration, which is not disclosed in the patent, not discussed in the prosecution history, and would be inconsistent with PO's statements in district court litigation.

-01242: Pet. Reply [62] at 2-3

Third, PO's argument that Kawagoe only teaches "using a graded slope to *impede* carrier movement" is incomprehensible. POR, 16 (emphasis in original). As PO's expert Dr. Glew admitted, whether an electric field from a graded dopant concentration aids movement or impedes movement ***depends on the direction of the movement***. EX1052, 83:13-89:13, 92:2-97:8, 102:2-109:14, 109:25-116:3, 121:19-123:15. It, thus, makes no sense to say an electric field would impede all movement (nor aid all movement): any given electric field will aid electron movement in one direction and impede electron movement in the opposite direction. *Id.* So, when Kawagoe says that "electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well," this means an electric field aids carrier movement "to the substrate body 2S" and impedes carrier movement in the opposite direction "entering the p-well." *Id.*; EX1007, 16:2-11, Figs. 17, 23; Petition, 27-28.

-01242: Pet. Reply [62] at 7

electric field would move carriers in the opposite direction. *Id.* So, "graded" does not mean "aided," but "graded" does mean "electric field," and an "electric field" means "aided" in one direction. This is why Dr. Blalock correctly focused on direction of the dopant concentration slope in Kawagoe (and Wieczorek). *See e.g.*, EX2058, 73:20-76:5, 167:9-169:7, 189:18-193:14, 196:8-198:8.

-01242: Pet. Reply [62] at 9

-01242: PO Sur-Reply [65] at 2-4

Petitioner's New Claim Construction

"[T]he petitioner's petition … is supposed to guide the life of the litigation."

SAS Inst. v. Iancu, 584 U.S. 357, 366, 138 S.Ct. 1348, 1356 (2018)

"Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case of unpatentability."

U.S. Patent Trial and Appeal Board, Consolidated Trial Practice Guide 73 (Nov. 2019)

Petitioner's New Claim Construction



"If [PO] had been given notice of the [new] theory, it could have challenged the Board's interpretation…. The Board deprived [PO] of that opportunity, and we have held similar deprivations of notice regarding non-prior-art [*i.e.*, claim constructions] to be violations of the APA."

M & K Holdings, Inc. v. Samsung Elecs. Co., Ltd., 985 F.3d 1376, 1385 (Fed. Cir. 2021)

Petitioner's New Claim Construction

- Petitioner's new claim construction reads out the requirement that the graded concentration "aid carrier movement from" the active region (or surface) to the substrate.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

Petitioner's New and Incorrect Claim Construction

"graded dopant concentration" → Electric field → "any given electric field will aid electron movement"

Correct Claim Construction

"graded dopant concentration" → Electric field → "aid carrier movement" from active region (or surface) to substrate

-01242: PO Sur-Reply [65] at 2-5

Petitioner's New Claim Construction

- Petitioner knew the specification mentions specific slopes, and the prosecution history reiterates that carrier movement depends on the slope.

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/cm^3$, whereas the base region is 10^{14} to $10^{16}/cm^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction (1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift

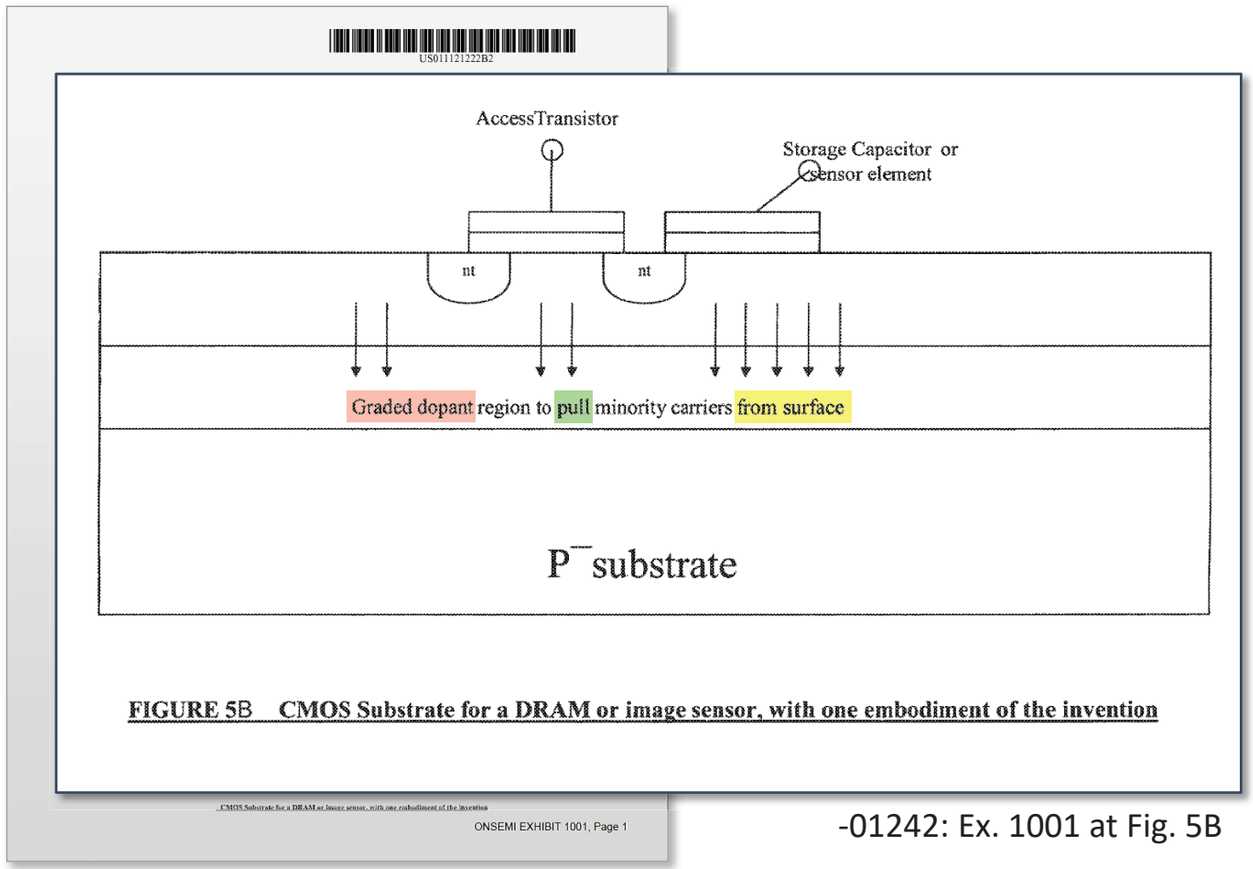
-01242: Ex. 1001 ('222 pat.) at 2:54-64

by drift due to the existence of this electric field."). Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept "down" (from the surface layer to the substrate) or "up" (from the substrate to the surface layer). *See* Applicant's Figs. 5(b) and 5(c).

'195 Applicant Remarks (4/17/2012)
-01242: Ex. 1016 at 289

Petitioner's New Claim Construction

- Petitioner knew the specification mentions "pulling" carriers, and Dr. Blalock understood "aid carrier movement" to mean "sweeping" carriers.



-01242: Ex. 1001 at Fig. 5B

not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n^-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n^-layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^-well and p^-wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in

-01242: Ex. 1001 ('222 pat.) at 3:52-66

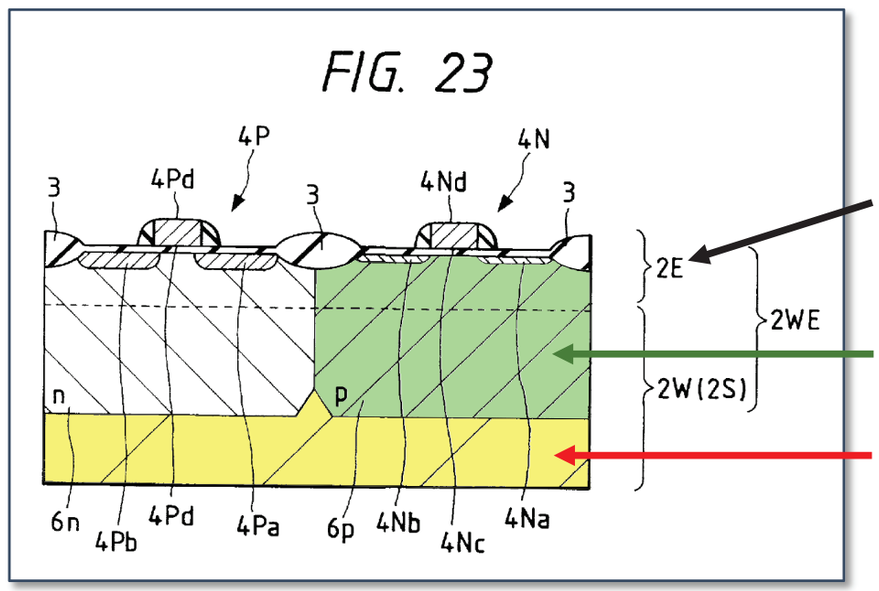
Petitioner's New Claim Construction

- Petitioner's new claim construction cannot save Kawagoe, when the electrons never enter the p-well.

Incidentally, in the present embodiment 4, the aforementioned p-well **6***p* and n-well **6***n* are formed to extend from the surface of the epitaxial layer **2**E to the upper portion of the semiconductor substrate body **2**S, as shown in FIGS. **16** and **17**, and the p-well **6***p* and n-well **6***n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer **2**E. Thus, the impurity concentration of the p-well **6***p* is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer **2**E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body **2**S by that concentration gradient and prevented from entering the p-well **6***p* so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well **6***p*. The impurity

ONSEMI EXHIBIT 1007, Page 1

-01242: Ex. 1007 at 15:62-16:11



active region/ surface

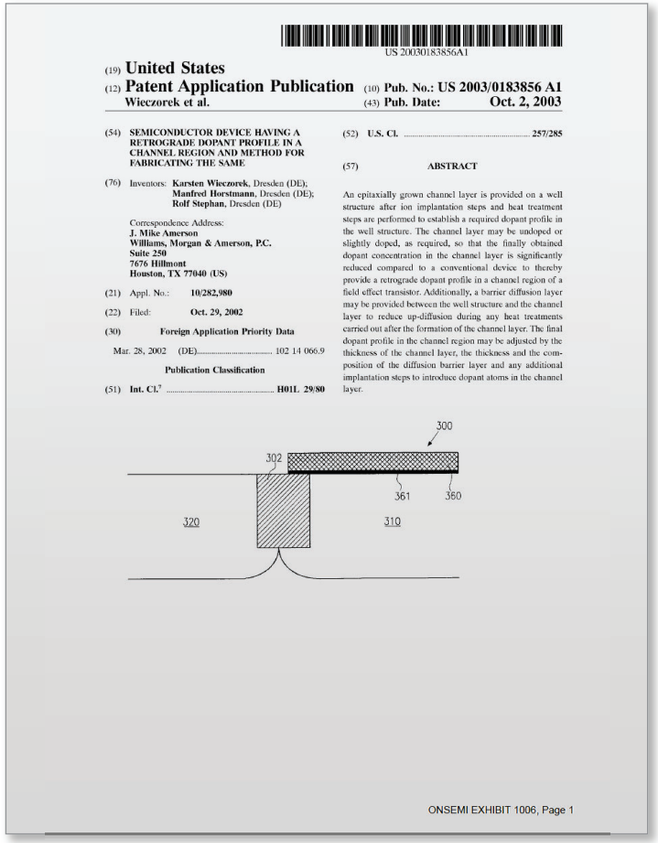
p-well

electrons do not enter p-well

-012242: Ex. 1007 (Kawagoe) at Fig. 23

Petitioner's New Claim Construction

- Petitioner's new claim construction cannot save Wieczorek, when there is absolutely no mention of carriers, much less moving carriers from the surface to the substrate.



US 20030183856A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2003/0183856 A1**

Wieczorek et al. (43) **Pub. Date: Oct. 2, 2003**

(54) **SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME**

(76) Inventors: **Karsten Wieczorek**, Dresden (DE); **Manfred Horstmann**, Dresden (DE); **Rolf Stephan**, Dresden (DE)

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(21) Appl. No.: **10/282,980**

(22) Filed: **Oct. 29, 2002**

(30) **Foreign Application Priority Data**

Mar. 28, 2002 (DE)..... 102 14 066.9

Publication Classification

(51) **Int. Cl.**[7] **H01L 29/80**

(52) **U.S. Cl.** **257/285**

(57) **ABSTRACT**

An epitaxially grown channel layer is provided on a well structure after ion implantation steps and heat treatment steps are performed to establish a required dopant profile in the well structure. The channel layer may be undoped or slightly doped, as required, so that the finally obtained dopant concentration in the channel layer is significantly reduced compared to a conventional device to thereby provide a retrograde dopant profile in a channel region of a field effect transistor. Additionally, a barrier diffusion layer may be provided between the well structure and the channel layer to reduce up-diffusion during any heat treatments carried out after the formation of the channel layer. The final dopant profile in the channel region may be adjusted by the thickness of the channel layer, the thickness and the composition of the diffusion barrier layer and any additional implantation steps to introduce dopant atoms in the channel layer.

ONSEMI EXHIBIT 1006, Page 1

[0009] **FIG. 2***a* is a graph, in which the dopant concentration of the N-well structure **120** and the P-well structure **110** is depicted with respect to the depth in the respective well structures. In particular, it is evident from **FIG. 2***a* that the V_T implantation (**114**, **124**), indicated by the same reference number as the respective implantation portions, leads to a dopant concentration that significantly decreases at the vicinity of the surface of the semiconductor device **100**. That is, the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile in the N-well structure **120** and the P-well structure **110** near the surface of the semiconductor device **100**, where, after completion of the device, a channel will form during operation of the device.

-01242: Ex. 1006 at [0009]

[0011] **FIG. 2***b* shows a corresponding graph with a typical dopant profile with respect to the depth of the respective well structure. Due to the up-diffusion of the dopant atoms during the heat treatment, the initially retrograde profile in the vicinity of the surface of the semiconductor device **100**, as indicated by reference number **200**, may have become substantially uniformly distributed.

-01242: Ex. 1006 at [0011]

[0013] Typically, the N-channel transistor **130** and the P-channel transistor **140** are formed by the following processes. After the heat treatment, the gate insulation layer **135** is formed, wherein the gate insulation layer may be deposited by chemical vapor deposition (CVD), or, if an oxide layer is used, a rapid thermal furnace process or a conventional furnace oxidation process may be used. Since, commonly, elevated temperatures are involved in fabricating the gate insulation layer **135**, this process also contributes to a further diffusion of the dopants within the P-well structure **110** and the N-well structure **120**. Thereafter, polysilicon is deposited and patterned by sophisticated photolithography techniques to form the gate electrodes **134** and **144**. With a first implantation, the extensions **132** and **142** are defined, and, subsequently, the spacer elements **133**, **143** are formed and serve as an implantation mask during a subsequent implantation process for defining the source and drain regions **131**, **141**. Since a further heat treatment is necessary to activate the dopants within the regions **131**, **132** and **141**, **142** and to cure any crystal damage caused by the preceding implantation steps, the initial dopant concentration, as shown in **FIG. 2***a*, will be even more strongly affected so that, after the plurality of heat treatments, the actual dopant concentration will be represented by the graph shown in **FIG. 2***b*. In particular, it is thus very difficult to obtain or to maintain a retrograde dopant profile in the channel regions **136** and **146**, which would be desirable to achieve an improved carrier mobility therein.

-01242: Ex. 1006 (Wieczorek) at [0013]

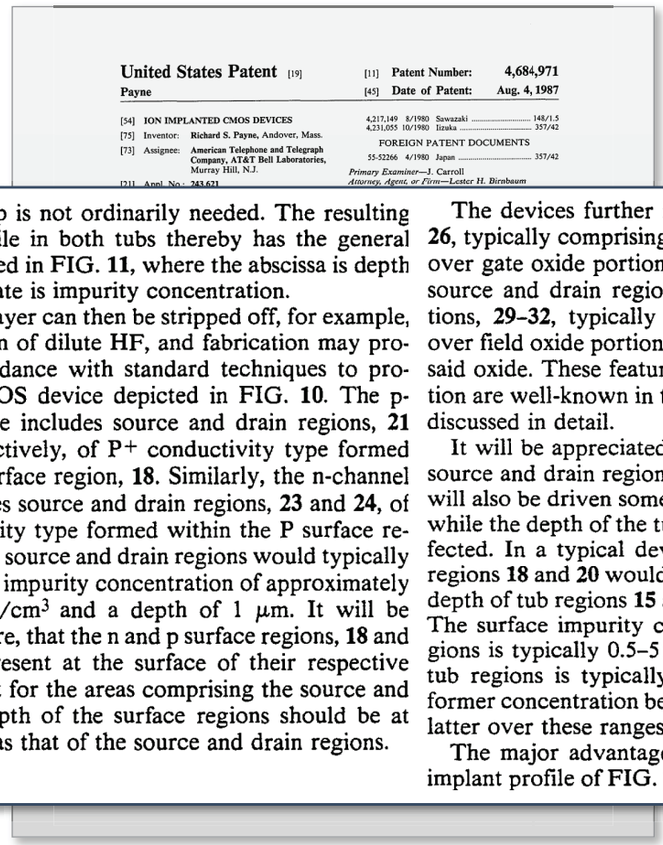
Petitioner's New Claim Construction

- Petitioner's new claim construction cannot save Payne, when there is absolutely no mention of carriers, much less moving carriers from the surface to the substrate.

Next, as shown in FIG. **8**, a thick oxide portion **19** is formed over the previously implanted regions **18** and **15** utilizing the nitride layer, **12**, as a mask. The thickness of this portion should be sufficient to block the subsequent ion implantation to be described. In this example, the layer is approximately 4000 Angstroms thick, but in general would fall within the range 3000–4500 Angstroms. The portion is formed by heating in wet O_2 at a temperature of approximately 1000 degrees Celsius for 1 hour. Any means of growing the requisite thickness of SiO_2 masked by the Si_3N_4 is suitable. Typically, heating in wet O_2 at 900–1050 degrees Celsius for 1–4 hours will be useful.

It should be appreciated that in the formation of the oxide a portion of the semiconductor surface will be consumed. The N region **18** will diffuse ahead of the growing oxide and so will remain at the new surface. For purposes of illustration, the semiconductor surface is shown as flat, although, as a result of oxidation, there will be an indentation in the area of the N tub.

-01244: Ex. 1005 (Payne) at 4:38-59



United States Patent [19]
Payne

[11] Patent Number: 4,684,971
[45] Date of Patent: Aug. 4, 1987

[54] ION IMPLANTED CMOS DEVICES
[75] Inventor: Richard S. Payne, Andover, Mass.
[73] Assignee: American Telephone and Telegraph Company, AT&T Bell Laboratories, Murray Hill, N.J.

4,217,149 8/1980 Sawazaki 148/1.5
4,231,055 10/1980 Iizuka 357/42

FOREIGN PATENT DOCUMENTS
55-52266 4/1980 Japan 357/42

Primary Examiner—J. Carroll
Attorney, Agent, or Firm—Lester H. Birnbaum

a separate step is not ordinarily needed. The resulting impurity profile in both tubs thereby has the general shape illustrated in FIG. **11**, where the abscissa is depth and the ordinate is impurity concentration.

The oxide layer can then be stripped off, for example, with a solution of dilute HF, and fabrication may proceed in accordance with standard techniques to produce the CMOS device depicted in FIG. **10**. The p-channel device includes source and drain regions, **21** and **22**, respectively, of P^+ conductivity type formed with the N surface region, **18**. Similarly, the n-channel device includes source and drain regions, **23** and **24**, of N^+ conductivity type formed within the P surface region **20**. These source and drain regions would typically have a surface impurity concentration of approximately 10^{19}–10^{20} ions/cm^3 and a depth of 1 μm. It will be noted, therefore, that the n and p surface regions, **18** and **20**, will be present at the surface of their respective devices except for the areas comprising the source and drain. The depth of the surface regions should be at least as great as that of the source and drain regions.

The devices further include gate electrodes, **25** and **26**, typically comprising polycrystalline silicon, formed over gate oxide portions **27** and **28**. Ohmic contacts to source and drain regions are provided by metal portions, **29–32**, typically comprising aluminum, formed over field oxide portions **33–35** and contact windows in said oxide. These features and their method of fabrication are well-known in the art and consequently are not discussed in detail.

It will be appreciated that during the drive-in of the source and drain regions, **21–24**, the regions **18**, and **20** will also be driven somewhat further into the substrate, while the depth of the tubs **15** and **17** is essentially unaffected. In a typical device, the final depth of surface regions **18** and **20** would be approximately 1–2μ and the depth of tub regions **15** and **17** would be typically 3–8μ. The surface impurity concentration of the surface regions is typically $0.5–5\times10^{16}$ ions/cm^3 and that of the tub regions is typically 10^{15}–10^{16} ions/cm^3, with the former concentration being at least twice as much as the latter over these ranges.

The major advantage in formation of the high-low implant profile of FIG. **11** is illustrated in FIGS. **12** and

Ex. 1005 at 5:14-57

device. In a device fabricated in accordance with the present invention, as illustrated in FIG. **13**, the composite profiles remain high and then fall off rapidly at a much closer distance from the boundary. This is due to the high impurity concentration of surface regions **18** and **20** as well as the short diffusion lengths of these regions. On each side of the boundary, therefore, the high impurity concentration of the surface region (e.g., **18**) is compensated for only by the low concentration tub region of the adjacent device (**17**) and substantial overlap is permitted. In a typical device, it is expected

-01244: Ex. 1005 at 6:7-17

Summary

- **“Aid carrier movement”**
  - **“Graded dopant concentration” does not necessarily “aid carrier movement.”**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- Petitioner cannot rely on inherency for “aid carrier movement”
- Kawagoe’s “graded dopant concentration” and improper claim mapping
- Petitioner’s Wieczorek grounds fail
- Petitioner’s Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

All of the Grounds Fail

- All of the Grounds rely on Kawagoe, Wieczorek, or Payne.

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe
II	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf
III	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe, Gupta
IV	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf, Gupta
V	§103	19, 37	Kawagoe, Silverbrook
VI	§103	19, 37	Wieczorek, Wolf, Silverbrook

-01242: Pet. [1] at 5

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-2, 4-10, 12-18	Kawagoe
II	§103	1-3, 5-11, 13-18	Wieczorek, Wolf
III	§103	1-2, 4-10, 12-18	Kawagoe, Gupta
IV	§103	1-3, 5-11, 13-18	Wieczorek, Wolf, Gupta

-01243: Pet. [1] at 5

Ground	Basis	Challenged Claim	Reference(s)
I	§ 103	44	Payne
II	§ 103	44	Sakai, Kawagoe

-01244: Pet. [1] at 5

-01242: PO Resp. [47] at 20-31; -01243: PO Resp. [46] at 21-3;
-01244: PO Resp. [46] at 19-27

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

No Evidence for Kawagoe

- There is no evidence that Kawagoe moves carriers from the active region (surface) to the substrate.

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe
II	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf
III	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe, Gupta
IV	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf, Gupta
V	§103	19, 37	Kawagoe, Silverbrook
VI	§103	19, 37	Wieczorek, Wolf, Silverbrook

-01242: Pet. [1] at 5

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-2, 4-10, 12-18	Kawagoe
II	§103	1-3, 5-11, 13-18	Wieczorek, Wolf
III	§103	1-2, 4-10, 12-18	Kawagoe, Gupta
IV	§103	1-3, 5-11, 13-18	Wieczorek, Wolf, Gupta

-01243: Pet. [1] at 5

Ground	Basis	Challenged Claim	Reference(s)
I	§ 103	44	Payne
II	§ 103	44	Sakai, Kawagoe

-01244: Pet. [1] at 5

-01242: PO Resp. [47] at 20-20; -01243: PO Resp. [46] at 21-29;
-01244: PO Resp. [46] at 19-23

No Evidence for Wieczorek

- There is no evidence that Wieczorek moves carriers from the active region (surface) to the substrate.

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe
II	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf
III	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe, Gupta
IV	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf, Gupta
V	§103	19, 37	Kawagoe, Silverbrook
VI	§103	19, 37	Wieczorek, Wolf, Silverbrook

-01242: Pet. [1] at 5

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-2, 4-10, 12-18	Kawagoe
II	§103	1-3, 5-11, 13-18	Wieczorek, Wolf
III	§103	1-2, 4-10, 12-18	Kawagoe, Gupta
IV	§103	1-3, 5-11, 13-18	Wieczorek, Wolf, Gupta

-01243: Pet. [1] at 5

Ground	Basis	Challenged Claim	Reference(s)
I	§ 103	44	Payne
II	§ 103	44	Sakai, Kawagoe

-01244: Pet. [1] at 5

No Evidence for Payne

- There is no evidence that Payne moves carriers from the active region (surface) to the substrate.

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe
II	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf
III	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe, Gupta
IV	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf, Gupta
V	§103	19, 37	Kawagoe, Silverbrook
VI	§103	19, 37	Wieczorek, Wolf, Silverbrook

-01242: Pet. [1] at 5

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IV	§103	1-3, 5-11, 13-18	Wieczorek, Wolf, Gupta

-01243: Pet. [1] at 5

Ground	Basis	Challenged Claim	Reference(s)
I	§ 103	44	Payne
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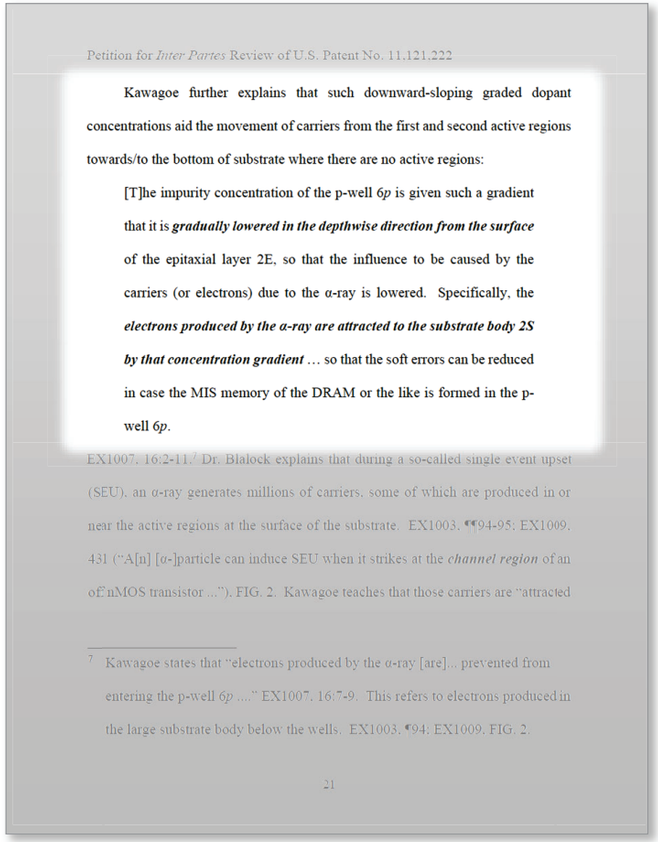
-01244: Pet. [1] at 5

Summary

- **"Aid carrier movement"**
  - **"Graded dopant concentration" does not necessarily "aid carrier movement."**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- **Petitioner cannot rely on inherency for "aid carrier movement"**
  - **Petition never mentions inherency**
  - **There is no evidence carriers necessarily move from the surface to the substrate**
- Petitioner's Kawagoe grounds fail
- Petitioner's Wieczorek grounds fail
- Petitioner's Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

Petition Never Mentions Inherency

- Petitioner never argued "inherency" for Kawagoe.



Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222

Kawagoe further explains that such downward-sloping graded dopant concentrations aid the movement of carriers from the first and second active regions towards/to the bottom of substrate where there are no active regions:

> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction from the surface*** of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** … so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

EX1007, 16:2-11.[7] Dr. Blalock explains that during a so-called single event upset (SEU), an α-ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate. EX1003, ¶¶94-95; EX1009, 431 ("A[n] [α-]particle can induce SEU when it strikes at the *channel region* of an of nMOS transistor ..."). FIG. 2. Kawagoe teaches that those carriers are "attracted

[7] Kawagoe states that "electrons produced by the α-ray [are]... prevented from entering the p-well 6*p* ...." EX1007, 16:7-9. This refers to electrons produced in the large substrate body below the wells. EX1003, ¶94; EX1009, FIG. 2.

21

Kawagoe further explains that such downward-sloping graded dopant concentrations aid the movement of carriers from the first and second active regions towards/to the bottom of substrate where there are no active regions:

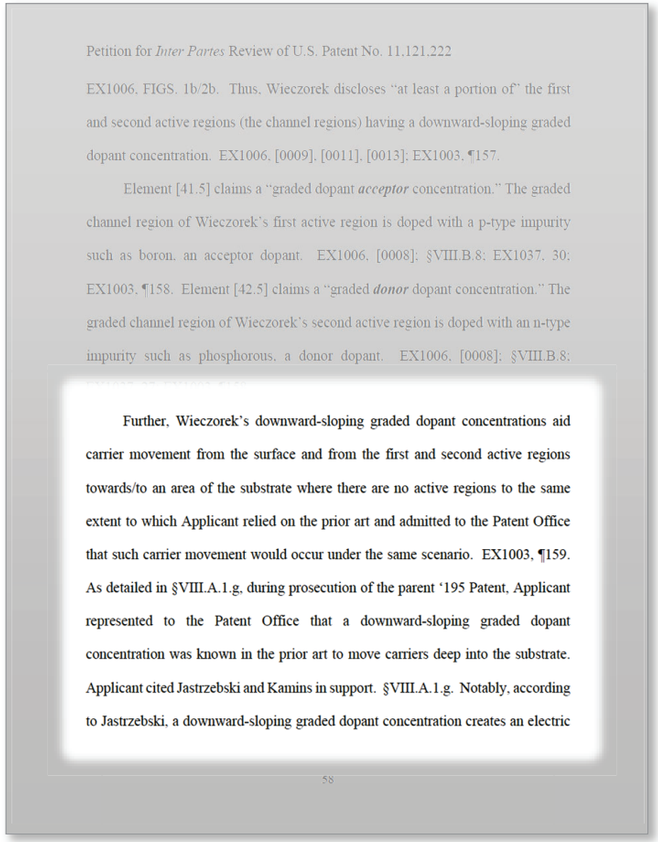
> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction from the surface*** of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** … so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

EX1007, 16:2-11.[7] Dr. Blalock explains that during a so-called single event upset

-01242: Pet. [1] at 21

Petition Never Mentions Inherency

- Petitioner never argued "inherency" for Wieczorek.



Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222

EX1006, FIGS. 1b/2b. Thus, Wieczorek discloses "at least a portion of" the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. EX1006, [0009], [0011], [0013]; EX1003, ¶157.

Element [41.5] claims a "graded dopant ***acceptor*** concentration." The graded channel region of Wieczorek's first active region is doped with a p-type impurity such as boron, an acceptor dopant. EX1006, [0008]; §VIII.B.8; EX1037, 30; EX1003, ¶158. Element [42.5] claims a "graded ***donor*** dopant concentration." The graded channel region of Wieczorek's second active region is doped with an n-type impurity such as phosphorous, a donor dopant. EX1006, [0008]; §VIII.B.8;

Further, Wieczorek's downward-sloping graded dopant concentrations aid carrier movement from the surface and from the first and second active regions towards/to an area of the substrate where there are no active regions to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. EX1003, ¶159. As detailed in §VIII.A.1.g, during prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded dopant concentration was known in the prior art to move carriers deep into the substrate. Applicant cited Jastrzebski and Kamins in support. §VIII.A.1.g. Notably, according to Jastrzebski, a downward-sloping graded dopant concentration creates an electric

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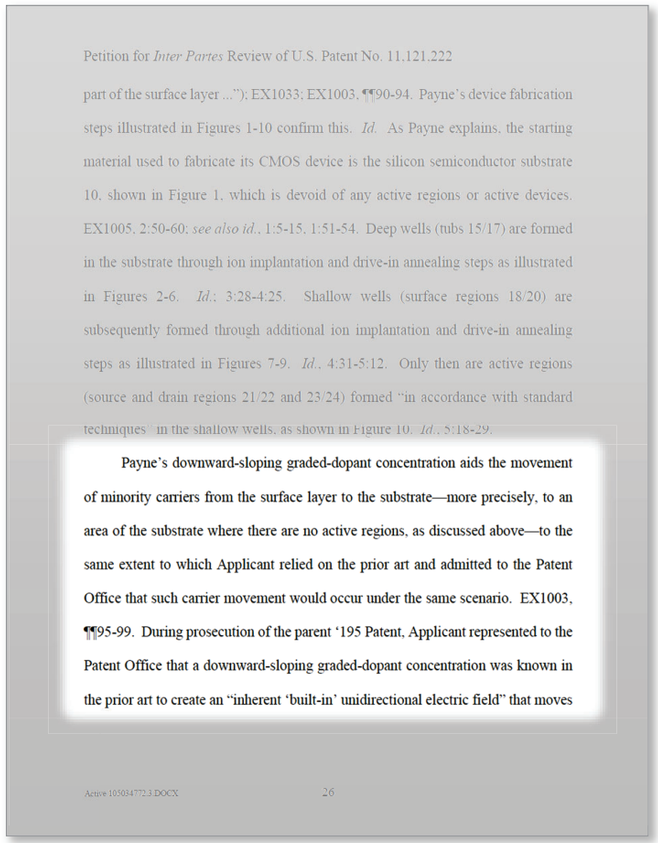
Further, Wieczorek's downward-sloping graded dopant concentrations aid carrier movement from the surface and from the first and second active regions towards/to an area of the substrate where there are no active regions to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. EX1003, ¶159. As detailed in §VIII.A.1.g, during prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded dopant concentration was known in the prior art to move carriers deep into the substrate. Applicant cited Jastrzebski and Kamins in support. §VIII.A.1.g. Notably, according to Jastrzebski, a downward-sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers ... ***deep into the substrate***[.]" EX1010, 2:27-32, 5:14-22.

-01242: Pet. [1] at 58-59

-01242: PO Resp. [47] at 29-31; PO Sur-Reply [65] at 14-15

Petition Never Mentions Inherency

- Petitioner never argued "inherency" for Payne.



Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222

part of the surface layer ..."); EX1033; EX1003, ¶¶90-94. Payne's device fabrication steps illustrated in Figures 1-10 confirm this. *Id.* As Payne explains, the starting material used to fabricate its CMOS device is the silicon semiconductor substrate 10, shown in Figure 1, which is devoid of any active regions or active devices. EX1005, 2:50-60; *see also id.*, 1:5-15, 1:51-54. Deep wells (tubs 15/17) are formed in the substrate through ion implantation and drive-in annealing steps as illustrated in Figures 2-6. *Id.*, 3:28-4:25. Shallow wells (surface regions 18/20) are subsequently formed through additional ion implantation and drive-in annealing steps as illustrated in Figures 7-9. *Id.*, 4:31-5:12. Only then are active regions (source and drain regions 21/22 and 23/24) formed "in accordance with standard techniques" in the shallow wells, as shown in Figure 10. *Id.*, 5:18-29.

Payne's downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate—more precisely, to an area of the substrate where there are no active regions, as discussed above—to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. EX1003, ¶¶95-99. During prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded-dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that moves

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Payne's downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate—more precisely, to an area of the substrate where there are no active regions, as discussed above—to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. EX1003, ¶¶95-99. During prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded-dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that moves carriers deep into the substrate (while an upward-sloping concentration, not at issue in Payne, would move those carriers in the opposite direction towards the surface):

> [T]he graded dopant concentration itself creates a ***'built-in' electrical field*** that forces the movement of carriers into a particular direction, whereby ***the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***

EX1020, 289-290 (underlining in original); EX1003, ¶¶95-99. Applicant further

-01244: Pet. [1] at 26-27

-01244: PO Resp. [46] at 13, 23-24; PO Sur-Reply [64] at 11

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Petition Never Mentions Inherency

"[T]he petitioner's petition … is supposed to guide the life of the litigation."

SAS Inst. v. Iancu, 584 U.S. 357, 366, 138 S.Ct. 1348, 1356 (2018)

"Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case of unpatentability."

U.S. Patent Trial and Appeal Board, Consolidated Trial Practice Guide 73 (Nov. 2019)

Summary

- **"Aid carrier movement"**
  - **"Graded dopant concentration" does not necessarily "aid carrier movement."**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- **Petitioner cannot rely on inherency for "aid carrier movement"**
  - **Petition never mentions inherency**
  - **There is no evidence carriers necessarily move from the surface to the substrate**
- Petitioner's Kawagoe grounds fail
- Petitioner's Wieczorek grounds fail
- Petitioner's Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

Petitioner Cannot Rely on Inherency



"[T]he Board's analysis rests upon the very kind of ***probability or possibility*** … that this court has pointed out ***is insufficient*** to establish inherency."

In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999)

"[A]nticipation by inherent disclosure is appropriate only when the reference discloses prior art that ***must necessarily include the unstated limitation***."

Transclean Corp. v. Bridgewood Servs., Inc., 290 F.3d 1364, 1373 (Fed. Cir. 2002)

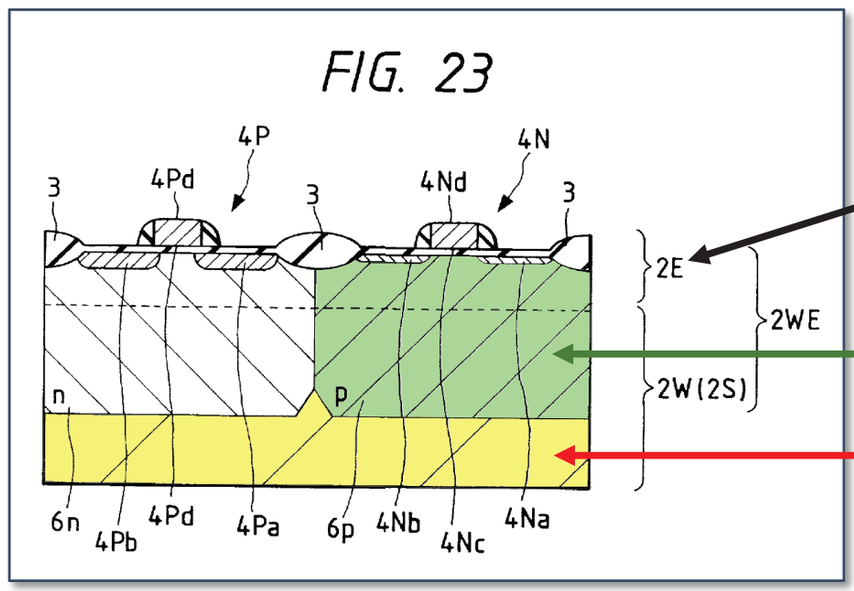
Petitioner Cannot Rely on Inherency

- In Kawagoe, the electrons do <u>not</u> enter the p-well.
- So the electrons do <u>not</u> necessarily move from the active region (or surface) to the substrate.

Incidentally, in the present embodiment 4, the aforementioned p-well **6***p* and n-well **6***n* are formed to extend from the surface of the epitaxial layer **2**E to the upper portion of the semiconductor substrate body **2**S, as shown in FIGS. **16** and **17**, and the p-well **6***p* and n-well **6***n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer **2**E. Thus, the impurity concentration of the p-well **6***p* is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer **2**E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body **2**S by that concentration gradient and prevented from entering the p-well **6***p* so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well **6***p*. The impurity

ONSEMI EXHIBIT 1007, Page 1

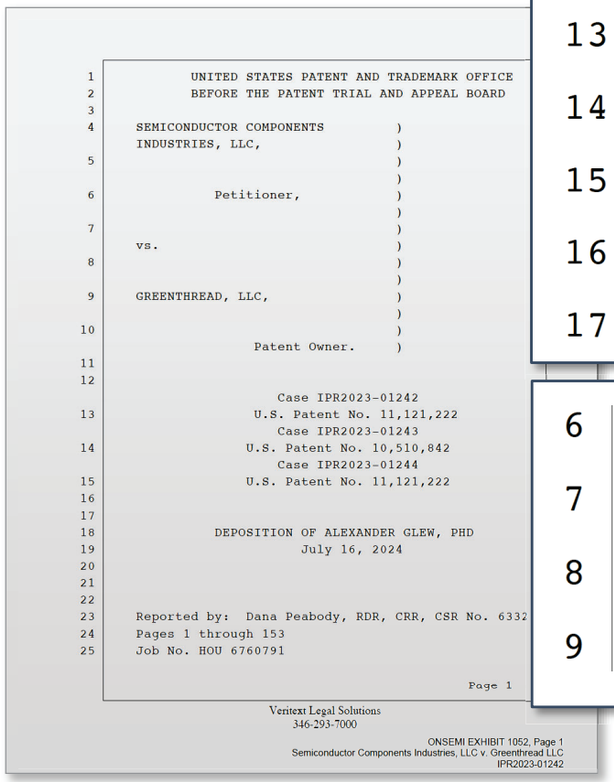
-01242: Ex. 1007 at 15:62-16:11



-01242: Ex. 1007 (Kawagoe) at Fig. 23

Petitioner Cannot Rely on Inherency

- Dr. Glew confirmed that electrons in Kawagoe do not necessarily move from the active region (or surface) to substrate.



UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,

Petitioner,

vs.

GREENTHREAD, LLC,

Patent Owner.

Case IPR2023-01242
U.S. Patent No. 11,121,222
Case IPR2023-01243
U.S. Patent No. 10,510,842
Case IPR2023-01244
U.S. Patent No. 11,121,222

DEPOSITION OF ALEXANDER GLEW, PHD
July 16, 2024

Reported by: Dana Peabody, RDR, CRR, CSR No. 6332
Pages 1 through 153
Job No. HOU 6760791

Page 1

Veritext Legal Solutions
346-293-7000

ONSEMI EXHIBIT 1052, Page 1
Semiconductor Components Industries, LLC v. Greenthread LLC
IPR2023-01242

Q. And this electric field resulting from the graded dopant concentration of Figure 17 would sweep those electrons from the active region down into the substrate?

MR. WHITEHURST: Object to the form.

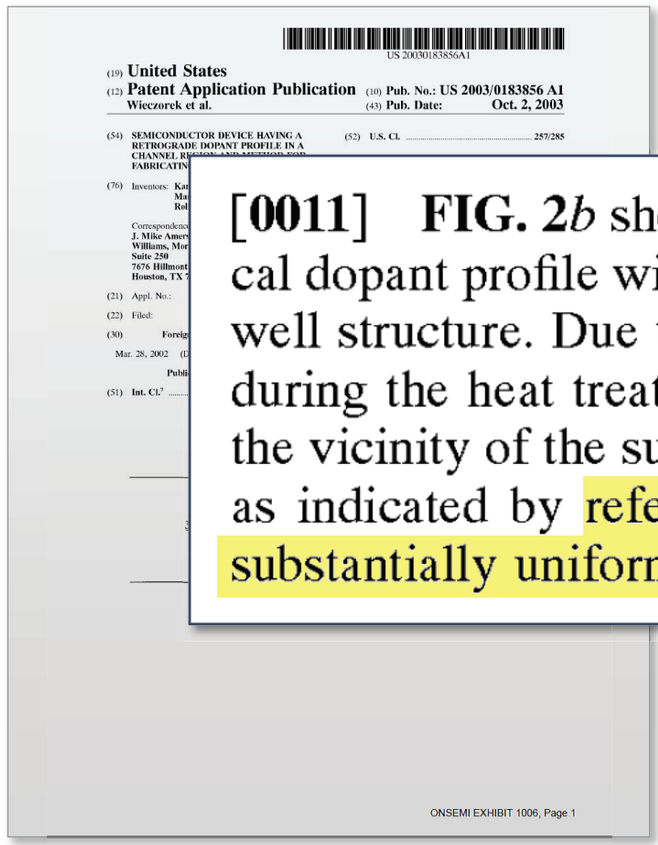
THE WITNESS: It doesn't disclose that it does that.

The patent only describes that this dopant gradient is able to keep SEU electrons out of the well. It doesn't tell you what's happening in the well.

-01242: Ex. 1052 (Glew Dep. Tr.) at 121:11-17; 122:6-9

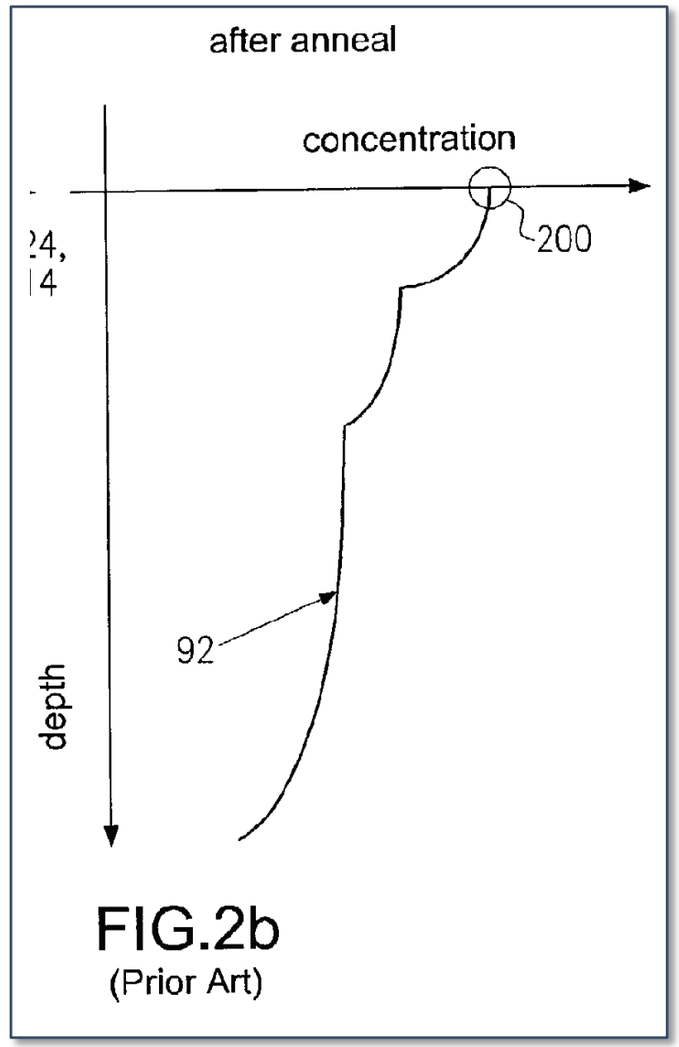
Petitioner Cannot Rely on Inherency

- In Wieczorek, the carriers do <u>not</u> necessarily move.
- The gradient concentration may be <u>uniform</u>.



[0011] **FIG. 2*b*** shows a corresponding graph with a typical dopant profile with respect to the depth of the respective well structure. Due to the up-diffusion of the dopant atoms during the heat treatment, the initially retrograde profile in the vicinity of the surface of the semiconductor device **100**, as indicated by reference number **200**, may have become substantially uniformly distributed.

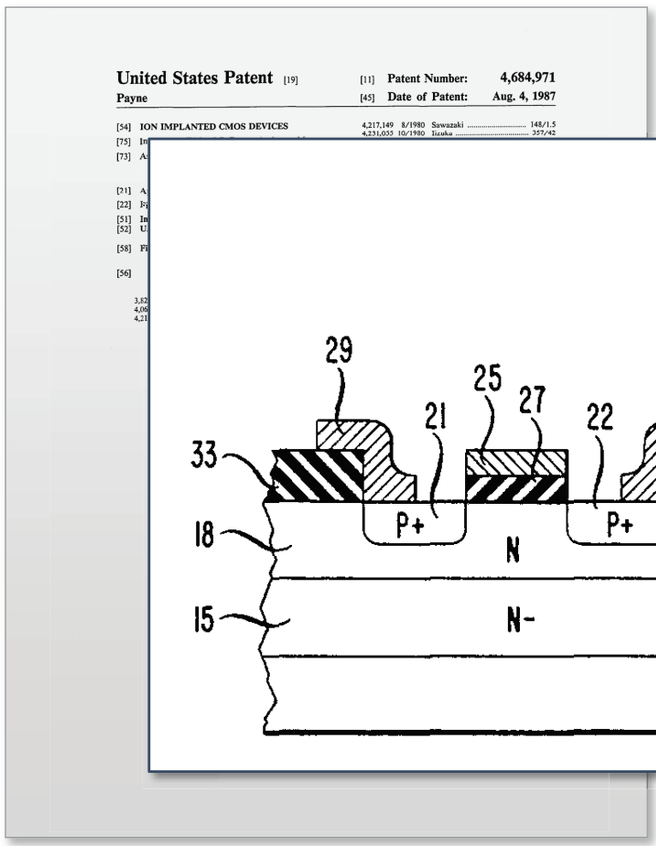
-01242: Ex. 1006 (Wieczorek) at [0011]



-01242: Ex. 1006 at Fig. 2b

Petitioner Cannot Rely on Inherency

- In Payne, the carriers do not necessarily move.

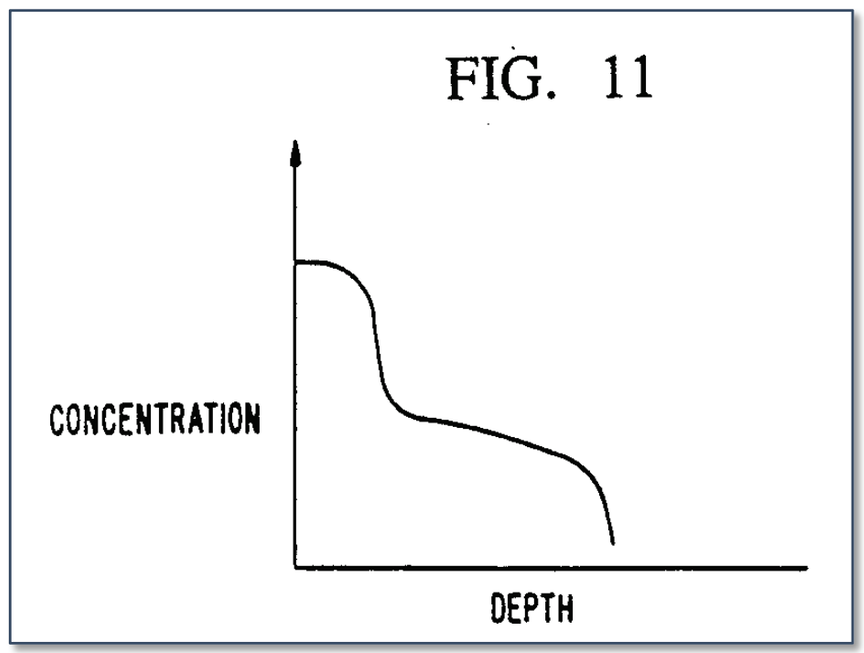

United States Patent [19]
Payne

[11] Patent Number: 4,684,971
[45] Date of Patent: Aug. 4, 1987

[54] ION IMPLANTED CMOS DEVICES

4,217,149 8/1980 Sawazaki 148/1.5
4,231,055 10/1980 Izuka 357/42

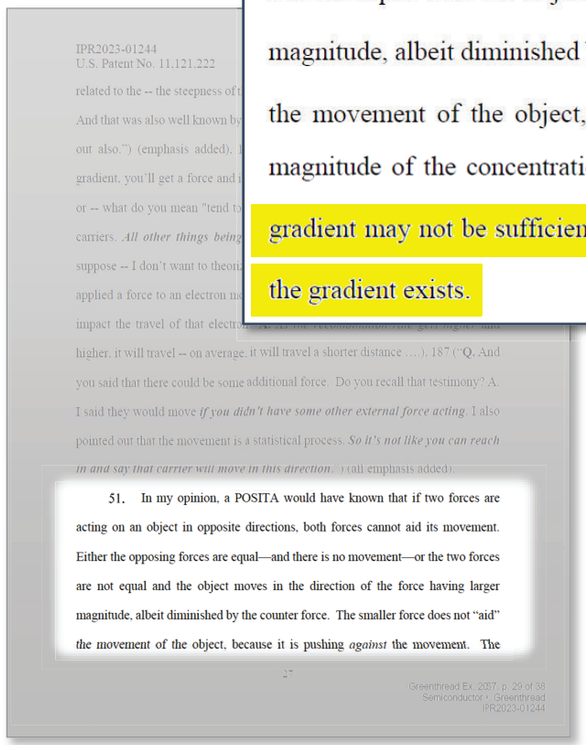
-01244: Ex. 1005 (Payne) at Fig. 10



-01244: Ex. 1005 at Fig. 11

Dr. Glew Testimony

- An electric field does <u>not</u> necessarily move carriers.


IPR2023-01244
U.S. Patent No. 11,121,222

related to the -- the steepness of t

And that was also well known by

out also.") (emphasis added).

gradient, you'll get a force and

or -- what do you mean "tend to

carriers. *All other things being*

suppose -- I don't want to theori

applied a force to an electron n

impact the travel of that electr

higher, it will travel -- on average, it will travel a shorter distance ….). 187 ("Q. And

you said that there could be some additional force. Do you recall that testimony? A.

I said they would move *if you didn't have some other external force acting*. I also

pointed out that the movement is a statistical process. *So it's not like you can reach*

in and say that carrier will move in this direction….") (all emphasis added).

51. In my opinion, a POSITA would have known that if two forces are acting on an object in opposite directions, both forces cannot aid its movement. Either the opposing forces are equal—and there is no movement—or the two forces are not equal and the object moves in the direction of the force having larger magnitude, albeit diminished by the counter force. The smaller force does not "aid" the movement of the object, because it is pushing *against* the movement. The

27

Greenthread Ex. 2057, p. 29 of 38
Semiconductor v. Greenthread
IPR2023-01244

51. In my opinion, a POSITA would have known that if two forces are acting on an object in opposite directions, both forces cannot aid its movement. Either the opposing forces are equal—and there is no movement—or the two forces are not equal and the object moves in the direction of the force having larger magnitude, albeit diminished by the counter force. The smaller force does not "aid" the movement of the object, because it is pushing *against* the movement. The magnitude of the concentration gradient plays a substantial role, because a small gradient may not be sufficient to overcome the resistance of the material in which the gradient exists.

-01242: Ex. 2057 (Glew Decl.) at ¶51-52

52. I see that in response to the question "have you looked at any aspect of the gradient other than its being downward sloping?" Dr. Blalock replied: "As I've said, the patent owner tells us that that's sufficient, so ***[t]hat's what I did. I have not done calculations of the slope per se***." Ex. 2058, 195 (emphasis added). And in response to the question: "Do you need to know the magnitude of the force on carriers to know if their movement is being aided?" Dr. Blalock said: "Well, the patent owner -- the patent hasn't given us a threshold for aiding. … *when I look at the prior art, when I find a concentration gradient*, … *if there was a gradient, then it was producing that force and aiding the movement*." Ex. 2058, 91-92 (emphasis added). Since the mere direction of the gradient is *not* sufficient to determine whether there is a "net force"—the premise of Dr. Blalock's analysis is incorrect. Therefore, I disagree with his conclusion about the "aid carrier movement…" feature being taught in the prior art (apparently by Kawagoe, though Dr. Blalock's declaration does not clearly say that Kawagoe inherently teaches the "aid carrier movement…" feature). As I explained above, since Kawagoe teaches inhibiting carrier movement, it does not teach aiding carrier movement. The SEU event is described as creating electrons, which are the minority carriers in a p-well, but not in an n-well. Kawagoe is not relevant for an n-well.

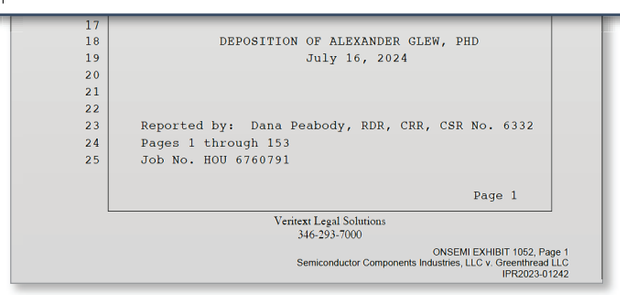
Dr. Glew Testimony

- An electric field does not necessarily move carriers.

Q. Is that what's creating the downward force we talked about in Figure 5B?

A. That's part of it. Mainly, what we talk about, there is a diffusion, diffusional force too. But, you know, if you think of a drop of ink in a pool, you put it a corner, it doesn't stay there. It will eventually diffuse out.

If I had a pile of electrons or holes in one area, and I didn't have them -- I had a dearth next to it, then there's a little bit of diffusional driving force to get them to move. Usually they don't move, really, on their own without some other



DEPOSITION OF ALEXANDER GLEW, PHD
July 16, 2024

Reported by: Dana Peabody, RDR, CRR, CSR No. 6332
Pages 1 through 153
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Veritext Legal Solutions
346-293-7000

ONSEMI EXHIBIT 1052, Page 1
Semiconductor Components Industries, LLC v. Greenthread LLC
IPR2023-01242

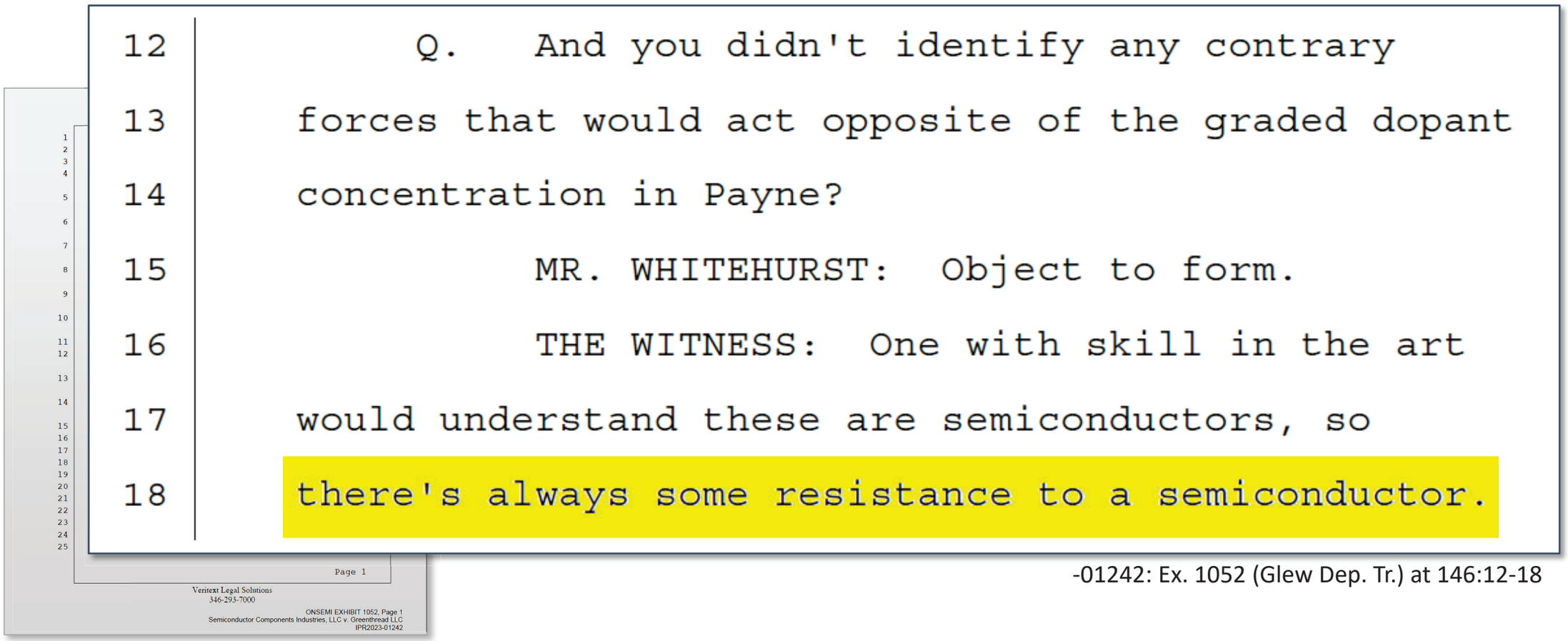
force, like a little bit of a temperature to activate or a little bit of voltage, but there is a diffusional force also.

There's other -- there's other forces that cause things to happen that we're not discussing here: Stress, energy. Any form of energy can cause things to happen, potentially.

-01242: Ex. 1052 (Glew Dep. Tr.) at 87:14-88:7

Dr. Glew Testimony

- An electric field does not necessarily overcome the resistance of the semiconductor.



Q. And you didn't identify any contrary forces that would act opposite of the graded dopant concentration in Payne?

MR. WHITEHURST: Object to form.

THE WITNESS: One with skill in the art would understand these are semiconductors, so there's always some resistance to a semiconductor.

Page 1

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346-293-7000

ONSEMI EXHIBIT 1052, Page 1
Semiconductor Components Industries, LLC v. Greenthread LLC
IPR2023-01242

-01242: Ex. 1052 (Glew Dep. Tr.) at 146:12-18

Summary

- **"Aid carrier movement"**
  - **"Graded dopant concentration" does not necessarily "aid carrier movement."**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- **Petitioner cannot rely on inherency for "aid carrier movement"**
  - **Petition never mentions inherency**
  - **There is no evidence carriers necessarily move from the surface to the substrate**
- **Petitioner's Kawagoe grounds fail**
  - **Kawagoe does not aid carrier movement from active region (or surface) to substrate**
  - **Petition does not identify a "second doping type opposite in conductivity"**
- Petitioner's Wieczorek grounds fail
- Petitioner's Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

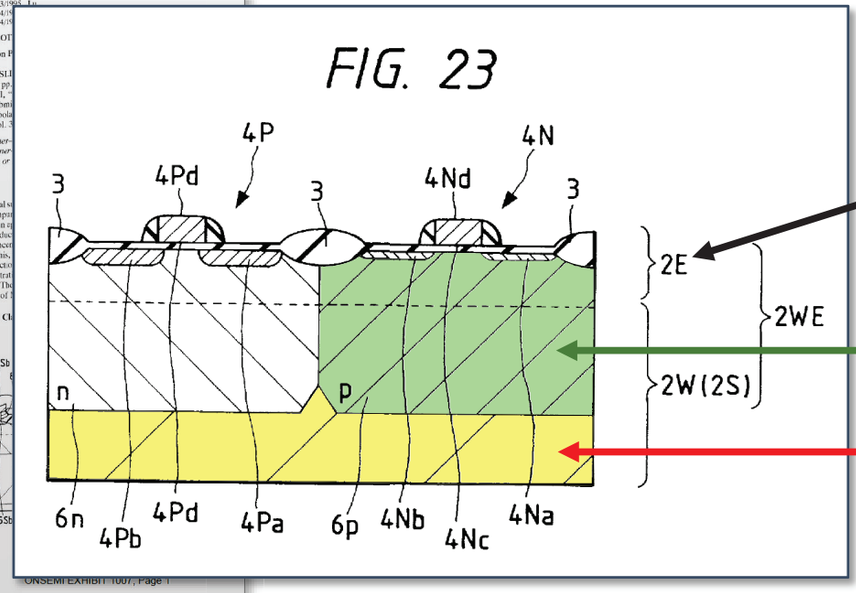
- Kawagoe does <u>not</u> aid movement, it <u>prevents</u> movement.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body **2S** by that concentration gradient and prevented from entering the p-well **6***p* so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well **6***p*. The impurity

Ex. 1007 at 15:62-16:11



active region/ surface

electrons do not enter p-well

electrons are here

-01242: Ex. 1007 (Kawagoe) at Fig. 23

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

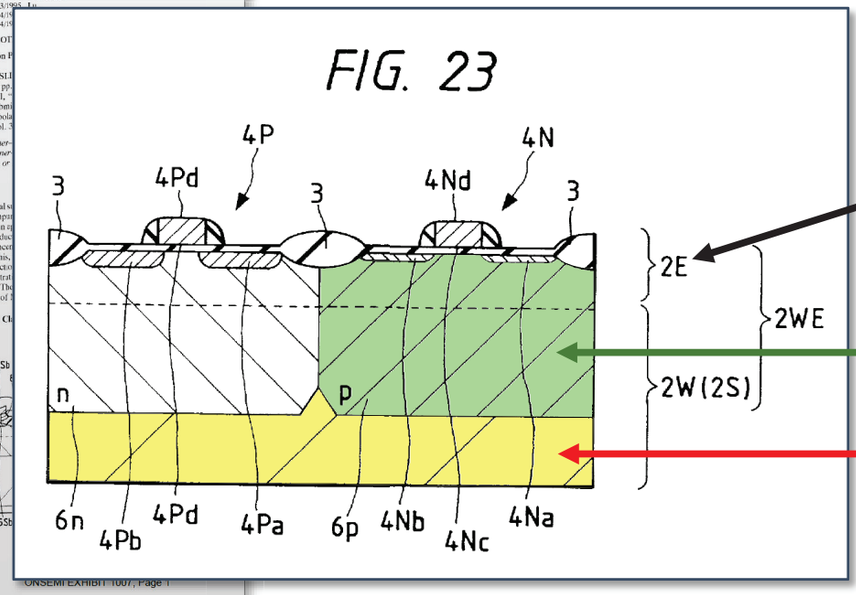
- Kawagoe does <u>not</u> aid movement from the active region to the substrate because the electrons do <u>not</u> enter the p-well.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body **2S** by that concentration gradient and prevented from entering the p-well **6***p* so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well **6***p*. The impurity

Ex. 1007 at 15:62-16:11



active region/ surface

electrons do not enter p-well

electrons are here

-01242: Ex. 1007 (Kawagoe) at Fig. 23

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Dr. Glew confirmed that Kawagoe does not move electrons from active region to substrate.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

11 Q. And this electric field resulting from the
12 graded dopant concentration of Figure 17 would sweep
13 those electrons from the active region down into the
14 substrate?
15 MR. WHITEHURST: Object to the form.
16 THE WITNESS: It doesn't disclose that it
17 does that.

-01242: Ex. 1052 at 121:11-17

6 The patent only describes that this dopant
7 gradient is able to keep SEU electrons out of the
8 well. It doesn't tell you what's happening in the
9 well.

-01242: Ex. 1052 (Glew Dep. Tr.) at 122:6-9

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Petition does <u>not</u> allege that Kawagoe moves electrons from active region to substrate.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

Kawagoe further explains that such downward-sloping graded dopant concentrations aid the movement of carriers from the first and second active regions towards/to the bottom of substrate where there are no active regions:

> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction from the surface*** of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** … so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

EX1007, 16:2-11.[7] Dr. Blalock explains that during a so-called single event upset (SEU), an α-ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate. EX1003, ¶¶94-95; EX1009, 431 ("A[n] [α-]particle can induce SEU when it strikes at the ***channel region*** of an off nMOS transistor ..."), FIG. 2. Kawagoe teaches that those carriers are "attracted to the substrate body by [the] concentration gradient" of the graded dopant concentration illustrated in Figure 17. EX1007, 16:2-11.

Wang

-01242: Pet. [1] at 21-22

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Petition does <u>not</u> allege that it would have been obvious to modify Kawagoe in view of Wang.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

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Wang

-01242: Pet. [1] at 21-22

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

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1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

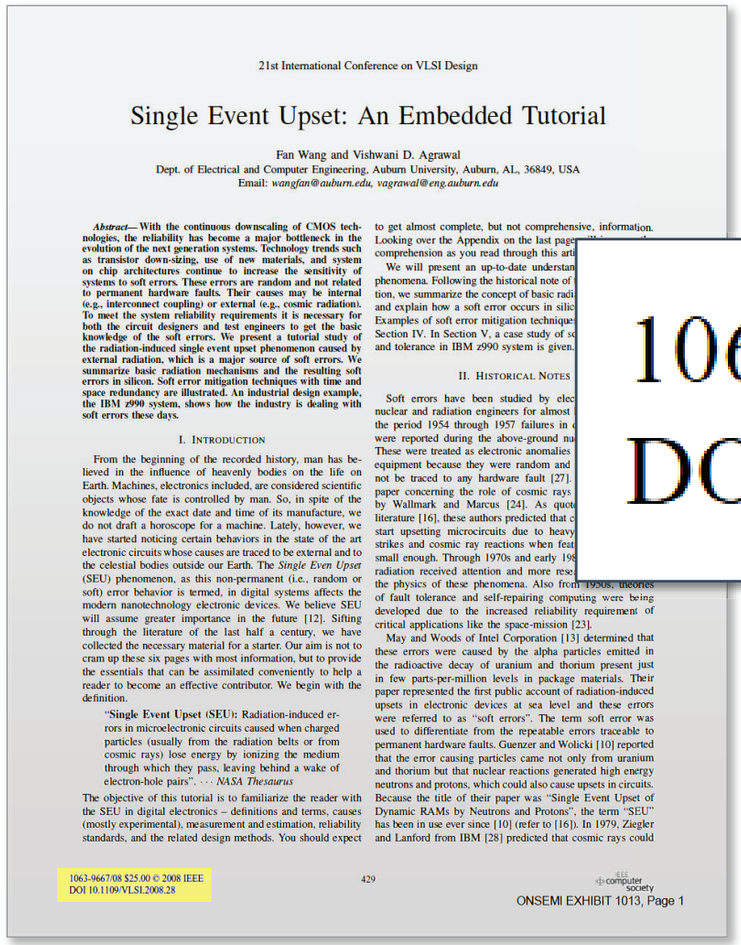
-01242: Ex. 1001 ('222 pat.) at 4:38-62

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe
II	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf
III	§103	1-9, 13-14, 16-21, 23-28, 32-42	Kawagoe, Gupta
IV	§103	1-2, 4-9, 13-23, 25-28, 32-42	Wieczorek, Wolf, Gupta
V	§103	19, 37	Kawagoe, Silverbrook
VI	§103	19, 37	Wieczorek, Wolf, Silverbrook

-01242: Pet. [1] at 5

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Wang is <u>not</u> even prior art.



21st International Conference on VLSI Design

Single Event Upset: An Embedded Tutorial

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***Abstract*— With the continuous downscaling of CMOS technologies, the reliability has become a major bottleneck in the evolution of the next generation systems. Technology trends such as transistor down-sizing, use of new materials, and system on chip architectures continue to increase the sensitivity of systems to soft errors. These errors are random and not related to permanent hardware faults. Their causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation). To meet the system reliability requirements it is necessary for both the circuit designers and test engineers to get the basic knowledge of the soft errors. We present a tutorial study of the radiation-induced single event upset phenomenon caused by external radiation, which is a major source of soft errors. We summarize basic radiation mechanisms and the resulting soft errors in silicon. Soft error mitigation techniques with time and space redundancy are illustrated. An industrial design example, the IBM z990 system, shows how the industry is dealing with soft errors these days.**

I. Introduction

From the beginning of the recorded history, man has believed in the influence of heavenly bodies on the life on Earth. Machines, electronics included, are considered scientific objects whose fate is controlled by man. So, in spite of the knowledge of the exact date and time of its manufacture, we do not draft a horoscope for a machine. Lately, however, we have started noticing certain behaviors in the state of the art electronic circuits whose causes are traced to be external and to the celestial bodies outside our Earth. The *Single Even Upset* (SEU) phenomenon, as this non-permanent (i.e., random or soft) error behavior is termed, in digital systems affects the modern nanotechnology electronic devices. We believe SEU will assume greater importance in the future [12]. Sifting through the literature of the last half a century, we have collected the necessary material for a starter. Our aim is not to cram up these six pages with most information, but to provide the essentials that can be assimilated conveniently to help a reader to become an effective contributor. We begin with the definition.

> "**Single Event Upset (SEU):** Radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs". · · · *NASA Thesaurus*

The objective of this tutorial is to familiarize the reader with the SEU in digital electronics – definitions and terms, causes (mostly experimental), measurement and estimation, reliability standards, and the related design methods. You should expect to get almost complete, but not comprehensive, information. Looking over the Appendix on the last page[illegible] comprehension as you read through this art[illegible]

We will present an up-to-date understan[illegible] phenomena. Following the historical note of t[illegible] tion, we summarize the concept of basic radi[illegible] and explain how a soft error occurs in silic[illegible] Examples of soft error mitigation technique[illegible] Section IV. In Section V, a case study of s[illegible] and tolerance in IBM z990 system is given.

II. Historical Notes

Soft errors have been studied by elec[illegible] nuclear and radiation engineers for almost [illegible] the period 1954 through 1957 failures in [illegible] were reported during the above-ground nu[illegible] These were treated as electronic anomalies [illegible] equipment because they were random and [illegible] not be traced to any hardware fault [27]. [illegible] paper concerning the role of cosmic rays [illegible] by Wallmark and Marcus [24]. As quot[illegible] literature [16], these authors predicted that c[illegible] start upsetting microcircuits due to heavy[illegible] strikes and cosmic ray reactions when feat[illegible] small enough. Through 1970s and early 198[illegible] radiation received attention and more rese[illegible] the physics of these phenomena. Also from 1950s, theories of fault tolerance and self-repairing computing were being developed due to the increased reliability requirement of critical applications like the space-mission [23].

May and Woods of Intel Corporation [13] determined that these errors were caused by the alpha particles emitted in the radioactive decay of uranium and thorium present just in few parts-per-million levels in package materials. Their paper represented the first public account of radiation-induced upsets in electronic devices at sea level and these errors were referred to as "soft errors". The term soft error was used to differentiate from the repeatable errors traceable to permanent hardware faults. Guenzer and Wolicki [10] reported that the error causing particles came not only from uranium and thorium but that nuclear reactions generated high energy neutrons and protons, which could also cause upsets in circuits. Because the title of their paper was "Single Event Upset of Dynamic RAMs by Neutrons and Protons", the term "SEU" has been in use ever since [10] (refer to [16]). In 1979, Ziegler and Lanford from IBM [28] predicted that cosmic rays could

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DOI 10.1109/VLSI.2008.28

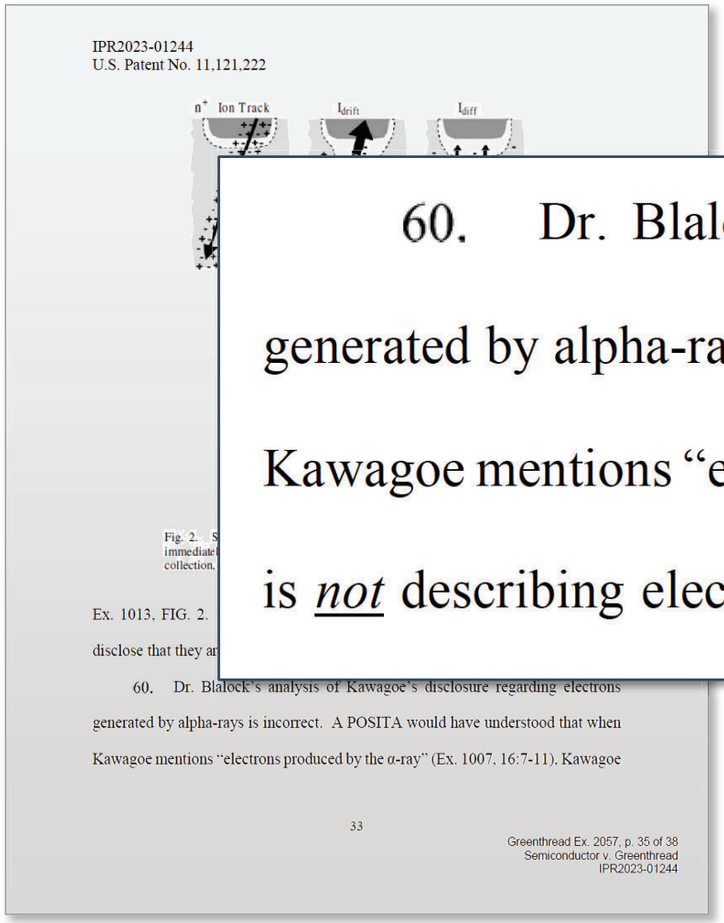
IEEE computer society
ONSEMI EXHIBIT 1013, Page 1

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DOI 10.1109/VLSI.2008.28

-01242: Ex. 1009 (Wang) at 1

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Kawagoe does <u>not</u> move electrons from the surface to the substrate.

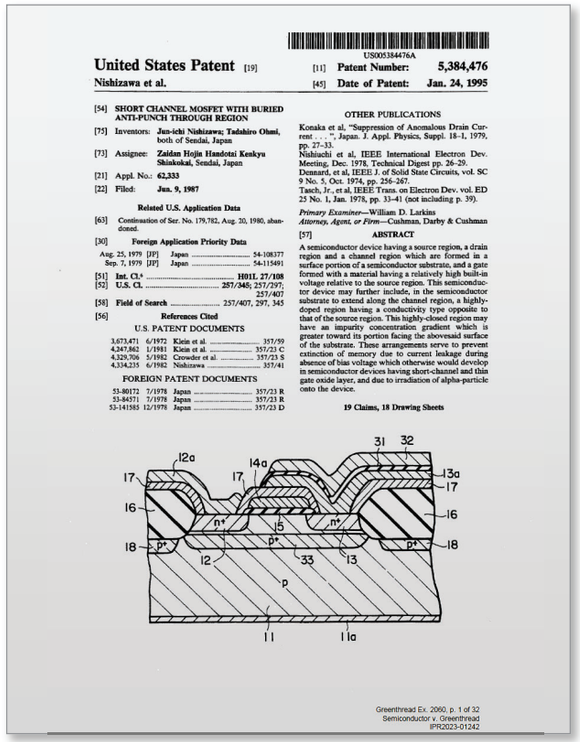


60. Dr. Blalock's analysis of Kawagoe's disclosure regarding electrons generated by alpha-rays is incorrect. A POSITA would have understood that when Kawagoe mentions "electrons produced by the α-ray" (Ex. 1007, 16:7-11), Kawagoe is *not* describing electrons near the surface. Nishizawa (Ex. 2060), demonstrates

-01242: Ex. 2057 (Glew Decl.) at ¶60

-01242: Grounds 1, 3 & 5; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Kawagoe does <u>not</u> move electrons from the surface to the substrate.



US005384476A

United States Patent [19]
Nishizawa et al.

[11] **Patent Number: 5,384,476**
[45] **Date of Patent: Jan. 24, 1995**

[54] **SHORT CHANNEL MOSFET WITH BURIED ANTI-PUNCH THROUGH REGION**

[75] Inventors: **Jun-ichi Nishizawa; Tadahiro Ohmi**, both of Sendai, Japan

[73] Assignee: **Zaidan Hojin Handotai Kenkyu Shinkokai**, Sendai, Japan

[21] Appl. No.: **62,333**

[22] Filed: **Jun. 9, 1987**

Related U.S. Application Data

[63] Continuation of Ser. No. 179,782, Aug. 20, 1980, abandoned.

[30] **Foreign Application Priority Data**

Aug. 25, 1979 [JP] Japan 54-108377
Sep. 7, 1979 [JP] Japan 54-115491

[51] **Int. Cl.**[6] **H01L 27/108**
[52] **U.S. Cl.** **257/345**; 257/297; 257/407
[58] **Field of Search** 257/407, 297, 345

[56] **References Cited**

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Dennard, et al, IEEE J. of Solid State Circuits, vol. SC 9 No. 5, Oct. 1974, pp. 256-267.
Tasch, Jr., et al, IEEE Trans. on Electron Dev. vol. ED 25 No. 1, Jan. 1978, pp. 33-41 (not including p. 39).

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

A semiconductor device having a source region, a drain region and a channel region which are formed in a surface portion of a semiconductor substrate, and a gate formed with a material having a relatively high built-in voltage relative to the source region. This semiconductor device may further include, in the semiconductor substrate to extend along the channel region, a highly-doped region having a conductivity type opposite to that of the source region. This highly-closed region may have an impurity concentration gradient which is greater toward its portion facing the abovesaid surface of the substrate. These arrangements serve to prevent extinction of memory due to current leakage during absence of bias voltage which otherwise would develop in semiconductor devices having short-channel and thin gate oxide layer, and due to irradiation of alpha-particle onto the device.

19 Claims, 18 Drawing Sheets

Greenthread Ex. 2060, p. 1 of 32
Semiconductor v. Greenthread
IPR2023-01242

into, for example, silicon. As shown in FIG. 33, when the alpha-particle gains an energy ϵ_3 of about 360 keV, it creates electron-hole pairs with highest probability. In case the alpha-particle gains an energy higher than that, the probability of generation of electron-hole pairs drops sharply. Accordingly, it will be understood that the alpha-particle immediately after irradiation to the surface of a semiconductor body has an energy of several MeV, for example about 5 MeV, and that, accordingly, the probability of creation of electron-hole pairs is extremely low near the surface. The alpha-particle will begin to create electron-hole pairs after it has entered into the semiconductor substrate to a certain distance. The number of electron-hole pairs which are

electrons is 1.9×10^6. That is, the amount of electrons created which adversely affect the memory action is no greater than only 10% of the stored electric charge, and thus it can be disregarded.

-01242: Ex. 2060 (Nishizawa) at 19:21-34; 20:19-22

-01243: Grounds 1 & 3; Elements 1.5 & 9.5

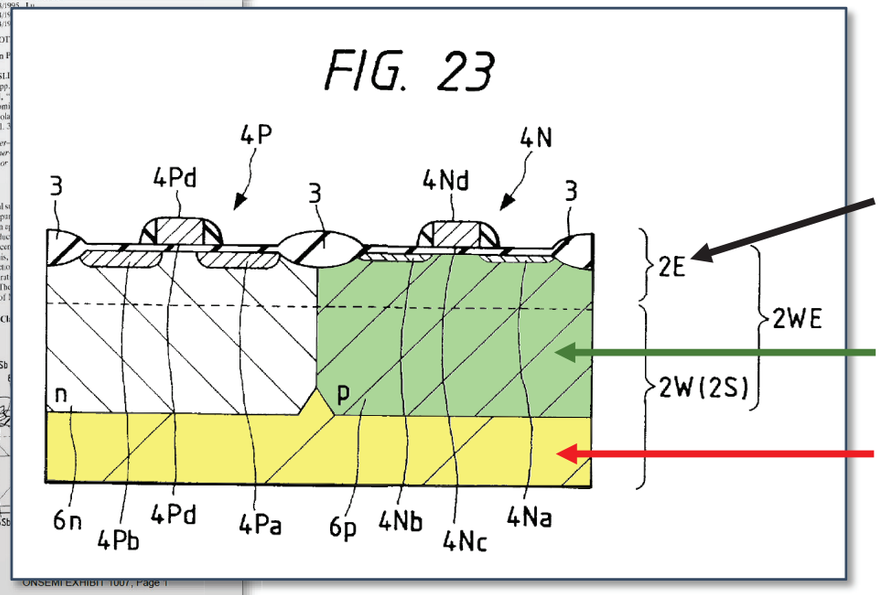
- The same points apply to the -01243 petition.

1. A semiconductor device, comprising:
a substrate of a first doping type at a first doping level having first and second surfaces;
a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region; and
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

-01243: Ex. 1001 ('842 pat.) at 4:45-60

lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body **2S** by that concentration gradient and prevented from entering the p-well **6***p* so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well **6***p*. The impurity

Ex. 1007 at 15:62-16:11



active region/ surface

electrons do not enter p-well

electrons are here

-01243: Ex. 1007 (Kawagoe) at Fig. 23

-01244: Ground 2; Element 44.5

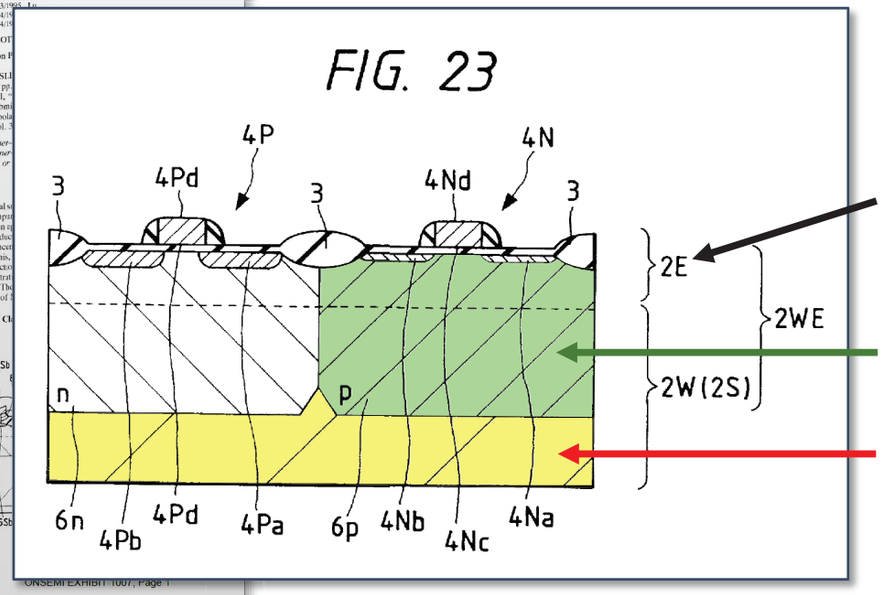
- The same points apply to the -01244 petition.

44. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of the surface layer;
a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and
at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

-01244: Ex. 1001 ('222 pat.) at 8:21-39

lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body **2S** by that concentration gradient and prevented from entering the p-well **6***p* so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well **6***p*. The impurity

Ex. 1007 at 15:62-16:11



-01244: Ex. 1007 (Kawagoe) at Fig. 23

Summary

- **"Aid carrier movement"**
  - **"Graded dopant concentration" does not necessarily "aid carrier movement."**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- **Petitioner cannot rely on inherency for "aid carrier movement"**
  - **Petition never mentions inherency**
  - **There is no evidence carriers necessarily move from the surface to the substrate**
- **Petitioner's Kawagoe grounds fail**
  - **Kawagoe does not aid carrier movement from active region (or surface) to substrate**
  - **Petition does not identify a "second doping type opposite in conductivity"**
- Petitioner's Wieczorek grounds fail
- Petitioner's Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- The Petition identifies the "first doping type" as p-type.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

Petition for *Inter Partes* Review of

UNITED STATES PAT

BEFORE THE PATEN

SEMICONDUCTOR C

GREE

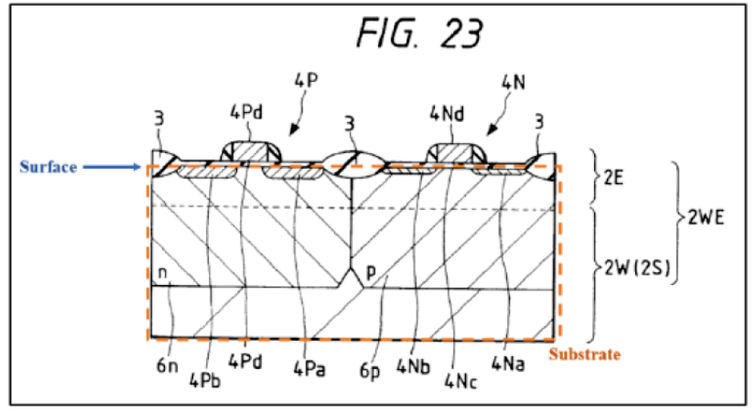
U.S. PAT

Case

PETITION FOR
UNDER 35 U.S.C.

Active 104900912.5.DOCX

Kawagoe discloses "semiconductor substrate body 2S" of a first doping type (p-type) having a silicon "epitaxial layer 2E [] doped with a ***p-type*** impurity such as boron" formed over non-epitaxial "semiconductor substrate body 2S [also] doped with a ***p-type*** impurity such as boron...."[6] EX1007, 14:61-15:12, 6:50-7:3. The substrate (orange) has a surface, shown below. EX1003, ¶69.



EX1007, FIG. 23.

-01242: Pet. [1] at 8-9

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

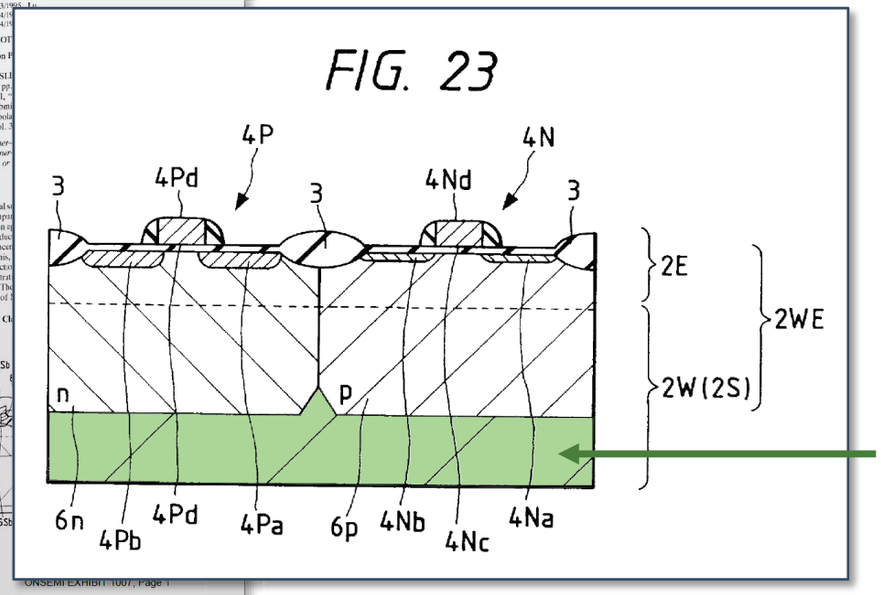
- In Kawagoe, the identified "substrate" is p-type.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

500 to 800 μm, for example. The semiconductor substrate body **2S** is doped with a p-type impurity such as boron (B) in a concentration of about 1.3×10^{15} atoms/cm^3.

-01242: Ex. 1007 at 6:62-63



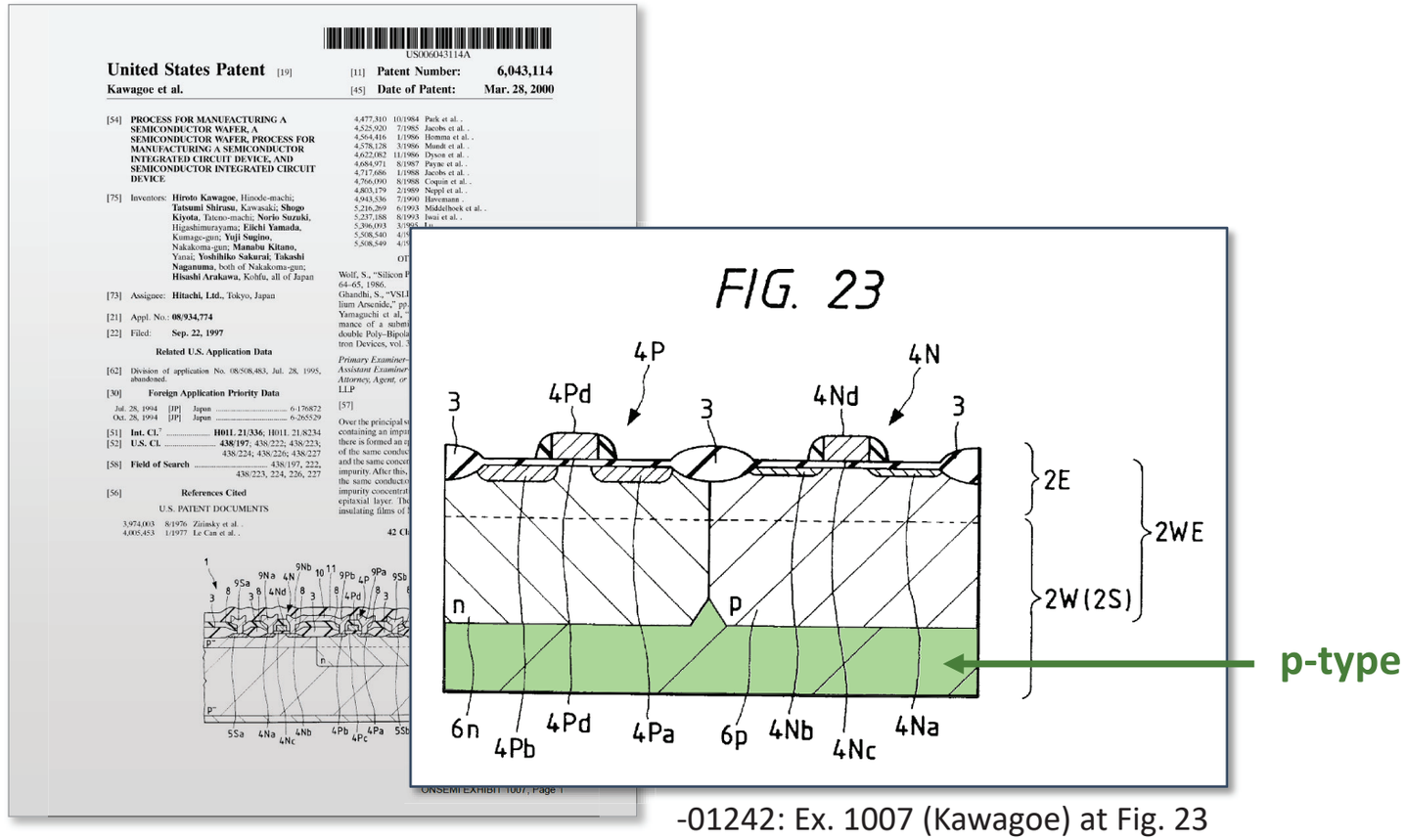
-01242: Ex. 1007 (Kawagoe) at Fig. 23

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- The claim requires a first active region with a “second doping type.”

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 (’222 pat.) at 4:38-62



-01242: Ex. 1007 (Kawagoe) at Fig. 23

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- The petition relies on transistor 4N.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62


Petition for *Inter Pa*

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Active 104900912.5.DOCX

Kawagoe discloses "semiconductor regions 4Na and 4Nb ... for forming the ***source-drain regions*** of the nMOS [n-channel transistor] 4N." EX1007, 8:66-67, 3:30-37, 8:46-52, 14:46-55, 15:26-40. Source-drain regions 4Na/4Nb (purple) form part of the claimed first active region, which also includes the channel region (light purple) between source-drain regions 4Na/4Nb and below insulating film 4Nc. *Id.*, 8:46-65, 14:46-55, 15:26-40; EX1003, ¶81; EX1008B, 299-300 ("The top surface of the [substrate] body consists of *active* or *transistor* regions as well as *passive* or (*field*) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source*** and ***drain*** regions."), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; EX1008C, 525, FIG. 8-1(e). As shown in Figure 23, nMOS transistor 4N is formed in the surface of the first active region, which is adjacent the surface of the substrate. EX1003, ¶81.

-01242: Pet. [1] at 13-14

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

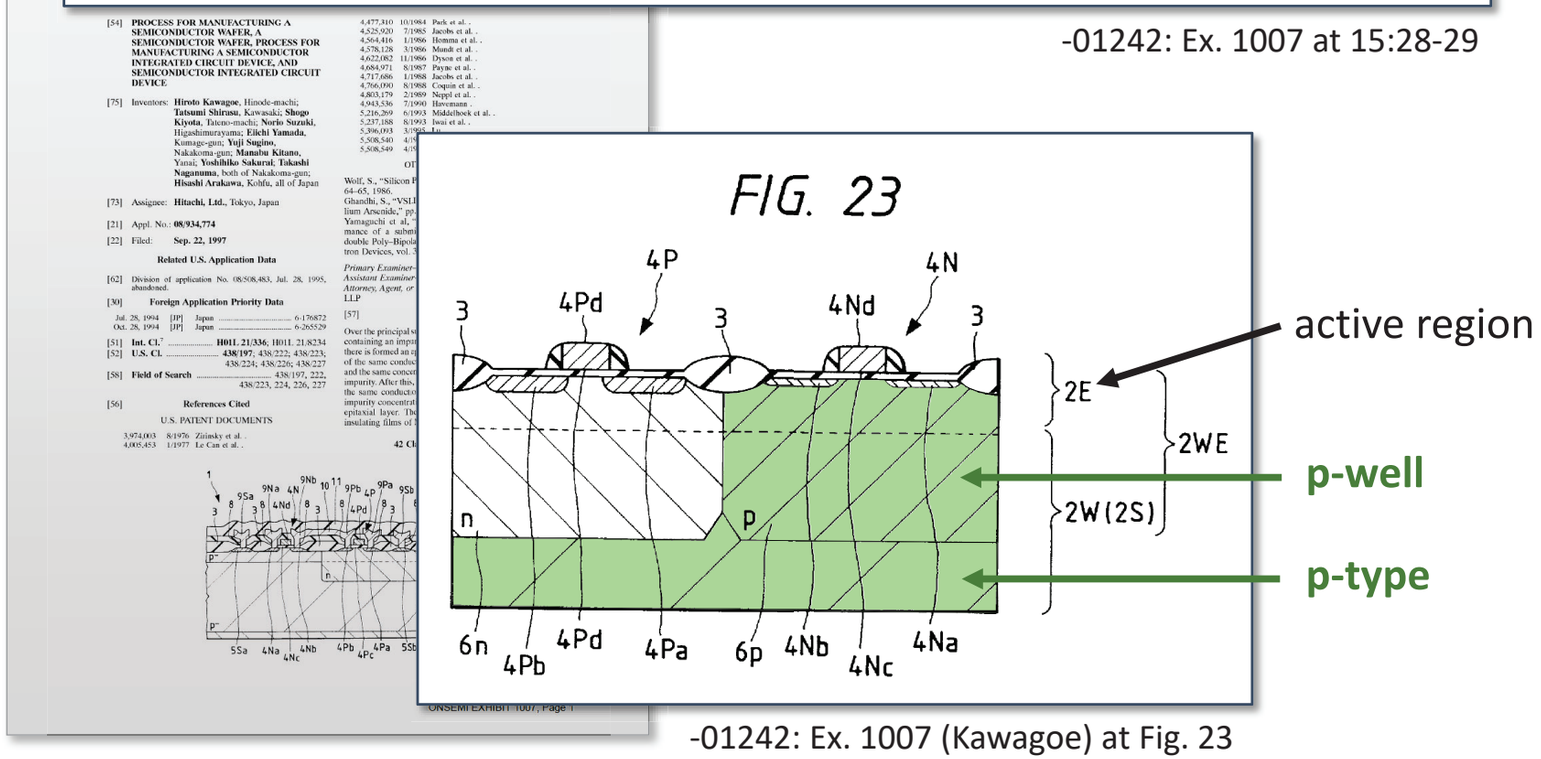
- The active region for transistor 4N is also p-type.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

and an n-well (i.e., the first semiconductor region) 6*n*. The p-well 6*p* is doped with a p-type impurity such as boron. The

-01242: Ex. 1007 at 15:28-29



-01242: Ex. 1007 (Kawagoe) at Fig. 23

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

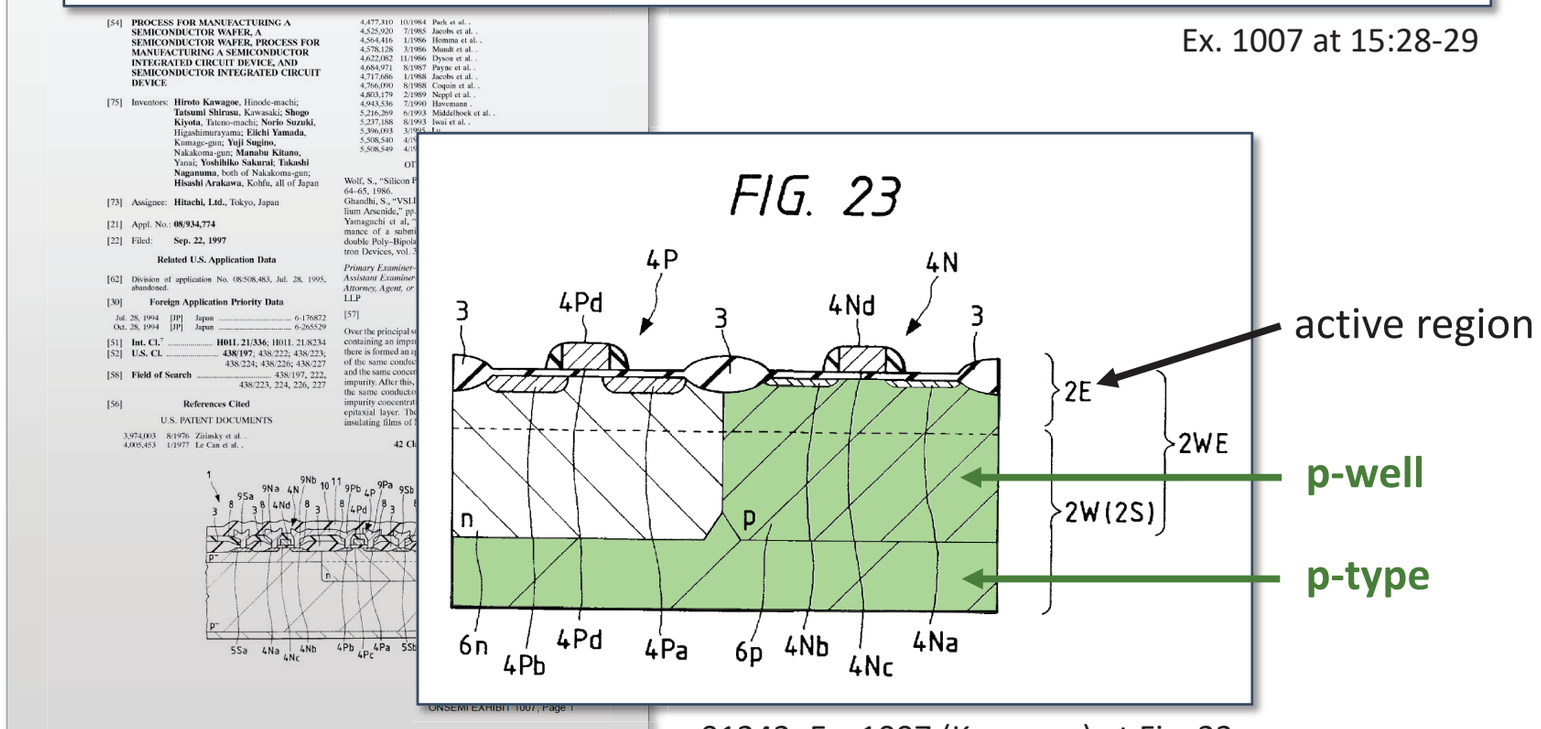
- The claim makes clear that the active region is where a transistor may be built.
- This means the doping type is determined by the well region before the source and drain are counter-doped.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

and an n-well (i.e., the first semiconductor region) 6*n*. The p-well 6*p* is doped with a p-type impurity such as boron. The

Ex. 1007 at 15:28-29



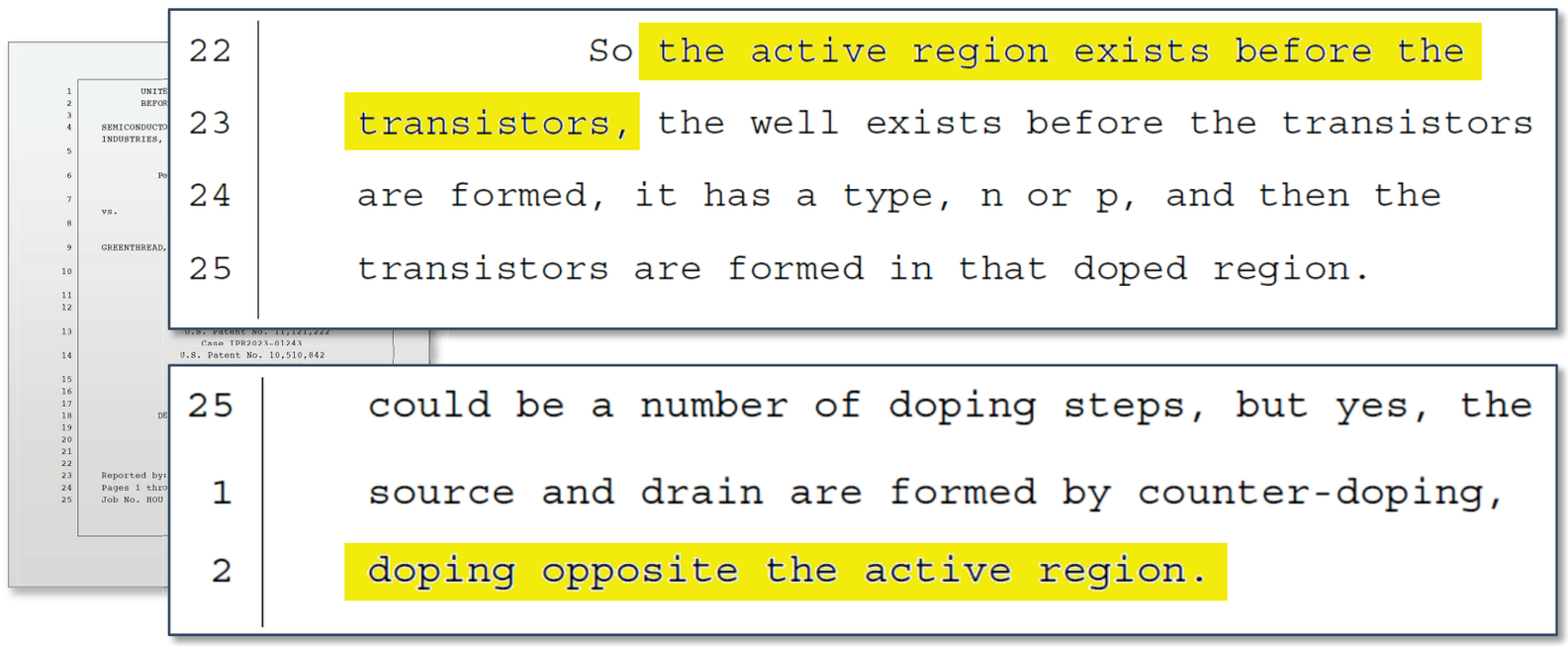
-01242: Ex. 1007 (Kawagoe) at Fig. 23

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- The claim makes clear that the active region is where a transistor may be built.
- This means the doping type is determined by the well region before the source and drain are counter-doped.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62



22 So the active region exists before the
23 transistors, the well exists before the transistors
24 are formed, it has a type, n or p, and then the
25 transistors are formed in that doped region.

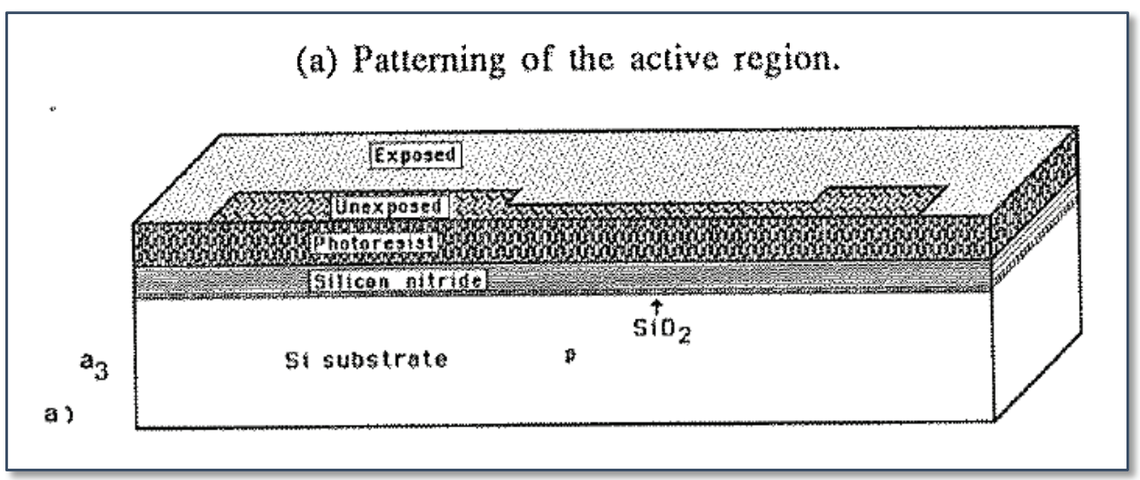
25 could be a number of doping steps, but yes, the
1 source and drain are formed by counter-doping,
2 doping opposite the active region.

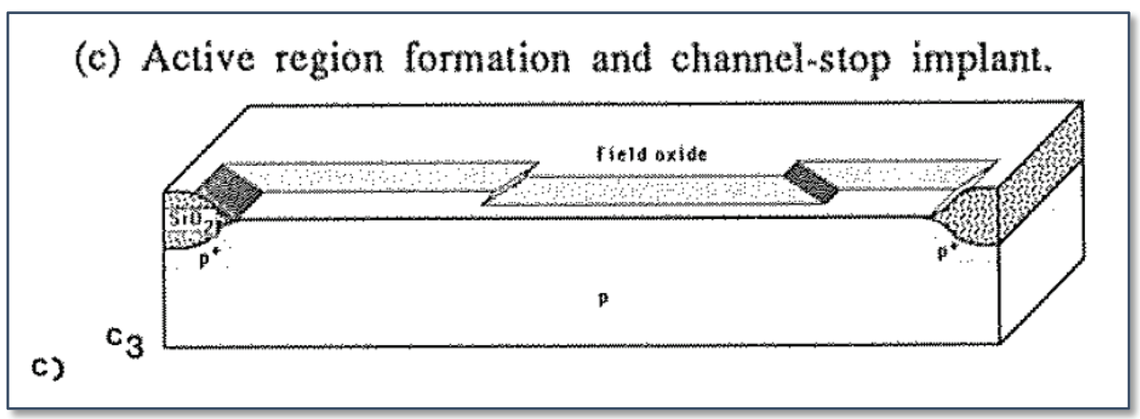
-01242: Ex. 1052 (Glew Dep. Tr.) at 24:22-25; 27:25-28:2

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- The claim makes clear that the active region is where a transistor may be built.
- This means the doping type is determined by the well region before the source and drain are counter-doped.

then used to cover the PMOS device active regions. An *n*-type implant heavy enough to overcompensate for the boron implant in the active regions of the *n*-channel devices is used to form the sources and drains of the NMOS transistors.



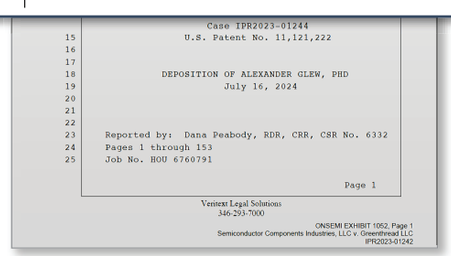


-01242: Ex. 1008A (Wolf) at 123; Ex. 1008B (Wolf) at 63, 64

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- The claim makes clear that the active region is where a transistor may be built.
- This means the doping type is determined by the well region before the source and drain are counter-doped.

are different types of active areas. Looking back at 5A, one can see a p-well and an n-well. Basically, sources and drains are of the opposite type of well or active area they're formed in, so wells -- sources and drains are counter-doped. So if I have an n-type source and drain, it will be formed in a p-type region. If I have a p-type source and drain, it's formed in an n-type region.


Case IPR2023-01244
U.S. Patent No. 11,121,222

DEPOSITION OF ALEXANDER GLEW, PHD
July 16, 2024

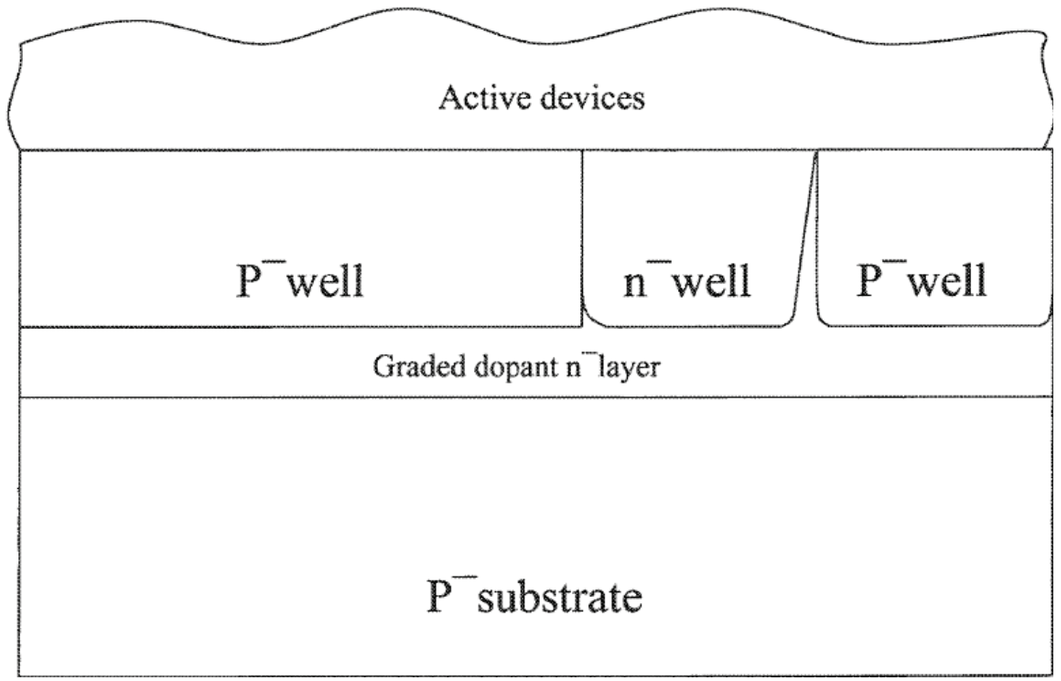
Reported by: Dana Peabody, RDR, CRR, CSR No. 6332
Pages 1 through 153
Job No. HOU 6760791

Page 1

Veritext Legal Solutions
346-293-7000

ONSEMI EXHIBIT 1052, Page 1
Semiconductor Components Industries, LLC v. Greenthread LLC
IPR2023-01242

-01242: Ex. 1052 (Glew Dep. Tr.) at 24:2-9



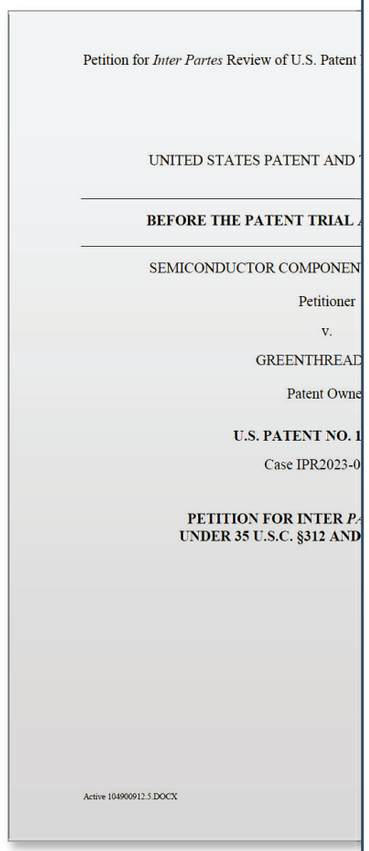
-01242: Ex. 1001 ('222 pat.) at FIG. 5A

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- The doping type for the active region is not n-type.
- The doping type for the active region is not opposite in conductivity.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62


Petition for *Inter Partes* Review of U.S. Patent

UNITED STATES PATENT AND

BEFORE THE PATENT TRIAL

SEMICONDUCTOR COMPONEN

Petitioner

v.

GREENTHREAD

Patent Owne

U.S. PATENT NO. 1

Case IPR2023-0

PETITION FOR INTER *P*
UNDER 35 U.S.C. §312 AND

Active 104900912.5.DOCX

Kawagoe discloses "semiconductor regions 4Na and 4Nb ... for forming the ***source-drain regions*** of the nMOS [n-channel transistor] 4N." EX1007, 8:66-67, 3:30-37, 8:46-52, 14:46-55, 15:26-40. Source-drain regions 4Na/4Nb (purple) form part of the claimed first active region, which also includes the channel region (light purple) between source-drain regions 4Na/4Nb and below insulating film 4Nc. *Id.*, 8:46-65, 14:46-55, 15:26-40; EX1003, ¶81; EX1008B, 299-300 ("The top surface of the [substrate] body consists of *active* or *transistor* regions as well as *passive* or (*field*) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source*** and ***drain*** regions."), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; EX1008C, 525, FIG. 8-1(e). As shown in Figure 23, nMOS transistor 4N is formed in the surface of the first active region, which is adjacent the surface of the substrate. EX1003, ¶81.

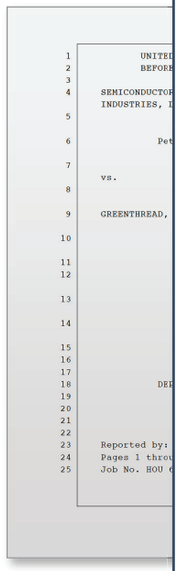
-01242: Pet. [1] at 13-14

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- The doping type for the active region is not n-type.
- The doping type for the active region is not opposite in conductivity.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62



18 Q. Okay. So when a transistor is formed in
19 the first active region, per the fourth element,
20 it's a p-type well; n-type dopants would be added to
21 form the transistor, right?
22 A. Yes, n-type dopants are added to form the
23 source and drain. There may be other doping steps
24 involved. That's sort of a simplification. There
25 could be a number of doping steps, but yes, the

1 source and drain are formed by counter-doping,
2 doping opposite the active region.

-01242: Ex. 1052 (Glew Dep. Tr.) at 27:18-28:2

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- Realizing its mistake, Petitioner identifies transistor 4P in its Reply.
- Petitioner is not permitted to rely on new arguments or evidence in its Reply.


UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC
Petitioner

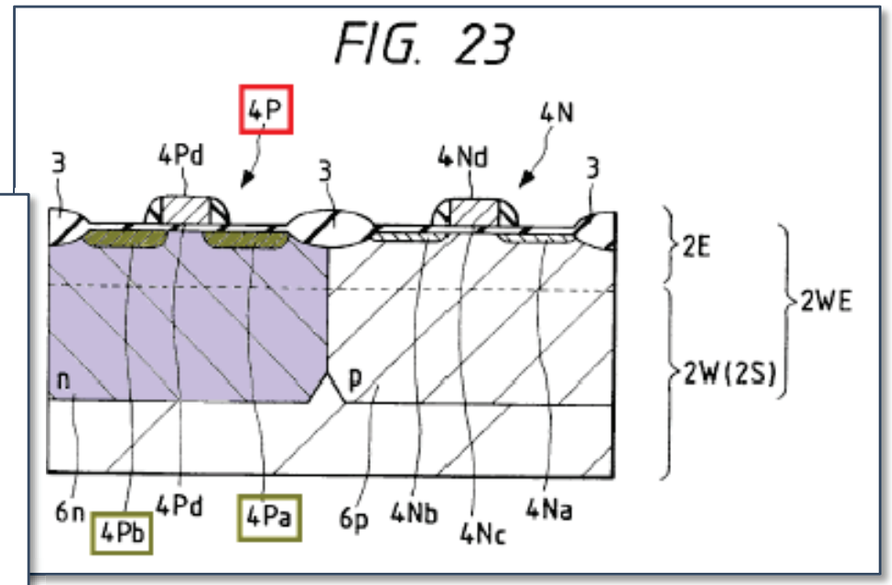
v.

GREENTHREAD LLC
Patent Owner

Case IPR2023-01242
U.S. Patent No. 11,121,222

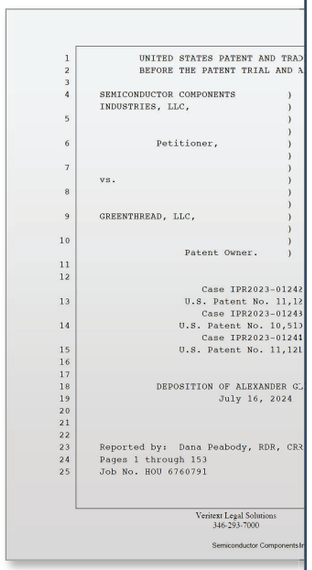
However, the Board need not resolve this dispute because even under the PO's incorrect interpretation, Kawagoe still teaches this limitation. Specifically, Kawagoe describes a CMOS device that has both the NMOS device ***and*** an adjacent PMOS transistor 4P having source and drain regions 4Pa, 4Pb formed with an n-type channel in n-type well 6n. EX1007, 9:40-54, 17:50-54, 18:15-23, 21:55-61, Fig. 23.

-01242: Pet. Reply [62] at 18



-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

- Realizing its mistake, Petitioner identifies transistor 4P in its Reply.
- Petitioner is not permitted to rely on new arguments or evidence in its Reply.



UNITED STATES PATENT AND TRA
BEFORE THE PATENT TRIAL AND A

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,

Petitioner,

vs.

GREENTHREAD, LLC,

Patent Owner.

Case IPR2023-01242
U.S. Patent No. 11,12
Case IPR2023-01243
U.S. Patent No. 10,51
Case IPR2023-01244
U.S. Patent No. 11,121

DEPOSITION OF ALEXANDER G.
July 16, 2024

Reported by: Dana Peabody, RDR, CR
Pages 1 through 153
Job No. HOU 6760791

Veritext Legal Solutions
346-293-7000

Semiconductor Components In

Q. Okay. You see on the left-hand side of this figure on 38, there's a PMOS transistor there, right?

THE WITNESS: Yes, there's a transistor there.

BY MR. SPEEGLE:

Q. It's a PMOS transistor on the left side?

(The requested portion was read back.)

THE WITNESS: I don't believe I analyzed that transistor.

-01242: Ex. 1052 (Glew Dep. Tr.) at 130:6-17

-01242: Grounds 1, 3 & 5; Elements 1.2, 21.2, 39.2, 41.2 & 42.2

Even if a part of a prior art reference is discussed in the petition, it cannot be used to satisfy a claim element when the Petition does not use it for that purpose.

Oren Techs., LLC v. Proppant Express Invs. LLC, 2021 WL 3120819, at *4 (Fed. Cir. July 23, 2021)

-01243: Grounds 1 & 3; Elements 1.2 & 9.2

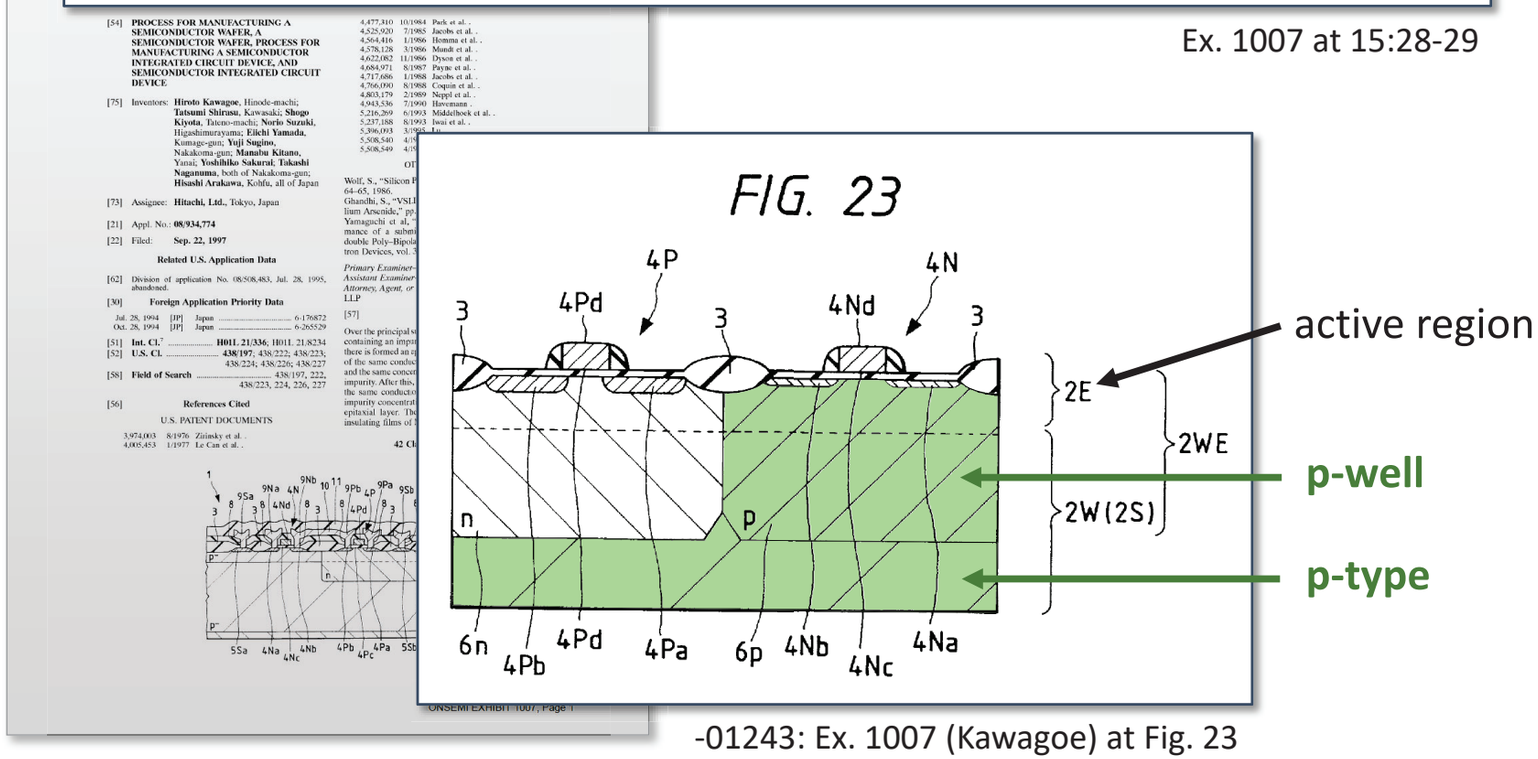
- The same points apply to the -01243 petition.

1. A semiconductor device, comprising:
a substrate of a first doping type at a first doping level having first and second surfaces;
a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region; and
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

-01243: Ex. 1001 ('842 pat.) at 4:45-60

and an n-well (i.e., the first semiconductor region) 6*n*. The p-well 6*p* is doped with a p-type impurity such as boron. The

Ex. 1007 at 15:28-29



-01243: Ex. 1007 (Kawagoe) at Fig. 23

Summary

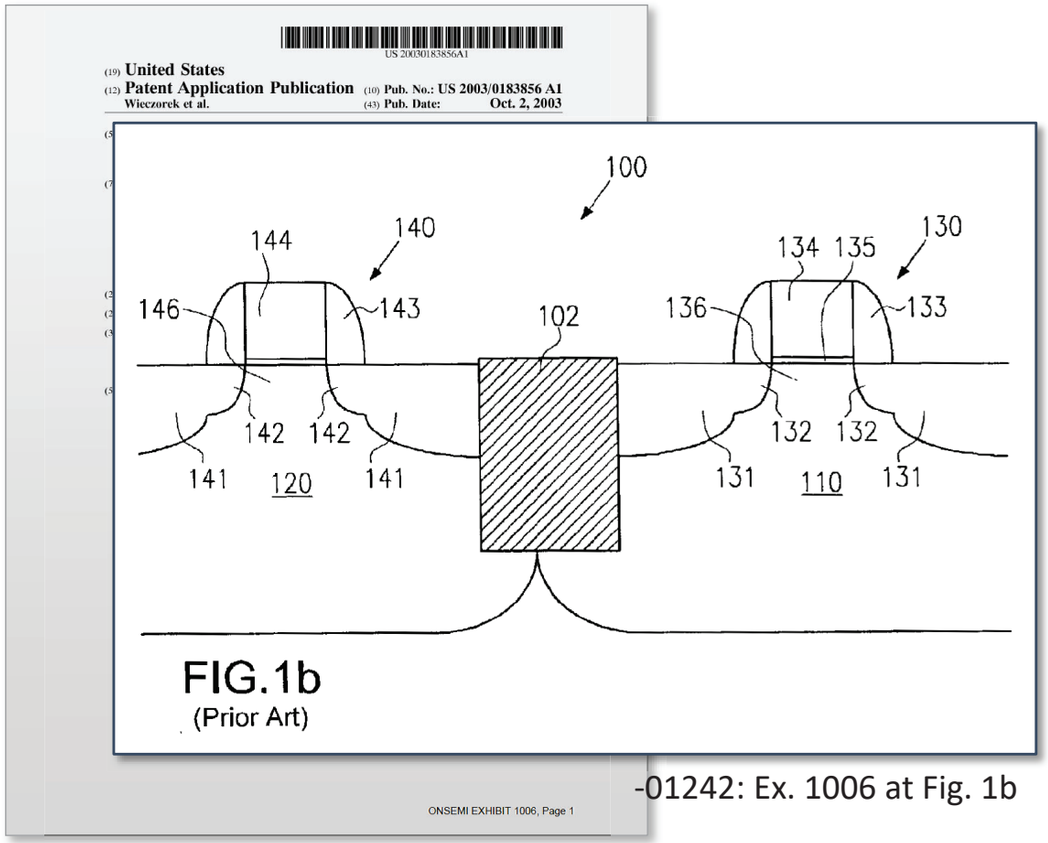
- **"Aid carrier movement"**
  - **"Graded dopant concentration" does not necessarily "aid carrier movement."**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- **Petitioner cannot rely on inherency for "aid carrier movement"**
  - **Petition never mentions inherency**
  - **There is no evidence carriers necessarily move from the surface to the substrate**
- **Petitioner's Kawagoe grounds fail**
  - **Kawagoe does not aid carrier movement from active region (or surface) to substrate**
  - **Petition does not identify a "second doping type opposite in conductivity"**
- **Petitioner's Wieczorek grounds fail**
- Petitioner's Payne ground fails
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

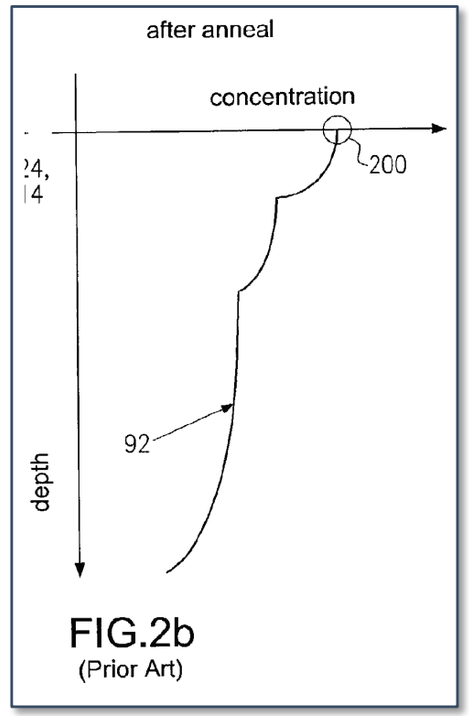
- There is no evidence that carriers move from the surface to the substrate.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62



-01242: Ex. 1006 at Fig. 1b



-01242: Ex. 1006 (Wieczorek) at Fig. 2b

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Wieczorek never mentions carriers, much less moving carriers from the surface to the substrate.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

[0009] **FIG. 2***a* is a graph, in which the dopant concentration of the N-well structure **120** and the P-well structure **110** is depicted with respect to the depth in the respective well structures. In particular, it is evident from **FIG. 2***a* that the V_T implantation (**114**, **124**), indicated by the same reference number as the respective implantation portions, leads to a dopant concentration that significantly decreases at the vicinity of the surface of the semiconductor device **100**. That is, the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile in the N-well structure **120** and the P-well structure **110** near the surface of the semiconductor device **100**, where, after completion of the device, a channel will form during operation of the device.

-01242: Ex. 1006 at [0009]

[0011] **FIG. 2***b* shows a corresponding graph with a typical dopant profile with respect to the depth of the respective well structure. Due to the up-diffusion of the dopant atoms during the heat treatment, the initially retrograde profile in the vicinity of the surface of the semiconductor device **100**, as indicated by reference number **200**, may have become substantially uniformly distributed.

-01242: Ex. 1006 at [0011]

[0013] Typically, the N-channel transistor **130** and the P-channel transistor **140** are formed by the following processes. After the heat treatment, the gate insulation layer **135** is formed, wherein the gate insulation layer may be deposited by chemical vapor deposition (CVD), or, if an oxide layer is used, a rapid thermal furnace process or a conventional furnace oxidation process may be used. Since, commonly, elevated temperatures are involved in fabricating the gate insulation layer **135**, this process also contributes to a further diffusion of the dopants within the P-well structure **110** and the N-well structure **120**. Thereafter, polysilicon is deposited and patterned by sophisticated photolithography techniques to form the gate electrodes **134** and **144**. With a first implantation, the extensions **132** and **142** are defined, and, subsequently, the spacer elements **133**, **143** are formed and serve as an implantation mask during a subsequent implantation process for defining the source and drain regions **131**, **141**. Since a further heat treatment is necessary to activate the dopants within the regions **131**, **132** and **141**, **142** and to cure any crystal damage caused by the preceding implantation steps, the initial dopant concentration, as shown in **FIG. 2***a*, will be even more strongly affected so that, after the plurality of heat treatments, the actual dopant concentration will be represented by the graph shown in **FIG. 2***b*. In particular, it is thus very difficult to obtain or to maintain a retrograde dopant profile in the channel regions **136** and **146**, which would be desirable to achieve an improved carrier mobility therein.

-01242: Ex. 1006 (Wieczorek) at [0013]

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5



"[A]nticipation by inherent disclosure is appropriate only when the reference discloses prior art that ***must necessarily include the unstated limitation***."

Transclean Corp. v. Bridgewood Servs., Inc., 290 F.3d 1364, 1373 (Fed. Cir. 2002)

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Wieczorek says the gradient concentration may be uniform.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62

US 20030183856A1

(19) **United States**
(12) **Patent Application Publication** (10) **Pub. No.: US 2003/0183856 A1**
Wieczorek et al. (43) **Pub. Date: Oct. 2, 2003**

(54) **SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME**

(76) Inventors: **Karsten Wieczorek**, Dresden (DE); **Manfred Horstmann**, Dresden (DE); **Rolf Stephan**, Dresden (DE)

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(21) Appl. No.: **10/282,980**
(22) Filed: **Oct. 29, 2002**
(30) **Foreign Application Priority Data**
Mar. 28, 2002 (DE) 102 14 066.9
Publication Classification
(51) **Int. Cl.**[7] **H01L 29/80**
(52) **U.S. Cl.** **257/285**
(57) **ABSTRACT**

An epitaxially grown channel layer is provided on a well structure after ion implantation steps and heat treatment steps are performed to establish a required dopant profile in the well structure. The channel layer may be undoped or slightly doped, as required, so that the finally obtained dopant concentration in the channel layer is significantly reduced compared to a conventional device to thereby provide a retrograde dopant profile in a channel region of a field effect transistor. Additionally, a barrier diffusion layer may be provided between the well structure and the channel layer to reduce up-diffusion during any heat treatments carried out after the formation of the channel layer. The final dopant profile in the channel region may be adjusted by the thickness of the channel layer, the thickness and the composition of the diffusion barrier layer and any additional implantation steps to introduce dopant atoms in the channel layer.

ONSEMI EXHIBIT 1006, Page 1

[0011] **FIG. 2*b*** shows a corresponding graph with a typical dopant profile with respect to the depth of the respective well structure. Due to the up-diffusion of the dopant atoms during the heat treatment, the initially retrograde profile in the vicinity of the surface of the semiconductor device **100**, as indicated by reference number **200**, may have become substantially uniformly distributed.

Ex. 1006 at [0011]

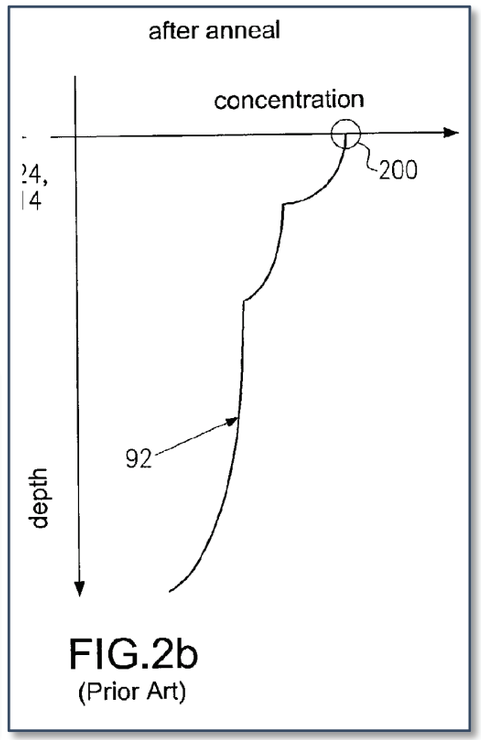


FIG.2b
(Prior Art)

-01242: Ex. 1006 (Wieczorek) at Fig. 2b

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Dr. Blalock admitted the force depends on the slope, and that he did not calculate the slope for any of the references.

Q. How do you know the magnitude of the force a dopant concentration puts on carriers?

A. Well, as the patent owner discussed -- I have references to it, but it's -- I don't know. Anyway, it's related to the -- the steepness of the gradient, the slope of the concentration gradient. And that was also well known by a POSITA as well, which the patent owner pointed out also.

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Greenthread Ex. 2058, p. 1 of 249
Semiconductor v. Greenthread
IPR2023-01242

-01242: Ex. 2058 at 89:3-10

Q. And regarding any of these three references, for the mapping of the claim phrase "aid carrier movement," have you looked at any aspect of the gradient other than its being downward sloping?

MR. SPEEGLE: Objection, form.

THE WITNESS: As I've said, the patent owner tells us that that's sufficient, so that's what I did. I have not done calculations of the slope per se.

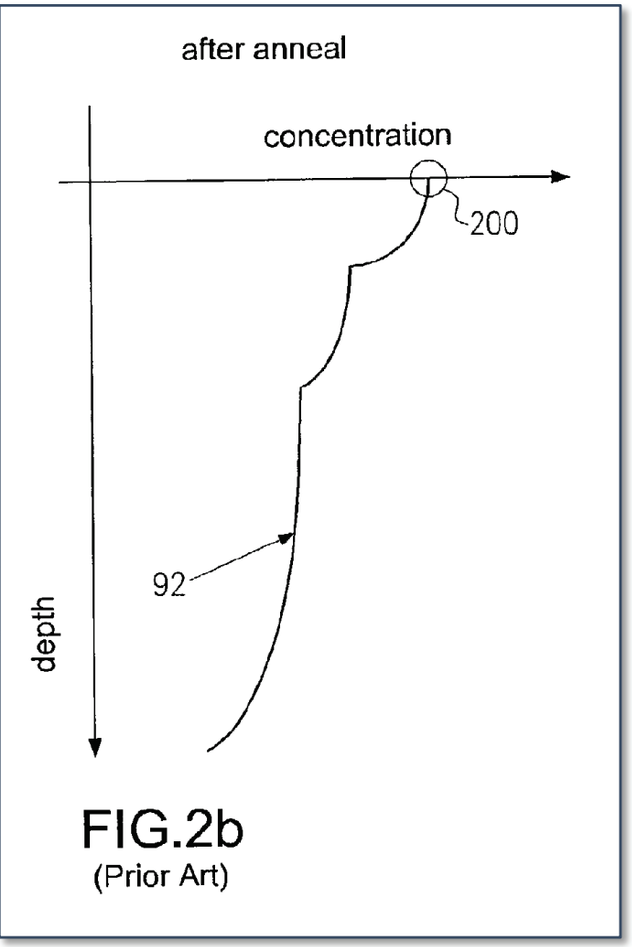
-01242: Ex. 2058 (Blalock Dep. Tr.) at 195:8-16

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- There is no way to determine the slope or whether there is a sufficient force.

60. Dr. Blalock testified that he did not calculate the slope of the concentration gradient that he said Wieczorek discloses. Ex. 2058, 195 ("Q. And regarding any of these three references [including Wieczorek], for the mapping of the claim phrase 'aid carrier movement,' have you looked at any aspect of the gradient other than its being downward sloping? … THE WITNESS: As I've said, the patent owner tells us that that's sufficient, so [t]hat's what I did. I have not done calculations of the slope per se."). It would have been impossible for Dr. Blalock to make such a calculation because the dopant gradient Petitioner points to in Figure 2B (and Wieczorek generally) does not have any values from which one could calculate a slope. In mathematical terms, the slope in each direction (X, Y, and Z) is known formally as the gradient vector. The magnitude of the slope is essential to determine the magnitude of the force the dopant gradient places on the carrier and thus the net force.

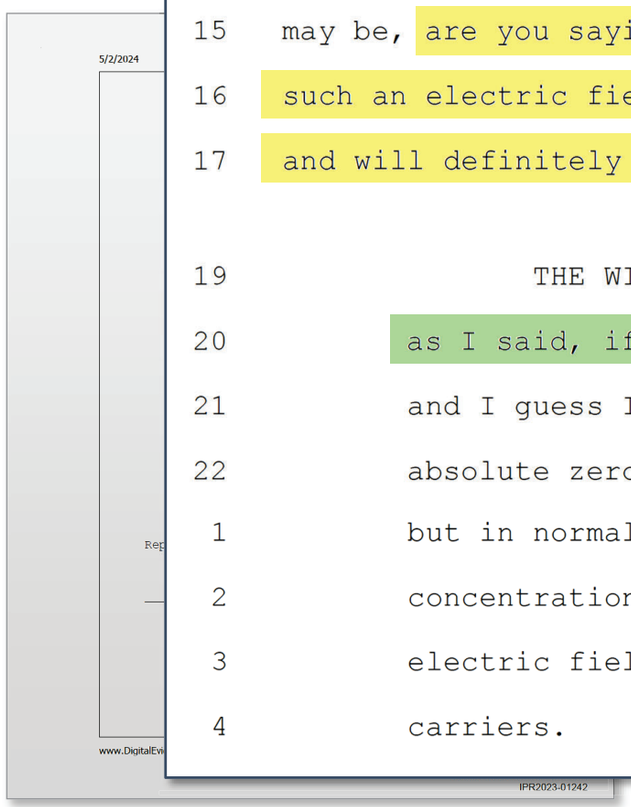
-01242: Ex. 2057 (Glew Decl.) at ¶60



-01242: Ex. 1006 (Wieczorek) at Fig. 2b

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Dr. Blalock admitted that an electric field does not always move carriers.



Q. I'm saying apart from what the patent owner said and whatever your interpretation of that may be, are you saying that as a matter of physics, such an electric field will definitely be created and will definitely move carriers?

* * *

THE WITNESS: I mean, it depends on -- as I said, if there are no other fields -- and I guess I should qualify for not an absolute zero temperature, all this stuff, but in normal circumstances, if you have a concentration gradient, it will result in an electric field, which will then act on the carriers.

Q. So you mentioned that if there aren't other fields present and the carrier was introduced into that field, you'll move the carrier.

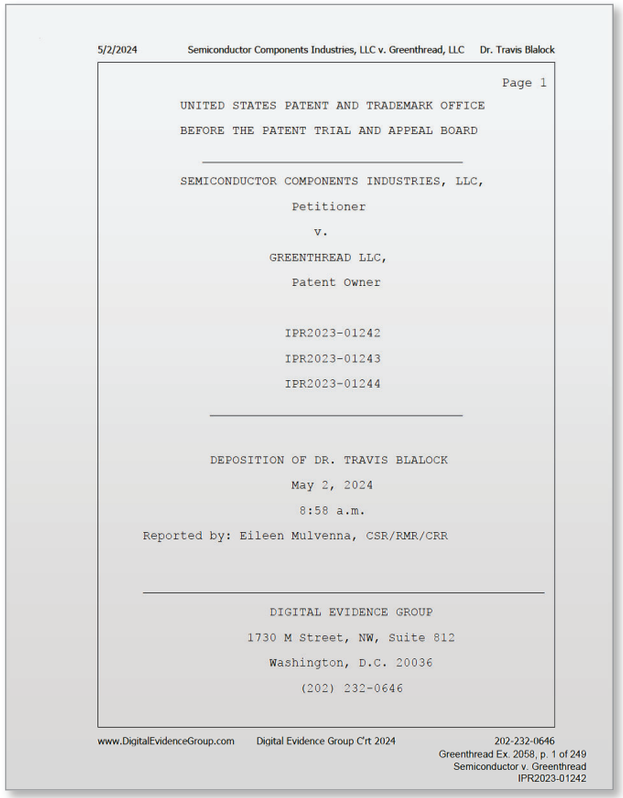
Where could other fields come from?

A. Externally applied voltages from the circuit, if the structure's in a circuit, things like that. Or I suppose some environmental effect. I don't know.

-01242: Ex. 2058 (Blalock Dep. Tr.) at 131:13-132:13

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- Dr. Blalock also admitted that there may be a force that is larger than the gradient force.



5/2/2024 Semiconductor Components Industries, LLC v. Greenthread, LLC Dr. Travis Blalock

Page 1

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,
Petitioner
v.
GREENTHREAD LLC,
Patent Owner

IPR2023-01242
IPR2023-01243
IPR2023-01244

DEPOSITION OF DR. TRAVIS BLALOCK
May 2, 2024
8:58 a.m.
Reported by: Eileen Mulvenna, CSR/RMR/CRR

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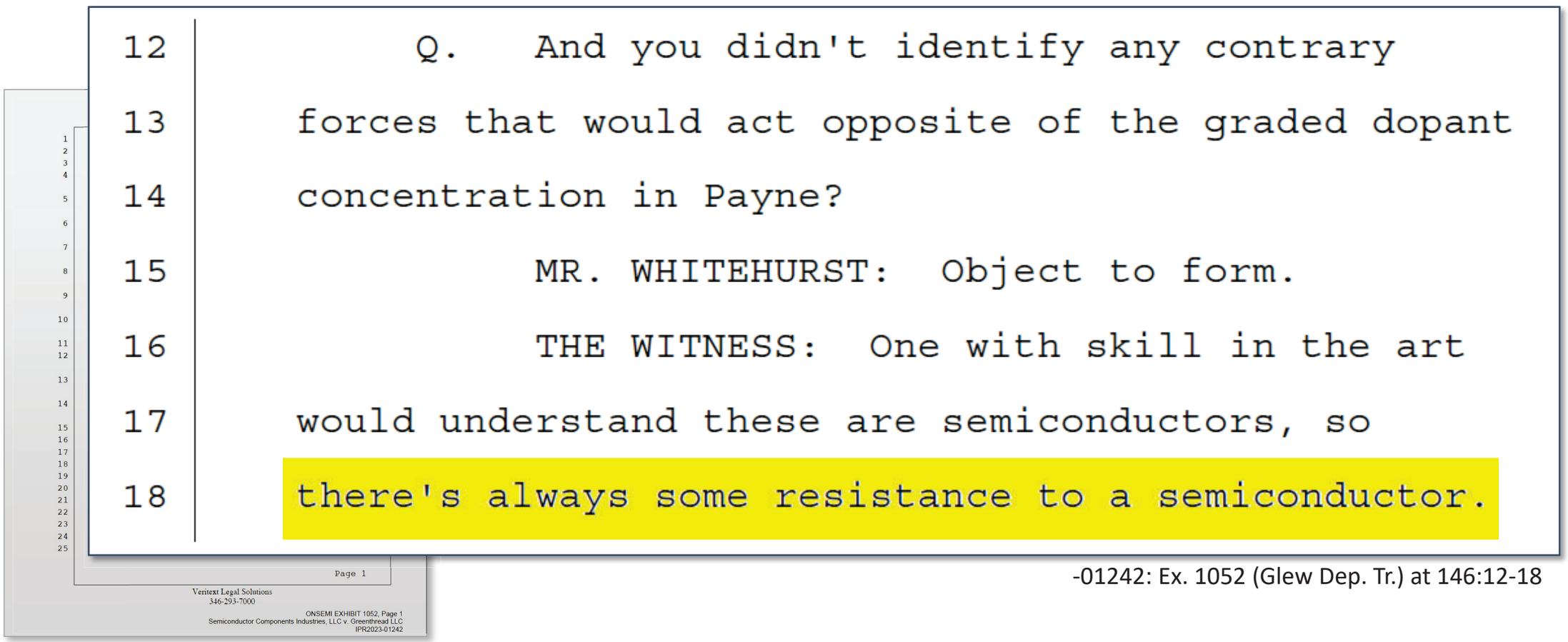
17 Q. Is there a gradient that would be so
18 steep or so shallow, that it would not aid carrier
19 movements?
* * *
22 THE WITNESS: It will create a force.

1 A shallow or a steep one will create a force.
2 As I said a few moments ago, as I've already
3 answered, if there are -- through some other
4 imagined, who knows, means, someone creates
5 an additional force, that might be larger
6 than the force created by the gradient.
7 But there will be a force -- that
8 mechanism, the gradient mechanism which
9 creates the force, which acts in the
10 direction to move the carriers, will be
11 there.

-01242: Ex. 2058 (Blalock Dep. Tr.) at 137:17-138:11

-01242: Grounds 2, 4 & 6; Elements 1.5, 21.5, 39.5, 41.5 & 42.5

- An electric field does <u>not</u> necessarily overcome the resistance of the semiconductor.



Q. And you didn't identify any contrary forces that would act opposite of the graded dopant concentration in Payne?

MR. WHITEHURST: Object to form.

THE WITNESS: One with skill in the art would understand these are semiconductors, so there's always some resistance to a semiconductor.

Page 1

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ONSEMI EXHIBIT 1052, Page 1
Semiconductor Components Industries, LLC v. Greenthread LLC
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-01242: Ex. 1052 (Glew Dep. Tr.) at 146:12-18

-01243: Grounds 2 & 4; Elements 1.5 & 9.5

- The same points apply to the -01243 petition.

1. A semiconductor device, comprising:
a substrate of a first doping type at a first doping level having first and second surfaces;
a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region; and
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

-01243: Ex. 1001 ('842 pat.) at 4:45-60

US 20030183856A1

(19) **United States**
(12) **Patent Application Publication** (10) **Pub. No.: US 2003/0183856 A1**
Wieczorek et al. (43) **Pub. Date: Oct. 2, 2003**

(54) **SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME**

(76) Inventors: **Karsten Wieczorek**, Dresden (DE); **Manfred Horstmann**, Dresden (DE); **Rolf Stephan**, Dresden (DE)

Correspondence Address:
J. Mike Amerson
Williams, Morgan & Amerson, P.C.
Suite 250
7676 Hillmont
Houston, TX 77040 (US)

(21) Appl. No.: **10/282,980**

(22) Filed: **Oct. 29, 2002**

(30) **Foreign Application Priority Data**

Mar. 28, 2002 (DE) 102 14 066.9

Publication Classification

(51) **Int. Cl.**[7] **H01L 29/80**

(52) **U.S. Cl.** **257/285**

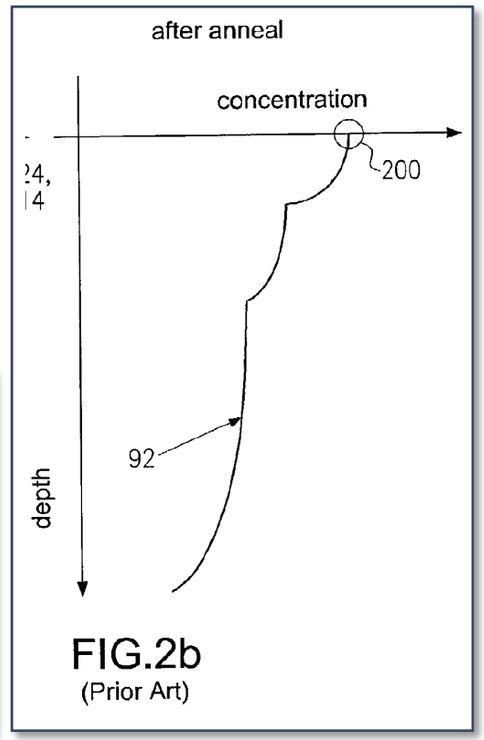
(57) **ABSTRACT**

An epitaxially grown channel layer is provided on a well structure after ion implantation steps and heat treatment steps are performed to establish a required dopant profile in the well structure. The channel layer may be undoped or slightly doped, as required, so that the finally obtained dopant concentration in the channel layer is significantly reduced compared to a conventional device to thereby provide a retrograde dopant profile in a channel region of a field effect transistor. Additionally, a barrier diffusion layer may be provided between the well structure and the channel layer to reduce up-diffusion during any heat treatments carried out after the formation of the channel layer. The final dopant profile in the channel region may be adjusted by the thickness of the channel layer, the thickness and the composition of the diffusion barrier layer and any additional implantation steps to introduce dopant atoms in the channel layer.

[0011] **FIG. 2*b*** shows a corresponding graph with a typical dopant profile with respect to the depth of the respective well structure. Due to the up-diffusion of the dopant atoms during the heat treatment, the initially retrograde profile in the vicinity of the surface of the semiconductor device **100**, as indicated by reference number **200**, may have become substantially uniformly distributed.

ONSEMI EXHIBIT 1006, Page 1

Ex. 1006 at [0011]



-01243: Ex. 1006 (Wieczorek) at Fig. 2b

Summary

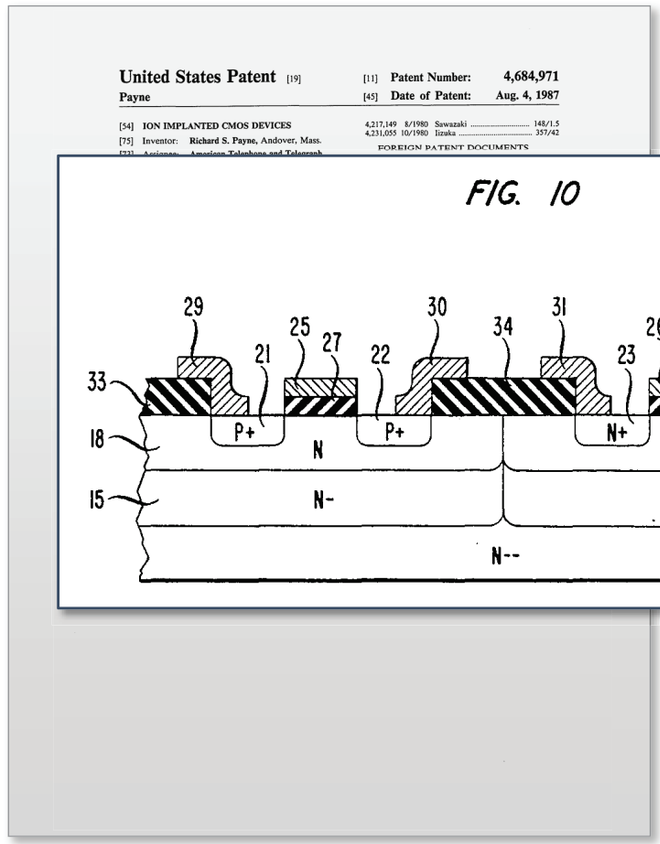
- **"Aid carrier movement"**
  - **"Graded dopant concentration" does not necessarily "aid carrier movement."**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- **Petitioner cannot rely on inherency for "aid carrier movement"**
  - **Petition never mentions inherency**
  - **There is no evidence carriers necessarily move from the surface to the substrate**
- **Petitioner's Kawagoe grounds fail**
  - **Kawagoe does not aid carrier movement from active region (or surface) to substrate**
  - **Petition does not identify a "second doping type opposite in conductivity"**
- **Petitioner's Wieczorek grounds fail**
- **Petitioner's Payne ground fails**
- Substantial evidence of objective indicia of non-obviousness
- Petitioner has not shown that the Petitions are timely

-01244: Ground 1; Element 44.5

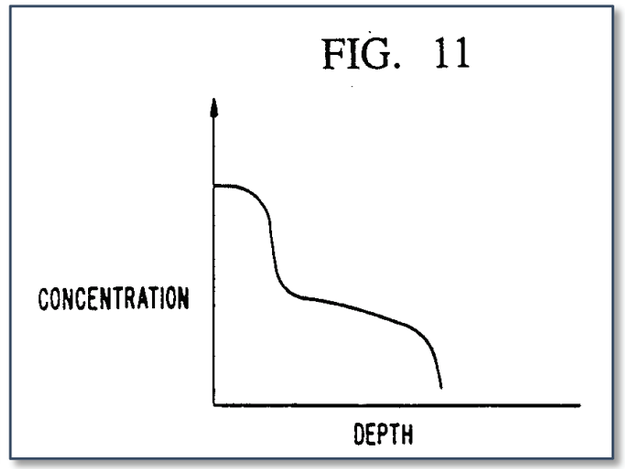
- There is no evidence that carriers move from the surface to the substrate.

1. A VLSI semiconductor device, comprising:
a substrate of a first doping type at a first doping level having a surface;
a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region;
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

-01242: Ex. 1001 ('222 pat.) at 4:38-62



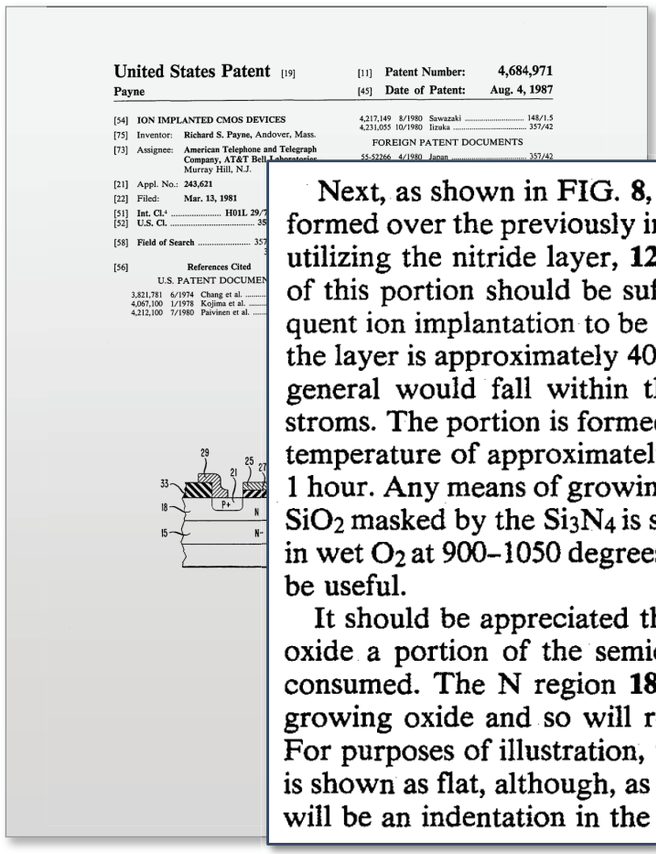
-01244: Ex. 1005 (Payne) at Fig. 10



-01244: Ex. 1005 at Fig. 11

-01244: Ground 1; Element 44.5

- Payne <u>never</u> mentions carriers, much less moving carriers from the surface to the substrate.



United States Patent [19]
Payne

[11] Patent Number: 4,684,971
[45] Date of Patent: Aug. 4, 1987

[54] ION IMPLANTED CMOS DEVICES
[75] Inventor: Richard S. Payne, Andover, Mass.
[73] Assignee: American Telephone and Telegraph Company, AT&T Bell Laboratories, Murray Hill, N.J.
[21] Appl. No.: 243,621
[22] Filed: Mar. 13, 1981
[51] Int. Cl.[4] H01L 29/7
[52] U.S. Cl. 35
[58] Field of Search 357
[56] References Cited
U.S. PATENT DOCUMEN
3,821,781 6/1974 Chang et al. .....
4,067,100 1/1978 Kojima et al. .....
4,212,100 7/1980 Paviinen et al. .....
4,217,149 8/1980 Sawazaki 148/1.5
4,231,055 10/1980 Iizuka 357/42
FOREIGN PATENT DOCUMENTS
55-52266 4/1980 Japan 357/42

Next, as shown in FIG. **8**, a thick oxide portion **19** is formed over the previously implanted regions **18** and **15** utilizing the nitride layer, **12**, as a mask. The thickness of this portion should be sufficient to block the subsequent ion implantation to be described. In this example, the layer is approximately 4000 Angstroms thick, but in general would fall within the range 3000–4500 Angstroms. The portion is formed by heating in wet O_2 at a temperature of approximately 1000 degrees Celsius for 1 hour. Any means of growing the requisite thickness of SiO_2 masked by the Si_3N_4 is suitable. Typically, heating in wet O_2 at 900–1050 degrees Celsius for 1–4 hours will be useful.

It should be appreciated that in the formation of the oxide a portion of the semiconductor surface will be consumed. The N region **18** will diffuse ahead of the growing oxide and so will remain at the new surface. For purposes of illustration, the semiconductor surface is shown as flat, although, as a result of oxidation, there will be an indentation in the area of the N tub.

-01244: Ex. 1005 (Payne) at 4:38-59

a separate step is not ordinarily needed. The resulting impurity profile in both tubs thereby has the general shape illustrated in FIG. **11**, where the abscissa is depth and the ordinate is impurity concentration.

The oxide layer can then be stripped off, for example, with a solution of dilute HF, and fabrication may proceed in accordance with standard techniques to produce the CMOS device depicted in FIG. **10**. The p-channel device includes source and drain regions, **21** and **22**, respectively, of P^+ conductivity type formed with the N surface region, **18**. Similarly, the n-channel device includes source and drain regions, **23** and **24**, of N^+ conductivity type formed within the P surface region **20**. These source and drain regions would typically have a surface impurity concentration of approximately 10^{19}–10^{20} ions/cm^3 and a depth of 1 μm. It will be noted, therefore, that the n and p surface regions, **18** and **20**, will be present at the surface of their respective devices except for the areas comprising the source and drain. The depth of the surface regions should be at least as great as that of the source and drain regions.

The devices further include gate electrodes, **25** and **26**, typically comprising polycrystalline silicon, formed over gate oxide portions **27** and **28**. Ohmic contacts to source and drain regions are provided by metal portions, **29–32**, typically comprising aluminum, formed over field oxide portions **33–35** and contact windows in said oxide. These features and their method of fabrication are well-known in the art and consequently are not discussed in detail.

It will be appreciated that during the drive-in of the source and drain regions, **21–24**, the regions **18**, and **20** will also be driven somewhat further into the substrate, while the depth of the tubs **15** and **17** is essentially unaffected. In a typical device, the final depth of surface regions **18** and **20** would be approximately 1–2μ and the depth of tub regions **15** and **17** would be typically 3–8μ. The surface impurity concentration of the surface regions is typically $0.5–5 \times 10^{16}$ ions/cm^3 and that of the tub regions is typically 10^{15}–10^{16} ions/cm^3, with the former concentration being at least twice as much as the latter over these ranges.

The major advantage in formation of the high-low implant profile of FIG. **11** is illustrated in FIGS. **12** and

-01244: Ex. 1005 at 5:14-57

device. In a device fabricated in accordance with the present invention, as illustrated in FIG. **13**, the composite profiles remain high and then fall off rapidly at a much closer distance from the boundary. This is due to the high impurity concentration of surface regions **18** and **20** as well as the short diffusion lengths of these regions. On each side of the boundary, therefore, the high impurity concentration of the surface region (e.g., **18**) is compensated for only by the low concentration tub region of the adjacent device (**17**) and substantial overlap is permitted. In a typical device, it is expected

-01244: Ex. 1005 at 6:7-17

-01244: Ground 1; Element 44.5



"[A]nticipation by inherent disclosure is appropriate only when the reference discloses prior art that ***must necessarily include the unstated limitation***."

Transclean Corp. v. Bridgewood Servs., Inc., 290 F.3d 1364, 1373 (Fed. Cir. 2002)

-01244: Ground 1; Element 44.5

- Dr. Blalock admitted the force depends on the slope, and that he did not calculate the slope for any of the references.

Q. How do you know the magnitude of the force a dopant concentration puts on carriers?

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-01244: Ex. 2058 at 89:3-10

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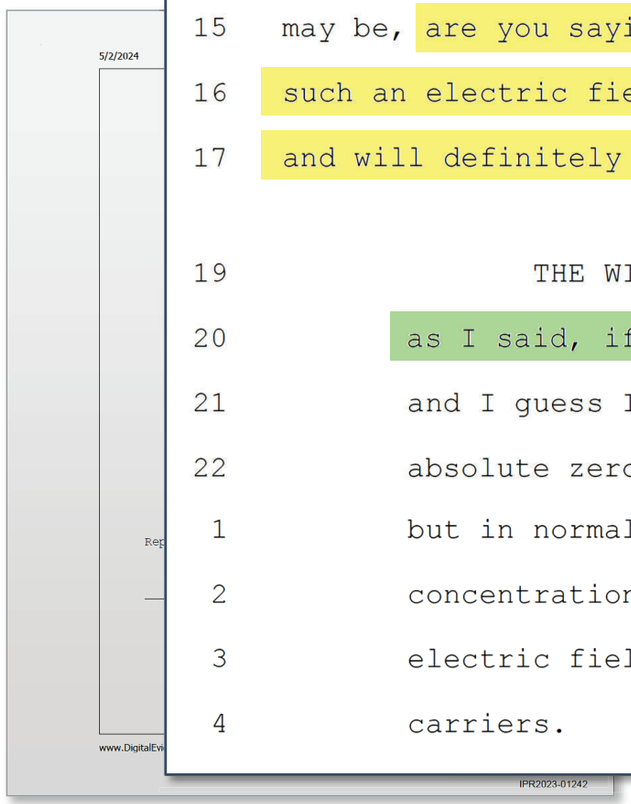
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THE WITNESS: As I've said, the patent owner tells us that that's sufficient, so that's what I did. I have not done calculations of the slope per se.

-01244: Ex. 2058 (Blalock Dep. Tr.) at 195:8-16

-01244: Ground 1; Element 44.5

- Dr. Blalock admitted that an electric field does <u>not</u> always move carriers.



Q. I'm saying apart from what the patent owner said and whatever your interpretation of that may be, are you saying that as a matter of physics, such an electric field will definitely be created and will definitely move carriers?

* * *

THE WITNESS: I mean, it depends on -- as I said, if there are no other fields -- and I guess I should qualify for not an absolute zero temperature, all this stuff, but in normal circumstances, if you have a concentration gradient, it will result in an electric field, which will then act on the carriers.

Q. So you mentioned that if there aren't other fields present and the carrier was introduced into that field, you'll move the carrier.

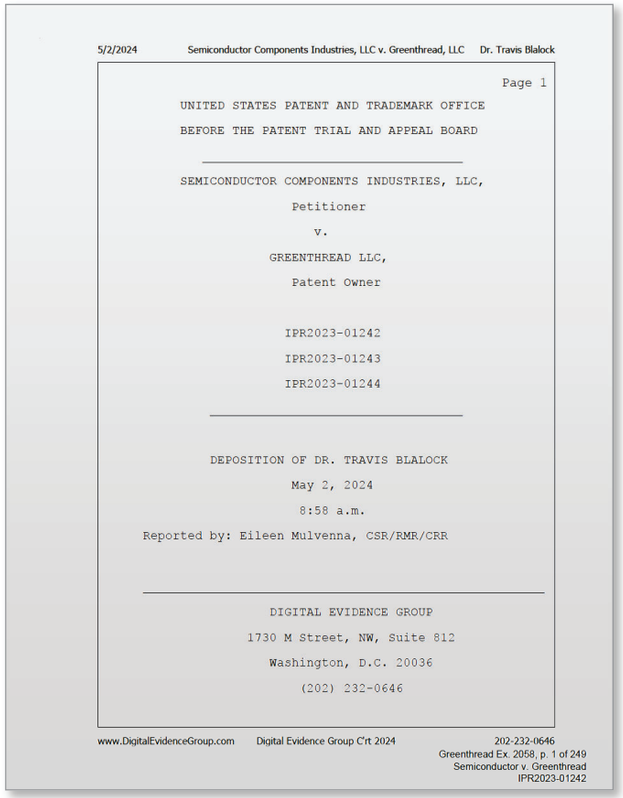
Where could other fields come from?

A. Externally applied voltages from the circuit, if the structure's in a circuit, things like that. Or I suppose some environmental effect. I don't know.

Ex. 2058 (Blalock Dep. Tr.) at 131:13-132:13

-01244: Ground 1; Element 44.5

- Dr. Blalock also admitted that there may be a force that is <u>larger</u> than the gradient force.



5/2/2024 Semiconductor Components Industries, LLC v. Greenthread, LLC Dr. Travis Blalock

Page 1

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IPR2023-01242
IPR2023-01243
IPR2023-01244

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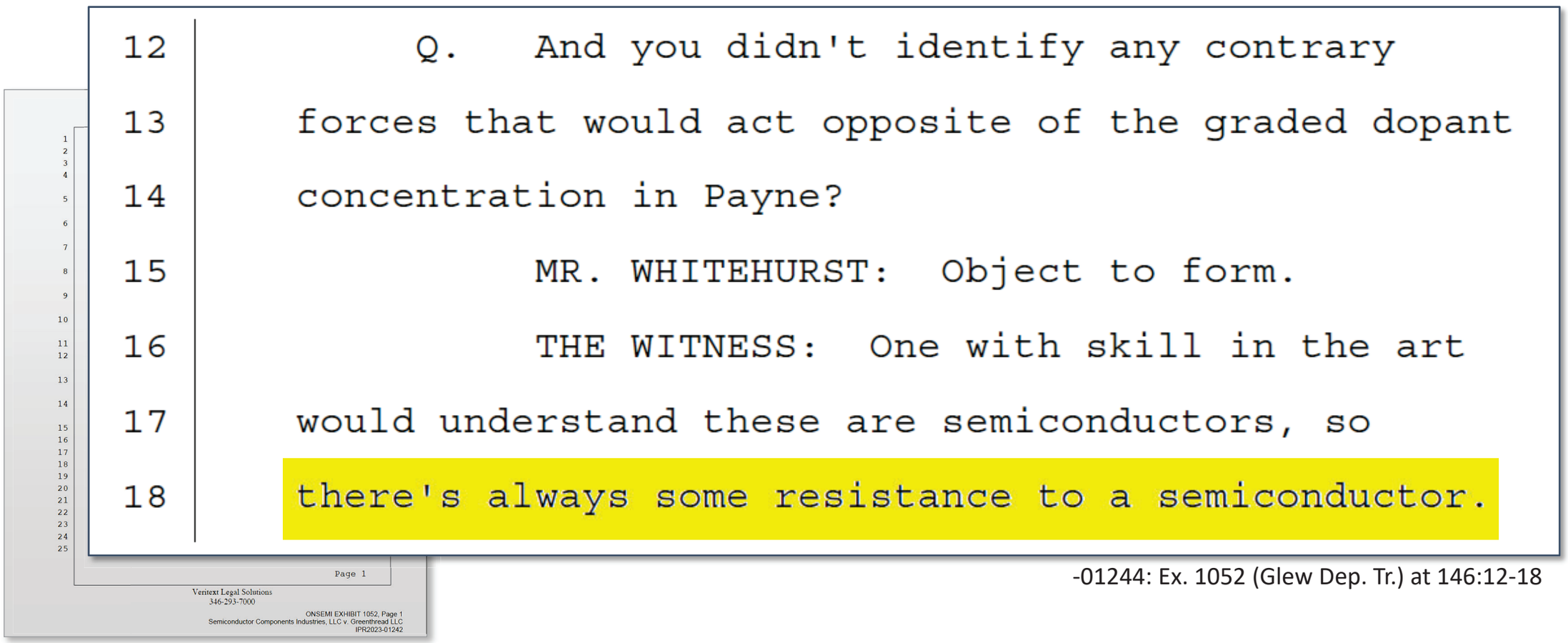
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7 But there will be a force -- that
8 mechanism, the gradient mechanism which
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-01244: Ex. 2058 (Blalock Dep. Tr.) at 137:17-138:11

-01244: Ground 1; Element 44.5

- An electric field does not necessarily overcome the resistance of the semiconductor.



Q. And you didn't identify any contrary forces that would act opposite of the graded dopant concentration in Payne?

MR. WHITEHURST: Object to form.

THE WITNESS: One with skill in the art would understand these are semiconductors, so there's always some resistance to a semiconductor.

Page 1

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ONSEMI EXHIBIT 1052, Page 1
Semiconductor Components Industries, LLC v. Greenthread LLC
IPR2023-01242

-01244: Ex. 1052 (Glew Dep. Tr.) at 146:12-18

Summary

- **"Aid carrier movement"**
  - **"Graded dopant concentration" does not necessarily "aid carrier movement."**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
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- **Petitioner's Wieczorek grounds fail**
- **Petitioner's Payne ground fails**
- **Substantial evidence of objective indicia of non-obviousness**
- Petitioner has not shown that the Petitions are timely

Objective Indicia of Non-Obviousness



"Objective evidence of nonobviousness … may often be the most probative and cogent evidence in the record. It may often establish that an invention appearing to have been obvious in light of the prior art was not."

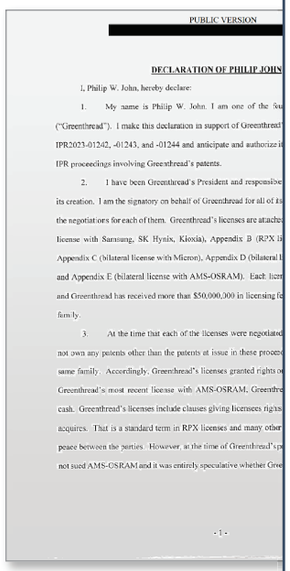
* * *

"[L]icenses with companies under no apparent threat of litigation" are especially probative of non-obviousness.

Transocean Offshore Deepwater Drilling, Inc. v. Maersk Drilling USA, Inc., 699 F.3d 1340, 1349, 1353 (Fed. Cir. 2012)

Objective Indicia of Non-Obviousness

- Two semiconductor companies took licenses without any threat of litigation.
- There is no evidence that these companies took a license to save litigation costs.
- The license was for the entire patent family and all of the patents involved graded dopant concentrations.


PUBLIC VERSION

DECLARATION OF PHILIP JOHN

I, Philip W. John, hereby declare:

1. My name is Philip W. John. I am one of the fou
("Greenthread"). I make this declaration in support of Greenthread
IPR2023-01242, -01243, and -01244 and anticipate and authorize it
IPR proceedings involving Greenthread's patents.

2. I have been Greenthread's President and responsible
its creation. I am the signatory on behalf of Greenthread for all of its
the negotiations for each of them. Greenthread's licenses are attache
license with Samsung, SK Hynix, Kioxia), Appendix B (RPX li
Appendix C (bilateral license with Micron), Appendix D (bilateral l
and Appendix E (bilateral license with AMS-OSRAM). Each licen
and Greenthread has received more than $50,000,000 in licensing fe
family.

3. At the time that each of the licenses were negotiated
not own any patents other than the patents at issue in these proceed
same family. Accordingly, Greenthread's licenses granted rights o
Greenthread's most recent license with AMS-OSRAM, Greenthre
cash. Greenthread's licenses include clauses giving licensees rights
acquires. That is a standard term in RPX licenses and many other
peace between the parties. However, at the time of Greenthread's sp
not sued AMS-OSRAM and it was entirely speculative whether Gree

- 1 -

4. Greenthread has never threatened litigation—implicitly, explicitly, or otherwise—against [redacted] or any of their affiliates.

5. In 2020, after Greenthread sued Samsung for infringing Greenthread's patents, RPX Corp. ("RPX") approached Greenthread to negotiate a license on behalf of some of its members, including [redacted] Greenthread and RPX negotiated a license to RPX (Appendix A) which gave RPX the right to sublicense those companies to the Greenthread family of patents and which I understand RPX did in fact grant to them.

-01242: Ex. 2072 (John Decl.) at 2

Objective Indicia of Non-Obviousness

- Intel, Sony, Micron, and Western Digital have also licensed the patents.

EXHIBIT E

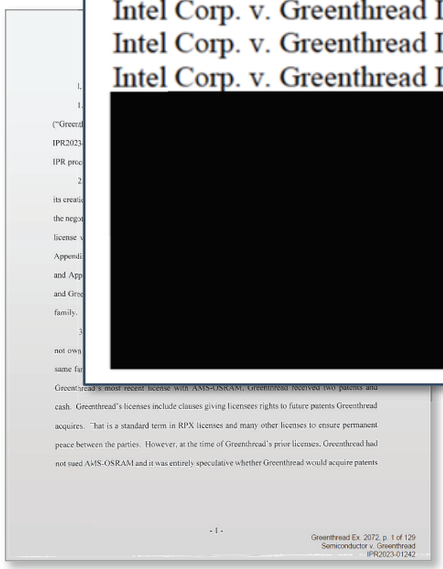
LICENSEE NULLITY PROCEEDINGS AND LICENSOR LITIGATIONS

Greenthread, LLC v. Intel Corporation, 22-cv-02001-JR (D. Or.)

[redacted]

Intel Corp. v. Greenthread LLC, IPR2023-00260
Intel Corp. v. Greenthread LLC, IPR2023-00308
Intel Corp. v. Greenthread LLC, IPR2023-00386
Intel Corp. v. Greenthread LLC, IPR2023-00420
Intel Corp. v. Greenthread LLC, IPR2023-00541
Intel Corp. v. Greenthread LLC, IPR2023-00548
Intel Corp. v. Greenthread LLC, IPR2023-00552

[redacted]



-01242: Ex. 2072 at 55

EXHIBIT D – LITIGATION

Greenthread, LLC v. Micron Technology, Inc. et al., 23-cv-00333 (D. Del.)

-01242: Ex. 2072 at 81

EXHIBIT D – LITIGATION

Greenthread, LLC v. Western Digital Corporation et al., 1:23-cv-00326-RGA (D. Del.)

-01242: Ex. 2072 at 101

GREENTHREAD-AMS-OSRAM SETTLEMENT

EXHIBIT D – LITIGATION and IPRs

Greenthread, LLC v. OSRAM GmbH et al., 2:23-cv-00179-JRG (E.D. Tex.)

IPR2024-00001, IPR2024-00016, IPR2024-00017, IPR2024-00018, IPR2024-00019, IPR2024-00020, IPR2024-00021 and all other proceedings challenging the validity of a Licensed Patent.

-01242: Ex. 2072 (John Decl.) at 122

Objective Indicia of Non-Obviousness



"Appreciation by contemporaries skilled in the field of the invention is a useful indicator of whether the invention would have been obvious…"

Vulcan Eng'g Co. v. Fata Aluminum, Inc., 278 F.3d 1366, 1373 (Fed. Cir. 2002)

Summary

- **"Aid carrier movement"**
  - **"Graded dopant concentration" does not necessarily "aid carrier movement."**
  - **Petitioner has presented no evidence that carriers move from the surface to the substrate.**
  - **Petitioner introduced a new and incorrect claim construction in its Reply.**
  - **All of the grounds in all of the petitions must be dismissed for lack of evidence.**
- **Petitioner cannot rely on inherency for "aid carrier movement"**
  - **Petition never mentions inherency**
  - **There is no evidence carriers necessarily move from the surface to the substrate**
- **Petitioner's Kawagoe grounds fail**
  - **Kawagoe does not aid carrier movement from active region (or surface) to substrate**
  - **Petition does not identify a "second doping type opposite in conductivity"**
- **Petitioner's Wieczorek grounds fail**
- **Petitioner's Payne ground fails**
- **Substantial evidence of objective indicia of non-obviousness**
- **Petitioner has not shown that the Petitions are timely**

Petitions are Untimely

Since it is well established that customer-manufacturer relationships can create privity, Petitioner's admission that those relationships exist is ***"some evidence" that it is in privity with them***.

Worlds Inc. v. Bungie, Inc., 903 F.3d 1237, 1242-44 (Fed. Cir. 2018)