UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC and TEXAS INSTRUMENTS INCORPORATED,

Petitioner,

v.

GREENTHREAD, LLC,

Patent Owner

IPR2023-01242[1]
Patent 11,121,222

PETITIONER'S UPDATED EXHIBIT LIST

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[1] Texas Instruments Incorporated, which filed a petition in IPR2024-00673, has been joined as a petitioner in this proceeding.

EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 11,121,222 to Rao (the "'222 Patent")
1002	Prosecution History of the '222 Patent
1003	Declaration of Travis Blalock, PhD
1004	Curriculum Vitae of Travis Blalock, PhD
1005	Publication Declaration of Sean O'Bryan for Maziasz ("O'Bryan Decl.")
1006	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek")
1007	U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe")
1008A	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol 1, Lattice Press (2000) ("Wolf.1")
1008B	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 2, Lattice Press (2000) ("Wolf.2")
1008C	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 3, Lattice Press (2000) ("Wolf.3")
1008D	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 4, Lattice Press (2000) ("Wolf.4")
1009	Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang")
1010	U.S. Patent No. 4,481,522 ("Jastrzebski")
1011	Publication Declaration of Martin L. Knott for Rabaey ("Knott Decl.")
1012	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 ("Resnick Decl.")
1013	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 ("Watters Decl.")
1014	U.S. Patent No. 6,163,877 ("Gupta")
1015	U.S. Patent No. 6,534,805 ("Jin")
1016	Excerpts from the Prosecution History of U.S. Patent No. 8,421,195 (the "'195 Patent")
1017	Patent Owner's Proposed Constructions
1018	Defendants' Preliminary Proposed Constructions
1019	Defendants' Opening Claim Construction Brief
1020	Patent Owner's Responsive Claim Construction Brief
1021	Defendants' Reply Claim Construction Brief

Exhibit No.	Description
1022	Sze, *Semiconductor Devices Physics and Technology*, 2d Ed., John Wiley & Sons (2002)
1023	Maziasz and Hayes, *Layout Minimization of CMOS Cells*, Kluwer Academic Publishers (1992) ("Maziasz")
1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics, dated March 31, 2023
1025	Rabaey *et al.*, *Digital Integrated Circuits, A Design Perspective,* Prentice Hall Electronics and VLSI Series (2003) ("Rabaey")
1026	Gregory and Shafer, "Latch-Up In CMOS Integrated Circuits," IEEE Transactions on Nuclear Science, Volume 20, Issue 6 (1973)
1027	U.S. Patent Application Publication No. 2007/0045682 to Hong *et al*. ("Hong")
1028	Excerpts from the Prosecution History of U.S. Patent Application No. 10/934,915 (the "'915 App.")
1029	Excerpts from the Prosecution History of U.S. Patent No. 9,190,502 (the "'502 Patent")
1030	Excerpts from the Prosecution History of U.S. Patent Application No. 13/854,319 (the "'319 App.")
1031	U.S. Patent No. 4,160,985 to Kamins *et al.* ("Kamins")
1032	McGraw-Hill Dictionary of Scientific and Technical Terms (2003)
1033	U.S. Patent No. 9,647,070 to Rao (the "'070 Patent")
1034	U.S. Patent Application Publication No. 2003/0030488 to Hueting *et al.* ("Hueting")
1035	[Intentionally Omitted]
1036	Proposed Claim Constructions in the Intel Litigation
1037	Howe and Sodini, *Microelectronics, An Integrated Approach*, Prentice Hall Electronics and VLSI Series (1997) ("Howe")
1038	Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits In Deep Submicron Technology,* 3rd Ed., McGraw-Hill (2004) ("Hodges")
1039	Publication Declaration of Martin L. Knott for Hodges ("Knott Decl.")
1040	Jaeger, *Microelectronic Circuit Design*, McGraw-Hill (1997) ("Jaeger")
1041	Kang and Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, McGraw-Hill (2003) ("Kang")

Exhibit No.	Description
1042	U.S. Patent No. 6,614,560 ("Silverbrook")
1043	Publication Declaration of Sylvia Hall-Ellis for Wolf
1044	Wong, H. P., et al. "CMOS active pixel image sensors fabricated using a 1.8-V, 0.25-µm CMOS technology." IEEE Transactions on Electron Devices 45.4 (1998): 889-894.
1045	Law360 Article "Stays Pending IPR In Del. District Courts Are Here To Stay," Kraning and Del Dotto, March 11, 2022.
1046	E-mail from Nicholas T. Matich on October 11, 2023 at 5:31 PM.
1047	E-mail from Nicholas T. Matich on October 12, 2023 at 12:09 AM.
1048	Greenthread's Second Amended Complaint in *Greenthread, LLC v. Dell Inc., Dell Technologies, Inc., Sony Group Corporation, Sony Semiconductor Solutions Corp., Sony Semiconductor Manufacturing Corp., Sony Mobile Communications, Inc., Sony Interactive Entertainment Inc., Sony Interactive Entertainment LLC, Sony Corporation of America, and Sony Electronics Inc.*, Civil Action No. 6:22-cv-105-ADA, filed January 23, 2023.
1049	Greenthread's First Amended Complaint in *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.*, Civil Action No. 6:22-cv-105-ADA, filed April 29, 2022.
1050	Joint Motion to Stay All Deadlines and Notice of Settlement in *Greenthread, LLC v. Intel Corporation*, Civil Action No. 3:22-cv-2001-JR, filed April 12, 2023.
1051	RPX FAQs
1052	Transcript of Deposition of Alexander Glew, PHD in IPR2023-01242, -01243, -01244
1053	Transcript of Deposition of Philip John in IPR2023-01242, -01243, -01244
1054	Office Action Response, dated August 1, 2024, in U.S. Patent Application No. 17/728,588
1055	Declaration of Douglas Holberg, dated August 1, 2024, in U.S. Patent Application No. 17/728,588
1056	Petitioner's Hearing Demonstratives
1057	Transcript of Conference Call on May 01, 2025

Dated: May 08, 2025

Respectfully submitted,
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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 8th day of May 2025, **PETITIONER'S UPDATED EXHIBITS LIST AND EXHIBIT 1057** was served by email on the following counsel for Patent Owner and the Joined Petitioner:

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