UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELL TECHNOLOGIES INC. AND DELL INC.,

Petitioners,

v.

GREENTHREAD LLC,

Patent Owner.

Case: IPR2023-00509

U.S. Patent No. 11,121,222

PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

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1004	Curriculum Vitae of Travis Blalock, PhD
1005	Publication Declaration of Sean O'Bryan for Maziasz ("O'Bryan Decl.")
1006	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek")
1007	U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe")
1008A	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol 1, Lattice Press (2000) ("Wolf.1")
1008B	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 2, Lattice Press (2000) ("Wolf.2")
1008C	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 3, Lattice Press (2000) ("Wolf.3")
1008D	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 4, Lattice Press (2000) ("Wolf.4")
1009	Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang")
1010	U.S. Patent No. 4,481,522 ("Jastrzebski")
1011	Publication Declaration of Martin L. Knott for Rabaey ("Knott Decl.")

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1022	Sze, Semiconductor Devices Physics and Technology, 2d Ed., John Wiley & Sons (2002)
1023	Maziasz and Hayes, Layout Minimization of CMOS Cells, Kluwer Academic Publishers (1992) ("Maziasz")
1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics, per Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation" at n.4, dated June 21, 2022
1025	Rabaey et al., Digital Integrated Circuits, A Design Perspective, Prentice Hall Electronics and VLSI Series (2003) ("Rabaey")

1026	Gregory and Shafer, "Latch-Up In CMOS Integrated Circuits," IEEE Transactions on Nuclear Science, Volume 20, Issue 6 (1973)
1027	U.S. Patent Application Publication No. 2007/0045682 to Hong et al. ("Hong")
1028	Excerpts from the Prosecution History of U.S. Patent Application Publication No. 10/934,915 (the "'915 App.")
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1031	U.S. Patent No. 4,160,985 to Kamins et al. ("Kamins")
1032	McGraw-Hill Dictionary of Scientific and Technical Terms (2003)
1033	U.S. Patent No. 9,647,070 to Rao (the "'070 Patent")
1034	U.S. Patent Application Publication No. 2003/0030488 to Hueting et al. ("Hueting")
1035	Patent Owner's August 29, 2022 Amended Preliminary Infringement Contentions in the District Court Case
1036	Proposed Claim Constructions in the District Court Case
1037	Howe and Sodini, Microelectronics, An Integrated Approach, Prentice Hall Electronics and VLSI Series (1997) ("Howe")
1038	Hodges et al., Analysis and Design of Digital Integrated Circuits In Deep Submicron Technology, 3rd Ed., McGraw-Hill (2004) ("Hodges")
1039	Publication Declaration of Martin L. Knott for Hodges ("Knott Decl.")

1040	Jaeger, Microelectronic Circuit Design, McGraw-Hill (1997) ("Jaeger")
1041	Kang and Leblebici, CMOS Digital Integrated Circuits Analysis and Design, McGraw-Hill (2003) ("Kang")
1042	Redacted District Court Case Transfer Order
1043	Order Cancelling Markman Hearing

Dell Technologies Inc. and Dell Inc. ("Petitioners" or "Dell") request *inter partes* review ("IPR") of claims 1-9, 13-18, 20-28, 32-36, and 38-42 (the "Challenged Claims") of U.S. Patent No. 11,121,222 (Ex.1001, "the '222 Patent").

I. INTRODUCTION

The '222 Patent is directed to a semiconductor device having a graded dopant concentration in its active/well region(s) to aid carrier movement. Ex.1001, Claim 1. This Petition demonstrates that the Challenged Claims are unpatentable.

II. MANDATORY NOTICES

A. Real Party in Interest

Dell Technologies Inc. and Dell Inc. ("Petitioners" or "Dell") are the real parties-in-interest.[1]

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[1] Certain suppliers of components of products at issue in the district court litigation are obligated to indemnify Dell against claims asserted in that litigation. However, none of these suppliers have directed, controlled, funded, reviewed, participated in, or otherwise influenced Dell's IPR petition. For at least these reasons, Dell does not believe that these suppliers constitute real parties in interest. Furthermore, none of those suppliers are currently statutorily barred or estopped from filing an IPR petition directed to this patent.

B. Related Matter

The following litigation or *inter partes* reviews related to the ’222 Patent are pending:

- *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.,* Civil Action No. 6:22-cv-105 in the Western District of Texas (“District Court Case”), filed January 27, 2022;
- *Intel Corporation v. Greenthread LLC*, IPR2023-00420, filed December 28, 2022;
- *Sony Group Corporation v. Greenthread, LLC,* IPR2023-00324, filed December 12, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 3-22-cv-02001 in the District of Oregon, filed December 29, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6-22-cv-01293 in the Western District of Texas, filed December 21, 2022.

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D. 37 C.F.R. §42.8(b)(4): Service Information

Dell concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email addresses: Dell-Greenthread@alston.com; and christopher.douglas@alston.com.

III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 160605. Review of 33 claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the ’222 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Prior Art Printed Publications

The ’222 Patent claims priority to September 3, 2004.[2] Petitioner’s challenge is based on the following prior-art references, none of which were discussed by the Patent Office during prosecution of the ’222 Patent:

- U.S. Patent No. 6,043,114 to Kawagoe *et al.* (“Kawagoe”) (Ex.1007) issued March 28, 2000 and is prior art under §102(b).[3]
- U.S. Patent Application Publication 2003/0183856 to Wieczorek *et al.* (“Wieczorek”) (Ex.1006) was filed October 29, 2002 and published October 2, 2003. Wieczorek is prior art under §§102(a), (e).
- Stanley Wolf and Richard N. Tauber, *Silicon Processing for the VLSI Era*, Lattice Press (2000) (“Wolf”) (Exs.1008A-D), was published and publicly available no later than 2002, and is prior art under §102(b). *See* Exs.1012-1013.

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[2] Petitioner reserves the right to challenge the priority date in other proceedings.

[3] Cites to §§102/103 are to the pre-America Invents Act (pre-AIA).

- U.S. Patent No. 6,163,877 to Gupta (Ex.1014) issued December 19, 2000 and is prior art under §102(b).

B. Relief Requested

Petitioner requests cancellation of the Challenged Claims as unpatentable under 35 U.S.C. §103. The specific grounds of the challenge are set forth below and are supported by the declaration of Dr. Blalock (Ex.1003).

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-9, 13-14, 16-18, 20-21, 23-28, 32-36, and 38-42	Kawagoe
II	§103	1-2, 4-9, 13-18, 20-23, 25-28, 32-36, and 38-42	Wieczorek, Wolf
III	§103	1-9, 13-14, 16-18, 20-21, 23-28, 32-36, and 38-42	Kawagoe, Gupta
IV	§103	1-2, 4-9, 13-18, 20-23, 25-28, 32-36, and 38-42	Wieczorek, Wolf, Gupta

VI. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") of the subject matter of the '222 Patent would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Ex.1003, ¶49. Additional education might compensate for a deficiency in experience, and vice-versa. *Id.*

VII. CLAIM CONSTRUCTION

Claims in an IPR are construed under *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). Ex.1036 lists District Court Case proposed constructions. Exs.1017-1021.

Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition, as the Challenged Claims are unpatentable under either party's proposed constructions (except for the term "active region ... within which transistors can be formed," which is addressed under Patent Owner's proposed construction). Ex.1003 ¶54.

VIII. SPECIFIC GROUNDS FOR PETITION

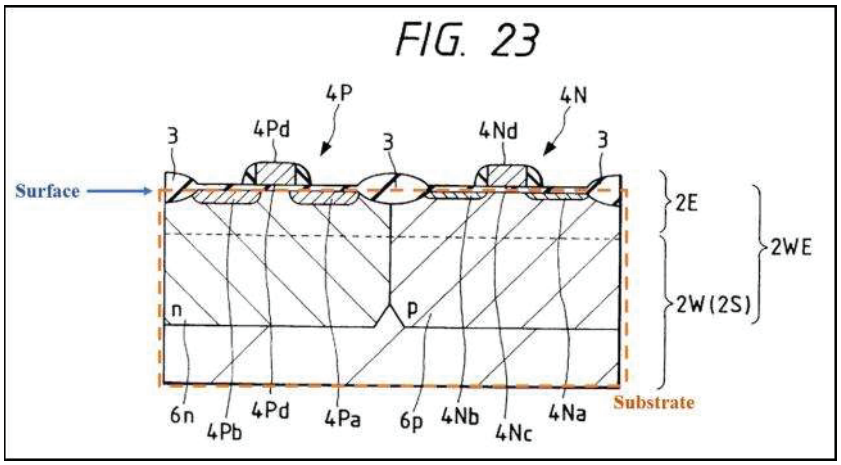
A. Ground I:

Kawagoe renders claims 1-9, 13-14, 16-18, 20-21, 23-28, 32-36, and 38-42 obvious. Ex.1003, ¶¶65-135.

1. Claims 1/21/39/41/42

a. Preambles: "A [VLSI] semiconductor device, comprising:"[4]

To the extent the preamble is limiting, Kawagoe is directed to a "semiconductor integrated circuit device." Ex.1007, Title, 1:13-23, 14:46-67, FIGS. 16-17/23; Ex.1003, ¶66. Ground I focuses on the CMOS device of Figure 23 (Embodiment 4), fabricated on a uniformly-doped epitaxial substrate taught in Embodiment 1.[5] *See* §VIII.A.1.b.



[4] Bracketed language shows the difference between the claims. Appendix A lists the elements and corresponding language for all Challenged Claims.

[5] Figures 16-17 and 23 are directed to Kawagoe's Embodiment 4. Ex.1007, 14:4660. Figure 23 shows the CMOS structures of Figure 16 without the metal layers not relevant to the claims. Ex.1007, 17:10-18:38; Ex.1003, ¶67.

Ex.1007, FIG. 23.[6]

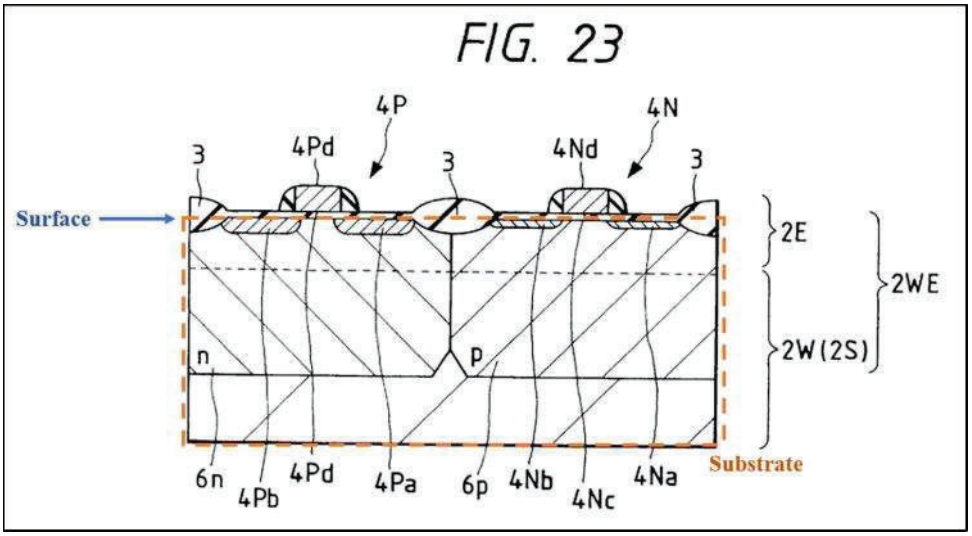
Kawagoe's teachings apply to "VLSI" DRAM, flash memory, and microcomputer devices. *Id.*, 1:24-30; §§VIII.A.1.h, VIII.A.11/12/14. Notably, Kawagoe's teachings apply to multi-Megabit DRAM devices with at least one transistor per memory cell, totaling millions of transistors. Ex.1007, 19:15-18, 20:1-15; Ex.1003, ¶68; Ex.1016, 73 (VLSI refers to "at least one million active elements"). Wolf, which applies to "the VLSI Era," also confirms that such devices at the time were understood to have at least one million active elements. Ex.1008A, cover, xxxiii, FIG. 1 (microprocessor with at least one million transistors); Ex.1008B, 596-597 (1-Megabit CMOS DRAM with one transistor per memory cell), 633-635 (1-Megabit CMOS flash EEPROM with one floating gate per memory cell and other transistors, totaling at least one million active elements); Ex.1003 ¶68.

b. Elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1]: "a substrate of a first doping type at a first doping level [having a surface];"

Kawagoe discloses "semiconductor substrate 2" of a first doping type (p-type) having a silicon "epitaxial layer 2E [] doped with a ***p-type*** impurity such as boron" formed over non-epitaxial "semiconductor substrate body 2S [also] doped with a ***p-***

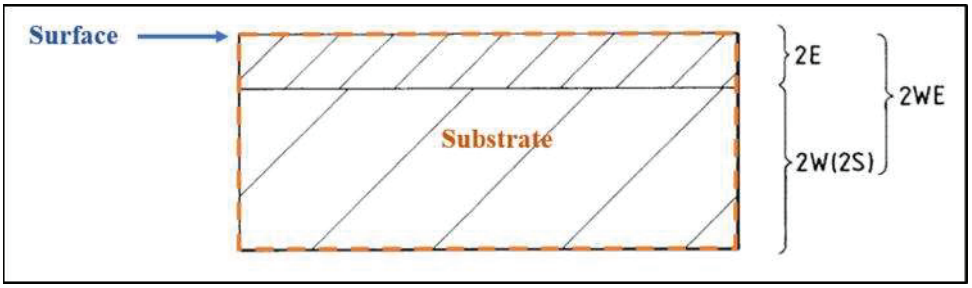
[6] All colors and colored annotations to figures added.

type impurity such as boron....”[6] Ex.1007, 14:61-15:12, 6:50-7:3. The substrate (orange) has a surface, as shown below. Ex.1003, ¶69.



Ex.1007, FIG. 23.

Kawagoe satisfies elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1] under Patent Owner’s plain meaning construction and under Petitioner’s proposed construction because Kawagoe’s epitaxial substrate is the initial material within or on which Kawagoe’s “semiconductor integrated circuit device 1” is later fabricated. Ex.1036; Ex.1007, 6:51-56, 14:61-67, 17:10-18:38; Ex.1003, ¶70.



Ex.1007, FIG. 20. As detailed below, Ground I relies on a uniformly-doped epitaxial substrate in which silicon epitaxial layer 2E of the substrate is doped at the same

level as silicon substrate body 2S, so that the entire substrate in Figure 20 is "at a first doping level" as claimed. Ex.1007, 6:60-7:3; Ex.1003, ¶71.

"at a first doping level" - Kawagoe teaches an epitaxial substrate (2S+2E), illustrated in Figure 20, in which the non-epitaxial silicon substrate body (2S) is either doped at the same or higher level compared to the epitaxial silicon layer (2E). For example, Embodiment 1 describes a uniformly-doped epitaxial substrate in which the "epitaxial layer 2E is doped ... in a concentration ***equal*** to the [concentration] of the semiconductor substrate body 2S, e.g., $1.3x10^{15}$ atoms/cm^3." Ex.1007, 6:60-7:3; *id.*, Abstract (describing "an epitaxial layer which contains an impurity of the ***same*** conduction type [and at] ... the ***same concentration***" as the bulk substrate), 2:57-3:9 (same). This uniformly-doped epitaxial substrate is Kawagoe's "benchmark" substrate repeatedly discussed in other embodiments, including Embodiment 4. Ex.1007, 12:64-65, 13:12-15, 13:66-67, 14:18-20, 15:725. Embodiment 4 introduces an optional latchup-resistant substrate in which "the impurity concentration of the semiconductor substrate body 2S is made ***higher*** than that of the epitaxial layer 2E ... ***to improve*** the resistance to latchup." Ex.1007, 15:13-17; Ex.1003, ¶¶72-73.

A POSITA would have understood that Kawagoe teaches forming Figure 23's twin-well CMOS device (Embodiment 4) on either Embodiment 1's uniformly-doped epitaxial substrate or Embodiment 4's optional latchup-resistant substrate.

Ex.1003, ¶74. Indeed, Kawagoe emphasizes the benefits of Embodiment 1's uniformly-doped epitaxial substrate and explains that the substrate used in Embodiment 4 is formed "***as in the foregoing embodiment 1*** so that... the cost of the semiconductor substrate 2 is lowered to about one half." Ex.1007, 15:7-25. A POSITA would have been motivated to use a uniformly-doped epitaxial substrate to form Figure 23's twin-well CMOS device because this substrate provides "excellent film quality" that "drastically reduce[s] the defect densities of the gate insulating films" and "improve[s] the [device's] performance, reliability and production yield." Ex.1003, ¶75; Ex.1007, 12:8-40; *id*., 15:7-25. This substrate is also easier to manufacture, helping "lower the cost" of the substrate and chip. Ex.1003, ¶75; Ex.1007, 12:8-40. The use of uniformly-doped epitaxial substrate as the starting material in lieu of Embodiment 4's latchup-resistant substrate to form Figure 23's twin-well CMOS devices is a simple substitution of one known element with another known, closely-related element, both of which are described in Kawagoe, and would have been obvious to try because it involves nothing more than choosing one of two ways of doping an epitaxial substrate that are both described in Kawagoe.[7] Ex.1003,

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[7] *Bos. Sci. Scimed, Inc. v. Cordis Corp.,* 554 F.3d 982, 991 (Fed. Cir. 2009) ("Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.").

¶76. Twin-well CMOS devices (illustrated in Figure 23) fabricated on a uniformly-doped epitaxial substrate would have worked for their intended purpose. *Id.*, ¶77. As discussed in Wolf, twin-well CMOS devices were commonly formed over a "***uniform***, lightly doped *p*- or *n*-type substrate" that provides no improved latchup resistance. Ex.1008C, 523; *id.,* 530 ("With the twin-tub [(twin-well)] approach, two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate ..."); Ex.1008B, 387-389; Ex.1007, 2:57-65 (discussing a uniform, "lightly doped" epitaxial substrate).

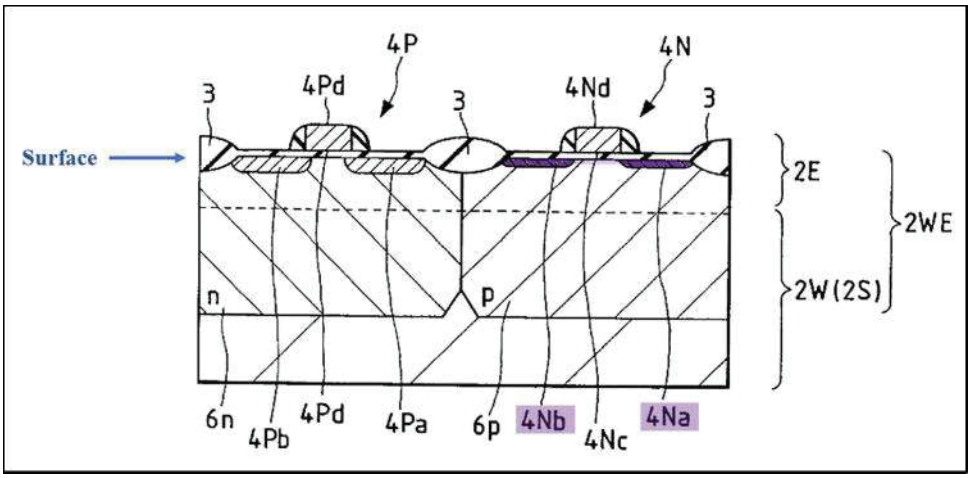
There would be reasonable expectation of success because Kawagoe describes in detail the use of both uniformly-doped epitaxial substrates and latchup-resistant substrates in forming CMOS devices, and repeatedly emphasizes their similarity. Ex.1007, 8:40-52; 12:8-40, 14:58-60, 15:7-12 (substrate), 15:18-25 (epitaxial layer), 15:26-40 (transistors); Ex.1003, ¶78. A uniformly-doped ***epitaxial*** substrate is also better than the bulk (non-epitaxial) substrate commonly used to fabricate twin-well CMOS devices. Ex.1007, 1:33-40 ("The epitaxial wafer is advantageous [compared to bulk wafer/substrate] in that ... the gate insulating film to be formed over the epitaxial layer can have excellent breakdown characteristics to drastically reduce the defect density of the gate insulating film."); *id.*, 12:8-40; Ex.1008B, 387-88 (discussing twin-well CMOS devices fabricated over bulk substrate); Ex.1003, ¶78.

Kawagoe characterizes the improved latchup tolerance provided by Embodiment 4's optional latchup-tolerant substrate as just another "effect[] [that] can be achieved in addition to those of the foregoing embodiment 1." Ex.1007, 19:49-63. Consistent with Kawagoe's teachings, a POSITA would have understood that a uniformly-doped epitaxial substrate is a suitable substrate because, among other benefits, it "drastically reduce[s] the defect densities of the gate insulating films" of CMOS transistors. Ex.1007, 12:8-40 Ex.1003, ¶79. Moreover, a POSITA would have understood that improved latchup resistance is not needed for CMOS chips that are not susceptible to latchup or for which latchup (a "short-circuit" failure condition in poorly designed circuits) is not a concern. Ex.1003, ¶79; Ex.1008B, 406 ("four conditions must exist in a CMOS circuit in order for latchup to occur."); Ex.1026, 1 ("several conditions must be met" to cause latchup). Indeed, twin-well CMOS devices were commonly fabricated on uniformly-doped bulk substrates that provide no improved latchup resistance. Ex.1008B, 387-388 ("With the [twin-well] approach, ... [t]he substrate may be [] a lightly doped wafer ..."); Ex.1003, ¶80. Even if latchup were to remain a concern, a POSITA would have understood that improved latchup resistance can be achieved by other means unrelated to the choice of substrate, such as careful circuit layout. Ex.1003, ¶80; Ex.1008B, 381 ("Latchup tolerance can [] be improved by spacing *n*- and *p*-channel transistors farther apart"),

419 ("Increasing the number of well contacts to VDD reduces latchup susceptibility" and thus "can serve as an alternative approach to improving latchup immunity.").

c. Elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2]: "a first active region disposed adjacent [the/to a] surface [of the substrate] with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed [in the surface thereof];"

Kawagoe discloses "semiconductor regions 4Na and 4Nb ... for forming the ***source-drain regions*** of the nMOS [n-channel transistor] 4N." Ex.1007, 8:66-67; *id*., 3:35-37, 8:46-52, 14:46-55, 15:26-40. Source-drain regions 4Na/4Nb (purple) form part of the claimed first active region, which also includes the channel region (light purple) between source-drain regions 4Na/4Nb and below insulating film 4Nc. *Id.*, 8:46-65, 14:46-55, 15:26-40; Ex.1003, ¶81; Ex.1008B, 299-300 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source*** and ***drain*** regions."), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e). As shown in Figure 23, nMOS transistor 4N is formed in the surface of the first active region, which is adjacent the surface of the substrate. Ex.1003, ¶81.

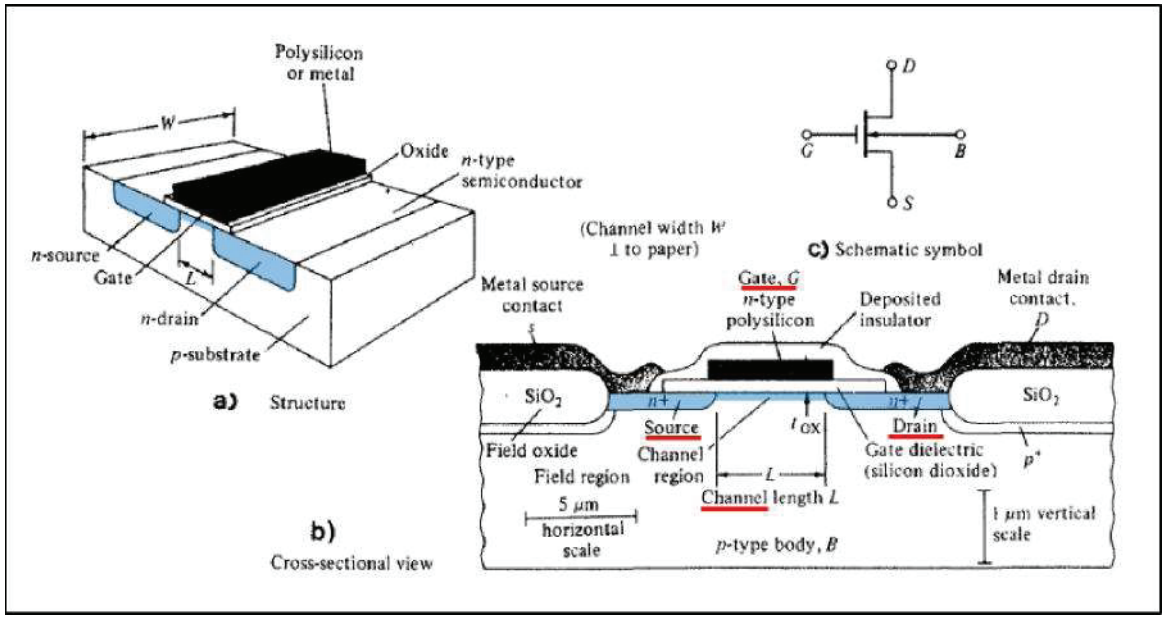


Ex.1007, FIG. 23. "[S]emiconductor regions 4Na and 4Nb are doped with an ***n-type impurity***" and thus have a second doping type (n-type) opposite in conductivity to the first doping type (p-type) of the substrate. *Id.*, 8:67-9:3, 14:46-55, 15:26-40; Ex.1003, ¶81.

While Figure 23 illustrates an exemplary nMOS transistor 4N in the first active region, a POSITA would have understood that Kawagoe teaches forming multiple nMOS transistors in this region to minimize chip area, as good layout practice dictates. Ex.1003, ¶82; Ex.1014, 1:52-54, 2:17-21. Regardless, according to Patent Owner, an "active region .. within which transistors can be formed" means "an active region .. where ***a transistor*** can be formed." Ex.1020, 31.

Kawagoe satisfies elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed" because the active region of a MOS

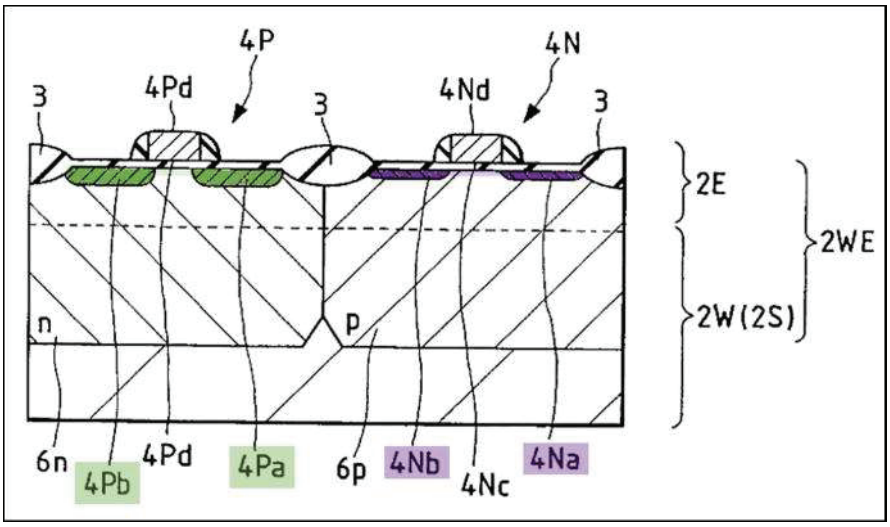
transistor is "[its] channel and [its] heavily doped source and drain regions," highlighted in blue in the figure below. Ex.1036; Ex.1008B, 299; Ex.1003, ¶83.



Ex.1008B, FIG. 5-1; *id*., 298-301, FIGS. 5-2/6-4. Kawagoe also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device" because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Ex.1036; Ex.1008B, 299-301, FIGS. 5-1/5-2; Ex.1008D, 197, FIG. 5-13; Ex.1003, ¶84. Patent Owner does not dispute this. Ex.1020, 3-4 ("when a positive voltage is applied to the gate ... a conductive ***channel*** [is formed] between the ***source*** and the ***drain***, and ***current*** can begin to flow through the transistor").

d. Elements [1.3]/[21.3]/[39.3]/[41.3]/[42.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed [in the surface thereof];"

Kawagoe discloses "semiconductor regions 4Pa and 4Pb ... for forming the source-drain regions of the pMOS [p-channel transistor] 4P." Ex.1007, 3:35-37, 8:46-52, 9:41-48, 15:26-40. Source-drain regions 4Pa/4Pb (green) are part of the claimed second active region, which also includes the channel region (light green) between them and below gate 4Pd. Ex.1007, 8:46-57, 9:41-46, 14:46-55, 15:26-40; Ex.1008B, 299-301, FIGS. 5-1/5-2/6-4; §VIII.A.1.c; Ex.1003, ¶85. As shown in Figure 23, pMOS transistor 4P is formed in the surface of the second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex.1007, 14:46-55; Ex.1003, ¶85. Adjacent active regions are separated by an isolation region (*e.g.*, insulating film 3). Ex.1008A, 818-20, FIG. 16-11(f); Ex.1003, ¶86. Indeed, claim 6 (depends from claim 1) recites, "the first active region and second active region are each separated by at least one isolation region." Ex.1001, Cl. 6.



Ex.1007, FIG. 23.

While Figure 23 illustrates an exemplary pMOS transistor 4P formed in the second active region, a POSITA would have understood that Kawagoe teaches forming multiple pMOS transistors in this region. Ex.1003, ¶87; §VIII.A.1.c. Regardless, according to Patent Owner, an "active region ... within which transistors can be formed" means "an active region ... where ***a transistor*** can be formed." Ex. 1020, 31.

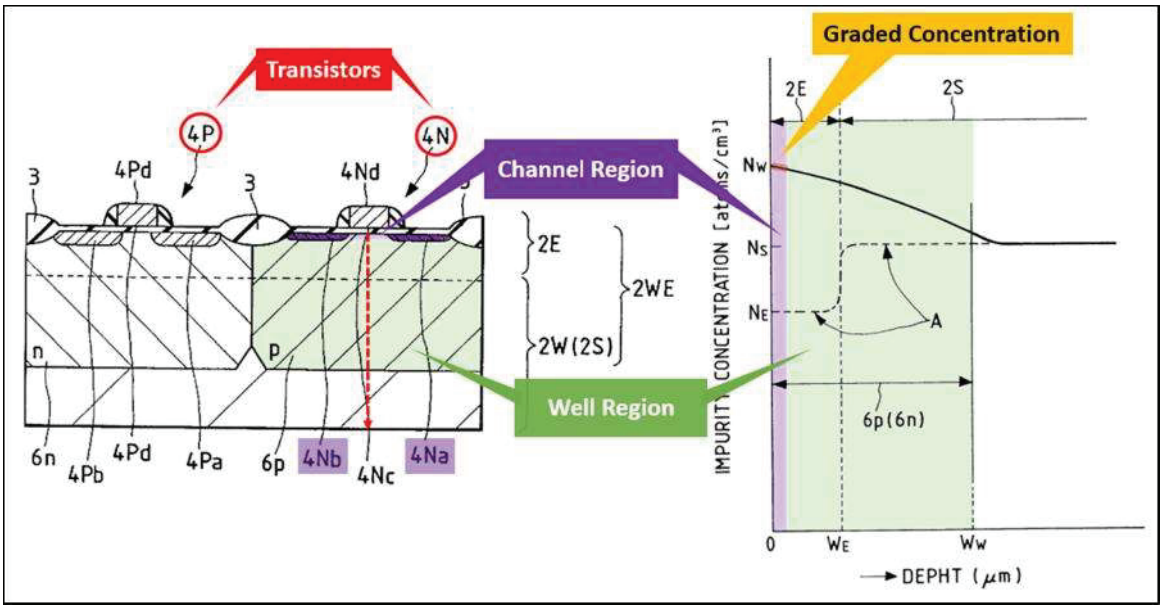
Kawagoe satisfies elements [1.3]/[21.3]/[39.3]/[41.3]/[42.3] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Ex.1003, ¶88; §VIII.A.1.c. Kawagoe also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device." *Id*.

e. Elements [1.4]/[21.4]/[39.4]/[41.4]/[42.4]: "transistors formed in at least one of the first active region or second active region;"

§§VIII.A.1.c-d.

f. Elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5]: "at least a portion of at least one of the first and second active regions having at least one graded [dopant/dopant acceptor/donor dopant] concentration to aid carrier movement from the [first and second active regions/surface/first or second active region] [towards/to] [an area of the substrate/at least one substrate area] where there [are/is] no active region[s]; and"

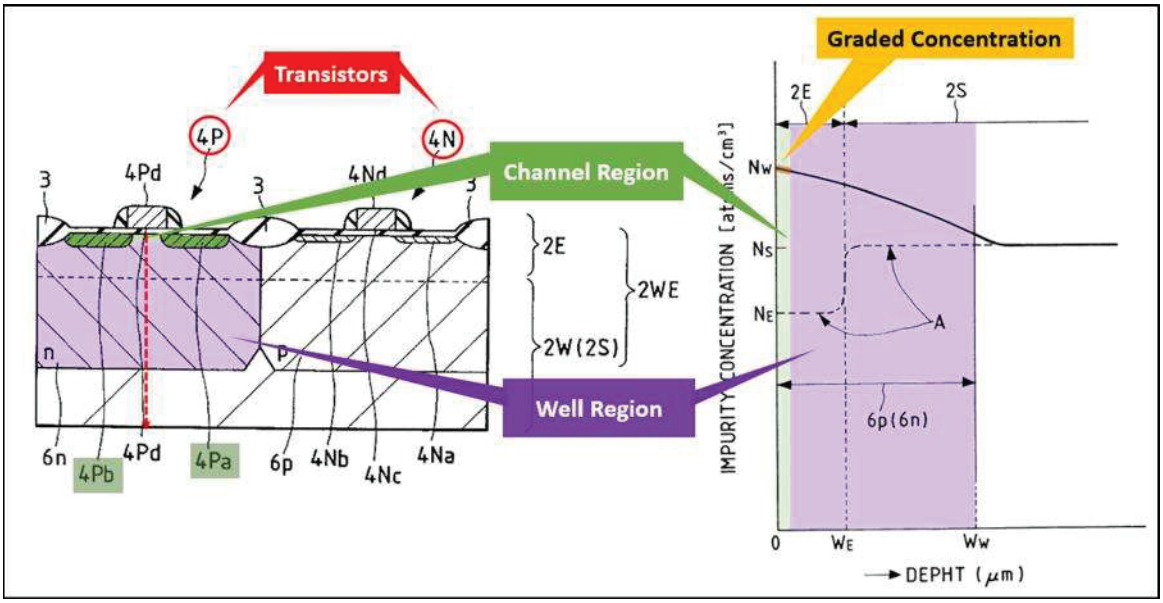
As illustrated in Figure 23 (below left), a channel region (light purple) formed at the top surface of the substrate connects source-drain regions 4Na/4Nb (purple) of transistor 4N. Ex.1008B, 298 ("A channel region in the semiconductor under the gate electrode separates the source and drain"), 300-301 ("When positive bias is applied to an NMOS transistor gate ... an *n*-type ***channel*** connects the ***source*** and ***drain*** regions"), FIG. 5-2; Ex.1007, 8:60-67, 14:46-55, 15:26-30, 15:37-40; Ex.1003, ¶90. Patent Owner does not dispute this. Ex.1020, 4 (the channel is "a thin layer below the surface" connecting the source and drain).



Ex.1007, FIGS. 17/23. Kawagoe's Figure 17 (above right) illustrates the doping concentration measured along the red dotted line in Figure 23 (above left), which starts from the top surface of the substrate (depth=0) and includes the doping profile in the channel region (light purple). *Id.*, 5:41-45. As Figure 17 shows, the dopant concentration is "gradually lowered in the depthwise direction ***from the principal surface*** (having an impurity concentration NW) of the epitaxial layer 2E." *Id.*, 15:6216:40. The dopant concentration is thus graded in the channel region of transistor 4N, which is a portion of the first active region formed at "the principal surface" of epitaxial layer 2E. Ex.1003, ¶91.

The same applies to the channel region of pMOS transistor 4P (a portion of the second active region), as illustrated below. Ex.1007, 15:62-16:2 ("p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise

direction from the principal surface [] of the epitaxial layer 2E."), 9:41-48, 14:4655, 15:32, 15:37-40; Ex.1008B, 298-301, FIGS. 5-2/6-4; Ex.1003, ¶92.



Ex.1007, FIGS. 17/23. Thus, Kawagoe discloses "at least a portion of" the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. Ex.1003, ¶92.

Element [41.5] claims a "graded dopant ***acceptor*** concentration." The graded channel region of Kawagoe's first active region "is doped with a p-type impurity such as boron." Ex.1007, 15:28-29; §VIII.A.9. Boron is an acceptor dopant. Ex.1037, 30; Ex.1003, ¶93. Element [42.5] claims a "graded ***donor*** dopant concentration." The graded channel region of Kawagoe's second active region "is doped with an n-type impurity such as phosphor." Ex.1007, 15:30-32; §VIII.A.9. Phosphor is a donor dopant. Ex.1037, 27; Ex.1003, ¶93.

Kawagoe further explains that such downward-sloping graded dopant concentrations aid the movement of carriers from the first and second active regions towards/to the bottom of substrate where there are no active regions:

> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

Ex.1007, 16:2-11.[8] Dr. Blalock explains that during a so-called single event upset (SEU), an α-ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate. Ex.1003, ¶¶94-95; Ex.1009, 431 ("A[n] [a-]particle can induce SEU when it strikes at the ***channel region*** of an off nMOS transistor ..."), FIG. 2. Kawagoe teaches that those carriers are "attracted to the substrate body by [the] concentration gradient" of the graded dopant concentration illustrated in Figure 17. Ex.1007, 16:2-11.

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[8] Kawagoe states that "electrons produced by the a-ray [are]... prevented from entering the p-well 6*p* ...." Ex.1007, 16:7-9. This refers to electrons produced in the large substrate body below the wells. Ex.1003, ¶94; Ex.1009, FIG. 2.

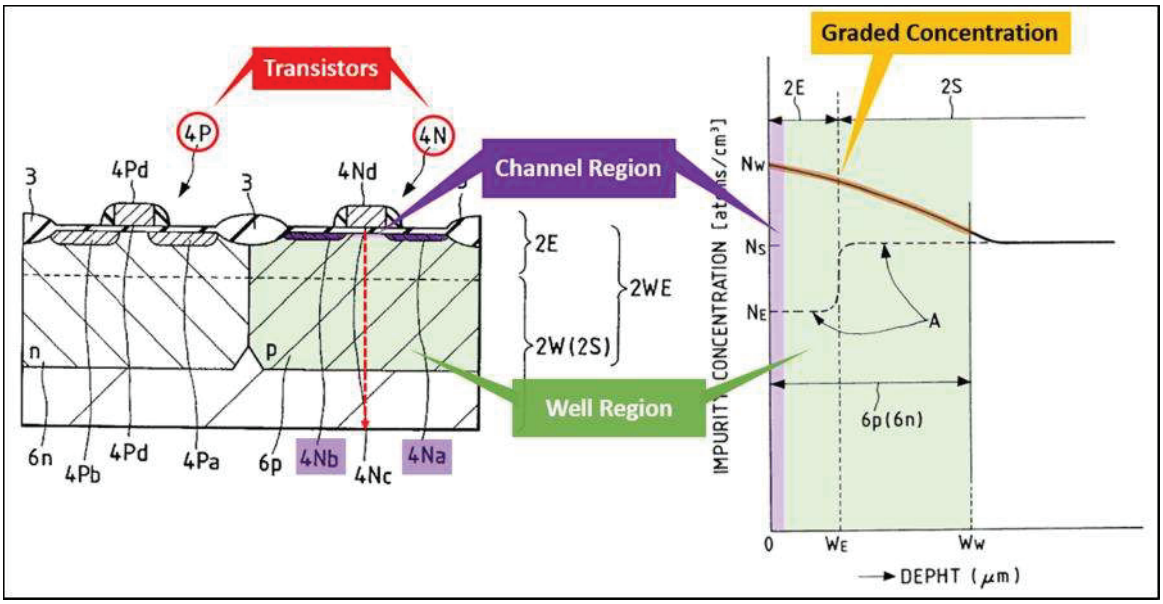
In light of the above, Kawagoe satisfies elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. Ex.1036; Ex.1003, ¶97. According to Patent Owner, the claims make clear that "carriers [must move] in a particular direction (from the surface layer to the substrate)" and "when the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction ...." Ex.1020, 2, 29. Here, Kawagoe's Figure 17 shows that the dopant concentration is downward-sloping with increasing depth towards/to the bottom of the substrate where there are no active regions, and thus, according to Patent Owner (and also in light of Patent Owner's representation to the Patent Office, discussed in §VIII.A.1.g), causes carriers to move deeper into the substrate as well. Ex.1003, ¶97.

Kawagoe also satisfies these claim elements under Petitioner's alternative proposed construction that the term means "to sweep the carriers from the [first and second active regions/surface/first or second active region] [towards/to] [an area of the substrate/at least one substrate area] where there [are/is] no active region[s]." Ex.1036; Ex.1003, ¶98. Notably, Kawagoe's Figure 17 illustrates a downward-sloping graded dopant concentration and Applicant represented to Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in'

unidirectional electric field" that sweeps carriers down into the substrate (where there are no active regions), as detailed below in §VIII.A.1.g. Ex.1016, 289-290; Ex.1003, ¶98.

g. Elements [1.6]/[21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface [towards/to] the area of the substrate where there are no active regions,"

As shown in Figure 23 (below left), Kawagoe discloses "p-well 6p" (light green) adjacent to the first active region (purple/light purple). Ex.1007, 8:66-67, 14:46-55, 15:26-40; Ex.1003, ¶99. And, as discussed above and as shown in the dopant concentration profile (brown) of Figure 17 (below right), the dopant concentration in p-well 6p—measured along the exemplary red dotted line in Figure 23—gradually decreases with depth. §VIII.A.1.f; Ex.1007, 14:46-55, 15:62-16:40 ("p-well 6p and n-well 6n have their impurity concentrations ***gradually lowered*** in the depthwise direction from the principal surface (having an impurity concentration NW) of the epitaxial layer 2E"), 16:11-15. Thus, Kawagoe discloses a well region containing at least one graded dopant region (*e.g.,* the region highlighted in light green in both Figures 23 and 17) having a downward-sloping graded dopant concentration. Ex.1003, ¶100.



Ex.1007, FIGS. 17/23.

Kawagoe further explains that this downward-sloping graded dopant concentration aids carrier movement from the surface of the epitaxial layer towards/to the area of the substrate where there are no active regions:

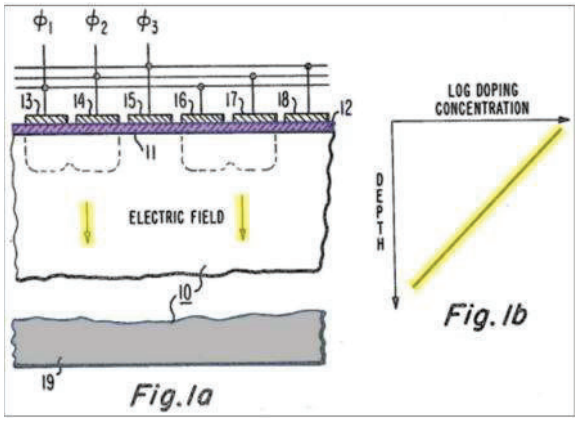
[T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

Id., 16:2-11. Kawagoe's teaching is consistent with Applicant's representation to the Patent Office during prosecution of the parent '195 Patent that a downward-

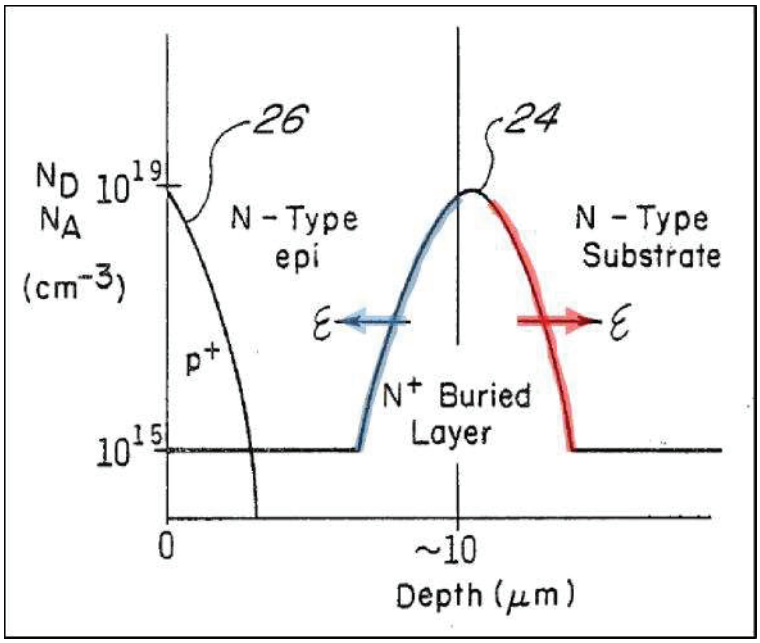
sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that moves carriers deep into the substrate (while an upward-sloping concentration, not at issue in Kawagoe, would move carriers in the opposite direction towards the surface):

> [T]he graded dopant concentration itself creates a ***'built-in' electrical field*** that forces the movement of carriers into a particular direction, whereby ***the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***

Ex.1016, 289-290 (underlining in original); Ex.1003, ¶¶101-102. Applicant also represented that "a unidirectional drift (electric) field necessarily affects ***all*** the present minority carriers in the same way.... Depending on the particular slope of the graded concentration of dopant, ***all*** minority carriers are either ***swept*** 'down' ... or 'up.'" Ex.1016, 289. Applicant cited Jastrzebski in support. *Id.*, 290. In Jastrzebski, the doping concentration is "decreasing with depth" from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. Ex.1010, 5:14-22. Jastrzebski teaches that this downward-sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers ... ***deep into the substrate***[.]" *Id.*, 2:27-32, 5:14-22.



Id., FIGS. 1a-1b. Applicant made the same representation to the Patent Office regarding Kamins. Ex.1016, 237-238. According to Applicant, Kamins' Figure 3 shows "two electric fields with opposing directions" (highlighted in blue and red) that correspond to increasing and decreasing graded dopant concentrations, respectively. *Id.*, 237 (citing Ex.1031, 3:6-13). Applicant explained that the electric field associated with the downward-sloping graded concentration at depth beyond ~10mm (red) causes "carriers created [in that region to be] .. ***accelerated into the substrate*** ..." *Id.* (citing Ex.1031, 3:6-13, FIGS. 2-3).



Ex.1031, FIG. 3.

In light of the above, Kawagoe satisfies elements [1.6]/[21.6] under Patent Owner's construction that the term "well region" means "a doped region that surrounds the active region of a semiconductor device." Ex.1020, 30; Ex.1036; Ex.1003, ¶105. As shown in Figure 23 above, p-well 6p (light green) is a doped region that surrounds the first active region (purple/light purple). Ex.1003, ¶105. Kawagoe also satisfies elements [1.6]/[21.6] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. Ex.1036; Ex.1003, ¶105.

Kawagoe also satisfies Petitioner's proposed constructions of these terms. Ex.1036; Ex.1003, ¶106. The mapping of "well region" to Kawagoe's p-well 6p satisfies Petitioner's construction of the term because p-well 6p is formed by implanting ions of "a p-type impurity such as boron." Ex.1007, 17:43-49; Ex.1036;

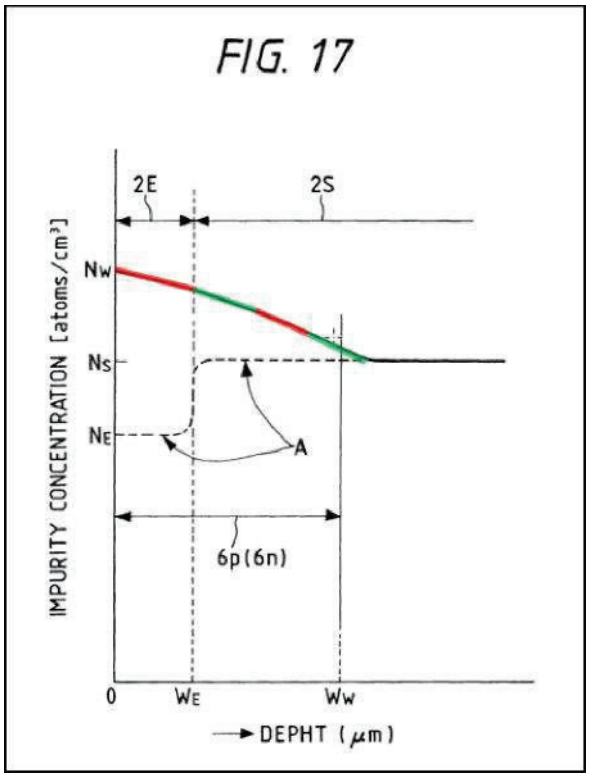
Ex.1003, ¶106. With regard to the "aid carrier movement" term, Kawagoe satisfies Petitioner's alternative proposed construction that the term means "to sweep the carriers from the surface [towards/to] the area of the substrate where there are no active regions." Ex.1036; Ex.1003, ¶106. Indeed, as discussed in Wang and as was well understood in the art, an cc-ray generates a stream of millions of carriers (*e.g.,* electrons) that can cause single-event upset (SEU) soft errors. Ex.1009, 431, FIG. 2; §VIII.A.1.f; Ex.1003, ¶106. Kawagoe explains that the graded dopant concentration illustrated in Figure 17 reduces soft errors by sweeping those carriers towards/to the bottom of the substrate where there are no active regions. Ex.1007, 16:2-11; Ex.1003, ¶107.

h. Element [1.7]: "wherein at least some of the transistors form digital logic of the VLSI semiconductor device."

Kawagoe teaches that the transistors in its active regions form digital logic in teaching that they form "a CMOS ... circuit" and that its "techniques ... can ... be applied to ... a ***logic circuit*** such as [a] 'microcomputer'" and to a "peripheral circuit region" of DRAM and flash memory. Ex.1007, 8:46-52, 14:46-55, 15:26-40, 20:133, 22:10-29, 22:51-23:2, 24:28-31; Ex.1008A, 810-811 (CMOS used "***to form low-power IC logic gates***"); Ex.1003, ¶108.

i. Element [21.7]: "wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

As shown below, the graded dopant concentration is linear or nearly linear (quasilinear). Ex.1003, ¶109. It is also a combination of linear/quasilinear segments, illustrated in green/red—as the segments get smaller, they become even more linear/quasilinear. *Id.*



Ex.1007, FIG. 17.

2. Claims 2/23: "The VLSI semiconductor device of claim [1/21], wherein the substrate is a p-type substrate."

§VIII.A.1.b.

3. Claims 3/24: "The VLSI semiconductor device of claim [1/21], wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

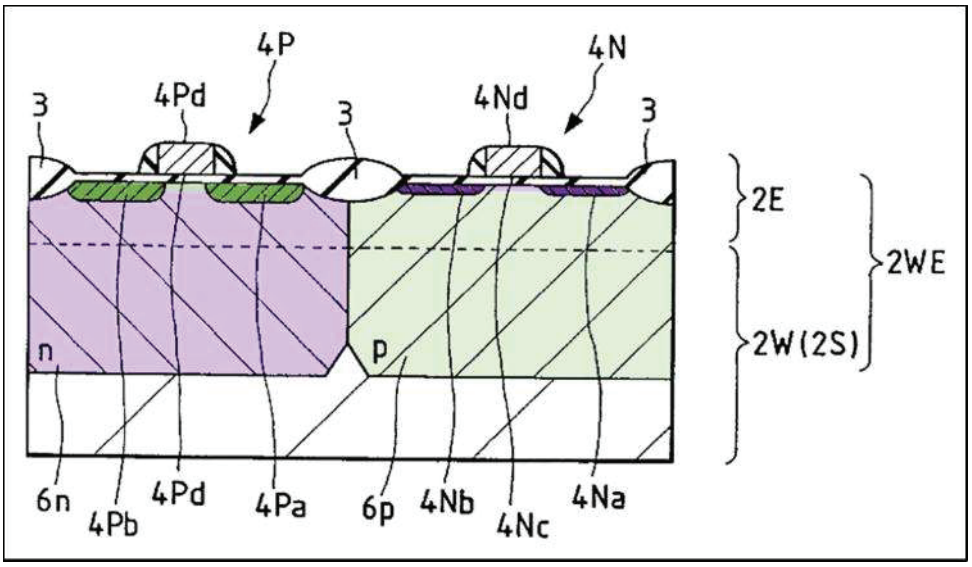
§VIII.A.1.b.

4. Claims 4/25: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain [digital logic formed by/at least] one of either p-channel and n-channel devices."

§§VIII.A.1.c-e, VIII.A.1.h.

5. Claims 5/26: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant."

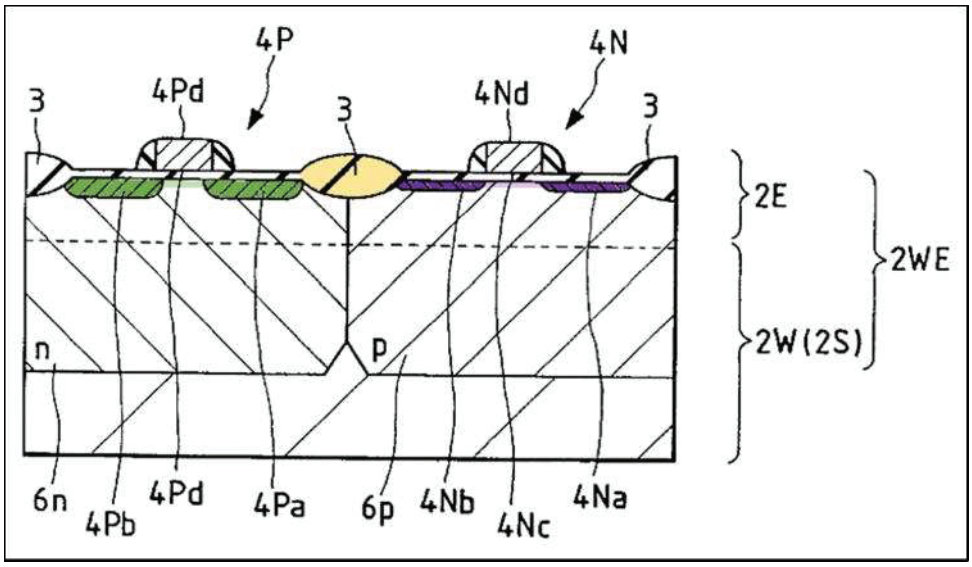
Kawagoe's Figure 23 illustrates conventional twin-well architecture, whereby the first active region contains nMOS (n-channel) transistor 4N formed in p-well 6p, and the second active region contains pMOS (p-channel) transistor 4P formed in n-well 6n. Ex.1007, 8:46-52, 14:46-55, 15:26-43; §§VIII.A.1.c-d; Ex.1008B, 387-88; Ex.1003, ¶113. This mapping satisfies this claim under Patent Owner's interpretation that a claimed active region can contain "***a transistor***." Ex.1020, 31; Ex.1003, ¶114. A POSITA would have also understood that Kawagoe teaches forming multiple transistors in an active region to save chip area. Ex.1003, ¶114.



Ex.1007, FIG. 23. Further, Kawagoe's n-wells and p-wells have graded dopants. *Id.*, 14:46-55, 15:62-16:2 ("as shown in FIGS. 16 and 17, ...the p-well 6p and n-well 6n have their impurity concentrations ***gradually lowered*** in the depthwise direction from the principal surface (having an impurity concentration NW) of the epitaxial layer 2E."); §VIII.A.1.g (discussing graded dopants in p-well 6p); Ex.1003, ¶115.

6. Claims 6/27: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region are each separated by at least one isolation region."

As shown below, the first (purple/light purple) and second active regions (green/light green) are separated by "field insulating film 3" (claimed "isolation region") (yellow). Ex.1007, 8:40-52, 15:37-40, 17:62-18:8; Ex.1008A, 818-20, FIG. 16-11(f); Ex.1003, ¶116.



Ex.1007, FIG. 23.

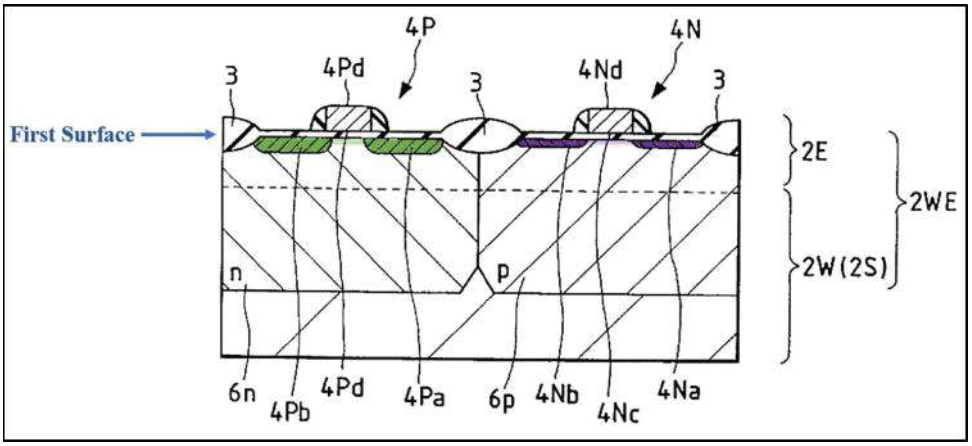
7. Claims 7/32: "The VLSI semiconductor device of claim [1/21], wherein the graded dopant is fabricated with an ion implantation process."

Kawagoe discloses that the graded dopants in n-well 6n and p-well 6p are "formed by the ion implantation method." Ex.1007, 4:11-12, 15:26-36, 17:10-12, 17:31-39 (n-well 6n formed by implanting "ions of an n-type impurity such as phosphor"), 17:43-49 (p-well 6p formed by implanting ions of "a p-type impurity such as boron"); §§VIII.A.1.f-g; Ex.1003, ¶117.

8. Claim 8: "The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

As shown below, Kawagoe discloses that the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (blue). Ex.1007, 8:66-9:6, 9:47-54, 15:37-40, 17:10-12, 17:31-18:35;

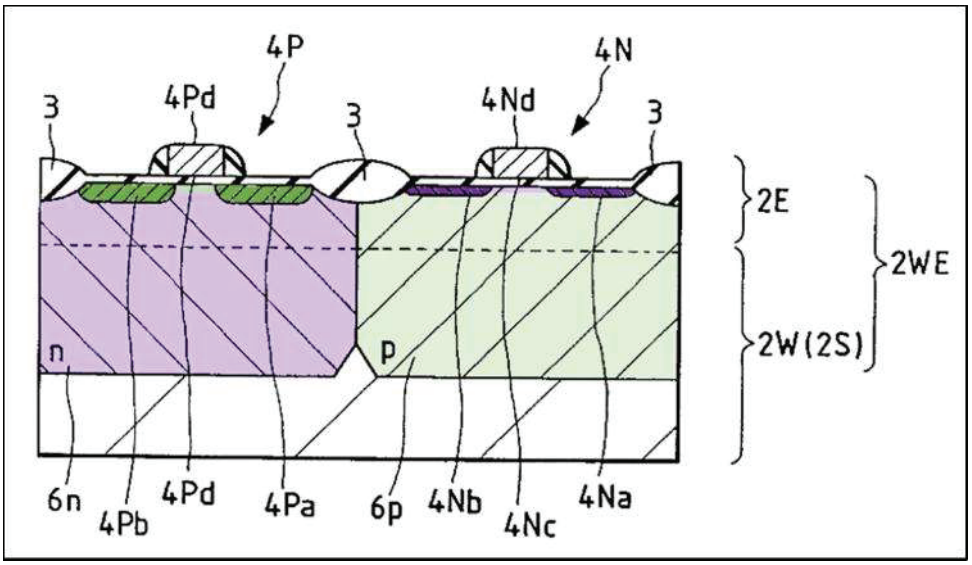
Ex.1003, ¶118 Ex.1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions...."), 298, 300-301, FIG. 5-2; §§VIII.A.1.c-d.



Ex.1007, FIG. 23.

9. Claims 9/28: "The VLSI semiconductor device of claim [1/21], wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type."

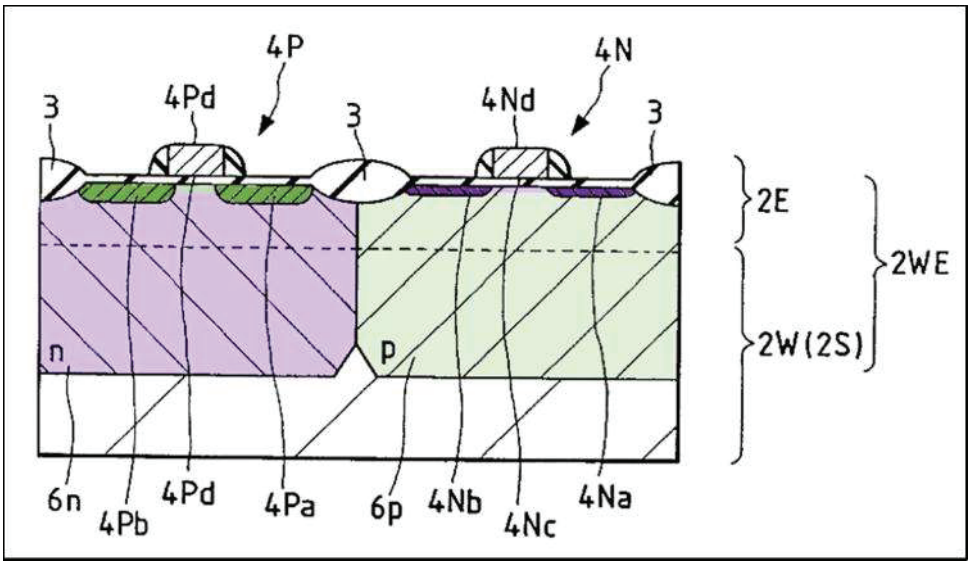
As shown in Figure 23, the channel region (light purple) of the first active region—between source-drain regions 4Na/4Nb—formed at the top of p-well 6p is of the same doping type (p-type) as p-well 6p. Ex.1007, 15:26-36 ("The p-well 6p is doped with a p-type impurity such as boron."); *id.*, 17:10-12, 17:43-49; Ex.1003, ¶119. Likewise, the channel region (light green) of the second active region—between source-drain regions 4Pa/4Pb—formed at the top of n-well 6n is of the same doping type (n-type) as n-well 6n. Ex.1007, 15:26-36 ("n-well 6n is doped with an n-type impurity such as phosphor"), 17:10-12, 17:33-39; Ex.1003, ¶120.



Ex.1007, FIG. 23. Those channel regions have graded dopant concentrations. §VIII.A.1.f; Ex.1003, ¶121.

10. Claim 13: "The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel."

Kawagoe teaches nMOS transistor 4N formed in the first active region and pMOS transistor 4P formed in the second active region, which are CMOS digital logic transistors. Ex.1007, 8:45-52, 14:46-55, 15:37-40; Ex.1003, ¶122; §VIII.A.1.h.



Ex.1007, FIG. 23. Each of the CMOS digital logic transistors includes a source, drain, gate, and channel. Ex.1003, ¶123. The nMOS transistor 4N includes "source-drain regions" 4Na/4Nb spaced apart by an "n-channel" region, and gate electrode 4Nd, and pMOS transistor 4P includes "source-drain regions" 4Pa/4Pb spaced apart by a "p-channel" region, and gate electrode 4Pd. Ex.1007, 8:42-67, 9:41-48, 14:46-55, 15:37-40, FIG. 23; Ex.1003, ¶123; §§VIII.A.1.c-d, VIII.A.1.f.

11. Claim 14: "The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM)."

Kawagoe explains that "embodiment 4" (Figures 16-17, 20-24), relied upon for claim 1, can be advantageously used to fabricate DRAM devices (having "MOS capacitors") with reduced soft errors, reduced defect density, and "excellent gate breakdown performance." Ex.1007, 16:2-11 (explaining that the graded dopant concentration in p-well 6p (illustrated in Figure 17) moves "electrons produced by

the a-ray" to the substrate body 2S so that "soft errors can be reduced in case ... DRAM or the like is formed in the p-well 6p"), 19:15-23 ("the structure of the present embodiment 4 is applied to a 4M.DRAM"), 19:31-32, 19:43-48, 20:1-33 (DRAM with "transfer MOS.FET[s] [] and [] capacitor[s]" formed in accordance with embodiment 5, which uses Embodiment 4's downward sloping graded dopant concentration); Ex.1003, ¶124.

12. Claims 16/34: "The VLSI semiconductor device of claim [1/21], wherein the device is a flash memory."

Kawagoe teaches a semiconductor flash memory device. Ex.1007, 22:14-18 ("The semiconductor integrated circuit device 1 of the present embodiment 7, as shown in FIG. 28, is exemplified by a flash memory."). The flash memory device includes a CMOS "peripheral circuit region [] formed with the nMOS 4N and the pMOS 4P...." Ex.1007, 22:51-23:2. This peripheral circuit is fabricated according to twin-well CMOS technology, whereby NMOS transistors (*e.g.*, 4N) are formed in "p-well 6p3," and PMOS transistors (*e.g.*, 4P) are formed in "n-well 6n2." *Id.*, 22:51-65, FIG. 28. Significantly, Kawagoe explains that the teachings of Embodiment 4 (relied upon in mapping for claim 1) are applicable to Embodiment 7 and therefore flash memory. Ex.1003, ¶¶125-126. In particular, Embodiment 7 applies the teachings of Embodiment 4 relating to the use of an epitaxial substrate to form a twin-well architecture with pMOS transistor 4P formed in an n-well and nMOS transistor 4N formed in a p-well, where both wells have a downward-sloping graded

dopant concentration. Ex.1007, 22:22-29 ("In the present embodiment 7, too, the semiconductor substrate 2 is formed thereover with a p-well 6*p*3 and an n-well 6*n*2. The p-well 6*p*3 and n-well 6*n*2 are formed, ***as in the foregoing embodiments 4 and 6***, to extend from the surface of the epitaxial layer 2E to the upper portion of the semiconductor substrate body 2S. Moreover, their impurity concentrations are made gradually lower depthwise of the semiconductor region 2, ***as in the foregoing embodiment 4***."), FIG. 28.

13. Claim 17: "The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors."

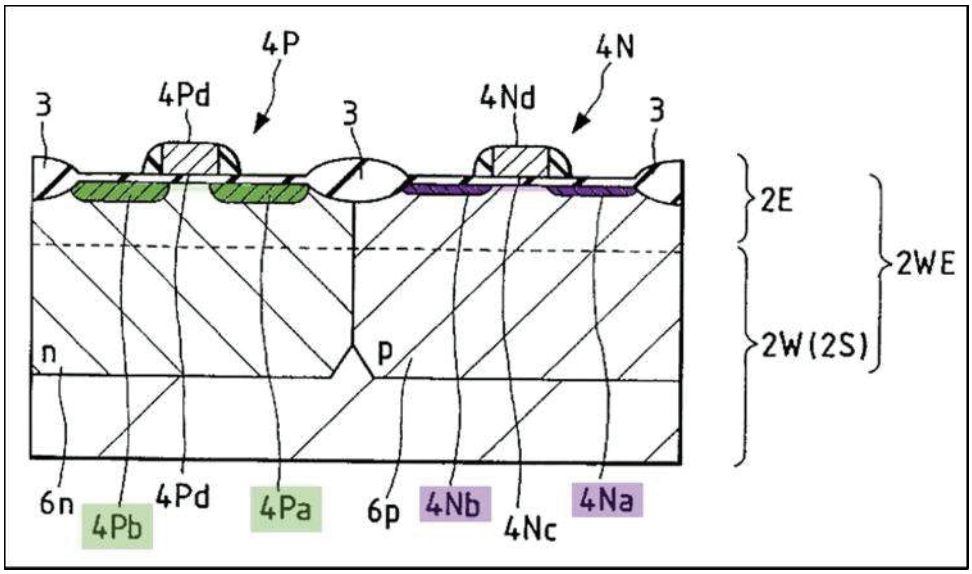
§§VIII.A.1.h, VIII.A.11.

14. Claims 18/36: "The VLSI semiconductor device of claim 11/21], wherein the device is central processing unit."

Kawagoe teaches that its disclosures can be applied to a "microcomputer," which a POSITA would have understood includes a central processing unit (CPU). §VIII.A.1.h; Ex.1032, 1334; Ex.1003, ¶128.

15. Claims 20/38: "The VLSI semiconductor device of claim 11/21], wherein each of the first and second active regions are in the lateral or vertical direction."

As shown in Figure 23 below, the first (purple/light purple) and second (green/light green) active regions are in the lateral direction. Ex.1003, ¶129.



Ex.1007, FIG. 23.

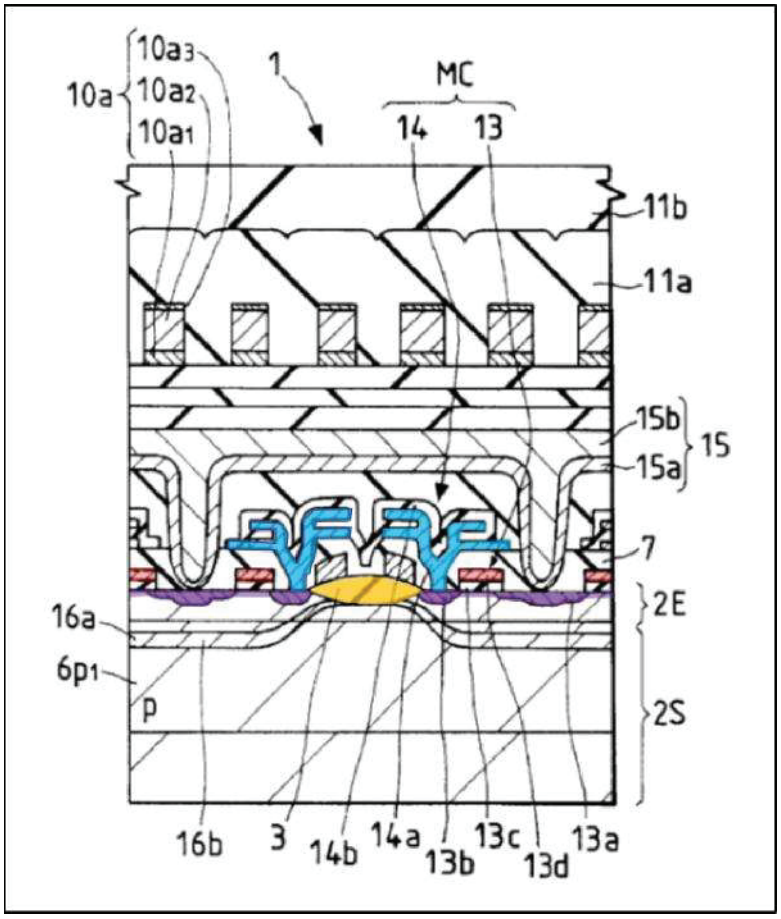
16. Claim 33: "The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device."

Kawagoe teaches that "nMOS 4N and pMOS 4P constitute a CMOS" device formed in and including a substrate. Ex.1007, 8:46-52, 15:26-40, 8:60-9:6, 9:41-54, 14:46-55; Ex.1003, ¶130; *see also* §VIII.A.1.b.

17. Claim 35: "The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions."

Kawagoe's teachings apply to 16-Megabit DRAM logic devices. §§VIII.A.1.a/h, VIII.A.11; Ex.1007, 19:64-20:67. As shown below, capacitors 14 (blue electrodes) are in first and second n-type active regions (purple/light purple), which are adjacent the substrate surface and separate from and adjacent to one another, as described above. Ex.1007, 20:12-28, 20:39-52; §§VIII.A.1.c-d.

Transistors 13 (red gates) are formed in the surface of each active region, the channel regions of which (light purple) have a graded dopant concentration to aid carrier movement, as described above. Ex.1007, 20:12-28, FIG. 17; §§VIII.A.1.c-f. P-well 6p1, adjacent the active regions, also has a graded dopant region to aid carrier movement, as described above. Ex.1007, 20:12-28, FIG. 17; §VIII.A.1.g; Ex.1003, ¶131.



Ex.1007, FIG. 26(A).

To the extent the claim requires multiple first/second active regions, a POSITA would have understood Kawagoe to disclose this because Kawagoe's 16M

DRAM has over 16 million memory cells (Figure 26A only shows a small portion of them (*i.e.*, a few memory cells, each with transistor 13 and capacitor 14)). Ex.1007, 20:1-14; Ex.1003, ¶132. Figure 26(A)'s DRAM also includes a peripheral circuit region with the same structure as Embodiment 4 and, therefore, additional first/second active regions. Ex.1007, 20:1-8.

Further, MOS transistors are commonly used as capacitors to form dynamic circuits such as voltage bootstrapping circuits, charge pump circuits, delay/timing circuits, and to form decoupling capacitors ("decaps"). Ex.1003, ¶133. Hodges' figure below shows an NMOS transistor configured as a capacitor by connecting its gate to VDD and its source/drain to VSS. Ex.1038, 493-494.

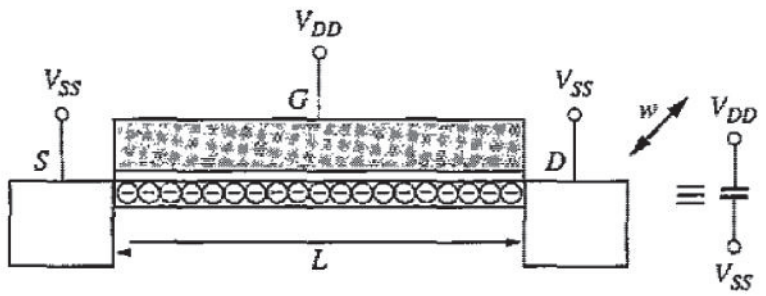


Figure 11.11
On-chip decap using MOS capacitance.

Id., FIG. 11.11. A POSITA would have understood (and found it obvious) that some of Kawagoe's transistors formed in some of the first/second active regions are configured as capacitors. Ex.1003, ¶¶133-134. For example, the voltage bootstrapping circuit below—a "very useful" and commonly used circuit—includes

a transistor configured as a capacitor (Cboot) connected to other transistors (M1-M3). Ex.1041, 370-373.

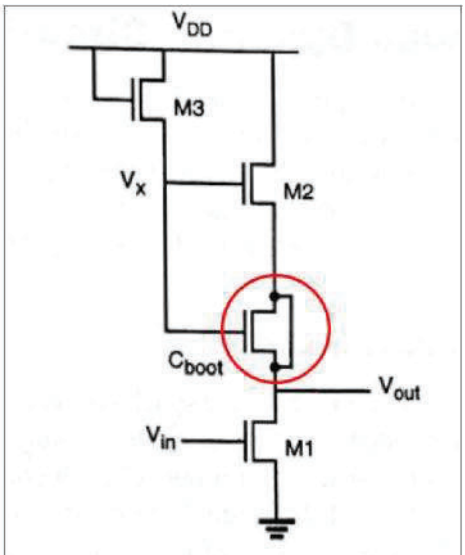


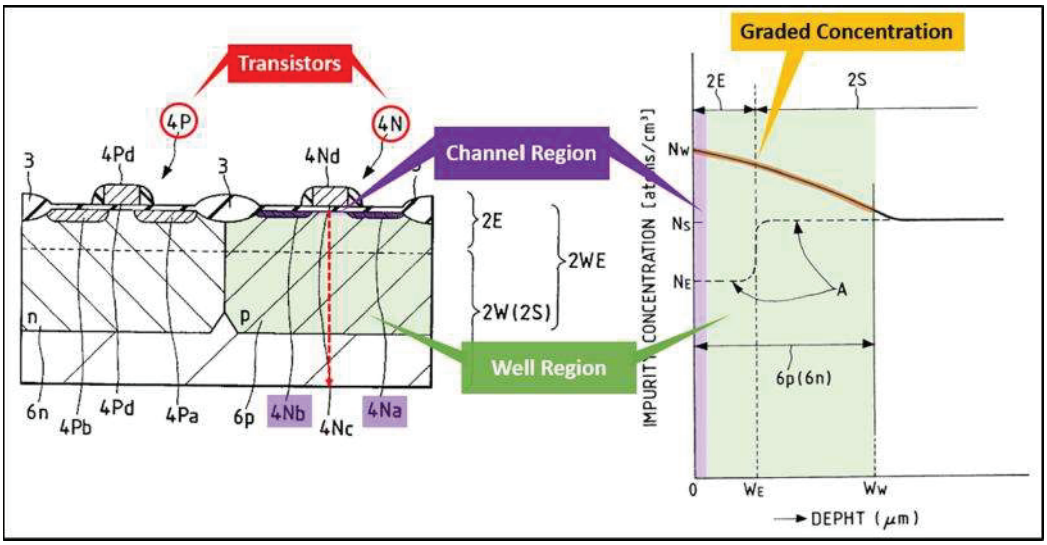
Figure 9.13 Realization of the bootstrapping capacitor with a dummy MOS device.

Id., FIG. 9.13. A POSITA would also find it obvious to configure transistors as decaps "scattered throughout the design" to filter out power supply noise and reduce "*IR* drop." Ex.1038, 493 ("On-chip decoupling capacitors (decaps) are ***commonly used*** to keep the power supply within the noise budget, especially during peak demand periods in high-frequency switching operations."); *id*., 498 ("The ***most effective approach*** [to reduce *IR* drop] is to use *decoupling capacitors* between power and ground ... These decoupling caps are usually ***scattered*** throughout the design in any available space, using ***transistors*** with their gates tied to VDD and their source-drain regions tied to Gnd.") (italics in original); *id.,* 499 ("you can never have enough" decaps); Ex.1003, ¶133. Doing so would have amounted to combining

prior art elements (Kawagoe's devices and decaps) according to known methods (scattering transistor decaps wherever available) and amounted to use of a known technique (scattering transistor decaps) to improve similar devices (Kawagoe's devices) in the same way (filter noise and reduce IR drop). *Id.* There is reasonable expectation of success with predictable results because the use of transistors as capacitors was a well-known, intended use of MOS transistors. *Id*.

18. Claim 40: "The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well."

§VIII.A.1.g. As illustrated below, Kawagoe's graded dopant concentration is downward-sloping throughout each well (green) and moves carriers from any region of the well to deeper areas of the substrate where there is no well. Ex.1003, ¶135.



Ex.1007, FIGS. 17/23.

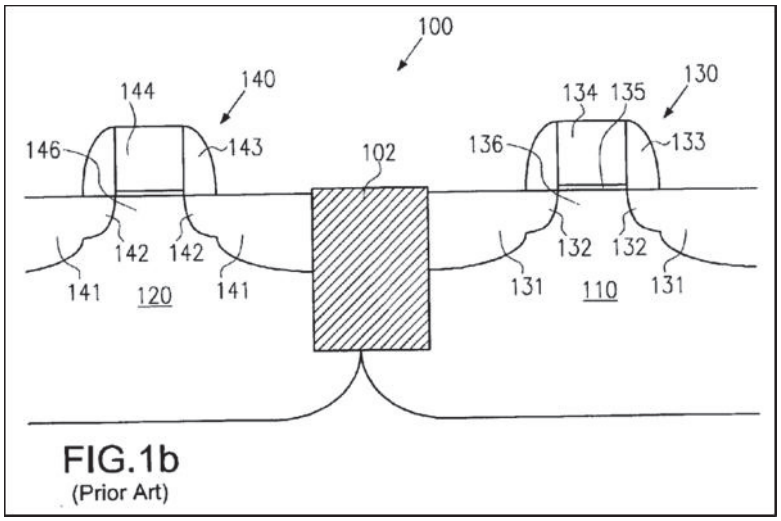
B. Ground II

Wieczorek in combination with Wolf (hereinafter, "Wieczorek-Wolf") renders claims 1-2, 4-9, 13-18, 20-23, 25-28, 32-36, and 38-42 obvious. Ex.1003, ¶¶136-138. A POSITA would have been motivated to combine Wieczorek with Wolf. *Id.*, ¶137. This Petition relies on Wieczorek's description of a conventional prior-art CMOS device. Ex.1006, [0020]-[0021], [0004] ("Field effect transistors, such as MOS transistors, represent one of the most frequently used circuit elements in modem [*sic*] integrated circuits."), [0007]-[0008] (describing "[a] typical process flow for forming the semiconductor device 100" which is "a complementary MOS transistor pair"), [0012], FIG. 1b. Wolf is a well-known textbook that teaches known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices. *See generally* Ex.1008A; *id.*, Chapter 16 ("CMOS Process Integration"); Ex.1003, ¶138. A POSITA would have therefore understood and expected that the teachings of Wolf would apply to Wieczorek's conventional CMOS device. *Id*. A POSITA would have looked to Wolf for additional details related to conventional CMOS devices, as detailed below. *Id*.

1. Claim 1/21/39/41/42

a. Preambles: "A [VLSI] semiconductor device, comprising:"

To the extent the preamble is limiting, Wieczorek teaches a "semiconductor device 100." Ex.1006, [0012]; Ex.1003, ¶139. Wieczorek's Figure 1b illustrates a conventional twin-well CMOS device. §VIII.B.1.b.



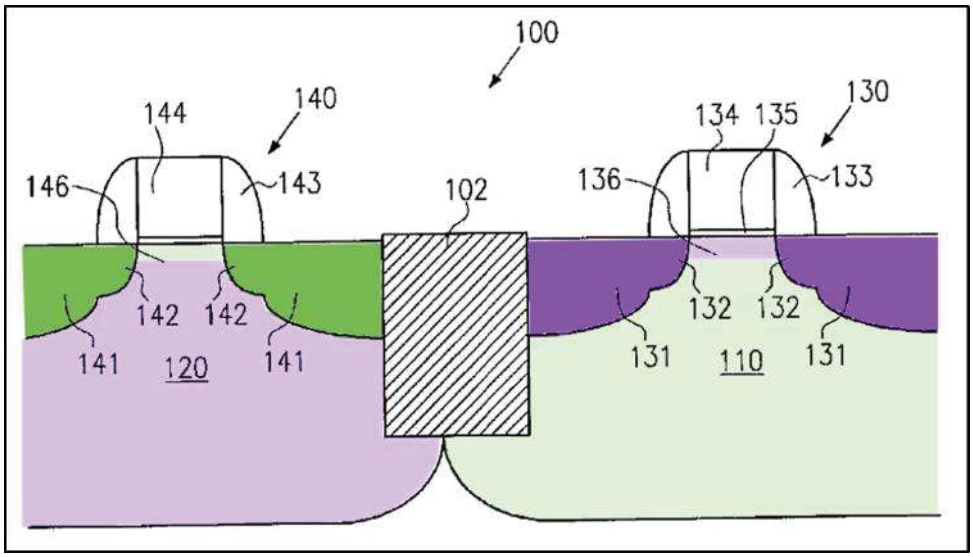
Ex.1006, FIG. 1b.

Wieczorek-Wolf renders obvious using Wieczorek's teachings to fabricate DRAM, microprocessor, and flash memory devices. §§VIII.B.10/12/14; Ex.1003, ¶139. Wolf, which applies to "the VLSI Era," confirms that such devices at the time were understood to be VLSI devices having at least one million active elements. Ex.1008A, cover, xxxiii, FIG. 1 (microprocessor with at least one million transistors); Ex.1008B, 596-597 (1-Megabit CMOS DRAM with one transistor per memory cell, totaling at least one million transistors), 633-635 (1-Megabit CMOS

flash EEPROM with one floating gate per memory cell and other transistors, totaling at least one million active elements); Ex.1016, 73 (VLSI refers to "at least one million active elements").

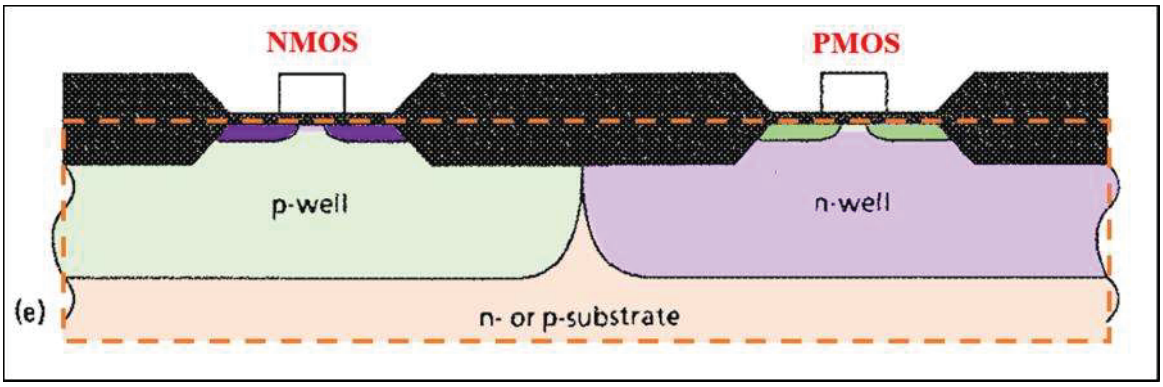
b. Elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1]: "a substrate of a first doping type at a first doping level [having a surface];"

Wieczorek's Figure 1b illustrates a twin-well CMOS device, where N-channel transistor 130 (nMOS) with source/drain regions 131-132 (purple) and channel region 136 (light purple) is formed in P-well 110 (light green), and P-channel transistor 140 (pMOS) with source/drain regions 141-142 (green) and channel region 146 (light green) is formed in N-well 120 (light purple). Ex.1006, [0007], [0012], [0020]-[0021]; Ex.1008C, 525, FIG. 8-1(e); Ex.1003, ¶140.



Ex.1006, FIG. 1b (labelled "Prior Art"). A POSITA would have understood that a twin well approach "is independent of starting material type" for the substrate.

Ex.1008C, 524; Ex.1006, [0004] (discussing use of "an appropriate substrate" for forming MOS transistors without further specificity); Ex.1003, ¶141. Because Wieczorek does not specify what constitutes an appropriate substrate, a POSITA would have been motivated to consult Wolf, which confirms that a "***uniform***, lightly doped *p*- or *n*-type substrate" is commonly used in twin-well CMOS devices. Ex.1008C, 523, 530 ("With the twin-tub [(twin-well)] approach, two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate ... of *n* or *p* material."); Ex.1008B, 387-389; Ex.1003, ¶142.

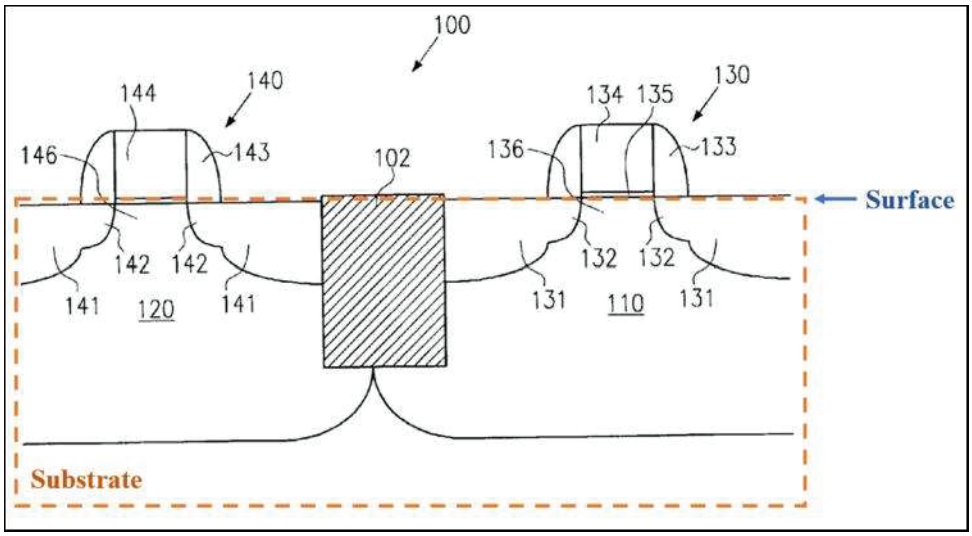


Ex.1008C, 525, FIG. 8-1(e) ("twin-well CMOS on *n*- or *p*-substrate").

Consistent with Wieczorek's teaching, a POSITA would have found it obvious to use a uniformly doped n- or p-type substrate ("a substrate of a first doping type at a first doping level") as a suitable substrate for Wieczorek's CMOS device in Figure 1b. Ex.1003, ¶143. Doing so would amount to combining known prior art elements (*i.e.*, use of a uniform, lightly doped n- or p-type substrate with Wieczorek's process for forming a conventional CMOS device) according to known

methods (*i.e.*, known use of an "appropriate substrate" for the conventional process of forming the CMOS device in Wieczorek [0007]-[0013]) to obtain predictable results (*i.e.*, conventional CMOS device in Wieczorek's Figure 1b). Ex.1003, ¶143. Doing so would have also been obvious to try because it involves nothing more than choosing one of a finite number of known appropriate substrates that are described by Wolf as suitable for use in forming a twin-well CMOS device like Wieczorek's. *Id*. There would have been reasonable expectation of success because Wolf shows that a POSITA would have known how to use a uniformly doped n- or p-type substrate to form a twin-well CMOS device similarly as described in Wieczorek. *Id*.

For purpose of claim mapping, Wieczorek-Wolf's substrate is taken as a p-type non-epitaxial substrate, which has the advantage of lower cost compared to an epitaxial substrate. Ex.1003, ¶144; Ex.1008A, 816 ("in twin-well CMOS the starting material is also ***either*** a lightly *p*-doped wafer (***p-bulk wafer***, Fig. 16-7a), or a heavily *p*-doped wafer on which a thin, lightly *p*-doped epi layer is grown" and noting the cost disadvantage of epitaxial wafers), FIG. 16-7. Consistent with the teachings of Wolf, Wieczorek's substrate in Figure 1b below, has a surface. Ex.1008B, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e); Ex.1003, ¶144.



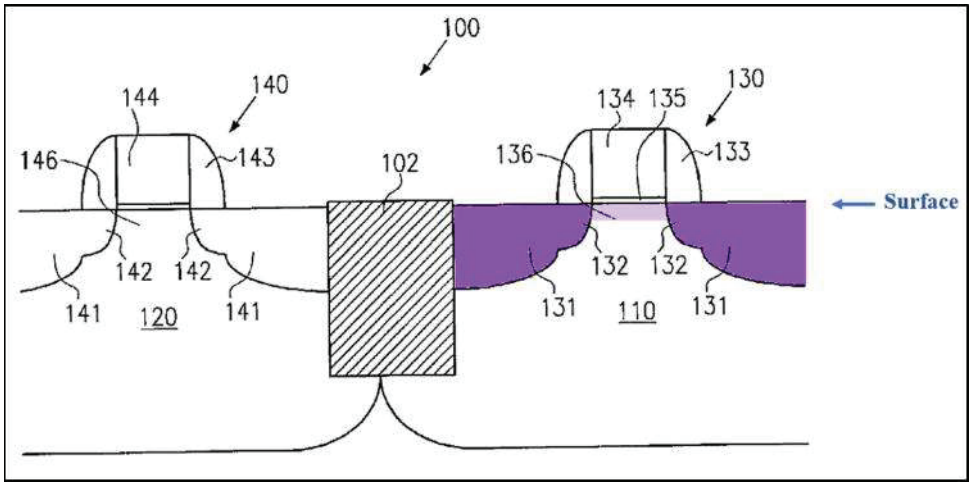
Ex.1006, FIG. 1b.

Wieczorek-Wolf satisfies elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1] under Patent Owner's plain meaning construction and under Petitioner's proposed construction because Wieczorek-Wolf's substrate is the initial material within or on which Wieczorek's "semiconductor device 100" is fabricated. Ex.1036; Ex.1006, [0004], [0012]; Ex.1003, ¶145.

c. Elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2]: "a first active region disposed adjacent [the/to a] surface [of the substrate] with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed [in the surface thereof];"

Wieczorek discloses "an N-channel transistor 130" that includes "heavily N-doped ***source and drain regions*** 131, including lightly doped extensions 132," and "***channel region*** 136." Ex.1006, [0012]-[0013]; *id.,* [0004] ("[A] field effect transistor comprises two highly doped semiconductor regions...referred to as ***drain and source regions***, [] embedded in a lightly and inversely doped semiconductor

region, the so-called N-well or P-well [and] spaced apart with a ***channel region*** interposed, wherein a conductive channel forms between the drain and source regions in the channel region" when the transistor is active). The source-drain regions 131-132 (purple) form part of the claimed first active region, which also includes channel region 136 (light purple) between them. Ex.1006, [0012]; Ex.1003, ¶146; Ex.1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source and drain*** regions."), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e). As shown in Figure 1b, nMOS transistor 130 is formed in the surface of the first active region, which is adjacent the surface of the substrate. Ex.1003, ¶146.

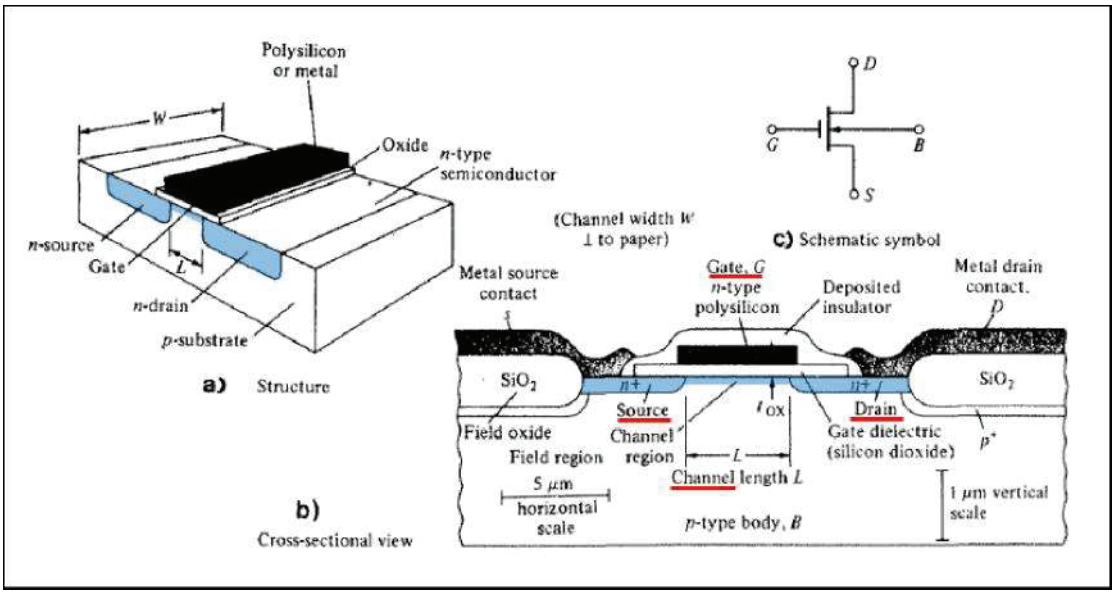


Ex.1006, FIG. 1b, [0007]. Because the source-drain regions of the first active region are N-doped, Wieczorek-Wolf's first active region has a second doping type (N-

type) opposite in conductivity to the first doping type (P-type) of the substrate. Ex.1006, [0012]; Ex.1003, ¶147.

While Figure 1b illustrates an exemplary nMOS transistor 130 formed in the first active region, a POSITA would have understood that Wieczorek teaches forming multiple nMOS transistors in the first active region to minimize chip area, as good layout practice dictates. Ex.1006, [0004]; Ex.1003, ¶148; Ex.1014, 1:52-54, 2:17-21. In any event, according to Patent Owner, an "active region ... within which transistors can be formed" means "an active region ... where ***a transistor*** can be formed." Ex.1020, 31.

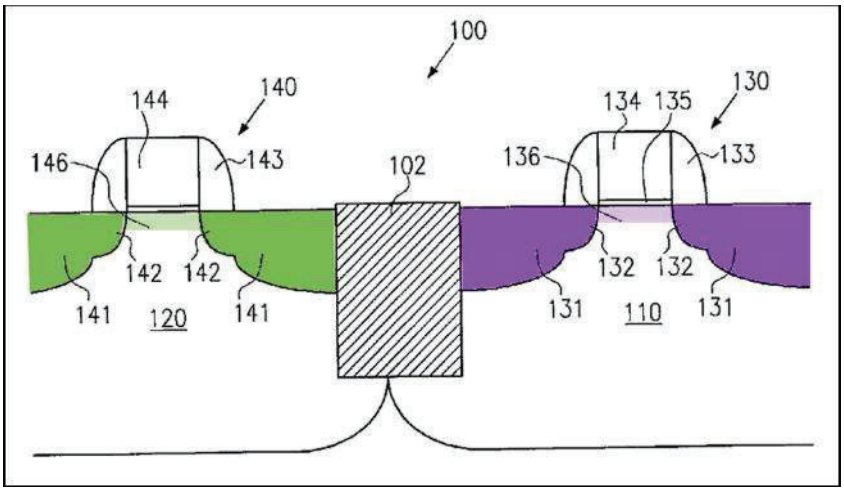
Wieczorek satisfies elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2] under Patent Owner's construction that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Ex.1020, 20; Ex.1036; Ex.1003, ¶149. Indeed, the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions" (blue). Ex.1008B, 299.



Ex.1008B, FIG. 5-1; *id*., 298-301, FIGS. 5-2/6-4. Wieczorek also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device" because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Ex.1036; Ex.1008B, 299-301; Ex.1008D, 197, FIG. 5-13; Ex.1003, ¶150. Patent Owner does not dispute this. Ex.1020, 3-4 ("when a positive voltage is applied to the gate ... a ***conductive channel*** [is formed] between the ***source*** and the ***drain***, and ***current*** can begin to flow through the transistor").

d. Elements [1.3]/[21.3]/[39.3]/[41.3]/[42.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed [in the surface thereof];"

Wieczorek discloses "P-channel transistor 140," including "heavily P-doped source and drain regions 141, including lightly doped extensions 142," and "channel region 146." Ex.1006, [0004], [0007], [0012]-[0013]; Ex.1003, ¶151. Source and drain regions 141-142 (green) are part of the claimed second active region, which also includes channel region 146 (light green) between them. Ex.1006, [0012]; Ex.1008B, 298-301, FIGS. 5-1/5-2/6-4; §VIII.B.1.c; Ex.1003, ¶151. As shown in Figure 1b, pMOS transistor 140 is formed in the surface of the second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex.1006, [0012]; Ex.1003, ¶152. Adjacent active regions are separated by an isolation region (*e.g.,* shallow trench isolation 102). Ex.1006, [0007]; Ex.1008A, 818-20, FIG. 16-11(f); Ex.1001, Cl. 6; Ex.1003, ¶152; §VIII.A.1.d.



Ex.1006, FIG. 1b, [0007].

While the figure shows an exemplary pMOS transistor 140 formed in the second active region, a POSITA would have understood that Wieczorek teaches forming multiple pMOS transistors in the second active region. Ex.1006, [0004]; Ex.1003, ¶153; §VIII.B.1.c. Regardless, according to Patent Owner, an "active region ... within which transistors can be formed" means "an active region ... where ***a transistor*** can be formed." Ex.1020, 31.

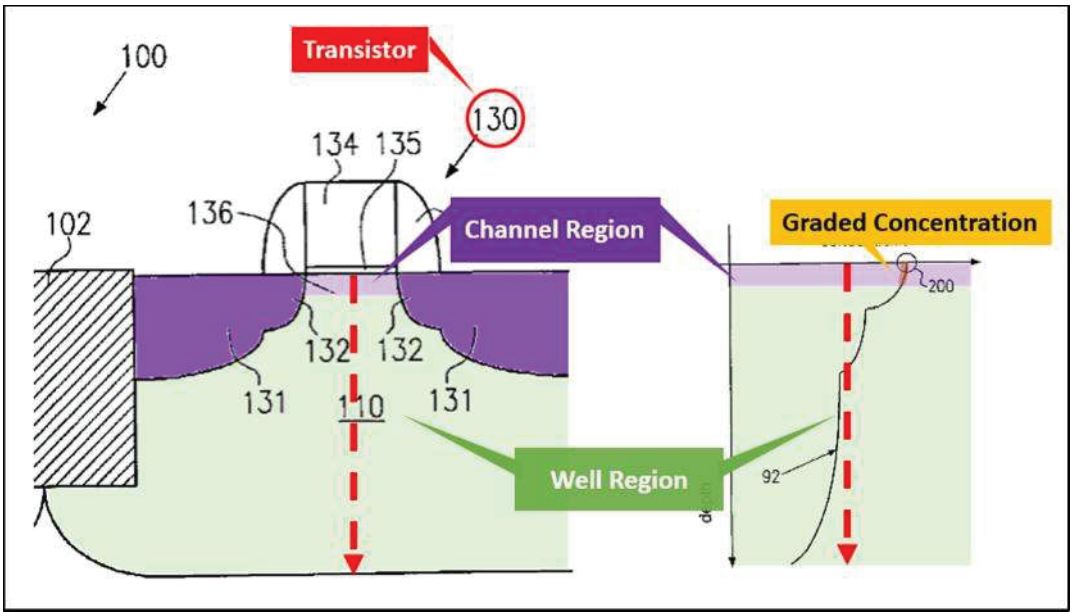
Wieczorek satisfies elements [1.3]/[21.3]/[39.3]/[41.3]/[42.3] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." §VIII.B.1.c; Ex.1003, ¶154. Wieczorek also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device." *Id*.

e. Elements [1.4]/[21.4]/[39.4]/[41.4]/[42.4]: "transistors formed in at least one of the first active region or second active region;"

§§VIII.B.1.c-d.

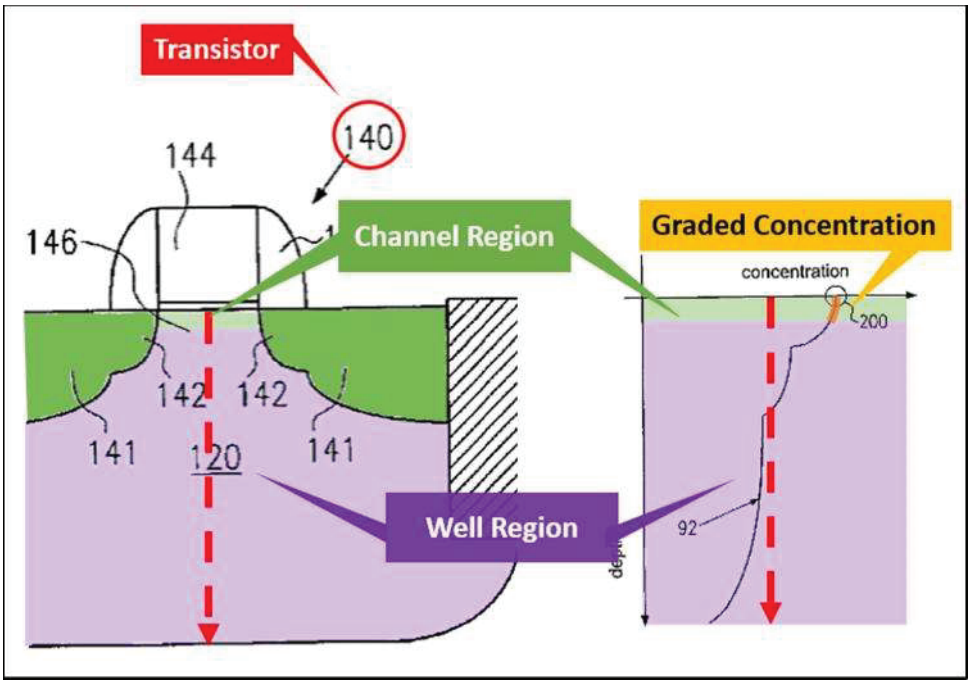
f. Elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5]: "at least a portion of at least one of the first and second active regions having at least one graded [dopant/dopant acceptor/donor dopant] concentration to aid carrier movement from the [first and second active regions/surface/first or second active region] [towards/to] [an area of the substrate/at least one substrate area] where there [are/is] no active region[s]; and"

In Figure 1b (below left), channel region 136 (light purple) of nMOS transistor 130, formed at the top surface of the substrate, is a portion of the first active region. Ex.1006, [0012]-[0013], [0004] ("The drain and source regions are spaced apart with a ***channel region*** interposed"); Ex.1008B, 298-301 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source and drain*** regions."), FIG. 5-2; Ex.1003, ¶156.



Ex.1006, FIGS. 1b/2b. The doping concentration in the channel region is highlighted in brown in the doping profile of Figure 2b (above right), measured for example along the red dotted line in Figure 1b that traverses the channel region. *Id*., [0011] ("FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure."), [0013] ("after the plurality of heat treatments, the actual dopant concentration will be represented by the graph shown in FIG. 2b."), [0009], FIG. 2a.

As Figure 2b shows, the dopant concentration is highest at the surface of the substrate and decreases with depth. Ex.1003, ¶157. Therefore, channel region 136 has a graded dopant concentration. *Id*. And as shown in the figures below, Wieczorek teaches that channel region 146 (light green) of pMOS transistor 140, which is a portion of the second active region, also has a graded dopant concentration for the same reasons. Ex.1006, [0004], [0009], [0011]-[0013], FIGS. 2a-2b; Ex.1008B, 298-301, FIG. 5-2; Ex.1003, ¶157.

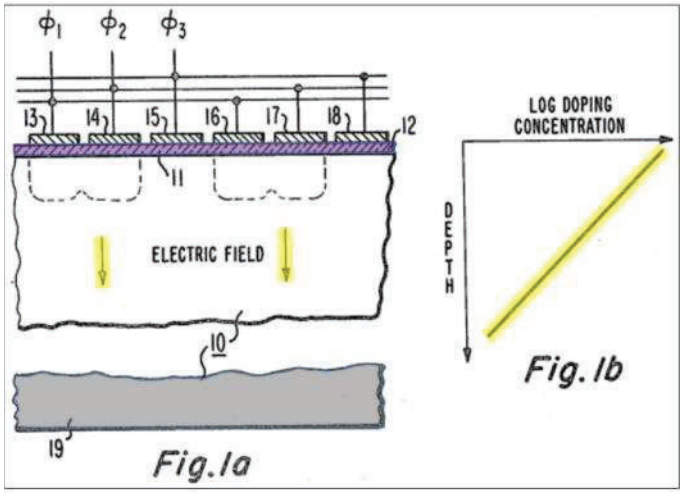


Ex.1006, FIGS. 1b/2b. Thus, Wieczorek discloses "at least a portion of" the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. Ex.1006, [0009], [0011], [0013]; Ex.1003, ¶157.

Element [41.5] claims a "graded dopant ***acceptor*** concentration." The graded channel region of Wieczorek's first active region is doped with a p-type impurity such as boron, an acceptor dopant. Ex.1006, [0008]; §VIII.B.8; Ex.1037, 30; Ex.1003, ¶158. Element [42.5] claims a "graded ***donor*** dopant concentration." The graded channel region of Wieczorek's second active region is doped with an n-type impurity such as phosphorous, a donor dopant. Ex.1006, [0008]; §VIII.B.8; Ex. 1037, 27; Ex.1003, ¶158.

Further, Wieczorek's downward-sloping graded dopant concentrations aid carrier movement from the surface and from the first and second active regions

towards/to an area of the substrate where there are no active regions to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. Ex.1003, ¶159. As detailed in §VIII.A.1.g, during prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded dopant concentration was known in the prior art to move carriers deep into the substrate. Applicant cited Jastrzebski and Kamins in support. §VIII.A.1.g. Notably, according to Jastrzebski, a downward-sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers ... ***deep into the substrate***[.]" Ex.1010, 2:27-32, 5:14-22.



Id., FIGS. 1a-1b.

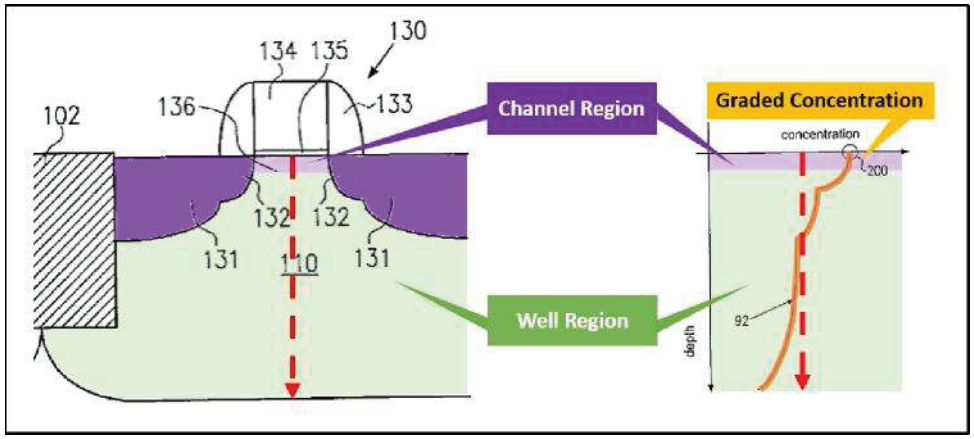
In light of the above, Wieczorek satisfies elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. Ex.1036; Ex.1003, ¶162. According to Patent

Owner, the claims make clear that "carriers [must move] in a particular direction (from the surface layer to the substrate)." Ex.1020, 29. Also, according to Patent Owner, "when the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction ...". *Id*., 2. Here, Wieczorek's Figure 2b shows that the dopant concentration is downward-sloping with increasing depth towards/to the bottom of the substrate where there are no active regions, and thus, according to Patent Owner, causes carriers to move deeper into the substrate as well. Ex.1003, ¶162.

Wieczorek also satisfies Petitioner's alternative proposed construction that the term means "to sweep the carriers from the [first and second active regions/surface/first or second active region] [towards/to] [an area of the substrate/at least one substrate area] where there [are/is] no active region[s]." Ex.1036; Ex.1003, ¶163. Wieczorek's Figure 2b illustrates a downward-sloping graded dopant concentration in the channel regions and Applicant represented to Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers into the substrate (where there are no active regions), as further detailed in §VIII.A.1.g. Ex.1016, 289-290.

g. Elements [1.6]/[21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface [towards/to] the area of the substrate where there are no active regions,"

As shown in Figure 1b (below left), Wieczorek discloses a "P-well structure 110" (light green) adjacent to the first active region (purple/light purple). Ex.1006, [0012]-[0013]; Ex.1003, ¶164. And, as shown in the dopant concentration profile (brown) of Figure 2b (below right), the dopant concentration in P-well 110—measured along the exemplary red dotted line in Figure 1b—is gradually decreasing with depth. Ex.1006, [0009], [0011] ("FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure [110 and 120]"), [0013]; Ex.1003, ¶164. Thus, Wieczorek discloses a well region containing at least one graded dopant region (*e.g.*, the region highlighted in light green in both Figures 1b and 2b) having a downward-sloping graded dopant concentration. Ex.1003, ¶164.



Ex.1006, FIGS. 1b/2b. Under Applicant's representation to the Patent Office, discussed above in §VIII.A.1.g, such a downward-sloping graded dopant concentration was known in the prior art to create a "built-in" electric field that moves carriers deep into the substrate and thus aids carrier movement from the surface towards/to the area of the substrate where there are no active regions. Ex.1003, ¶165.

In light of the above, Wieczorek satisfies elements [1.6]/[21.6] under Patent Owner's construction that the term "well region" means "a doped region that surrounds the active region of a semiconductor device." Ex.1020, 30; Ex.1036; Ex.1003, ¶166. As shown in Figure 1b above, P-well 110 (light green) is a doped region that surrounds the first active region (purple/light purple). Ex.1006, FIG. 1b. Wieczorek also satisfies elements [1.6]/[21.6] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. Ex.1036; Ex.1003, ¶166.

Wieczorek also satisfies Petitioner's proposed constructions of these terms. Ex.1036; Ex.1003, ¶167. The mapping of "well region" to Wieczorek's P-well 110 satisfies Petitioner's construction because P-well 110 and N-well 120 are formed using "ion implantation processes." Ex.1006, [0008], [0007]-[0012], FIGS. 1a/2a-2b; Ex.1003, ¶167. With regard to the "aid carrier movement" term, Wieczorek satisfies Petitioner's alternative proposed construction that the term means "to sweep the carriers from the surface towards/to the area of the substrate where there are no

active regions." Ex.1003, ¶167. Notably, Wieczorek's Figure 2b illustrates a graded dopant region with a downward-sloping graded dopant concentration and Applicant represented to Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers into the substrate (where there are no active regions), as further detailed in §VIII.A.1.g. Ex.1016, 289-290.

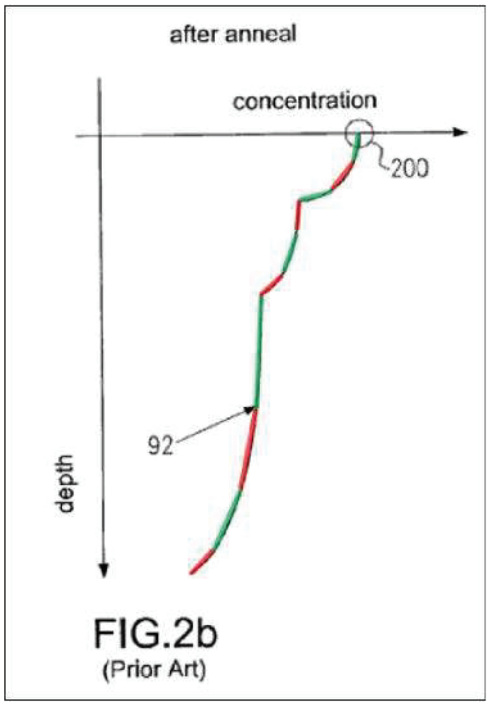
h. Element [1.7]: "wherein at least some of the transistors form digital logic of the VLSI semiconductor device."

Wieczorek's "complementary MOS transistor pair" is "a frequently used semiconductor device in modern integrated circuits" and was understood by a POSITA to form digital logic gates. Ex.1006, [0007], [0026]; Ex.1008A, 810-811 (CMOS, or "[t]he pairing of complementary n- and p-channel transistors ***to form low-power IC logic gates*** ... is now the dominant integrated-circuit technology"); Ex.1003, ¶168.

i. Element [21.7]: "wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

As shown in Figure 2b below, the graded dopant concentration is a combination of linear or nearly linear (quasilinear) segments, illustrated in green/red

below. Ex.1003, ¶169. As the segments get smaller, they become even more linear/quasilinear. *Id.*



Ex.1006, FIG. 2b.

2. Claims 2/23: "The VLSI semiconductor device of claim [1/21], wherein the substrate is a p-type substrate."

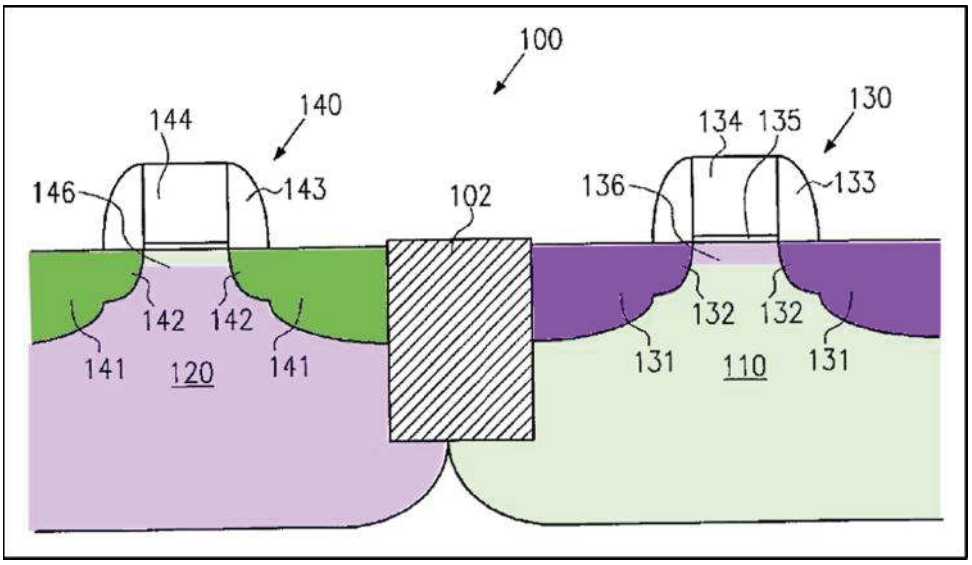
§VIII.B.1.b.

3. Claims 4/25: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain [digital logic formed by/at least] one of either p-channel and n-channel devices."

§§VIII.B.1.c-e, VIII.B.1.h.

4. Claims 5/26: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant."

Wieczorek's Figure 1b illustrates a conventional twin-well architecture, whereby the first active region contains "N-channel transistor 130" in "P-well" 110, and the second active region contains "P-channel transistor 140" in "N-well" 120. Ex.1006, [0012]-[0013], [0004]; Ex.1003, ¶172; §§VIII.B.1.c-d. This mapping satisfies this claim element under Patent Owner's interpretation that a claimed active region can contain "***a transistor***." Ex.1020, 31; Ex.1003, ¶172. A POSITA would have also understood that Wieczorek teaches forming multiple transistors in an active region to save chip area. Ex.1003, ¶172.

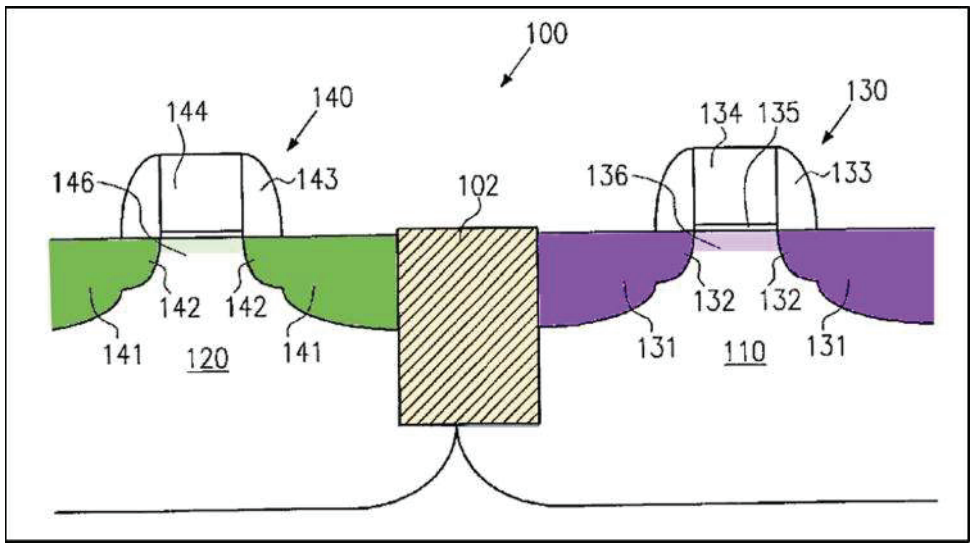


Ex.1006, FIG. 1b. Further, Wieczorek's wells have a graded concentration of dopants. Ex.1006, [0009]-[0011] ("FIG. 2b shows ... a typical dopant profile with

respect to the depth of the respective well structure [110/120]."), [0013], FIGS. 2a-2b; §VIII.B.1.g (discussing graded dopants in P-well 110); Ex.1003, ¶173.

5. Claims 6/27: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region are each separated by at least one isolation region."

As shown below, the first (purple/light purple) and second (green/light green) active regions are separated by "shallow trench isolation 102" (yellow). Ex.1006, [0007]; Ex.1003, ¶174.



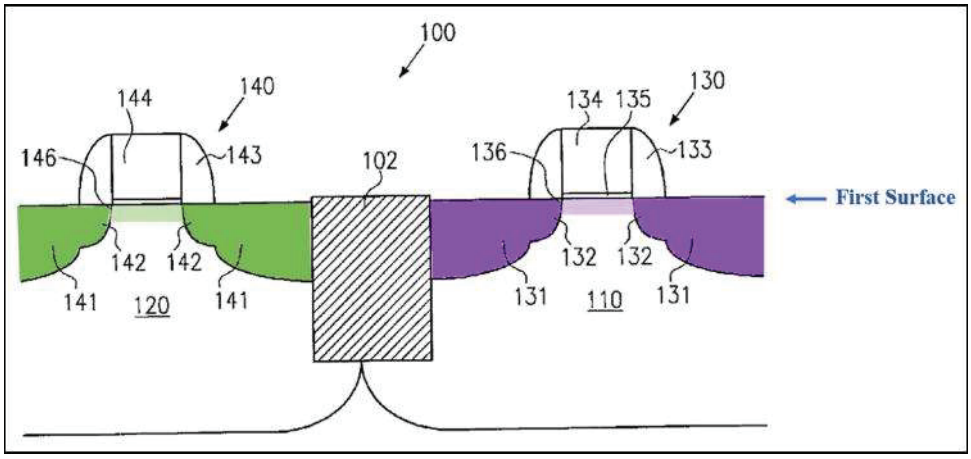
Ex.1006, FIG. 1b.

6. Claims 7/32: "The VLSI semiconductor device of claim [1/21], wherein the graded dopant is fabricated with an ion implantation process."

Wieczorek teaches that the graded dopants in "P-well structure 110 and [] N-well structure 120 are defined by sequentially performed ion implantation processes." Ex.1006, [0008], [0007]-[0011], FIGS. 1a/2a/2b; Ex.1003, ¶175; §§VIII.B.1.f-g.

7. Claim 8: "The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

As shown below, the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (blue). Ex.1006, [0007]-[0010], [0012]-[0013]; Ex.1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions..."), 298-301, FIG. 5-2; Ex.1003, ¶176; §§VIII.B.1.c-d.

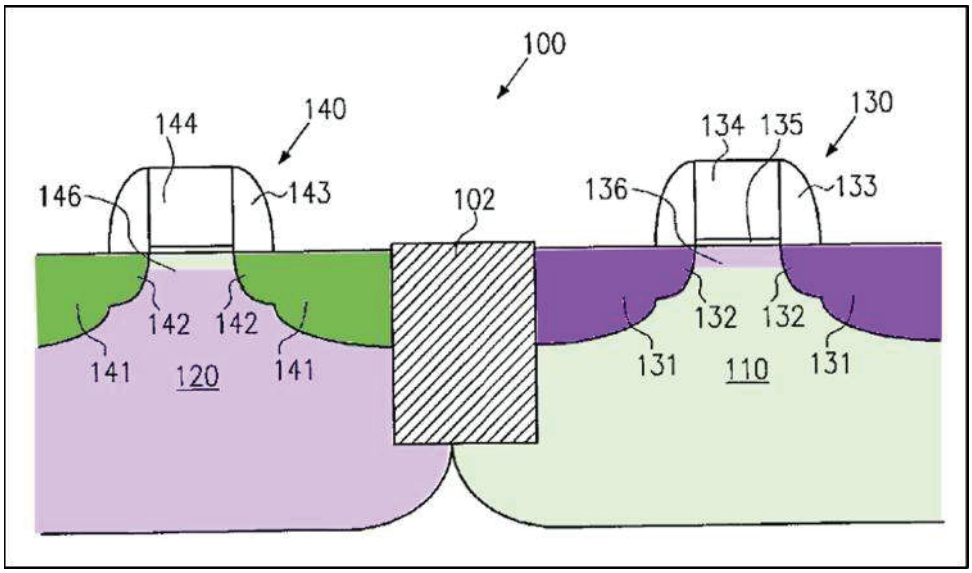


Ex.1006, FIG. 1b.

8. Claims 9/28: "The VLSI semiconductor device of claim [1/21], wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type."

As shown in Figure 1b below, channel region 136 (light purple) of the first active region is formed at the top of P-well 110 and is of the same doping type (p-type) as P-well 110. Ex.1006, [0008] ("for defining the P-well structure 110, typically boron ions are employed"); Ex.1007, 15:28-29; Ex.1003, ¶177. Likewise,

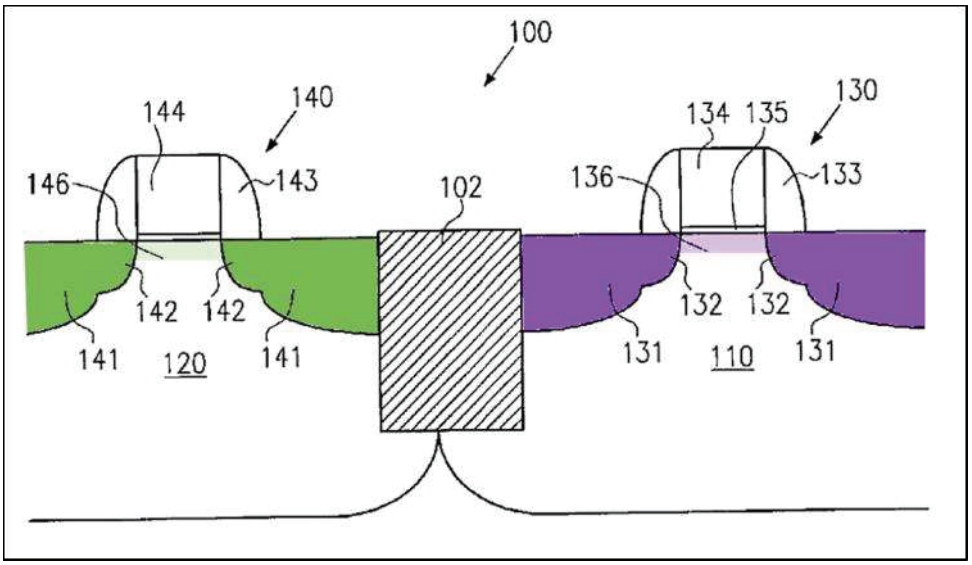
channel region 146 (light green) of the second active region is formed at the top of N-well 120 and is of the same doping type (n-type) as N-well 120. Ex.1006, [0008] ("[f]or defining the N-well structure 120, typically phosphorous or arsenic ions are used"); Ex.1007, 9:33-35; Ex.1003, ¶178.



Ex.1006, FIG. 1b. Those channel regions have a graded dopant concentration, as discussed above. §VIII.B.1.f; Ex.1003, ¶179.

9. Claim 13: "The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel."

Wieczorek-Wolf discloses "a complementary [digital logic] MOS [(CMOS)] transistor pair" comprising "N-channel transistor 130" in the first active region (purple/light purple) and "P-channel transistor 140" in the second active region (green/light green). Ex.1006, [0007], [0012]-[0013]; §VIII.B.1.h; Ex.1003, ¶180.



Ex.1006, FIG. 1b. Each of the CMOS digital logic transistors include a source, drain, gate, and channel. Ex.1003, ¶181. N-channel transistor 130 includes "heavily N-doped source and drain regions 131" (purple), "gate electrode 134," and "channel region 136" (light purple). Ex.1006, [0012]-[0013]; Ex.1003, ¶181. P-channel transistor 140 includes "heavily P-doped source and drain regions 141" (green), "gate electrode 144," and "channel region 146" (light green). *Id.*; §§VIII.B.1.c-d, VIII.B.1.f.

10. Claim 14: "The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM)."

Wieczorek's teaching relied on in this petition is directed to conventional CMOS technology. §VIII.B.1.b. It would have been obvious to fabricate DRAMs, which include transistors and capacitors (Ex.1008B, 589), using Wieczorek's conventional CMOS technology to take advantage of "lower power dissipation []

and smaller soft error rates" of CMOS technology and "the advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible) [which] have made DRAMs the most widely used form of semiconductor memory to date." Ex.1008B, 587, 597; Ex.1003, ¶182. Wieczorek also suggests doing so in teaching the frequent application of its technology to "modern integrated circuits." Ex.1006, [0004], [0026]; Ex.1003, ¶182. Indeed, DRAMs were known to be designed using CMOS technology, and such DRAMs included capacitors." Ex.1008B, 596-597; Ex.1003, ¶182.

Additionally, using Wieczorek's technology to form a DRAM would have merely amounted to combining known, conventional prior art elements (*i.e.*, Wieczorek's CMOS process and known CMOS DRAM designs) according to known methods (*i.e.*, Wieczorek's CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology contemplated by Wolf for DRAM) with another (*i.e.*, Wieczorek's conventional CMOS technology). Ex.1003, ¶183. There would have been reasonable expectation of success with predictable results because Wieczorek's conventional CMOS process was known and would have been used for its intended purpose in manufacturing a known DRAM designed for implementation using CMOS technology. *Id*.

11. Claim 15: "The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate."

§VIII.B.1.b.

12. Claims 16/34: "The VLSI semiconductor device of claim [1/21], wherein the device is a flash memory."

Wieczorek's teaching relied on in this petition is directed to conventional CMOS technology. §VIII.B.1.b. It would have been obvious to fabricate flash memory using Wieczorek's conventional CMOS technology to achieve the benefits of "lower power-dissipation" of CMOS technology and "high density [], small-die size, lower cost, and hot-electron writability of EPROMs, together with the easy erasability, on-board reprogrammability, and electron-tunneling erasure features of EEPROMs." Ex.1008B, 634; Ex.1008A, 808-810; Ex.1003, ¶185. Wieczorek also suggests doing so in teaching the frequent application of its technology to "modern integrated circuits." Ex.1006, [0004], [0026]; Ex.1003, ¶185. Indeed, flash memory devices commonly used CMOS technology. Ex.1008B, 633-635 (describing known "CMOS flash-EEPROM" devices); Ex.1007, 22:16-17 (flash EEPROM is flash memory), 22:10-23:2, FIG. 28 (peripheral flash memory circuit with CMOS transistors); Ex.1003, ¶185; §VIII.A.12.

Additionally, using Wieczorek's technology to form flash memory would have merely amounted to combining known, conventional prior art elements (*i.e.*, Wieczorek's CMOS process and known CMOS flash memory designs) according to

known methods (*i.e.*, Wieczorek's CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology for prior art flash memory) with another (*i.e.*, Wieczorek's conventional CMOS technology). Ex.1003, ¶186. There would have been reasonable expectation of success with predictable results because Wieczorek's conventional CMOS process was known and would have been used for its intended purpose in manufacturing a known flash memory designed for implementation using CMOS technology. *Id*.

13. Claim 17: "The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors."

§§VIII.B.1.h, VIII.B.10.

14. Claims 18/36: "The VLSI semiconductor device of claim [1/21], wherein the device is central processing unit."

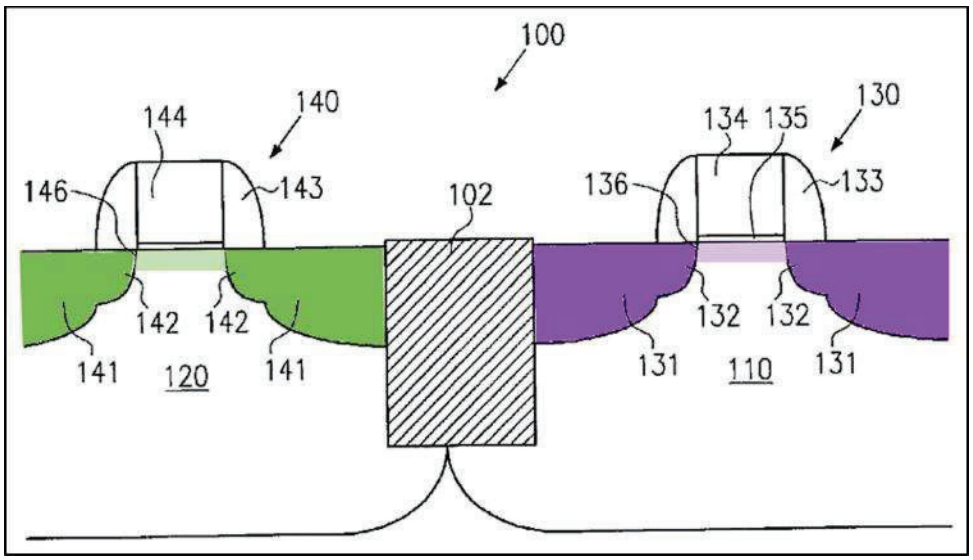
Wieczorek's teaching relied on in this petition is directed to conventional twin-well CMOS technology. §VIII.B.1.b. It would have been obvious to fabricate known microprocessors (CPUs), using Wieczorek's conventional CMOS technology to achieve the benefits of "lower power-dissipation" of CMOS technology in such devices. Ex.1008B, 368-370; Ex.1032, 1334; Ex.1003, ¶188. Wieczorek suggests doing so in teaching the frequent application of its technology to "modern integrated circuits." Ex.1006, [0004], [0026]; Ex.1003, ¶188. Indeed, twin-well CMOS technology was, by the early 2000s, "the dominant CMOS technology in IC production." Ex.1008D, 181; Ex.1003, ¶188.

Rabaey confirms this. Ex.1025, 180 ("The [CMOS] inverter is truly the nucleus of all digital [logic] designs" and, together with other "[logic] gates such as NAND, NOR, or XOR ... form the building blocks for modules such as multipliers and processors."), 37 ("Modern [CMOS] processes are increasingly using a dual-well [(twin-well)] approach that uses both n- and p-wells ..."), 383-84, FIG. 8-6 (showing Intel Pentium processor "designed in a 0.18mm CMOS technology."); Ex.1003, ¶189. Sze also confirms this, describing a system-on-a-chip that includes CMOS "***logic IC (e.g., CPU)***" fabricated using twin-well CMOS technology. Ex.1022, 525-26, FIGS. 37-38; Ex.1003, ¶189.

Additionally, using Wieczorek's technology to form CPUs would have merely amounted to combining known, conventional prior art elements (*i.e.*, conventional twin-well CMOS process described in Wieczorek and known CPU designs) according to known methods (*i.e.*, Wieczorek's conventional twin-well CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology for prior art CPUs) with another (*i.e.*, Wieczorek's conventional CMOS technology). Ex.1003, ¶190. There would have been a reasonable expectation of success with predictable results because Wieczorek's conventional twin-well CMOS process was known and would have been used for its intended purpose in manufacturing known CPUs, designed for implementation using CMOS technology. *Id*.

15. Claims 20/38: "The VLSI semiconductor device of claim [1/21], wherein each of the first and second active regions are in the lateral or vertical direction."

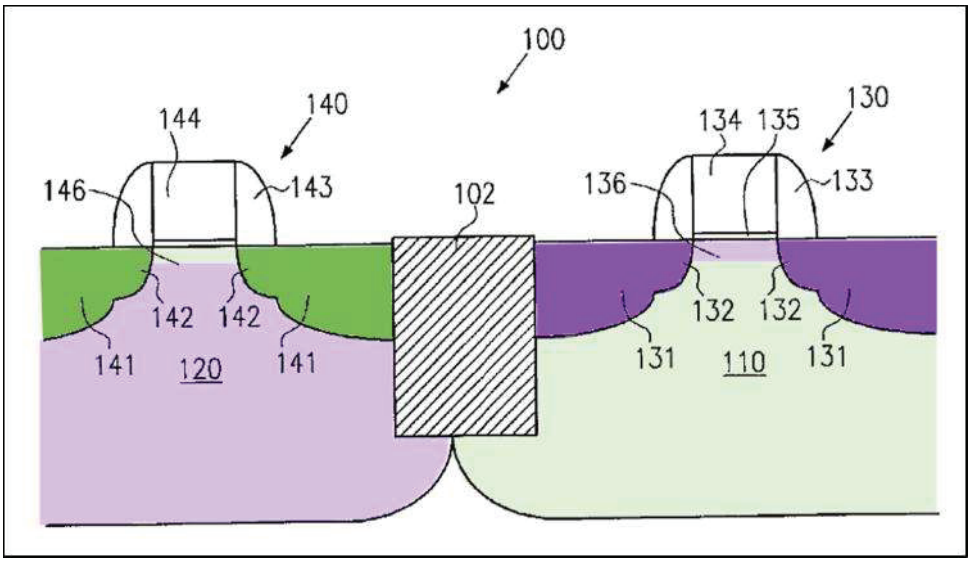
As shown in Figure 1b below, the first (purple/light purple) and second (green/light green) active regions are in the lateral direction. Ex.1003, ¶191.



Ex.1006, FIG. 1b.

16. Claim 22: "The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate."

As explained in §VIII.B.1.b, n-type and p-type substrates are both suitable for Wieczorek's CMOS device. §VIII.B.1.b; Ex.1003, ¶192. With an n-type substrate, element [21.2] is met by mapping the first active region to the source/drain/channel regions 141/142/146 (green/light green) of pMOS transistor 140, and element [21.3] is met by mapping the second active region to the source/drain/channel regions 131/132/136 (purple/light purple) of nMOS transistor 130. *Id.*



Ex.1006, FIG. 1b.

17. Claim 33: "The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device."

Wieczorek teaches "a complimentary MOS [(CMOS)] transistor pair" formed in and including a substrate. Ex.1006, [0007], [0012]-[0013]; Ex.1003, ¶193; §VIII.B.1.b.

18. Claim 35: "The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions."

§§VIII.B.1.e/h, VIII.B.10/12/14. MOS transistors are commonly used as capacitors to form dynamic circuits such as voltage bootstrapping circuits, charge pump circuits, delay/timing circuits, and to form decoupling capacitors ("decaps"). Ex.1003, ¶¶194-197. Hodges' figure below shows an NMOS transistor configured

as a capacitor by connecting its gate to V_{DD} and its source/drain to V_{SS}. Ex.1038, 493-494.

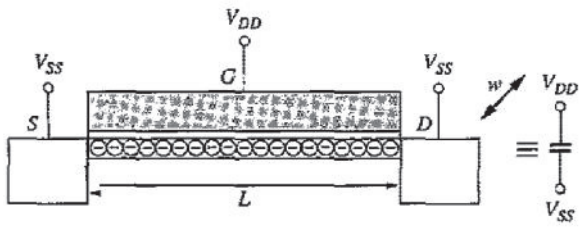


Figure 11.11
On-chip decap using MOS capacitance.

Id., FIG. 11.11. A POSITA would have understood (and found it obvious) that some of Wieczorek's transistors formed in some of the first/second active regions are configured as capacitors, for the same reasons discussed above regarding claim 35 in Ground I. §VIII.A.17; Ex.1003, ¶195. For example, the voltage bootstrapping circuit below—a "very useful" and commonly used circuit—includes a transistor configured as a capacitor (C_{boot}) connected to other transistors (M1-M3). Ex.1041, 370-373.

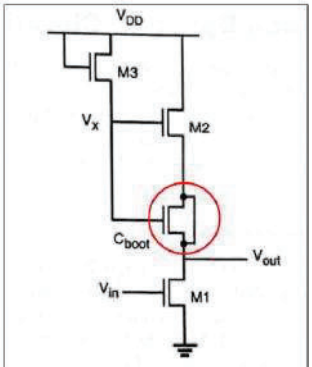
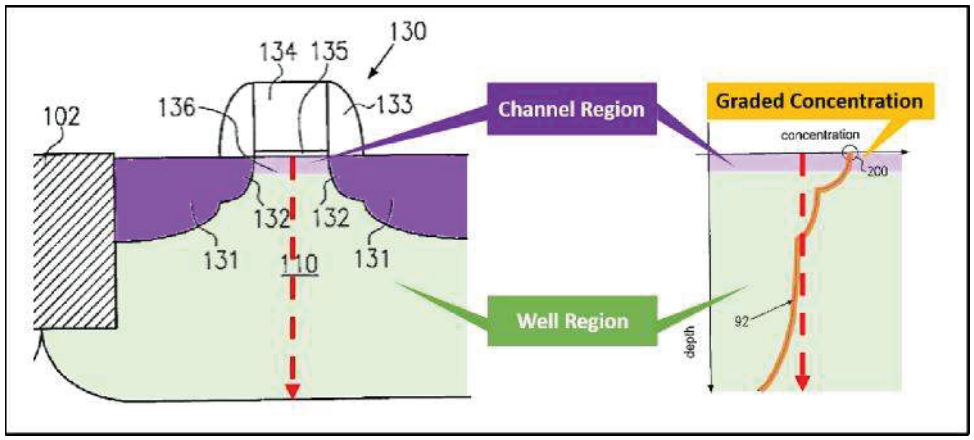


Figure 9.13 Realization of the bootstrapping capacitor with a dummy MOS device.

Id., FIG. 9.13. A POSITA would also find it obvious to configure transistors as decaps to filter out power supply noise and reduce "*IR* drop." Ex.1038, 493; *id.*, 498499; Ex.1003, ¶196. There is reasonable expectation of success with predictable results because the use of transistors as capacitors was a well-known, intended use of MOS transistors. *Id.*; §VIII.A.17.

19. Claim 40: "The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well."

§VIII.B.1.g. As illustrated below, Wieczorek's graded dopant concentration is downward-sloping throughout each well (green) and moves carriers from any region of the well to deeper areas of Wieczorek-Wolf's substrate where there is no well. Ex.1008C, 525, FIG. 8-1(e); §VIII.B.1.b; Ex.1003, ¶198.



Ex.1006, FIGS. 1b/2b.

C. GROUNDS III/IV

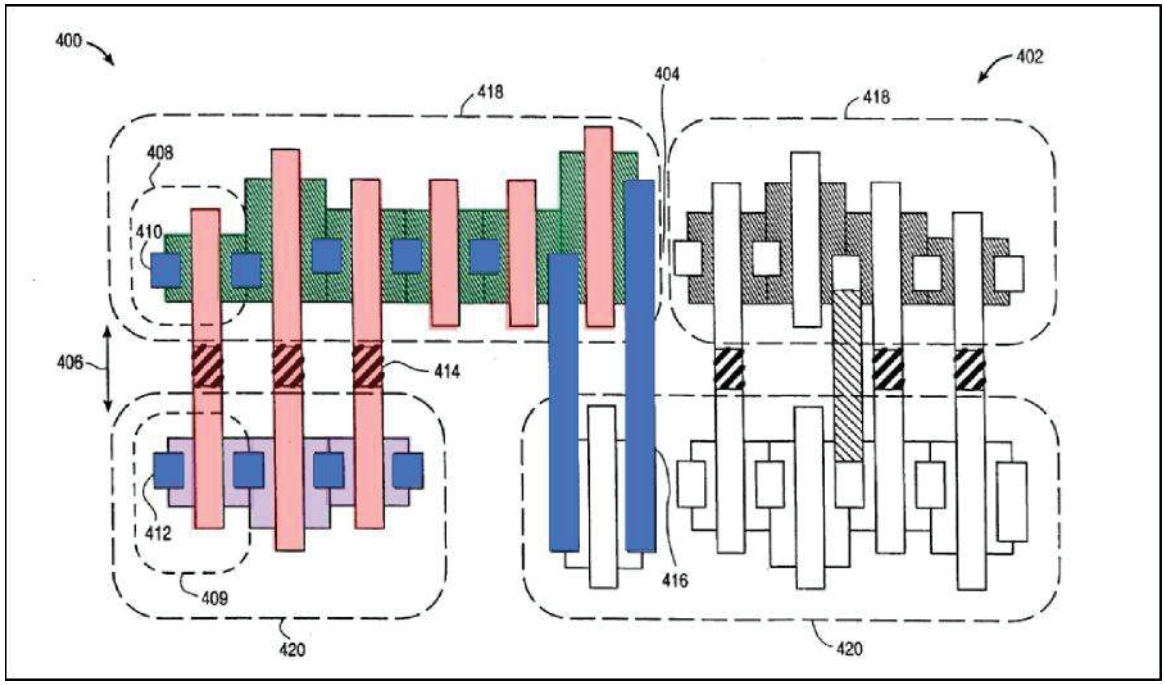
Several claim elements of the Challenged Claims recite "transistors" or "devices." *See* Elements [1.2]-[1.4]/[1.7]/[21.2]-[21.4]/[39.2]-[39.4]/[41.2]-[41.4], [42.2]-[42.4]; Cls. 4-5/13/25-26. As discussed under Grounds I-II, Patent Owner interprets these elements as requiring one or more transistors, and not a plurality of transistors. §§VIII.A.1.c-d, VIII.B.1.c-d.

The present Grounds III-IV mirror Grounds I-II, respectively, except that Gupta is explicitly combined with Kawagoe of Ground I and Wieczorek-Wolf of Ground II to render obvious those claim elements under an interpretation of "transistors" or "devices" to require a plurality of such devices. Ex.1003, ¶¶199-208.

Gupta is directed to "automatically producing layouts for CMOS circuits," recognizing that "semiconductor chips [have] become ever larger, incorporating ever more devices." Ex.1014, 1:7-10, 1:28-31. A "primary goal" of semiconductor chip development has therefore been to minimize the chip area required to form a circuit so that more transistors can be packed in the same chip, regardless of the technology and chip fabrication process. Ex.1014, 1:28-35 ("[I]t becomes increasingly important to minimize semiconductor area used by a given number of devices. Conservation of semiconductor area is a primary goal in semiconductor chip development...."); Ex.1003, ¶201. Gupta further explains that good circuit layout practice dictates forming as many transistors in the same active region through diffusion abutment as

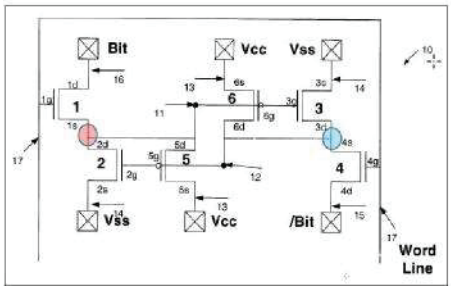
possible to minimize area-wasting diffusion gaps. Ex.1014, 1:52-54 ("One technique conserves area by placing transistors so as to ***share diffusion area***."), 2:17-21 ("Transistors which are abutted in a layout form transistor chains. It is desirable to produce a layout with a ***maximum number of transistors chained*** so as to minimize diffusion gaps."). Gupta describes several techniques to achieve optimal layout, such as transistor folding and chaining. Ex.1014, 1:49-2:24, 3:64-4:1, FIGS. 2-3.

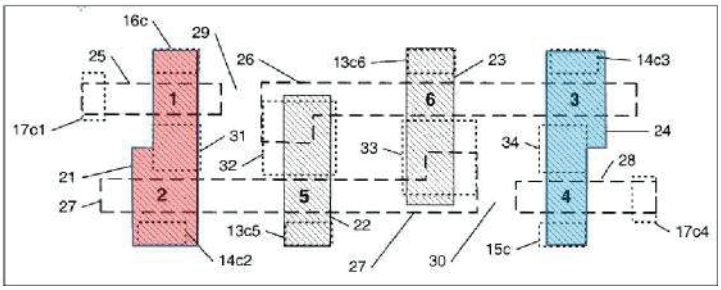
Gupta's Figure 4 (below)—where transistor gates and metal contacts that overlay the active regions are colored red and blue, respectively—illustrates ***six*** chained PMOS transistors formed in a p-channel active region (green) and ***three*** chained NMOS transistors formed in an n-channel active region (purple). Ex.1014, 4:12-43; Ex.1003, ¶202.



Ex.1014; FIG. 4

Jin confirms that transistors arranged as in Gupta are formed in a common active region. Ex.1003, ¶203. Below left is the circuit schematic of an SRAM cell, and the cell layout (below right) shows transistors 1/2 in active region 21 (red), and transistors 3/4 in active region 24 (blue). Ex.1015, 6:17-29; Ex.1025, 48 ("*Diffusion regions* (n^+ and p^+), which define the areas where transistors can be formed[,] are often called the *active areas*.") (italics in original).





Ex.1015, FIGS. 1-2.

A POSITA would have been motivated to fabricate a CMOS chip according to the combined teachings of Kawagoe and Gupta (and likewise, of Wieczorek-Wolf and Gupta) to achieve high packing density (taught by Gupta) at submicron dimensions (for which a twin-well CMOS process of the type taught in Kawagoe and Wieczorek-Wolf was known to be the technology of choice (Ex.1008B, 373, 388)). Ex.1003, ¶204. The combinations gain the additional benefit of improved immunity to soft errors through appropriate well doping. Ex.1007, 15:62-16:11; Ex.1003, ¶205. Combining Gupta with Kawagoe or Wieczorek-Wolf merely amounts to (1) use of a known technique (*i.e.*, Kawagoe's or Wieczorek's CMOS

fabrication process) to improve similar devices (*i.e.*, CMOS chips designed with Gupta's layout) in the same way (*i.e.*, to achieve submicron dimensions and improve immunity to soft errors); (2) use of a known technique (*i.e.*, Gupta's optimal layout generation) to improve similar devices (*i.e.*, submicron CMOS chips fabricated according to Kawagoe or Wieczorek-Wolf's CMOS fabrication process) in the same way (*i.e.*, to minimize chip area and increase packing density); and (3) combining prior art elements (*i.e.*, Kawagoe or Wieczorek's CMOS fabrication process and Gupta's CMOS layout generation) according to known methods (*i.e.*, as taught by Kawagoe or Wieczorek and Gupta). Ex.1003, ¶205. There is reasonable expectation of success with predictable results because Kawagoe's and Wieczorek's CMOS fabrication process would be used for their intended purpose of fabricating CMOS circuits according to known CMOS layouts generated by Gupta, also for its intended purpose. *Id*. Further, Gupta's optimal circuit layout is process-agnostic and applies to the layout of ***any*** CMOS semiconductor chip, including the layout of CMOS chips fabricated according to the teachings of Kawagoe and/or Wieczorek-Wolf. *Id.*

A POSITA would have understood that, in such a combination, the active regions in Gupta's figures are formed in wells (n-channel active regions are formed in p-wells, and p-channel active regions are formed in n-wells) having downward-sloping graded dopant concentrations as shown in Kawagoe's Figure 17 and Wieczorek's Figure 2b. *Id.*, ¶206. The n-channel active region (purple) in Gupta's

Figure 4 is an example of the claimed first active region, and the p-channel active region (green) is an example of the claimed second active region. *Id*., ¶206. The two active regions are adjacent and separated by an isolation region (field oxide), as required under elements [1.3], [21.3], [39.3], [41.3], and [42.3] and claims 6 and 27. Ex.1014, 1:16-19, 4:39; Ex.1008A, 818-820; §§VIII.A.1.d, VIII.A.6, VIII.B.1.d, VIII.B.5, Ex.1003, ¶206.

Conversely, a POSITA would have understood that each of the active regions of Kawagoe's and Wieczorek's CMOS devices typically contain many transistors, as taught by and illustrated in Gupta's Figure 4. Ex.1003, ¶207. This is the case whether the device is a DRAM, flash memory, logic device with capacitors, or CPU (as claimed in claims 14, 16-18, 34-36). *Id.* Each such device is a "very large scale integrated circuit" for which "it becomes increasingly important to minimize semiconductor area used[,]" and this requires forming as many transistors as possible in any active region. Ex.1014, 1:13-14, 1:28-34, 2:17-21; Ex.1003, ¶207.

In light of the above, Kawagoe in view of Gupta renders claims 1-9, 13-14, 16-18, 20-21, 23-28, 32-36, and 38-42 obvious (Ground III). Likewise, Wieczorek-Wolf in view of Gupta renders claims 1-2, 4-9, 13-18, 20-23, 25-28, 32-36, and 3842 obvious (Ground IV). Ex.1003, ¶208.

IX. THE BOARD SHOULD INSTITUTE IPR

A. 35 U.S.C. § 314(a)

The merits of this Petition are strong, which alone warrants institution. On June 21, 2022, Director Vidal issued an interim procedure regarding application of the *Fintiv* factors clarifying that "the PTAB will not deny institution [] under *Fintiv* (i) when a petition presents compelling evidence of unpatentability." Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," 9 (June 21, 2022). Here, each ground in the Petition presents compelling evidence of unpatentability. For example, Ground I is a single-reference obviousness ground explaining how Kawagoe discloses or, at a minimum, renders obvious nearly all of the Challenged Claims. This evidence, "if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable" (*id*., 4) and the Board must decline to exercise its discretion under §314(a). *Id.*; *PopSockets LLC v. Flygrip, Inc.*, IPR2022-00938, Paper 8 (P.T.A.B. Nov. 1, 2022).

The *Fintiv* factors also weigh in favor of institution. ***First***, this Petition is substantially identical to the Petition filed in IPR2023-00420. The Petition in IPR2023-00420 was filed on December 28, 2022, an Institution Decision is expected on or before June 2023, and a final written decision (FWD) should issue in June 2024. Petitioner is filing a motion for joinder with respect to IPR2023-00420.

While trial in the District Court Case is set for December 2023, the Director noted in its Interim Procedure that "[a] court's scheduled trial date [] is not by itself a good indicator of whether the district court trial will occur before the statutory deadline for a [FWD]," and directed the PTAB to consider "statistics on median time-to-trial for civil actions in the district court in which the parallel litigation resides." Interim Procedure, 8-9. The median time to trial in the Western District of Texas is 28.3 months (Ex.1024, 37), giving a trial date of no earlier than June 2024.

Additionally, on December 27, 2022, the district court severed the claims against co-defendant Intel and transferred to the District of Oregon (*see* Section II), while staying Greenthread's claims against Dell based on the Accused Intel Products. (Ex.1042, 22). The Markman hearing that was initially scheduled for January 19th, 2023 was subsequently canceled, without any indication if or when it would be rescheduled. (Ex.1043). Dell also has a pending motion to transfer venue, which may result in further delays to the existing schedule.

Second, fact discovery just recently opened in the District Court litigation, and as mentioned above the claims against Dell based on the Accused Intel Products have been stayed. Because the district court has not yet invested significant resources this factor weighs against discretionary denial. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 13 (P.T.A.B. May 19, 2021).

Third, "there is a reasonable likelihood that the Board will address the overlapping validity issues prior to the district court reaching them at trial..., thereby providing the possibility of simplifying issues for trial." *Juniper Networks, Inc. v. Packet Intelligence LLC*, IPR2020-00339, Paper 21 at 18 (P.T.A.B Sept. 10, 2020).

B. 35 U.S.C. § 325(d)

The Board should likewise not deny institution under §325(d) because all six *Becton Dickinson* factors weigh in favor of institution. *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017); *see also Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020).

The Board has consistently "held that a reference that 'was neither applied against the claims nor discussed by the Examiner' does not weigh in favor of exercising ... discretion under §325(d)." *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 7-11 (P.T.A.B. Nov. 5, 2019). Here, Kawagoe, Gupta and Wolf Volumes 1-3 were not cited. Wieczorek and Wolf Volume 4 were cited, but were not discussed. Moreover, the arguments presented herein are not the same or substantially the same as those considered during prosecution.

Wieczorek and Kawagoe are also not cumulative of references considered during prosecution. Hong, the only reference mentioned during prosecution, is not prior art because it was filed on August 31, 2005, long after the claimed priority date

of the ’222 Patent. Ex.1027; Ex.1002, 176-177. Further, Wieczorek and Kawagoe are not cumulative to any art cited or discussed during prosecution of the ’222 Patent’s parents, such as Rhodes, Jastrzebski, Kamins, or Hueting. Indeed, other than during prosecution of the parent ’842 and ’481 Patents where the non-prior-art Hong was also the only reference discussed, prosecution of the other parent applications involved claims that are wholly different from the Challenged Claims. *Fasteners for Retail*, IPR2019-00994, Paper 9 at 10 (refusing to deny institution because, despite allegation that the petition art was considered during prosecution, “enough differences exist [between the two sets of claims] to convince us that the challenges presented in this petition are not cumulative to those already considered by the examiner.”) Most significantly, none of the claims prosecuted in the parent applications (other than the ’842 and ’481 Patents) claim graded dopants ***in an active region*** to aid carrier movement “***[towards/to] an area of the substrate where there are no active regions***” as claimed in the Challenged Claims. For example, the claims of the parent ’070 Patent are directed to bipolar transistors (not at issue in the District Court Case or in the present Petition) and claim aiding carrier movement “to a collector in the substrate,” and not “[towards/to] an area of the substrate where there are no active regions.” Ex.1034, Cl. 1; Ex.1003, ¶46. Other claims that claim graded dopant in an active region were withdrawn prior to substantive examination. Ex.1016, 73 (withdrawing claims 1-2); Ex.1028, 9 (same); Ex.1029, 7 (canceling

claims 1-2); Ex.1030, 18 (same); Ex.1003, ¶46. "Here, the Examiner did not consider [] the grounds asserted in the Petition, and certainly not with respect to the challenged claims" and therefore "there [is] no overlap between arguments made during examination and in the Petition." *Bowtech*, Paper 14 at 5-6.

C. Just-Filed Sony Petition Does Not Warrant Denying Institution

This Petition is Dell's first petition challenging claims of the '222 Patent. On December 12, 2022, Sony filed a petition challenging claims 1-44 of the '222 Patent. *See Sony Group Corp. v. Greenthread LLC*, No. IPR2023-00324, Paper 1 (P.T.A.B. Dec. 12, 2022). Intel likewise filed a petition challenging claims 1-9, 13-18, 20-28, 32-36, and 38-42. *See Intel Corp. v. Greenthread LLC*, No. IPR2023-00420, Paper 1 (P.T.A.B. Dec. 28, 2022). This Petition is identical to the Intel Petition in substance, while being substantively different than the Sony petition. Dell is concurrently filing a motion for joinder to join the Intel IPR filed on the '222 Patent – IPR2023-00420.

This Petition should not be denied in view of the relationship between Sony and Dell. While Sony listed Dell as an RPI in IPR2023-00324, the two are unrelated companies, and have not funded, reviewed, or directed either's IPR filings. Dell further has other interests to protect due to other accused Dell products that are not provided by Sony. The prior art and grounds do not overlap in any way with the Sony petition. Finally, neither the Board nor the Patent Owner have substantively

addressed the Sony Petition removing any potential that Dell is using the Sony case as a roadmap. The *General Plastic* factors thus weigh strongly against discretionary denial. *Xilinx, Inc. v. Arbor Global Strategies, LLC*, IPR2020-01568, Paper 12 at 10 (P.T.A.B. Mar. 5, 2021).

Dated: January 27, 2023

Respectfully submitted,

/Christopher TL Douglas/
Christopher TL Douglas
Reg. No. 56,950
Counsel for Petitioner

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222 contains, as measured by the word-processing system used to prepare this paper, 13,999 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Dated: January 27, 2023

Respectfully submitted,

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CERTIFICATE OF SERVICE ON PATENT OWNER UNDER 37 C.F.R. § 42.105

I hereby certify that on January 27, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center:

Munck Wilson Mandala LLP
P.O. Drawer 800889
Dallas, TX 75230

A courtesy copy was also served via electronic mail on Patent Owner's counsel of record in Western District of Texas litigation:

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Dated: January 27, 2023

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Christopher TL Douglas
Counsel for Petitioner Reg. No. 56,950

APPENDIX A

Element	Claim Language
[1.pre]	A VLSI semiconductor device, comprising:
[1.1]	a substrate of a first doping type at a first doping level having a surface;
[1.2]	a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[1.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[1.4]	transistors formed in at least one of the first active region or second active region;
[1.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
[1.6]	at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,
[1.7]	wherein at least some of the transistors form digital logic of the VLSI semiconductor device.
2	The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.
3	The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
4	The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.
5	The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or nchannel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.
6	The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

Element	Claim Language
7	The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.
8	The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.
9	The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
13	The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.
14	The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).
15	The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.
16	The VLSI semiconductor device of claim 1, wherein the device is a flash memory.
17	The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.
18	The VLSI semiconductor device of claim 1, wherein the device is central processing unit.
20	The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.
[21.pre]	A VLSI semiconductor device, comprising:
[21.1]	a substrate of a first doping type at a first doping level having a surface;
[21.2]	a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[21.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[21.4]	transistors formed in at least one of the first active region or second active region;

Element	Claim Language
[21.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and
[21.6]	at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and
[21.7]	wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.
22	The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate.
23	The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.
24	The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
25	The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.
26	The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n⁻wells or p⁻wells, respectively, and each well has at least one graded dopant.
27	The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.
28	The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
32	The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.
33	The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.
34	The VLSI semiconductor device of claim 21, wherein the device is a flash memory.

Element	Claim Language
35	The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.
36	The VLSI semiconductor device of claim 21, wherein the device is central processing unit.
38	The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.
[39.pre]	A semiconductor device, comprising:
[39.1]	a substrate of a first doping type at a first doping level;
[39.2]	a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[39.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[39.4]	transistors formed in at least one of the first active region or second active region;
[39.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active region to at least one substrate area where there is no active region.
40	The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.
[41.pre]	A semiconductor device, comprising:
[41.1]	a substrate of a first doping type at a first doping level;
[41.2]	a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[41.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[41.4]	transistors formed in at least one of the first active region or second active region; and

Element	Claim Language
[41.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.
[42.pre]	A semiconductor device, comprising:
[42.1]	a substrate of a first doping type at a first doping level;
[42.2]	a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[42.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[42.4]	transistors formed in at least one of the first active region or second active region; and
[42.5]	at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.