Exhibit 8

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

GREENTHREAD, LLC, **Plaintiff,** **v.** **INTEL CORPORATION, DELL INC., AND DELL TECHNOLOGIES INC.,** **Defendants.**	**Case No. 6:22-cv-00105-ADA**

GREENTHREAD'S AMENDED PRELIMINARY INFRINGEMENT CONTENTIONS

Plaintiff Greenthread, LLC ("Greenthread") hereby provides its amended infringement contentions, including identification of asserted claims, the priority date for each asserted claim, accused products, and accompanying document production. Claim charts are attached as Exhibits A-1 through A-6, B-1 through B-6, C-1 through C-6, D-1, D-2, D-3, and D-6, and E-1 through E-6 and F-1, F-2, F-3, and F-6.

Greenthread has thus far received only the initial document production of August 22, 2022 from Intel Corporation ("Intel"), Dell Inc., and Dell Technologies Inc. (Dell Inc. and Dell Technologies Inc. are collectively "the Dell Defendants" or "Dell," and Intel Corporation and the Dell Defendants are collectively "Defendants"). Greenthread has procured limited physical testing to the extent practicable, of certain products believed to be representative of, and similar to, the accused infringing products in pertinent respects. Greenthread explicitly reserves the right to supplement or alter its disclosures herein, as a matter of right, as permitted by the Court, based on

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the Court's claim constructions, based on additional information obtained through formal discovery or other means, and/or based on other circumstances.

I. ASSERTED CLAIMS AND PRIORITY DATE

Based on the information presently available to it, Greenthread identifies the asserted claims of each asserted patent that Greenthread alleges is infringed by Defendants, and the priority date of those claims, as set forth in the table below. Based on the information presently available to it, Greenthread alleges that all asserted claims of each particular asserted patent are entitled to the same priority date.

Patent	Asserted Claims[1]	Priority Date of Asserted Claims
10,510,842 ("the '842 patent")	1, 2, 4-10, 12-18	September 3, 2004
10,734,481 ("the '481 patent")	1-9, 13, 15-20, 22-27, 31-36	September 3, 2004
11,121,222 ("the '222 patent")	1-9, 13, 15- 21, 23-28, 32-42, 44	September 3, 2004
8,421,195 ("the '195 patent")	1-3, 5-6	September 3, 2004
9,190,502 ("the '502 patent")	7-9, 11	September 3, 2004
11,316,014 (the "'014 Patent")	1-9, 13, 15-21, 23-28	September 3, 2004

Greenthread notes that the claims identified in the table reflect the asserted claims in this case, and the absence of a claim from the list does not imply that the claim is not infringed. Greenthread explicitly reserves the right to supplement or alter its identification of asserted claims and priority dates, as a matter of right, as permitted by the Court, based on any further claim

[1] To the extent Exhibits A-1 through A-6, B-1 through B-6, C-1 through C-6, D-1, D-2, D-3, and D-6, and E-1 through E-6 and F-1, F-2, F-3, and F-6 describe infringement of additional claims those claims are likewise asserted.

constructions, additional information obtained through formal discovery or other means, and/or based on other circumstances.

II. ACCUSED PRODUCTS

Based upon information presently available to it, Greenthread asserts infringement by the accused products set forth below in this section. For each accused product identified below, Greenthread's contentions apply to the accused product and any other similar past, present, or future products, as well as systems incorporating the accused products or other products with the same or substantially similar features.

A. Intel Accused Products

As described further in Exhibits A-1 through A-6 and Exhibits B-1 through B-6 below, Intel's CPU products and Intel's flash memory products infringe one or more asserted claims of each of the asserted patents.

Intel Accused CPUs include all CPUs designed or manufactured (in whole or in part) by Intel, that have the same or similar structures, features, or functionalities as the exemplary Intel Core i7 11800H CPU shown in Exhibits A-1 through A-6. As shown in Exhibits A-1 through A-6, Intel Accused CPUs each infringe one or more claims of U.S. Patent Nos. 8,421,195 (claims 1-3, 5-6), 9,190,502 (claims 7-9), 10,510,842 (claims 1-2, 4-10, 12-18), 10,734,481 (claims 1-9, 13, 15, 17-18, 20, 22-27, 31-32, 34-35), 11,121,222 (claims 1-9, 13, 15, 17-18, 20-21, 23-28, 32-33, 35-36, 38-42, 44), 11,316,014 (claims 1-9, 13, 15, 17-18, 20-21, 23-28). Intel Accused CPUs include the 12th generation semiconductor products labeled as "Alder Lake," the 11th generation semiconductor products labeled as "Tiger Lake," the 10th generation semiconductor products labeled as "Comet Lake," and certain Intel Atom processors. The following listing of Intel 10th, 11th, and 12th generation and Atom semiconductor products is derived from publicly available

information at Intel's website, e.g., as noted in Exhibit G to Greenthread's Complaint (Dkt. 1-7), and also from https://www.cpu-world.com/CPUs/Atom/index.html.

Greenthread reserves the right to supplement the list of Intel Accused Products as discovery proceeds.

Intel Atom Processors

1. Intel Atom C2308
2. Intel Atom C2316
3. Intel Atom C2338
4. Intel Atom C2350
5. Intel Atom C2358
6. Intel Atom C2508
7. Intel Atom C2516
8. Intel Atom C2518
9. Intel Atom C2530
10. Intel Atom C2538
11. Intel Atom C2550
12. Intel Atom C2558
13. Intel Atom C2718
14. Intel Atom C2730
15. Intel Atom C2738
16. Intel Atom C2750
17. Intel Atom C2758
18. Intel Atom C3308
19. Intel Atom C3336
20. Intel Atom C3338
21. Intel Atom C3338R
22. Intel Atom C3436L
23. Intel Atom C3508
24. Intel Atom C3538
25. Intel Atom C3558
26. Intel Atom C3558R
27. Intel Atom C3708
28. Intel Atom C3750
29. Intel Atom C3758
30. Intel Atom C3758R
31. Intel Atom C3808
32. Intel Atom C3830
33. Intel Atom C3850
34. Intel Atom C3858
35. Intel Atom C3950
36. Intel Atom C3955
37. Intel Atom C3958
38. Intel Atom C5115
39. Intel Atom C5125
40. Intel Atom C5310
41. Intel Atom C5315
42. Intel Atom C5320
43. Intel Atom C5325
44. Intel Atom P5322
45. Intel Atom P5332
46. Intel Atom P5342
47. Intel Atom P5352
48. Intel Atom P5362
49. Intel Atom P5721
50. Intel Atom P5731
51. Intel Atom P5742
52. Intel Atom P5752
53. Intel Atom P5942B
54. Intel AtomP5931B
55. Intel Atom P5962B
56. Intel Atom P5921B
57. Intel Atom T5700
58. Intel Atom x6200FE
59. Intel Atom x6211E
60. Intel Atom x6212RE
61. Intel Atom x6413E
62. Intel Atom x6414RE
63. Intel Atom x6425E
64. Intel Atom x6425RE
65. Intel Atom x6427FE

12th Generation "Alder Lake" Intel Products

1. Intel Core i5-12400

2. Intel Core i5-12400F
3. Intel Core i5-12400T
4. Intel Core i5-12450H
5. Intel Core i5-12500
6. Intel Core i5-12500E
7. Intel Core i5-12500H
8. Intel Core i5-12500T
9. Intel Core i5-12500TE
10. Intel Core i5-12600
11. Intel Core i5-12600KF
12. Intel Core i5-12600H
13. Intel Core i5-12600HE
14. Intel Core i5-12600T
15. Intel Core i5-12600K
16. Intel Core i5-12600KF
17. Intel Core i7-12650H
18. Intel Core i7-12700
19. Intel Core i7-12700E
20. Intel Core i7-12700F
21. Intel Core i7-12700H
22. Intel Core i7-12700T
23. Intel Core i7-12700TE
24. Intel Core i7-12800H
25. Intel Core i7-12800HE
26. Intel Core i7-12700K
27. Intel Core i7-12700KF
28. Intel Core i9-12900
29. Intel Core i9-12900E
30. Intel Core i9-12900F
31. Intel Core i9-12900H
32. Intel Core i9-12900HK
33. Intel Core i9-12900T
34. Intel Core i9-12900TE
35. Intel Core i9-12900K
36. Intel Core i9-12900KF
37. Intel Core i9-12900KF

11th Generation "Tiger Lake" Intel Products

1. Intel Core i3 11100HE
2. Intel Core i3 1115G4E
3. Intel Core i3 1115GRE
4. Intel Core i3 1120G4
5. Intel Core i3 1125G4
6. Intel Core i3 1110G4
7. Intel Core i3 1115G4
8. Intel Core i5 11500HE
9. Intel Core i5 11320H
10. Intel Core i5 1155G7
11. Intel Core i5 11260H
12. Intel Core i5 11400H
13. Intel Core i5 11500H
14. Intel Core i5 11600
15. Intel Core i5 11600
16. Intel Core i5 11600T
17. Intel Core i5 11500
18. Intel Core i5 11600KF
19. Intel Core i5 11600K
20. Intel Core i5 11400T
21. Intel Core i5 11500T
22. Intel Core i5 11400F
23. Intel Core i5 11400
24. Intel Core i5 11300H
25. Intel Core i5 1140G7
26. Intel Core i5 1145G7
27. Intel Core i5 1145GZE
28. Intel Core i5 1145GRE
29. Intel Core i5 1135G7
30. Intel Core i5 1130G7
31. Intel Core i7 11850HE
32. Intel Core i7 11600H
33. Intel Core i7 11390H
34. Intel Core i7 1195G7
35. Intel Core i7 11800H
36. Intel Core i7 11850H
37. Intel Core i7 11700KF
38. Intel Core i7 11700F
39. Intel Core i7 11700
40. Intel Core i7 11700T
41. Intel Core i7 11700K
42. Intel Core i7 11370H
43. Intel Core i7 1180G7
44. Intel Core i7 11375H
45. Intel Core i7 1185GRE
46. Intel Core i7 1185G7E
47. Intel Core i7 1167G7
48. Intel Core i7 1185G7
49. Intel Core i7 1165G7
50. Intel Core i7 1160G7
51. Intel Core i9 11950H

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52. Intel Core i9 11980HK
53. Intel Core i9 11900H
54. Intel Core i9 11900
55. Intel Core i9 11900F
56. Intel Core i9 11900T
57. Intel Core i9 11900KF
58. Intel Core i9 11900K

10th Generation "Comet Lake" Intel Products

1. Intel Core i3 10105
2. Intel Core i3 10105F
3. Intel Core i3 10105T
4. Intel Core i3 10305
5. Intel Core i3 10305T
6. Intel Core i3 10325
7. Intel Core i3 10100Y
8. Intel Core i3 10100F
9. Intel Core i3 10100
10. Intel Core i3 10100E
11. Intel Core i3 10100T
12. Intel Core i3 10100TE
13. Intel Core i3 100300
14. Intel Core i3 100300T
15. Intel Core i3 10320
16. Intel Core i3 10110U
17. Intel Core i3 10110Y
18. Intel Core i3 1000G1
19. Intel Core i3 1000G4
20. Intel Core i3 1005G1
21. Intel Core i5 10505
22. Intel Core i5 10500H
23. Intel Core i5 10200H
24. Intel Core i5 10310U
25. Intel Core i5 1038NG7
26. Intel Core i5 10400
27. Intel Core i5 10400F
28. Intel Core i5 10400T
29. Intel Core i5 10500
30. Intel Core i5 10500E
31. Intel Core i5 10500T
32. Intel Core i5 10500TE
33. Intel Core i5 10600
34. Intel Core i5 10600K
35. Intel Core i5 10600KF
36. Intel Core i5 10600T
37. Intel Core i5 10300H
38. Intel Core i5 10400H
39. Intel Core i5 10210U
40. Intel Core i5 10210Y
41. Intel Core i5 10310U
42. Intel Core i5 1030G4
43. Intel Core i5 1030G7
44. Intel Core i5 1035G1
45. Intel Core i5 1035G4
46. Intel Core i5 1035G7
47. Intel Core i7 10870H
48. Intel Core i7 10610U
49. Intel Core i7 10810U
50. Intel Core i7 1068NG7
51. Intel Core i7 10700
52. Intel Core i7 10700E
53. Intel Core i7 10700F
54. Intel Core i7 10700K
55. Intel Core i7 10700KF
56. Intel Core i7 10700T
57. Intel Core i7 10700TE
58. Intel Core i7 10750H
59. Intel Core i7 10850H
60. Intel Core i7 10875H
61. Intel Core i7 10510U
62. Intel Core i7 10710U
63. Intel Core i7 1060G7
64. Intel Core i7 1065G7
65. Intel Core i9 10850K
66. Intel Core i9 10885H
67. Intel Core i9 10900
68. Intel Core i9 10900E
69. Intel Core i9 10900F
70. Intel Core i9 10900KF
71. Intel Core i9 10900T
72. Intel Core i9 10900TE
73. Intel Core i9 10900HK

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"Intel Accused Flash Memory Products" include flash memory products designed or manufactured (in whole or in part) by Intel that have the same or similar structures, features, or functionalities as the exemplary Micron 16 nm node NAND flash memory analyzed in Exhibits B-1 through B-6 regardless of how they are branded. That exemplary product was manufactured by Intel and bears Intel die marks.

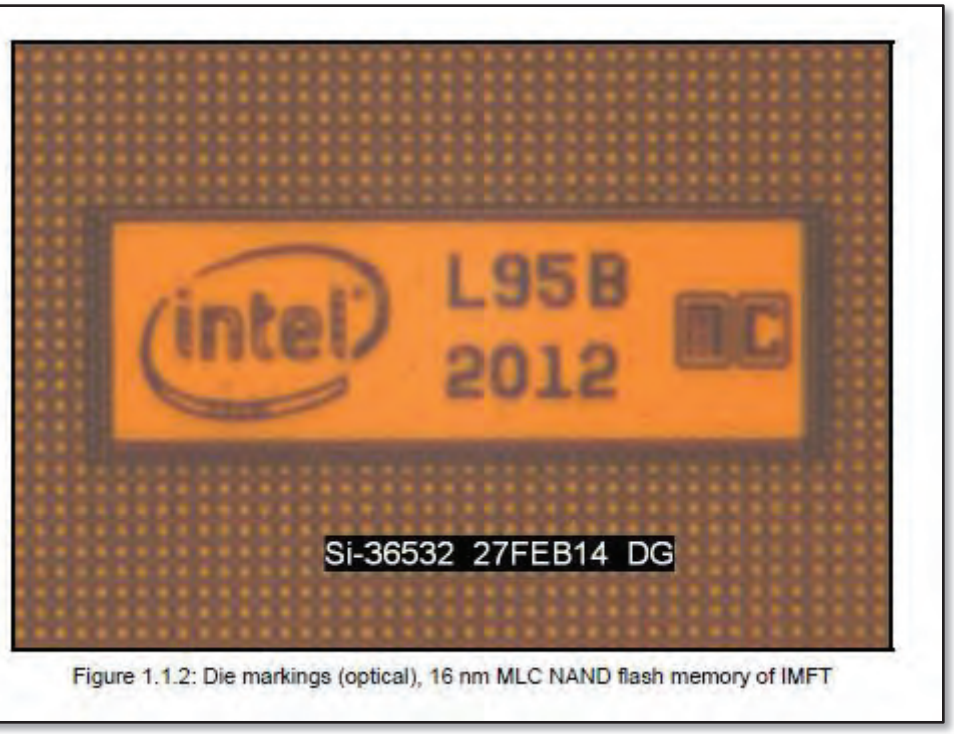


Figure 1.1.2: Die markings (optical), 16 nm MLC NAND flash memory of IMFT

On information and belief, Intel designs and/or fabricates flash memory products using similar designs according to a limited number of processes, many or all of which utilize substantially similar process steps, including process steps for creating regions with graded dopant concentrations. Accordingly, statements in Exhibits B-1 through B-6 referring to Micron's flash memory products are equally applicable to Intel Accused Flash Memory Products.

As shown in Exhibits B-1 through B-6, Intel Accused Flash Memory Products each infringe one or more claims of U.S. Patent Nos. 8,421,195 (claims 1-3, 5-6), 9,190,502 (claims 7-8, 11), 10,510,842 (claims 1-2, 4-5, 7-10, 12-13, 15-18), 10,734,481 (claims 1-4, 6-9, 13, 15-16,

20, 22-24, 26-27, 31-33), 11,121,222 (claims 1-4, 6-9, 13, 15-17, 20-21, 23-25, 27-28, 32-34, 38-42, 44), 11,316,014 (claims 1-4, 6-9, 13, 15-17, 20-21, 23-25, 27-28).

Intel Accused CPU Products and Intel Accused Flash Memory Products are collectively the "Intel Accused Products."

B. Sony Accused Products

Sony Accused Products include products containing or comprising image sensors or transistors designed or manufactured (in whole or in part) by Sony (as defined in the operative complaint) and its affiliates, that have the same or similar structures, features, or functionalities as the exemplary image sensor product shown in Exhibits D-1, D-2, D-3 and D-6, and Sony Transistor Products shown in Exhibits F-1, F-2, F-3, and F-6 regardless of how such products are branded. As described in Exhibits D-1, D-2, D-3 and D-6, and F-1, F-2, F-3, and F-6, Dell-Sony Accused Products each infringe one or more claims of U.S. Patent Nos. 10,510,842, 10,734,481, 11,121,222, and 11,316,014. Exemplary Sony Accused Products are listed below and further below, describing "Dell-Sony Accused Products." Many Sony Accused Products, such as camcorders and handsets are both Sony Accused Image Sensor Products and Sony Accused Transistor Products, because they contain both Sony Accused Images Sensors and Sony Accused Transistors.

1. Sony Accused Televisions

Televisions sold or designed by Sony contain Sony Accused Transistors and/or Image Sensors and are Sony Accused Products. Exemplary Sony Accused Products that are televisions are listed below.

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Add to compare



SALE

BRAVIA XR 65" Class A80K 4K HDR OLED TV with Google TV (2022)

Model: XR-65A80K

55" 65" 77"

Est. Shipping Jan 23

$1,699.99 ~~$2,299.99~~

Add to cart

Add to compare



SALE

BRAVIA XR 75" Class X90K 4K HDR Full Array LED TV with Google TV (2022)

Model: XR-75X90K

55" 65" 75" 85"

Est. Shipping Jan 23

$1,499.99 ~~$1,899.99~~

Add to cart

Add to compare



SALE

BRAVIA XR 65" Class A90J 4K HDR OLED with Google TV (2021)

Model: XR-65A90J

55" 65" 83"

Est. Shipping Jan 23

$2,499.99 ~~$2,999.99~~

Add to cart

Add to compare



BUNDLE SAVINGS

BRAVIA XR 75" Class Z9K 8K HDR Mini LED TV with Google TV (2022)

Model: XR-75Z9K

75" 85"

Est. Shipping Jan 23

$5,999.99

Add to cart

Add to compare



SALE

BRAVIA XR 65" Class A95K 4K HDR OLED TV with Google TV (2022)

Model: XR-65A95K

55" 65"

Est. Shipping Jan 23

$2,999.99 ~~$3,499.99~~

Add to cart

Add to compare



SALE

BRAVIA XR 42" Class A90K 4K HDR OLED TV with Google TV (2022)

Model: XR-42A90K

42" 48"

Est. Delivery Jan 24-25

$1,149.99 ~~$1,399.99~~

Add to cart

Add to compare



SALE

BRAVIA XR 65" Class X95K 4K HDR Mini LED TV with Google TV (2022)

Model: XR-65X95K

65" 75" 85"

Est. Shipping Jan 23

$1,799.99 ~~$2,799.99~~

Add to cart

Add to compare



SALE

BRAVIA XR 50" Class X90J 4K HDR Full Array LED with Google TV (2021)

Model: XR-50X90J

50" 55" 65" 75"

Est. Delivery Jan 24-25

$799.99 ~~$999.99~~

Add to cart

Add to compare



SALE

55" Class X85K 4K HDR LED TV with Google TV (2022)

Model: KD-55X85K

43" 50" 55" 65" 75" 85"

Est. Shipping Jan 23

$699.99 ~~$999.99~~

Add to cart

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Add to compare



SALE

43" Class X80K 4K HDR LED TV with Google TV (2022)

Model: KD-43X80K

43" 50" 55" 65" 75" 85"

Est. Delivery Jan 24-25

$449.99 ~~$599.99~~

Add to cart

Add to compare



SALE

32" Class W830K 720p HD LED HDR TV with Google TV (2022)

Model: KD-32W830K

32"

Est. Delivery Jan 24-25

$349.99 ~~$369.99~~

Add to cart

Add to compare



50" Class X80J 4K HDR LED with Google TV (2021)

Model: KD-50X80J

43" 50" 55" 65" 75"

Item no longer available

$699.99

See similar products

Add to compare



85" Class X85J 4K HDR LED with Google TV (2021)
Model: KD-85X85J

43" 50" 55" 65" 75" 85"

Item no longer available

$2,499.99

See similar products

Add to compare



BRAVIA XR 55" Class A80J 4K HDR OLED with Google TV (2021)
Model: XR-55A80J

55" 65" 77"

Item no longer available

$1,899.99

See similar products

Add to compare



BRAVIA XR 75" Class Z9J 8K HDR Full Array LED with Google TV (2021)
Model: XR-75Z9J

75" 85"

Item no longer available

$3,999.99

See similar products

Add to compare



BRAVIA XR 65" Class X95J 4K HDR Full Array LED with Google TV (2021)
Model: XR-65X95J

65" 75" 85"

Item no longer available

$1,999.99

See similar products

Add to compare



85" Class X91J 4K HDR Full Array LED with Google TV (2021)
Model: KD-85X91J

85"

Item no longer available

$2,799.99

See similar products

Add to compare



48" Class A9S 4K HDR OLED with Android TV (2020)
Model: XBR-48A9S

48"

Item no longer available

$1,499.99

See similar products

Add to compare



BRAVIA XR 55" Class A80CJ 4K HDR OLED with Google TV (2021)
Model: XR-55A80CJ

55" 65" 77"

See similar products

Add to compare



43" Class X80J 4K HDR LED with Google TV (2021)
Model: KD-43X80CJ

43" 50" 55" 65" 75"

See similar products

Add to compare



85" Class X91CJ 4K HDR Full Array LED with Google TV (2021)
Model: KD-85X91CJ

85"

See similar products

Add to compare



BRAVIA XR 50" Class X90CJ 4K HDR Full Array LED with Google TV (2021)
Model: XR-50X90CJ

50" 55" 65" 75"

See similar products

Add to compare



55" Class X80CK 4K HDR LED TV with Google TV (2022)
Model: KD-55X80CK

55" 65" 75" 85"

See similar products

Add to compare

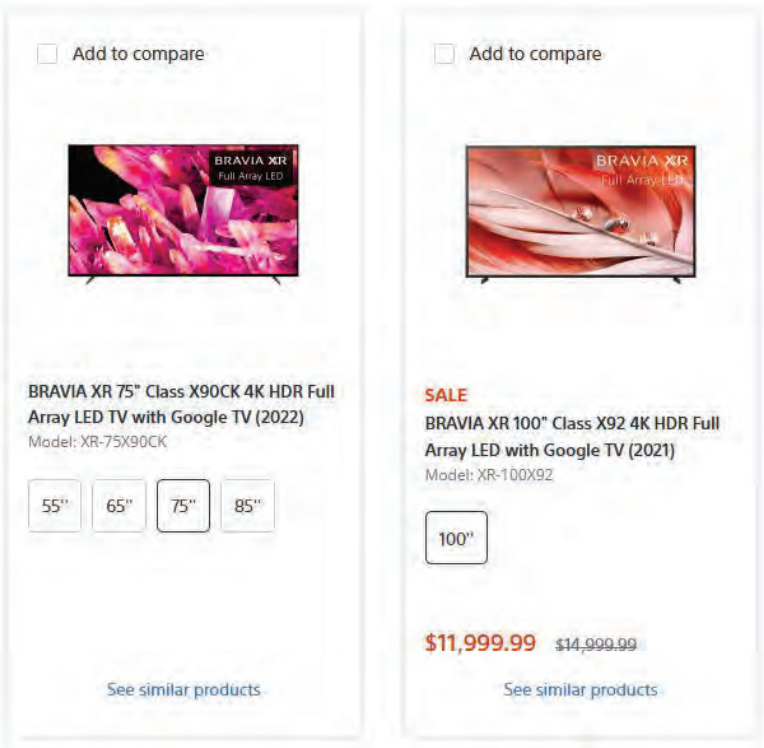


BRAVIA XR 55" Class A80CK 4K HDR OLED TV with Google TV (2022)
Model: XR-55A80CK

55" 65" 77"

See similar products

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2. Sony-Branded Accused Handsets

Handsets or Smartphones sold or designed by Sony contain Sony Accused Transistors and/or Image Sensors and are Sony Accused Products. Exemplary Sony Accused Products that are Sony-Branded handsets or Smartphones are listed below.

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Xperia 5 IV – 5G[1], 8GB RAM, 128GB Smartphone, 6.1" FHD 120Hz HDR OLED Display[2], 4K HDR 120fps video recording[4] on all rear cameras

Model: Xperia 5 IV

Black

Est. Delivery Jan 24-25

$999.99

Add to cart



SALE

Xperia 1 IV 512GB, bright 6.5" 4K 120Hz HDR OLED, 4K 120fps HDR video, true optical zoom, 5G

Model: Xperia 1 IV

Black

Est. Delivery Jan 24-25

$1,399.99 ~~$1,599.99~~

Add to cart



SALE

Xperia PRO-I 512GB, 1" (1.0-type) image sensor camera w/ 4K 120fps and dual aperture, 5G

Model: Xperia PRO-I

Est. Delivery Jan 24-25

$1,099.99 ~~$1,799.99~~

Add to cart



SALE

Xperia 5 III 128GB, 6.1" 120Hz HDR OLED, four optical focal lengths triple camera array, 5G

Model: Xperia 5 III

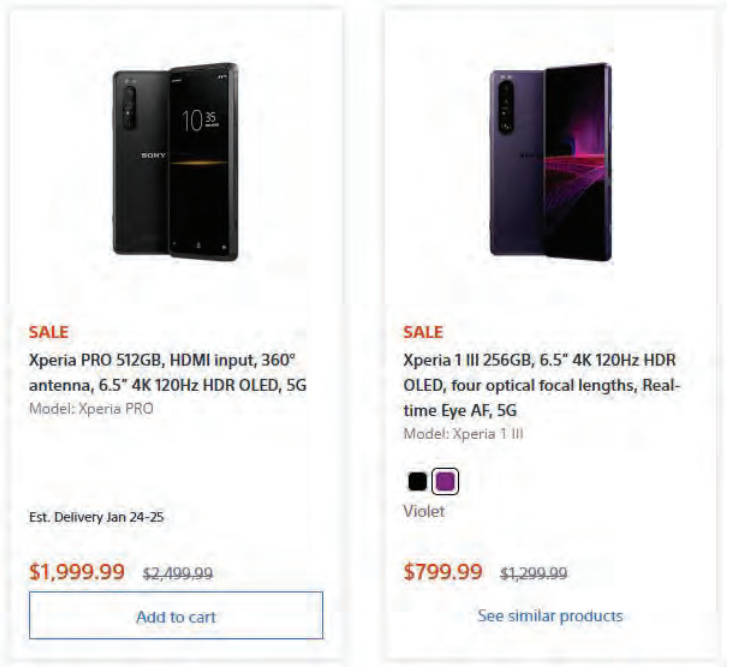
Black

Est. Delivery Jan 24-25

$699.99 ~~$999.99~~

Add to cart

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3. Apple-Branded Sony Accused Image Sensors

Sony manufactures the image sensor sold as part of Apple's iPhone. Greenthread accuses the image sensors in the following iPhone models: iPhone 7, 7 Plus, 8, 8 Plus, X, XR, XS, XS Max, 11, 11 Pro, 11 Pro Max, SE (2nd gen), 12, 12 Mini, 12 Pro, 12 Pro Max, 13, 13 mini, 13 Pro, 13 Pro Max, SE (3rd Gen), 14, 14 Plus, 14 Pro, 14 Pro Max.

4. Sony Accused Gaming Systems

Gaming systems and associated peripheral equiment sold or designed by Sony contain Sony Accused Transistors and/or Image Sensors and are Sony Accused Products. Exemplary Sony Accused products that are gaming products include Playstation VR2, Playstation 5, Playstation 4, and associated perhieral equipment.

5. Sony Accused Audio Equipment

Audio equipment sold or designed by Sony contain Sony Accused Transistors and/or Image Sensors and are Sony Accused Products. Exemplary Sony Accused Products in the audio equipment category are listed below.

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Add to compare



LinkBuds S Truly Wireless Noise Canceling Earbuds
Model: LinkBuds S

White
Est. Delivery Jan 24-25

$199.99

Add to cart

Add to compare



WH-1000XM5 Wireless Industry Leading Noise Canceling Headphones
Model: WH-1000XM5

Black
Out Of Stock

$399.99

Email me when available

Add to compare



WF-1000XM4 Industry Leading Noise Canceling Truly Wireless Earbuds
Model: WF-1000XM4

Black
Est. Delivery Jan 24-25

$279.99

Add to cart

Add to compare



WH-1000XM4 Wireless Premium Noise Canceling Headphones
Model: WH-1000XM4

Black

Est. Delivery Jan 24-25

$349.99

Add to cart

Add to compare



LinkBuds Truly Wireless Earbuds

Model: LinkBuds

White

Est. Delivery Jan 24-25

$179.99

Add to cart

Add to compare



WH-XB910N Wireless Noise Canceling EXTRA BASS™ Headphones with Microphone
Model: WH-XB910N

Black
Est. Delivery Feb 3-6

$249.99

Add to cart

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Add to compare



WF-C500 Truly Wireless In-ear Headphones
Model: WF-C500

Black

Est. Delivery Jan 24-25

$99.99

Add to cart

Add to compare



WH-CH710N Wireless Noise Canceling Headphones with Microphone
Model: WH-CH710N

Black

Est. Delivery Jan 26-27

$149.99

Add to cart

Add to compare



SALE
MDR-Z1R Signature Series Premium Hi-Res Headphones
Model: MDR-Z1R

Black

Est. Delivery Jan 24-25

$1,799.99 ~~$1,999.99~~

Add to cart

Add to compare



SALE
MDR-1AM2 Premium Hi-Res Headphones
Model: MDR-1AM2

Black

Out Of Stock

$249.99 ~~$299.99~~

Email me when available

Add to compare



WH-CH510 Wireless Headphones with Microphone
Model: WH-CH510

Black

Est. Delivery Jan 24-25

$59.99

Add to cart

Add to compare



MDR-ZX310AP Wired On-ear Folding Headphones
Model: MDR-ZX310AP

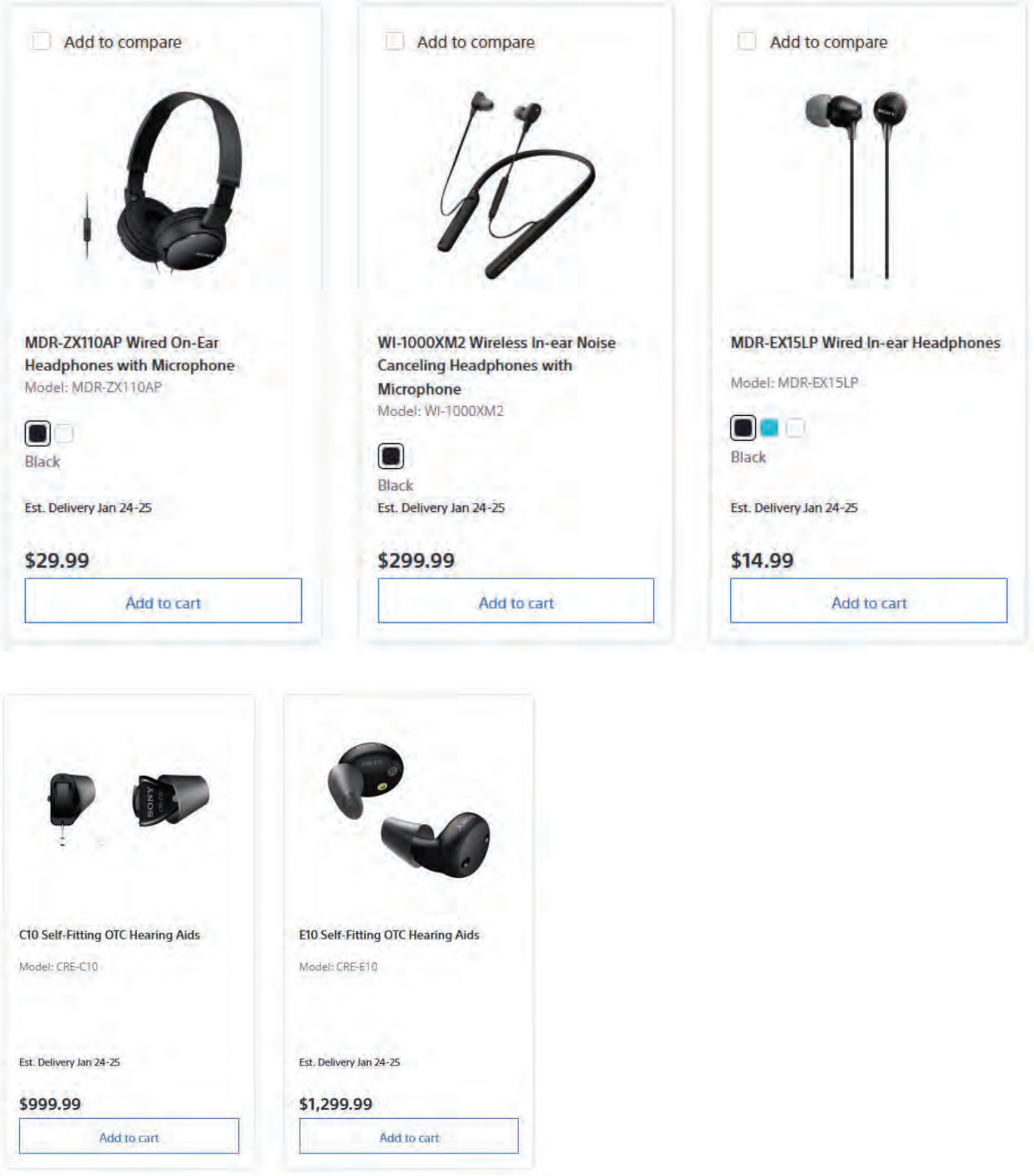
Black

Est. Delivery Jan 24-25

$39.99

Add to cart

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6. Sony Accused Cameras and Camcorders

Cameras and camcorders sold or designed by Sony contain Sony Accused Transistors and/or Image Sensors and are Sony Accused Products. Exemplary Sony Accused Products that are cameras and camcorders are listed below.

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Add to compare



CX405 Handycam® with Exmor R® CMOS sensor

Model: HDR-CX405

Est. Delivery Jan 26-27

$229.99

Add to cart

Add to compare



AX53 4K Handycam® with Exmor R® CMOS sensor

Model: FDR-AX53

Est. Delivery Jan 24-25

$1,099.99

Add to cart

Add to compare



AX43 4K Handycam® with Exmor R® CMOS sensor

Model: FDR-AX43

Out Of Stock

$949.99

Email me when available

Greenthread Ex. 2048, p. 22
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Add to compare



FDR-AX700 4K HDR Camcorder

Model: FDR-AX700

Est. Delivery Jan 24-25

$1,899.99

Add to cart

Add to compare



AX100 4K Expert Handycam®

Model: FDR-AX100

Item no longer available

$1,499.99

See similar products

Add to compare



AX43A 4K Handycam® with Exmor R® CMOS sensor

Model: FDR-AX43A

Est. Delivery Jan 24-25

$949.99

Add to cart

Add to compare



BUNDLE SAVINGS

Alpha 7R V Full-frame Mirrorless Interchangeable Lens Camera

Model: ILCE-7RM5

Est. Delivery Jan 24-25

$3,899.99

Add to cart

Add to compare



BUNDLE SAVINGS

Alpha 7 IV - Full-frame Interchangeable Lens Camera 33MP, 10FPS, 4K/60p

Model: ILCE-7M4

Body Only

Body + 28-70mm Zoom Lens

Est. Delivery Jan 24-25

$2,499.99

Add to cart

Add to compare



Alpha 7 III - Full-frame Interchangeable Lens Camera 24.2MP, 10FPS, 4K/30p

Model: ILCE-7M3

Body Only

Body + 28-70mm Zoom Lens

Est. Delivery Jan 24-25

$1,999.99

Add to cart

Add to compare



SALE

Alpha 7 II - Full-frame Interchangeable Lens Camera 24.2MP, 5FPS, Full HD 1080p

Model: ILCE-7M2

Body Only

Body + 28-70mm Power Zoom Lens

Est. Delivery Jan 24-25

$899.99 ~~$1,399.99~~

Add to cart

Add to compare



Alpha 7C - Full-frame Interchangeable Lens Camera 24.2MP, 10FPS, 4K/30p, Compact

Model: ILCE-7C

Silver

Body only

Body+ 28-60mm Zoom Lens

Est. Delivery Jan 24-25

$1,799.99

Add to cart

Add to compare



Alpha 7R III - Full-frame Interchangeable Lens Camera 42.4MP, 10FPS, 4K/30p

Model: ILCE-7RM3A

Est. Delivery Jan 24-25

$2,499.99

Add to cart

Add to compare



Alpha 7R IV - Full-frame Interchangeable Lens Camera 61MP, 10FPS, 4K/30p
Model: ILCE-7RM4A

Est. Delivery Jan 24-25

$3,499.99

Add to cart

Add to compare



BUNDLE SAVINGS
Alpha ZV-E10 - APS-C Interchangeable Lens Vlog Camera 24MP, 4K/30p, Vlog style camera
Model: ZV-E10

White

Body Only

Body + 16-50mm Zoom Lens

Est. Delivery Jan 24-25

$699.99

Add to cart

Add to compare



Alpha 6600 - APS-C Interchangeable Lens Camera 24.2MP, 11FPS, 4K/30p
Model: ILCE-6600

Body Only

Body + 18-135mm Zoom Lens

Out Of Stock

$1,399.99

Email me when available

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Add to compare



Alpha 6400 - APS-C Interchangeable Lens Camera & Lens Kit 24.2MP, 11FPS, 4K/30p

Model: ILCE-6400L

Body + 16-50mm Power Zoom Lens

Body + 18-135mm Power Zoom Lens

Body Only

Out Of Stock

$999.99

Email me when available

Add to compare



Alpha 6100 - APS-C Interchangeable Lens Camera & Lens Kit 24.2MP, 11FPS, 4K/30p

Model: ILCE-6100L

Body + 16-50mm Power Zoom Lens

Body + Zoom Lenses (16-50 mm & 55-210 mm)

Body only

Out Of Stock

$849.99

Email me when available

Add to compare



Alpha 6000 - APS-C Interchangeable Lens Camera 24.3MP, 11FPS, Full HD 1080p

Model: ILCE-6000

Black

Body Only

Body + Zoom Lenses (16-50 mm & 55-210 mm)

Body + 16-50 mm Zoom Lens

Out Of Stock

$549.99

Email me when available

Add to compare



BUNDLE SAVINGS

Alpha 7S III - Full-frame Interchangeable Lens Camera 12.1MP, 10FPS, 4K/120p High Sensitivity

Model: ILCE-7SM3

Est. Delivery Jan 24-25

$3,499.99

Add to cart

Add to compare



Alpha 9 II - Full-frame Interchangeable Lens Camera 24.2MP, 20FPS, 4K/30p

Model: ILCE-9M2

Out Of Stock

$4,499.99

Email me when available

Add to compare



BUNDLE SAVINGS

Alpha 1 - Full-frame Interchangeable Lens Camera 50.1MP, 30FPS, 4K/120p /8K/30p

Model: ILCE-1

Est. Delivery Jan 24-25

$6,499.99

Add to cart

Add to compare



Alpha 7R IV - Full-frame Interchangeable Lens Camera 61MP, 10FPS, 4K/30p

Model: ILCE-7RM4

$3,499.99

See similar products

Add to compare



Alpha 7R III - Full-frame Interchangeable Lens Camera 42.4MP, 10FPS, 4K/30p

Model: ILCE-7RM3

Item no longer available

$2,499.99

See similar products

Add to compare



Alpha 7R II - Full-frame Interchangeable Lens Camera 42.4MP, 5FPS, 4K/30p

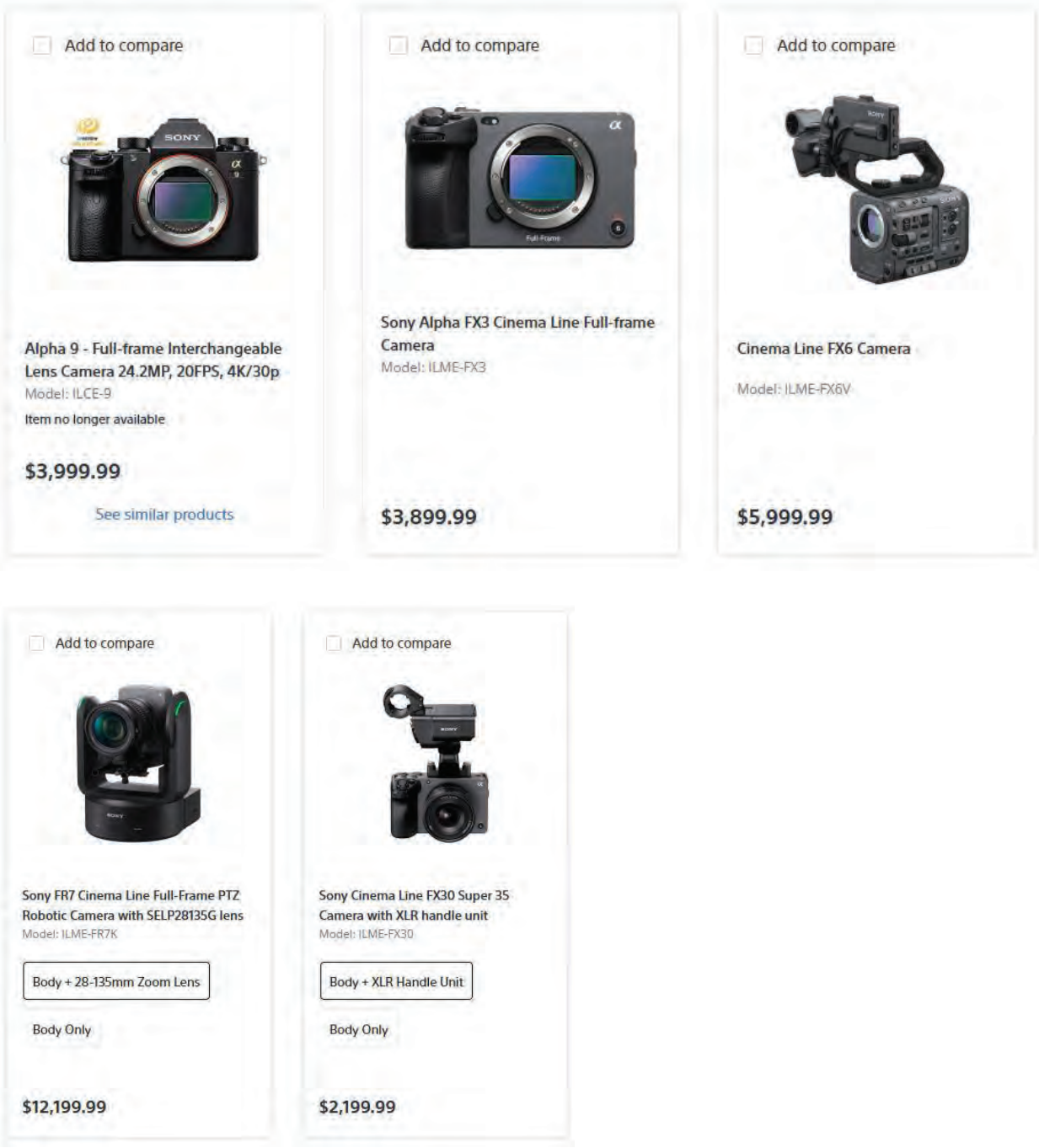
Model: ILCE-7RM2

Item no longer available

$1,799.99

See similar products

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C. Dell Accused Products

Dell's products infringe one or more asserted claims of the asserted patents ("Dell Accused Products"). Dell Accused Products include Dell Products (as defined in the First Amended Complaint, Dkt. 38) that incorporate or comprise Intel Accused Products ("Dell-Intel

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Accused Products"), Dell-Micron Accused Products (defined in the First Amended Complaint), Dell-Micron-Flash Accused Products (defined below), Dell-WD Accused Products (defined in the First Amended Complaint), Dell-Sony Accused Products (defined in the Operative Complaint), and Dell-Micron-DRAM Accused Products (defined below).

1. Dell-Intel Accused Products

Dell Products comprising or containing Intel Accused Products are Dell-Intel Accused Products and infringe the same claims of the Greenthread Patents as the Intel Accused Products for the same reasons. The following listing of Dell-Intel Accused Products is derived from publicly available information at Dell's website, as noted in Exhibit G to Greenthread's Complaint (Dkt. 1-7). Greenthread reserves the right to supplement the list of Dell Accused Products, e.g., as discovery proceeds.

1. New XPS Desktop
2. Alienware Aurora R13 Gaming Desktop
3. New XPS Desktop
4. Alienware x17 Gaming Laptop
5. Alienware x15 Gaming Laptop
6. XPS 17 Touch Laptop
7. Alienware m15 R6 Gaming Laptop
8. XPS 15 Laptop
9. XPS 15 Touch Laptop
10. XPS 13 Touch Laptop
11. G15 Special Edition Gaming Laptop
12. XPS 13 Laptop
13. XPS 13 2-in-1 Laptop
14. Inspiron 15 2-in-1 Laptop
15. XPS 13 Touch Laptop
16. New Inspiron 16 Plus Laptop
17. G15 Gaming Laptop
18. XPS 17 Laptop
19. XPS 13 Laptop
20. Inspiron 17 2-in-1 Laptop
21. Inspiron 14 2-in-1 Laptop
22. Inspiron 13 Laptop
23. Inspiron 13 2-in-1 Plus Laptop
24. Inspiron 15 Laptop
25. Inspiron 14 Laptop
26. Inspiron 15 3000 Laptop
27. New Inspiron 15 1300 Laptop
28. Alienware m15 R4 Gaming Laptop
29. Inspiron Desktop
30. XPS Desktop
31. Other Dell products incorporating Intel Accused Products.

This identification of Dell-Intel Accused Products is based upon Greenthread's investigation to date, which has included limited physical testing to the extent practicable and has been undertaken at significant expense to Greenthread.

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2. Dell-Micron-Flash Accused Products

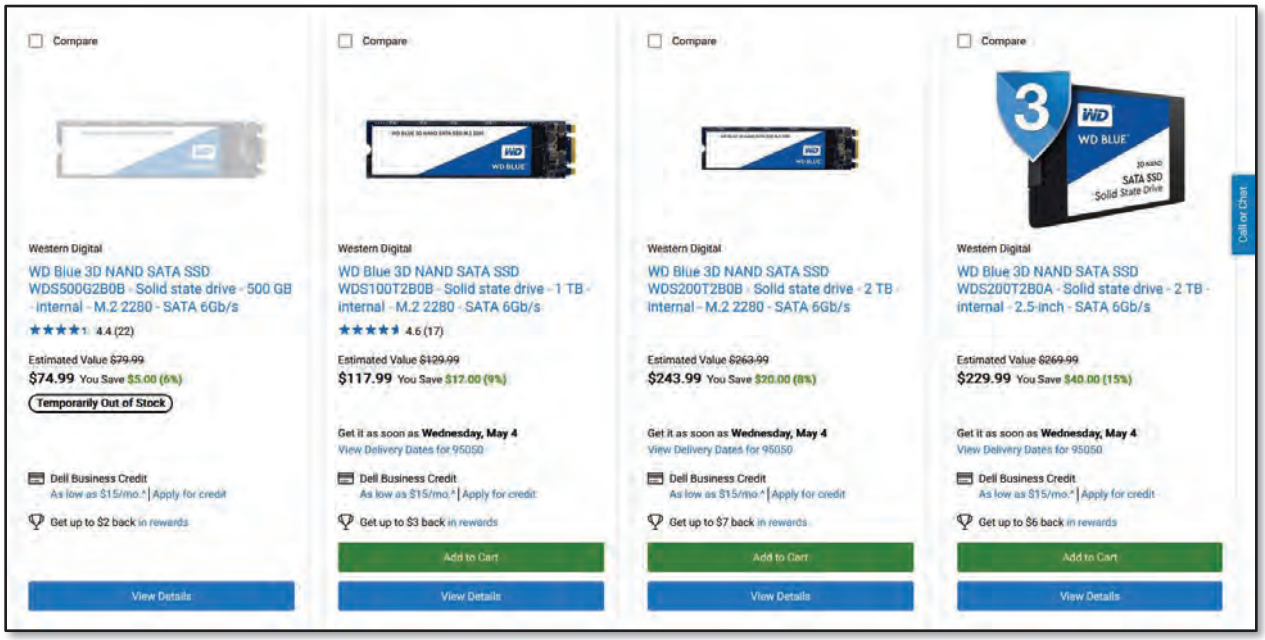
Dell-Micron-Flash Accused Products include all Dell Products containing or comprising flash memory designed or manufactured (in whole or in part) by Micron Technology, Inc., Micron Semiconductor Products, Inc., Micron Technology Texas, LLC and/or their affiliates ("Micron"), that have the same or similar structures, features, or functionalities as the exemplary product shown in Exhibits B-1 through B-6, regardless of how such products are branded. Flash memory products include SSDs, microSD/SD cards, and thumb drives. As described in Exhibits B-1 through B-6, Dell-Micron-Flash Accused Products each infringe one or more claims of U.S. Patent Nos. 8,421,195 (claims 1-3, 5-6), 9,190,502 (claims 7-8, 11), 10,510,842 (claims 1-2, 4-10, 12-18), 10,734,481 (claims 1-9, 13, 15-16, 20, 22-27, 31-33), 11,121,222 (claims 1-9, 13, 15-17, 20-21, 23-28, 32-34, 38-42, 44), 11,316,014 (claims 1-9, 13, 15-17, 20-21, 23-28). Dell-Micron-Flash Accused Products include Precision Fixed Workstations, Precision Mobile Workstations, Latitude, Optiplex, XPS Desktops, XPS Notebooks, Vostro Desktops, Inspiron Desktops, Inspiron Netbooks, Alienware Desktops, and Alienware Notebooks.

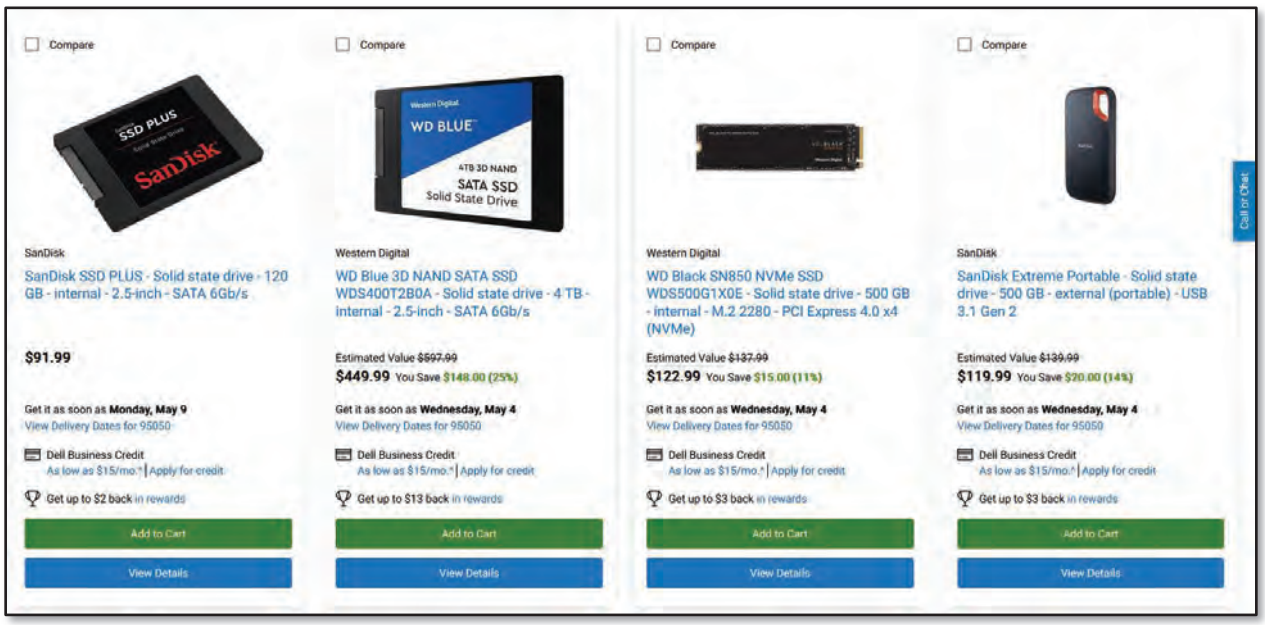
3. Dell-WD Accused Products

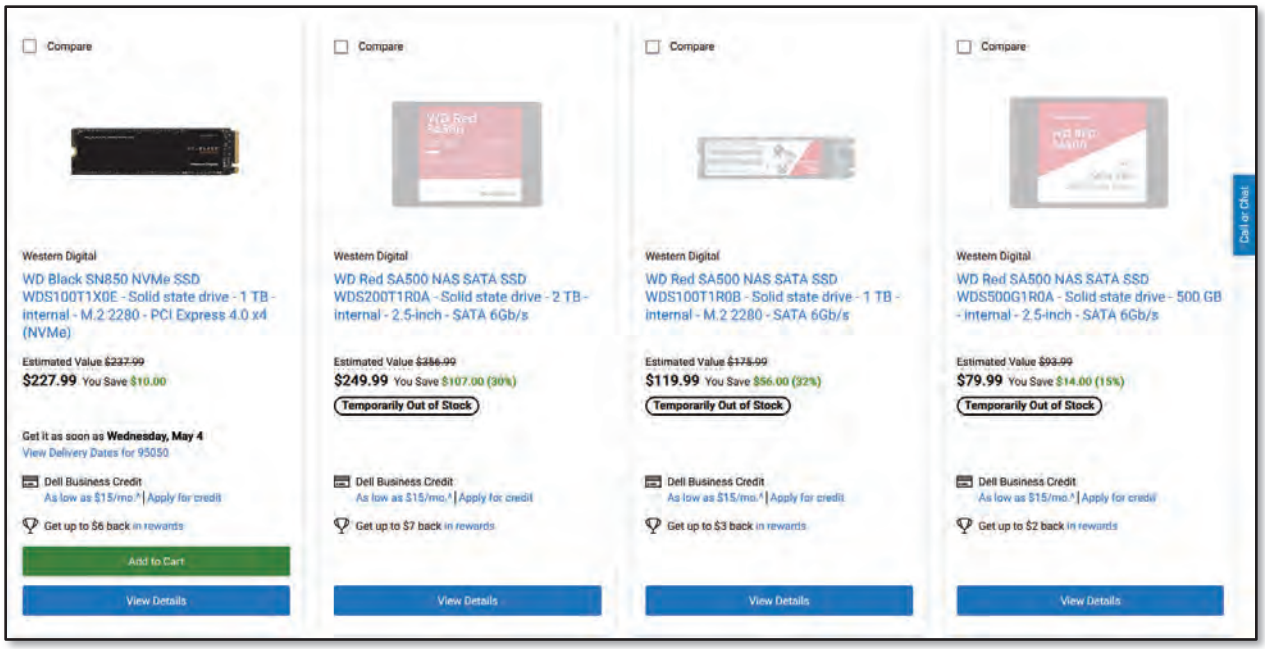
"Dell-WD Accused Products" include all Dell Products containing or comprising flash memory designed or manufactured (in whole or in part) by Western Digital Corporation, Western Digital Technologies, Inc., HGST, Inc., SanDisk LLC, SanDisk Holdings LLC, SanDisk Technologies LLC and/or their affiliates ("Western Digital" or "WD") that have the same or similar structures, features, or functionalities as the exemplary product shown in Exhibits C-1 through C-6, regardless of how such products are branded, regardless of how such products are branded. As described in Exhibits C-1 through C-6, Dell-WD Accused Products each infringe one or more claims of U.S. Patent Nos. 8,421,195 (claims 1-3, 5-6), 9,190,502 (claims 7-11), 10,510,842 (claims 1-2, 4-10, 12-18), 10,734,481 (claims 1-9, 13, 15-16, 20, 22-27, 31-33),

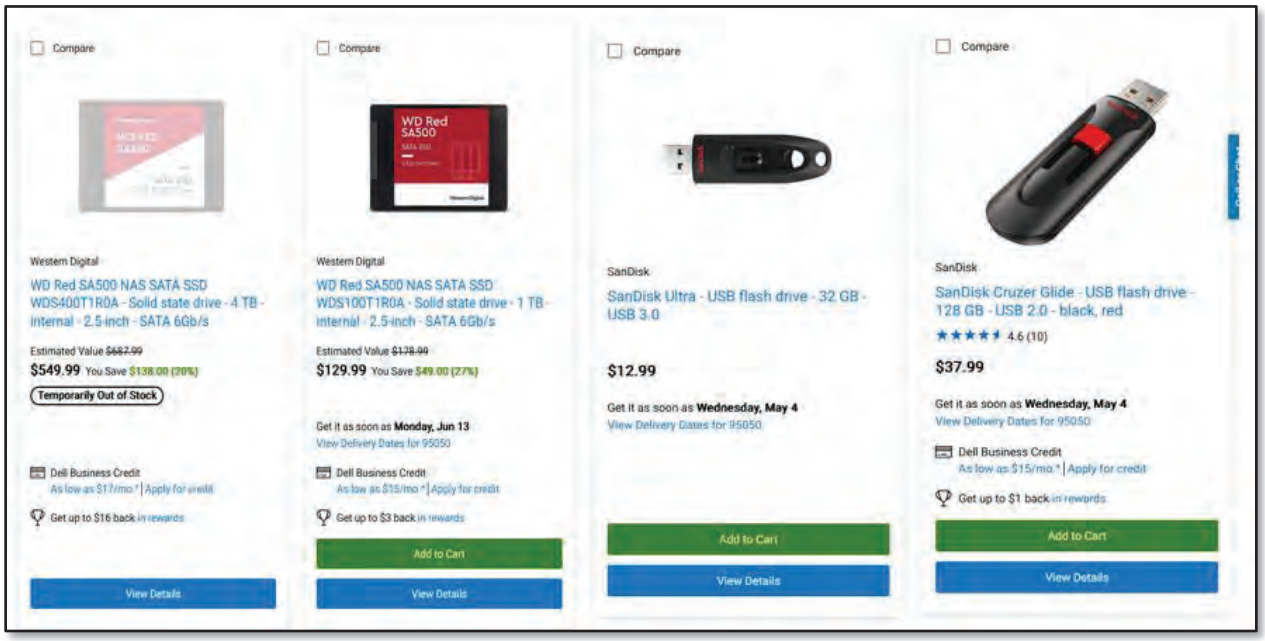
Greenthread Ex. 2048, p. 30
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IPR2023-01243

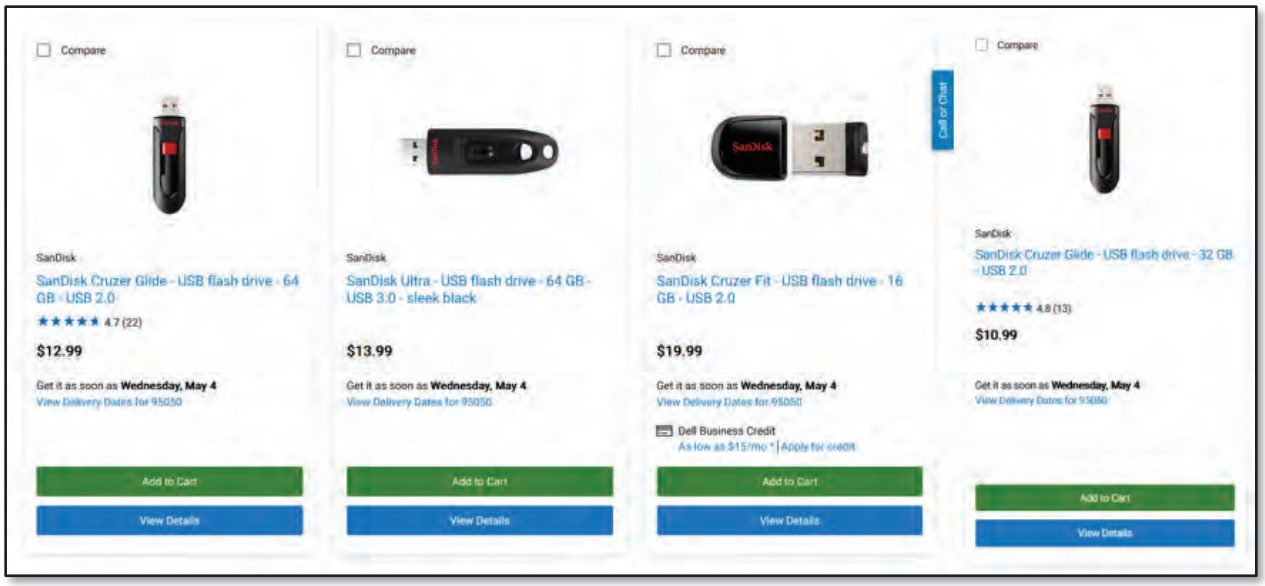
11,121,222 (claims 1-9, 13, 15-17, 20-21, 23-28, 32-34, 38-42, 44), 11,316,014 (claims 1-9, 13, 15-17, 20-21, 23-28). Flash memory products include SSDs, microSD/SD cards, and thumb drives. Exemplary Dell-WD Accused Products are listed below. All images were taken from dell.com.

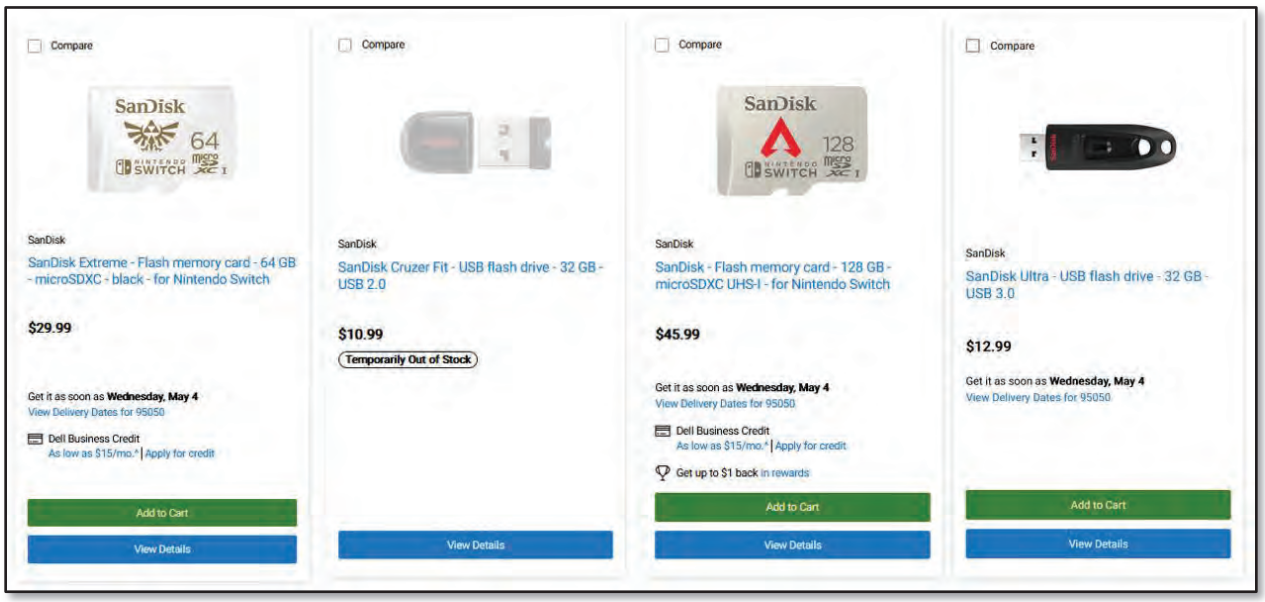


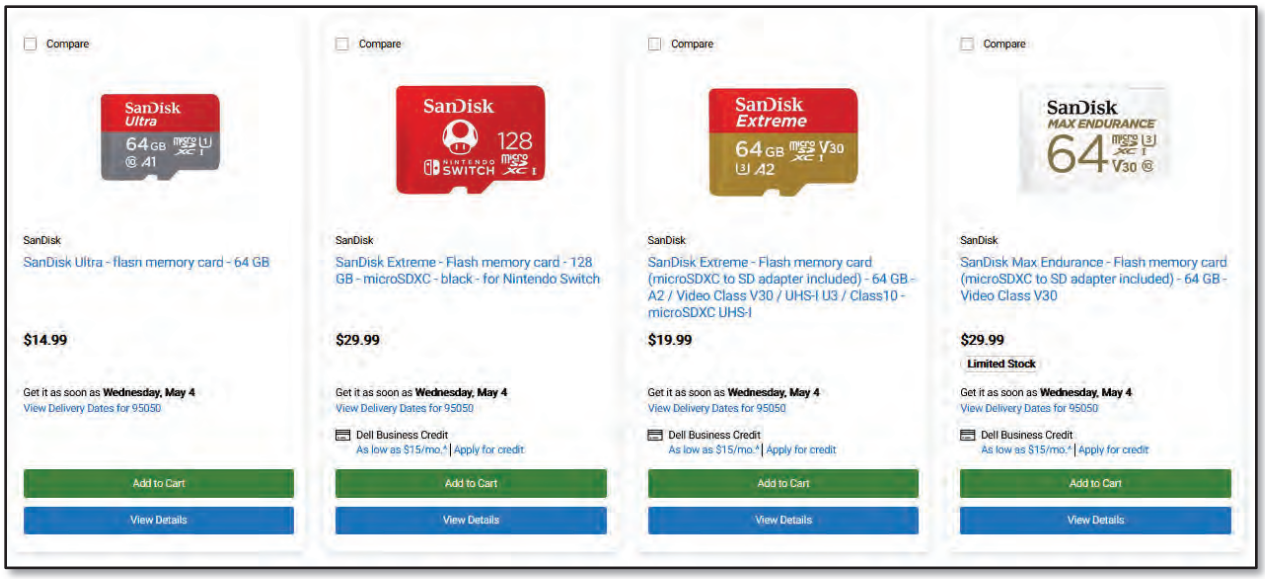


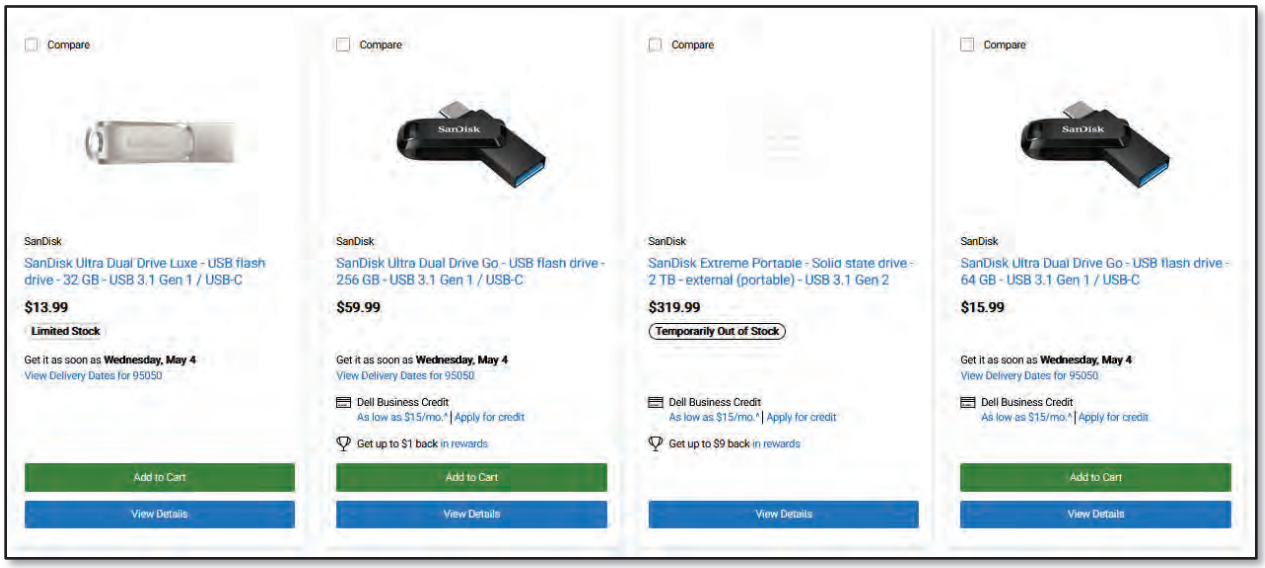

Compare
Western Digital
WD Black SN850 NVMe SSD WDS100T1X0E - Solid state drive - 1 TB - internal - M.2 2280 - PCI Express 4.0 x4 (NVMe)
Estimated Value $237.99
$227.99 You Save $10.00
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Get up to $6 back in rewards
Add to Cart
View Details
Compare
Western Digital
WD Red SA500 NAS SATA SSD WDS200T1R0A - Solid state drive - 2 TB - internal - 2.5-inch - SATA 6Gb/s
Estimated Value $356.99
$249.99 You Save $107.00 (30%)
Temporarily Out of Stock
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Get up to $7 back in rewards
View Details
Compare
Western Digital
WD Red SA500 NAS SATA SSD WDS100T1R0B - Solid state drive - 1 TB - internal - M.2 2280 - SATA 6Gb/s
Estimated Value $175.99
$119.99 You Save $56.00 (32%)
Temporarily Out of Stock
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Get up to $3 back in rewards
View Details
Compare
Western Digital
WD Red SA500 NAS SATA SSD WDS500G1R0A - Solid state drive - 500 GB - internal - 2.5-inch - SATA 6Gb/s
Estimated Value $93.99
$79.99 You Save $14.00 (15%)
Temporarily Out of Stock
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Get up to $2 back in rewards
View Details

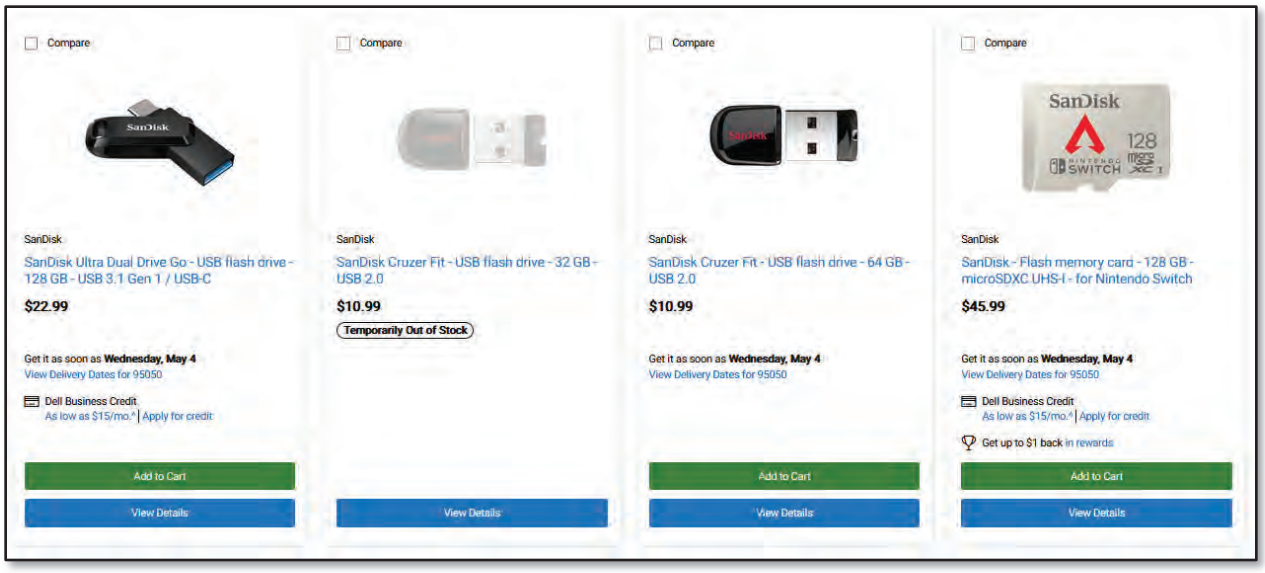

Compare
Western Digital
WD Red SA500 NAS SATA SSD WDS400T1R0A - Solid state drive - 4 TB - internal - 2.5-inch - SATA 6Gb/s
Estimated Value $682.99
$549.99 You Save $138.00 (20%)
Temporarily Out of Stock
Dell Business Credit
As low as $17/mo.^ | Apply for credit
Get up to $16 back in rewards
View Details
Compare
WD Red SA500
Western Digital
WD Red SA500 NAS SATA SSD WDS100T1R0A - Solid state drive - 1 TB - internal - 2.5-inch - SATA 6Gb/s
Estimated Value $178.99
$129.99 You Save $49.00 (27%)
Get it as soon as Monday, Jun 13
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Dell Business Credit
As low as $15/mo.^ | Apply for credit
Get up to $3 back in rewards
Add to Cart
View Details
Compare
SanDisk
SanDisk Ultra - USB flash drive - 32 GB - USB 3.0
$12.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Add to Cart
View Details
Compare
SanDisk
SanDisk Cruzer Glide - USB flash drive - 128 GB - USB 2.0 - black, red
4.6 (10)
$37.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Get up to $1 back in rewards
Add to Cart
View Details

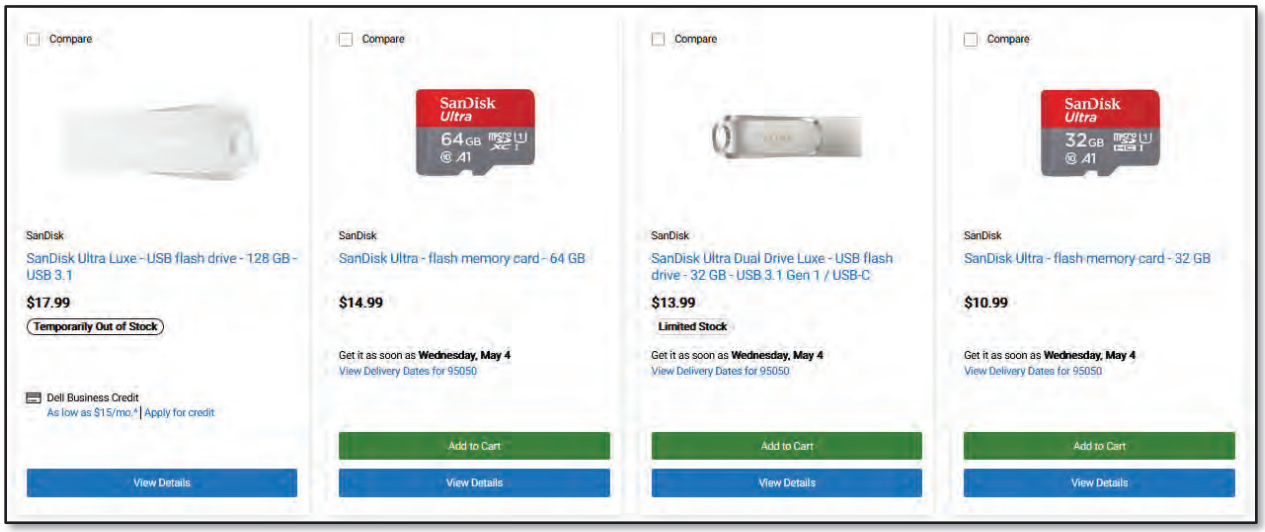

Compare
SanDisk
SanDisk Cruzer Glide - USB flash drive - 64 GB - USB 2.0
4.7 (22)
$12.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Add to Cart
View Details
Compare
SanDisk
SanDisk Ultra - USB flash drive - 64 GB - USB 3.0 - sleek black
$13.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Add to Cart
View Details
Compare
SanDisk
SanDisk Cruzer Fit - USB flash drive - 16 GB - USB 2.0
$19.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.* | Apply for credit
Add to Cart
View Details
Call or Chat
Compare
SanDisk
SanDisk Cruzer Glide - USB flash drive - 32 GB - USB 2.0
4.8 (13)
$10.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Add to Cart
View Details

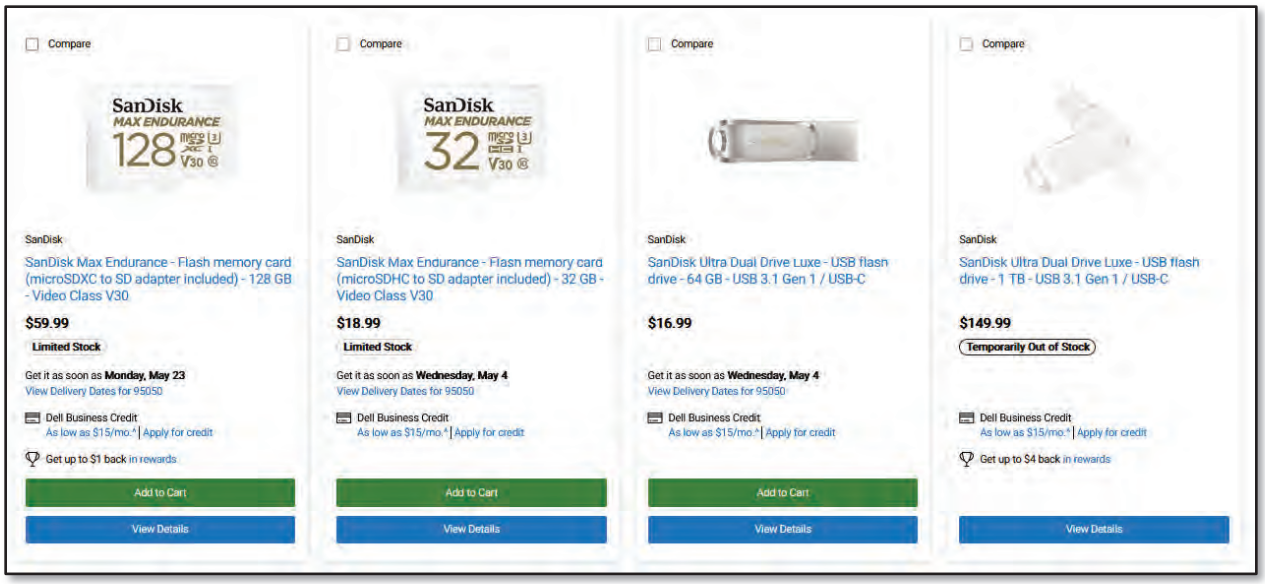

Compare
SanDisk
SanDisk Extreme - Flash memory card - 64 GB - microSDXC - black - for Nintendo Switch
$29.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.* | Apply for credit
Add to Cart
View Details
Compare
SanDisk
SanDisk Cruzer Fit - USB flash drive - 32 GB - USB 2.0
$10.99
Temporarily Out of Stock
View Details
Compare
SanDisk
SanDisk - Flash memory card - 128 GB - microSDXC UHS-I - for Nintendo Switch
$45.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.* | Apply for credit
Get up to $1 back in rewards
Add to Cart
View Details
Compare
SanDisk
SanDisk Ultra - USB flash drive - 32 GB - USB 3.0
$12.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Add to Cart
View Details

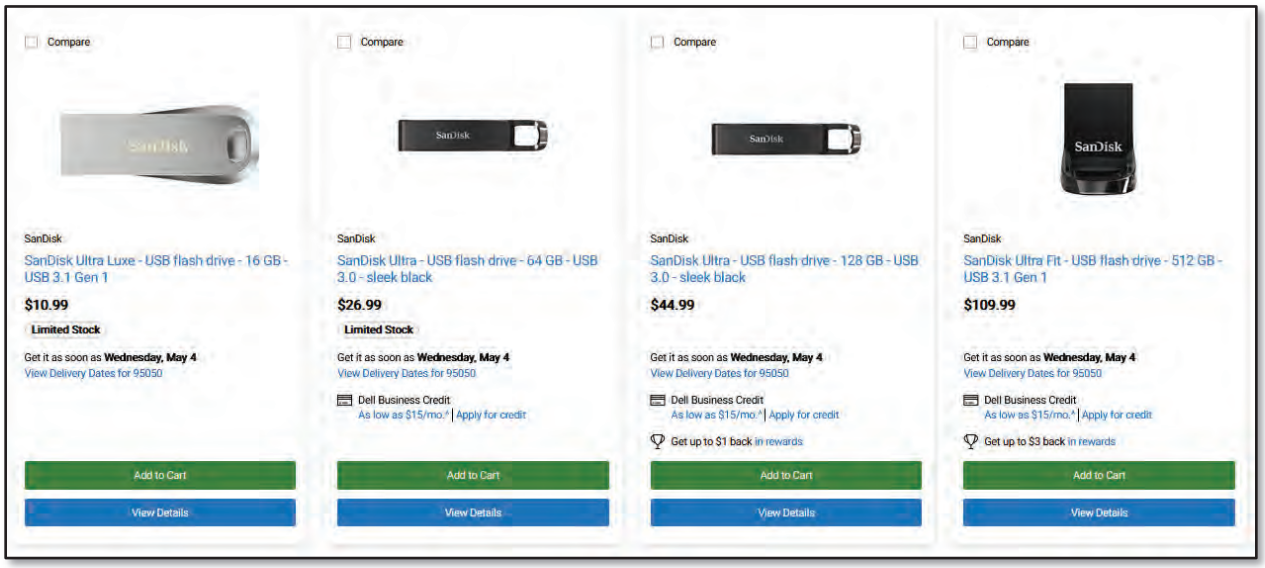

Compare
SanDisk Ultra - flash memory card - 64 GB
$14.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Add to Cart
View Details
Compare
SanDisk Extreme - Flash memory card - 128 GB - microSDXC - black - for Nintendo Switch
$29.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Add to Cart
View Details
Compare
SanDisk Extreme - Flash memory card (microSDXC to SD adapter included) - 64 GB - A2 / Video Class V30 / UHS-I U3 / Class10 - microSDXC UHS-I
$19.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Add to Cart
View Details
Compare
SanDisk Max Endurance - Flash memory card (microSDXC to SD adapter included) - 64 GB - Video Class V30
$29.99
Limited Stock
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Add to Cart
View Details

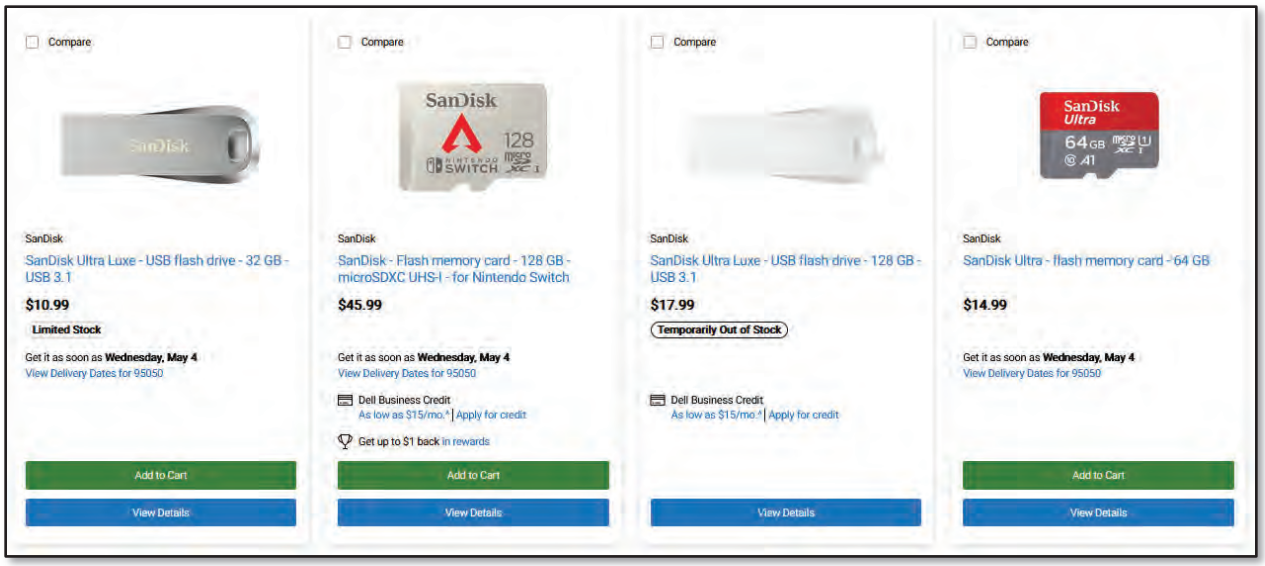

Compare
SanDisk Ultra Dual Drive Luxe - USB flash drive - 32 GB - USB 3.1 Gen 1 / USB-C
$13.99
Limited Stock
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Add to Cart
View Details
Compare
SanDisk Ultra Dual Drive Go - USB flash drive - 256 GB - USB 3.1 Gen 1 / USB-C
$59.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Get up to $1 back in rewards
Add to Cart
View Details
Compare
SanDisk Extreme Portable - Solid state drive - 2 TB - external (portable) - USB 3.1 Gen 2
$319.99
Temporarily Out of Stock
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Get up to $9 back in rewards
View Details
Compare
SanDisk Ultra Dual Drive Go - USB flash drive - 64 GB - USB 3.1 Gen 1 / USB-C
$15.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.^ | Apply for credit
Add to Cart
View Details

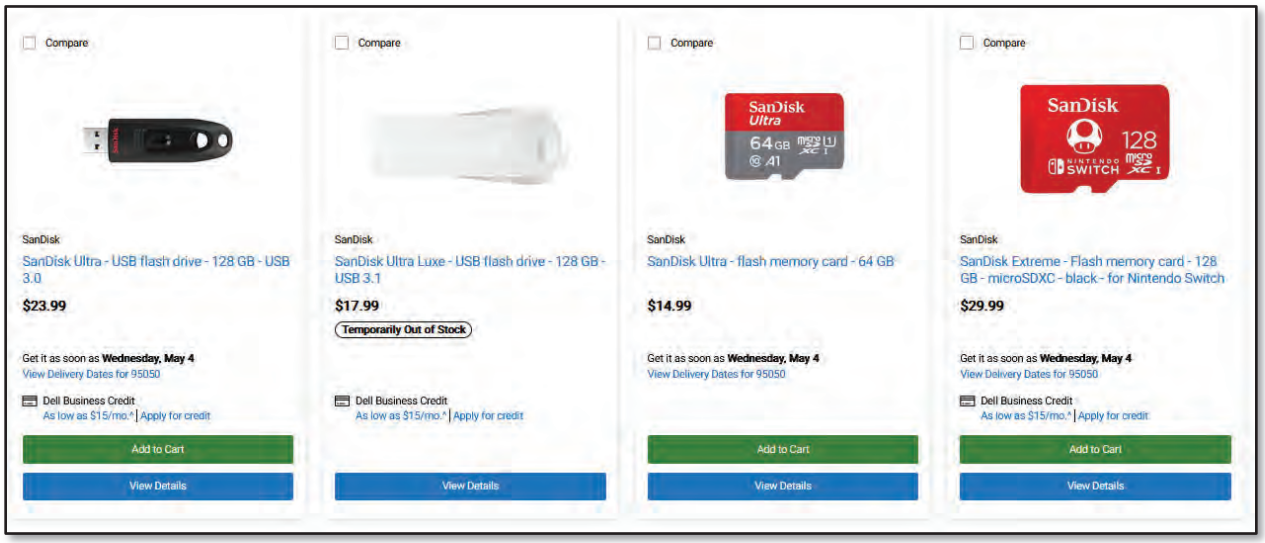

Compare
SanDisk
SanDisk Ultra Dual Drive Go - USB flash drive - 128 GB - USB 3.1 Gen 1 / USB-C
$22.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Dell Business Credit
As low as $15/mo.* | Apply for credit
Add to Cart
View Details
Compare
SanDisk
SanDisk Cruzer Fit - USB flash drive - 32 GB - USB 2.0
$10.99
Temporarily Out of Stock
View Details
Compare
SanDisk
SanDisk Cruzer Fit - USB flash drive - 64 GB - USB 2.0
$10.99
Get it as soon as Wednesday, May 4
View Delivery Dates for 95050
Add to Cart
View Details
Compare
SanDisk
SanDisk - Flash memory card - 128 GB - microSDXC UHS-I - for Nintendo Switch
$45.99
Get it as soon as Wednesday, May 4
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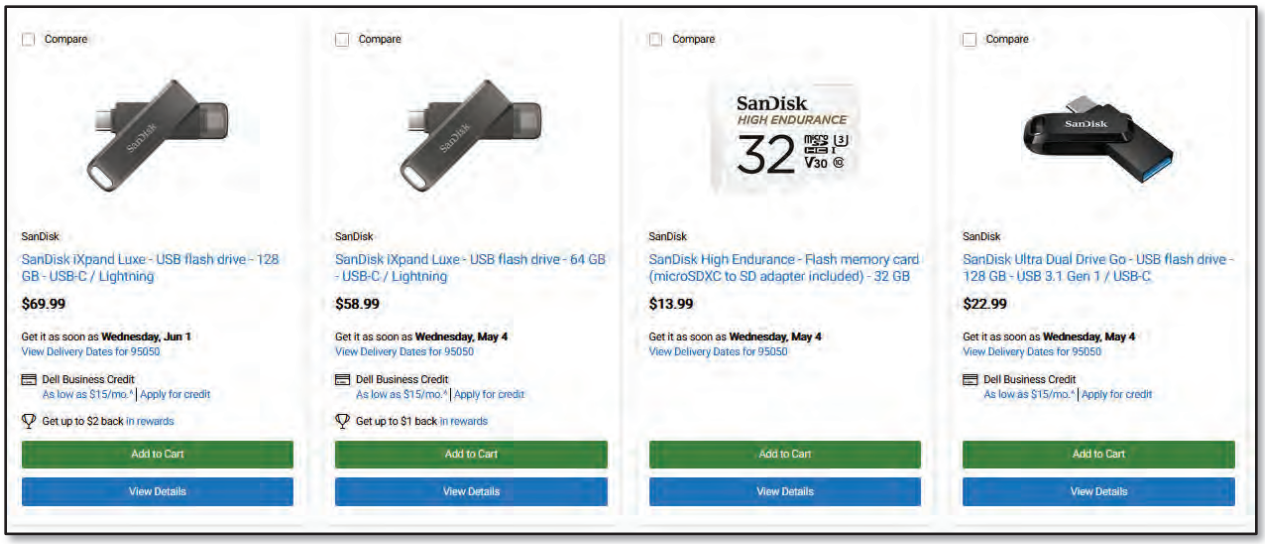

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SanDisk
SanDisk Ultra Luxe - USB flash drive - 128 GB - USB 3.1
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SanDisk
SanDisk Ultra - flash memory card - 32 GB
$10.99
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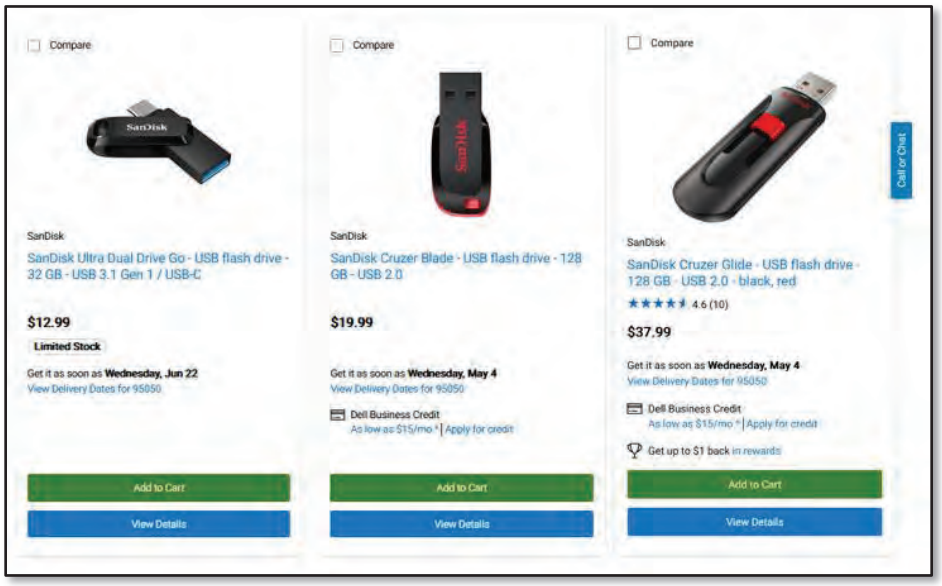

Compare
SanDisk
MAX ENDURANCE
128
SanDisk
SanDisk Max Endurance - Flash memory card (microSDXC to SD adapter included) - 128 GB - Video Class V30
$59.99
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SanDisk
MAX ENDURANCE
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SanDisk
SanDisk Max Endurance - Flash memory card (microSDHC to SD adapter included) - 32 GB - Video Class V30
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SanDisk Ultra Dual Drive Luxe - USB flash drive - 64 GB - USB 3.1 Gen 1 / USB-C
$16.99
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SanDisk Ultra Luxe - USB flash drive - 16 GB - USB 3.1 Gen 1
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SanDisk
SanDisk Ultra - USB flash drive - 64 GB - USB 3.0 - sleek black
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SanDisk Ultra Fit - USB flash drive - 512 GB - USB 3.1 Gen 1
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SanDisk Ultra Luxe - USB flash drive - 32 GB - USB 3.1
$10.99
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SanDisk
SanDisk - Flash memory card - 128 GB - microSDXC UHS-I - for Nintendo Switch
$45.99
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SanDisk Ultra Luxe - USB flash drive - 128 GB - USB 3.1
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SanDisk Extreme - Flash memory card - 128 GB - microSDXC - black - for Nintendo Switch
$29.99
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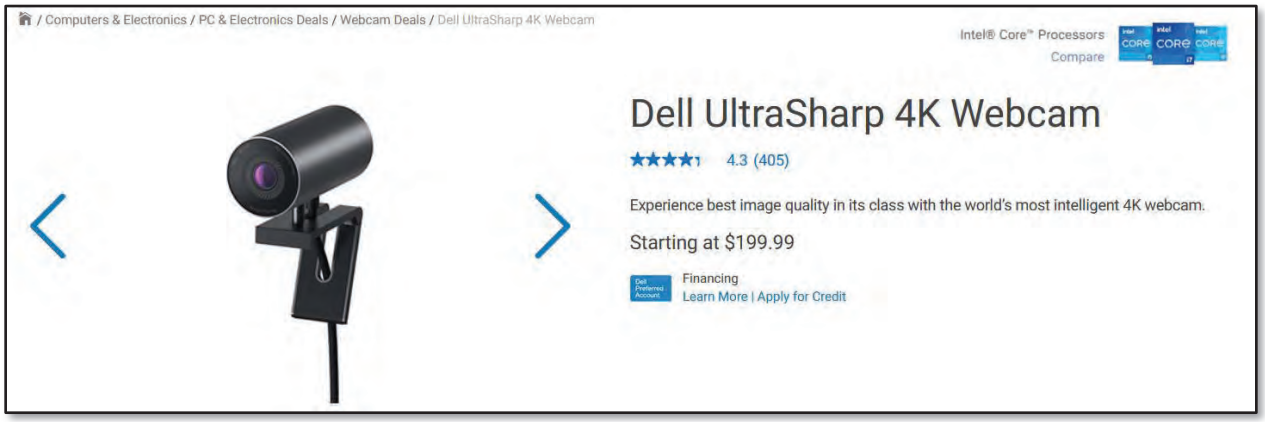


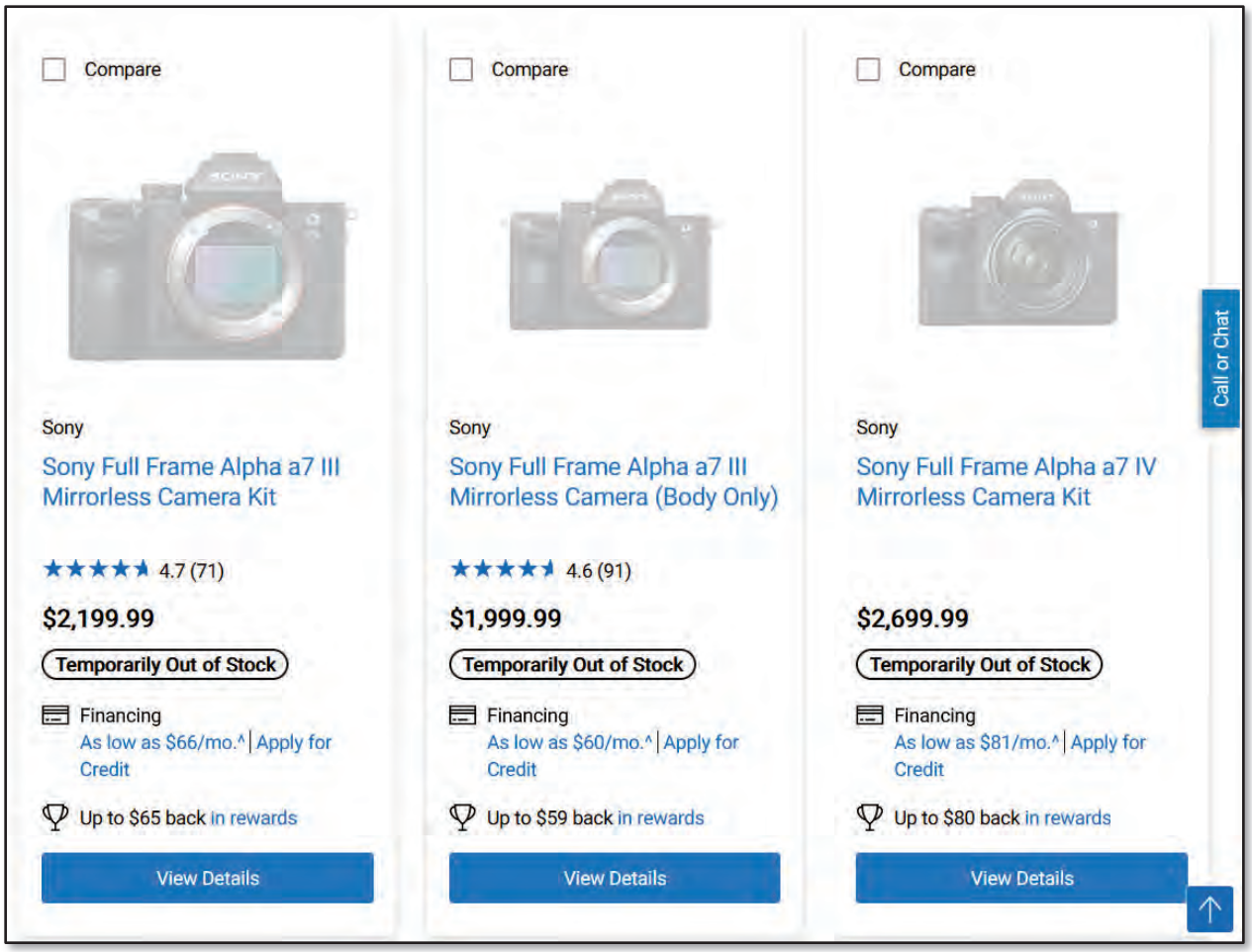


4. Dell-Sony Accused Products

Dell-Sony Accused Products include all Dell Products containing or comprising image sensors or transistors designed or manufactured (in whole or in part) by Sony Corporation, Sony Semiconductor Solutions, Sony Global Manufacturing & Operations, Sony Electronics Inc., Sony Corporation of America or their affiliates ("Sony"), that have the same or similar structures, features, or functionalities as the exemplary product shown in Exhibits D-1, D-2, D-3 and D-6,

and F-1, F-2, F-3, and F-6 regardless of how such products are branded. As described in Exhibits D-1, D-2, D-3 and D-6, and F-1, F-2, F-3, and F-6, Dell-Sony Accused Products each infringe one or more claims of U.S. Patent Nos. 10,510,842, 10,734,481, 11,121,222, and 11,316,014. Exemplary Dell-Sony Accused Products are listed below. All images are taken from dell.com.





Upon information and belief, Dell also incorporates further Sony image sensors into other Dell Products, such as webcams that Dell integrates into Dell laptops, desktops, and other computing devices. Greenthread reserves the right to amend its list of Dell-Sony Accused Products, including based on information learned in discovery.

5. Dell-Micron-DRAM Accused Products

Dell-Micron-DRAM Accused Products include all Dell Products containing or comprising dynamic random access memories (DRAMs) designed or manufactured (in whole or in part) by Micron), that have the same or similar structures, features, or functionalities as the exemplary discussed in Exhibits E-1 through E-6, regardless of how such products are branded. The identities

of such products are in the possession of the Dell Defendants and are expected to be learned over the course of this litigation, e.g., obtained through discovery. As described in Exhibits E-1 through E-6, Dell-Micron-DRAM Accused Products each infringe one or more claims of U.S. Patent Nos. 8,421,195 (claims 1-3, 5-6), 9,190,502 (claims 7-11), 10,510,842 (claims 1-2, 4-10, 12-18), 10,734,481 (claims 1-9, 13, 15-16, 20, 22-27, 31-33), 11,121,222 (claims 1-9, 13, 15-17, 20-21, 23-28, 32-34, 38-42, 44), 11,316,014 (claims 1-9, 13, 15-17, 20-21, 23-28). Greenthread reserves the right to amend its infringement contentions and claim charts regarding Dell-Micron-DRAM Accused Products, including based on information learned in discovery.

6. Additional Dell Accused Products

Upon information and belief, Dell products infringe one or more asserted claims of the asserted patents through their incorporation of dynamic random access memories (DRAMs), flash memory devices (e.g., in solid-state drives) and image sensors that meet the limitations of one or more asserted claims. The identities of such DRAMs, flash memory devices, and image sensors, their specifications, and their manufacturers and/or suppliers (if other than Dell) are in the possession of the Dell Defendants and are expected to be learned over the course of this litigation, e.g., obtained through discovery. More complete information about the Accused Products is in the possession of Defendants and is expected to be obtained through discovery. Greenthread explicitly reserves the right to supplement or alter its identification of accused products, as a matter of right, as permitted by the Court, based on the Court's claim constructions, based on additional information obtained through formal discovery or other means, and/or based on other circumstances.

III. CLAIM CHARTS FOR LITERAL INFRINGEMENT

Based upon information presently available to it, Greenthread's preliminary infringement claim charts are provided as attached Exhibits A-1 through A-6, B-1 through B-6, C-1 through C-

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6, D-1, D-2, D-3, and D-6, and E-1 through E-6 and F-1, F-2, F-3, and F-6 In each claim chart, the discussion for dependent claims should be read as incorporating by reference the discussion corresponding to the claims from which they depend. In addition, the discussion for each row in the chart should be read within the context of the discussion for the entire claim to which that row pertains. Where the charts incorporate excerpts of particular documents, the reference to those excerpts is exemplary and not to the exclusion of any other excerpt or version of the document or any versions of related documents.

These infringement claim charts are based upon Greenthread's investigation to date. More complete information about the Accused Products is in the possession of Defendants and is expected to be obtained through discovery. Greenthread explicitly reserves the right to supplement or alter its preliminary infringement claim charts, as a matter of right, as permitted by the Court, based on the Court's claim constructions, based on additional information obtained through formal discovery or other means, and/or based on other circumstances.

IV. DOCTRINE OF EQUIVALENTS

Unless otherwise noted in the claim charts, Greenthread alleges that Defendants infringe literally all asserted claims. To the extent any differences are alleged to exist between the asserted claims and Defendants' Accused Products, such differences are insubstantial and Defendants' Accused Products perform substantially the same function, in substantially the same way, to yield substantially the same result, and therefore Defendants infringe under the doctrine of equivalents.

Greenthread explicitly reserves the right to supplement or alter its disclosure concerning the doctrine of equivalents, as a matter of right, as permitted by the Court, based on the Court's claim constructions, based on additional information obtained through formal discovery or other means, and/or based on other circumstances. In the event that a claim limitation is deemed to be

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missing under a literal infringement analysis, Greenthread also reserves the right to demonstrate the presence of a substantial equivalent of such limitation and to pursue infringement under the doctrine of equivalents.

V. DOCUMENT PRODUCTION

Greenthread has produced documents pursuant to § II, page 2 of the Court's Standing Order Governing Proceedings (OGP) 4.1—Patent Cases dated April 14, 2022 in the production range GREENTHREAD-WDTX-000001-002065, including (1) documents evidencing conception and reduction to practice for each claimed invention at GREENTHREAD-WDTX-000349-000367, GREENTHREAD-WDTX-000741-000759, GREENTHREAD-WDTX-001061-001095, GREENTHREAD-WDTX-001249-001283, GREENTHREAD-WDTX-001378-001416, GREENTHREAD-WDTX-001727-001857, GREENTHREAD-WDTX-002026-002051; and (2) a copy of the file history for each patent in suit at the following:

Patent	File History Production Range
'842 patent	GREENTHREAD-WDTX-001059-1246
'481 patent	GREENTHREAD-WDTX-001247-1375
'222 patent	GREENTHREAD-WDTX-001376-1649
'195 patent	GREENTHREAD-WDTX-000349-739
'502 patent	GREENTHREAD-WDTX-000740-905
'014 patent	GREENTHREAD-WDTX-001866-2065

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Dated: January 23, 2023

MCKOOL SMITH, P.C.

/s/ *Alan L. Whitehurst*

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Telephone: 713-485-7300
Telecopier: 713-485-7344

Attorneys for Plaintiff Greenthread, LLC

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing document was served on the following counsel of record on August 29, 2022 via electronic mail using the following contact information.

J. Stephen Ravel Texas State Bar No. 16584975 **KELLY HART &HALLMAN LLP** Email: steve.ravel@kellyhart.com	Gregory S. Arovas (*Pro Hac Vice* filed) Robert A. Appleby (*Pro Hac Vice* filed) Todd M. Friedman (*Pro Hac Vice* filed) Leslie M. Schmidt (*Pro Hac Vice* filed) Jon R. Carter (*Pro Hac Vice* filed) Christopher DeCoro (*Pro Hac Vice* filed) **KIRKLAND & ELLIS LLP** 601 Lexington Avenue New York, NY 10022 Email: greg.arovas@kirkland.com Email: robert.appleby@kirkland.com Email: todd.friedman@kirkland.com Email: leslie.schmidt@kirkland.com Email: jon.carter@kirkland.com Email: christopher.decoro@kirkland.com Nyika O. Strickland (*Pro Hac Vice* filed) **KIRKLAND & ELLIS LLP** 300 North LaSalle Street Chicago, IL 60654 Email: nyika.strickland@kirkland.com Abigail Lauer Litow (*Pro Hac Vice* filed) John R. Rhine (*Pro Hac Vice* filed) **KIRKLAND & ELLIS LLP** 1301 Pennsylvania Avenue, N.W. Washington, D.C. 20004 Email: abigail.litow@kirkland.com Email: john.rhine@kirkland.com Bao Nguyen (*Pro Hac Vice* filed) **KIRKLAND & ELLIS LLP** 555 California Street 27th Floor San Francisco, CA 94104 Email: bao.nguyen@kirkland.com Abhishek Bapna (*pro hac vice* filed) George S. Soussou (admitted *pro hac vice* filed) Ryan Joseph Sheehan (*pro hac vice* filed)

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IPR2023-01243

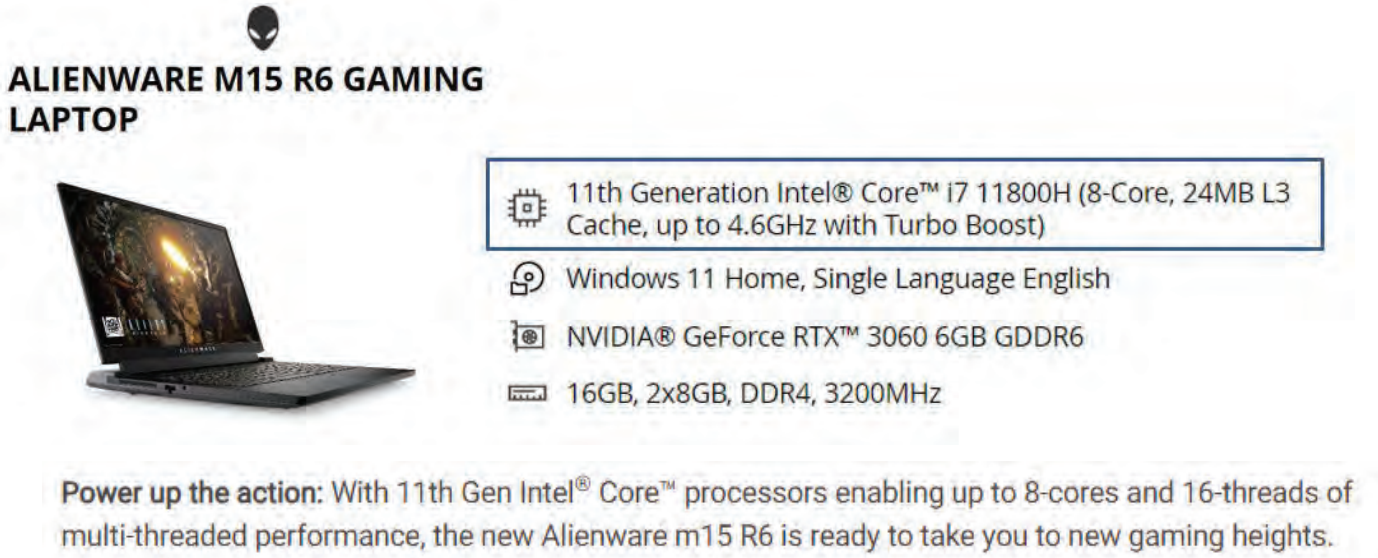
	Lupco (Lewis) V. Popovski (*pro hac vice* filed) **PATTERSON BELKNAP WEBB & TYLER LLP** 1133 Avenue Of The Americas New York, NY 10036 Email: abapna@pbwt.com Email: gsoussou@pbwt.com Email: rsheehan@pbwt.com Email: lpopovski@pbwt.com

/s/ *Alan L. Whitehurst*
Alan L. Whitehurst

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Exhibits A-1 to A-6
Intel Accused Products

Exhibit A-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs and Dell-Intel Accused Products include a semiconductor device. For example, each Dell-Intel Accused Products includes an Intel Accused CPU that comprises a semiconductor device as claimed. This chart includes exemplary information regarding a representative example of the Dell-Intel Accused Products, Dell's Alienware M15 R6 Gaming Laptop, which includes an Intel Core i7 11800H (a representative example of the 11th Generation "Tiger Lake" Intel Accused CPUs). The Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart and the other infringement contention claim charts because it includes a processor that is among the Intel Accused CPUs. The Intel Core i7 11800H is representative of the Intel Accused CPUs for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Intel Accused CPUs would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other Intel Accused CPUs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Similarly, the other Dell-Intel Accused Products would have been designed in a similar manner as the Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart because it includes a processor that is among the to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other Intel Accused CPUs contain similar features as the Core i7 11800H, and function in a similar way with respect to the features claimed in the asserted claims, and the other Dell-Intel Accused Products contain similar features as the Alienware M15 R6 Gaming Laptop, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.  *See* https://www.dell.com/en-us/shop/dell-laptops/alienware-m15-r6-gaming-laptop/spd/alienware-m15-r6-laptop#features_section

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Exhibit A-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products

Essentials — Export specifications

Product Collection	11th Generation Intel® Core™ i7 Processors
Code Name	Products formerly Tiger Lake
Vertical Segment	Mobile
Processor Number	i7-11800H
Status	Launched
Launch Date	Q2'21
Lithography	10 nm SuperFin
Recommended Customer Price	$395.00

See https://ark.intel.com/content/www/us/en/ark/products/213803/intel-core-i711800h-processor-24m-cache-up-to-4-60-ghz.html

SANTA CLARA, Calif., Sept. 2, 2020 – Intel today unleashed a new era of laptop performance with the launch of its next-generation mobile PC processors and the evolution of its broad ecosystem partnerships that are propelling the mobile PC industry forward. New 11th Gen Intel Core processors with Intel Iris Xe graphics (code-named "Tiger Lake") are the world's best processors for thin-and-light laptops with unmatched capabilities for real-world productivity, collaboration, creation, gaming and entertainment across Windows and ChromeOS-based laptops.

Leveraging Intel's new SuperFin process technology, 11th Gen Intel Core processors optimize power efficiency with leading performance and responsiveness while running at significantly higher frequencies versus prior generations. More than 150 designs based on 11th Gen Intel Core processors are expected from partners including Acer, Asus, Dell, Dynabook, HP, Lenovo, LG, MSI, Razer, Samsung and others.

See https://www.intel.com/content/www/us/en/newsroom/news/11th-gen-tiger-lake-evo.html#gs.xa0yxa

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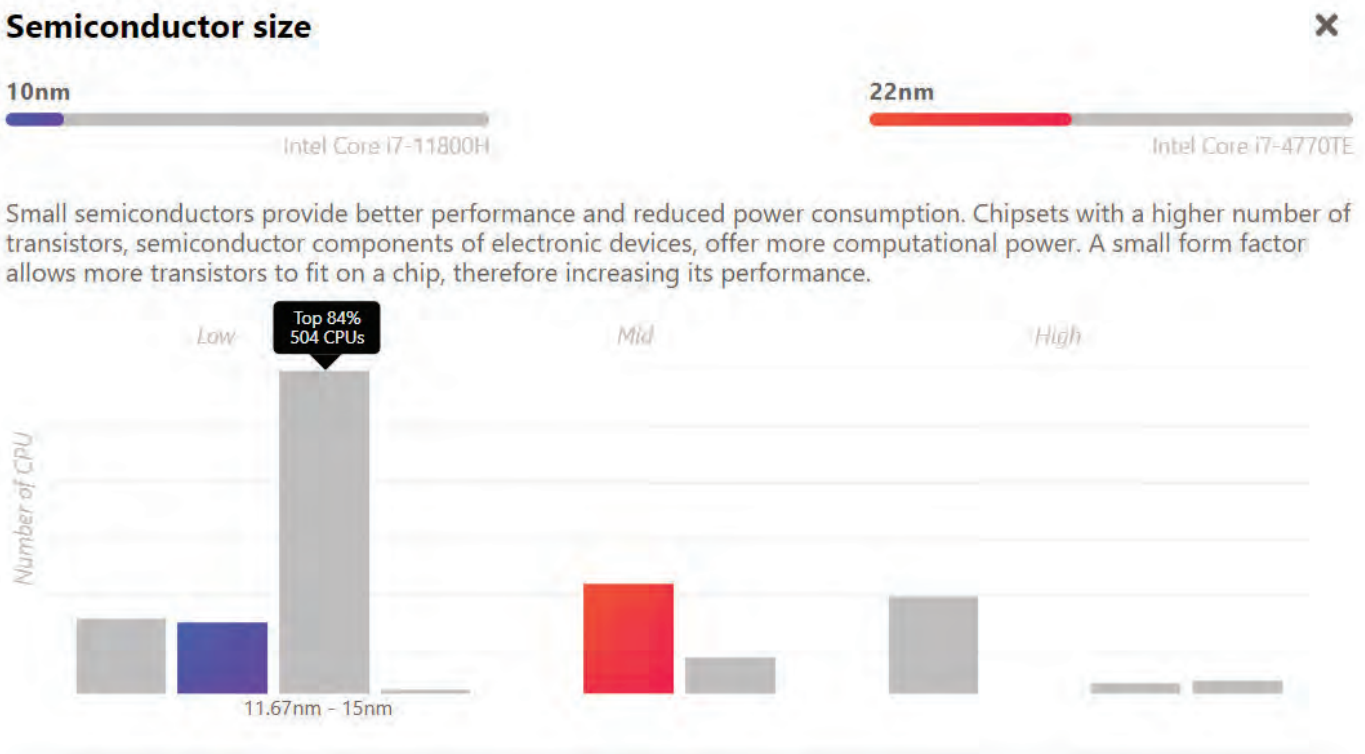
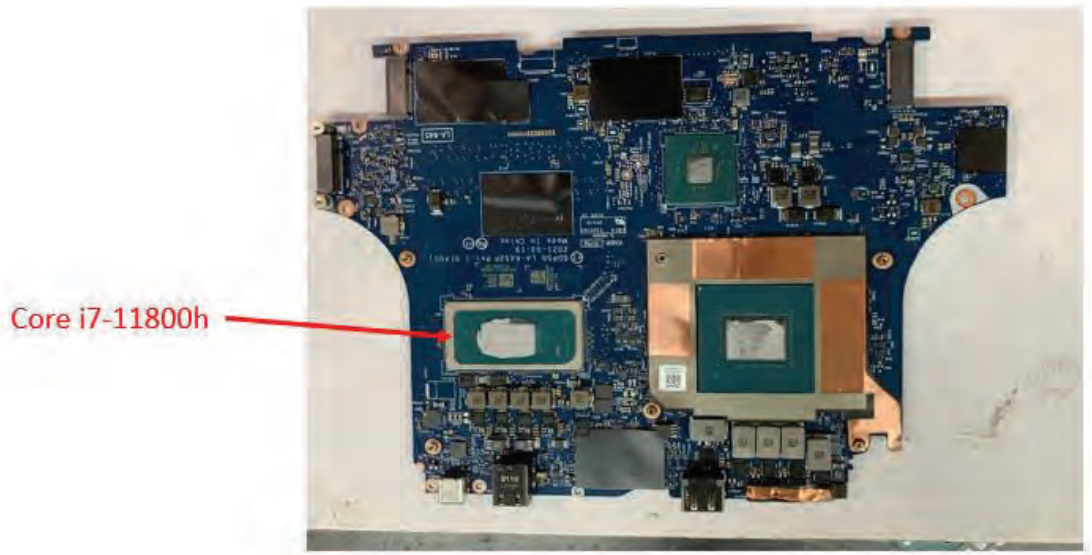
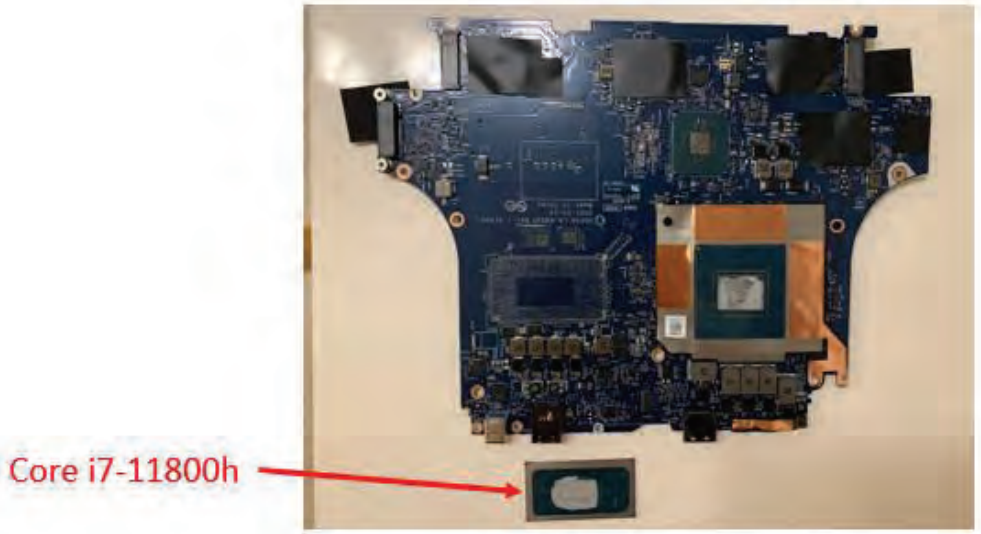
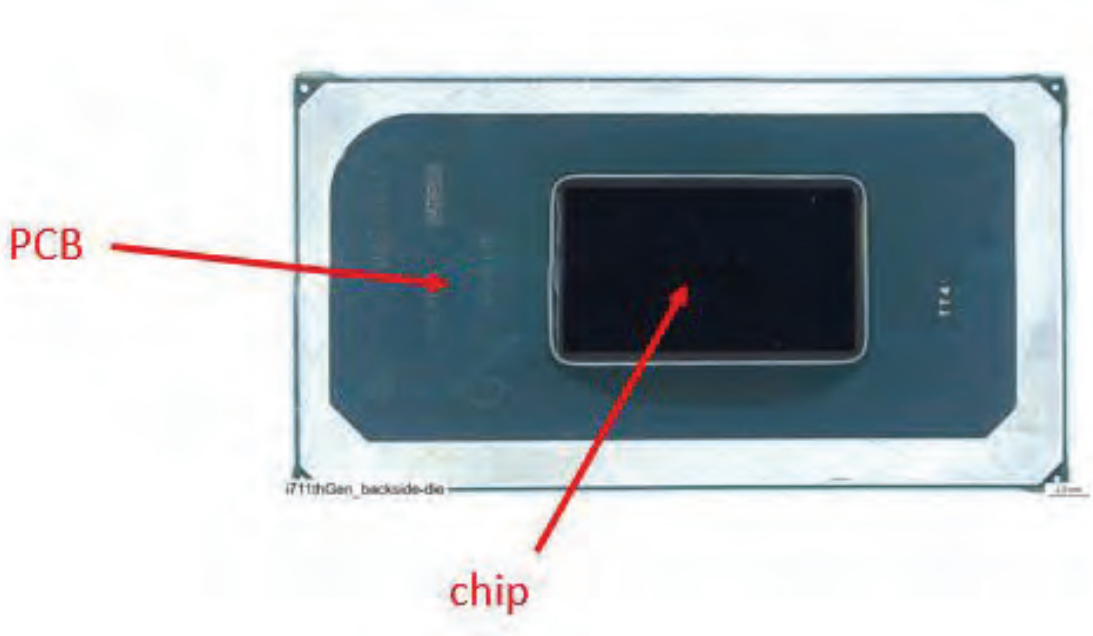
U.S. Patent No. 10,510,842	Accused Products
	The Intel Accused CPUs, of which the i7-11800H is one example, are semiconductor devices.  *See* https://versus.com/en/intel-core-i7-11800h-vs-intel-core-i7-4770te
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary Intel Accused CPUs (the Core i7-11800h discussed above) incorporated into an exemplary Dell Product (the Alienware M15 R6 Gaming Laptop discussed above) reveals the presence of such a substrate.

Exhibit A-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
	The Alienware M15 R6 Gaming Laptop is shown below:  The Core i7-11800h is shown below on the motherboard of the Alienware M15 R6 Gaming Laptop: 

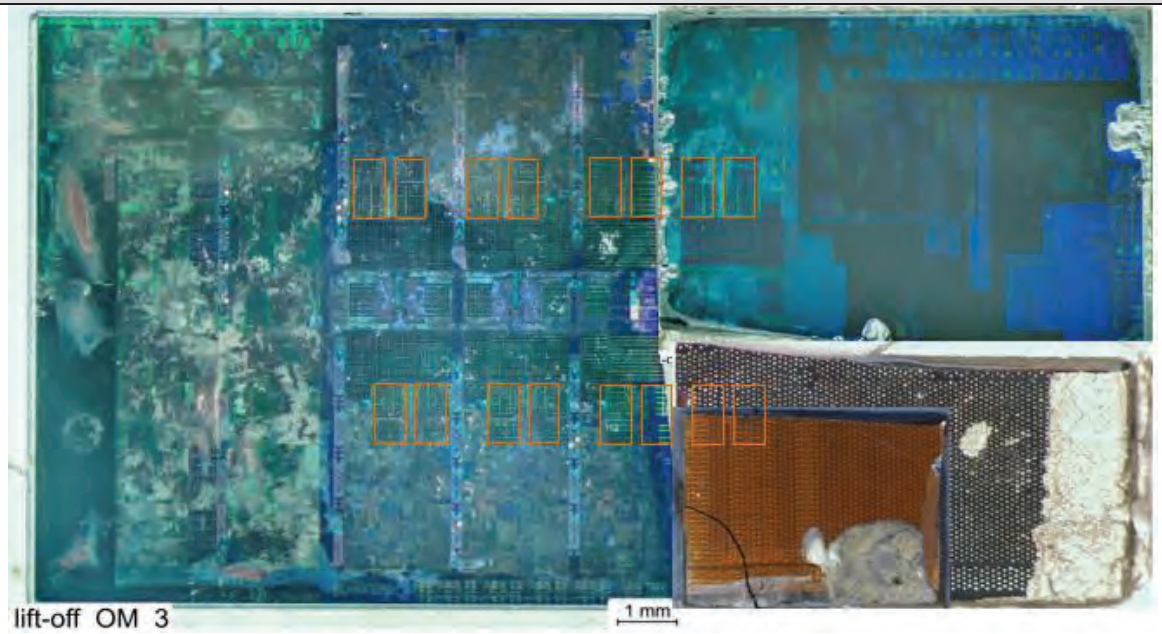
U.S. Patent No. 10,510,842	Accused Products
	The Core i7-11800h after removal from the motherboard is shown below:  The printed circuit board (PCB) of the Core i7-11800h before removal of the chip is shown below:

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U.S. Patent No. 10,510,842	Accused Products
	 The chip is shown below after etching to prepare it for scanning electron microscopy (SEM):

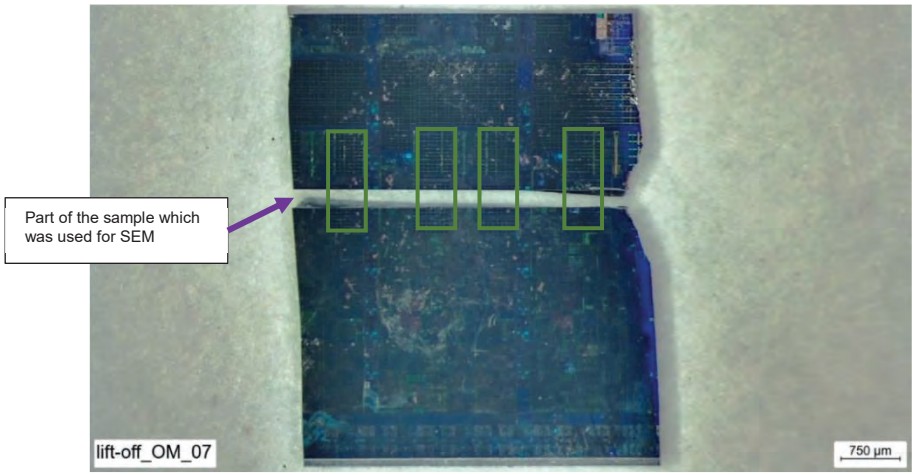
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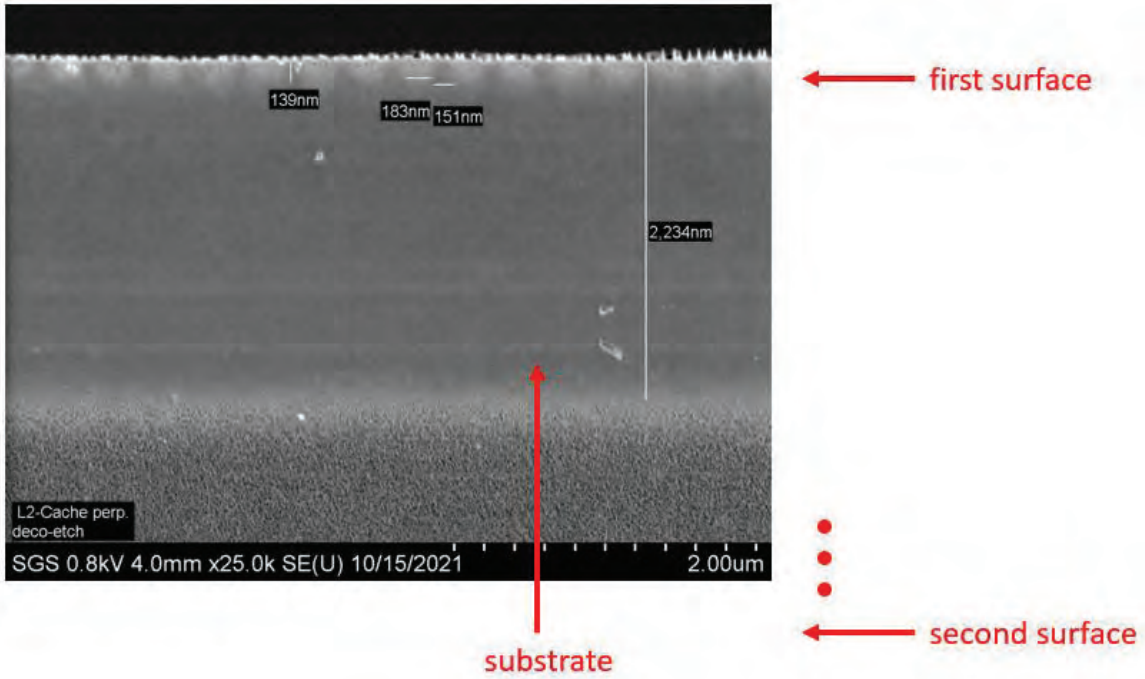
U.S. Patent No. 10,510,842	Accused Products

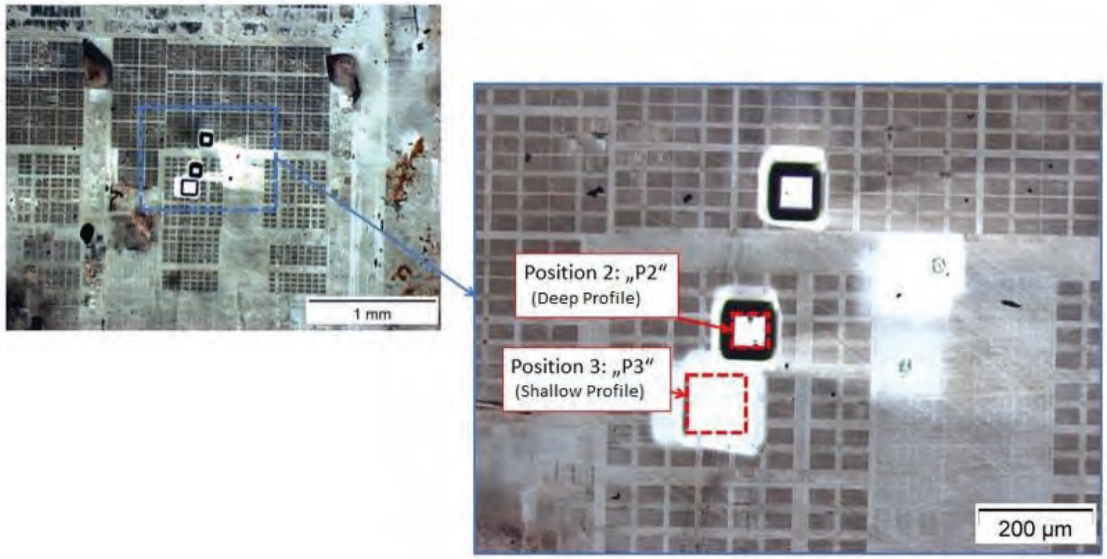


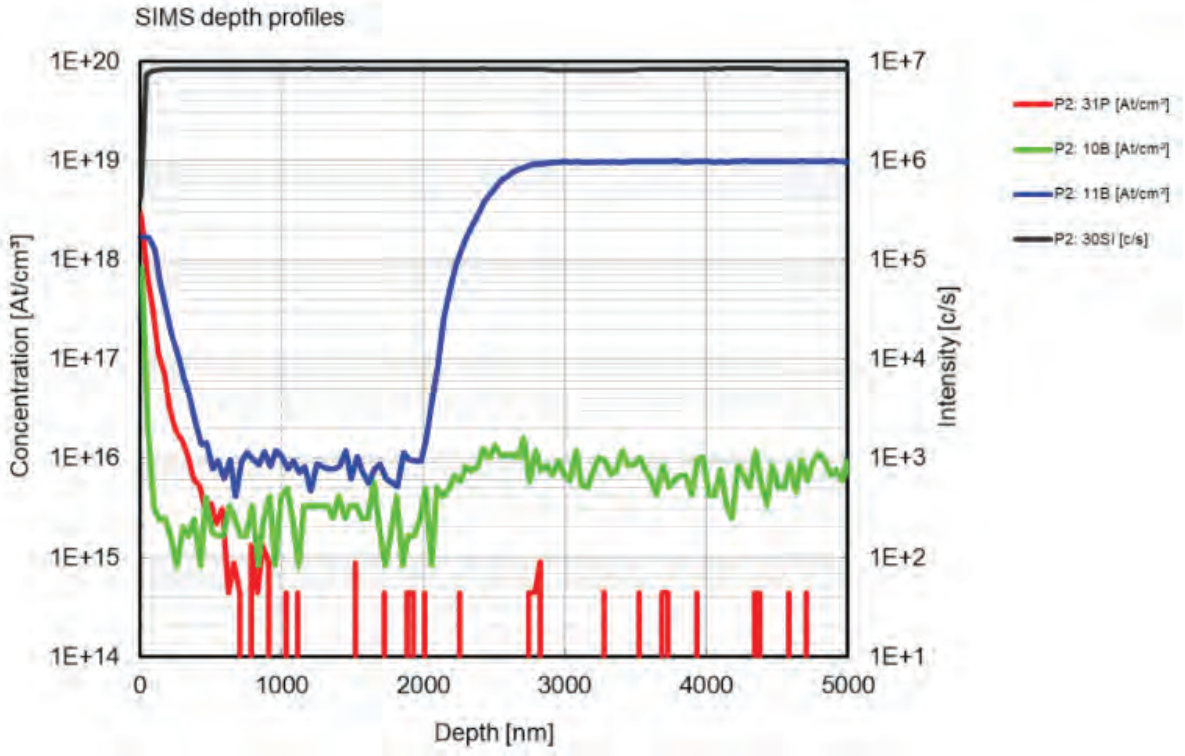
Orange rectangles have been superimposed in the above image to designate L2 cache areas of the chip.

To analyze the topography and composition of the chip, a horizontal cut was made (cleaved) through the L2 cache, as shown below:



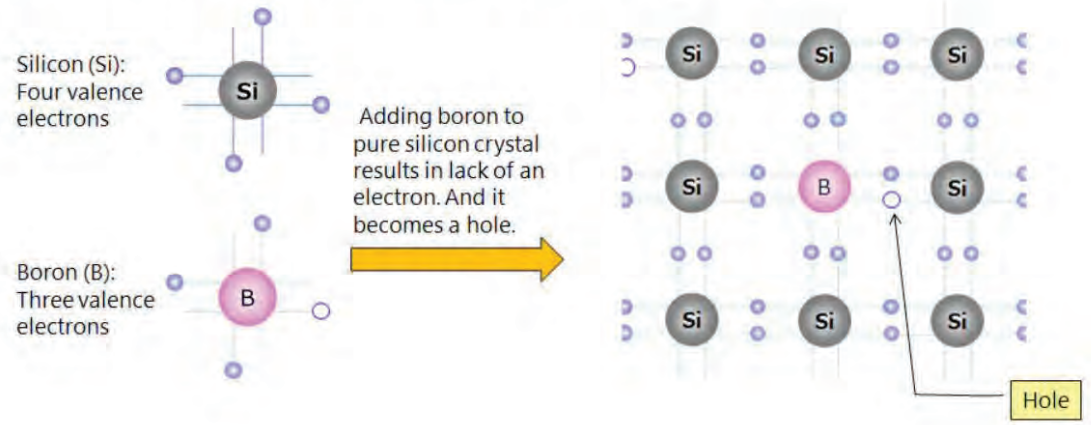
U.S. Patent No. 10,510,842	Accused Products
	The following cross sectional SEM image at the cleaved L2 cache sample after a decoration etch shows the claimed substrate. The first surface is shown near the top of the image, and the second surface is outside (below) the vertical range of this image.  Dynamic secondary ion mass spectrometry (SIMS) reveals information regarding the composition of the L2 cache sample. SIMS was performed at position P2 shown below:

U.S. Patent No. 10,510,842	Accused Products
	 The following graph obtained via SIMS analysis, which shows concentration at position P2, reveals the presence of p-type doping (a first doping type) in the substrate.

U.S. Patent No. 10,510,842	Accused Products
	 Boron (having chemical symbol B) has three valence electrons and is a p-type dopant.

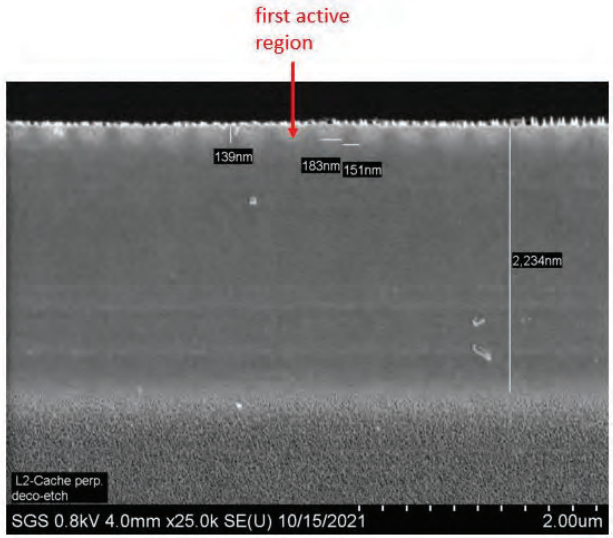
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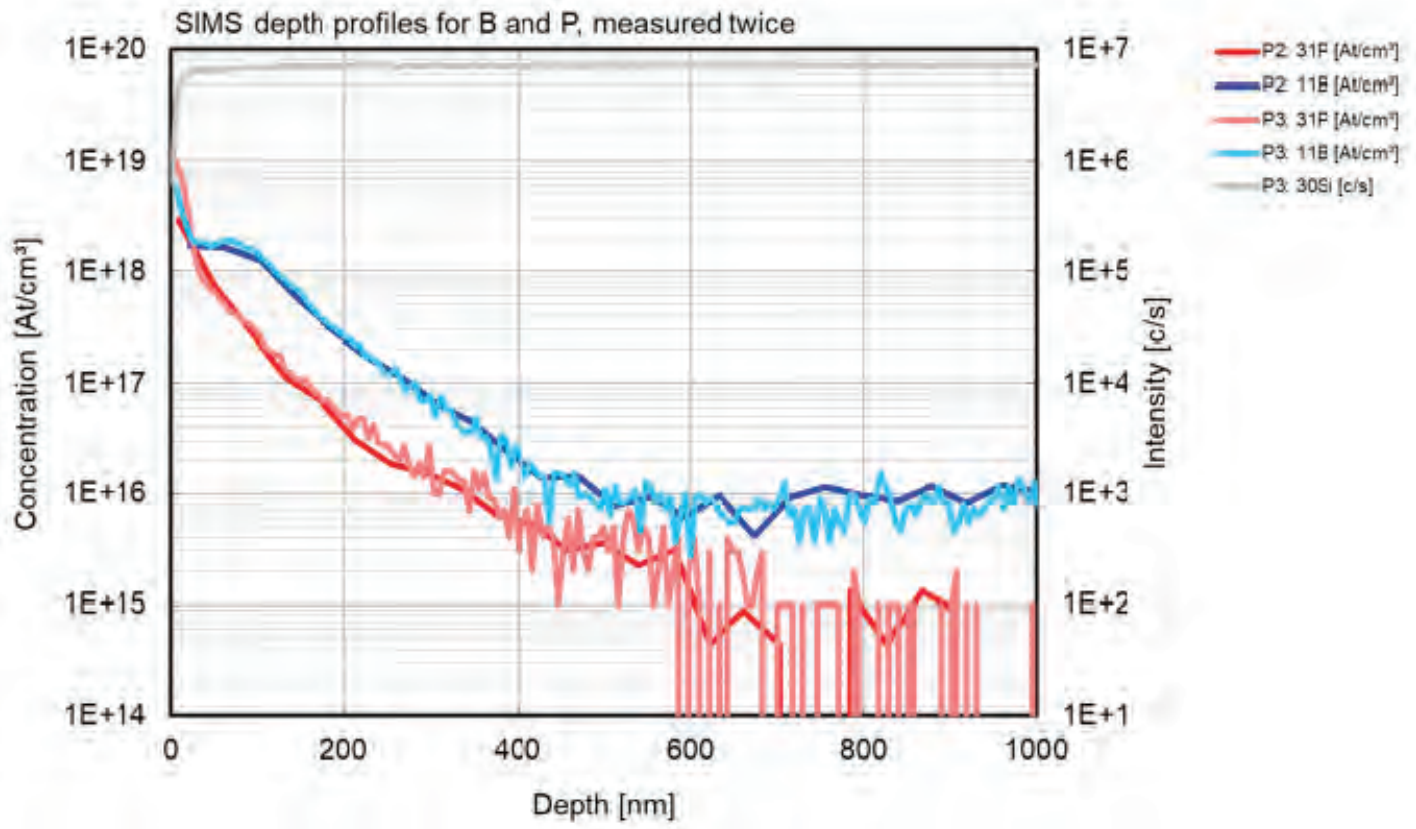
Exhibit A-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons. Thus, the SIMS graph above shows the concentration of boron, which is a p-type (first doping type) dopant, at a first doping level.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in SEM imagery, the Core i7-11800h (discussed above as an exemplary Intel Accused CPUs) incorporated into an exemplary Dell Product (the Alienware M15 R6 Gaming Laptop discussed above) includes a first active region disposed adjacent the first surface of the substrate.

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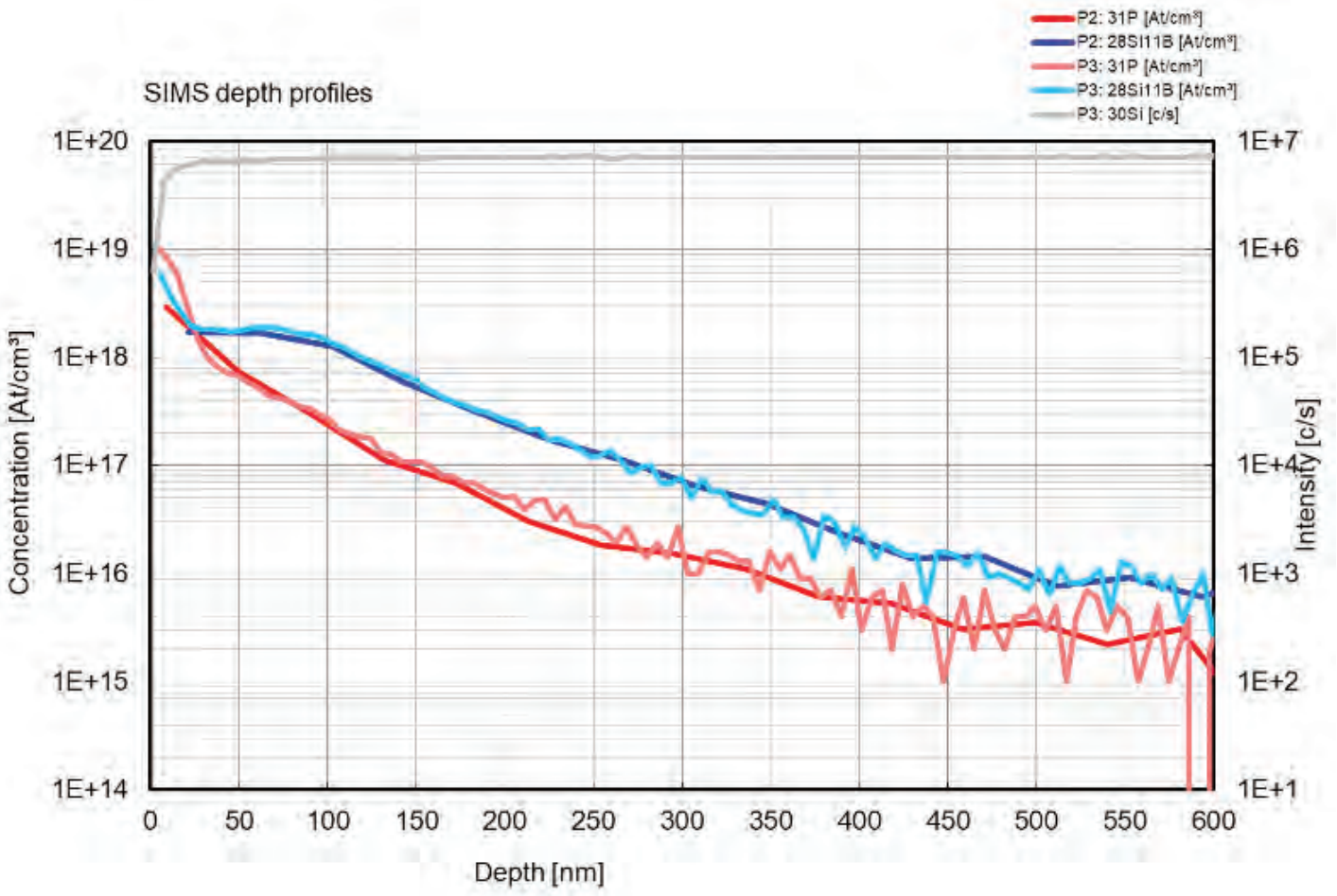
Exhibit A-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
	 The first active region has n-type doping (a second doping type opposite in conductivity to the first doping type), at the portion of the image having lighter shading than the substrate. The following graph obtained via SIMS analysis, which shows concentration at position P3 (P3 is discussed above for Element 1), reveals the presence of n-type doping (e.g., phosphorus-31).

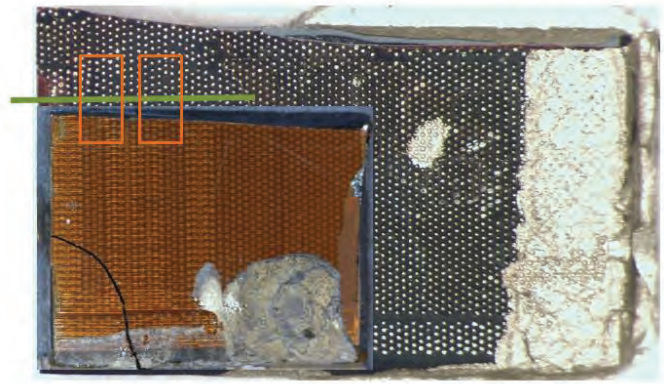
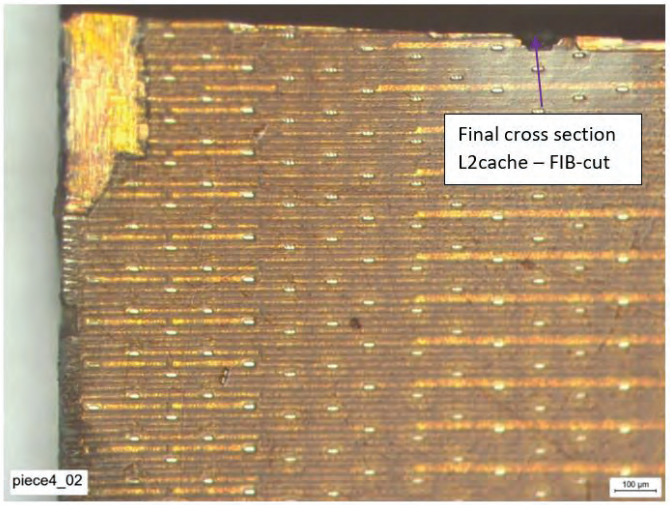
U.S. Patent No. 10,510,842	Accused Products
	 The following is the same data as above but shown only to depth of 600nm.

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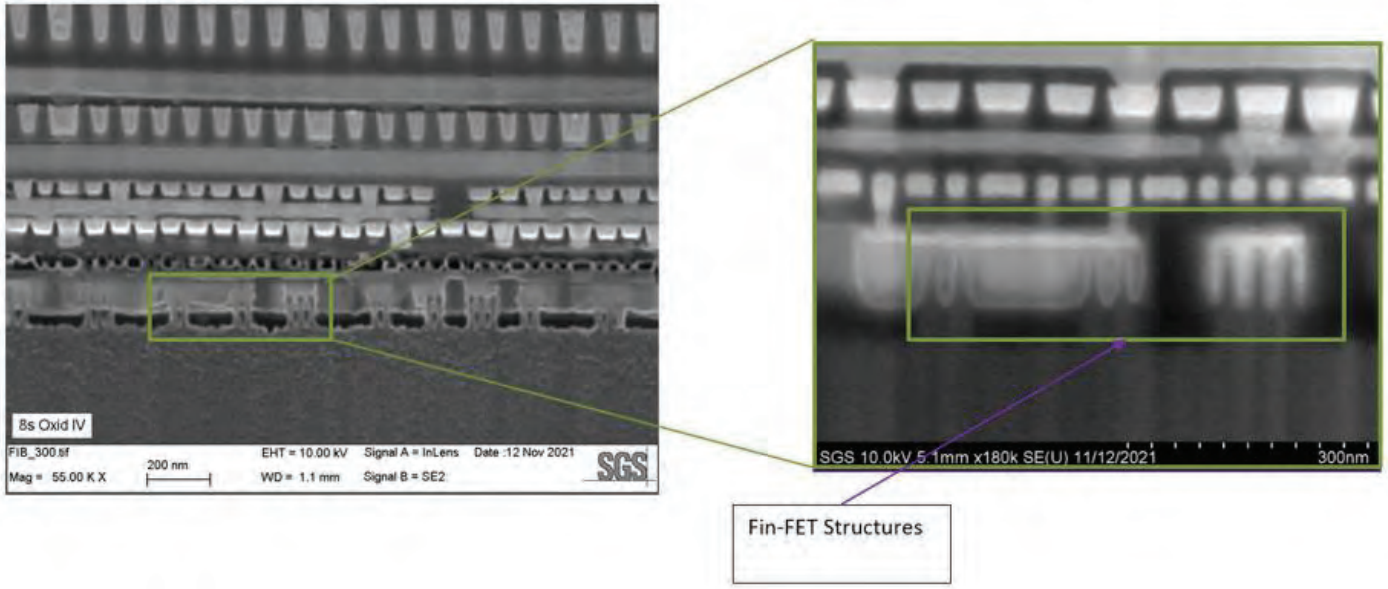
U.S. Patent No. 10,510,842	Accused Products

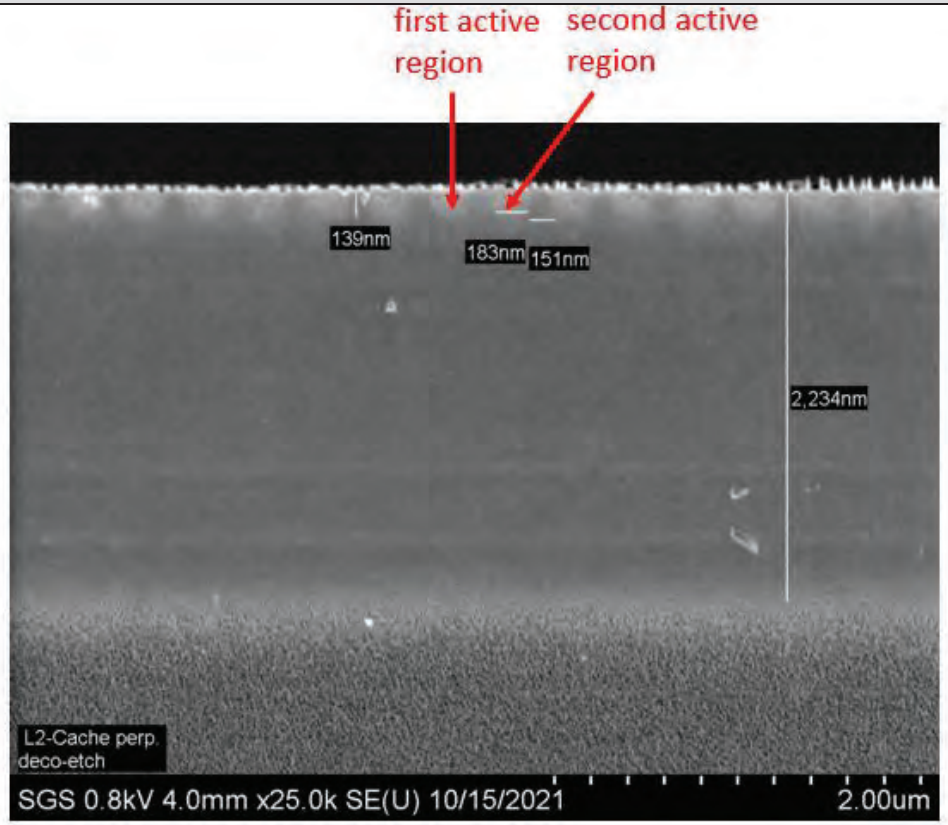


The first active region is a region within which transistors can be formed. For example, transistors are visible in SEM images as shown below. A cut was made (cleaved) at the position specified below in the L2 cache:

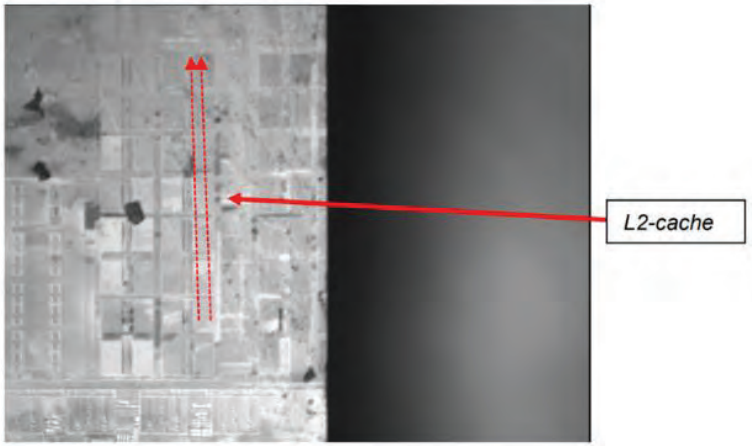
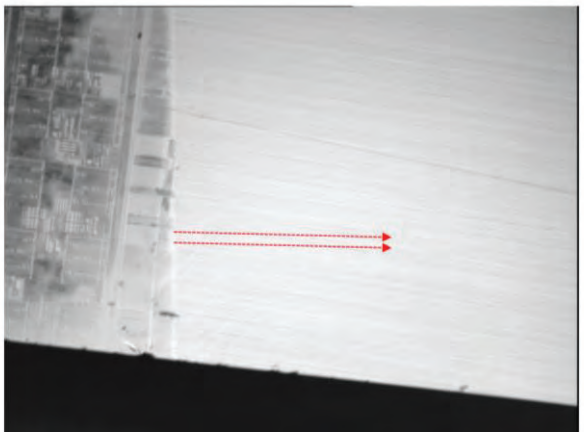
U.S. Patent No. 10,510,842	Accused Products
	  SEM performed at the above cut of the L2 cache reveals the presence of FinFETs (a type of transistors).

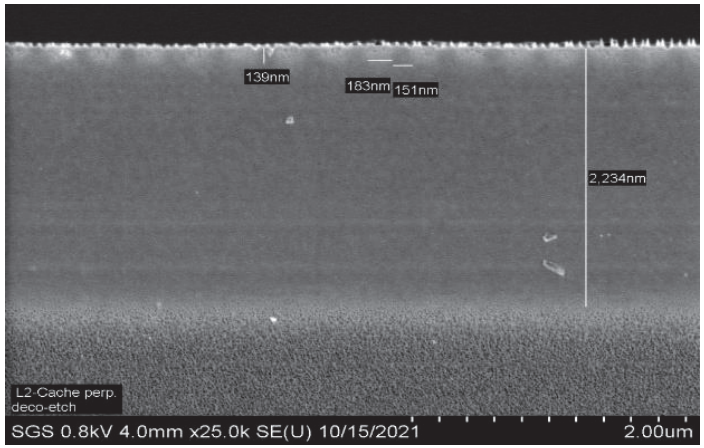
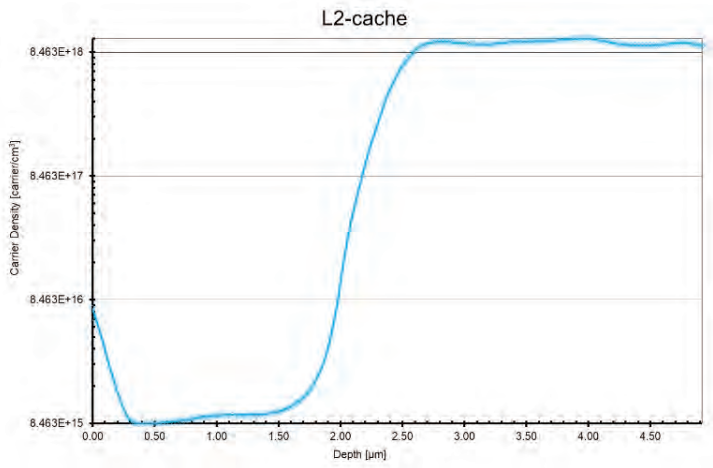
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	 Upon information and belief, the transistors (e.g., FinFETs) are formed in the first active region. Additional information regarding the details of the active region are in the possession of the Defendants and is expected to be obtained through discovery.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, as shown in the SEM image below, a second active region separate from the first active region is disposed adjacent to the first active region.

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	 The second active region is a region within which transistors can be formed. For example, as explained above for Element 2, the L2 cache includes transistors (e.g., FinFETs), and upon information and belief, transistors are formed in the second active region. Alternatively, the dark region to the right of the above-labeled first active region is also a second active region as claimed.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at Elements 2-3.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device comprising at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate. For example, spreading resistance profiling (SRP) analysis shows a graded dopant concentration, as explained below. SRP and SIMS are well-known methods of studying semiconductor devices. *See e.g.*, T. Clarysse, et al. *Characterization of electrically active dopant profiles with the spreading resistance probe*, Materials Science and

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concentration to aid carrier movement from the first surface to the second surface of the substrate.	Engineering (December 2004). SRP provides an "electrical depth profile" and "gives intrinsically electrical information." *Id.* at 141, 157. Each SRP data point reflects carrier movement and dopant concentration at the physical location at which it was taken. The plots of SRP data taken from accused products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. That is the SRP plots included in Greenthread's infringement charts evidence both dopant gradients and the corresponding vertical electric drift fields. The silicon sample from the L2 cache cut discussed above was polished at an angle toward the top surface, and a defined profile was generated over the depth of the sample via the grinding angle. The two adjacent parallel dashed arrows in the figures below indicate the direction of grinding used for this processing. The polished section was then electrically characterized using a step prober, which generated a depth profile.   A graded dopant concentration is visible in the concentration vs. depth graph shown at right below, which was obtained via SRP analysis

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	(the cross-section discussed above for Element 2 is reproduced at left below for reference).   As shown in the cross section above at left, the first and second regions are at a depth corresponding to the the initial negative-slope (downward sloping) portion of the concentration graph (which is shown above at right). Thus, at least a portion of at least one of the first and second active regions has at least one graded dopant concentration. The graded dopant concentration is to aid carrier movement from the first surface to the second surface of the substrate (e.g., downward in the cross section shown above at left). The graded dopant concentration is also observed from the SIMS analysis discussed above for Claim 1, Element 1 and shown below.

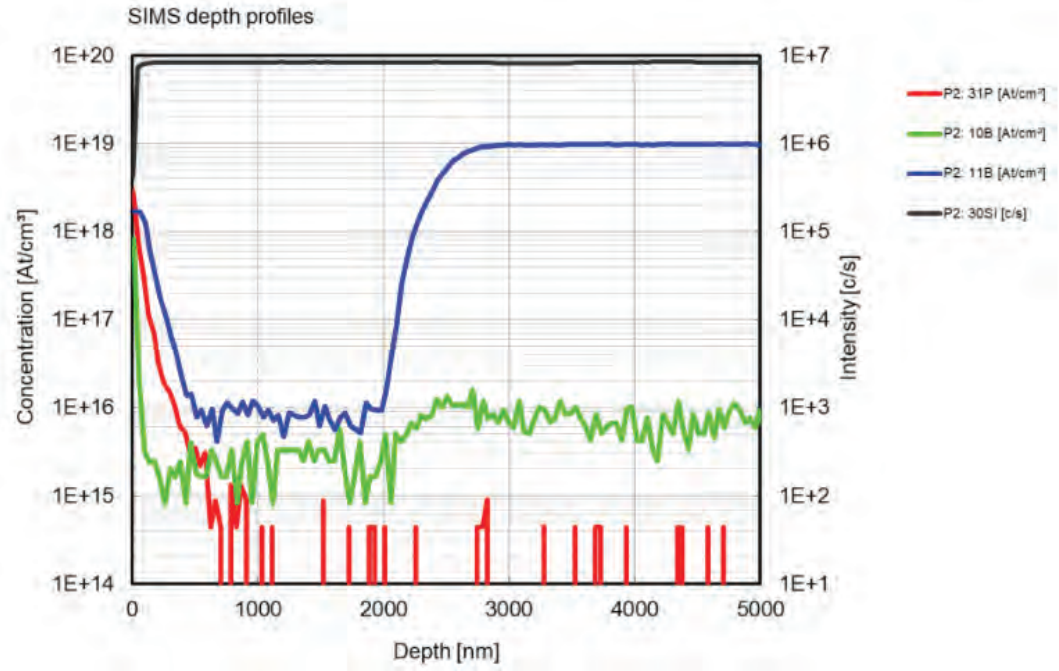
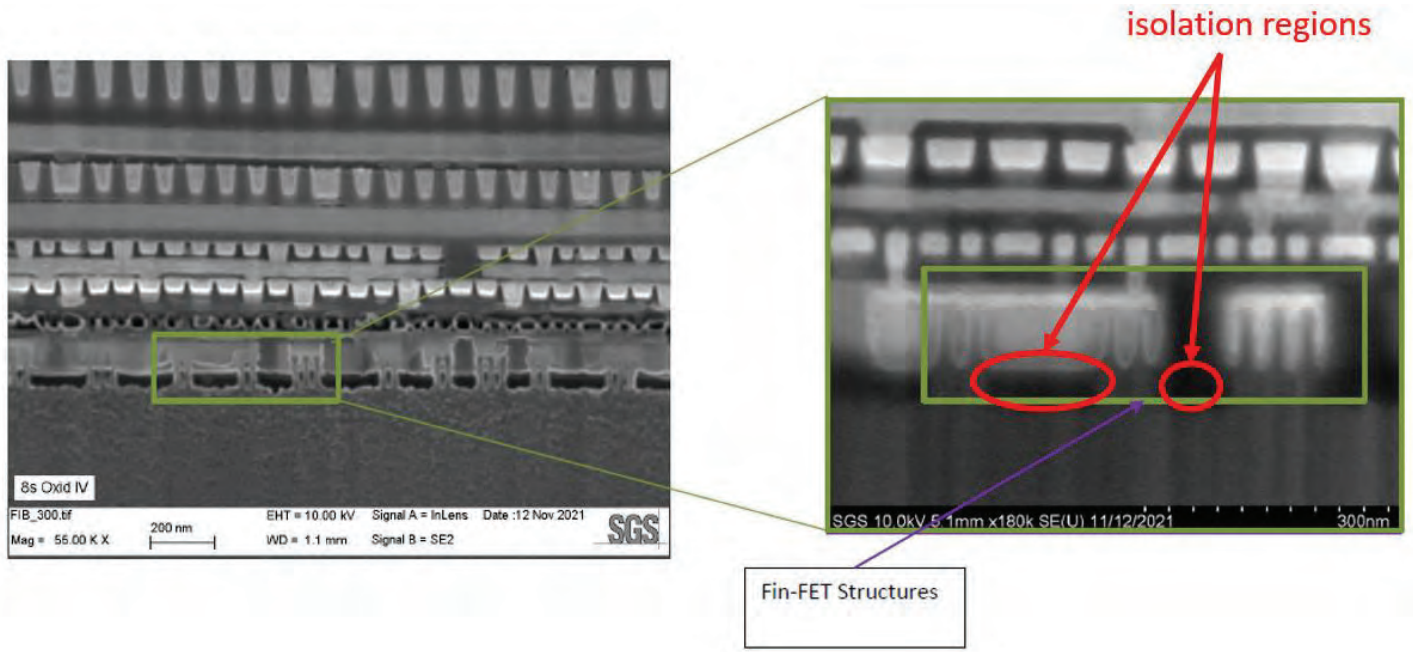
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2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The substrate of the semiconductor device of the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, is a p-type substance, as discussed above for Element 1 of Claim 1. For example, SIMS analysis shows that the substrate is a p-type substrate based on the concentration of boron shown in the SIMS graph discussed for Claim 1, Element 1.
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The substrate of the semiconductor device of the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, has epitaxial silicon on top of a nonepitaxial substrate. Upon information and belief, the substrate used in the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, is a single-crystal silicon wafer.
5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. As discussed above for element 2 of claim 1, the first active region has n-type doping. The first active region accordingly contains p-channel devices. The second active region also has n-type doping and contains p-channel devices. Thus, the first active region and second active region contain p-channel devices, which are located at the light-shaded regions out of the alternating light- and dark-shaded regions of the SEM image discussed above for Claim 1, Element 1. For example, FinFETs (discussed above for Claim 1) are active transistors, and they are located in the active regions.

Exhibit A-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. As shown in the SIMS graph discussed for Claim 1, Element 2, the first active region and second active region have n-type dopant and contain p-channel devices in n-wells. The wells have a graded dopant concentration as seen in the graph (P2: 31P, phosphorus).
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the first active region and second active region are each separated by at least one isolation region. For example, isolation regions are annotated with red ovals in the below right SEM image that shows FinFETs (discussed above for Claim 1, Element 2).  Information about the fabrication process for the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, including usage of isolation regions, which are commonly used in semiconductor processing, is in the possession of Defendants and is expected to be obtained through discovery.
8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them. Information about the fabrication process for the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, including usage of an ion implantation process, is in the possession of Defendants and is expected

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	to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 5.
10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 2.

U.S. Patent No. 10,510,842	Accused Products
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 6.
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Elements 2 and 3.
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. As discussed above for Claim 1, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include an L2 cache having the first and second active regions. Upon information and belief, the L2 cache includes CMOS transistors (e.g., the FinFET transistors discussed above for Claim 1, or other CMOS transistors) formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used in the L2 cache are in the possession of Defendants and are expected to be obtained through discovery.

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drain, a gate and a channel region.	

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Exhibit A-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device. *See* Exhibit A-1, Claim 1, Preamble. This chart includes exemplary information regarding a representative example of the Dell-Intel Accused Products, Dell's Alienware M15 R6 Gaming Laptop, which includes an Intel Core i7 11800H (a representative example of the 11th Generation "Tiger Lake" Intel Accused CPUs). The Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart and the other infringement contention claim charts because it includes a processor that is among the Intel Accused CPUs. The Intel Core i7 11800H is representative of the Intel Accused CPUs for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Intel Accused CPUs would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, the other Intel Accused CPUs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Similarly, the other Dell-Intel Accused Products would have been designed in a similar manner as the Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart because it includes a processor that is among the to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other Intel Accused CPUs contain similar features as the Core i7 11800H, and function in a similar way with respect to the features claimed in the asserted claims, and the other Dell-Intel Accused Products contain similar features as the Alienware M15 R6 Gaming Laptop, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.

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Exhibit A-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. As shown in the following graph obtained by SIMS analysis (*see* Exhibit A-1, Claim 1, Element 1 regarding the SIMS analysis), the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them (e.g., the Core i7-11800h incorporated into an exemplary Dell Product (the Alienware M15 R6 Gaming Laptop) as discussed in Exhibit A-1, Claim 1, Preamble) include at least one n-well (corresponding to phosphorus-31) or p-well (corresponding to boron-11), adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate. N-wells and p-wells in semiconductor devices often have a depth of about a few hundred nanometers, and at such depths a graded dopant concentration is seen in the below graph. *See also* SRP analysis discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.

Exhibit A-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

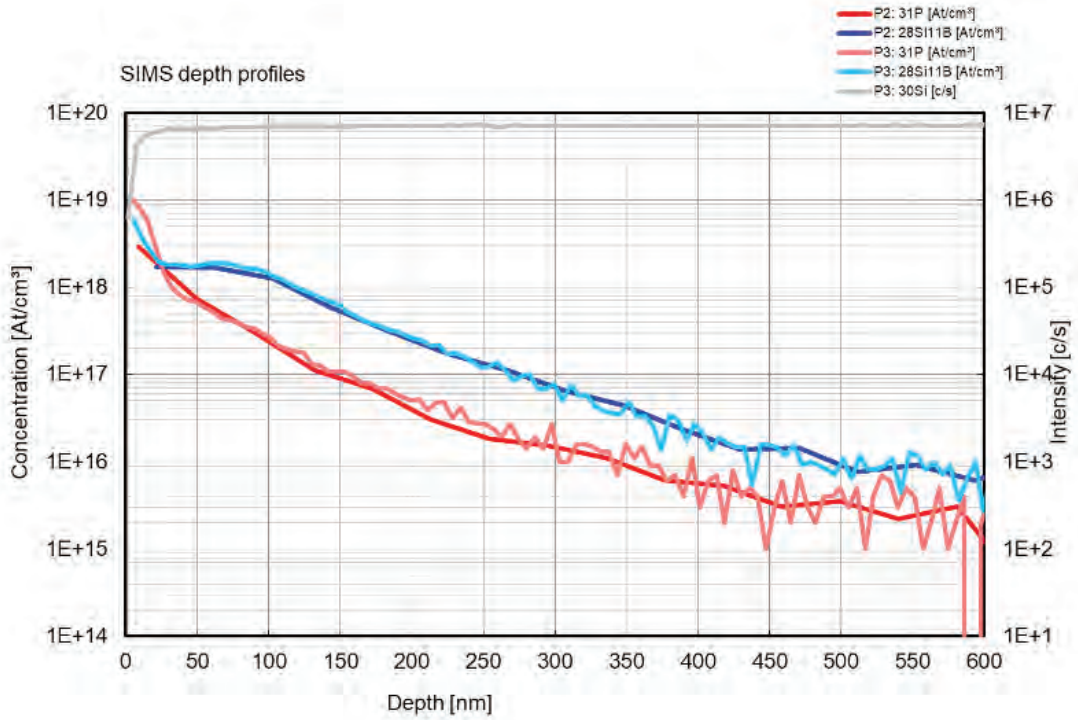
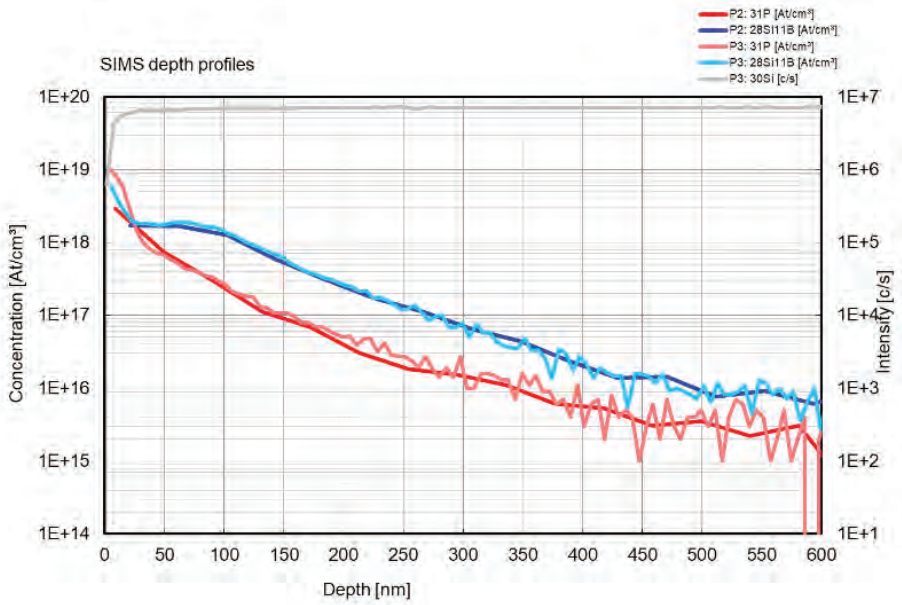
U.S. Patent No. 10,734,481	Accused Products
	
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 2.
3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 4.
4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 5.

Exhibit A-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 6.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 7.
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 8.
8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1-3.
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. Dopant composition is revealed by the SIMS graph below (*see* Exhibit A-1, Claim 1, Element 1 regarding the SIMS analysis), where boron-11 is a p-type dopant and phosphorus-31 is an n-type dopant.

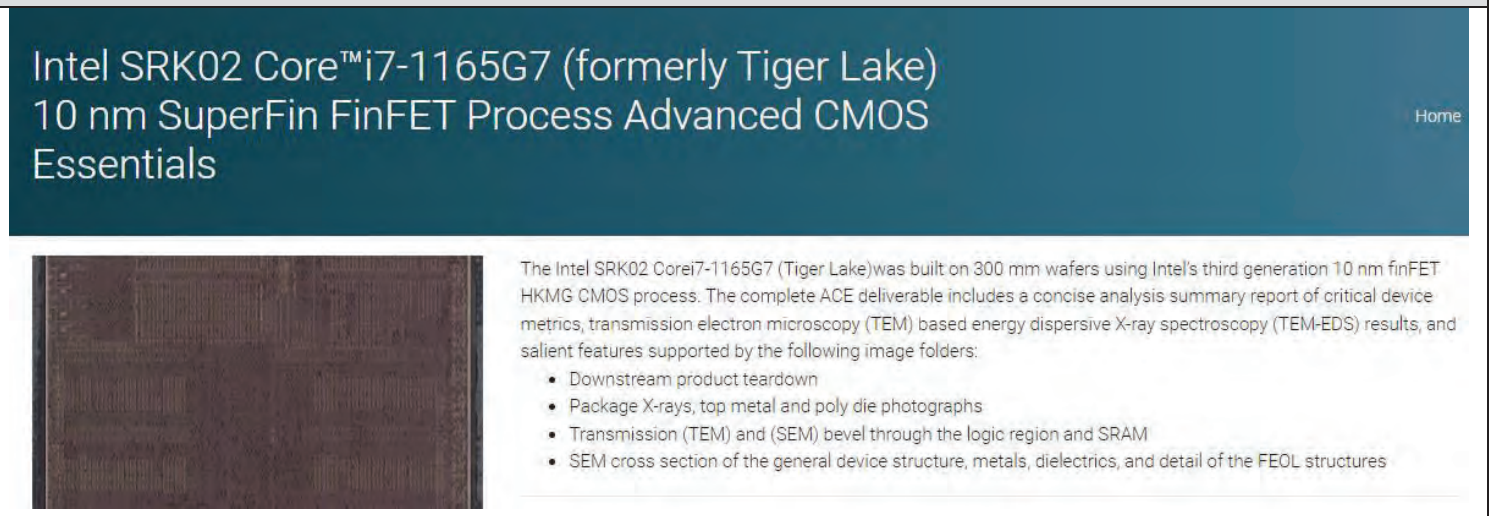
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U.S. Patent No. 10,734,481	Accused Products
	
13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 18.
15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claims 4 (regarding nonepitaxial substrate), 18 (regarding CMOS). Intel's Core i7-1165G7 (Tiger Lake) is a CMOS device, and the Core i7 11800H (which is another representative example of the 11th Generation Tiger Lake Intel Accused CPUs) is also a CMOS device.

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Exhibit A-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
	 *See* https://www.techinsights.com/products/ace-2010-801
17. The semiconductor device of claim 1, wherein the device is a logic device.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. For example, the L2 cache (discussed at Exhibit A-1, Claim 1, Element 1) is a logic device.
18. The semiconductor device of claim 17, wherein the device is central processing unit.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. For example, the Core i7-11800H (representative of the Intel Accused CPUs) is a central processing unit (CPU).

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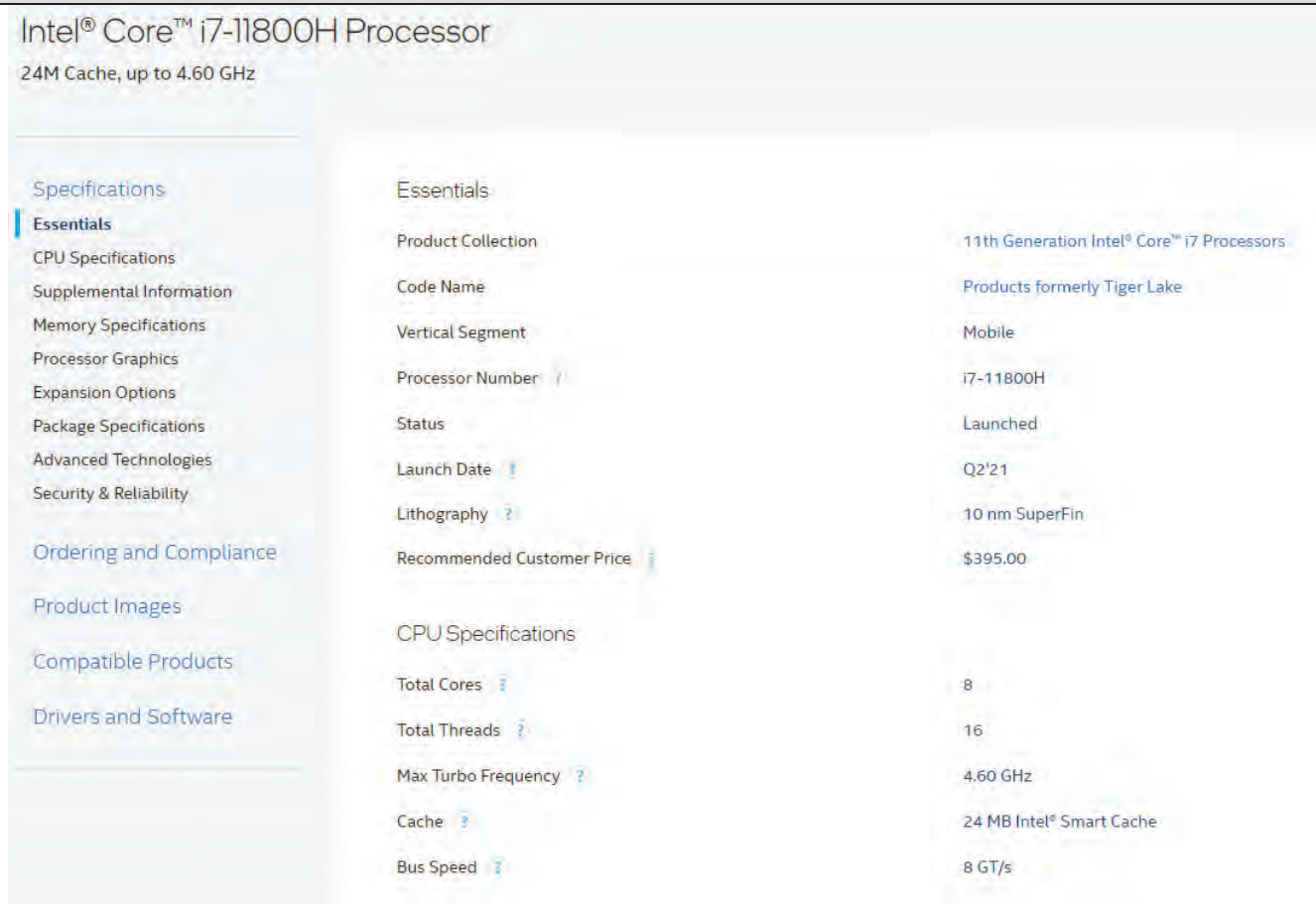
U.S. Patent No. 10,734,481	Accused Products
	 *See* https://ark.intel.com/content/www/us/en/ark/products/213803/intel-core-i711800h-processor-24m-cache-up-to-4-60-ghz.html
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.

Exhibit A-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 9, Element 2.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 9, Element 3.
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 6, Element 1.
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 2.

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Exhibit A-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 4.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 5.
25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 6.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 7.
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 8.
32. The semiconductor device of claim 20, wherein the substrate is a	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 15.

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U.S. Patent No. 10,734,481	Accused Products
complementary metal oxide semiconductor (CMOS) device.	
34. The semiconductor device of claim 20, wherein the device is a logic device.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 17.
35. The semiconductor device of claim 34, wherein the device is central processing unit.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 18.

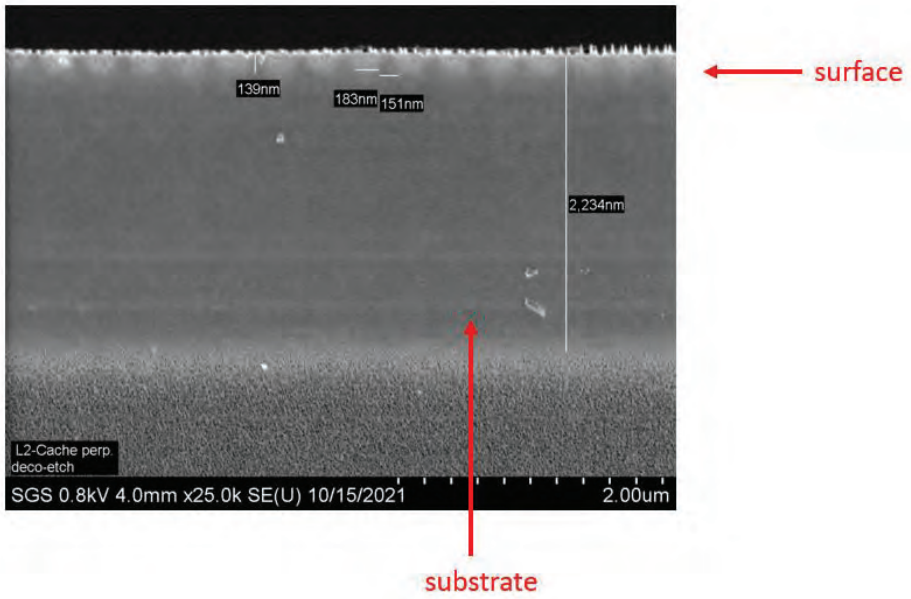
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Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a VLSI semiconductor device. Each Intel Accused CPU incorporated in each Dell-Intel Accused Product is a semiconductor device (*see* Exhibit A-1, Preamble of Claim 1) with millions of transistors, and is a VLSI semiconductor device. *See* https://www.dictionary.com/browse/vlsi **Intel Core i7-11800H specifications** **General Info** Name: Intel Core i7-11800H Core name: Tiger Lake-H Generation: 11th Architecture: x86 Release date: March 20, 2021 Frequency: 2.3 GHz Turbo frequency: 4.6 GHz Cores: 8 Threads: 16 Socket: FCBGA1440 Bus Speed: 8 GT/s Thermal Design Power (TDP): 40 W Min TDP: 35 W Max. Temperature: 100 °C Hyper-threading: Yes L3 Cache: 24 MB Cache: 24 MB Instruction Set Extensions: Intel SSE4.2, Intel AVX2, Intel SSE4.1 Word Size: 64 bit TSMC FinFET process (Lithography): 14 nm Transistor count: 8200 million *See* https://chipguider.com/?proc=intel-core-i7-11800h This chart includes exemplary information regarding a representative example of the Dell-Intel Accused Products, Dell's Alienware M15 R6 Gaming Laptop, which includes an Intel Core i7 11800H (a representative example of the 11th Generation "Tiger Lake" Intel Accused CPUs). The Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart and the other infringement contention claim charts because it includes a processor that is among the Intel Accused CPUs. The Intel Core i7 11800H is representative of the Intel Accused CPUs for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Intel Accused CPUs would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, the other Intel Accused CPUs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Similarly, the other Dell-Intel Accused Products would have been designed in a similar manner as the Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart because it includes a processor that is among the to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other Intel Accused CPUs

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U.S. Patent No. 11,121,222	Accused Products
	contain similar features as the Core i7 11800H, and function in a similar way with respect to the features claimed in the asserted claims, and the other Dell-Intel Accused Products contain similar features as the Alienware M15 R6 Gaming Laptop, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 1. 
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.

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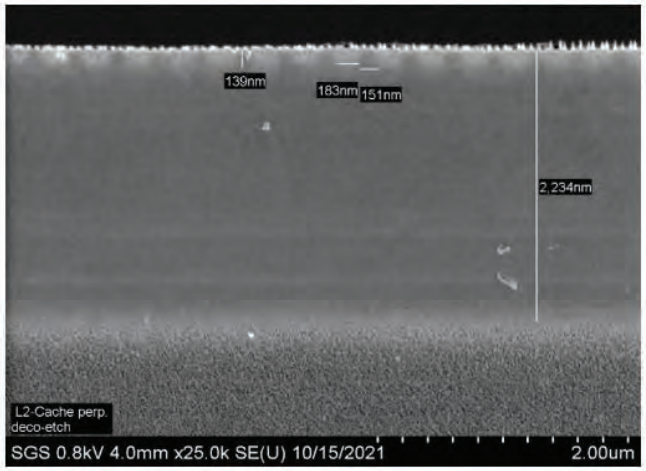
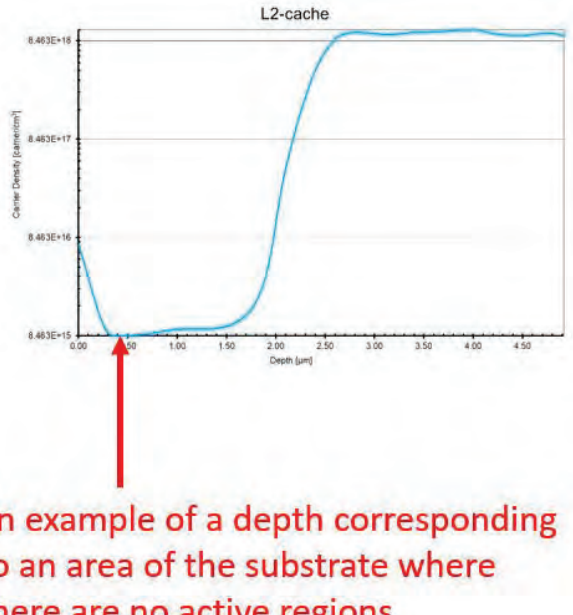
U.S. Patent No. 11,121,222	Accused Products
adjacent to the first active region and within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 5.  
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 1, Element 6; Exhibit A-2, Claim 17. The L2 cache (discussed at Exhibit A-1, Claim 1, Element 1) includes digital logic of the VLSI semiconductor device. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.

Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 2.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 6; Exhibit A-2, Claim 5; Exhibit A-2, Claim 17.
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 8.

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Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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graded dopant is fabricated with an ion implantation process.	
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 13.
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 15.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 17. The L2 cache comprises digital logic. The Intel Accused CPUs also include capacitors (e.g., super metal-insulator-metal (MIM) capacitors as shown below).

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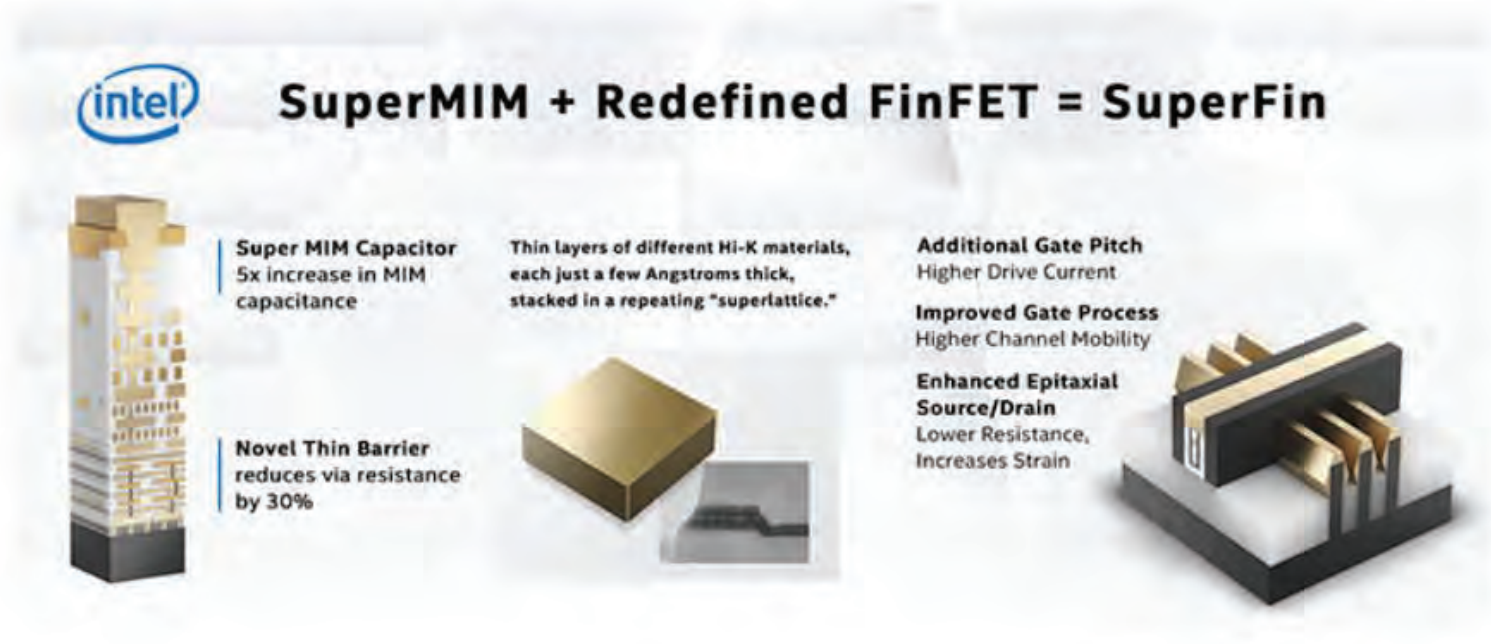
U.S. Patent No. 11,121,222	Accused Products
	
18. The VLSI semiconductor device of claim 1, wherein the device is central processing unit.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 18.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. As shown by SEM imaging (see Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1.

Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. As shown by SIMS analysis (*see* Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SIMS plot. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.

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Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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function, complementary error function, or any combination thereof.	
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 2.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 5.
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 9.

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U.S. Patent No. 11,121,222	Accused Products
region are either p-type or n-type.	
32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 8.
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 15.
35. The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 17; *see* above at Claim 17. Upon information and belief, the capacitors (e.g., super MIM capacitors discussed for claim 17) are in at least some of the first or second active regions, because capacitors are commonly formed in active regions of semiconductor devices.
36. The VLSI semiconductor device of claim 21, wherein the device is central processing unit.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 18.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 20.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device. *See* above at Claim 1, Preamble; Exhibit A-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 2; *see also* Exhibit A-1, Claim 1, Element 2.

Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 6; Exhibit A-1, Claims 6, 14.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device. *See* above at Claim 39, Preamble.

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Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 5. SIMS analysis (*see* Exhibit A-1, Claim 1, Element 1) reveals at least one graded dopant acceptor concentration (e.g., concentration of boron-11) as claimed.

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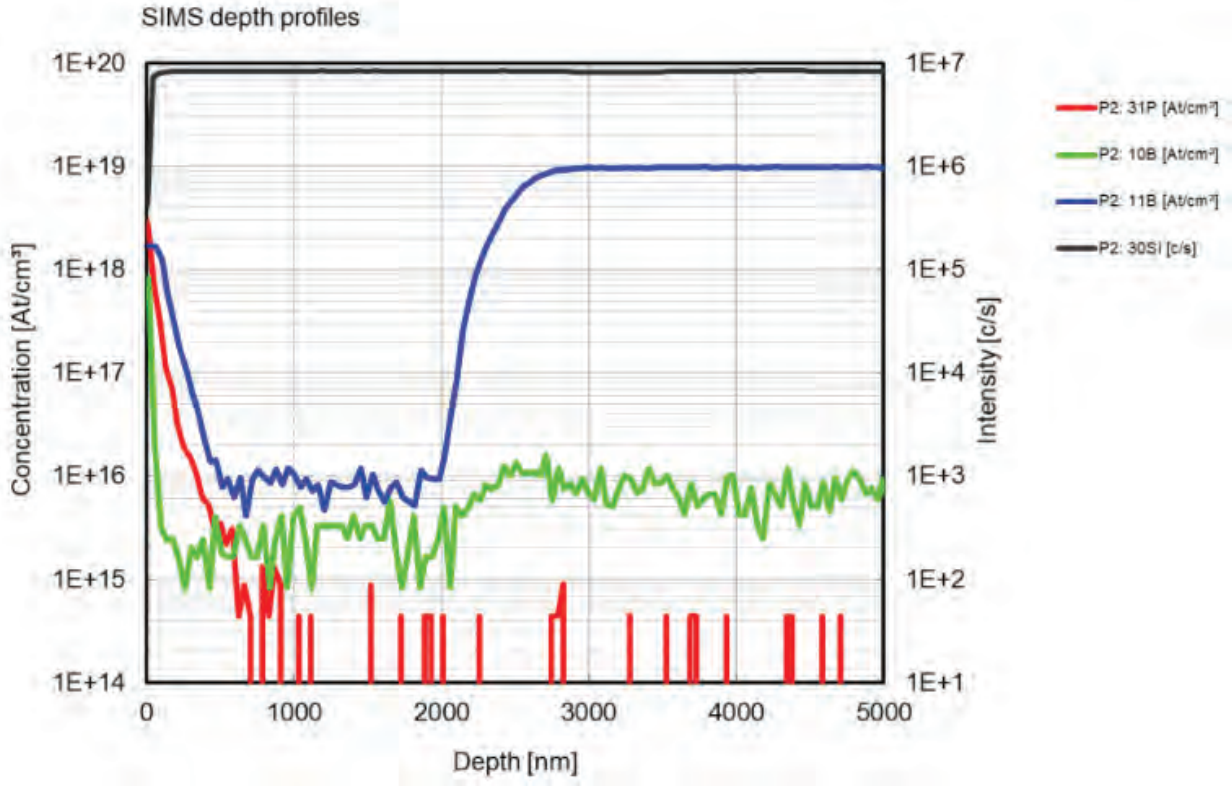
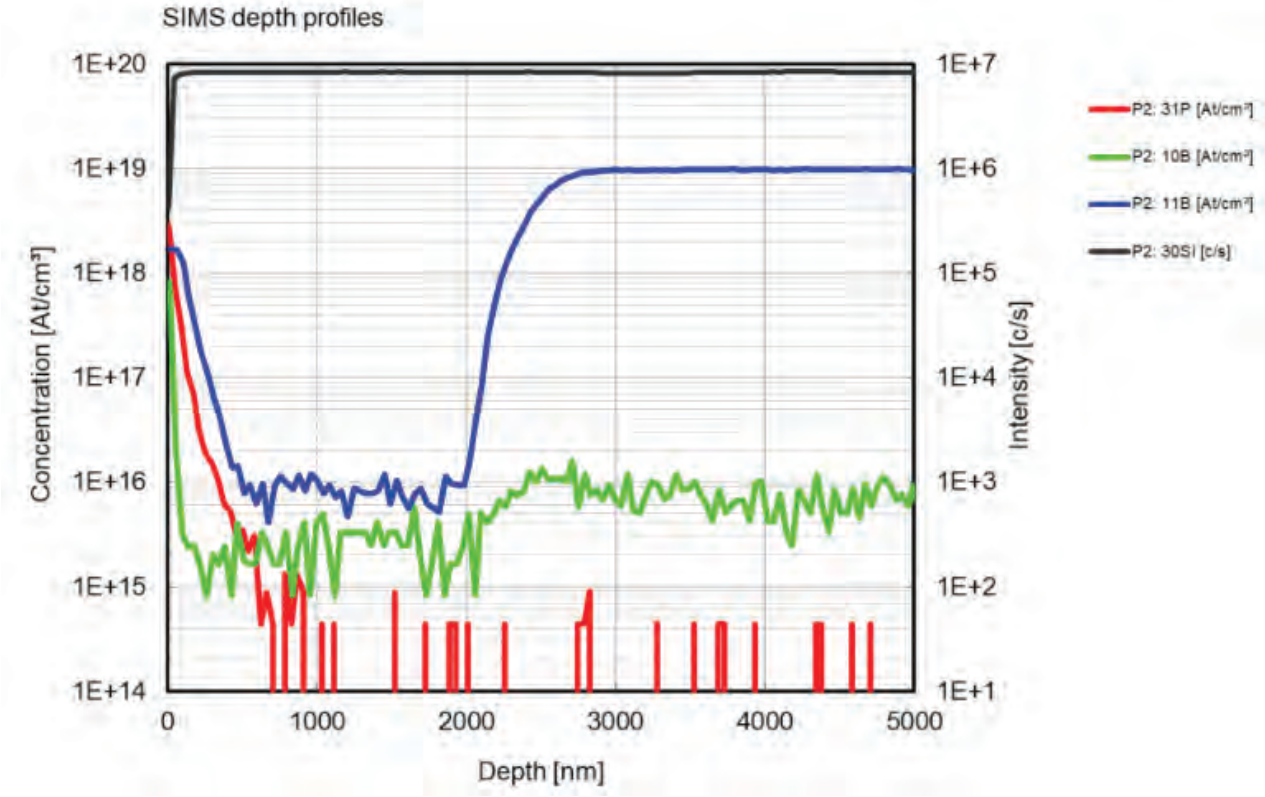
U.S. Patent No. 11,121,222	Accused Products
	 *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 39, Element 2.

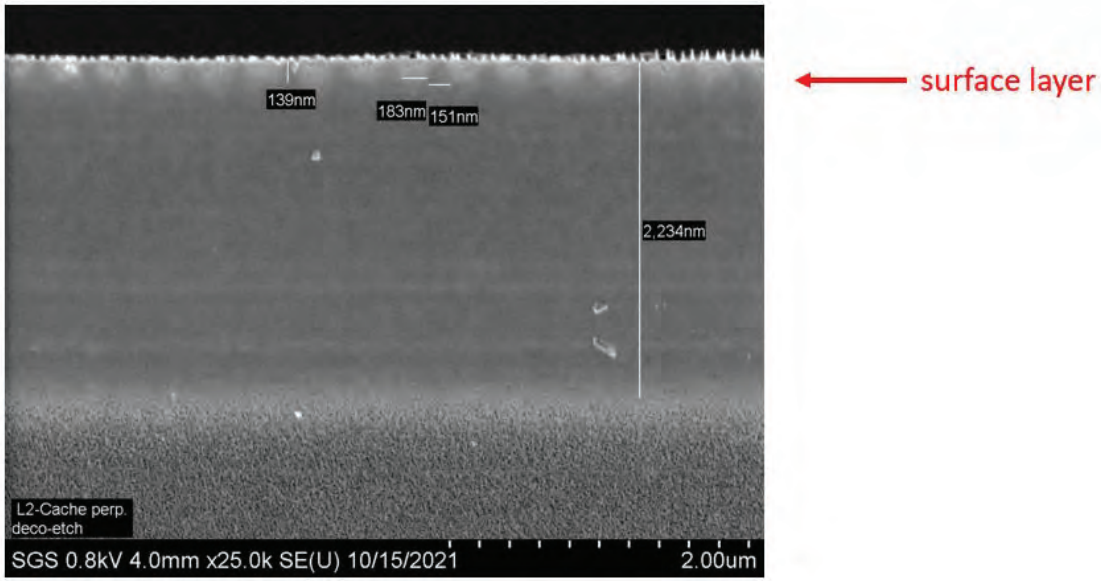
Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 39, Element 5. SIMS analysis (*see* Exhibit A-1, Claim 1, Element 1) reveals at least one graded donor dopant concentration (e.g., concentration of phosphorus-31) as claimed.

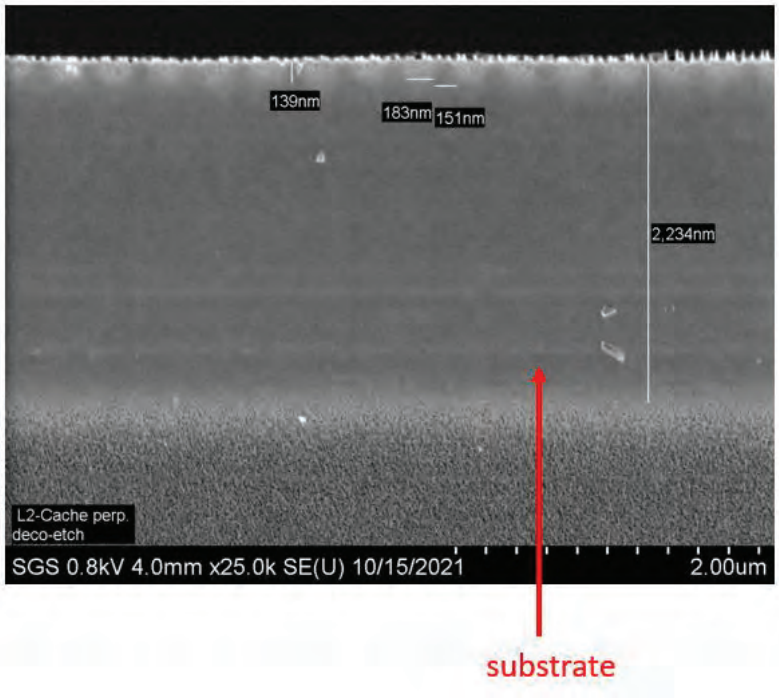
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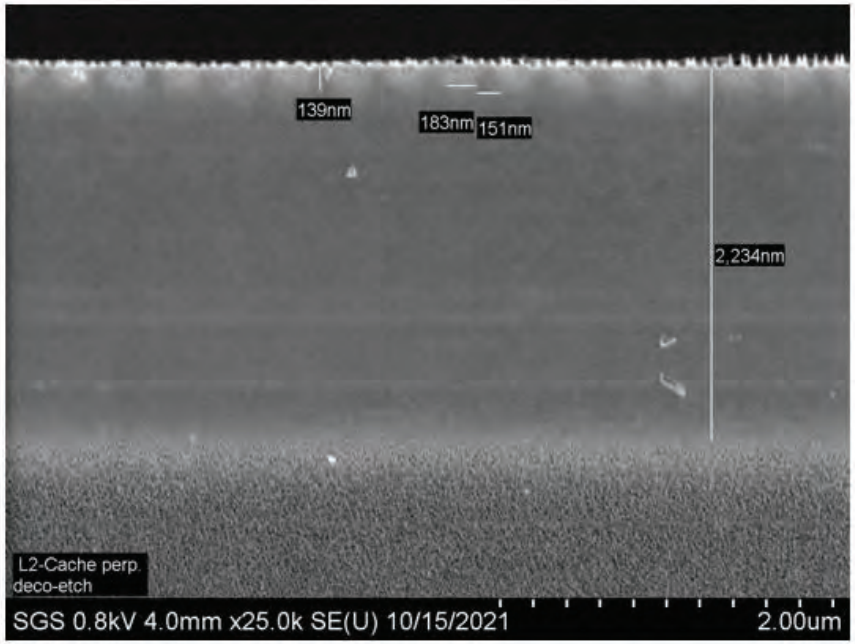
Exhibit A-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
	 *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Accused Products include a CMOS semiconductor device. *See* above at Claim 15; Claim 39, Preamble.
[Claim 44, Element 1]: a surface layer;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 1; *see also* above at Claim 1, Element 1.

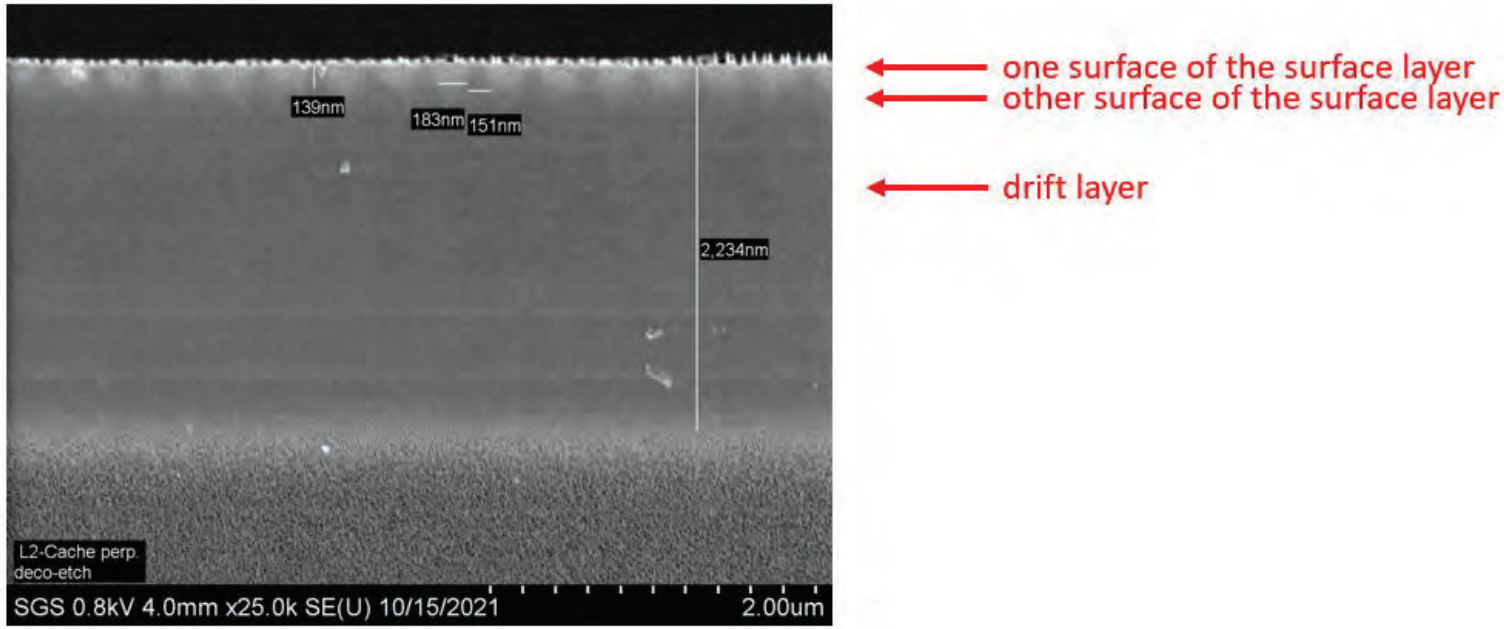
U.S. Patent No. 11,121,222	Accused Products
	
[Claim 44, Element 2] a substrate;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See above* at Claim 44, Element 1.

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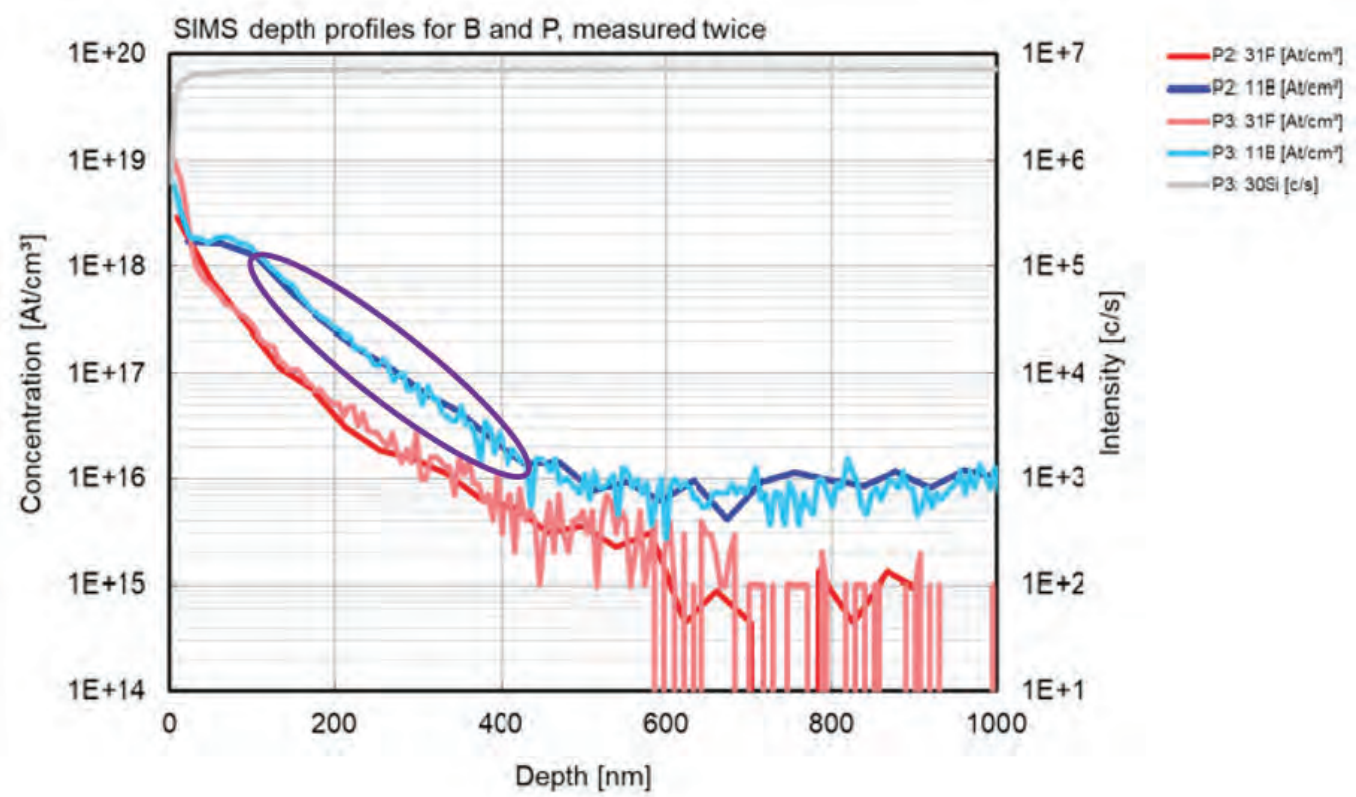
U.S. Patent No. 11,121,222	Accused Products
	
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Element 2 (discussion of active region); Exhibit A-1, Claim 18 (discussion of source and drain).

U.S. Patent No. 11,121,222	Accused Products
	 one surface of the surface layer
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 5.

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U.S. Patent No. 11,121,222	Accused Products
	 The drift layer has a graded concentration of dopants as claimed. For example, the purple oval in the below SIMS graph (*see* Exhibit A-1, Claim 1, Elements 1-2 for details regarding the SIMS analysis) shows such a graded concentration of dopants (e.g., boron-11).

U.S. Patent No. 11,121,222	Accused Products



Upon information and belief, the drift layer (*see* SEM image above) has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of Defendants and are expected to be obtained through discovery.

See also SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.

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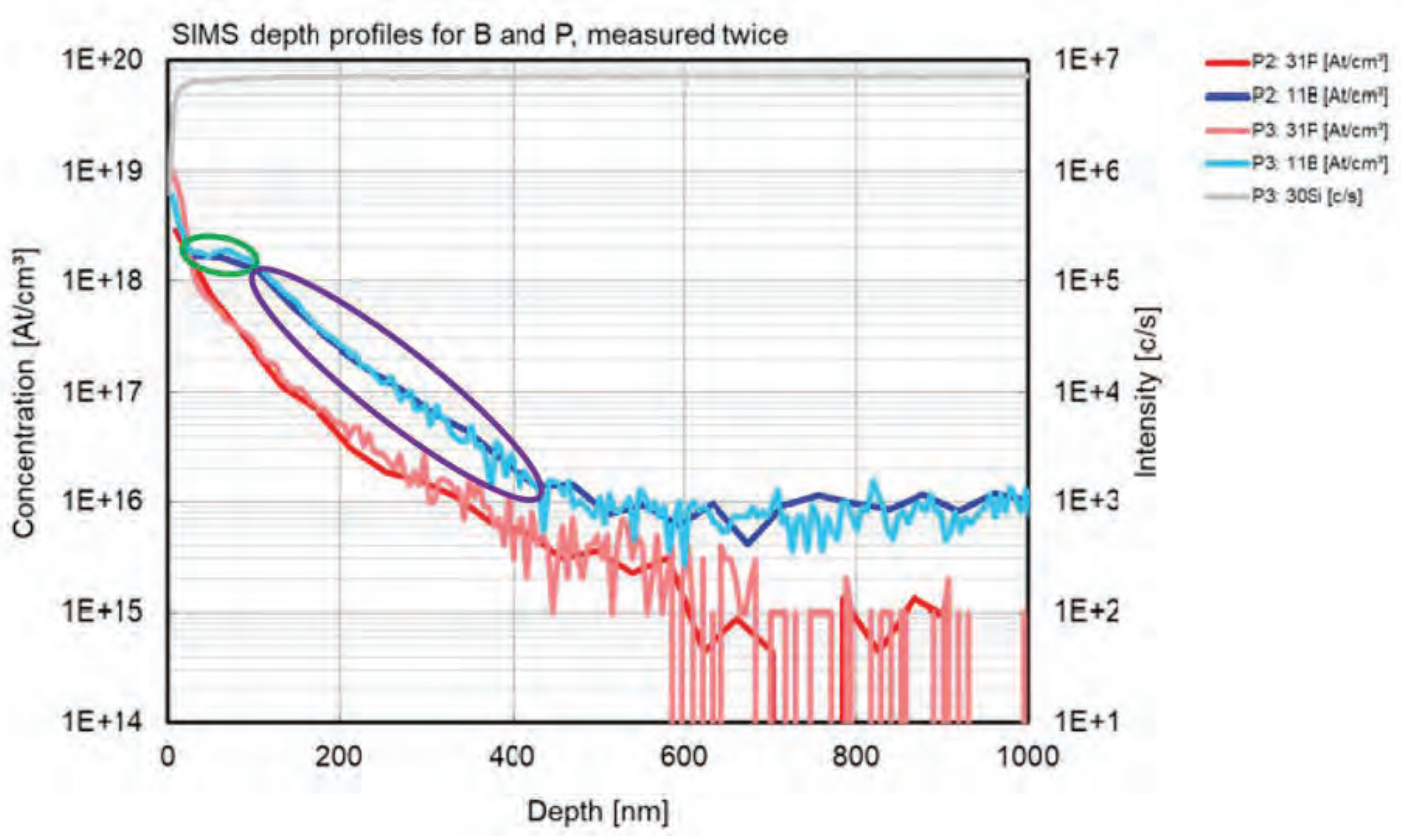
U.S. Patent No. 11,121,222	Accused Products
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 6 (explaining the presence of the well region). In the SEM image shown above for Claim 44, Element 1, the dark regions of the alternating light and dark regions at the surface layer are p-wells, upon information and belief. The p-wells have a depth of at least 139 nm, upon information and belief and based on the SEM image. This reflects one measurement in the SEM figure, but the well extends deeper, as shown by the light regions extending downward beyond 139 nm. As annotated by the green oval in the SIMS graph below (*see* Exhibit A-1, Claim 1, Elements 1-2 for details regarding the SIMS analysis), the well region has a graded concentration of dopants (e.g., boron-11), which is different than the graded concentration of dopants shown with a purple oval below.  Upon information and belief, and based on the above-discussed SEM image, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.

Exhibit A-4 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a CMOS semiconductor device. *See* Exhibit A-3, Claim 44, Preamble. This chart includes exemplary information regarding a representative example of the Dell-Intel Accused Products, Dell's Alienware M15 R6 Gaming Laptop, which includes an Intel Core i7 11800H (a representative example of the 11th Generation "Tiger Lake" Intel Accused CPUs). The Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart and the other infringement contention claim charts because it includes a processor that is among the Intel Accused CPUs. The Intel Core i7 11800H is representative of the Intel Accused CPUs for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Intel Accused CPUs would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other Intel Accused CPUs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Similarly, the other Dell-Intel Accused Products would have been designed in a similar manner as the Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart because it includes a processor that is among the to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other Intel Accused CPUs contain similar features as the Core i7 11800H, and function in a similar way with respect to the features claimed in the asserted claims, and the other Dell-Intel Accused Products contain similar features as the Alienware M15 R6 Gaming Laptop, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (*see* Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement and drift fields.

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Exhibit A-4 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 8,421,195	Accused Products
aid the movement of minority carriers from said surface layer to said substrate; and	
[Claim 1, Element 5] at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 44, Element 5. Upon information and belief, and based on the SEM image discussed regarding Claim 44, Element 5 in Exhibit A-3, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement and drift fields.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. SEM imaging (*see* Exhibit A-1, Claim 1, Element 1) shows a whitish horizontal stripe, which is an interface between epitaxy and single-crystal silicon.

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Exhibit A-4 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

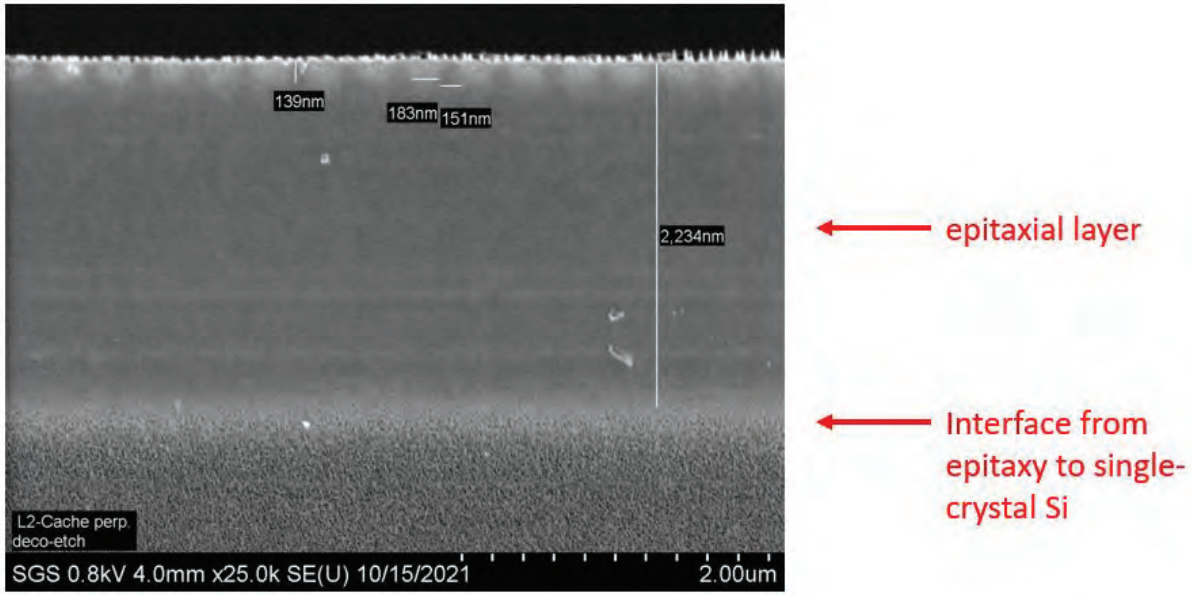
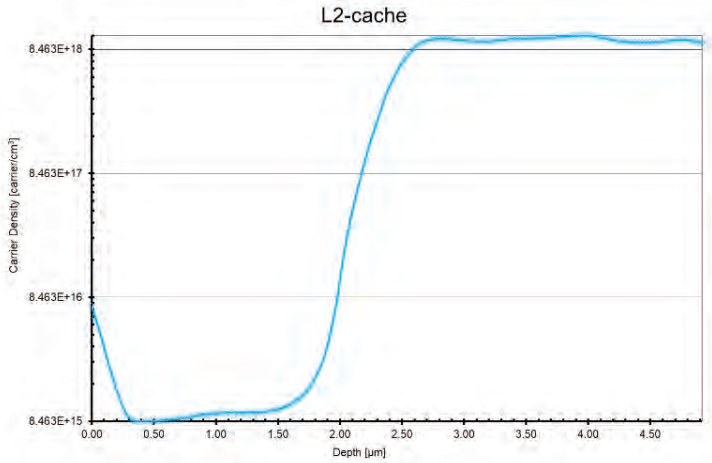
U.S. Patent No. 8,421,195	Accused Products
	
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.

Exhibit A-5 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include a semiconductor device. *See* Exhibit A-4, Claim 1, Preamble. This chart includes exemplary information regarding a representative example of the Dell-Intel Accused Products, Dell's Alienware M15 R6 Gaming Laptop, which includes an Intel Core i7 11800H (a representative example of the 11th Generation "Tiger Lake" Intel Accused CPUs). The Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart and the other infringement contention claim charts because it includes a processor that is among the Intel Accused CPUs. The Intel Core i7 11800H is representative of the Intel Accused CPUs for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Intel Accused CPUs would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, the other Intel Accused CPUs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Similarly, the other Dell-Intel Accused Products would have been designed in a similar manner as the Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart because it includes a processor that is among the to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other Intel Accused CPUs contain similar features as the Core i7 11800H, and function in a similar way with respect to the features claimed in the asserted claims, and the other Dell-Intel Accused Products contain similar features as the Alienware M15 R6 Gaming Laptop, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SIMS and SRP analysis (*see* Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement and electric fields.

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Exhibit A-5 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 9,190,502	Accused Products
carriers from said surface layer to said substrate;	
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-4, Claim 1, Element 5. *See also* SRP analysis reproduced below and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement and electric fields. 
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement and electric fields.
9. The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU).	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-2, Claim 18.

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Exhibit A-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include an electronic system. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each Intel Accused CPU (incorporated in a Dell-Intel Accused Product) is an electronic system, because a processor is an electronic system. Additionally, each Dell-Intel Accused Product is an electronic system, because a computer is an electronic system. This chart includes exemplary information regarding a representative example of the Dell-Intel Accused Products, Dell's Alienware M15 R6 Gaming Laptop, which includes an Intel Core i7 11800H (a representative example of the 11th Generation "Tiger Lake" Intel Accused CPUs). The Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart and the other infringement contention claim charts because it includes a processor that is among the Intel Accused CPUs. The Intel Core i7 11800H is representative of the Intel Accused CPUs for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Intel Accused CPUs would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, the other Intel Accused CPUs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Similarly, the other Dell-Intel Accused Products would have been designed in a similar manner as the Alienware M15 R6 Gaming Laptop is representative of the Dell-Intel Accused Products for purposes of this claim chart because it includes a processor that is among the to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other Intel Accused CPUs contain similar features as the Core i7 11800H, and function in a similar way with respect to the features claimed in the asserted claims, and the other Dell-Intel Accused Products contain similar features as the Alienware M15 R6 Gaming Laptop, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 1, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 1, Element 3.

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U.S. Patent No. 11,316,014	Accused Products
the first active region and within which transistors can be formed;	
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 1, Element 4.
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 1, Element 5. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 1, Element 6. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 2.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 4.

Exhibit A-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 5.
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 15.

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Exhibit A-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 17.
18. The system of Claim 1, wherein the at least one semiconductor device is a central processing unit.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 18.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1e.

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U.S. Patent No. 11,316,014	Accused Products
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. *See also* SRP analysis reproduced and discussed at Exhibit A-1, Claim 1, Element 5 showing carrier movement.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 26.

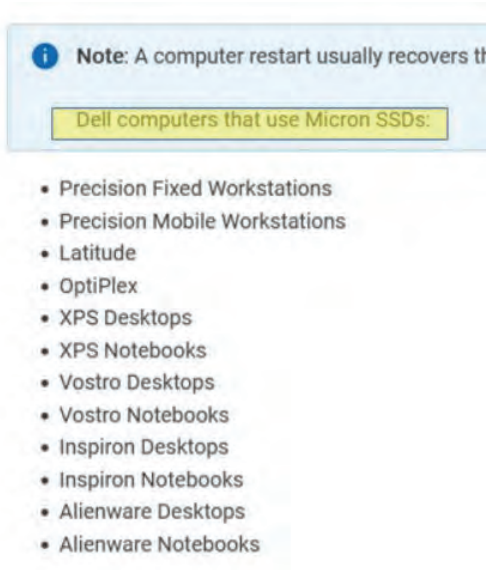
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Exhibit A-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Intel Accused CPUs, and Dell-Intel Accused Products incorporating them, meet this limitation. *See* Exhibit A-3, Claim 28.

Exhibits B-1 to B-6
Dell-Micron Flash Memory Products

Exhibit B-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. For example, upon information and belief, the Dell-Micron-Flash Accused Products include a Micron solid-state drive (SSD), which includes a flash memory device, which is a semiconductor device. Usage of a Micron SSD in Dell products is shown below, for example:  **Micron PCIe NVMe 2200S SSD Intermittently sees Blue Screen and Hard Drive Not Detected Errors** Several different families of Dell computer are experiencing an issue with Micron PCIe NVMe 2200S SSDs. *See* https://www.dell.com/support/kbdoc/en-nz/000126687/micron-2200s-pcie-nvme-ssds-exhibit-intermittent-bsod-and-drive-detection-errors **What is a flash solid-state drive (SSD)?** A flash solid-state drive (SSD) is a non-volatile storage device that stores persistent data in flash memory. There are two types of flash memory used in SSDs -- NAND and NOR. *See* https://www.techtarget.com/searchstorage/definition/flash-based-solid-state-drive-SSD

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U.S. Patent No. 10,510,842	Accused Products
	Solid state refers to electronic circuitry that is built entirely of semiconductors. The term was originally used to define those electronics, such as a transistor radio that used semiconductors rather than vacuum tubes in its construction. Most electronics today are built around semiconductors and chips. A solid state drive uses, as its primary storage medium, semiconductors rather than the magnetic platters of a conventional hard drive. *See* https://www.lifewire.com/solid-state-drive-833448 A Micron 16 nm node NAND flash memory has been analyzed via tear-down, as explained below. The Micron flash memory is discussed in this claim chart and other infringement contention claim charts (e.g., Exhibits B-2 through B-6) as an example of a Micron flash memory used in Dell-Micron-Flash Accused products. Upon information and belief, such a Micron flash memory is representative of Micron flash memory devices used in the Dell-Micron-Flash Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other Micron flash memory devices used in Dell-Micron-Flash Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, other Micron flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Therefore, upon information and belief, other Micron flash memory devices used in Dell-Micron-Flash Accused Products contain similar features as the Micron 16 nm node NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Micron-Flash Accused Products include a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, a die of the Micron flash memory discussed above for the preamble is shown below:

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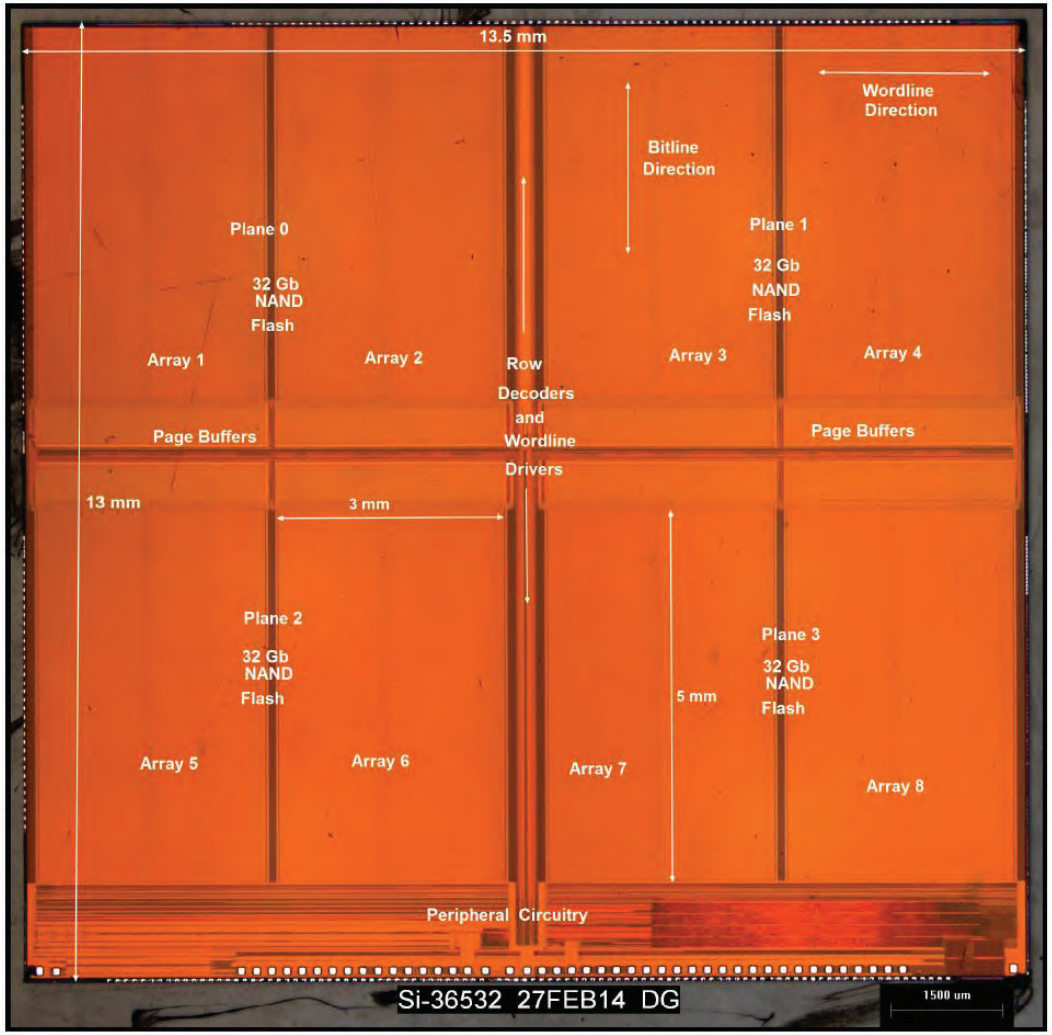
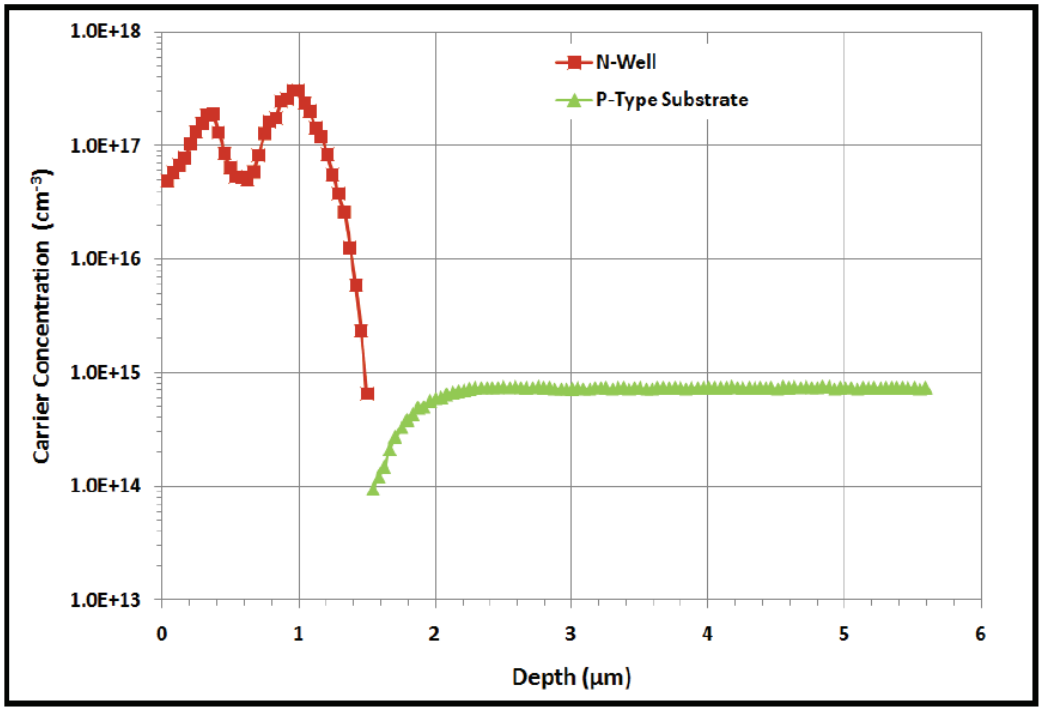


Figure 1.1.1: Die photograph (optical), 16 nm MLC NAND flash memory of IMFT

The following image of a cross-section of the flash memory die, obtained through scanning electron microscopy (SEM), shows the die having a thickness of 171 µm in this example. The flash memory die includes a substrate having first and second surfaces, as shown below:

U.S. Patent No. 10,510,842	Accused Products
	 Figure 1.1.7: Die Thickness (SEM Cross-section), 16 nm MLC NAND flash memory of IMFT A thickness (depth) of, e.g., 171 µm is consistent with the presence of a substrate. Spreading resistance profile (SRP) analysis conducted on the flash memory shows that the substrate is p-type (a first doping type) and has a first doping level (*see* concentration of p-type substrate in below graph).

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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-Flash Accused Products include a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, the following cross-sectional image (labeled Figure 2.3.15) of the Micron flash memory device discussed above, obtained through scanning electron microscopy (SEM), shows a first active region as claimed:

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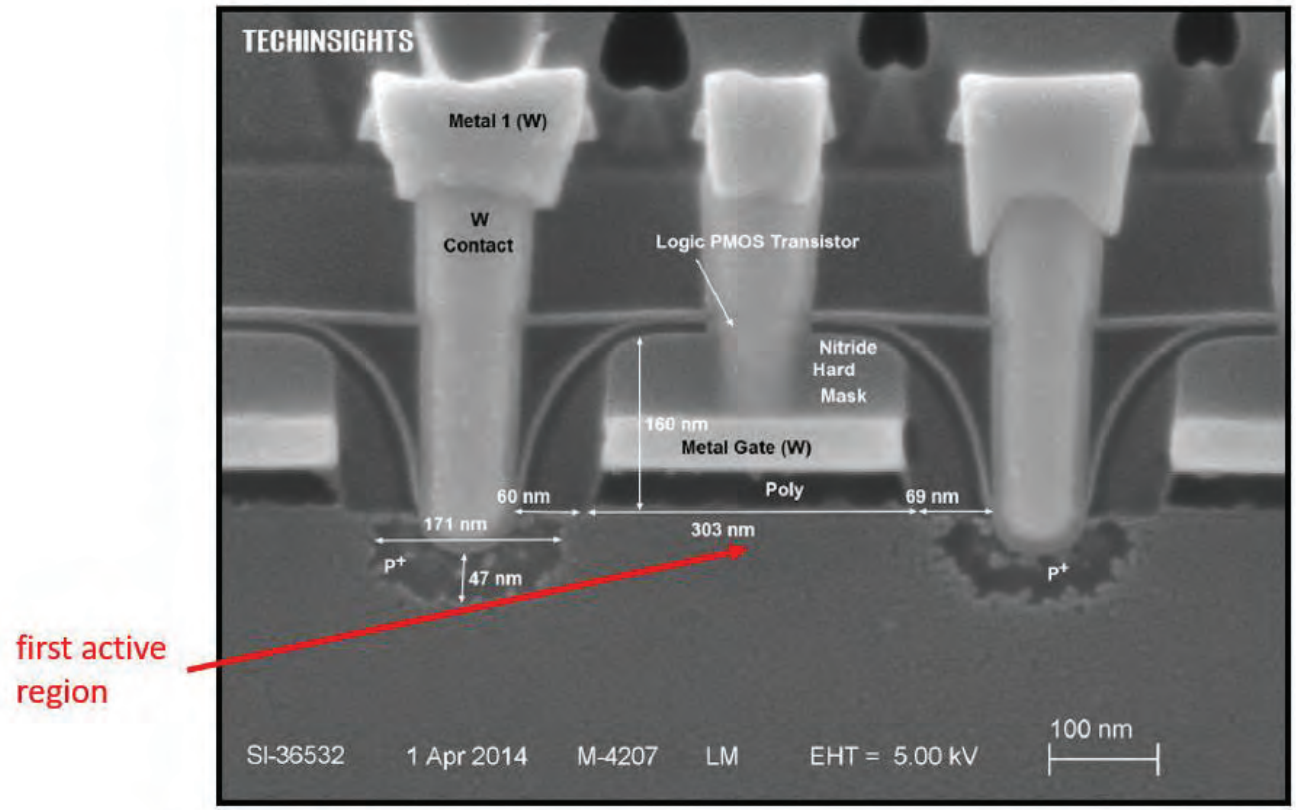
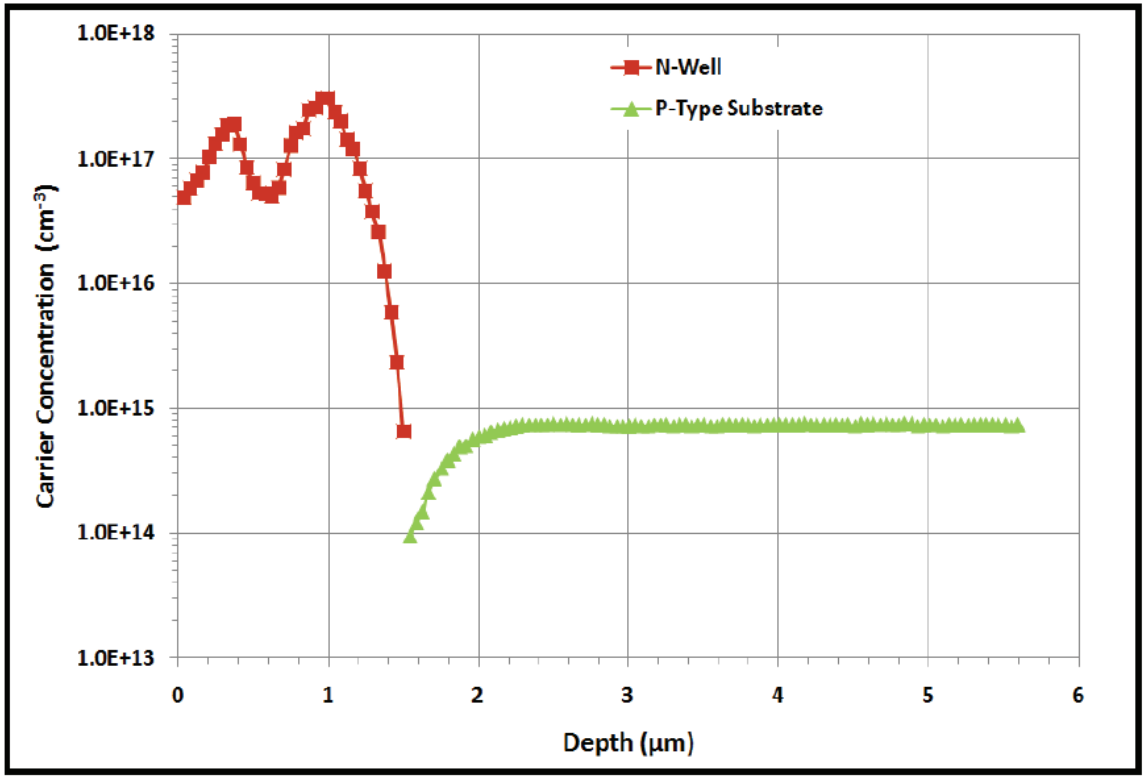


Figure 2.3.15: Peripheral PMOS logic transistors with Si-etch, 16 nm MLC NAND flash memory of IMFT

A transistor (labeled "Logic PMOS Transistor" in the above image) is shown above the first active region, and thus the first active region is a region within which transistors can be formed. For example, the gate of such a transistor is labeled in the above image. As shown in the above image, the first active region is disposed adjacent the first surface of the substrate.

The first active region has a second doping type (e.g., n-type) opposite in conductivity to the first doping type (p-type), e.g., as PMOS transistors are formed in n-wells. The presence of P^+ diffusion regions to the left and right of the first active region is consistent with the presence of the PMOS transistor. The n-type doping of the n-well is also shown in the following SRP graph.

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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT The n-well shown above contains the first active region which is n-type.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-Flash Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, a second active region as claimed is shown in the below SEM image (labeled Figure 2.3.14):

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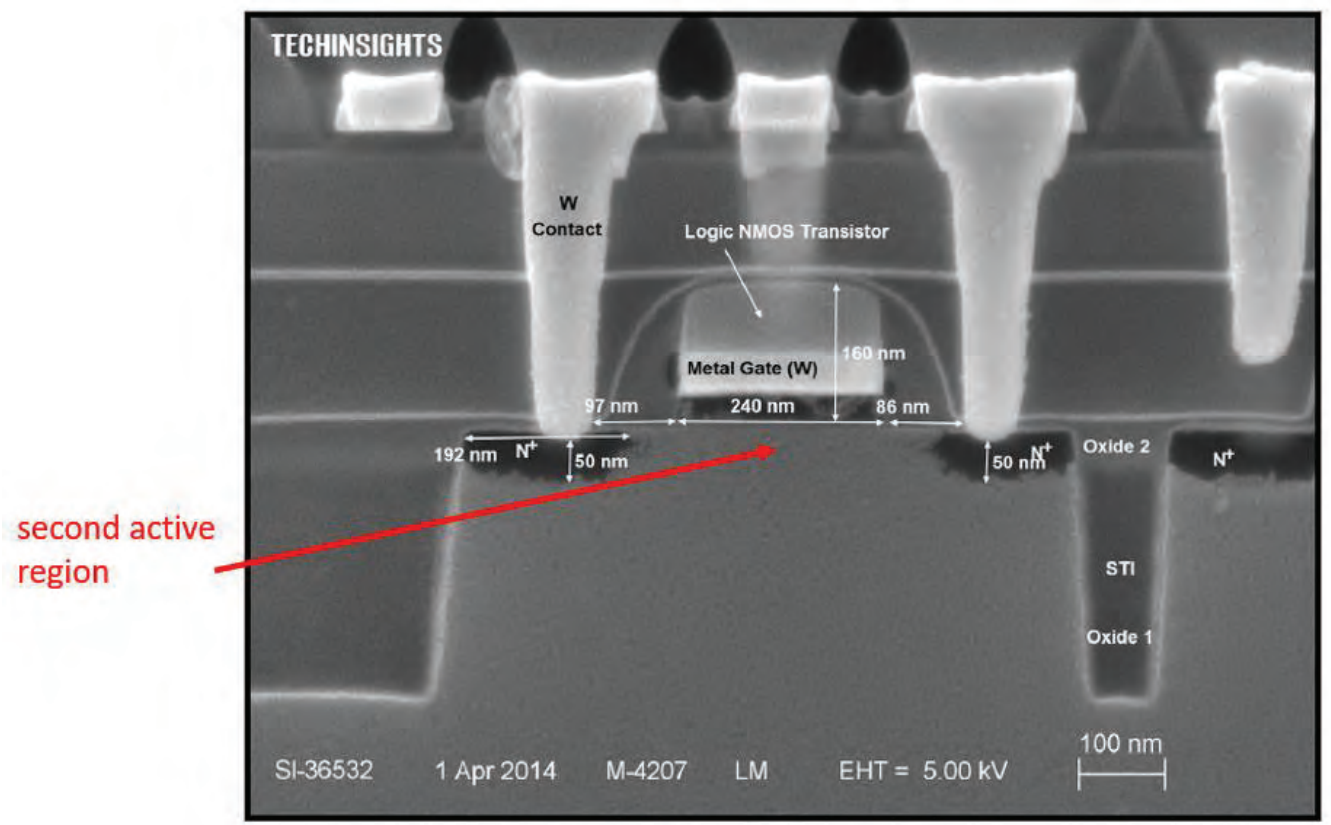
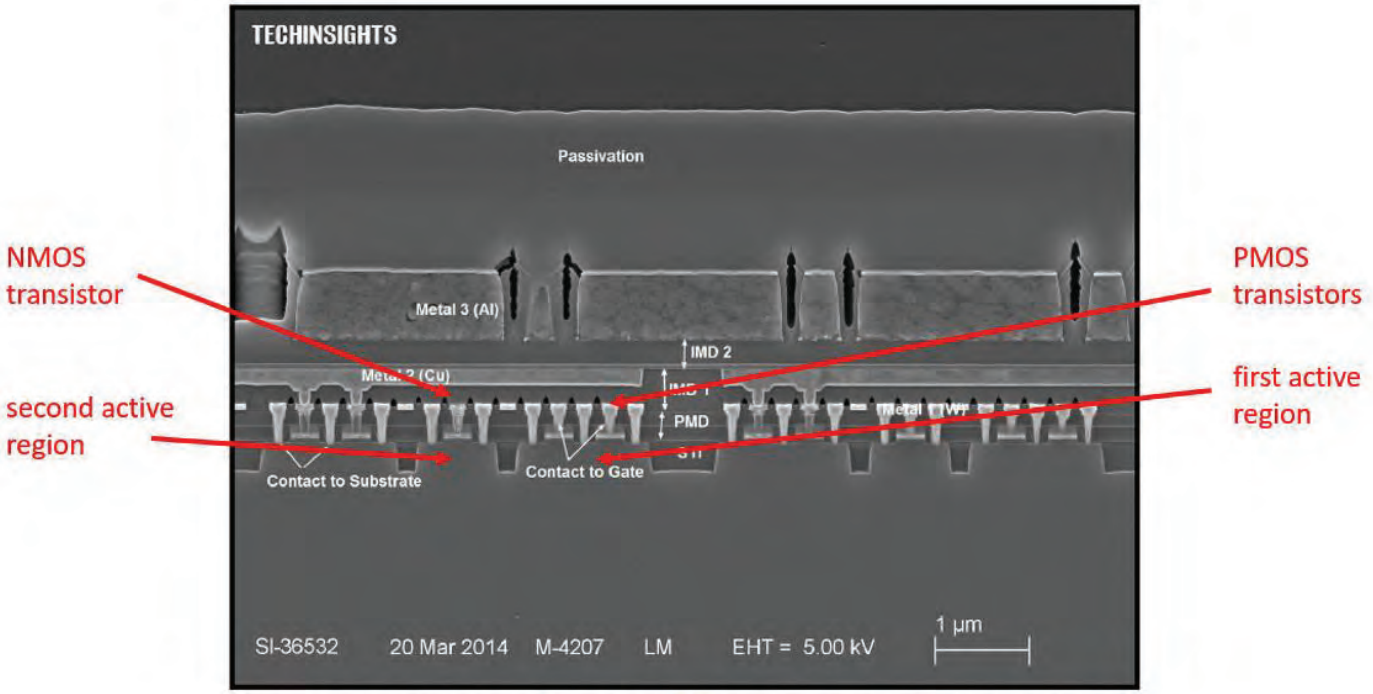
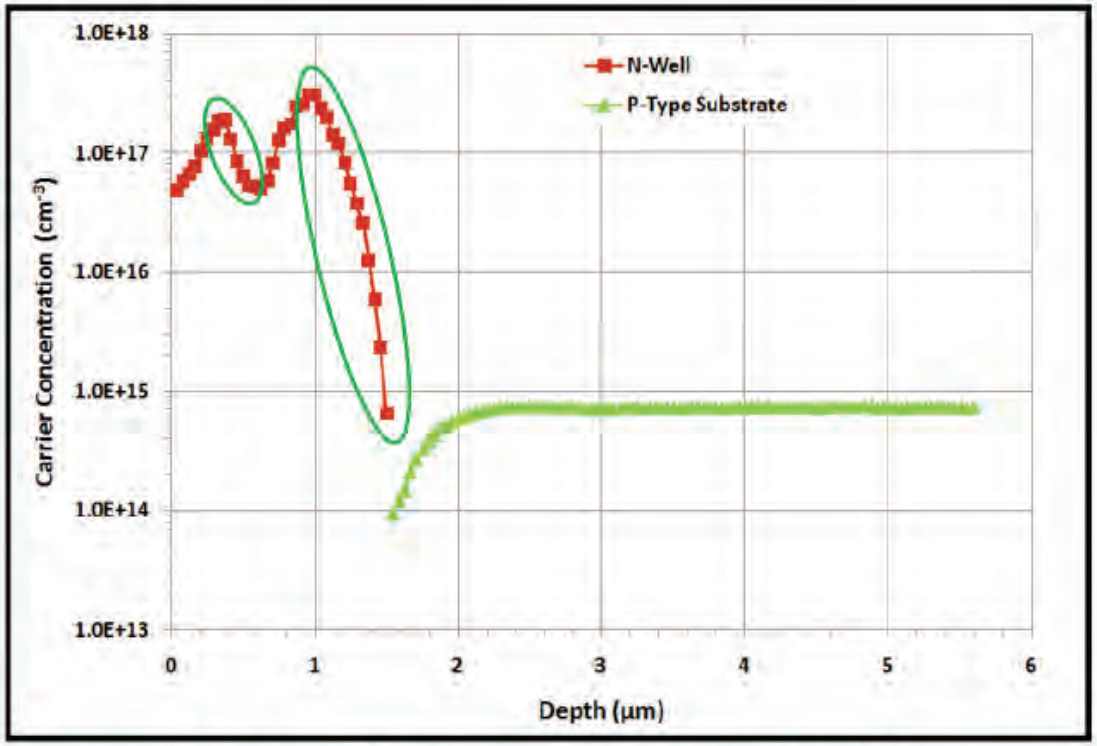
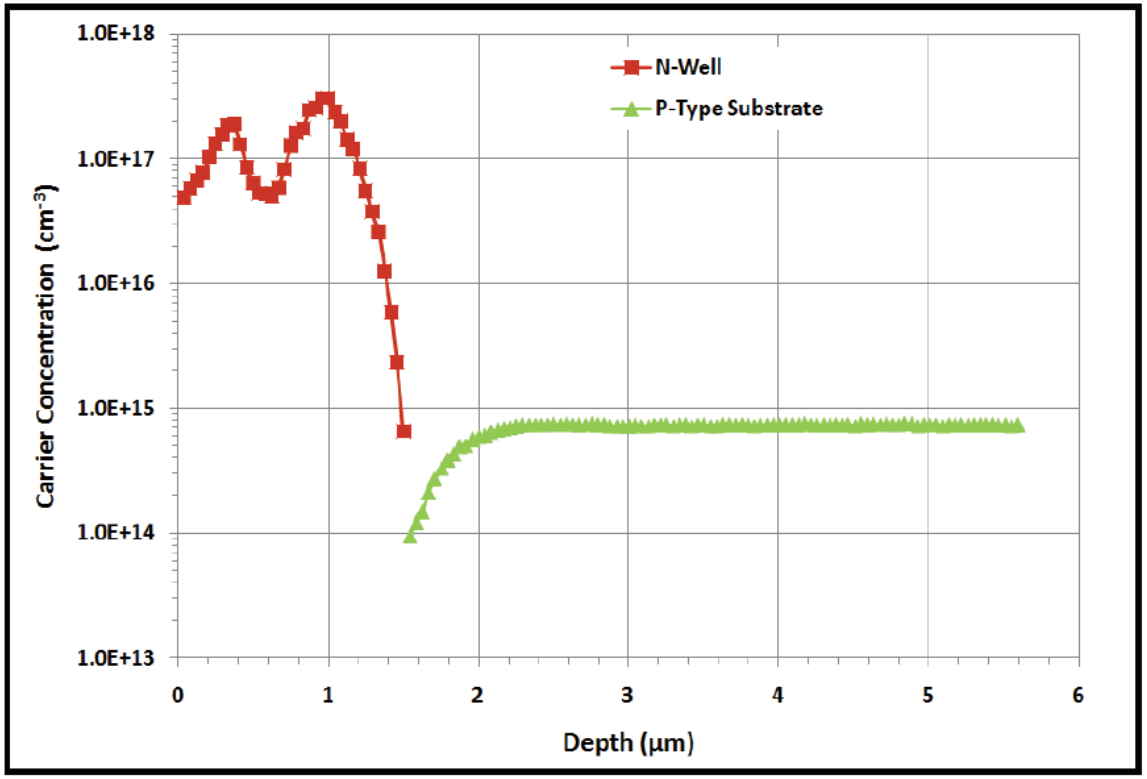


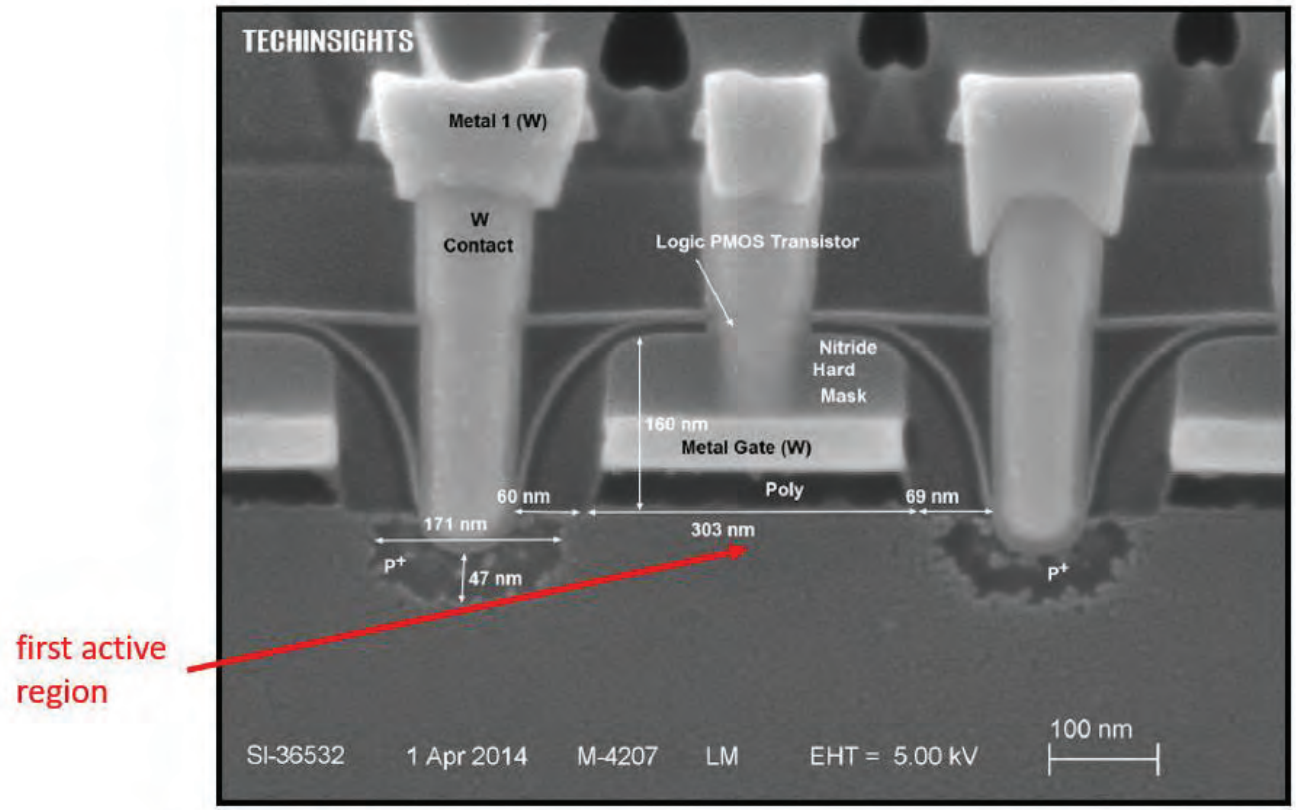
Figure 2.3.14: Peripheral NMOS logic transistors with Si-etch, 16 nm MLC NAND flash memory of IMFT

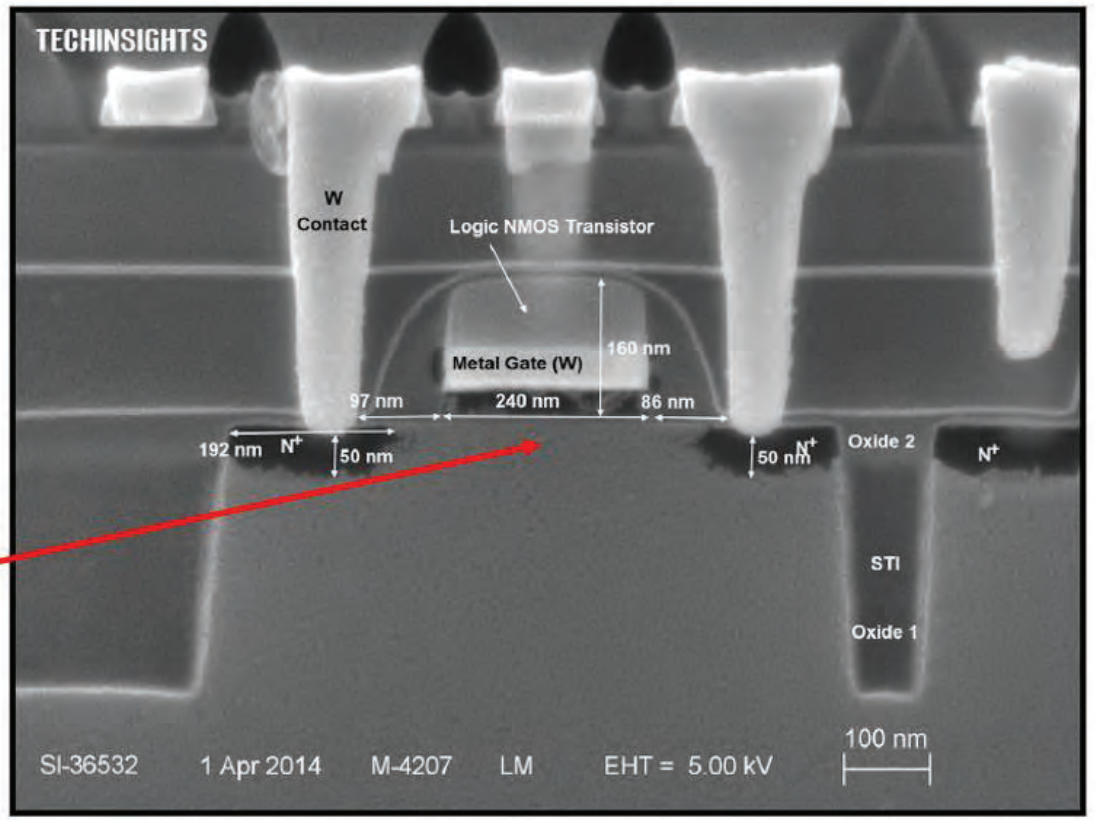
A transistor (labeled "Logic NMOS Transistor" in the above image) is shown above the second active region, and thus the second active region is a region within which transistors can be formed. For example, the gate of such a transistor is labeled in the above image.

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	 Figure 2.3.1: Peripheral logic transistor overview, (SEM cross-section), 16 nm MLC NAND flash memory of IMFT As shown in the above SEM image (labeled Figure 2.3.1), the second active region (which is shown below an NMOS transistor) is separate from the first active region (which is shown below PMOS transistors) and is disposed adjacent to the first active region.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-Flash Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at Elements 2-3.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-Micron-Flash Accused Products include a semiconductor device comprising at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate. For example, the graph below, obtained via SRP analysis, electrically characterizes the Dell-Micron-Flash Accused Products shows a graded dopant concentration (annotated with green ovals) in the first active region (e.g., as shown by the concentration corresponding to an n-well) to aid carrier movement from the first surface to the second surface of the substrate (e.g., downwards, corresponding to increasing depth, in the below graph). SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

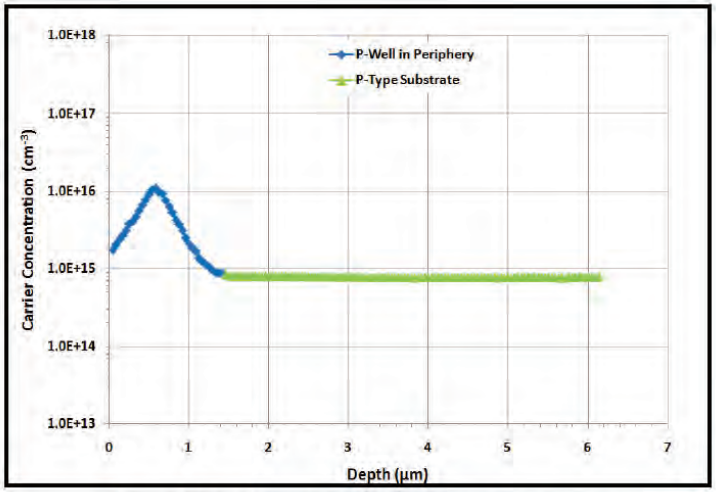
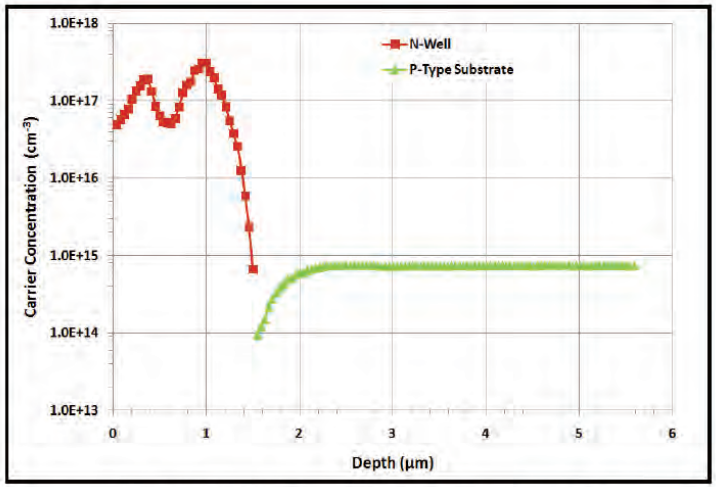
U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The substrate of the semiconductor device of the Dell-Micron-Flash Accused Products is a p-type substrate, as discussed above for Claim 1, Element 1.
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The substrate of the semiconductor device of the Dell-Micron-Flash Accused Products incorporating Micron SSDs has epitaxial silicon on top of a nonepitaxial substrate. Upon information and belief, the substrate used in the Dell-Micron-Flash Accused Products is a single-crystal silicon wafer. Additionally, SRP analysis shows a curve downwards in the below green (corresponding to substrate) plot (from 2 µm towards shallower depths) indicative of a purer layer grown on the substrate, and this is likely implemented via epitaxy.

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	 Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT
5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Dell-Micron-Flash Accused Products meet this limitation. For example, in the following SEM image, the first and second active regions correspond to PMOS and NMOS transistors, respectively, e.g., as shown in the following SEM images (labeled Figures 2.3.15 and 2.3.14, respectively; *see also* above at Claim 1, Elements 2-3) by the P+ diffusion regions on either side of the first active region and the N+ diffusion regions on either side of the second active region.

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	 Figure 2.3.15: Peripheral PMOS logic transistors with Si-etch, 16 nm MLC NAND flash memory of IMFT

U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.3.14: Peripheral NMOS logic transistors with Si-etch, 16 nm MLC NAND flash memory of IMFT Thus, the first active region and second active region contain one of either p-channel and n-channel devices (e.g., the first active region contains a p-channel device, and the second active region contains an n-channel device).
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Dell-Micron-Flash Accused Products meet this limitation. As discussed above for Claim 5, the periphery (region with peripheral NMOS and PMOS transistors shown in Figures 2.3.14 and 2.3.15) contains NMOS (n-channel) and PMOS (p-channel) devices in respective p-wells and n-wells. As discussed above for Claim 1, Elements 2-3 and Claim 5, the p-channel and n-channel devices are contained in the first and active regions (*see* annotated Figures 2.3.14 and 2.3.15 discussed above). The following graphs obtained via SRP analysis show a p-well having a graded dopant (e.g., depths of about 0.6-1.2 µm in first graph below) and an n-well having a graded dopant (e.g., depths of about 1-1.5 µm in second graph below).

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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.3: SRP analysis in the periphery, showing the peripheral P-well of 16 nm MLC NAND flash of IMFT  Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT The first and second active regions contain either p-channel or n-channel devices in these n-wells/p-wells because in CMOS technology a p-channel device is formed in an n-well and an n-channel device is formed in a p-well.
7. The semiconductor device of	The Dell-Micron-Flash Accused Products meet this limitation. The following SEM cross-sectional image shows that the first active

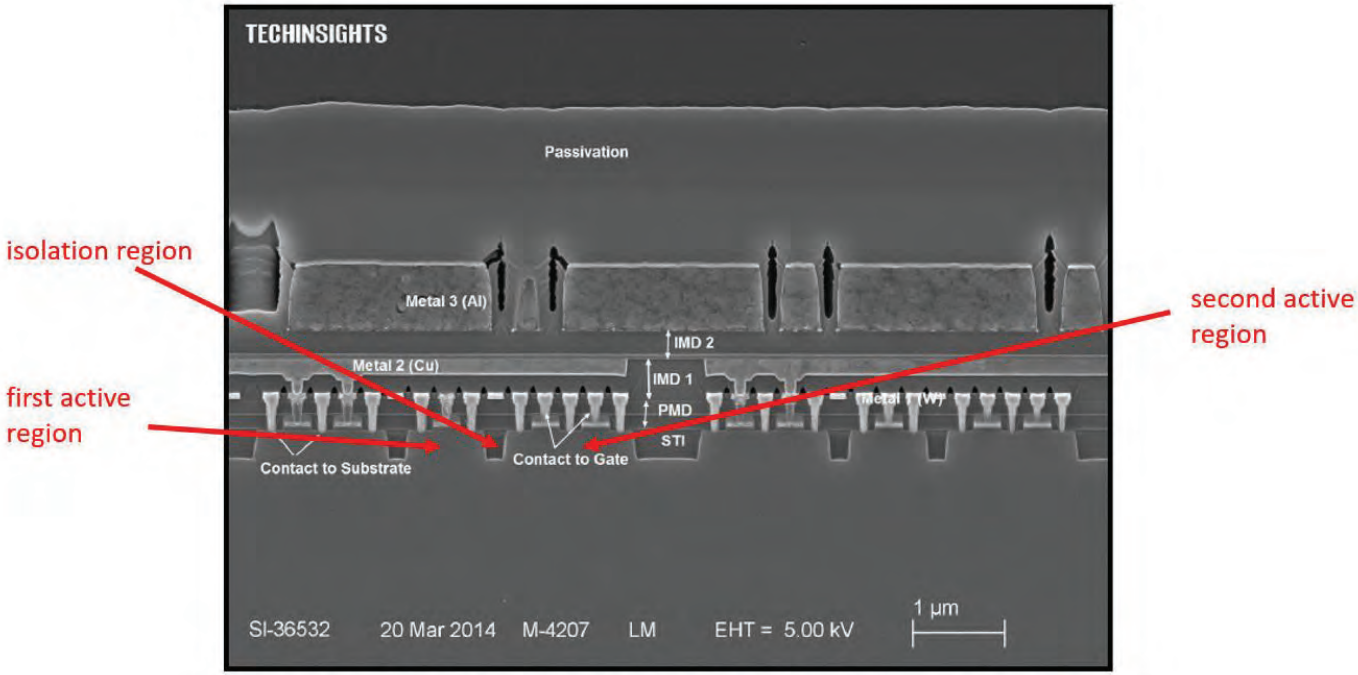
U.S. Patent No. 10,510,842	Accused Products
claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	region and second active region are each separated by at least one isolation region, which is a shallow-trench isolation as indicated by the label STI at another such isolation region shown in the image.  Figure 2.3.1: Peripheral logic transistor overview, (SEM cross-section), 16 nm MLC NAND flash memory of IMFT
8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, for the Dell-Micron-Flash Accused Products, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Dell-Micron-Flash Accused Products. Information about the fabrication process for Dell-Micron-Flash Accused Products, including usage of an ion implantation process, is in the possession of the Defendants and is expected to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1.

Exhibit B-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of the Defendants and are expected to be obtained through discovery.
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of the Defendants and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 5.
10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 2.
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 5.

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U.S. Patent No. 10,510,842	Accused Products
channel and n-channel devices.	
14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 6.
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3. The SEM images labeled Figures 2.3.15 and 2.3.14 discussed above for Claim 1, Elements 2-3 show PMOS and NMOS transistors, which are adjacent to one another as shown in the SEM image labeled Figure 2.3.1 discussed above for Claim 1, Element 3. Therefore, the transistors which can be formed in the first and second active regions are CMOS transistors. CMOS transistors require a source, a drain, a gate, and a channel region. The source and drain terminals of transistors are shown below, a gate is between each source-drain pair, and a channel region connects each source to a corresponding drain.

Exhibit B-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

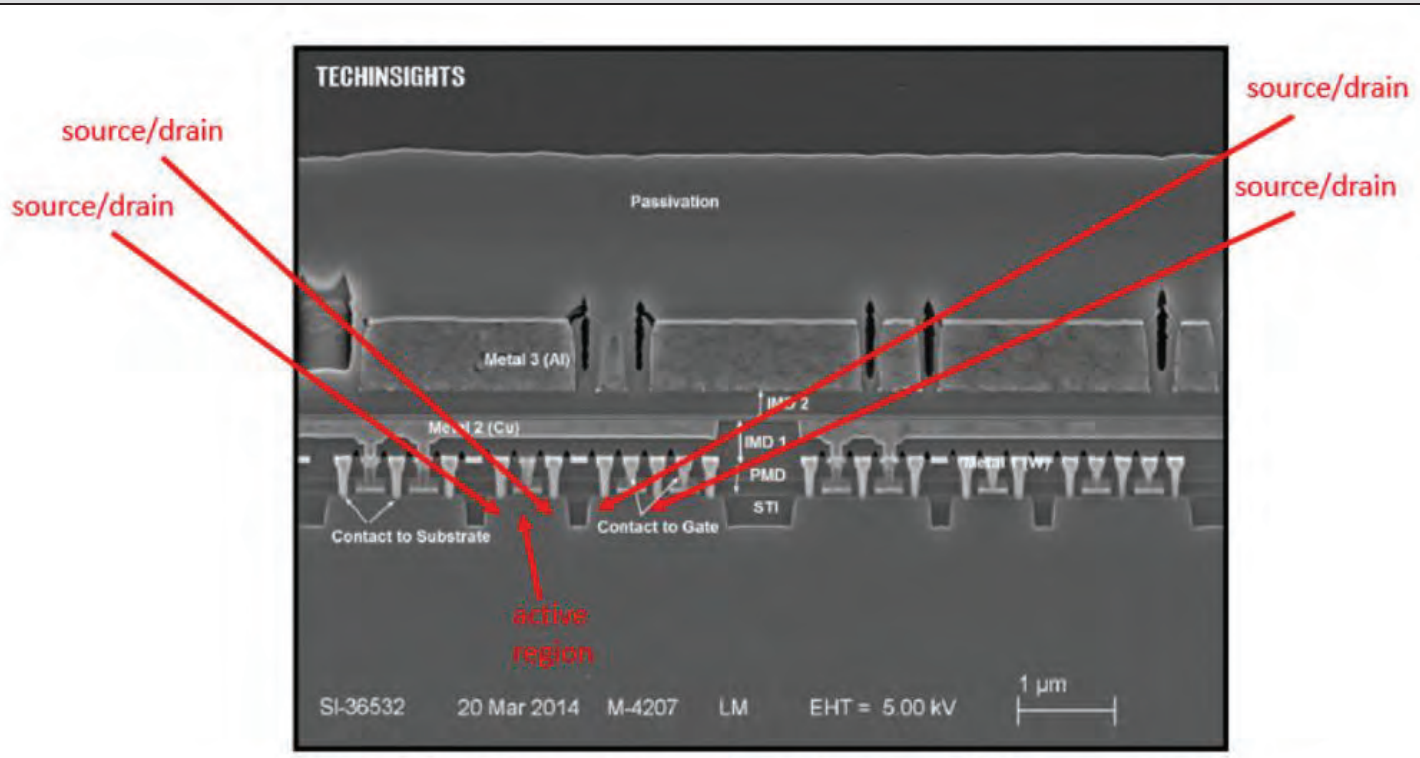
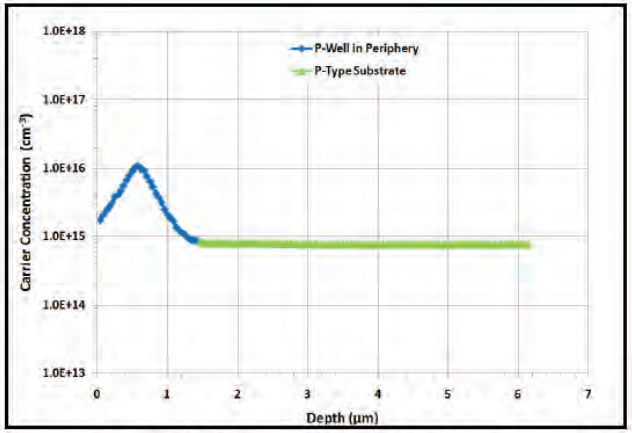
U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.3.1: Peripheral logic transistor overview, (SEM cross-section), 16 nm MLC NAND flash memory of IMFT

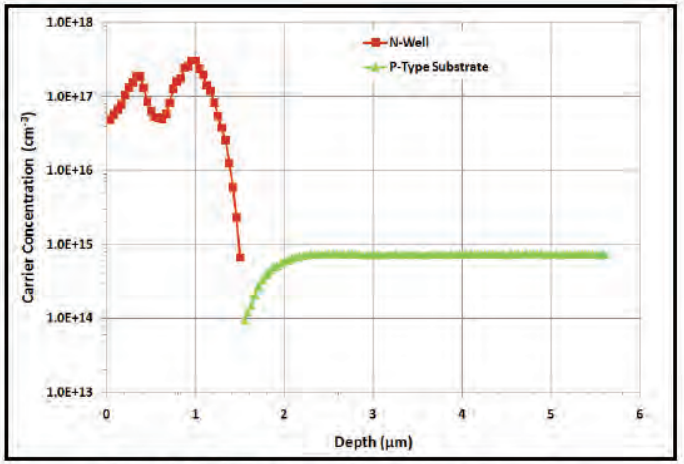
Exhibit B-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. *See* Exhibit B-1, Claim 1, Preamble. The Micron flash memory referenced in Exhibit B-1 is discussed in this claim chart and other infringement contention claim charts as an example of Dell-Micron-Flash Accused Products. Upon information and belief, such a Micron flash memory is representative of Micron flash memory devices used in the Dell-Micron-Flash Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other Micron memory devices used in Dell-Micron-Flash Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, other Micron flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Therefore, upon information and belief, other Micron flash memory devices used in Dell-Micron-Flash Accused Products contain similar features as the Micron 16 nm node NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 4.

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U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-Micron-Flash Accused Products meet this limitation. For example, the Micron flash memory includes a p-well (first graph below) and an n-well (second graph below) having graded dopant regions.  Figure 2.1.3: SRP analysis in the periphery, showing the peripheral P-well of 16 nm MLC NAND flash of IMFT

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U.S. Patent No. 10,734,481	Accused Products
	 Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT These graded dopant regions are to aid carrier movement from the first surface to the second surface of the substrate. *See* Exhibit B-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 2.
3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 4.
4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 5.
5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 6.

U.S. Patent No. 10,734,481	Accused Products
wells, respectively, and each well has at least one graded dopant.	
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 7.
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 8.
8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Elements 1-3.
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 5 (SRP analysis of Figure 2.1.4 (below) showing n-type doping at graded dopant concentration).

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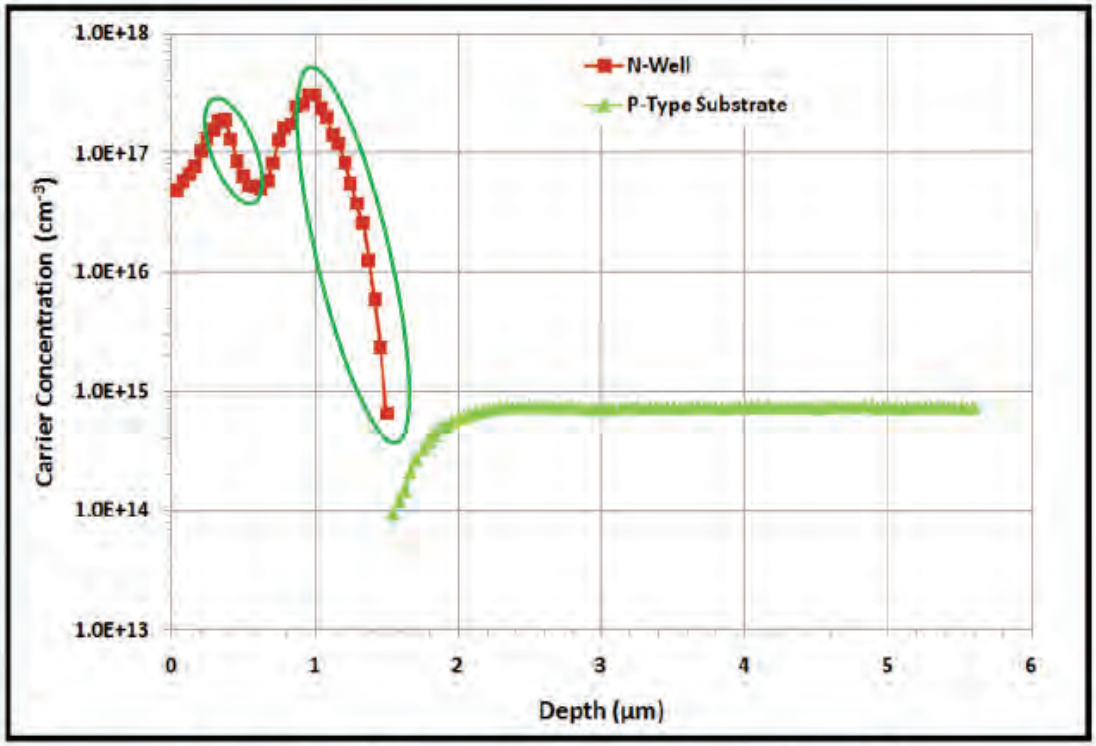
U.S. Patent No. 10,734,481	Accused Products
	 Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT
13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 18.
15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claims 4 (regarding nonepitaxial substrate), 18 (regarding CMOS).

Exhibit B-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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16. The semiconductor device of claim 1, wherein the device is a flash memory.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Preamble.
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 9, Element 2.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 9, Element 3.
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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U.S. Patent No. 10,734,481	Accused Products
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 6.
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 2.
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 4.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 5.
25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 6.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 7.
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 9.

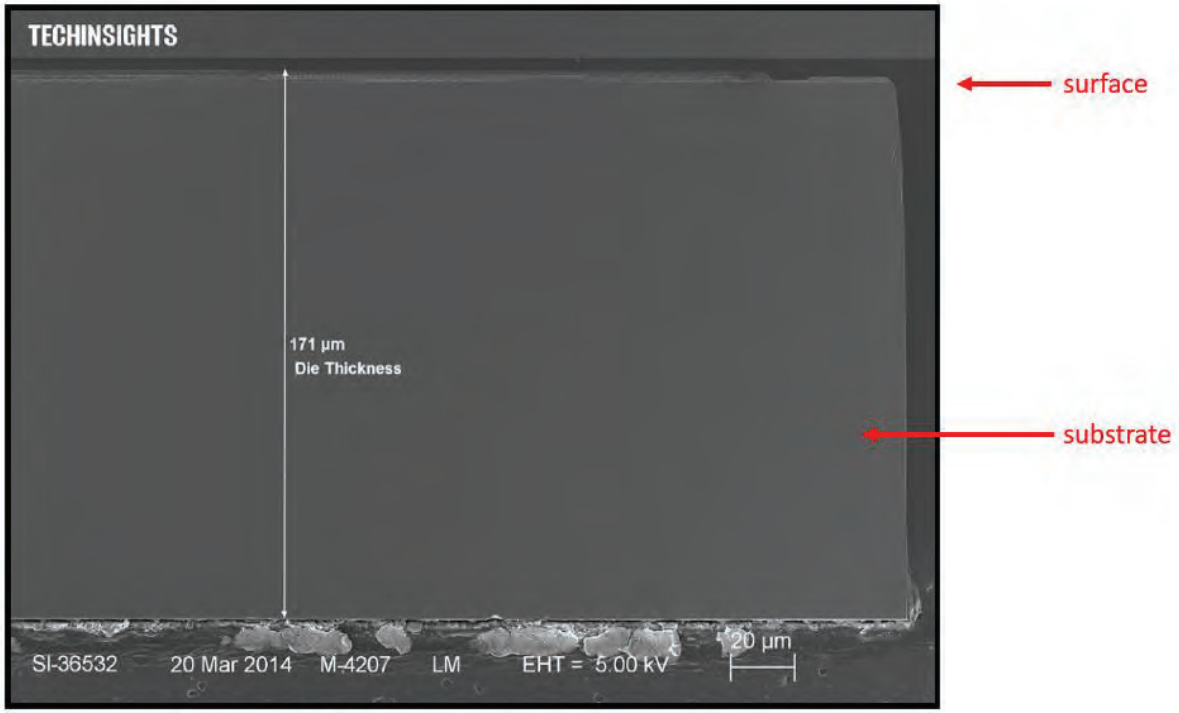
Exhibit B-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
first active region or the second active region are either p-type or n-type.	
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 8.
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 15.
33. The semiconductor device of claim 20, wherein the device is a flash memory.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 16.

Exhibit B-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a VLSI semiconductor device. A Micron SSD is a semiconductor device (*see* Exhibit B-1, Claim 1, Preamble) with millions of transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery. The Micron flash memory referenced in Exhibit B-1 is discussed in this claim chart and other infringement contention claim charts as an example of a Micron flash memory used in Dell-Micron-Flash Accused Products. Upon information and belief, such a Micron flash memory is representative of Micron memory devices used in the Dell-Micron-Flash Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other Micron flash memory devices used in Dell-Micron-Flash Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, other Micron flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Therefore, upon information and belief, other Micron memory devices used in Dell-Micron-Flash Accused Products contain similar features as the Micron 16 nm node NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 1.

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U.S. Patent No. 11,121,222	Accused Products
	 Figure 1.1.7: Die Thickness (SEM Cross-section), 16 nm MLC NAND flash memory of IMFT
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 3.

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U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 4.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 5. For example, referencing the SRP graph discussed at Exhibit B-1, Claim 1, Element 5, there are no active regions at depths of about 1.5 µm and greater. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the Dell-Micron-Flash Accused Products are in the possession of the Defendants and are expected to be obtained through discovery. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 2.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 5; Exhibit B-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. *See* above at Claim 1, Element 6.

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U.S. Patent No. 11,121,222	Accused Products
active region contain digital logic formed by one of either p-channel and n-channel devices.	
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.

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U.S. Patent No. 11,121,222	Accused Products
transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 15.
16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 16.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The Dell-Micron-Flash Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. *See* above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the Dell-Micron-Flash Accused Products are in the possession of the Defendants and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The Dell-Micron-Flash Accused Products meet this limitation. As shown by SEM imaging (*see* Exhibit B-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 9, Element 2.

U.S. Patent No. 11,121,222	Accused Products
conductivity to the first doping type and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 1, Element 6. As shown by SRP analysis (*see* Exhibit B-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SRP graph discussed at Exhibit B-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.

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Exhibit B-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

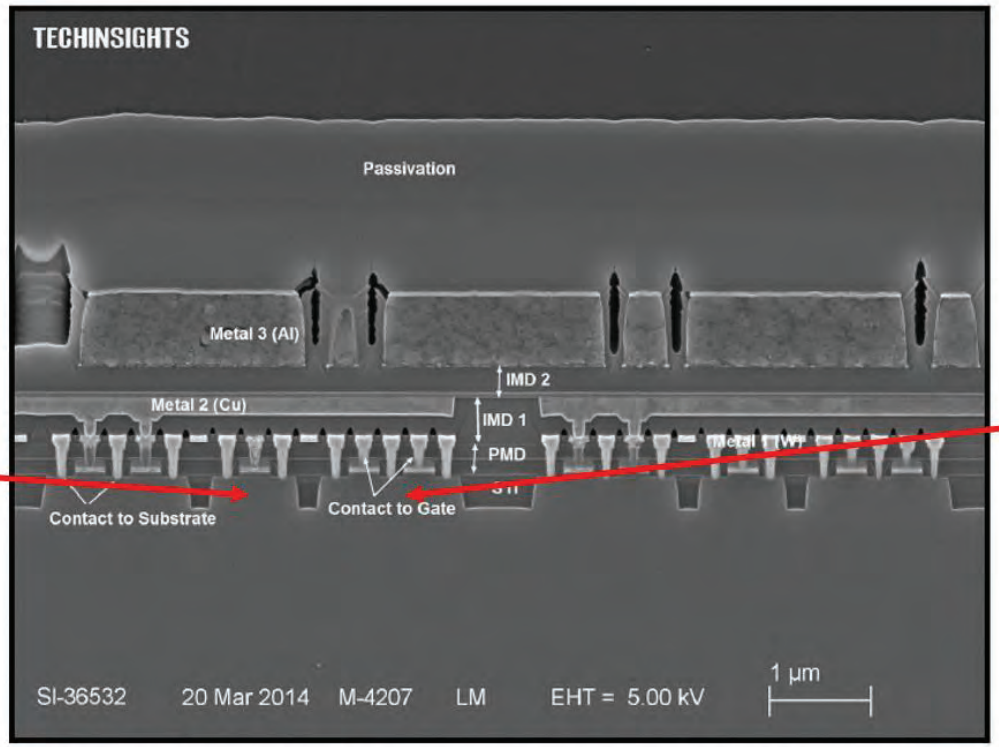
U.S. Patent No. 11,121,222	Accused Products
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 2.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 5.
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 8.

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graded dopant is fabricated with an ion implantation process.	
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 15.
34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 16.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	The Dell-Micron-Flash Accused Products meet this limitation. As shown by SEM imaging (*see* Figure 2.3.1 shown below and discussed at Exhibit B-1, Claim 1, Element 3), each of the first and second active regions are in the lateral or vertical direction.

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U.S. Patent No. 11,121,222	Accused Products
	 Figure 2.3.1: Peripheral logic transistor overview, (SEM cross-section), 16 nm MLC NAND flash memory of IMFT
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. *See* Exhibit B-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 2.

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Exhibit B-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

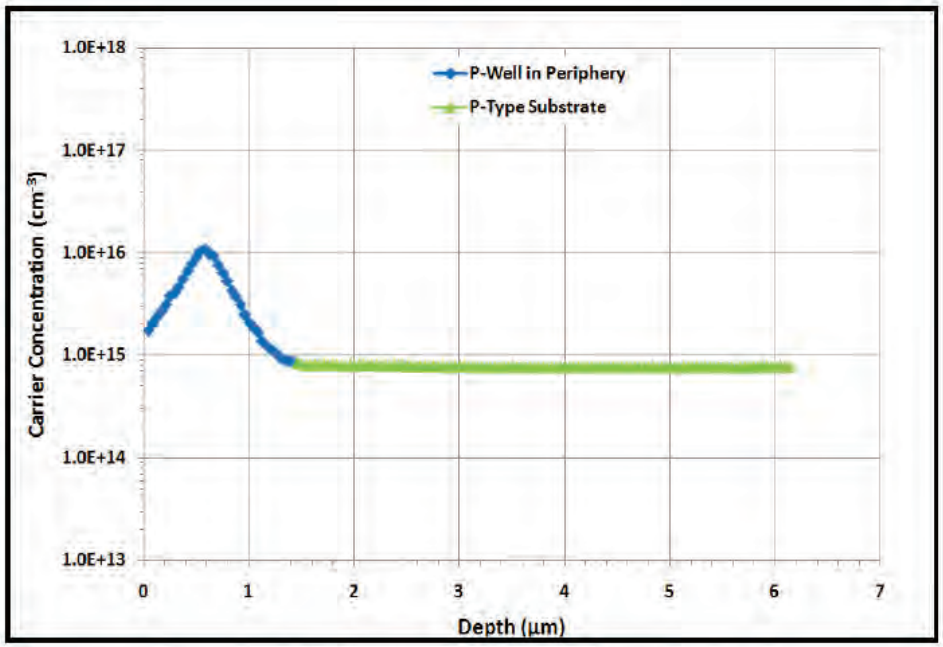
U.S. Patent No. 11,121,222	Accused Products
conductivity to the first doping type and within which transistors can be formed;	
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 5; *see* above at Claim 21, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 1, Element 6. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.

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Exhibit B-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

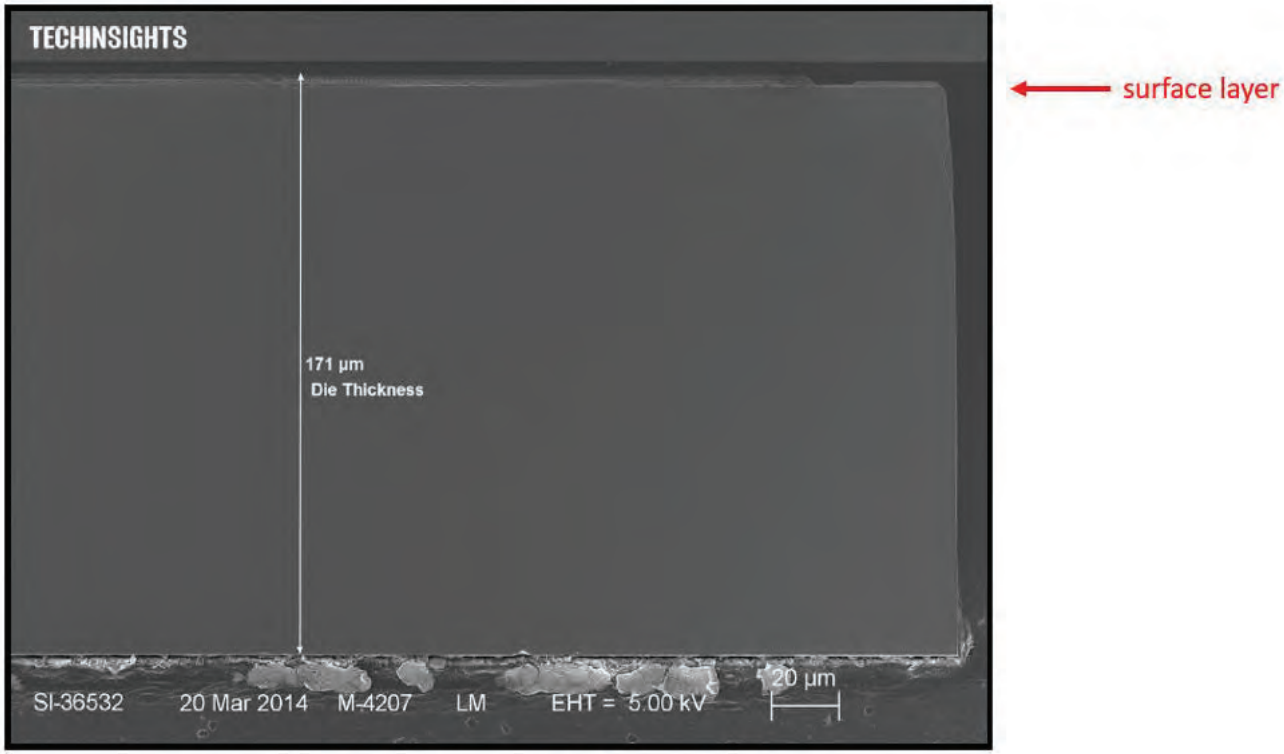
U.S. Patent No. 11,121,222	Accused Products
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 21, Element 5. The following graph obtained via SRP analysis reveals at least one graded dopant acceptor concentration (e.g., concentration in p-well) as claimed. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.

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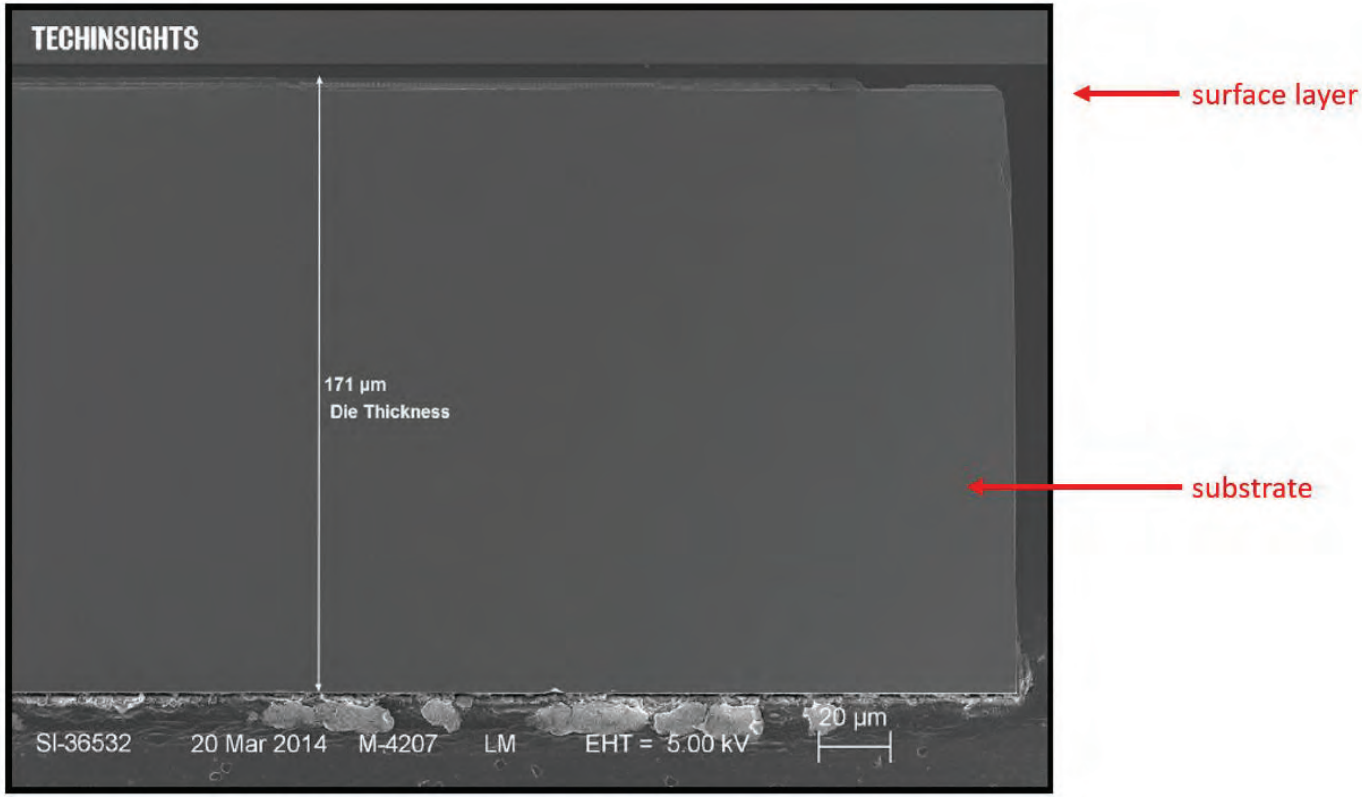
U.S. Patent No. 11,121,222	Accused Products
	 Figure 2.1.3: SRP analysis in the periphery, showing the peripheral P-well of 16 nm MLC NAND flash of IMFT
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 39, Element 2.

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type and within which transistors can be formed;	
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Micron-Flash Accused Products meet this limitation. SRP analysis (*see* Exhibit B-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a CMOS Semiconductor device. *See* Exhibit B-1, Claim 1, Preamble; Exhibit B-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 21, Element 1.

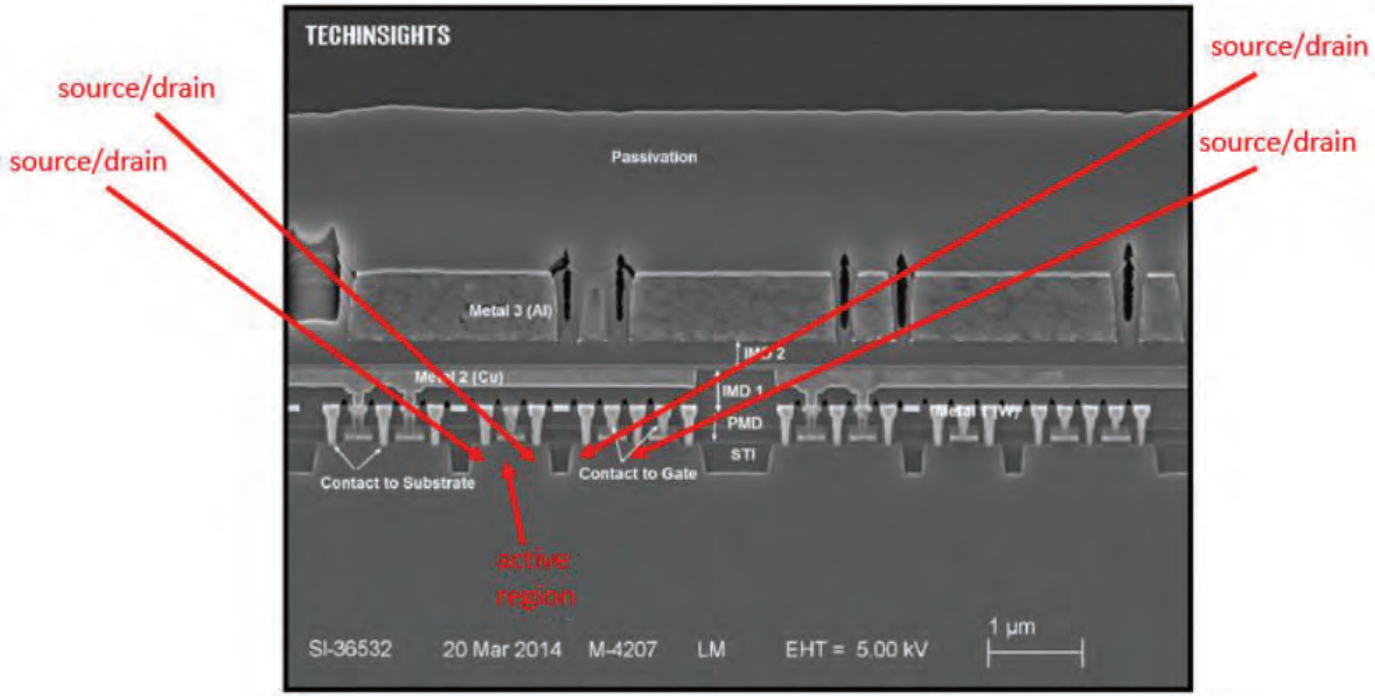
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U.S. Patent No. 11,121,222	Accused Products
	 Figure 1.1.7: Die Thickness (SEM Cross-section), 16 nm MLC NAND flash memory of IMFT As discussed below for Element 5, the surface layer can be, for example, the portion extending from the top of the above cross-section to a depth of about 1 µm.
[Claim 44, Element 2] a substrate;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 44, Element 1.

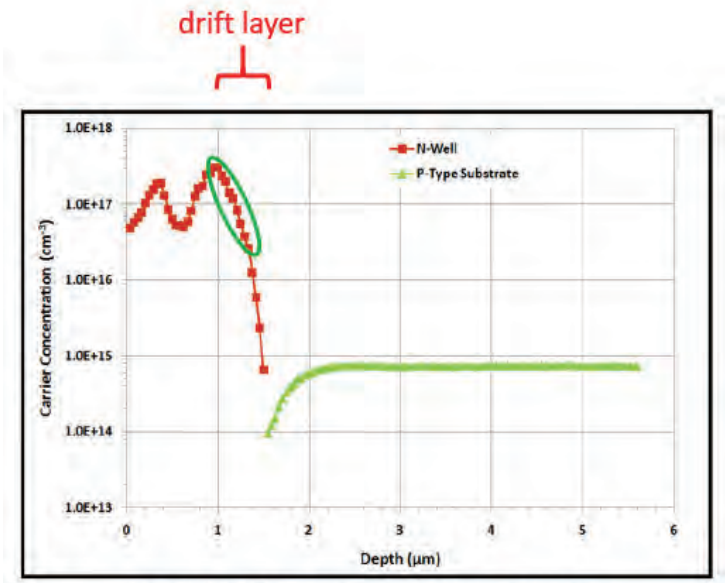
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U.S. Patent No. 11,121,222	Accused Products
	 Figure 1.1.7: Die Thickness (SEM Cross-section), 16 nm MLC NAND flash memory of IMFT
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Element 3. For example, the SEM image below (discussed at Exhibit B-1, Claim 1, Element 3) shows that the Micron flash memory includes an active region including a source and a drain disposed on one surface of the surface layer (e.g., as shown in the SEM image above for Claim 44, Element 2, the surface layer includes one surface facing away from the substrate (the active region is disposed on this surface) and another surface facing towards the substrate.

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	 Figure 2.3.1: Peripheral logic transistor overview, (SEM cross-section), 16 nm MLC NAND flash memory of IMFT
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 21, Element 5. For example, SRP analysis shows that the Micron flash memory includes a single drift layer having a graded concentration (annotated with green oval below) as claimed:

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U.S. Patent No. 11,121,222	Accused Products
	 Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants (annotated with purple oval below to indicate a region of relatively steeper slope in concentration, compared to the shallower region discussed for Claim 44, Element 4).

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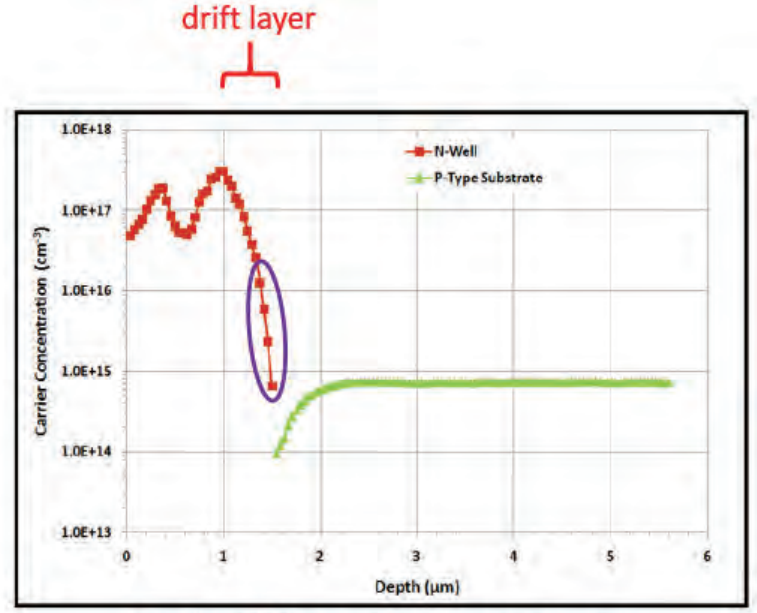
U.S. Patent No. 11,121,222	Accused Products
	 Figure 2.1.4: SRP analysis in the periphery, showing the peripheral N-well of 16 nm MLC NAND flash of IMFT Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.

Exhibit B-4 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a CMOS semiconductor device. *See* Exhibit B-3, Claim 44, Preamble. The Micron flash memory referenced in Exhibit B-1 is discussed in this claim chart and other infringement contention claim charts as an example of a Micron flash memory used in Dell-Micron-Flash Accused Products. Upon information and belief, such a Micron flash memory is representative of Micron flash memory used in the Dell-Micron-Flash Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other Micron flash memory devices used in Dell-Micron-Flash Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, other Micron flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Therefore, upon information and belief, other Micron flash memory devices used in Dell-Micron-Flash Accused Products contain similar features as the Micron 16 nm node NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 44, Element 4. Upon information and belief, the drift layer (*see* Exhibit B-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be obtained through discovery. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
[Claim 1, Element 5] at least one well region disposed in said single	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be

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U.S. Patent No. 8,421,195	Accused Products
drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	obtained through discovery. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The Dell-Micron-Flash Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 4; Exhibit B-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Elements 1, 5.

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Exhibit B-5 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include a semiconductor device. *See* Exhibit B-4, Claim 1, Preamble. The Micron flash memory referenced in Exhibit B-1 is discussed in this claim chart and other infringement contention claim charts as an example of a Micron flash memory used in Dell-Micron-Flash Accused Products. Upon information and belief, such a Micron flash memory is representative of Micron flash memory devices used in the Dell-Micron-Flash Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other Micron flash memory devices used in Dell-Micron-Flash Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, other Micron flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Therefore, upon information and belief, other Micron flash memory devices used in Dell-Micron-Flash Accused Products contain similar features as the Micron 16 nm node NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-4, Claim 1, Element 4. The graded concentration of dopants observed via SRP analysis (*see* Exhibit B-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-4, Claim 1, Element 5.

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Exhibit B-5 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 9,190,502	Accused Products
dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The Dell-Micron-Flash Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendants and are expected to be obtained through discovery. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
11. The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-2, Claim 16.

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Exhibit B-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include an electronic system. *See* Exhibit B-1, Claim 1, Preamble; Exhibit B-4, Claim 1, Preamble. Each Dell-Micron-Flash Accused Product is an electronic system, because a computer is an electronic system. The Micron flash memory referenced in Exhibit B-1 is discussed in this claim chart and other infringement contention claim charts as an example of a Micron flash memory used in Dell-Micron-Flash Accused Products. Upon information and belief, such a Micron flash memory is representative of Micron flash memory devices used in the Dell-Micron-Flash Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other Micron flash memory devices used in Dell-Micron-Flash Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, other Micron flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Therefore, upon information and belief, other Micron flash memory devices used in Dell-Micron-Flash Accused Products contain similar features as the Micron 16 nm node NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 1, Element 2; Exhibit B-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 1, Element 3; Exhibit B-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 1, Element 4.

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Exhibit B-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 1, Element 6; Exhibit B-3, Claim 21, Element 6. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 2.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 5.

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U.S. Patent No. 11,316,014	Accused Products
devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 15.
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 16.

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U.S. Patent No. 11,316,014	Accused Products
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 17.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-Micron-Flash Accused Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit B-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit B-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit B-1, Claim 9, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.

U.S. Patent No. 11,316,014	Accused Products
area of the substrate where there are no active regions; and	
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-Micron-Flash Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit B-3, Claim 21, Element 6. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. For SRP analysis showing carrier movement and electric fields, see Exhibit B-1, Claim 1, Element 5.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 26.
27. The system of Claim 21, wherein the first active region and second active region of the at least	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 27.

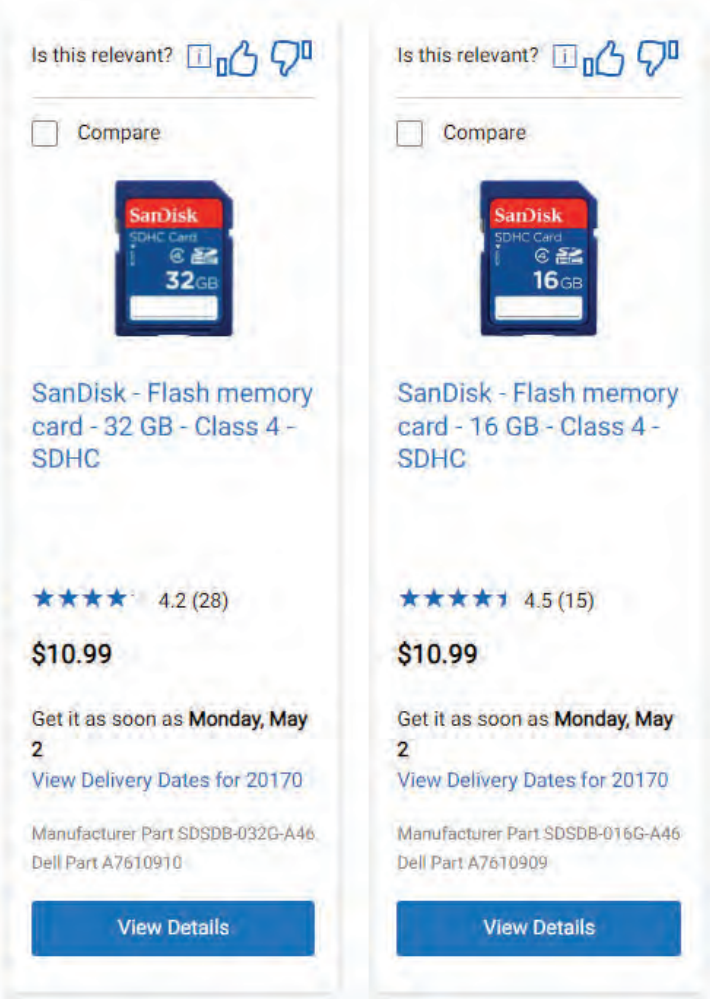
Exhibit B-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
one semiconductor device are each separated by at least one isolation region.	
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-Micron-Flash Accused Products meet this limitation. *See* Exhibit B-3, Claim 28.

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Exhibits C-1 to C-6
Dell-WD Accused Products

Exhibit C-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a semiconductor device. For example, as shown below, the Dell Defendants sell various examples of flash memory devices (e.g., microSD/SD cards and solid-state drives (SSDs), both of which contain flash memory). Below are examples of SanDisk SDHC (SD High Capacity) flash memory cards sold through Dell's website:  *See* https://www.dell.com/en-us/search/flash%20memory Below is an example of a SanDisk SSD sold through Dell's website:

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Exhibit C-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products



SanDisk Extreme Portable - Solid state drive - 500 GB - external (portable) - USB 3.1 Gen 2

Your life's an adventure. The SanDisk Extreme Portable SSD fits your mobile lifestyle and accelerates every move. Nearly 2x as fast as our previous generation!

Estimated Value ~~$139.99~~

$119.99 You Save $20.00 (14%)

Get it as soon as **Friday, Apr 29**

View Delivery Dates for 95050

Financing As low as $20/mo.^ | Apply for Credit

Up to $3 back in rewards

1 Add to Cart

Manufacturer Part SDSSDE61-500G-G25 | Dell Part AB609642 | Order Code Ab609642 | SanDisk

Compare

Tech Specs

General

Device Type

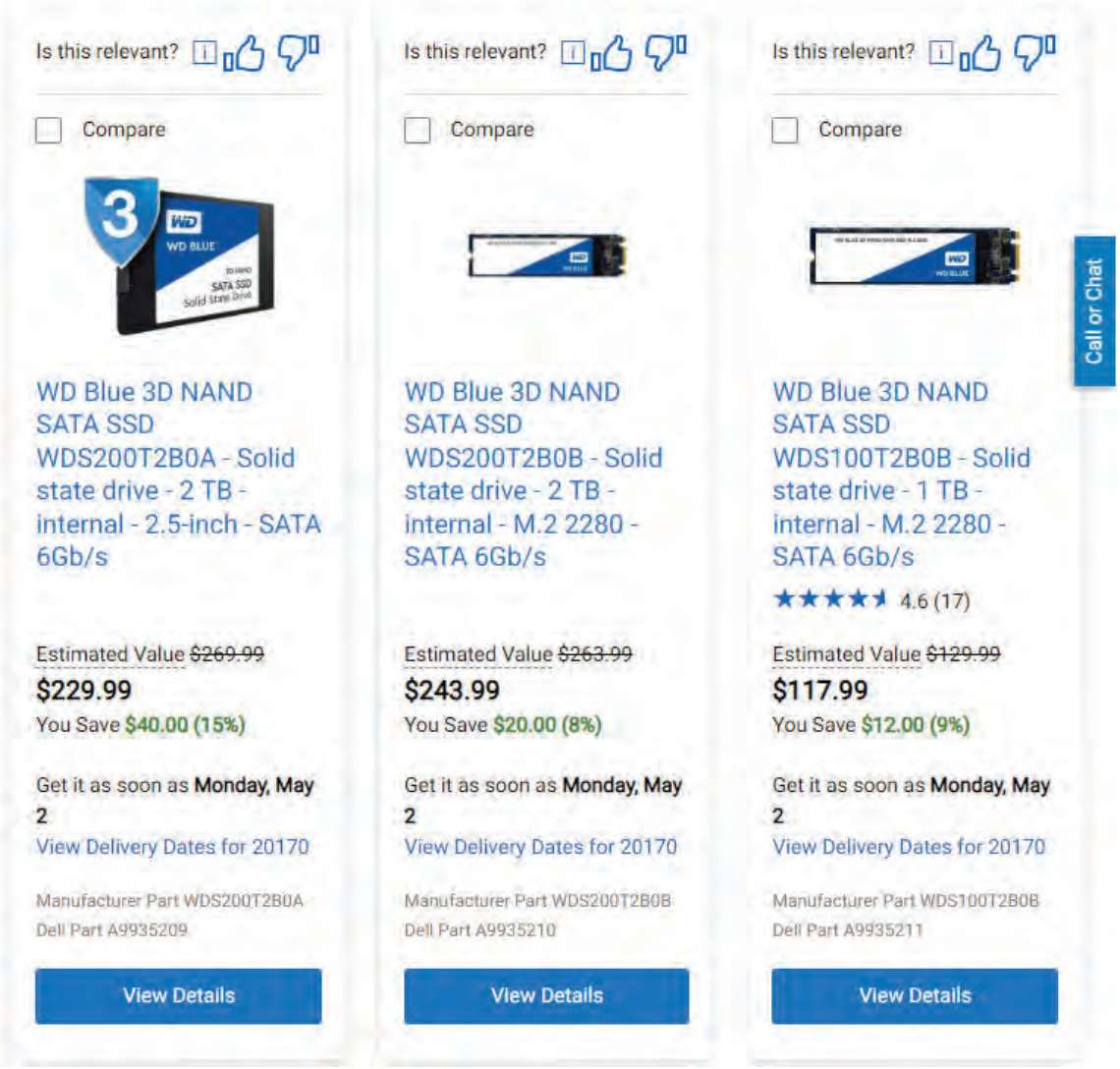
Solid state drive - external (portable)

See https://www.dell.com/en-us/shop/sandisk-extreme-portable-solid-state-drive-500-gb-external-portable-usb-31-gen-2/apd/ab609642/storage-drives-media

Below are examples of Western Digital SSDs sold through Dell's website:

Exhibit C-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products



See https://www.dell.com/en-us/search/wd%20ssd%20blue%203d

Such SSDs, like the other flash memory devices sold by Dell (e.g., SD/microSD cards), are semiconductor devices.

U.S. Patent No. 10,510,842	Accused Products
	What is a flash solid-state drive (SSD)? A flash solid-state drive (SSD) is a non-volatile storage device that stores persistent data in flash memory. There are two types of flash memory used in SSDs -- NAND and NOR. *See* https://www.techtarget.com/searchstorage/definition/flash-based-solid-state-drive-SSD Solid state refers to electronic circuitry that is built entirely of semiconductors. The term was originally used to define those electronics, such as a transistor radio that used semiconductors rather than vacuum tubes in its construction. Most electronics today are built around semiconductors and chips. A solid state drive uses, as its primary storage medium, semiconductors rather than the magnetic platters of a conventional hard drive. *See* https://www.lifewire.com/solid-state-drive-833448 The above SanDisk flash memory card and the above SanDisk and Western Digital SSDs are representative examples of the Dell-WD Accused Products, e.g., because all of these devices include a flash memory. A SanDisk 15 nm node NAND flash memory has been analyzed via tear-down and is described in this claim chart and other infringement contention claim charts (e.g., Exhibits C-1 through C-6), as explained below, as a representative example of the Dell-WD Accused Products. Upon information and belief, other flash memory devices sold or used by Dell would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Therefore, upon information and belief, other Dell-WD Accused Products contain similar features as the SanDisk 15 nm node NAND flash memory, and function in a similar way, with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-WD Accused Products include a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, a die of the SanDisk flash memory discussed above for the preamble is shown below:

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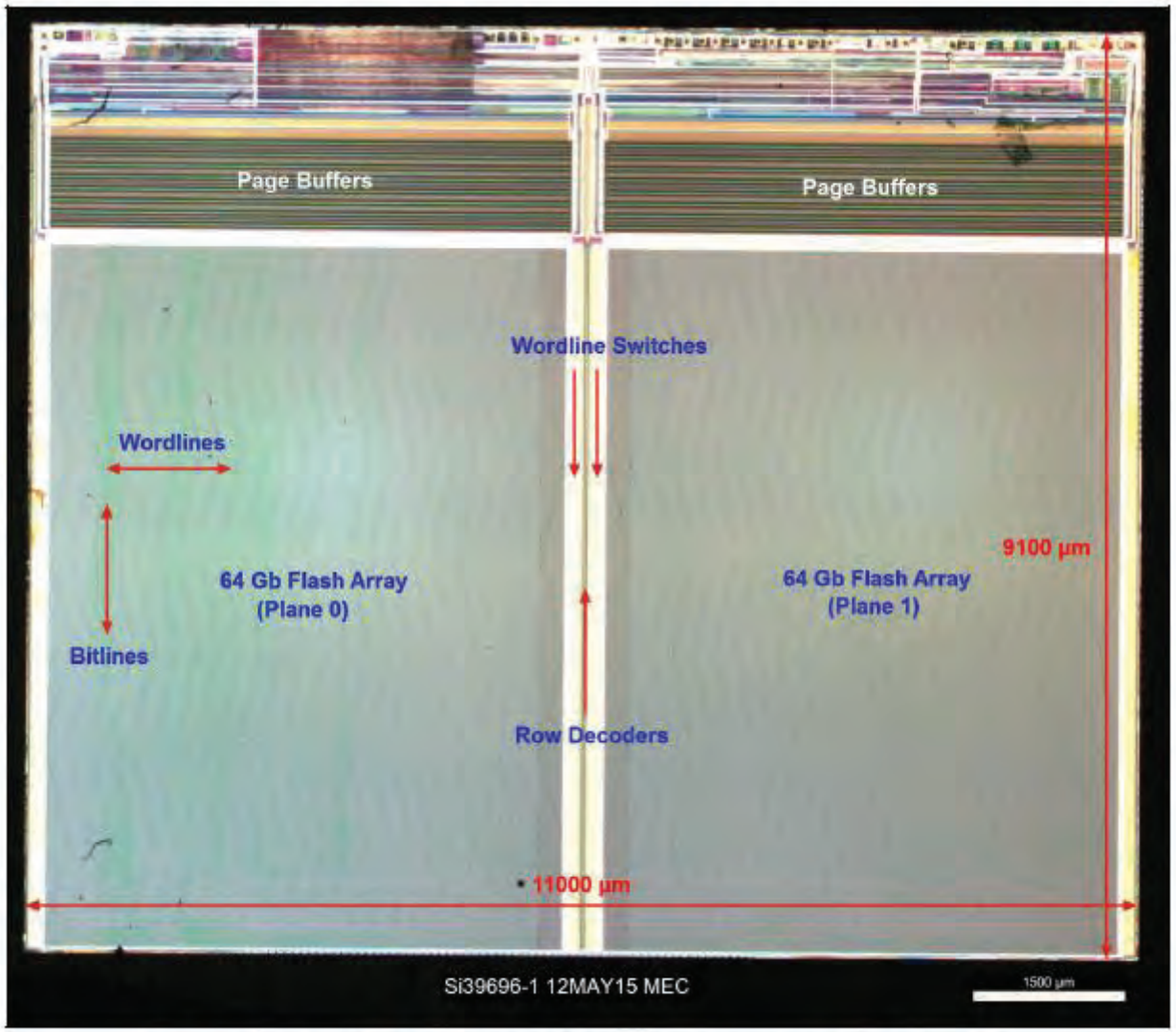
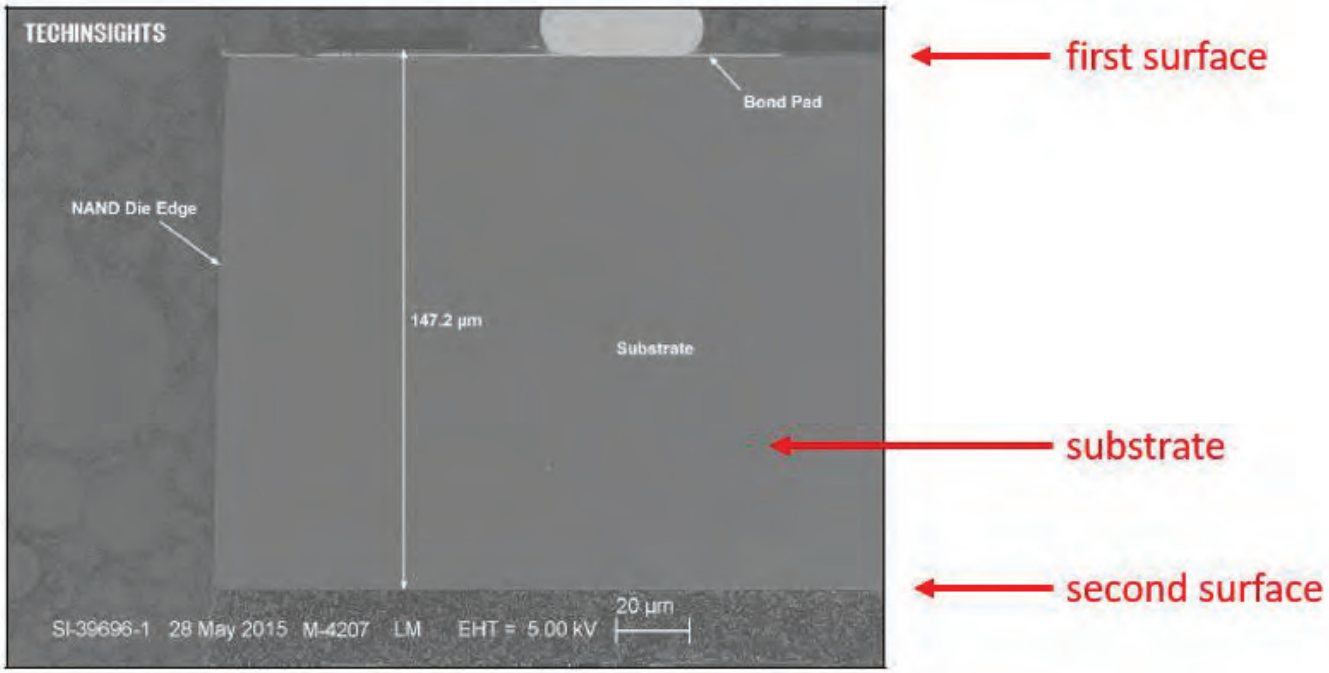


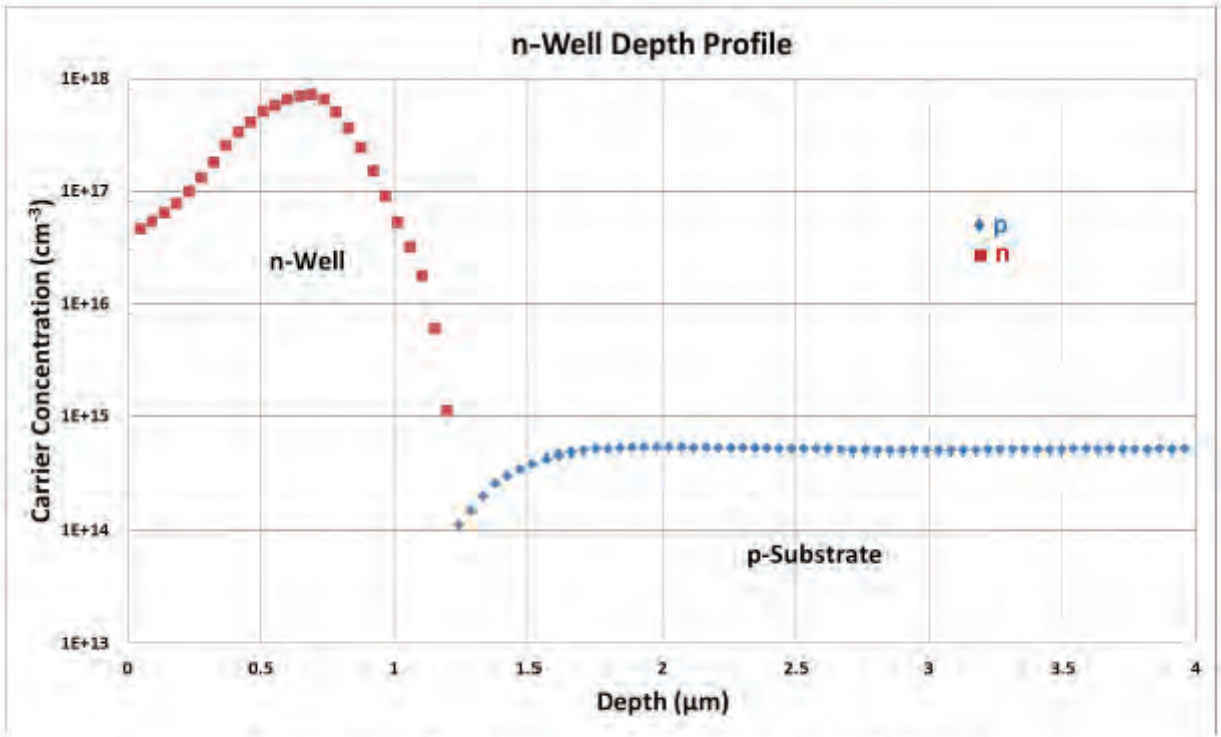
Figure 1.2.1: Die photograph of Toshiba/SanDisk 16 GB NAND die

The following image of a cross-section of the flash memory die, obtained through scanning electron microscopy (SEM), shows the die having a thickness of 147.2 µm in this example. The flash memory die includes a substrate having first and second surfaces, as shown

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U.S. Patent No. 10,510,842	Accused Products
	below:  Figure 1.2.3: Die thickness, SEM cross-sectional image A thickness (depth) of, e.g., 147.2 µm is consistent with the presence of a substrate. Spreading resistance profile (SRP) analysis conducted on the flash memory shows that the substrate is p-type (a first doping type) and has a first doping level (*see* concentration of p-type substrate in below graph).

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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-WD Accused Products include a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, the following cross-sectional image (labeled Figure 2.3.5) of the SanDisk flash memory device discussed above, obtained through scanning electron microscopy (SEM), shows a first active region as claimed:

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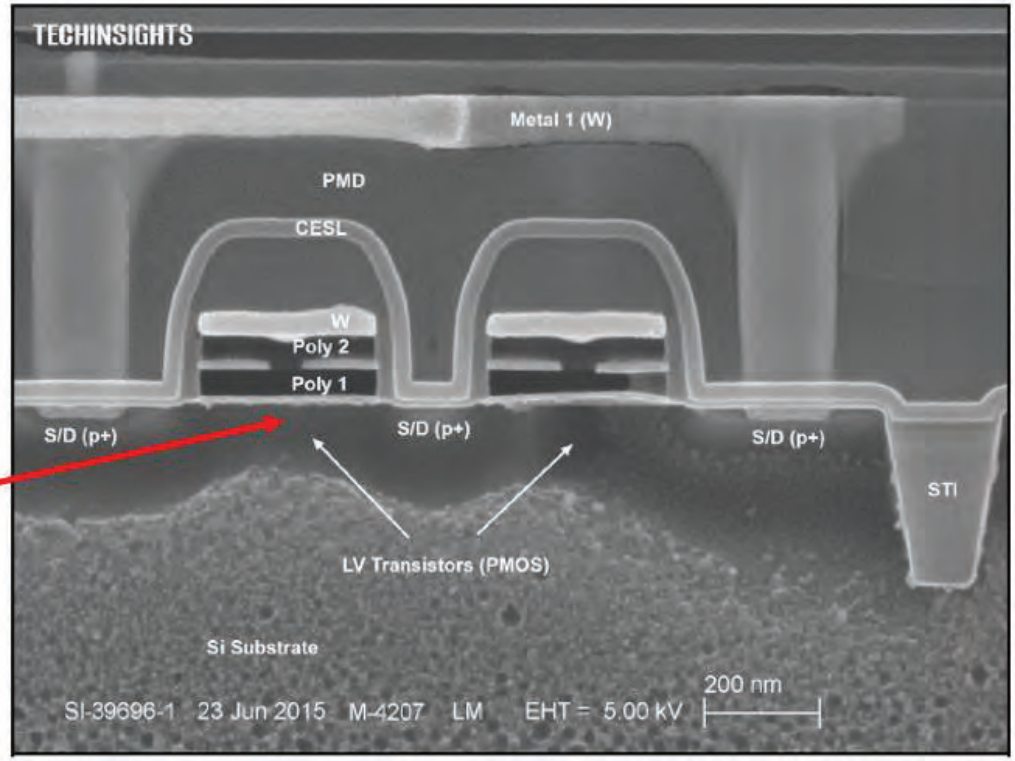
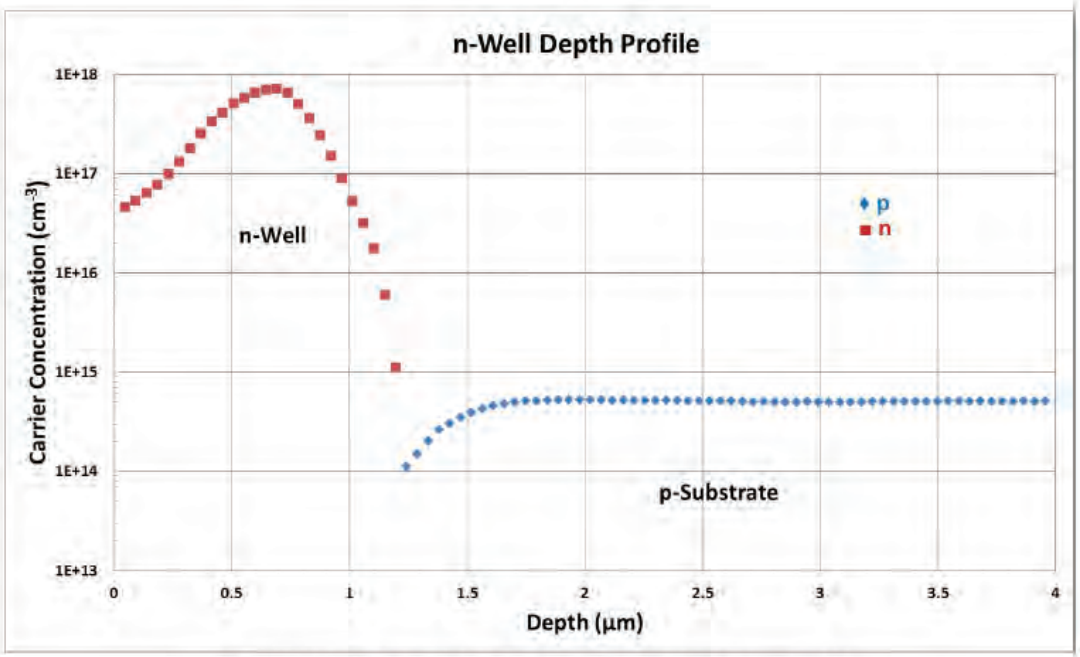


Figure 2.3.5: LV logic PMOS transistors, SEM cross-sectional image with Si etch

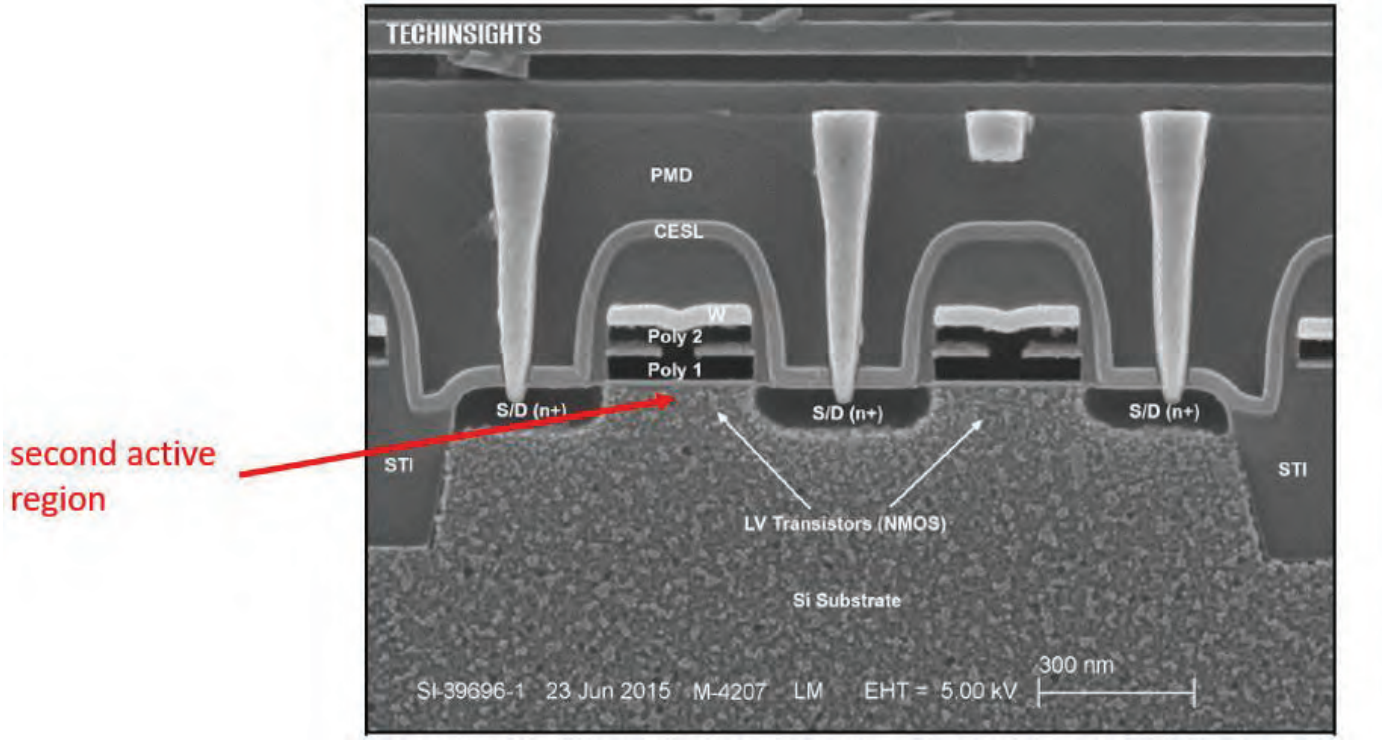
A PMOS transistor is shown above the first active region, and thus the first active region is a region within which transistors can be formed. For example, the gate of such a transistor is labeled in the above image. As shown in the above image, the first active region is disposed adjacent the first surface of the substrate.

The first active region has a second doping type (e.g., n-type) opposite in conductivity to the first doping type (p-type), e.g., as PMOS transistors are formed in n-wells. The presence of P^+ diffusion regions to the left and right of the first active region is consistent with the presence of PMOS transistors. The n-type doping of the n-well is also shown in the following SRP graph.

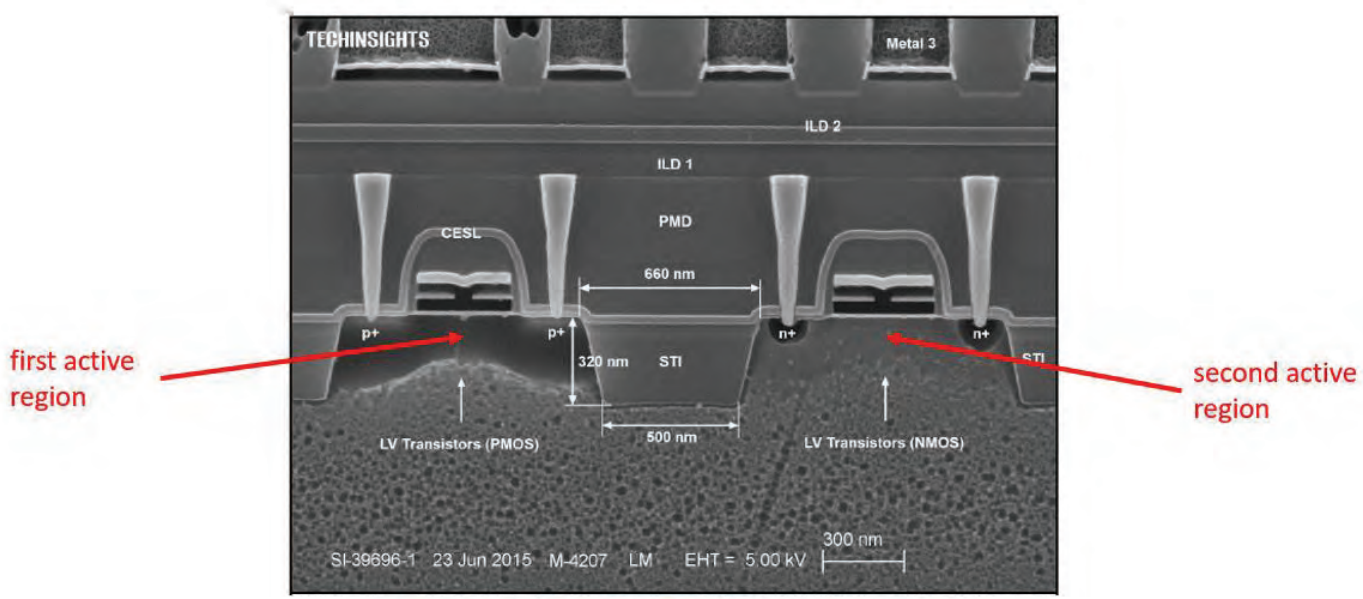
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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile The n-well shown above contains the first active region which is n-type.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-WD Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, a second active region as claimed is shown in the below SEM image (labeled Figure 2.3.4):

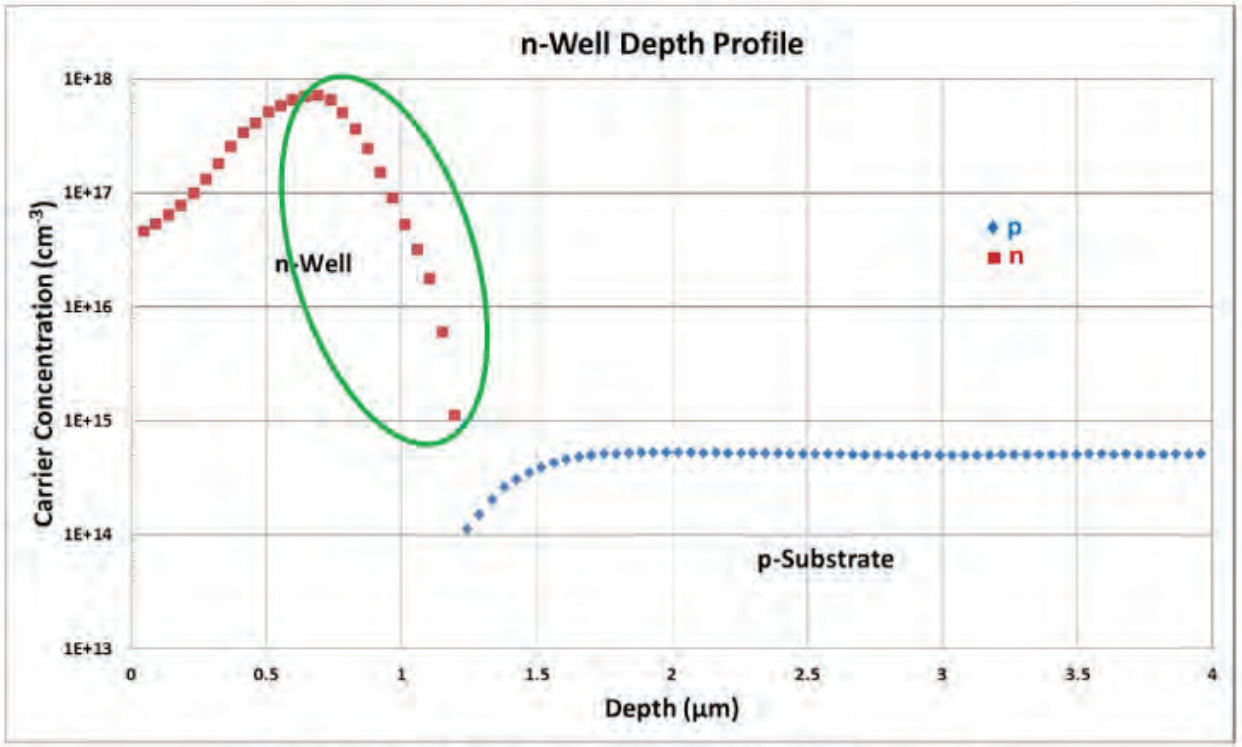
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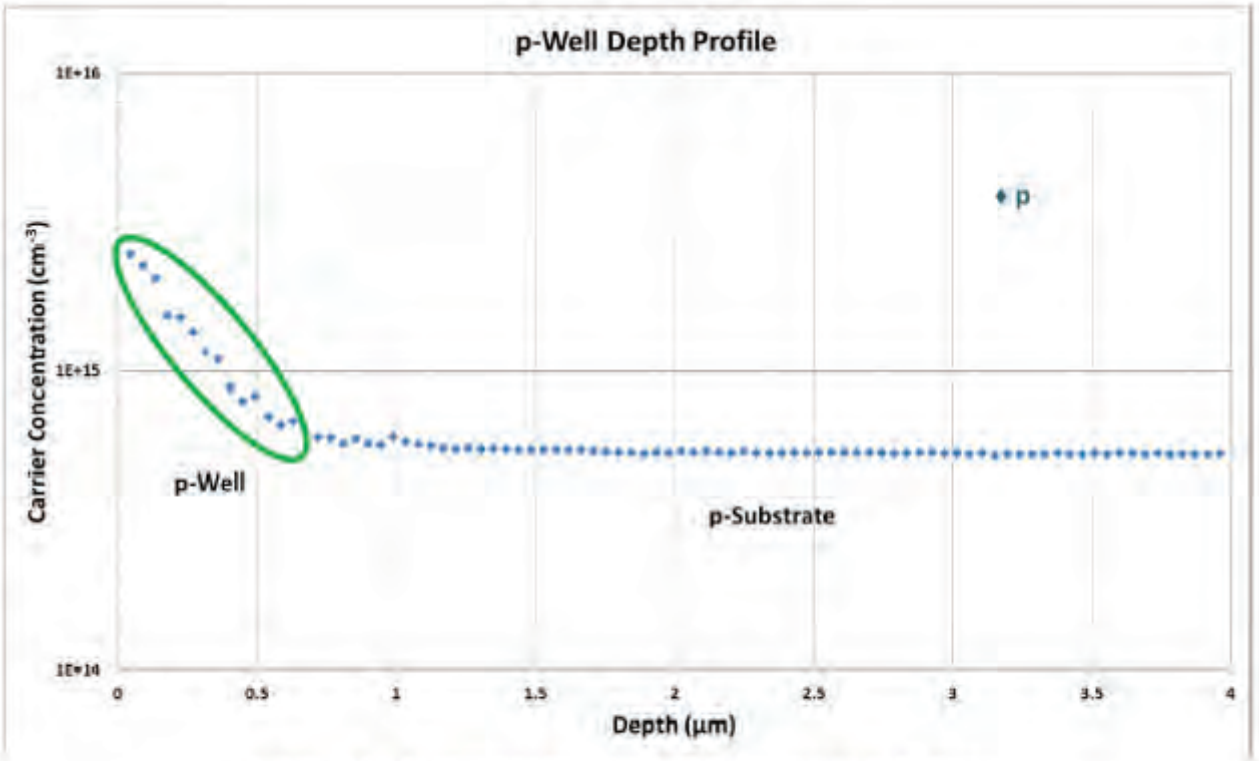
U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.3.4: LV logic NMOS transistors, SEM cross-sectional image with Si etch An NMOS transistor is shown above the second active region, and thus the second active region is a region within which transistors can be formed. For example, the gate of such a transistor is labeled in the above image.

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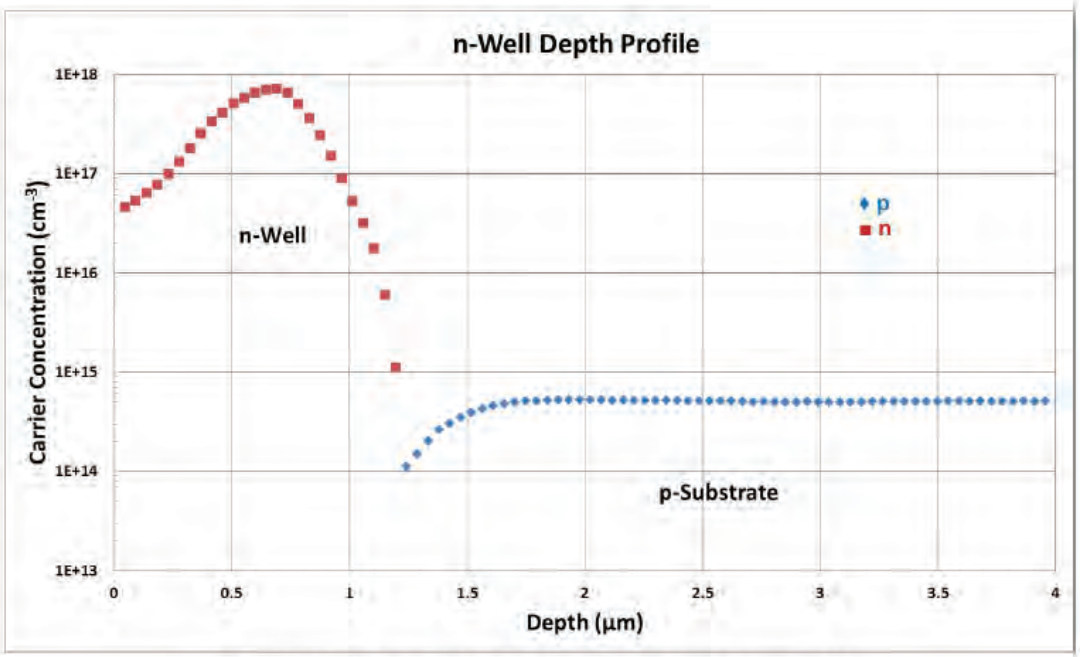
U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch As shown in the above SEM image (labeled Figure 2.3.9), the second active region (which is shown near an NMOS transistor) is separate from the first active region (which is shown near a PMOS transistor) and is disposed adjacent to the first active region.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-WD Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at Elements 2-3.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-WD Accused Products include a semiconductor device comprising at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate. For example, the graphs below, obtained via SRP analysis electrically characterizing the Dell-WD Accused Products, show a graded dopant concentration (annotated with green oval) in the first active region (e.g., as shown by the concentration corresponding to an n-well in the first graph below) and in the second active region (e.g., as shown by the concentration corresponding to a p-well in the second graph below) to aid carrier movement from the first surface to the second surface of the substrate (e.g., downwards, corresponding to increasing depth, in the below graphs). SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

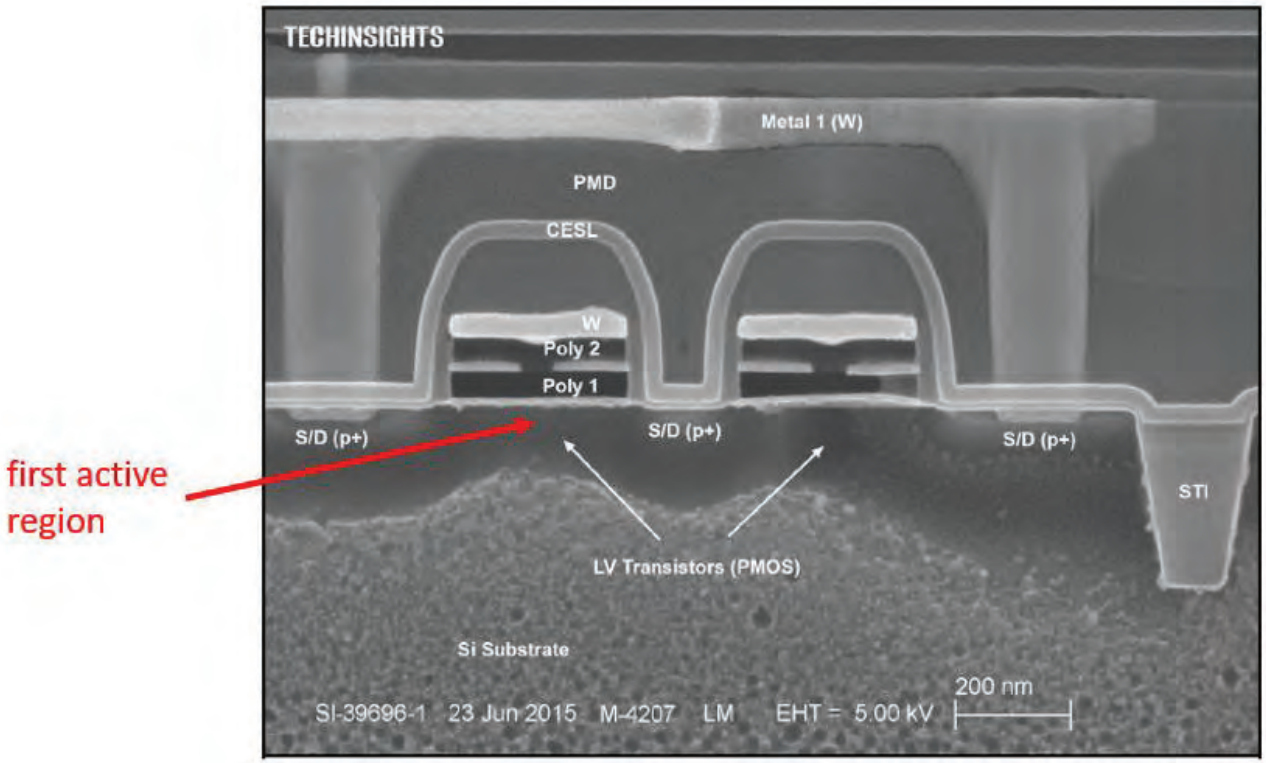
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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile

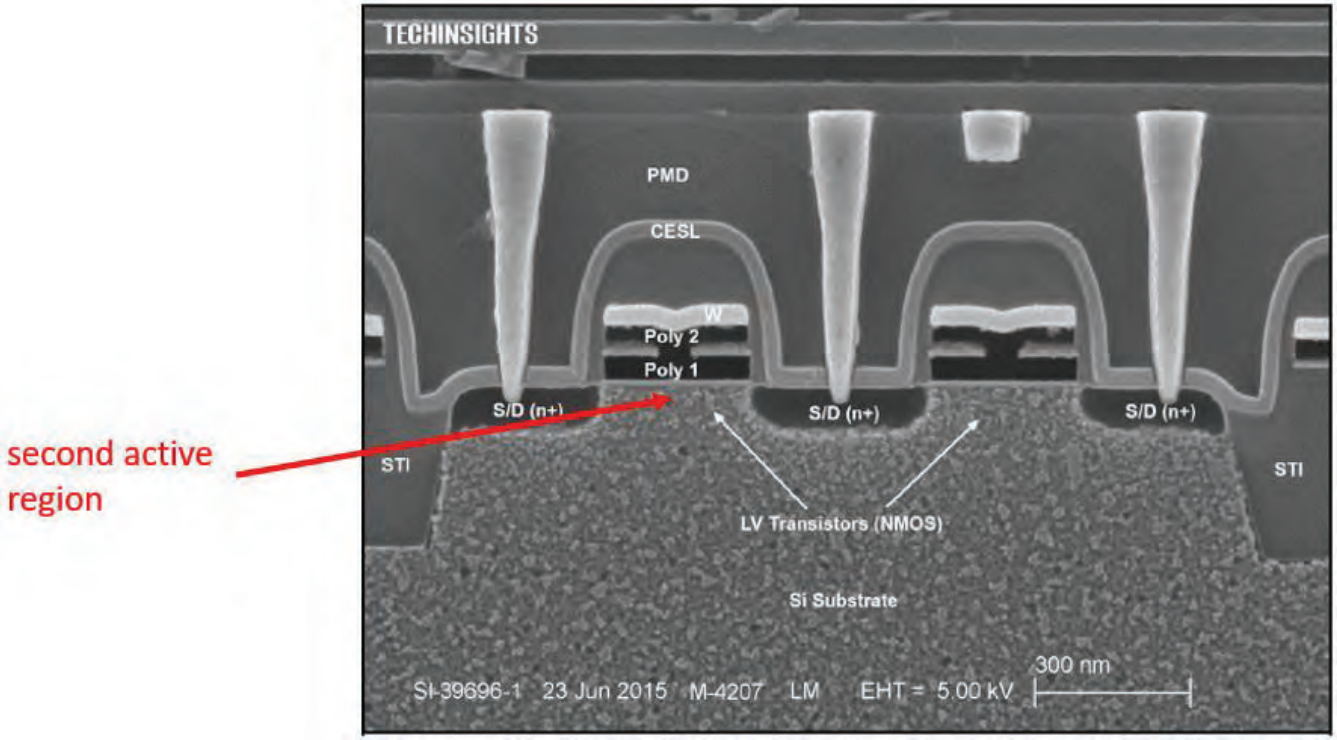
U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The substrate of the semiconductor device of the Dell-WD Accused Products is a p-type substrate, as discussed above for Claim 1, Element 1.
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The substrate of the semiconductor device of the Dell-WD Accused Products has epitaxial silicon on top of a nonepitaxial substrate. Upon information and belief, the substrate used in the Dell-WD Accused Products is a single-crystal silicon wafer. Additionally, SRP analysis shows a curve downwards in the below blue (corresponding to substrate) plot (from 1.7 µm towards shallower depths) indicative of a purer layer grown on the substrate, and this is likely implemented via epitaxy.

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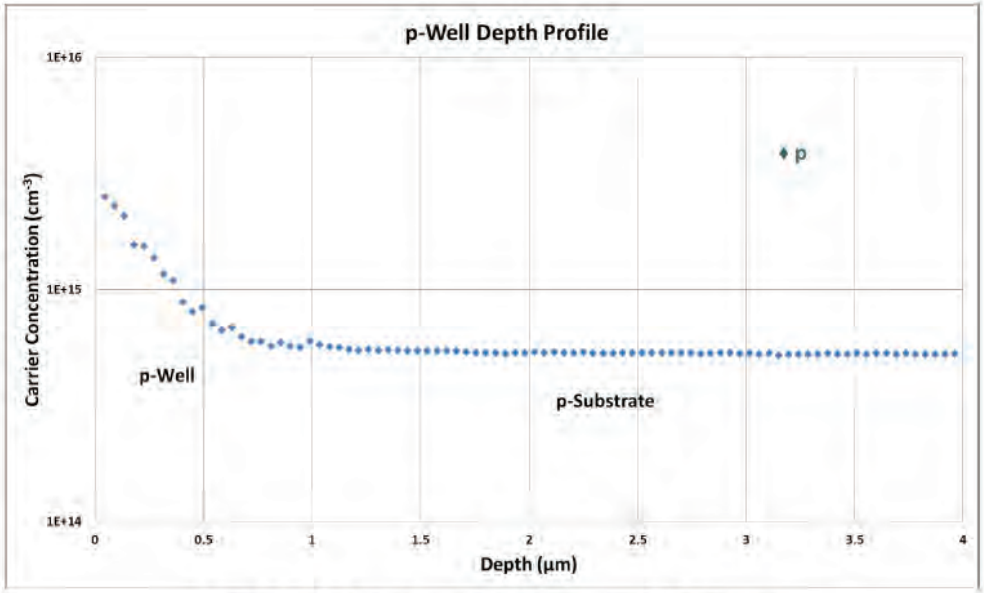
U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile
5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Dell-WD Accused Products meet this limitation. For example, in the following SEM image, the first and second active regions correspond to PMOS and NMOS transistors, respectively, e.g., as shown in the following SEM images (labeled Figures 2.3.14 and 2.3.15; *see also* above at Claim 1, Elements 2-3).

U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.3.5: LV logic PMOS transistors, SEM cross-sectional image with Si etch

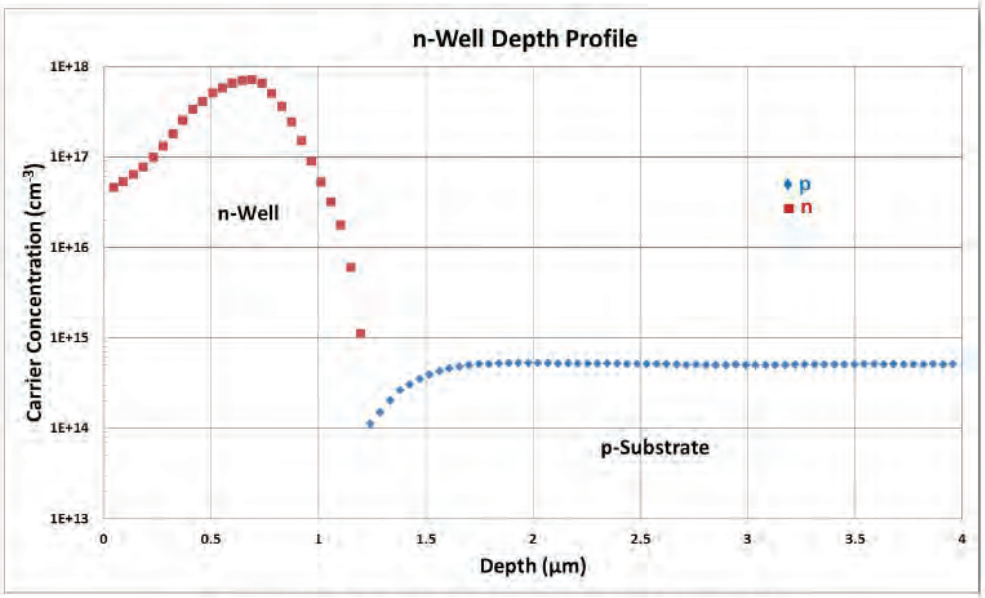
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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.3.4: LV logic NMOS transistors, SEM cross-sectional image with Si etch Thus, the first active region and second active region contain one of either p-channel and n-channel devices (e.g., the first active region contains a p-channel device, and the second active region contains an n-channel device).
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Dell-WD Accused Products meet this limitation. As discussed above for Claim 5, the periphery (region with peripheral NMOS and PMOS transistors shown in Figures 2.3.4 and 2.3.5) contains NMOS (n-channel) and PMOS (p-channel) devices in respective p-wells and n-wells. As discussed above for Claim 1, Elements 2-3 and Claim 5, the p-channel and n-channel devices are contained in the first and active regions (*see* annotated Figures 2.3.4 and 2.3.5 discussed above). The following graphs obtained via SRP analysis show a p-well having a graded dopant (e.g., depths from 0 to about 0.8 µm in first graph below) and an n-well having a graded dopant (e.g., depths of about 0.7-1.2 µm in second graph below).

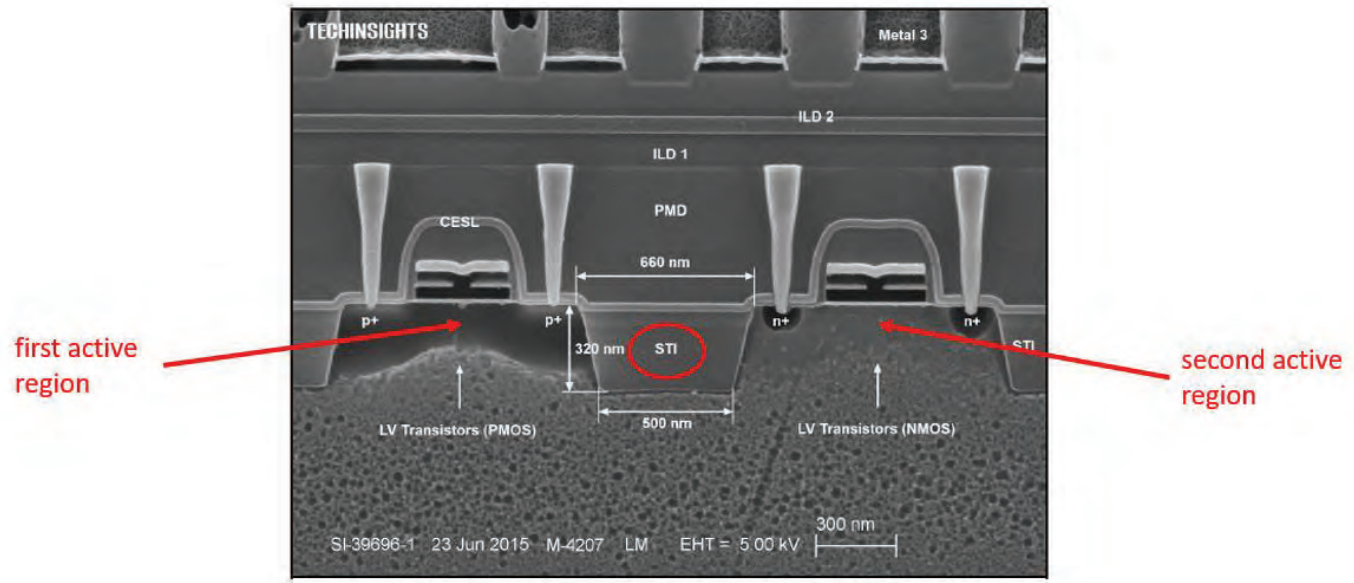
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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile

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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile The first and second active regions contain either p-channel or n-channel devices in these n-wells/p-wells because in CMOS technology a p-channel device is formed in an n-well and an n-channel device is formed in a p-well.
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-WD Accused Products meet this limitation. The following SEM cross-sectional image shows that the first active region and second active region are each separated by at least one isolation region, which is a shallow-trench isolation as indicated by the label STI (annotated below with red oval).

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U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch
8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Dell-WD Accused Products. Information about the fabrication process for Dell-WD Accused Products, including usage of an ion implantation process, is in the possession of the Dell Defendants and is expected to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of the Dell Defendants and are expected to be obtained through discovery.

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U.S. Patent No. 10,510,842	Accused Products
conductivity to the first doping type and within which transistors can be formed in the surface thereof;	
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of the Dell Defendants and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 5 SRP analysis electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 2.
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active	The Dell-WD Accused Products meet this limitation. *See* above at Claim 6.

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U.S. Patent No. 10,510,842	Accused Products
region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the Dell-WD Accused Products meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Dell-WD Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3; Claim 6. The SEM images labeled Figures 2.3.5 and 2.3.4 discussed above for Claim 1, Elements 2-3 and Claim 6 show NMOS and PMOS transistors, which are adjacent to one another as shown in the SEM image labeled Figure 2.3.9 discussed above for Claim 1, Element 3. Therefore, the transistors which can be formed in the first and second active regions are CMOS transistors. CMOS transistors require a source, a drain, a gate, and a channel region. The source and drain terminals of transistors are shown below, a gate is between each source-drain pair, and a channel region connects each source to a corresponding drain.

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Exhibit C-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

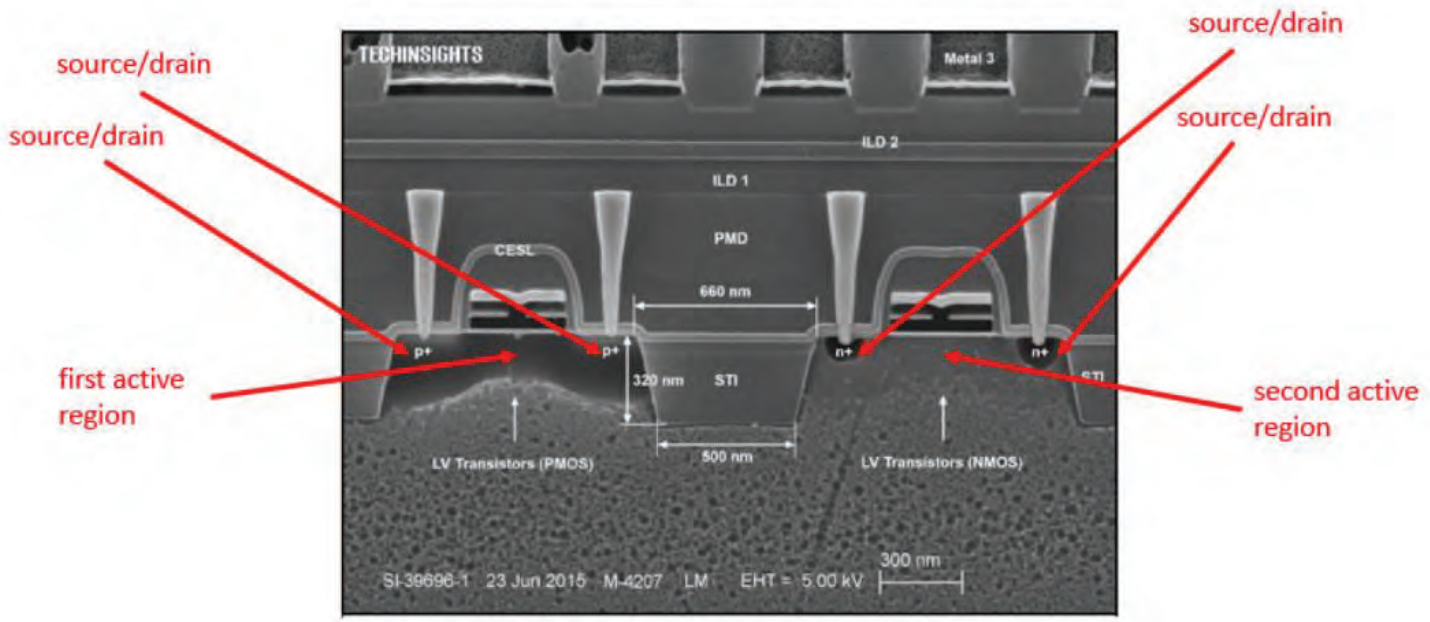
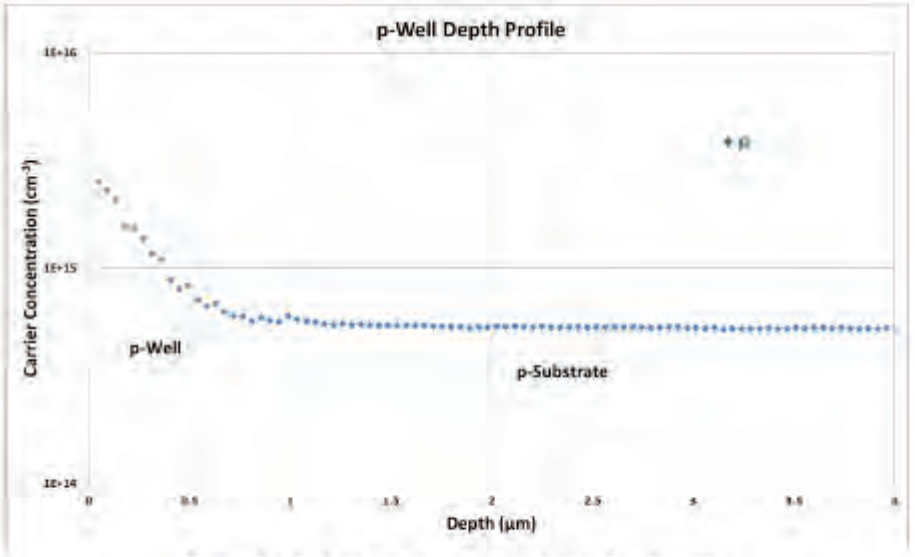
U.S. Patent No. 10,510,842	Accused Products
	 Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch

Exhibit C-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a semiconductor device. *See* Exhibit C-1, Claim 1, Preamble. The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit C-1 for tear-down analysis is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Dell-WD Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Dell-WD Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Dell-WD Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Dell-WD Accused Products contain similar features as the SanDisk 16 nm 16 GB NAND flash memory, and function in a similar way, with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 4.

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U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 5 SRP analysis electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-WD Accused Products meet this limitation. For example, the SanDisk flash memory includes a p-well (first graph below) and an n-well (second graph below) having graded dopant regions.  Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile

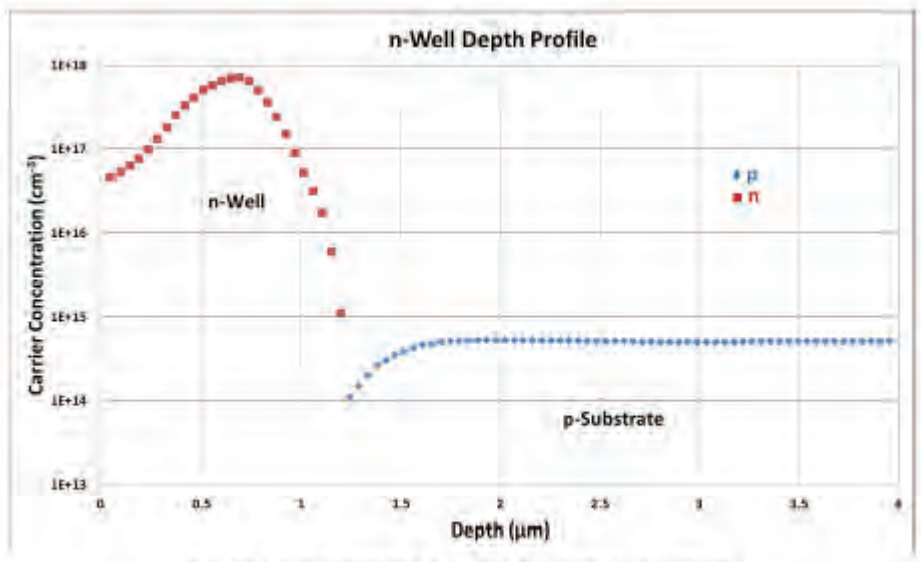
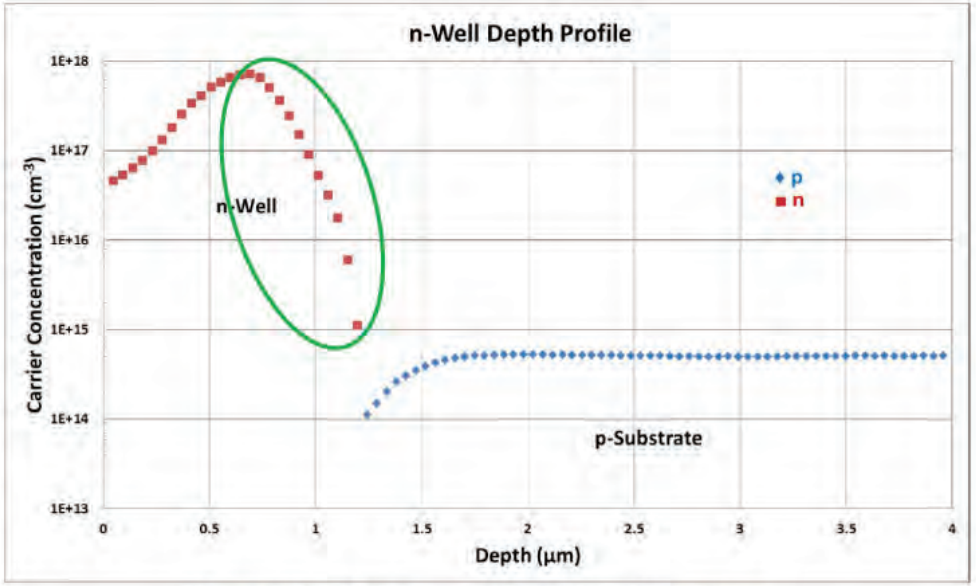
U.S. Patent No. 10,734,481	Accused Products
	 Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile These graded dopant regions are to aid carrier movement from the first surface to the second surface of the substrate. *See* Exhibit C-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 2.
3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 4.
4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 5.
5. The semiconductor device of claim 1, wherein the first active	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 6.

Exhibit C-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 7.
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 8.
8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Elements 1-3.
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 5 (SRP analysis of Figures 2.1.4 and 2.1.5 (below) showing n-type doping and p-type doping, respectively, at graded dopant concentration).

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	 Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile

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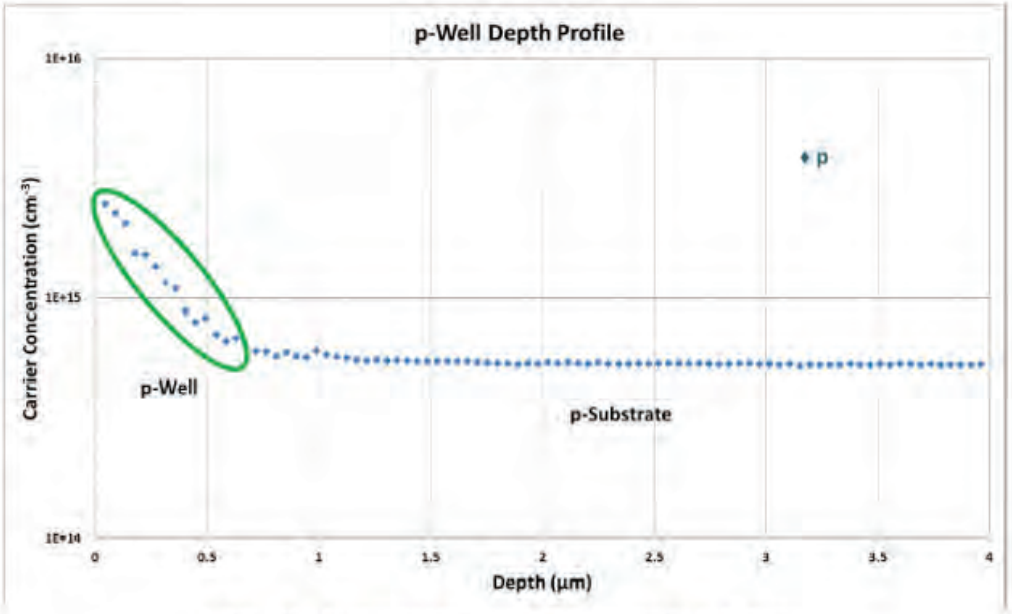
U.S. Patent No. 10,734,481	Accused Products
	 Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile
13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 18.
15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claims 4 (regarding nonepitaxial substrate), 18 (regarding CMOS).
16. The semiconductor device of claim 1, wherein the device is a flash memory.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Preamble.

Exhibit C-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products meet include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 9, Element 2.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 9, Element 3.
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 6. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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Exhibit C-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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movement from the first surface to the second surface of the substrate.	
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 2.
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 4.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 5.
25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 6.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 7.
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 9.

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Exhibit C-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 8.
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 15.
33. The semiconductor device of claim 20, wherein the device is a flash memory.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 16.

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Exhibit C-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a VLSI semiconductor device. The SanDisk flash memory discussed for claim 1 of Exhibit C-1 is a semiconductor device (*see* Exhibit C-1, Claim 1, Preamble) with millions of transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Dell Defendants and are expected to be obtained through discovery. The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit C-1 is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Dell-WD Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Dell-WD Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Dell-WD Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Dell-WD Accused Products contain similar features as the SanDisk 15 nm 16 GB NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 1.

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Exhibit C-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

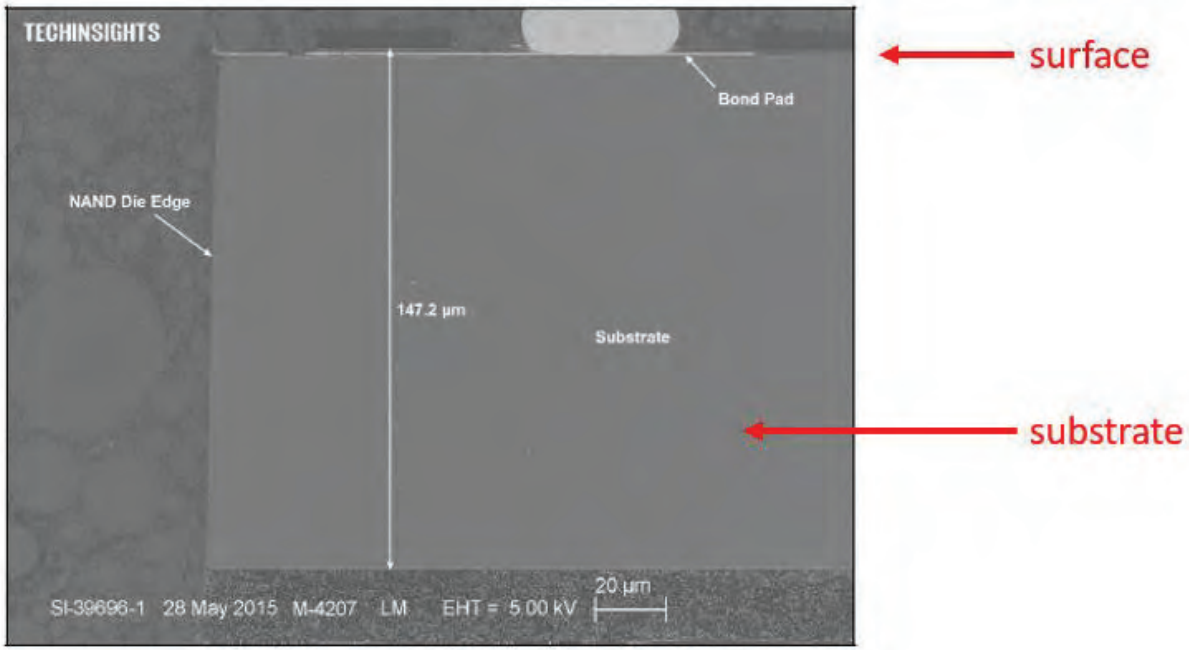
U.S. Patent No. 11,121,222	Accused Products
	 Figure 1.2.3: Die thickness, SEM cross-sectional image
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 3.

Exhibit C-3 to Greenthread's Amended Preliminary Infringement Contentions 1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 4.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 5. For example, referencing the SRP graph discussed at Exhibit C-1, Claim 1, Element 5, there are no active regions at depths of about 1.3 µm and greater. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the Dell-WD Accused Products are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 2.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 5; Exhibit C-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. *See* above at Claim 1, Element 6.

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U.S. Patent No. 11,121,222	Accused Products
active region contain digital logic formed by one of either p-channel and n-channel devices.	
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.

U.S. Patent No. 11,121,222	Accused Products
transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 15.
16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 16.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The Dell-WD Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. *See* above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the Dell-WD Accused Products are in the possession of the Dell Defendants and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The Dell-WD Accused Products meet this limitation. As shown by SEM imaging (*see* Exhibit C-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 9, Element 2.

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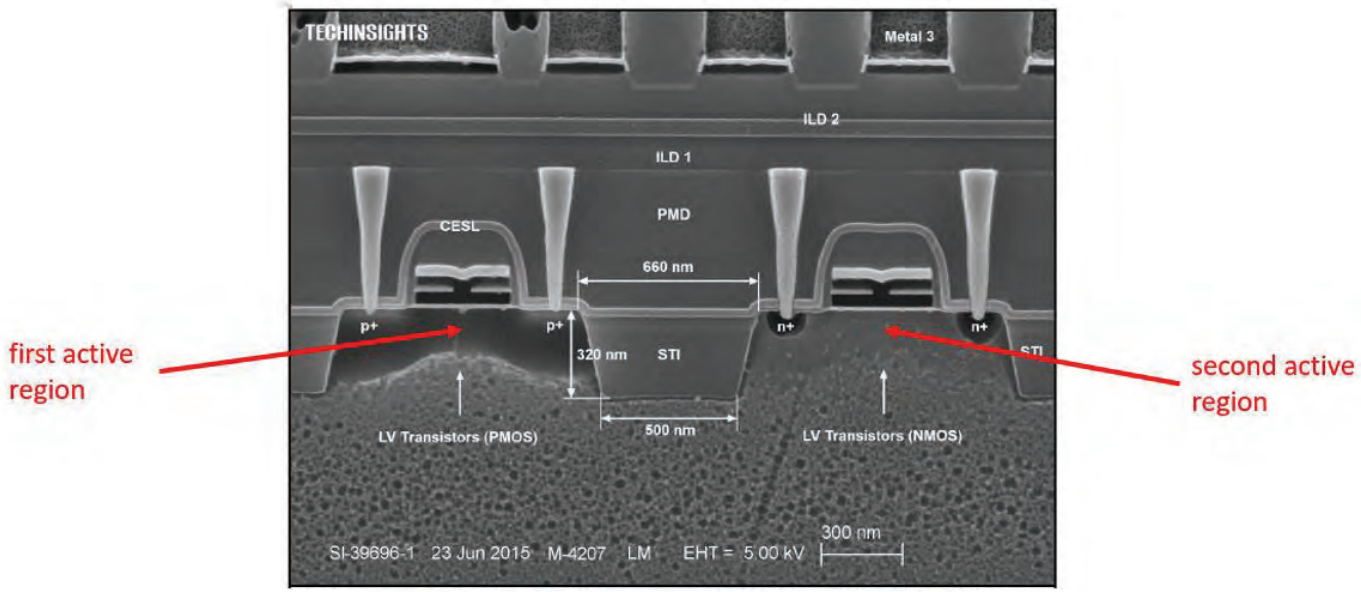
U.S. Patent No. 11,121,222	Accused Products
conductivity to the first doping type and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 1, Element 6. As shown by SRP analysis (*see* Exhibit C-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SRP graph discussed at Exhibit C-1, Claim 1, Element 5. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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Exhibit C-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 2.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 5.
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 8.

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graded dopant is fabricated with an ion implantation process.	
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 15.
34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 16.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	The Dell-WD Accused Products meet this limitation. As shown by SEM imaging (*see* Figure 2.3.9 shown below and discussed at Exhibit C-1, Claim 1, Element 3), each of the first and second active regions are in the lateral or vertical direction.  Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch

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Exhibit C-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

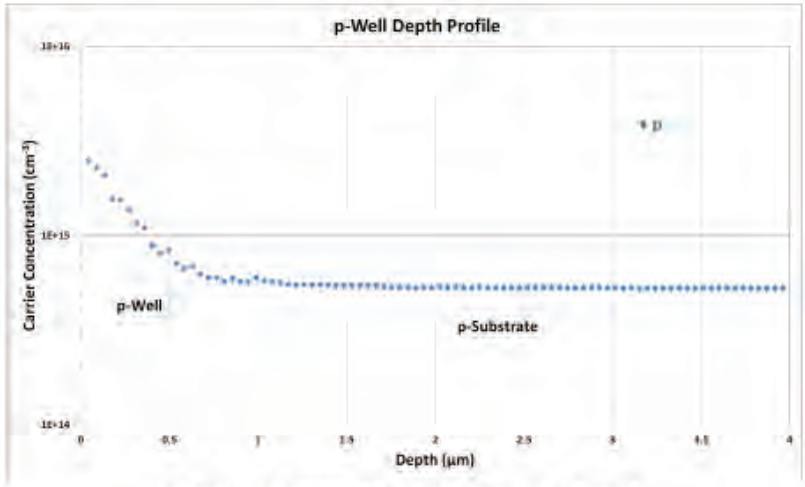
U.S. Patent No. 11,121,222	Accused Products
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a semiconductor device. *See* Exhibit C-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 5; *see* above at Claim 21, Element 5. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 1, Element 6. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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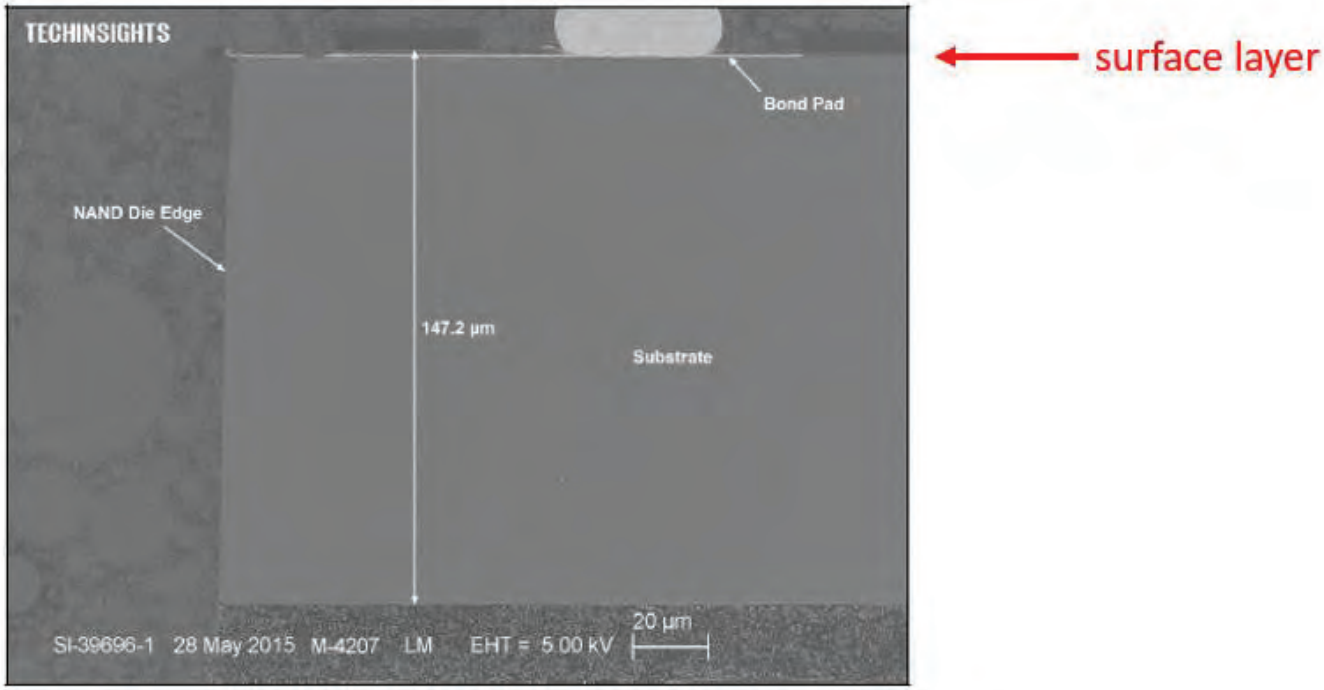
U.S. Patent No. 11,121,222	Accused Products
the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid	The Dell-WD Accused Products meet this limitation. *See* above at Claim 21, Element 5. The following graph obtained via SRP analysis reveals at least one graded dopant acceptor concentration (e.g., concentration in p-well) as claimed.

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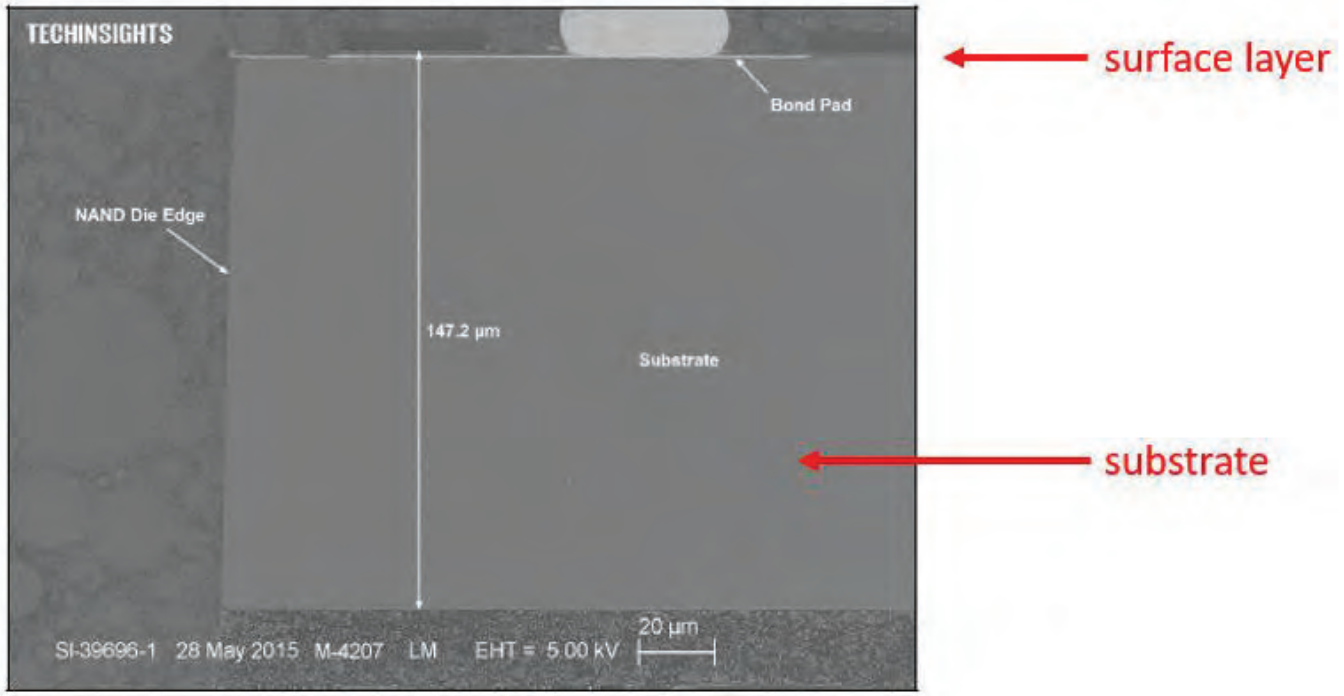
U.S. Patent No. 11,121,222	Accused Products
carrier movement from the first or second active region to at least one substrate area where there is no active region.	 Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 42, Element 3] a second active region separate from the first active region	The Dell-WD Accused Products meet this limitation. *See* above at Claim 39, Element 3.

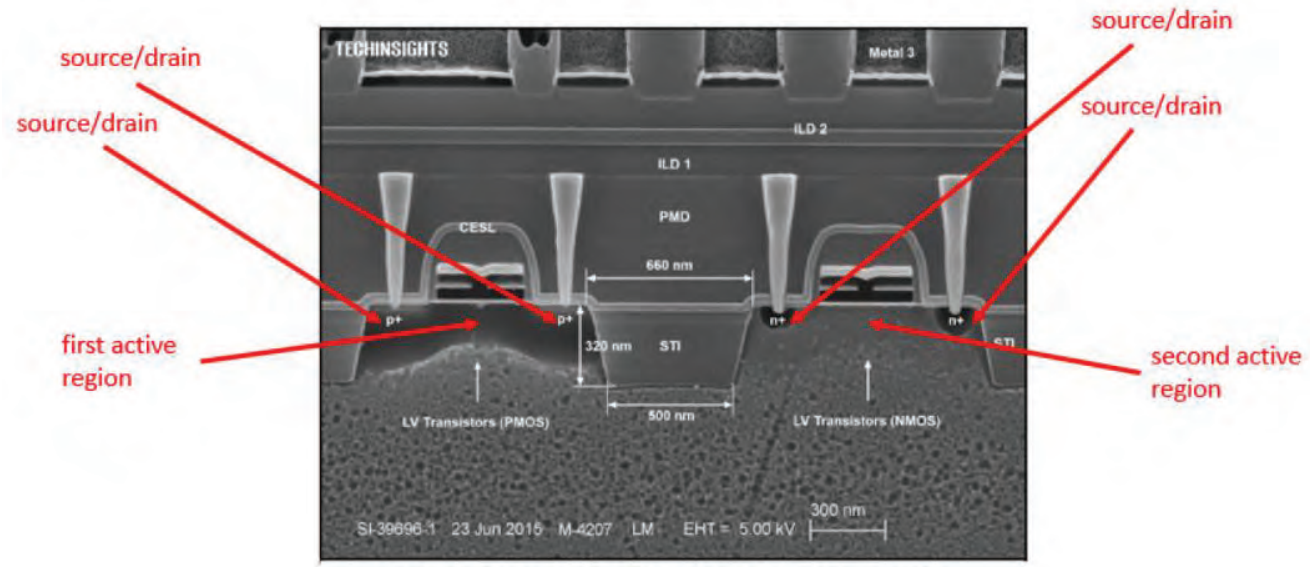
U.S. Patent No. 11,121,222	Accused Products
disposed adjacent to the first active region and within which transistors can be formed;	
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-WD Accused Products meet this limitation. SRP analysis (*see* Exhibit C-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a CMOS Semiconductor device. *See* Exhibit C-1, Claim 1, Preamble; Exhibit C-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 21, Element 1.

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	 Figure 1.2.3: Die thickness, SEM cross-sectional image
[Claim 44, Element 2] a substrate;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 44, Element 1.

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	 Figure 1.2.3: Die thickness, SEM cross-sectional image
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Element 3. For example, the SEM image below (discussed at Exhibit C-1, Claim 1, Element 3) shows that the Sandisk flash memory includes an active region including a source and a drain disposed on one surface of the surface layer (e.g., as shown in the SEM image above for Claim 44, Element 2, the surface layer includes one surface facing away from the substrate (the active region is disposed on this surface) and another surface facing towards the substrate).

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	 Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The Dell-WD Accused Products meet this limitation. *See* above at Claim 21, Element 5. For example, SRP analysis shows that the SanDisk flash memory includes a single drift layer having a graded concentration (annotated with green oval below) as claimed:

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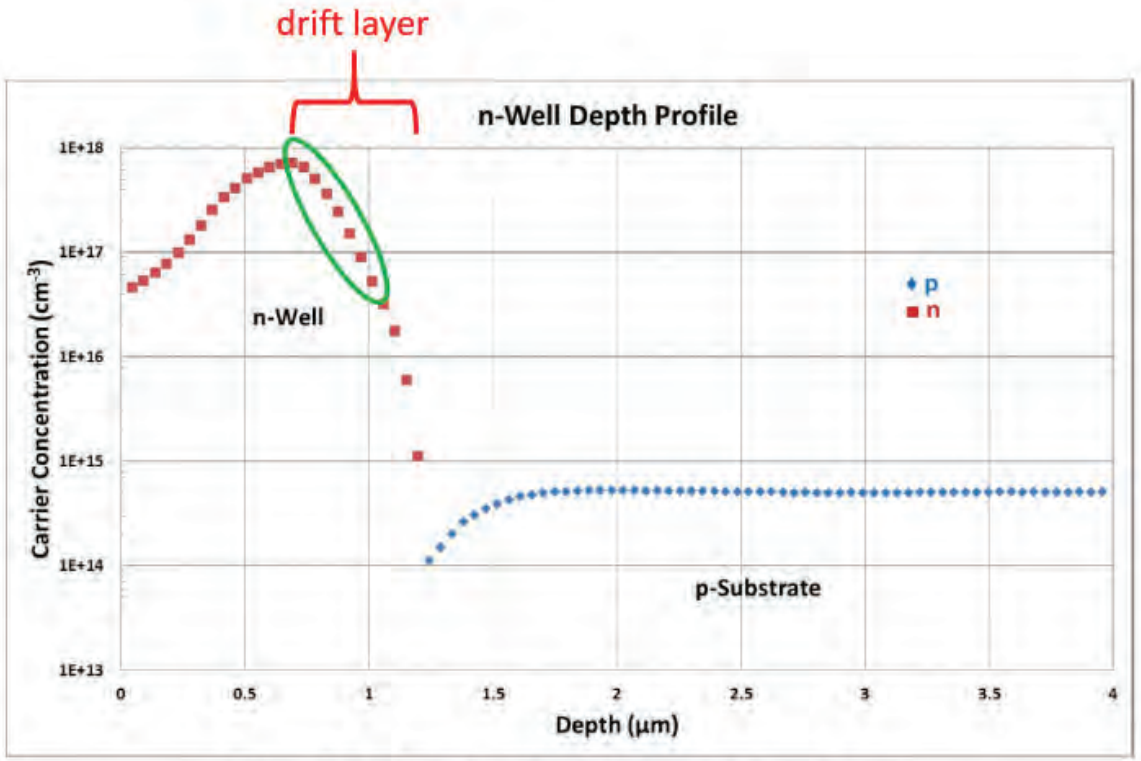


Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile

Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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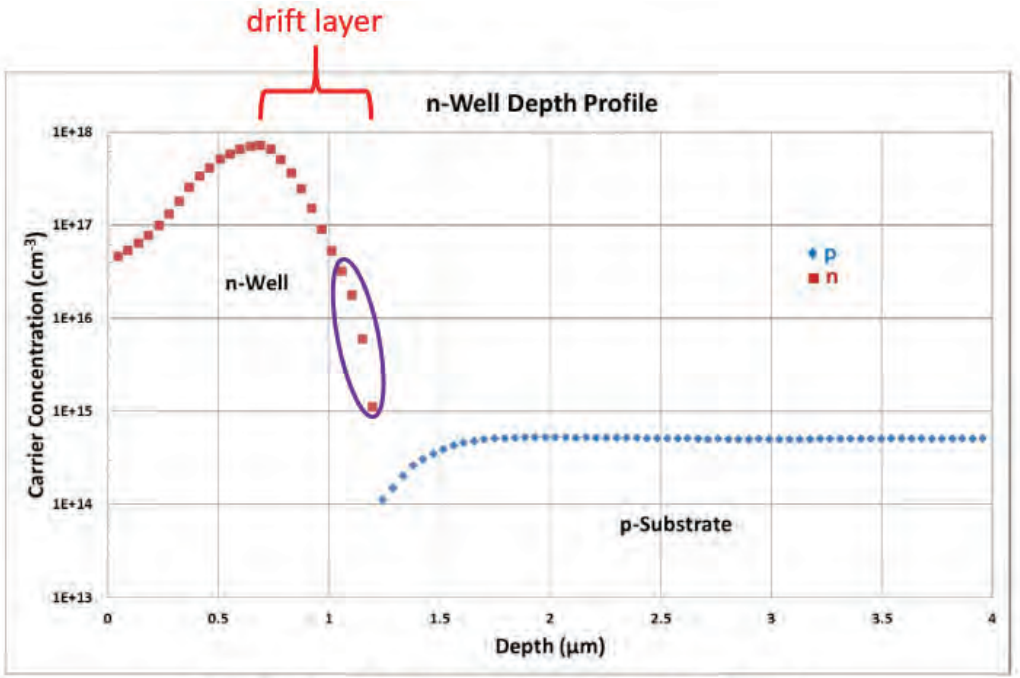
U.S. Patent No. 11,121,222	Accused Products
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants (annotated with purple oval below to indicate a region of relatively steeper slope in concentration, compared to the shallower region discussed for Claim 44, Element 4).  Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit C-4 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a CMOS semiconductor device. *See* Exhibit C-3, Claim 44, Preamble. The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit C-1 is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Dell-WD Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Dell-WD Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Dell-WD Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Dell-WD Accused Products contain similar features as the SanDisk 15 nm 16 GB NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 44, Element 4. Upon information and belief, the drift layer (*see* Exhibit C-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 5] at least one well region disposed in said single	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be obtained through

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Exhibit C-4 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 8,421,195	Accused Products
drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	discovery. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The Dell-WD Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 4; Exhibit C-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Elements 1, 5.

Exhibit C-5 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2022)

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include a semiconductor device. *See* Exhibit C-4, Claim 1, Preamble. The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit C-1 is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Dell-WD Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Dell-WD Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Dell-WD Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Dell-WD Accused Products contain similar features as the SanDisk 15 nm 16 GB NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-4, Claim 1, Element 4. The graded concentration of dopants observed via SRP analysis (*see* Exhibit C-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-4, Claim 1, Element 5. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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Exhibit C-5 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 9,190,502	Accused Products
dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The Dell-WD Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
11. The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-2, Claim 16.

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Exhibit C-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include an electronic system. *See* Exhibit C-1, Claim 1, Preamble; Exhibit C-4, Claim 1, Preamble. Each Dell-WD Accused Product is an electronic system, because a computer is an electronic system. The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit C-1 is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Dell-WD Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Dell-WD Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Dell-WD Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Dell-WD Accused Products contain similar features as the SanDisk 15 nm 16 GB NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 1, Element 2; Exhibit C-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 1, Element 3; Exhibit C-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 1, Element 4.
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 1, Element 5. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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U.S. Patent No. 11,316,014	Accused Products
at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 1, Element 6; Exhibit C-3, Claim 21, Element 6. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 2.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 5.

Exhibit C-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 15.
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 16.
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 17.

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U.S. Patent No. 11,316,014	Accused Products
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-WD Accused Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit C-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit C-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit C-1, Claim 9, Element 5. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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Exhibit C-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-WD Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit C-3, Claim 21, Element 6. *See also* SRP analysis reproduced at Exhibit C-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 26.
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 27.

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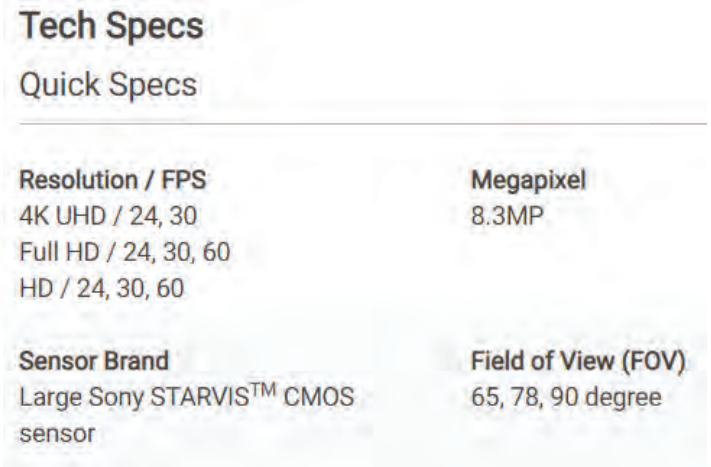
Exhibit C-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
region.	
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-WD Accused Products meet this limitation. *See* Exhibit C-3, Claim 28.

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Exhibits D-1 to D-6
Dell-Sony Accused Products

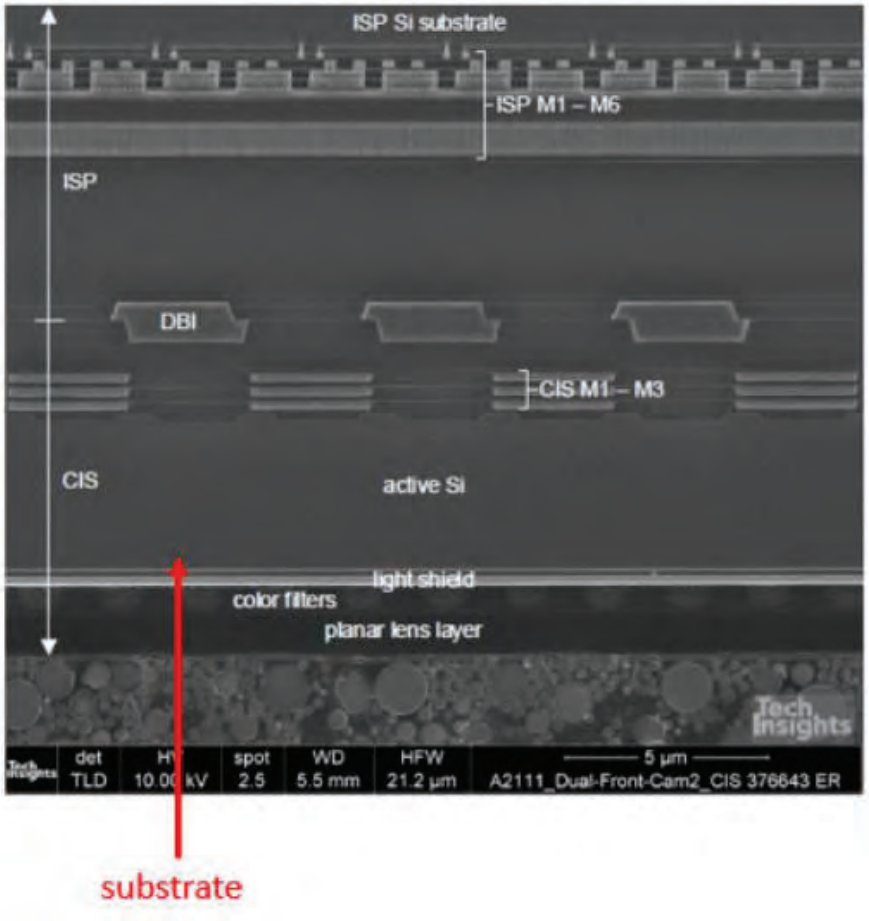
Exhibit D-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. Sony provides CMOS image sensors, and the Dell-Sony Accused Products include Sony CMOS image sensors, each of which is a semiconductor device. Sony Develops World's First[*1] Stacked CMOS Image Sensor Technology with 2-Layer Transistor Pixel Widens Dynamic Range and Reduces Noise by Approximately Doubling[*2] Saturation Signal Level[*3] Sony Semiconductor Solutions Corporation *See* https://www.sony-semicon.co.jp/e/news/2021/2021121601.html As an example, the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor is found in an Apple iPhone 11, and upon information and belief, this image sensor has similar components and functionality as the Sony CMOS image sensor in the Dell-Sony Accused Products. Usage of a Sony CMOS image sensor in Dell products is shown below, for example:  

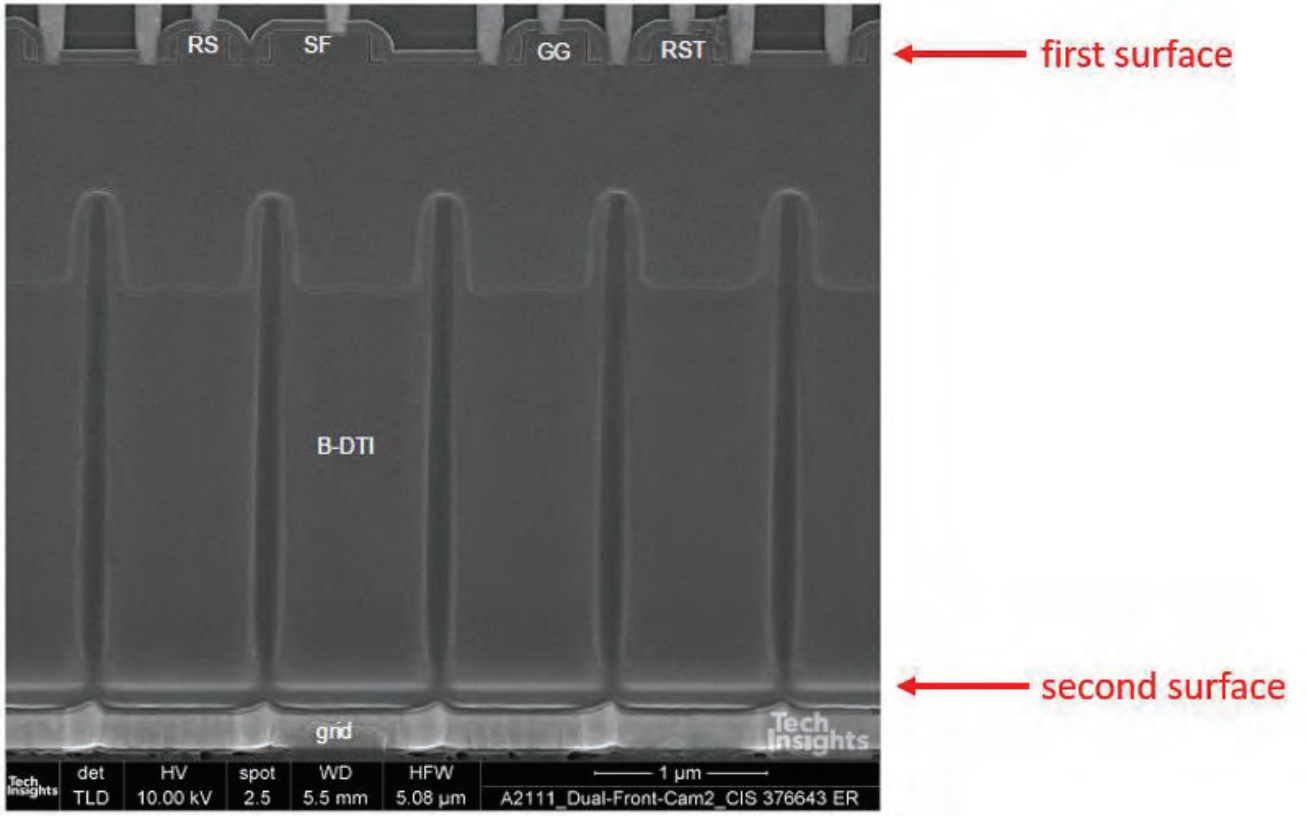
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U.S. Patent No. 10,510,842	Accused Products
	See https://deals.dell.com/en-us/productdetail/dtvv This representative Sony image sensor has been analyzed via tear-down, as explained below. The above Sony image sensor is discussed in this claim chart and other infringement contention claim charts (e.g., Exhibits D-2 through D-6) as an example of a Sony image sensor used in Dell-Sony Accused products. Upon information and belief, such a Sony image sensor is representative of Sony image sensors used in the Dell-Sony Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other Sony image sensors used in Dell-Sony Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, other Sony image sensors would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Therefore, upon information and belief, other Sony image sensors used in Dell-Sony Accused Products contain similar features as the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Sony Accused Products meet this limitation. For example, the Sony CMOS image sensor discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) and scanning capacitance microscopy (SCM), at the cross-section indicated below:

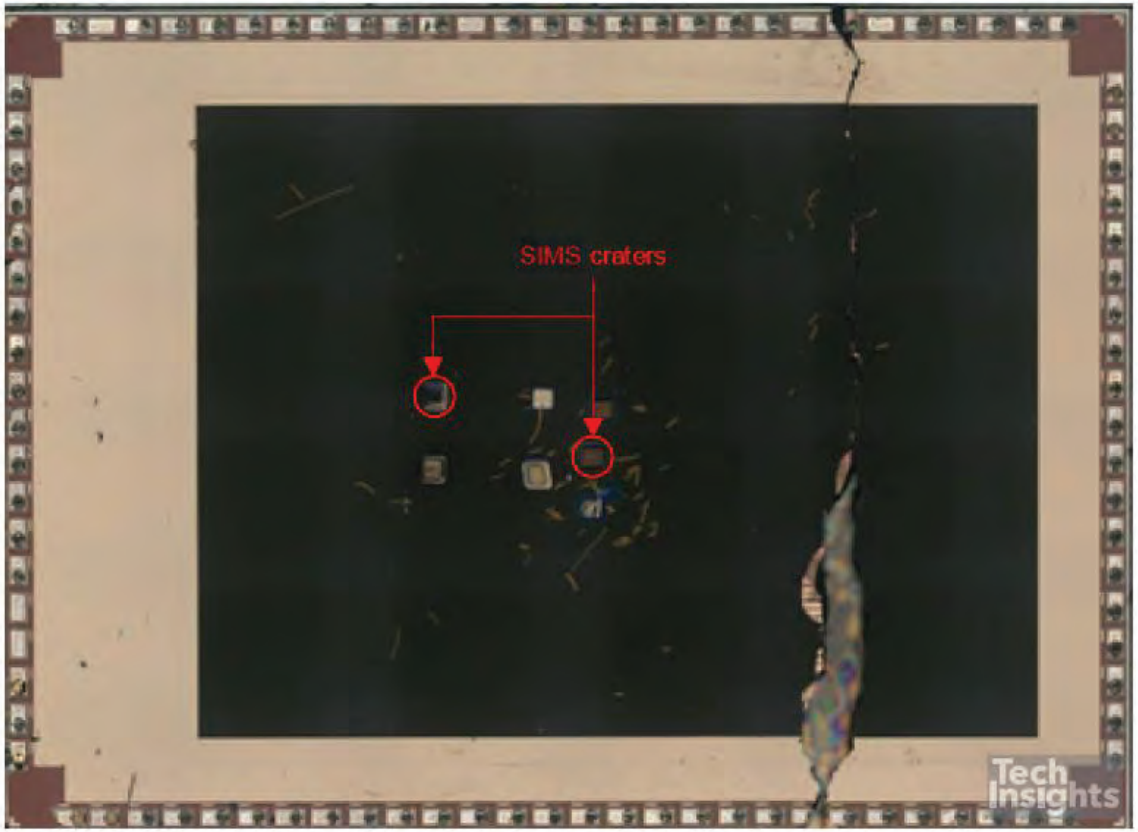
U.S. Patent No. 10,510,842	Accused Products
	 The SEM cross-sectional image below shows the image signal processor (ISP) / CMOS image sensor (CIS) die stack in the periphery region, with a direct bond interconnect (DBI) connecting the two wafers corresponding to the ISP and CIS, respectively:

U.S. Patent No. 10,510,842	Accused Products
	 The substrate has first and second surfaces, as shown in the following SEM cross-sectional image taken at the red dashed line labeled "A" and "SEM/SCM cross-section" in the first figure above:

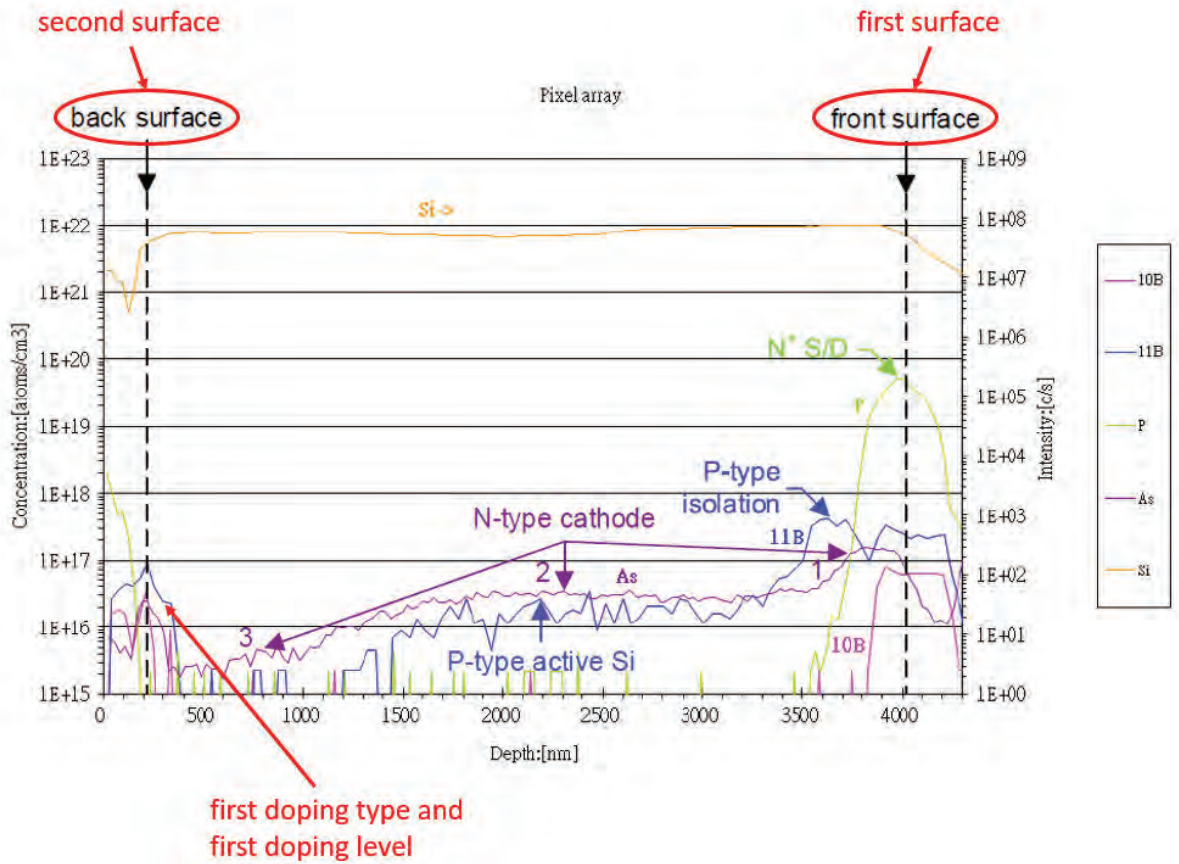
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U.S. Patent No. 10,510,842	Accused Products
	 Secondary ion mass spectroscopy (SIMS) was performed to analyze doping profiles. For example, a SIMS sample was used as shown below, with the location of SIMS craters annotated:

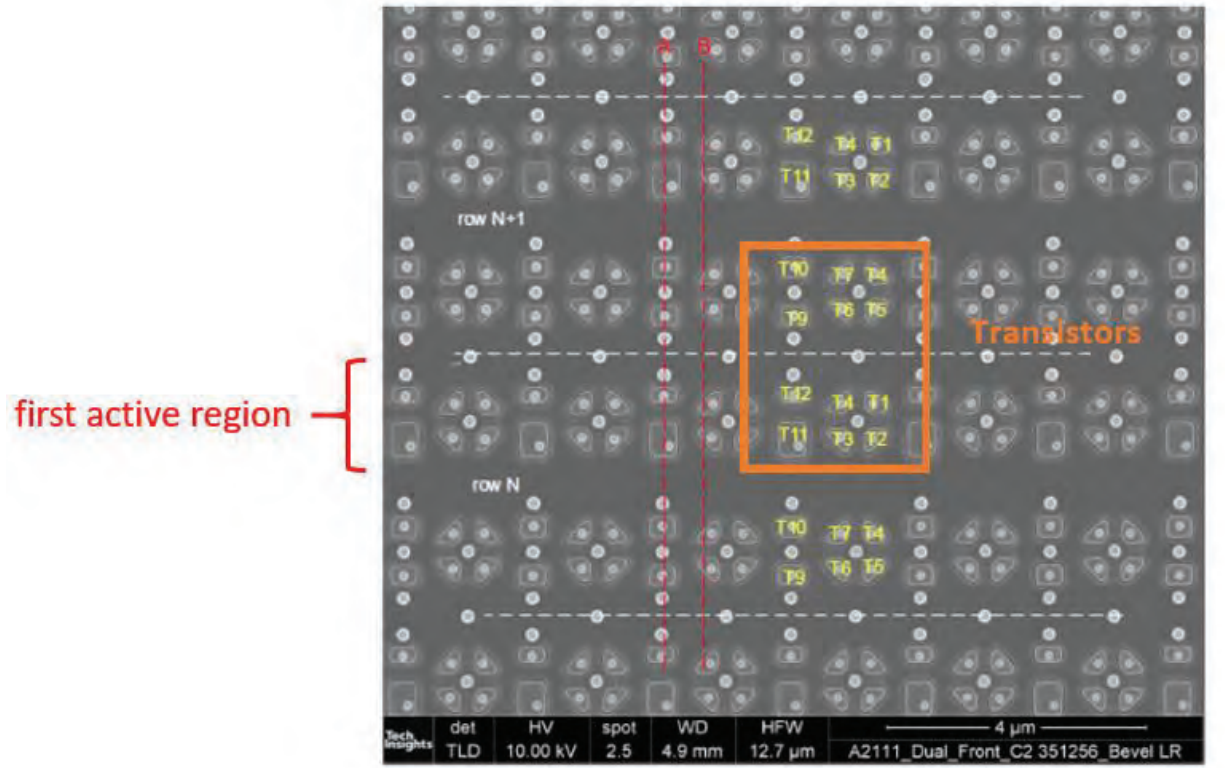
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U.S. Patent No. 10,510,842	Accused Products
	 The sample was prepared by removing the back layers down to the back of the active silicon. The SIMS crater for boron (B) analysis is 100 × 100 µm, and 80 × 80 µm for the remaining elements shown in the legend at the right side of the below graph.

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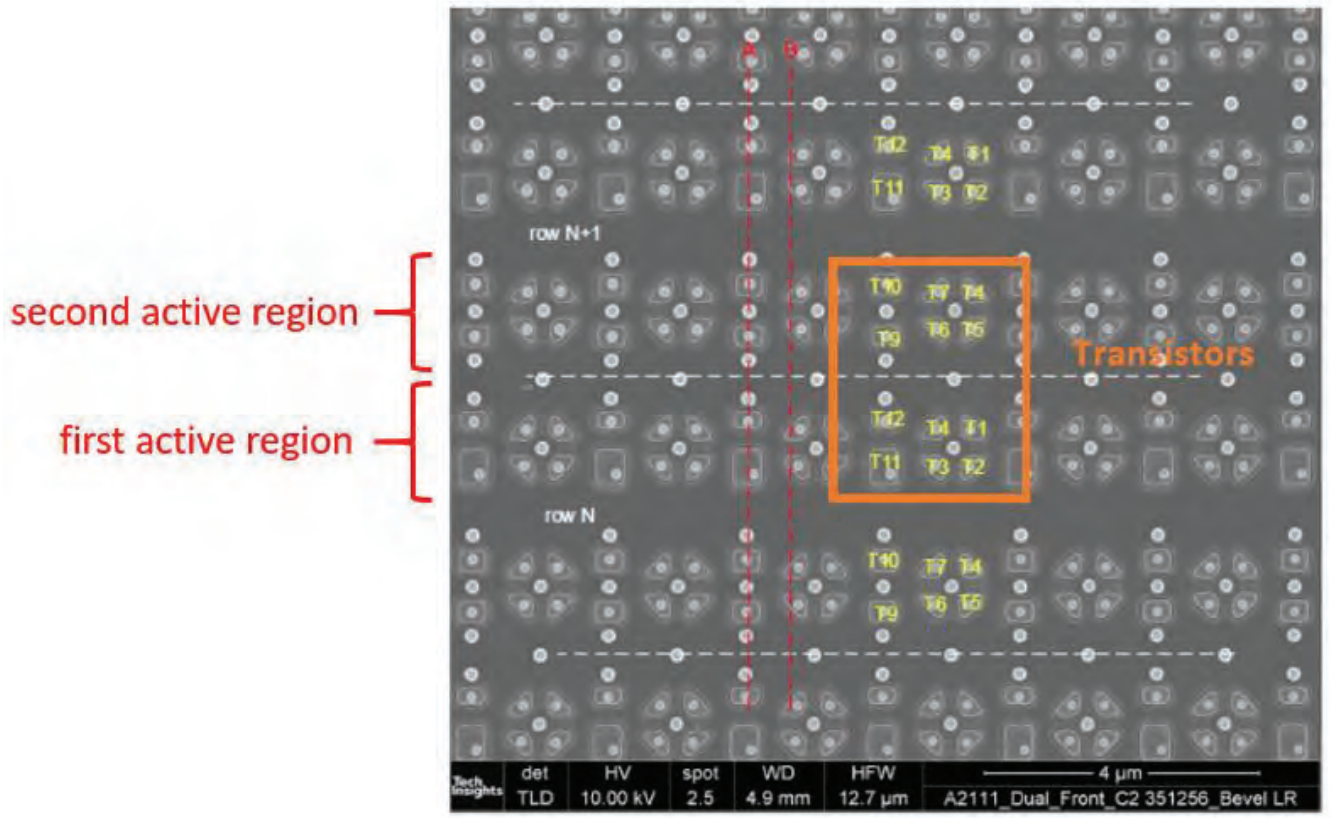
U.S. Patent No. 10,510,842	Accused Products
	 As shown above, the substrate is p-type (a first doping type) and has a first doping level.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. For example, the following scanning electron microscope (SEM) bevel image shows two adjacent rows of shared pixels, and thus shows first and second active regions. Transistors are formed in the first active region as shown below. Upon information and belief, the first active region (shown below) is n-type (a second doping type opposite in conductivity to the first doping type).

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U.S. Patent No. 10,510,842	Accused Products
	 The first active region is disposed adjacent the first surface of the substrate, as shown in the following SEM cross-sectional image discussed above for Element 1:

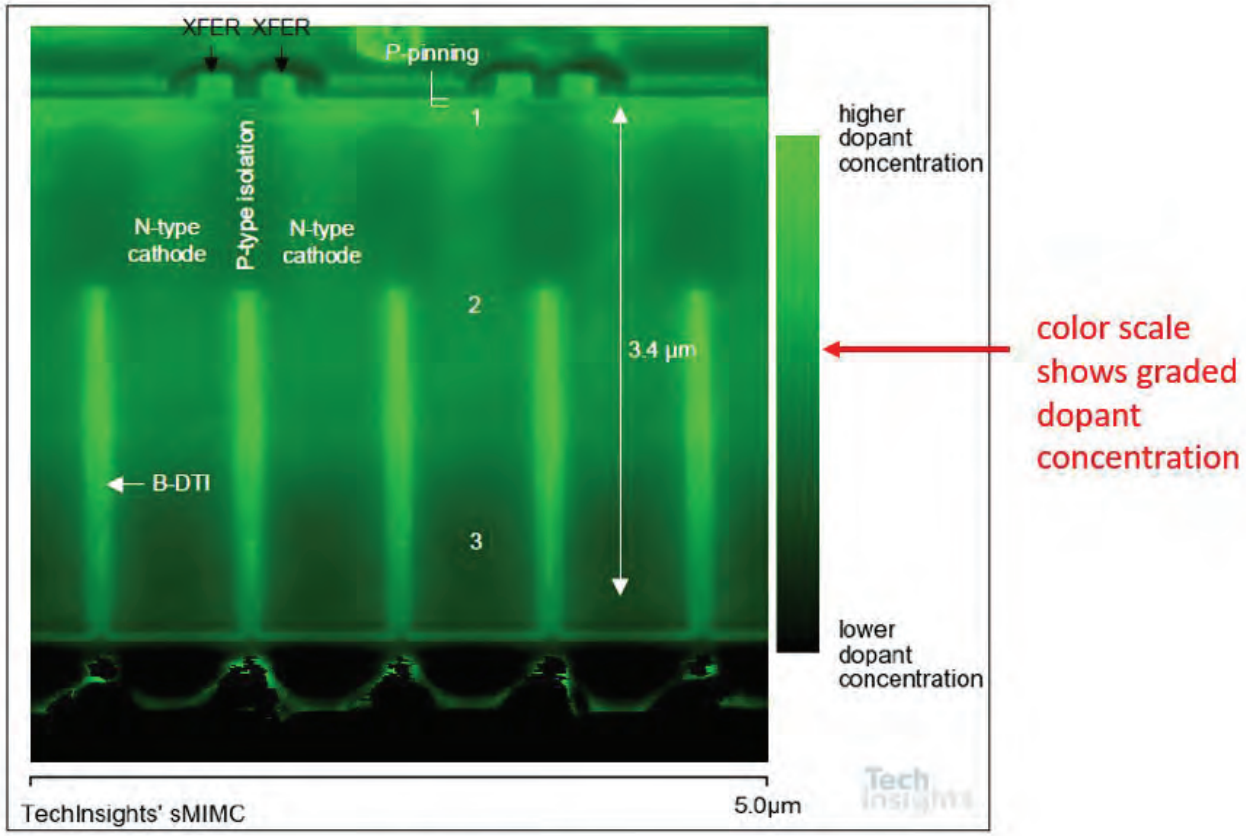
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U.S. Patent No. 10,510,842	Accused Products
	
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. For example, this is shown by the following SEM image of the Sony CMOS image sensor discussed above for Element 2. As discussed above for Element 2, the SEM image shows two adjacent rows of shared pixels, and thus shows first and second active regions.

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[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first	The Dell-Sony Accused Products meet this limitation. For example, this is shown by the SEM and scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis. SCM/SMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/SMIM maps taken from Dell-Sony Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black

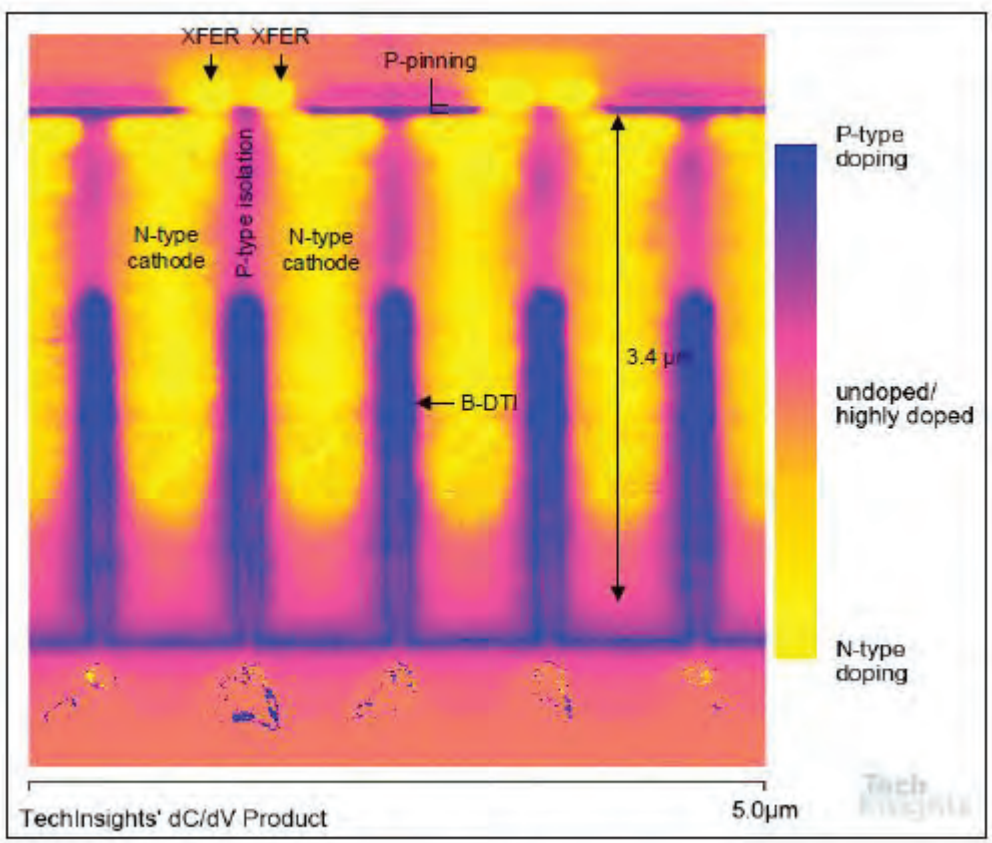
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surface to the second surface of the substrate.	corresponds to lower dopant concentration. Likewise, the SCM image below shows doping concentration and doping type as indicated in the legend to the right.



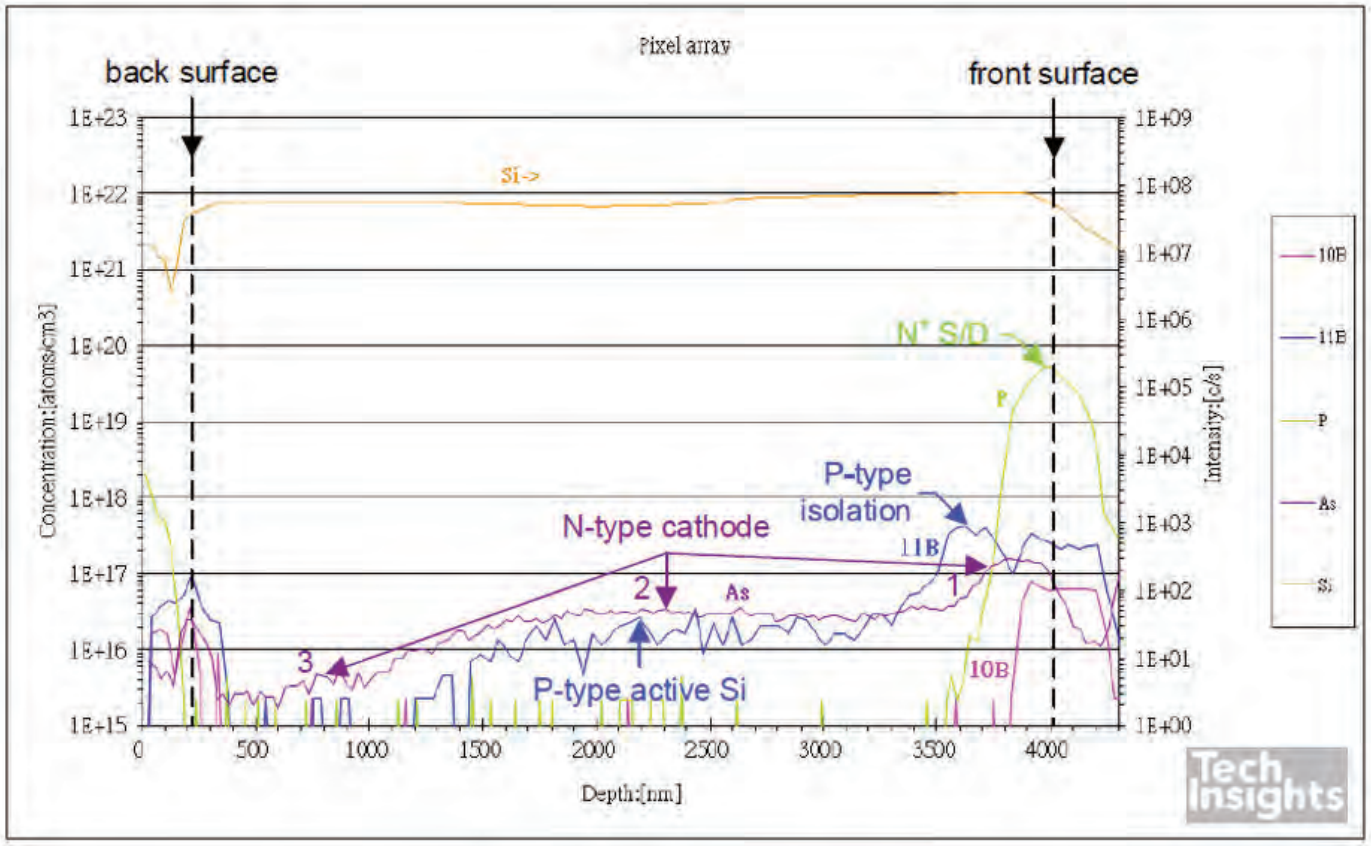
SMIM-C

U.S. Patent No. 10,510,842	Accused Products



SCM

As shown by the slope of the blue plot (boron-11, which is p-type) and the dark purple plot (arsenic, which is n-type) in the SIMS graph below, at least a portion of at least one of the first and second active regions has at least one graded dopant concentration to aid carrier movement from the front surface (first surface) to the back surface (second surface) of the substrate.

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	 For example, at least one downward sloped portion is shown in each of the boron-11 and arsenic plots above, viewed from right (less depth, relative to the first surface discussed above) to left (more depth, relative to the first surface).
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The substrate of the semiconductor device of the Dell-Sony Accused Products is a p-type substrate, as discussed above for Claim 1, Element 1.
5. The semiconductor device of claim 1, wherein the first active region and second active region	The Dell-Sony Accused Products meet this limitation. Upon information and belief, the first active region and second active region contain NMOS transistors (n-channel devices) or PMOS transistors (p-channel devices).

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contain one of either p-channel and n-channel devices.	
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. Upon information and belief, the first active region and second active region are each separated by at least one isolation region to avoid one pixel electrically interfering with an adjacent pixel. Information about isolation regions in Dell-Sony Accused Products is in the possession of the Dell Defendants and is expected to be obtained through discovery.
8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, for the Dell-Sony Accused Products, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Dell-Sony Accused Products. Information about the fabrication process for Dell-Sony Accused Products, including usage of an ion implantation process, is in the possession of the Dell Defendants and is expected to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of the Dell Defendants and are expected to be obtained through discovery.
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of the Dell Defendants and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 4.

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U.S. Patent No. 10,510,842	Accused Products
of the first active region or second active region; and	
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 2.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 5.
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the Dell-Sony Accused Products meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Dell-Sony Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Preamble and Elements 2-3 (discussing CMOS). CMOS transistors require a source, a drain, a gate, and a channel region.

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U.S. Patent No. 10,510,842	Accused Products
and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	

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Exhibit D-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* Exhibit D-1, Claim 1, Preamble. The Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor referenced in Exhibit D-1 for tear-down analysis is discussed in this claim chart and other infringement contention claim charts as an example of an image sensor representative of the Dell-Sony Accused Products. Upon information and belief, such a Sony image sensor is representative of image sensors used in the Dell-Sony Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other image sensors used in Dell-Sony Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, other image sensors would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Therefore, upon information and belief, other image sensors used in Dell-Sony Accused Products contain similar features as the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor, and function in a similar way, with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.

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Exhibit D-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	Upon information and belief, the Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement. Information about well regions and doping in such regions is in the possession of the Dell Defendants, and is expected to be obtained through discovery.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 2.
4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 5.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 7.
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 8.
8. The semiconductor device of claim 1, wherein the first and second	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Elements 1-3.

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Exhibit D-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
active regions are formed adjacent the first surface of the substrate.	
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 5 (SIMS graph showing p-type boron-11 doping).
13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 18.
19. The semiconductor device of claim 1, wherein the device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products meet include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 9, Element 2.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 9, Element 3.

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Exhibit D-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
which transistors can be formed in the surface thereof;	
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 6.
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 2.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 5.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 7.

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Exhibit D-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 8.
36. The semiconductor device of claim 20, wherein the device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.

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Exhibit D-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a VLSI semiconductor device. The Sony image sensor discussed for claim 1 of Exhibit D-1 is a semiconductor device (*see* Exhibit D-1, Claim 1, Preamble) and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Dell Defendants and are expected to be obtained through discovery. The Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor referenced in Exhibit D-1 is discussed in this claim chart and other infringement contention claim charts as an example of an image sensor representative of the Dell-Sony Accused Products. Upon information and belief, such a Sony image sensor is representative of image sensors used in the Dell-Sony Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other image sensors used in Dell-Sony Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, other image sensors would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Therefore, upon information and belief, other image sensors used in Dell-Sony Accused Products contain similar features as the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.

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active region or second active region;	
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 5. For example, referencing the SIMS graph discussed at Exhibit D-1, Claim 1, Element 5 and shown below, there are no active regions at the left side of the graph, e.g., at depths of less than about 1500 nm. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	Upon information and belief, the Dell-Sony Accused Products meet this limitation. Details regarding well regions and transistors of the Dell-Sony Accused Products are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 2.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 5; Exhibit D-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. *See* above at Claim 1, Element 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 7.

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active region are each separated by at least one isolation region.	
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.
19. The VLSI semiconductor device of claim 1, wherein the device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	Upon information and belief, the Dell-Sony Accused Products meet this limitation.

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U.S. Patent No. 11,121,222	Accused Products
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 9, Element 2.
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
[Claim 21, Element 6] at least one well region adjacent to the	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-2, Claim 1, Element 6. As shown by SIMS analysis (*see* Exhibit D-1, Claim 1, Element 5), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination

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first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	thereof. For example, the quasilinear nature of the concentration is shown in the SIMS graph discussed at Exhibit D-1, Claim 1, Element 5. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 2.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 5.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 8.

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graded dopant is fabricated with an ion implantation process.	
37. The VLSI semiconductor device of claim 21, wherein the device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	Upon information and belief, the Dell-Sony Accused Products meet this limitation.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* Exhibit D-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.

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[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement. ; *see* above at Claim 21, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 21, Element 5. The SIMS graph discussed at Exhibit D-1, Claim 1, Element 5 shows at least one graded dopant acceptor concentration (e.g., boron-11 concentration) as claimed. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.

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at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	

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Exhibit D-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include an electronic system. *See* Exhibit D-1, Claim 1, Preamble; Exhibit D-1, Claim 1, Preamble. Each Dell-Sony Accused Product is an electronic system, because a computer is an electronic system. The Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor referenced in Exhibit D-1 is discussed in this claim chart and other infringement contention claim charts as an example of an image sensor representative of the Dell-Sony Accused Products. Upon information and belief, such a Sony image sensor is representative of image sensors used in the Dell-Sony Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other image sensors used in Dell-Sony Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, other image sensors would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Therefore, upon information and belief, other image sensors used in Dell-Sony Accused Products contain similar features as the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 2; Exhibit D-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 3; Exhibit D-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 4.

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Exhibit D-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 6; Exhibit D-3, Claim 21, Element 6. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 2.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 4.
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 8.

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U.S. Patent No. 11,316,014	Accused Products
the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 13.
19. The system of Claim 1, wherein the at least one semiconductor device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	Upon information and belief, the Dell-Sony Accused Products meet this limitation.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit D-1, Claim 9, Element 2.

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U.S. Patent No. 11,316,014	Accused Products
and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit D-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit D-1, Claim 9, Element 5. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit D-3, Claim 21, Element 6. *See* Exhibit D-1 Claim 1, Element 5 discussing electrical characterization of the accused products using SCM/SMIM analysis and demonstration of carrier movement.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 23.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 25.

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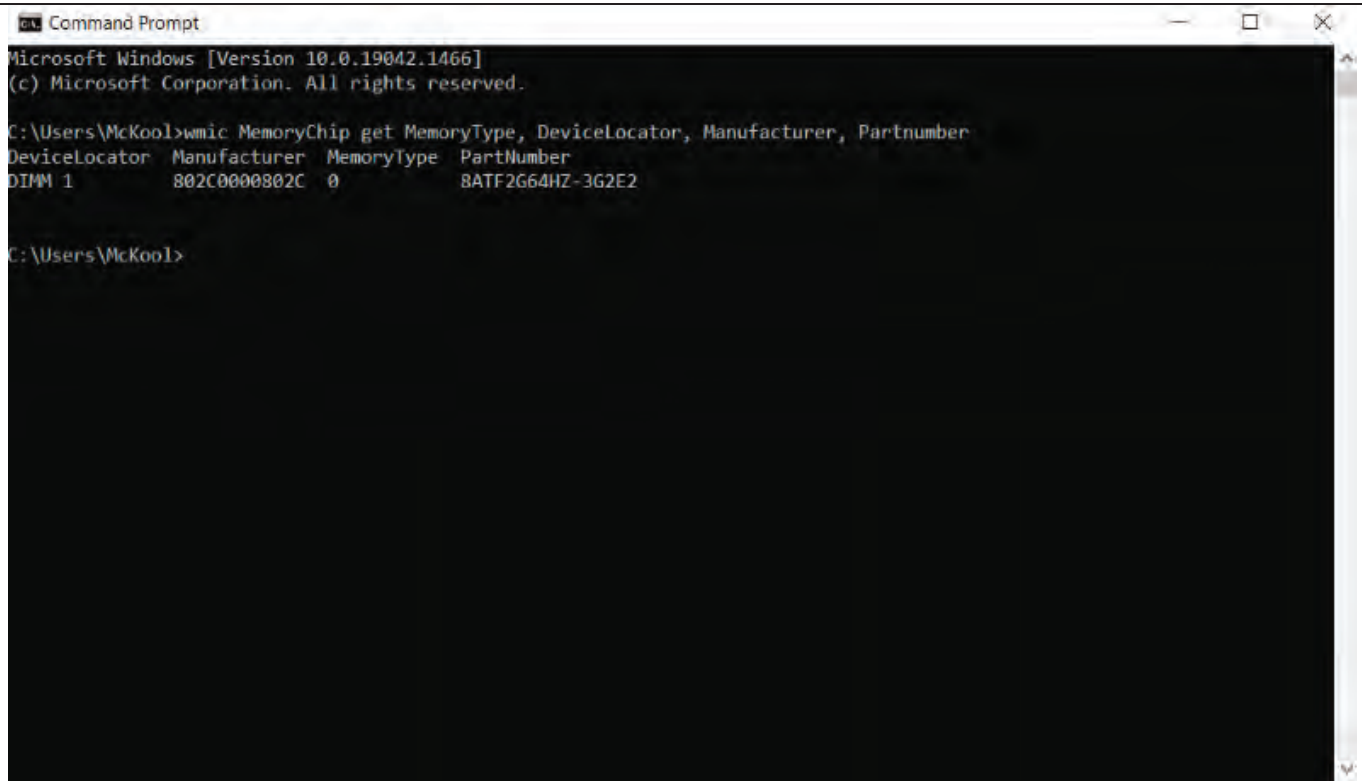
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least one of either p-channel and n-channel devices.	
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 28.

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Exhibits E-1 to E-6
Dell-Micron DRAM
Accused Products

Exhibit E-1 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a semiconductor device. For example, the Dell-Micron-DRAM Accused Products include a dynamic random access memory (DRAM) manufactured by Micron, and a DRAM is a semiconductor device, e.g., because it includes semiconductor-based components. An example Dell Accused Product was analyzed and found to include Micron DRAM, as described below. A Dell Latitude 5520 laptop computer containing an Intel i7 processor was tested:  Details regarding the memory in the above computer were determined. For example, using the "wmic MemoryChip" command (described at, e.g., https://www.windowscentral.com/how-get-full-memory-specs-speed-size-type-part-number-form-factor-windows-10), the following results from running the command show the presence of Micron DRAM within the Dell computer:



The DRAM referenced by the above part number is a Micron DRAM:

Micron Technology 8ATF2G64HZ-3G2E2 16GB

Price and performance details for the Micron Technology 8ATF2G64HZ-3G2E2 16GB can be found below. This is made using thousands of PerformanceTest benchmark results and is updated daily.

- The graphs shows the relative performance of the ram module compared up to 9 other common ram modules of same type. For DDR3 and DDR4, the values will be from systems using newer Intel CPUs where available.
- If pricing history data is available for the ram module, a chart with be created charting price changes.
- The last graph shows up to the last 5 baselines we have received for this particular ram module. Both Intel and AMD results are shown.

See https://www.memorybenchmark.net/ram.php?ram=Micron+Technology+8ATF2G64HZ-3G2E2+16GB&id=15773

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	 *See* https://www.newark.com/micron/mta8atf2g64hz-3g2e2/ram-module-ddr4-sodimm-16gb-25/dp/98AH1179 Upon information and belief, the above Micron DRAM is a representative example of various Micron DRAMs present in various Dell-Micron-DRAM Accused Products. Details regarding specific Micron DRAMs in Dell Accused Products are in the possession of the Dell Defendants and are expected to be obtained through discovery. A 20 nm node Micron MT58K256M32JA-100:A GDDR5X has been analyzed via tear-down and is described in this claim chart and other infringement contention claim charts (e.g., Exhibits E-1 through E-6), as explained below, as a representative example of the Dell-Micron-DRAM Accused Products. Upon information and belief, other Micron DRAMs would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, other DRAMs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Therefore, upon information and belief, other Dell-Micron-DRAM Accused Products contain similar features as the GDDR5X DRAM, and function in a similar way, with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Micron-DRAM Accused Products include a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, a die of the Micron DRAM discussed above for the preamble of claim 1 is shown below:

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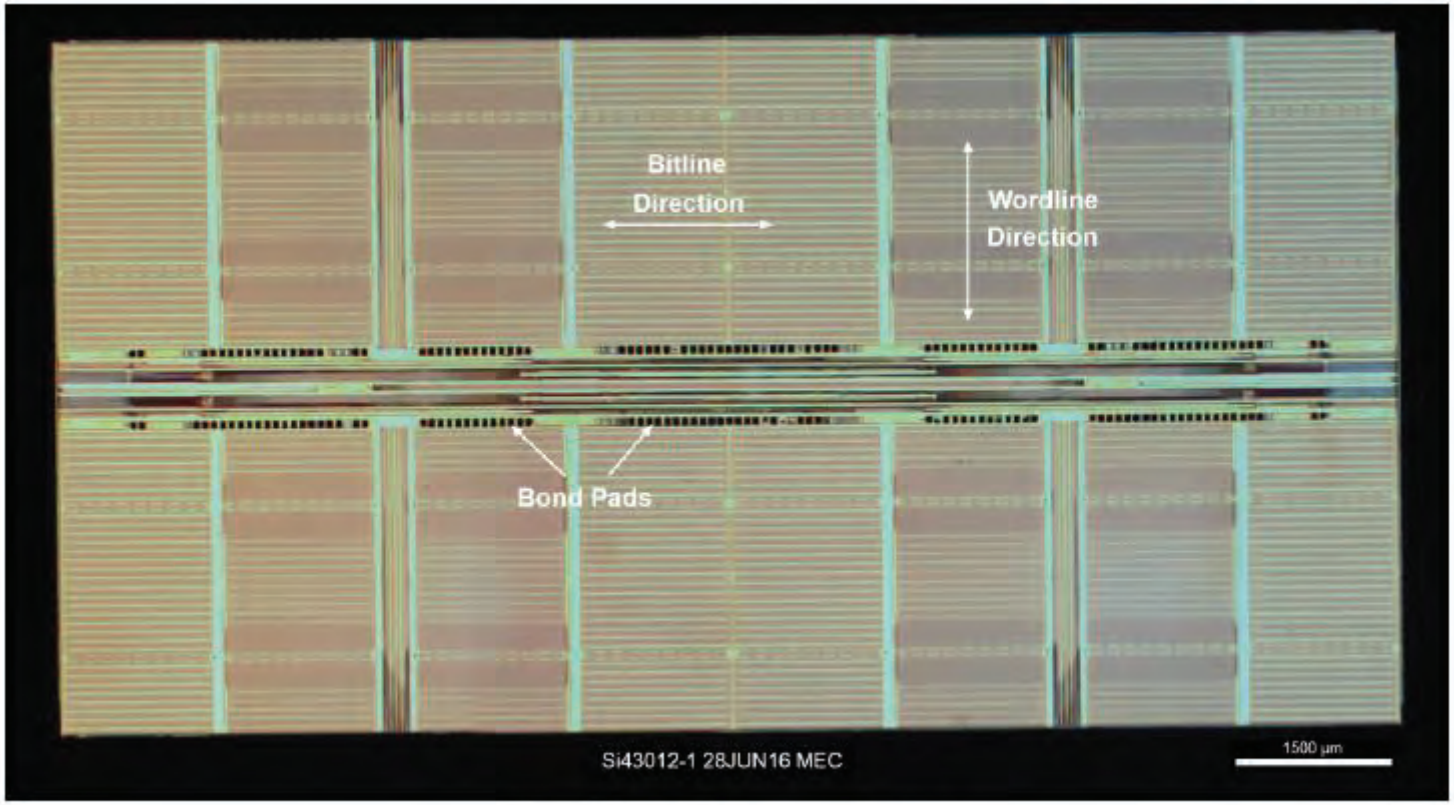


Figure 1.2.1: Die photograph

The following image of a cross-section of the flash memory die, obtained through scanning electron microscopy (SEM), shows the die having a thickness of 145 µm in this example. The DRAM die includes a substrate having first and second surfaces, as shown below:

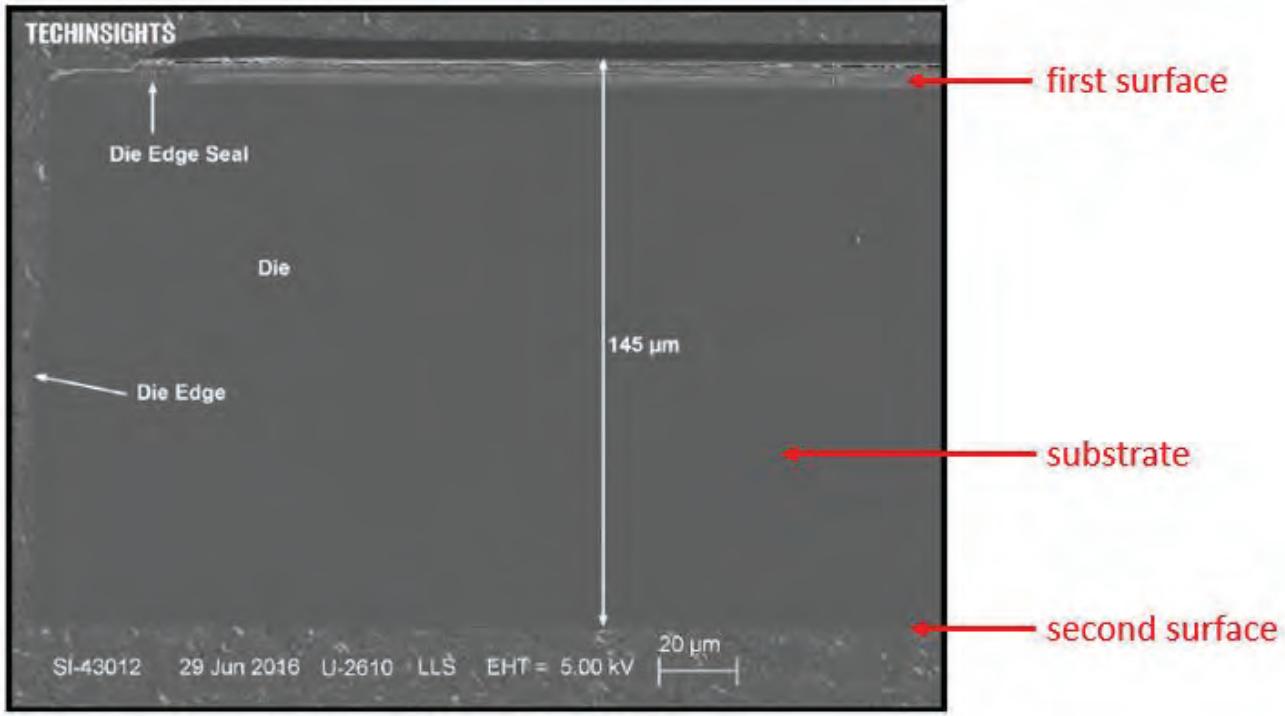
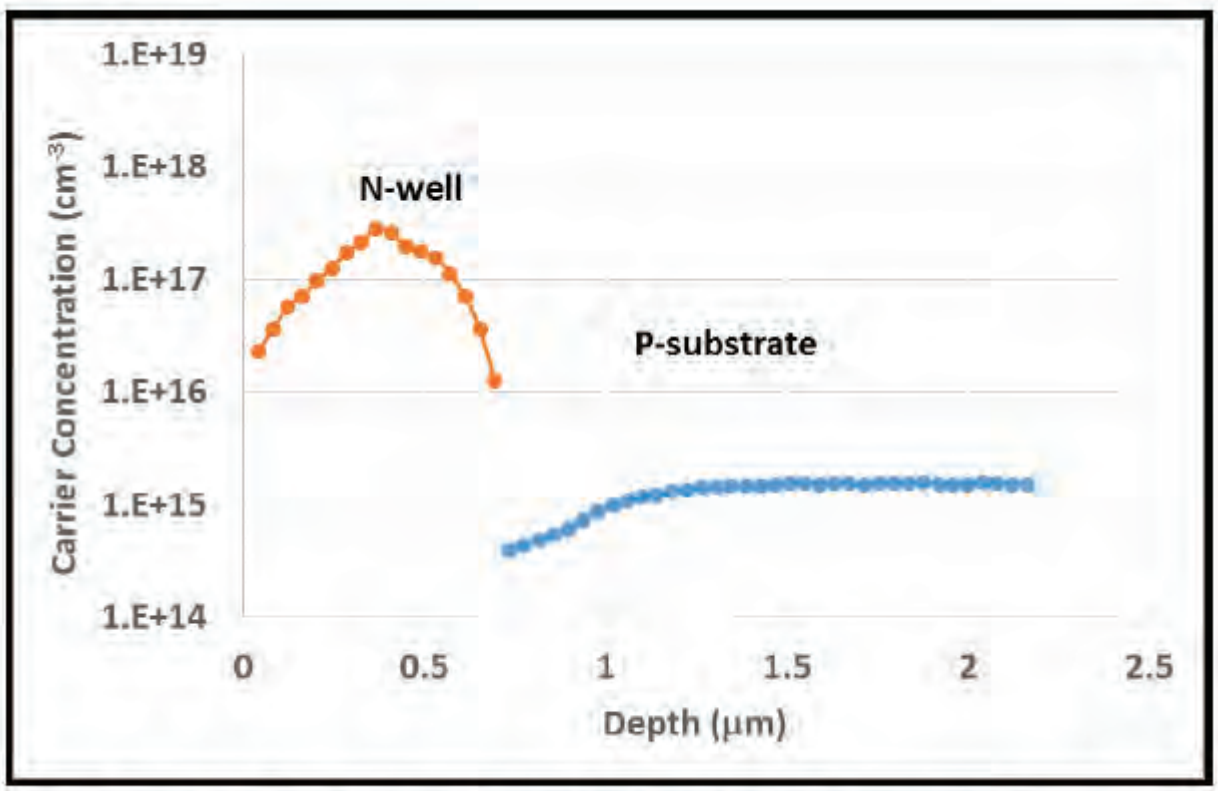


Figure 1.2.5: Die thickness (SEM)

A thickness (depth) of, e.g., 145 µm is consistent with the presence of a substrate.

Spreading resistance profile (SRP) analysis conducted on the DRAM shows that the substrate is p-type (a first doping type) and has a first doping level (*see* concentration of p-type substrate in below graph).

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	 Figure 2.1.2: Spreading resistance profile of a peripheral n-well
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products include a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, in accordance with a first mapping (Mapping A), the following cross-sectional image (labeled Figure 2.1.5) of a portion of the peripheral region (between DRAM arrays) of the Micron DRAM discussed above, obtained through scanning electron microscopy (SEM), shows a first active region as claimed:

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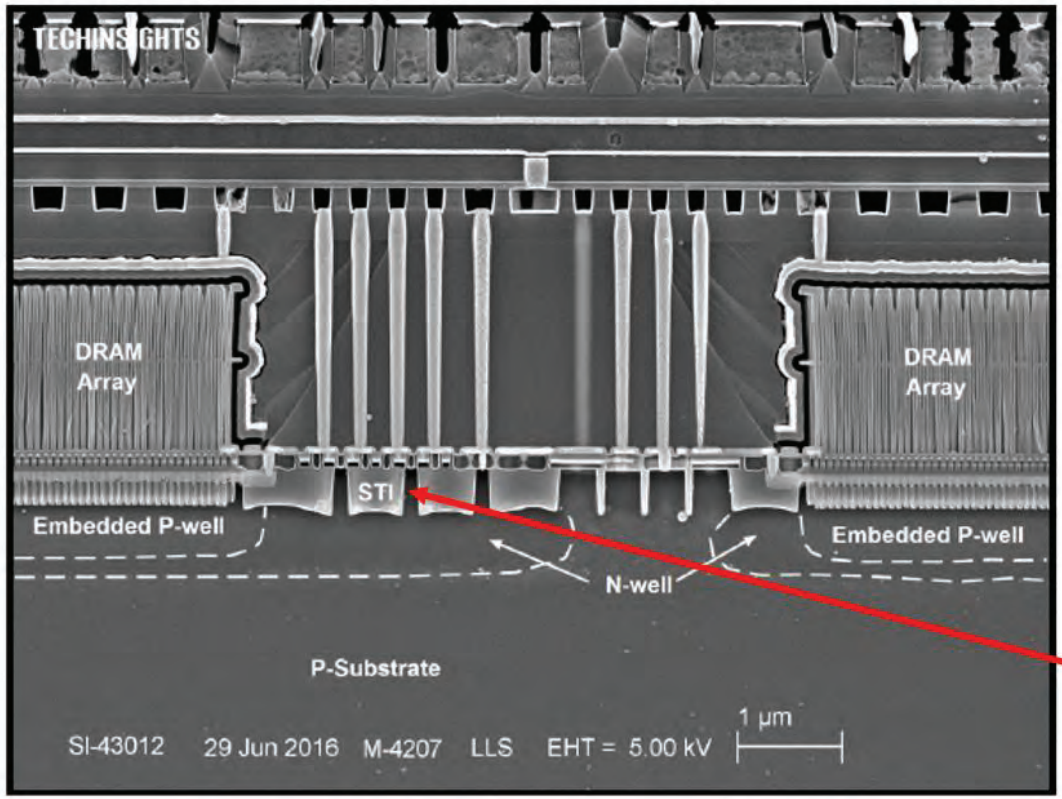


Figure 2.1.5: DRAM array well structure (SEM)

Upon information belief, a PMOS transistor is above the first active region, and thus the first active region is a region within which transistors can be formed. For example, upon information and belief, the gate of such a transistor is visible above the first active region in the above image. As shown in the above image, the first active region is disposed adjacent the first surface of the substrate.

As another example, in accordance with a second mapping (Mapping B), the following SEM cross-sectional image (labeled Figure 5.4.1) of another portion of the peripheral region of the Micron DRAM discussed above shows a first active region as claimed:

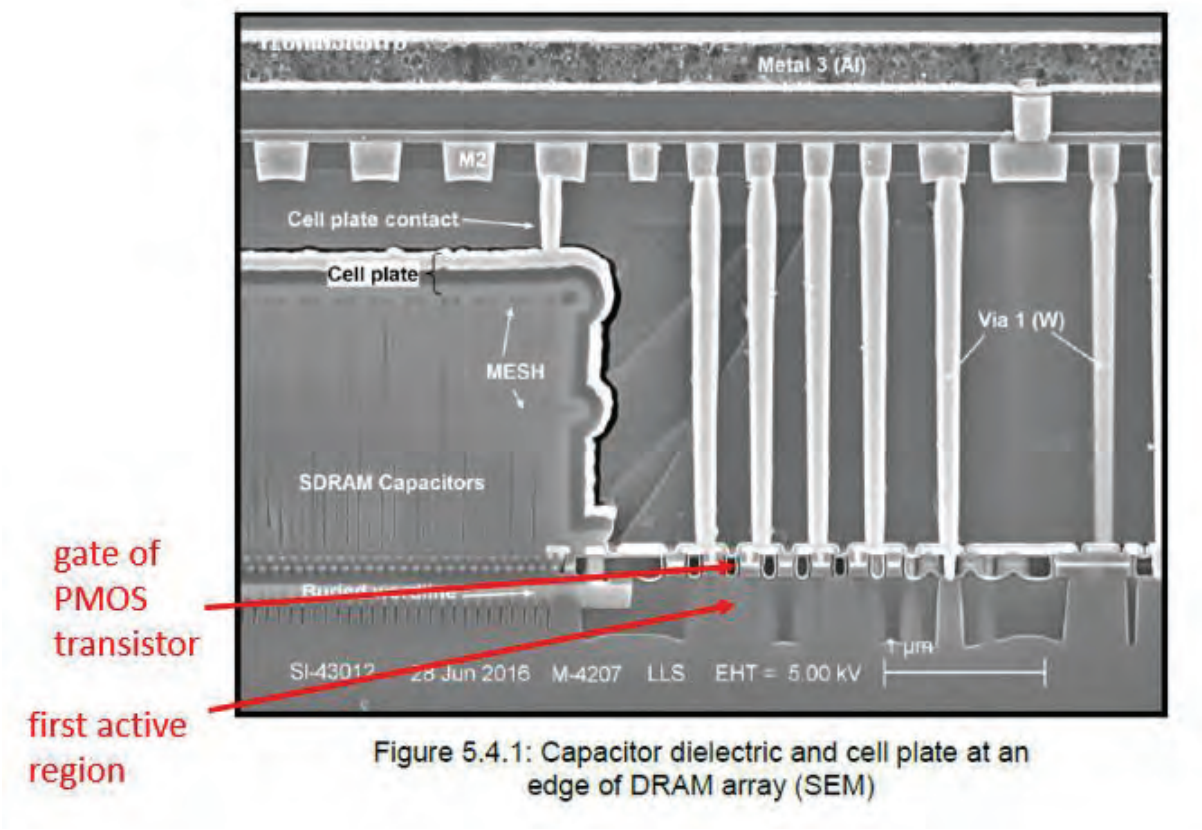
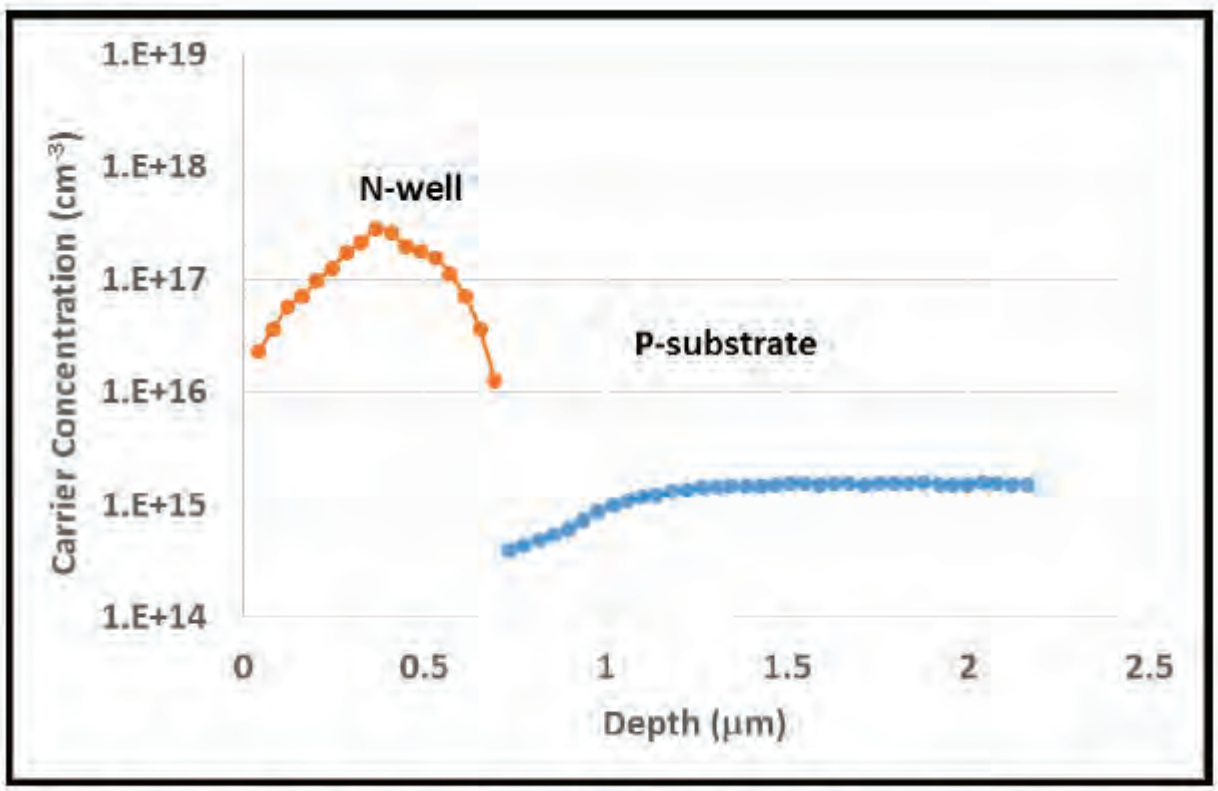


Figure 5.4.1: Capacitor dielectric and cell plate at an edge of DRAM array (SEM)

Upon information belief, a PMOS transistor is above the first active region, and thus the first active region is a region within which transistors can be formed. For example, the gate of such a transistor is shown above the first active region in the above image. As shown in the above image, the first active region is disposed adjacent the first surface of the substrate.

Under both Mapping A and Mapping B, the first active region has a second doping type (e.g., n-type) opposite in conductivity to the first doping type (p-type), e.g., as PMOS transistors are formed in n-wells. The n-type doping of the n-well is also shown in the following SRP graph.

	 Figure 2.1.2: Spreading resistance profile of a peripheral n-well The n-well shown above contains the first active region which is n-type.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, in accordance with Mapping A, a second active region as claimed is shown in the below SEM image (labeled Figure 2.1.5):

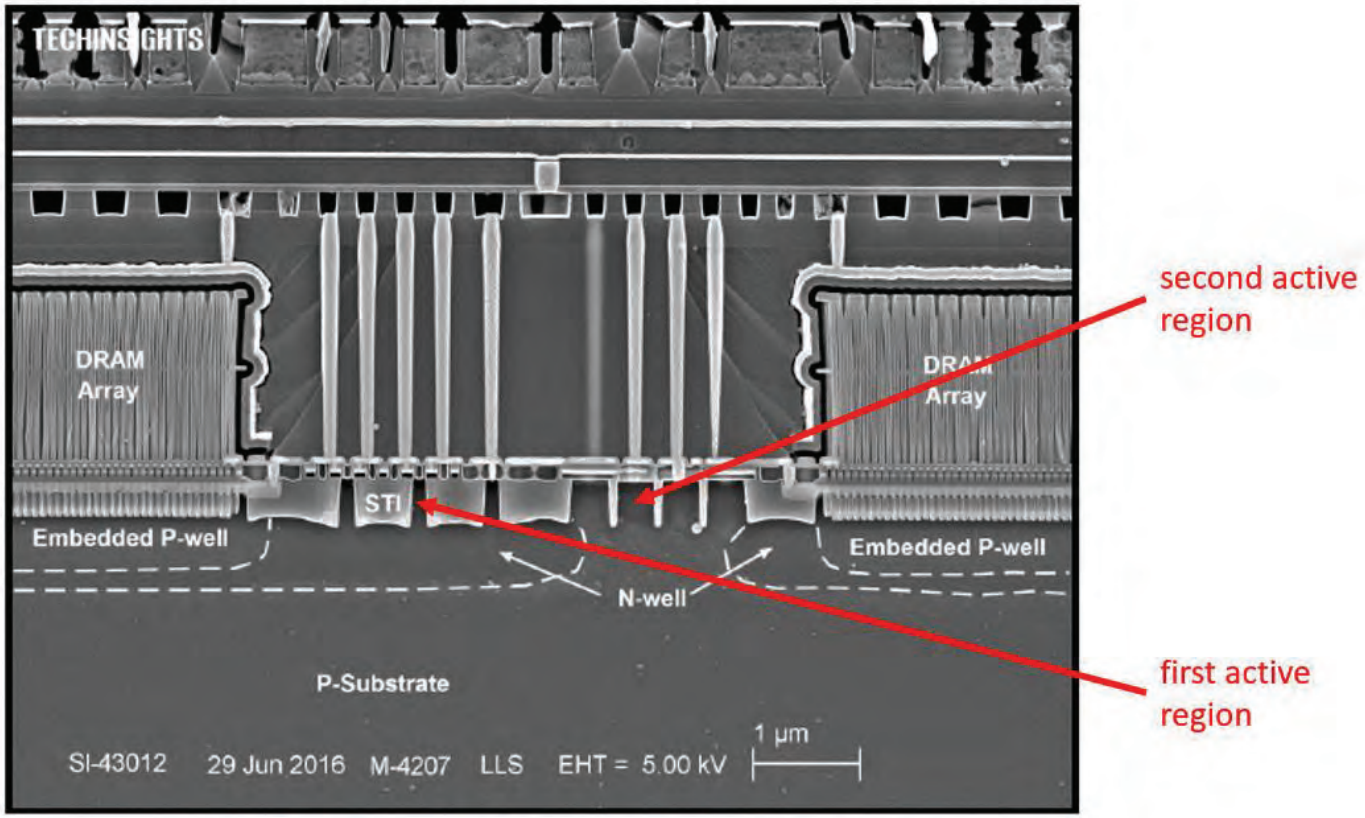
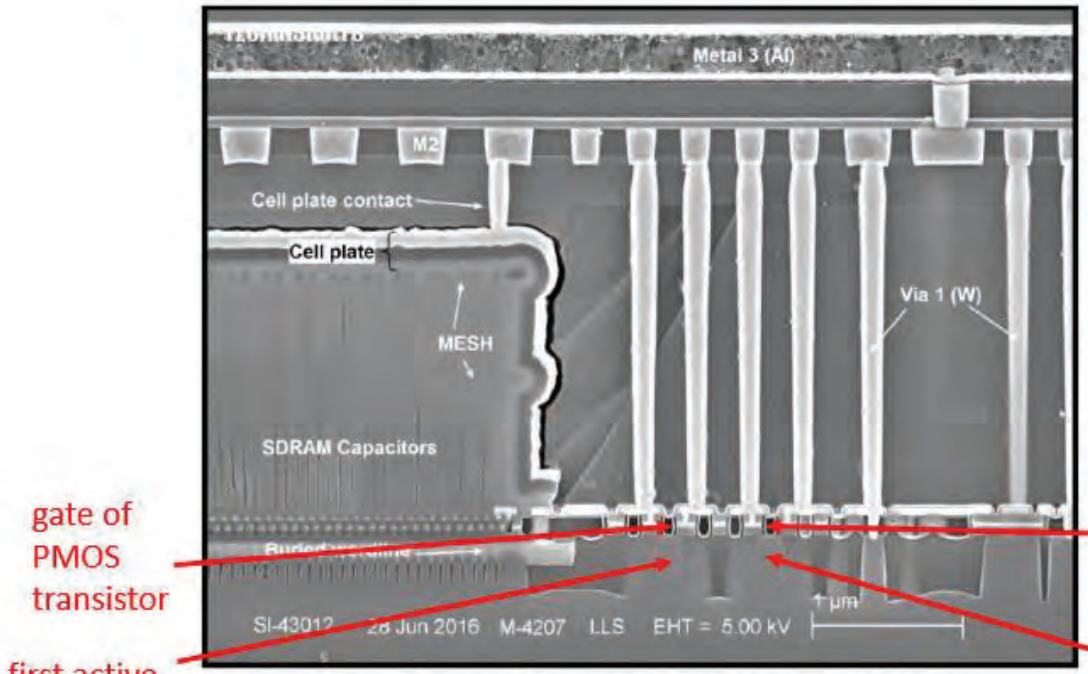


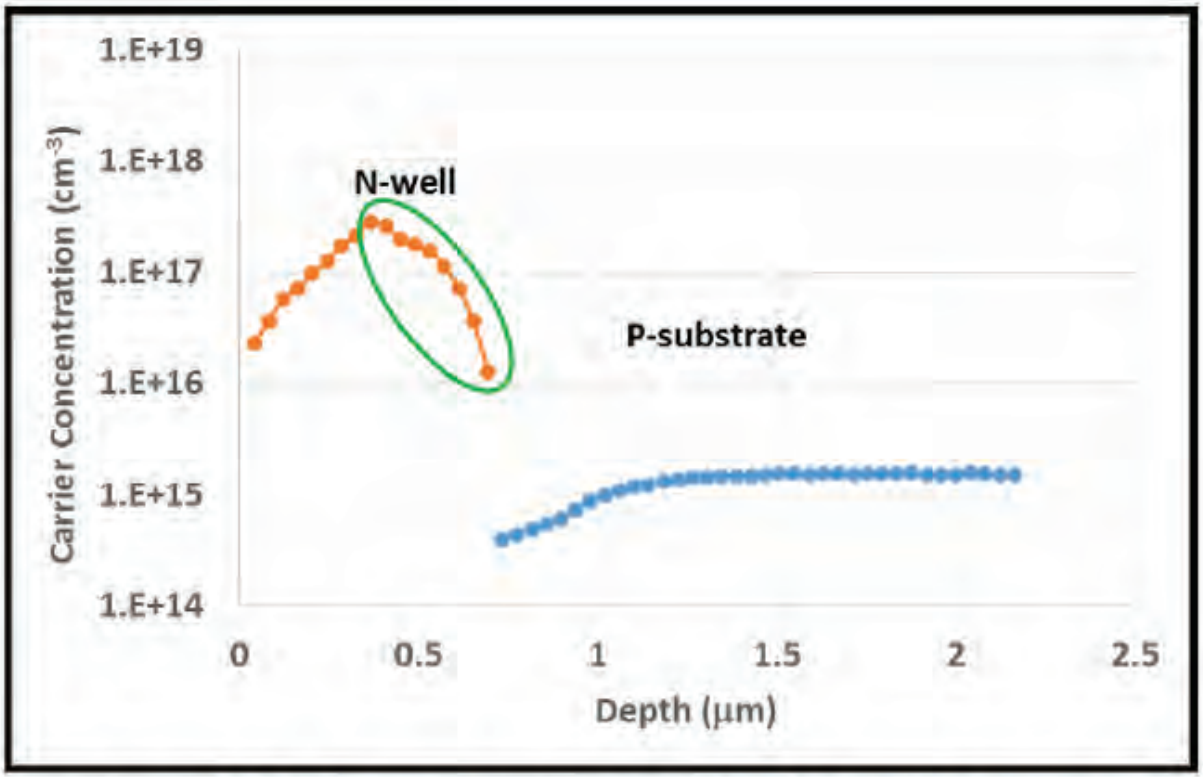
Figure 2.1.5: DRAM array well structure (SEM)

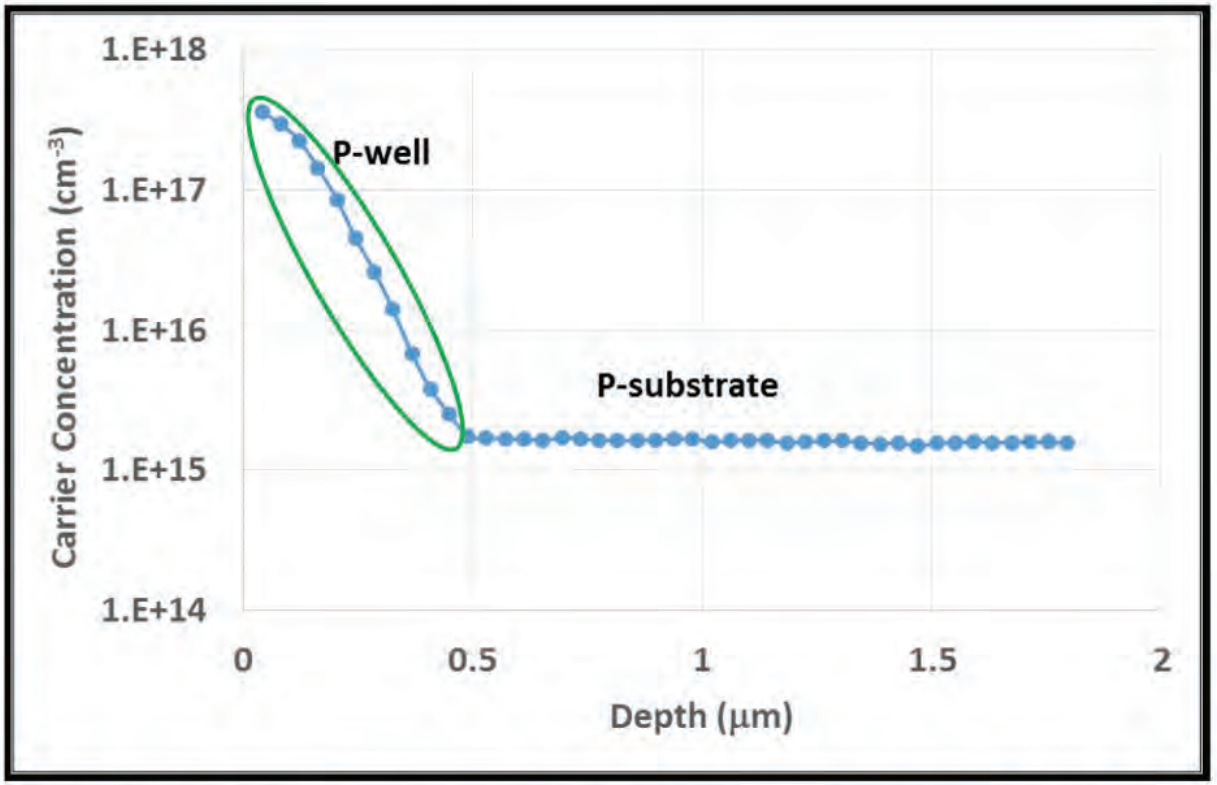
Upon information and belief, an NMOS transistor is above the second active region, and thus the second active region is a region within which transistors can be formed.

As shown in the above SEM image, the second active region (which is near an NMOS transistor) is separate from the first active region (which is near a PMOS transistor) and is disposed adjacent to the first active region, under Mapping A.

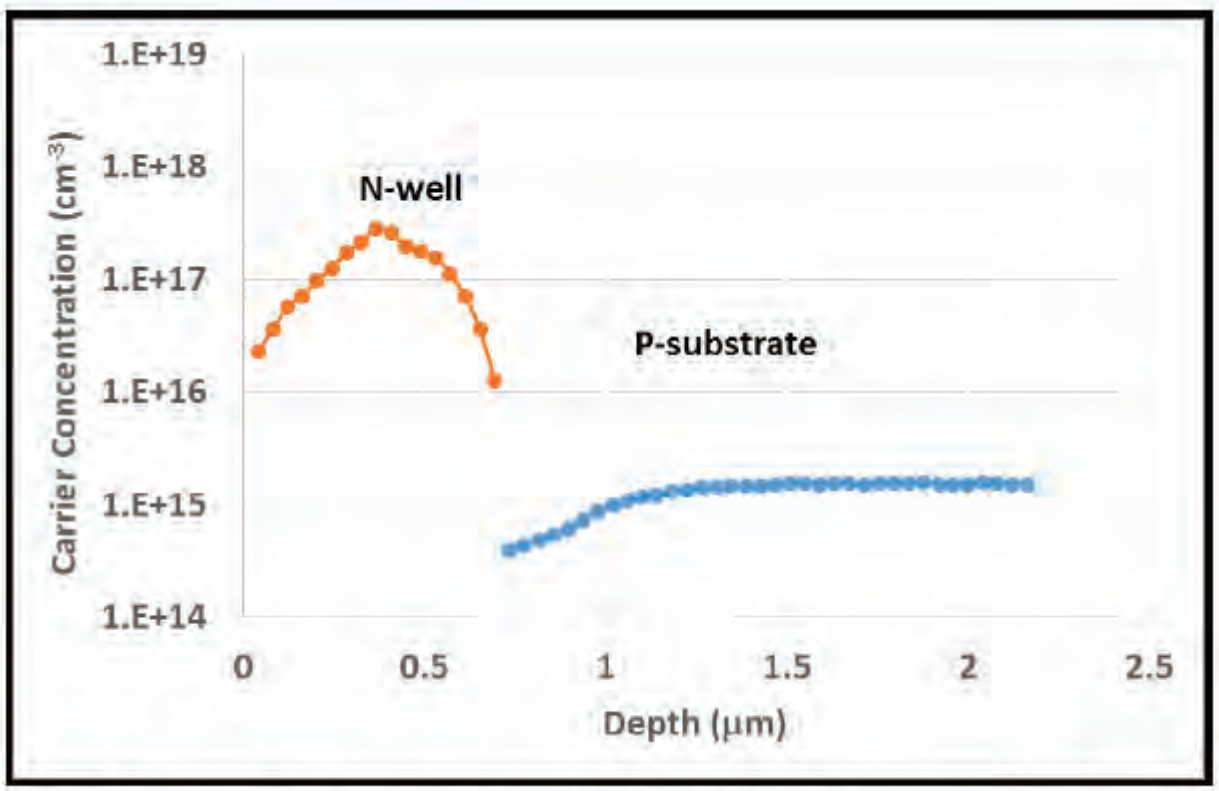
As another example, in accordance with Mapping B, a second active region as claimed is shown in the below SEM image (labeled Figure 5.4.1):

	 Figure 5.4.1: Capacitor dielectric and cell plate at an edge of DRAM array (SEM) Upon information and belief, an NMOS transistor is above the second active region, and thus the second active region is a region within which transistors can be formed. For example, the gate of such a transistor is shown above the second active region in the above image. As shown in the above SEM image, the second active region (which is near an NMOS transistor) is separate from the first active region (which is near a PMOS transistor) and is disposed adjacent to the first active region, under Mapping B.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-DRAM Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region, under both Mappings A and B. *See* above at Elements 2-3.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface	The Dell-Micron-DRAM Accused Products include a semiconductor device comprising at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate. For example, the graph below, obtained via SRP analysis electrically characterizing the Dell-Micron-DRAM Accused Products, shows a graded dopant concentration (annotated with green oval) in the first active region (e.g., as shown by the concentration corresponding to an

to the second surface of the substrate.	n-well) to aid carrier movement from the first surface to the second surface of the substrate (e.g., downwards, corresponding to increasing depth, in the below graph), under both Mappings A and B. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.  Figure 2.1.2: Spreading resistance profile of a peripheral n-well As another example, the graph below, also obtained via SRP analysis, shows a graded dopant concentration (annotated with green oval) in the second active region (e.g., as shown by the concentration corresponding to an p-well) to aid carrier movement from the first surface to the second surface of the substrate (e.g., downwards, corresponding to increasing depth, in the below graph), under both Mappings A and B.

	 Figure 2.1.1: Spreading resistance profile of a peripheral p-well
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The substrate of the semiconductor device of the Dell-Micron-DRAM Accused Products is a p-type substrate, as discussed above for Claim 1, Element 1.
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The substrate of the semiconductor device of the Dell-Micron-DRAM Accused Products has epitaxial silicon on top of a nonepitaxial substrate. Upon information and belief, the substrate used in the Dell-Micron-DRAM Accused Products is a single-crystal silicon wafer. Additionally, SRP analysis shows a curve downwards in the below blue (corresponding to substrate) plot (from about 1.2 µm towards shallower depths) indicative of a purer layer grown on the non-epitaxial substrate, and this is likely implemented via epitaxy.

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	 Figure 2.1.2: Spreading resistance profile of a peripheral n-well
5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Dell-Micron-DRAM Accused Products meet this limitation. For example, in the SEM images discussed above for Claim 1, Elements 2-3 (Figure 2.1.5 for Mapping A and Figure 5.4.1 for Mapping B), the first and second active regions (under both Mappings A and B) correspond to PMOS and NMOS transistors, respectively. Thus, the first active region and second active region contain one of either p-channel and n-channel devices (e.g., the first active region contains a p-channel device, and the second active region contains an n-channel device).
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Dell-Micron-DRAM Accused Products meet this limitation. As discussed above for Claim 1, the periphery (region with peripheral NMOS and PMOS transistors shown in Figures 2.1.5 and 5.4.1 contains NMOS (n-channel) and PMOS (p-channel) devices in respective p-wells and n-wells. As discussed above for Claim 1, Elements 2-3 and Claim 5, the p-channel and n-channel devices are contained in the first and active regions (*see* annotated Figures 2.1.5 and 5.4.1 discussed above). The following graphs obtained via SRP analysis show a p-well having a graded dopant (e.g., depths to about 0.5 µm in first graph below) and an n-well having a graded dopant (e.g., depths of about 0.3-0.7 µm in second graph below).

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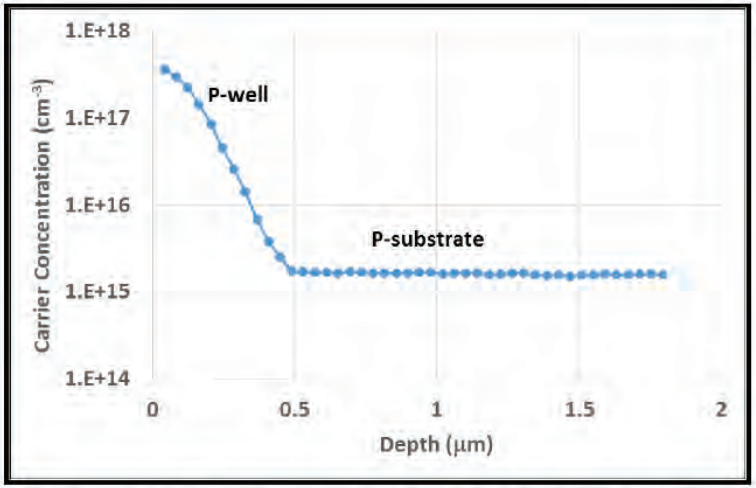


Figure 2.1.1: Spreading resistance profile of a peripheral p-well

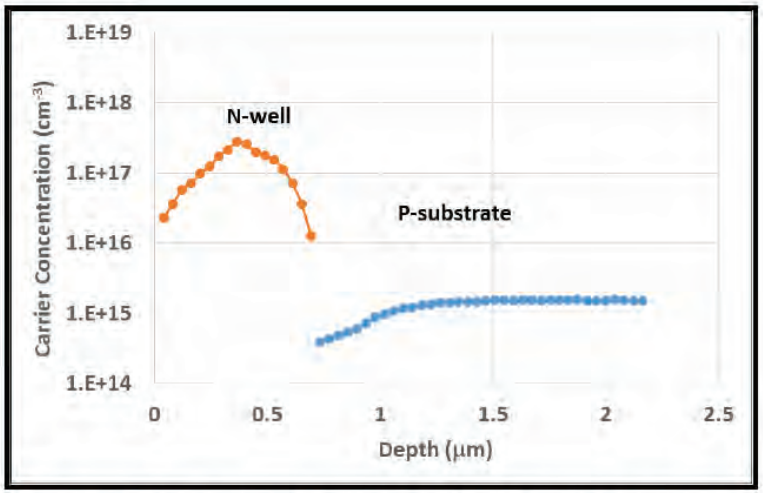
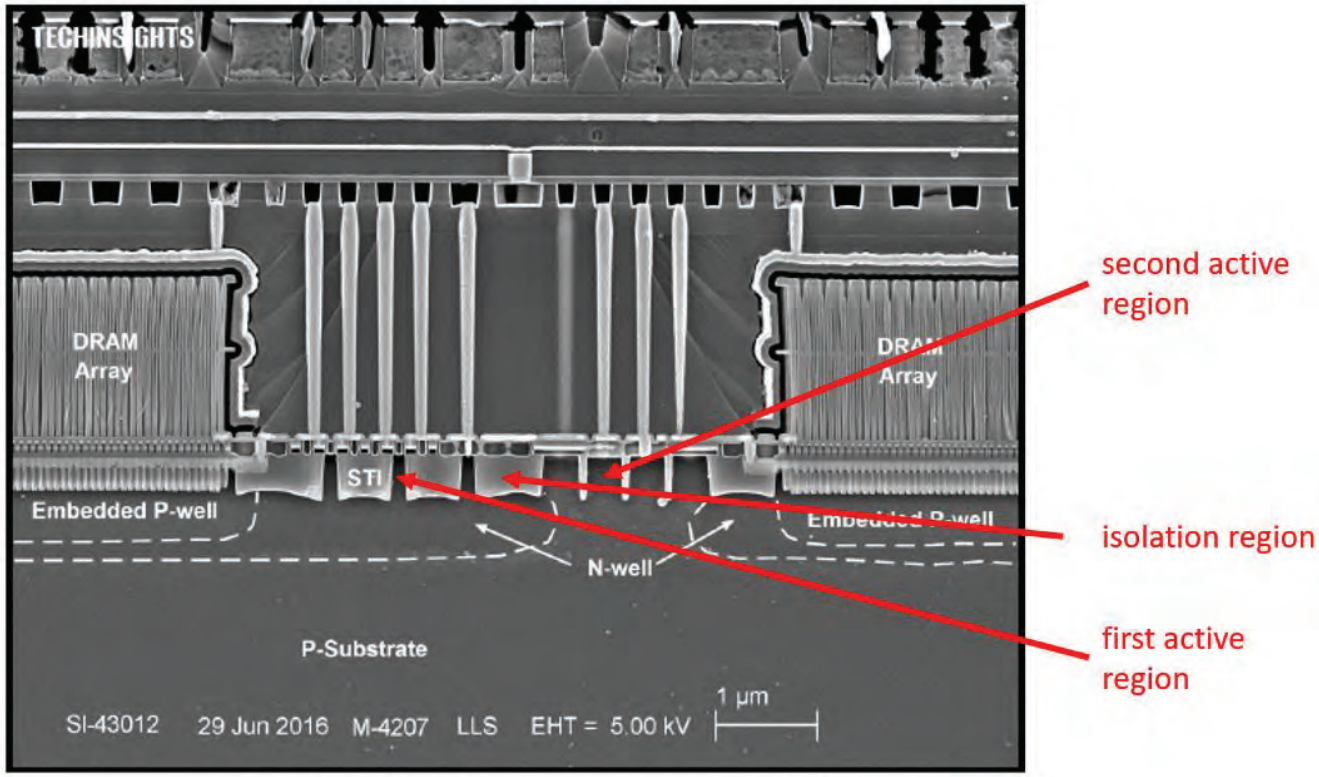


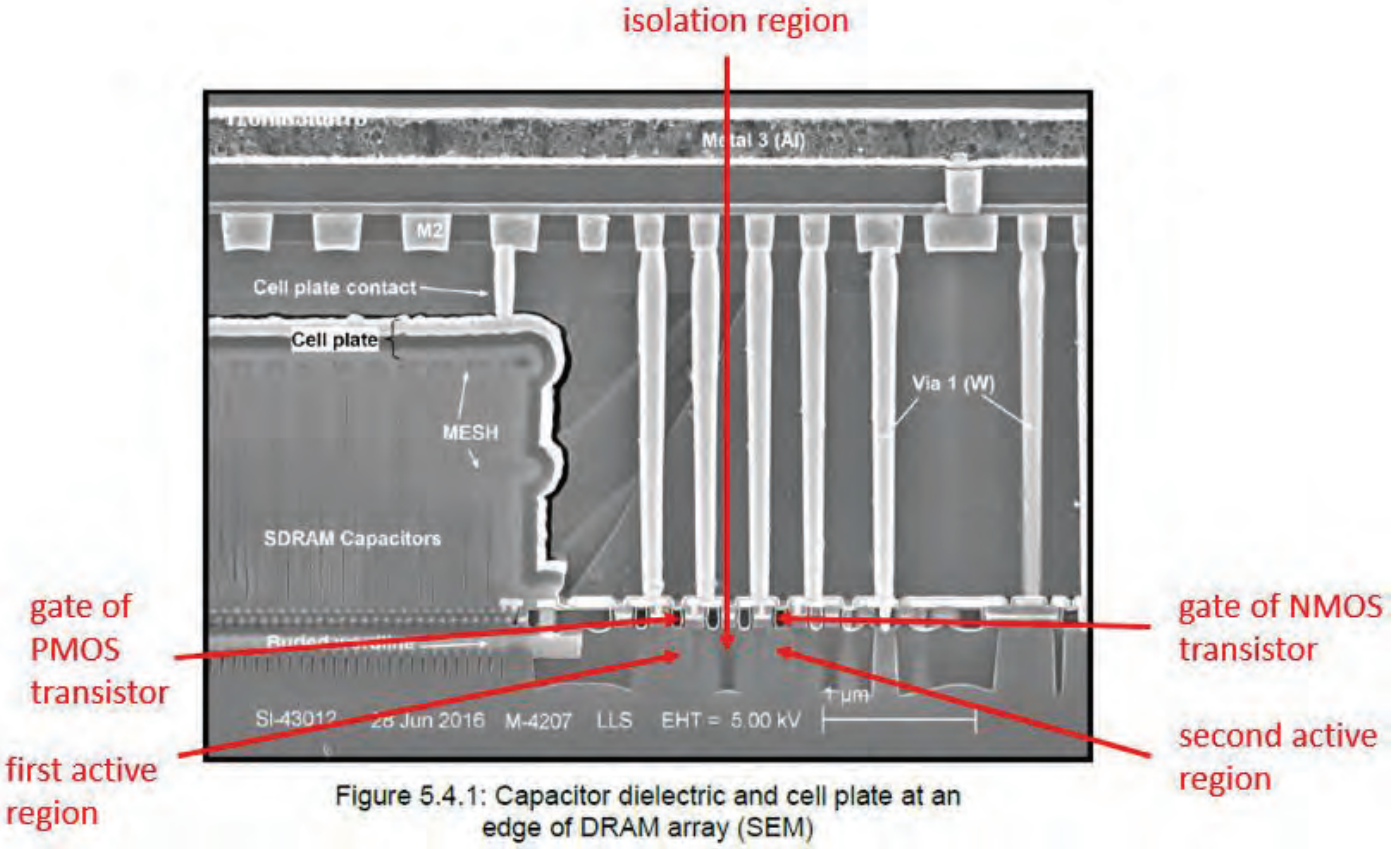
Figure 2.1.2: Spreading resistance profile of a peripheral n-well

The first and second active regions contain either p-channel or n-channel devices in these n-wells/p-wells because in CMOS technology a p-channel device is formed in an n-well and an n-channel device is formed in a p-well.

7. The semiconductor device of claim 1, wherein the first active region and second active region	The Dell-Micron-DRAM Accused Products meet this limitation.

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are each separated by at least one isolation region.	For example, under Mapping A discussed for Claim 1, the following SEM cross-sectional image shows that the first active region and second active region are each separated by at least one isolation region, which is a shallow-trench isolation as indicated by the label "STI" designating a similar isolation region to the left of the aforementioned isolation region.  Figure 2.1.5: DRAM array well structure (SEM) As another example, under Mapping B discussed for Claim 1, the following SEM cross-sectional image shows that the first active region and second active region are each separated by at least one isolation region.

	 Figure 5.4.1: Capacitor dielectric and cell plate at an edge of DRAM array (SEM)
8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Dell-Micron-DRAM Accused Products. Information about the fabrication process for Dell-Micron-DRAM Accused Products, including usage of an ion implantation process, is in the possession of the Dell Defendants and is expected to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1.

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[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region, under both Mappings A and B discussed for Claim 1. Details regarding formation of transistors are in the possession of the Dell Defendants and are expected to be obtained through discovery.
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region, under both Mappings A and B discussed for Claim 1. Details regarding formation of transistors are in the possession of the Dell Defendants and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 5 SRP analysis electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 2.
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 5.

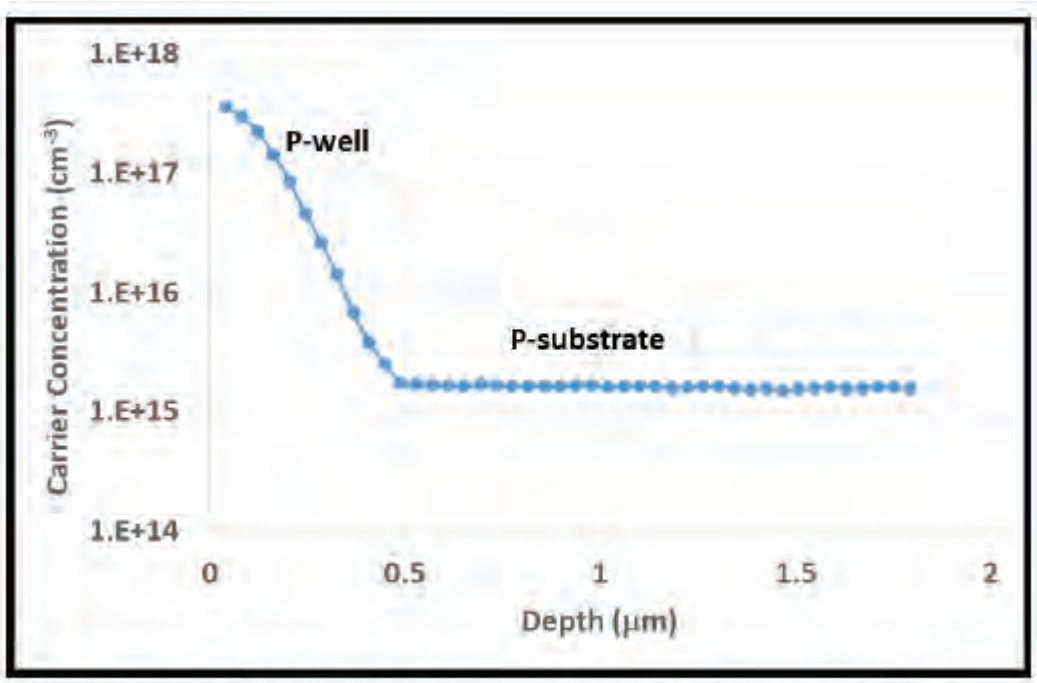
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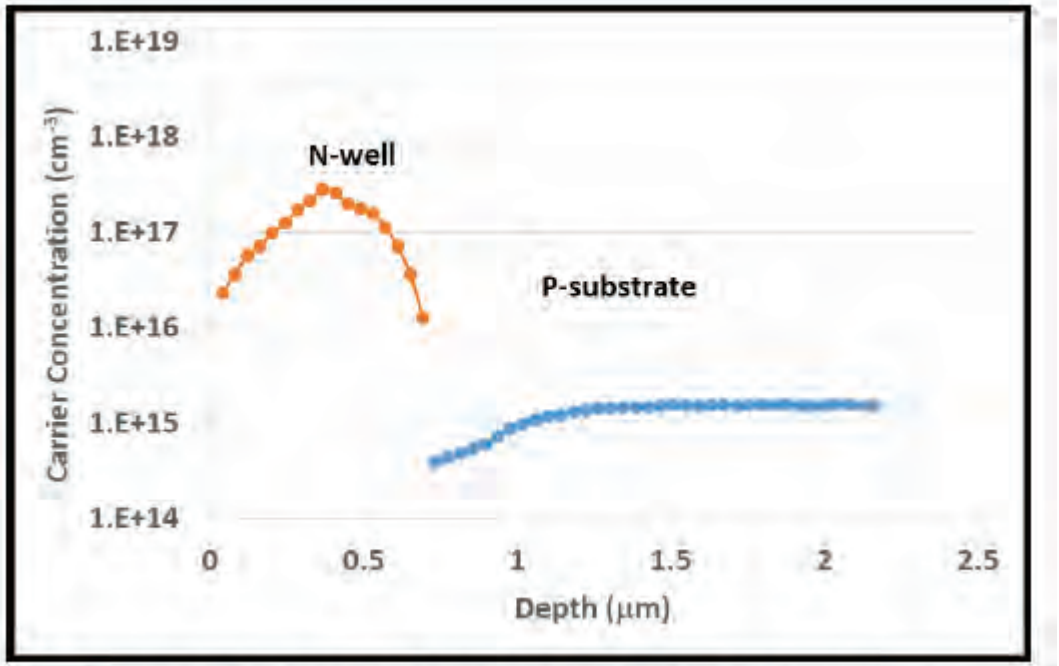
contain at least one of either p-channel and n-channel devices.	
14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 6.
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3. The SEM images labeled Figures 2.1.5 and 5.4.1 discussed above for Claim 1, Elements 2-3 show NMOS and PMOS transistors, which are adjacent to one another as discussed above for Claim 1, Element 3. Therefore, the transistors which can be formed in the first and second active regions are CMOS transistors. CMOS transistors require a source, a drain, a gate, and a channel region.

Exhibit E-2 to Greenthread's Amended Preliminary Infringement Contentions (1/29/2023)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a semiconductor device. *See* Exhibit E-1, Claim 1, Preamble. The Micron MT58K256M32JA-100:A GDDR5X DRAM referenced in Exhibit E-1 for tear-down analysis is discussed in this claim chart and other infringement contention claim charts as an example of a DRAM representative of the Dell-Micron-DRAM Accused Products. Upon information and belief, such a Micron DRAM is representative of DRAMs used in the Dell-Micron-DRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other DRAMs used in Dell-Micron-DRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, other DRAMs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Therefore, upon information and belief, other DRAMs used in Dell-Micron-DRAM Accused Products contain similar features as the Micron MT58K256M32JA-100:A GDDR5X DRAM, and function in a similar way, with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 4.

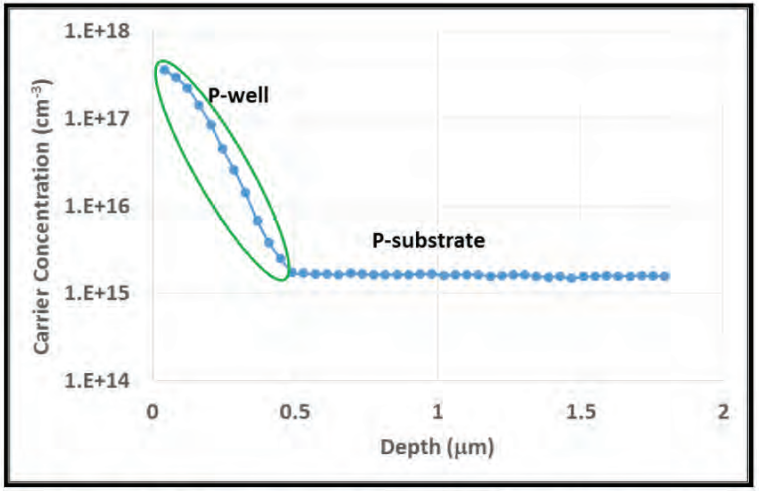
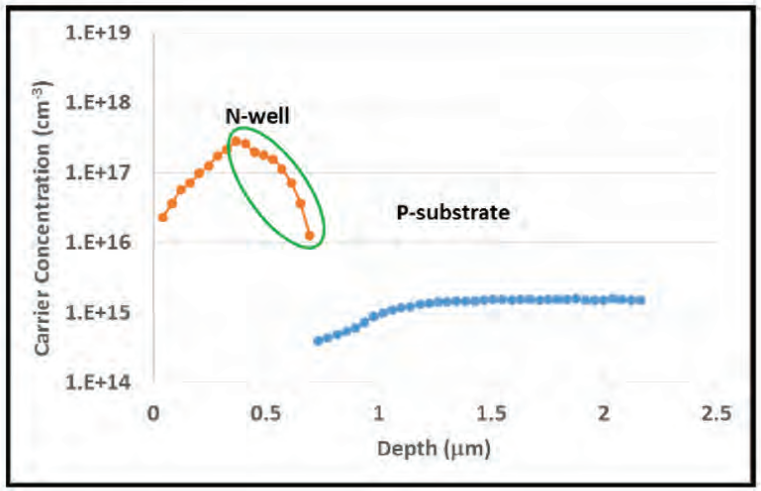
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U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 5 SRP analysis electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. For example, the Micron DRAM includes a p-well (first graph below) and an n-well (second graph below) having graded dopant regions.  Figure 2.1.1: Spreading resistance profile of a peripheral p-well

U.S. Patent No. 10,734,481	Accused Products
	 Figure 2.1.2: Spreading resistance profile of a peripheral n-well These graded dopant regions are to aid carrier movement from the first surface to the second surface of the substrate. *See* Exhibit E-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 2.
3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 4.
4. The semiconductor device of claim 1, wherein the first active region and second active region	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 5.

U.S. Patent No. 10,734,481	Accused Products
contain one of either p-channel and n-channel devices.	
5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-DRAM Products meet this limitation. See Exhibit E-1, Claim 6.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 7.
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 8.
8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Elements 1-3.
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 5 (SRP analysis of Figures 2.1.1 (below), 2.1.2 (below) showing p-type and n-type doping, respectively, at graded dopant concentration).

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U.S. Patent No. 10,734,481	Accused Products
	 Figure 2.1.1: Spreading resistance profile of a peripheral p-well  Figure 2.1.2: Spreading resistance profile of a peripheral n-well
13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 18.

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Exhibit E-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
transistors requiring at least a source, a drain, a gate and a channel.	
15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claims 4 (regarding nonepitaxial substrate), 18 (regarding CMOS).
16. The semiconductor device of claim 1, wherein the device is a flash memory.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Preamble.
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products meet include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 9, Element 2.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 9, Element 3.
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 4.

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[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 6. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 2.
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 4.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 5.
25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 6.

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Exhibit E-2 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 7.
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 8.
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 15.
33. The semiconductor device of claim 20, wherein the device is a flash memory.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 16.

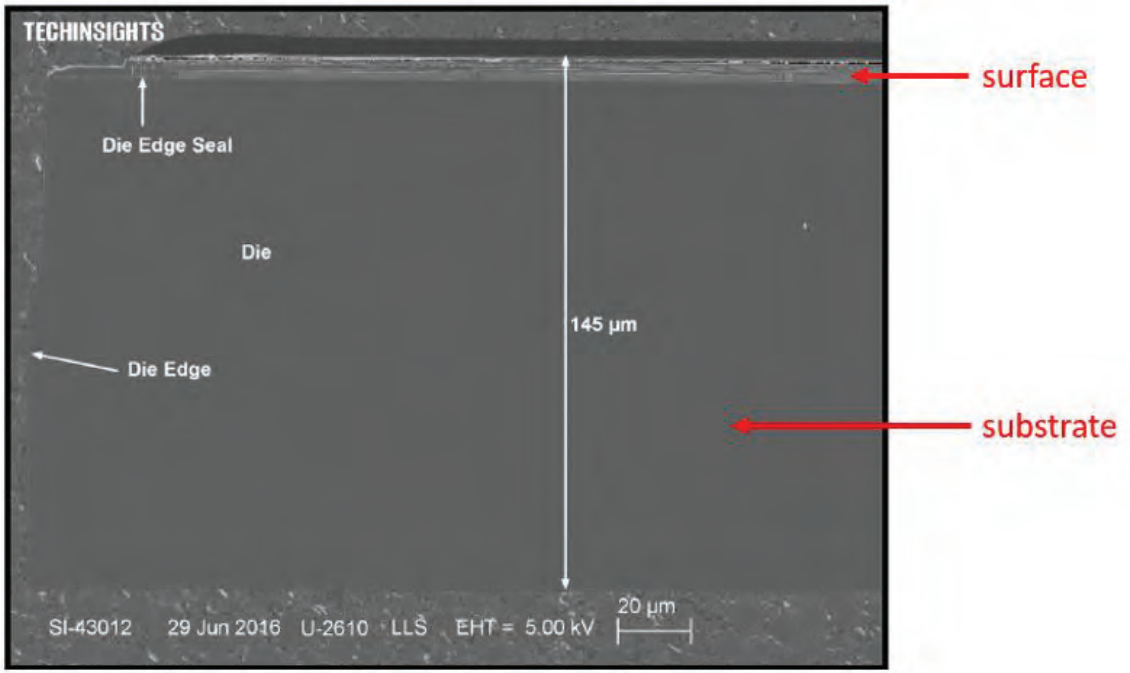
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Exhibit E-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a VLSI semiconductor device. The Micron DRAM discussed for claim 1 of Exhibit E-1 is a semiconductor device (*see* Exhibit E-1, Claim 1, Preamble) with millions of transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Dell Defendants and are expected to be obtained through discovery. The Micron MT58K256M32JA-100:A GDDR5X DRAM referenced in Exhibit E-1 is discussed in this claim chart and other infringement contention claim charts as an example of a DRAM representative of the Dell-Micron-DRAM Accused Products. Upon information and belief, such a Micron DRAM is representative of DRAMs used in the Dell-Micron-DRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other DRAMs used in Dell-Micron-DRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, other DRAMs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Therefore, upon information and belief, other DRAMs used in Dell-Micron-DRAM Accused Products contain similar features as the Micron MT58K256M32JA-100:A GDDR5X DRAM, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 1.

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	 Figure 1.2.5: Die thickness (SEM)
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 4.

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active region or second active region;	
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 5. For example, referencing the SRP graph discussed at Exhibit E-1, Claim 1, Element 5, there are no active regions at depths of about 1.3 µm and greater. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the Dell-Micron-DRAM Accused Products are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 2.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 5; Exhibit E-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. *See* above at Claim 1, Element 6.

Exhibit E-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

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logic formed by one of either p-channel and n-channel devices.	
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.

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U.S. Patent No. 11,121,222	Accused Products
in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 15.
16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 16.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The Dell-Micron-DRAM Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. *See* above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the Dell-Micron-DRAM Accused Products are in the possession of the Dell Defendants and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The Dell-Micron-DRAM Accused Products meet this limitation. As shown by SEM imaging (*see* Exhibit E-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 9, Element 2.

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type and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 1, Element 6. As shown by SRP analysis (*see* Exhibit E-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SRP graph discussed at Exhibit E-1, Claim 1, Element 5. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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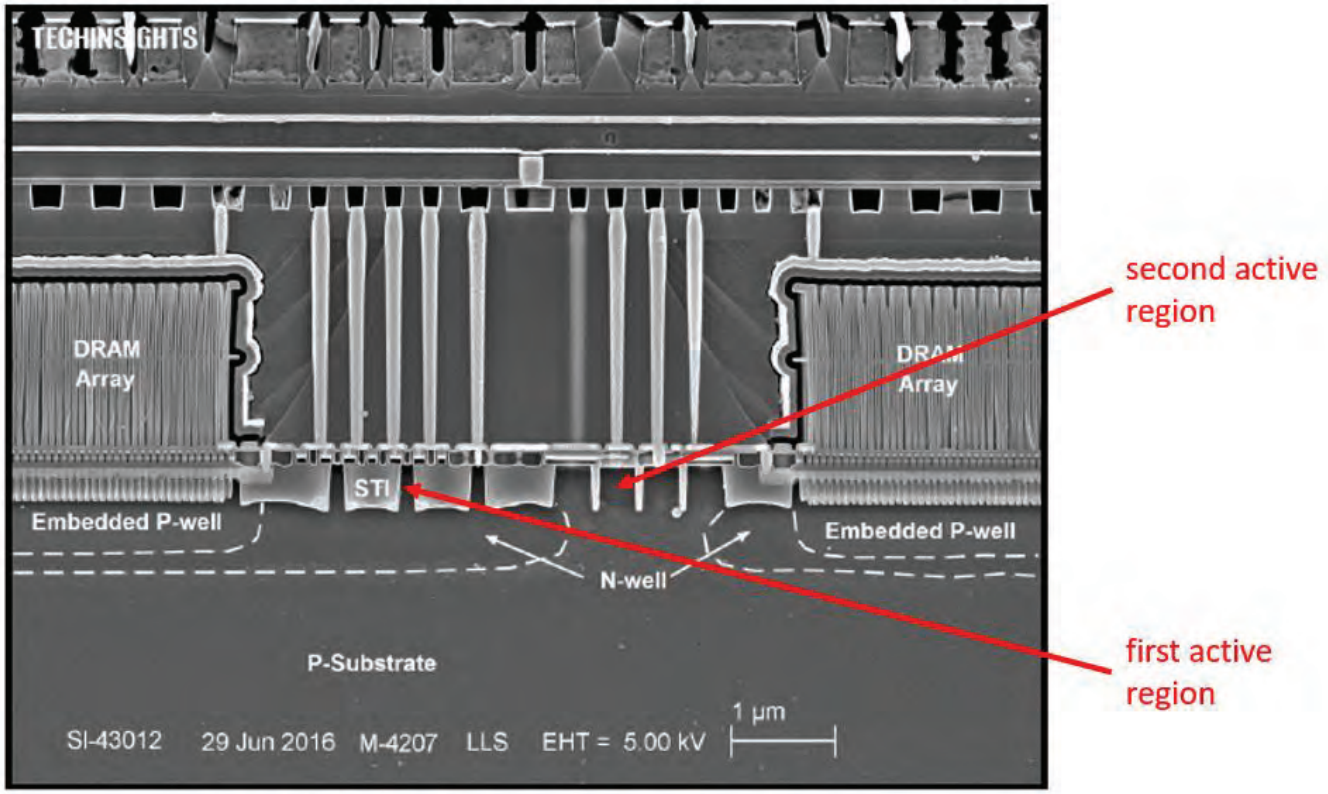
Exhibit E-3 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

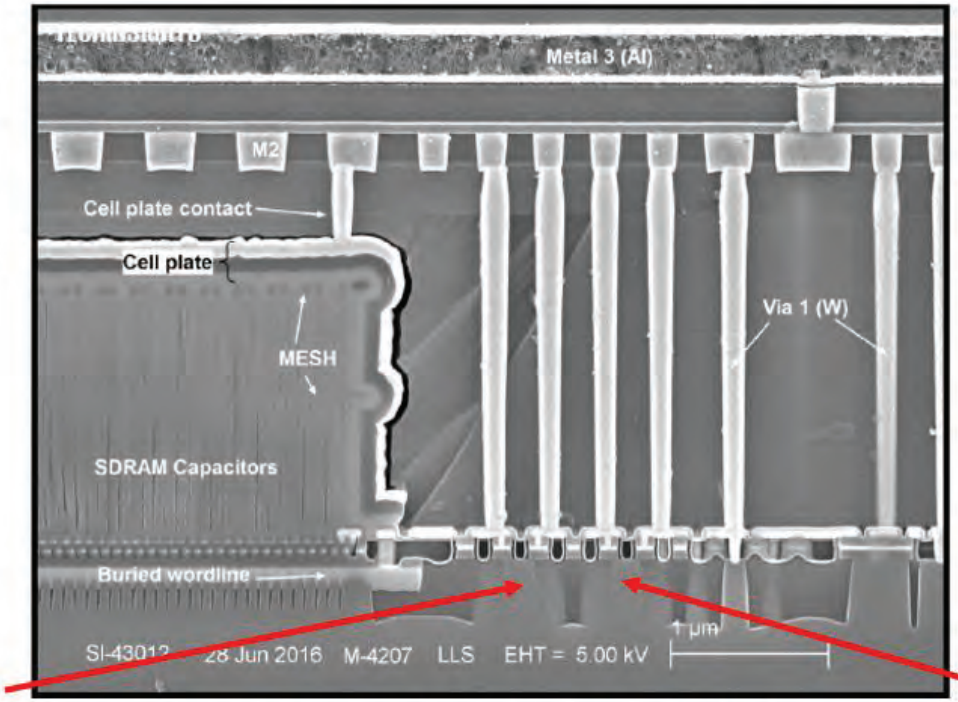
U.S. Patent No. 11,121,222	Accused Products
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 2.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 5.
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 8.

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graded dopant is fabricated with an ion implantation process.	
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 15.
34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 16.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	The Dell-Micron-DRAM Accused Products meet this limitation. As shown by SEM imaging (*see* Figures 2.1.5 and 5.4.1 shown below and discussed at Exhibit E-1, Claim 1, Element 3), each of the first and second active regions are in the lateral or vertical direction.

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	 Figure 2.1.5: DRAM array well structure (SEM)

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	 Figure 5.4.1: Capacitor dielectric and cell plate at an edge of DRAM array (SEM)
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a semiconductor device. *See* Exhibit E-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 2.

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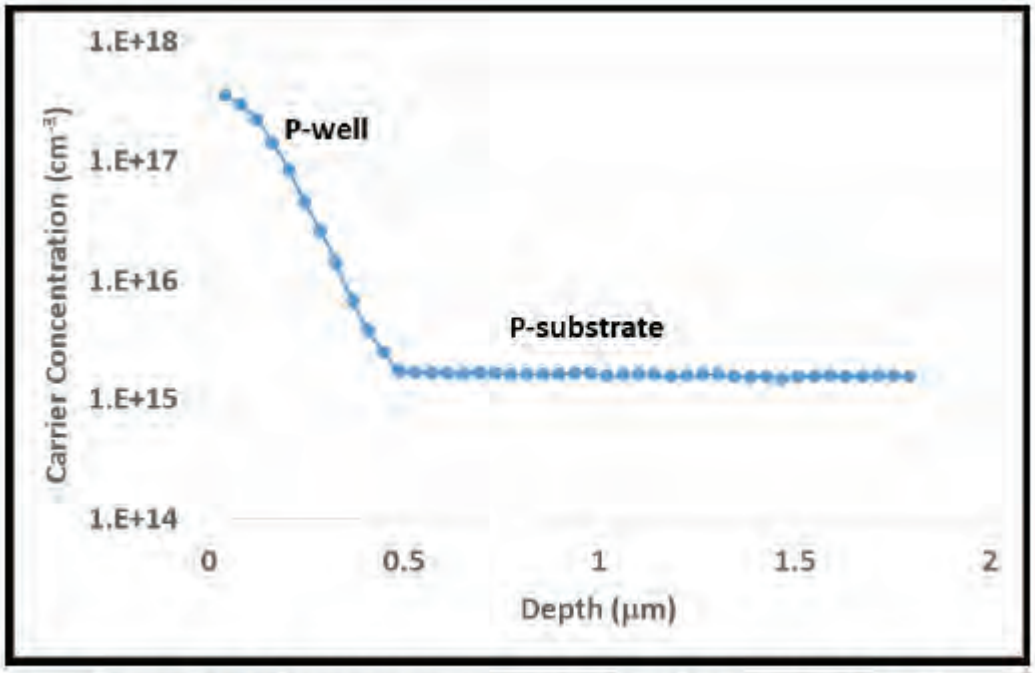
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type and within which transistors can be formed;	
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 5; *see* above at Claim 21, Element 5. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 1, Element 6. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.

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[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 21, Element 5. The following graph obtained via SRP analysis reveals at least one graded dopant acceptor concentration (e.g., concentration in p-well) as claimed. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

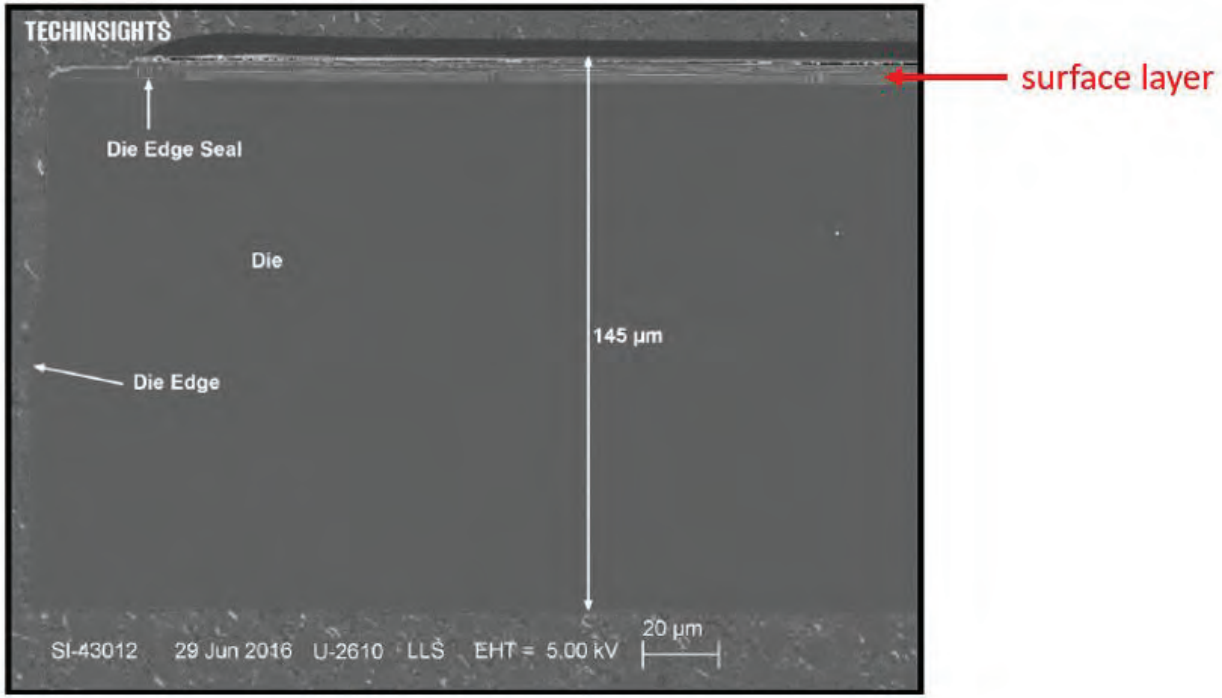
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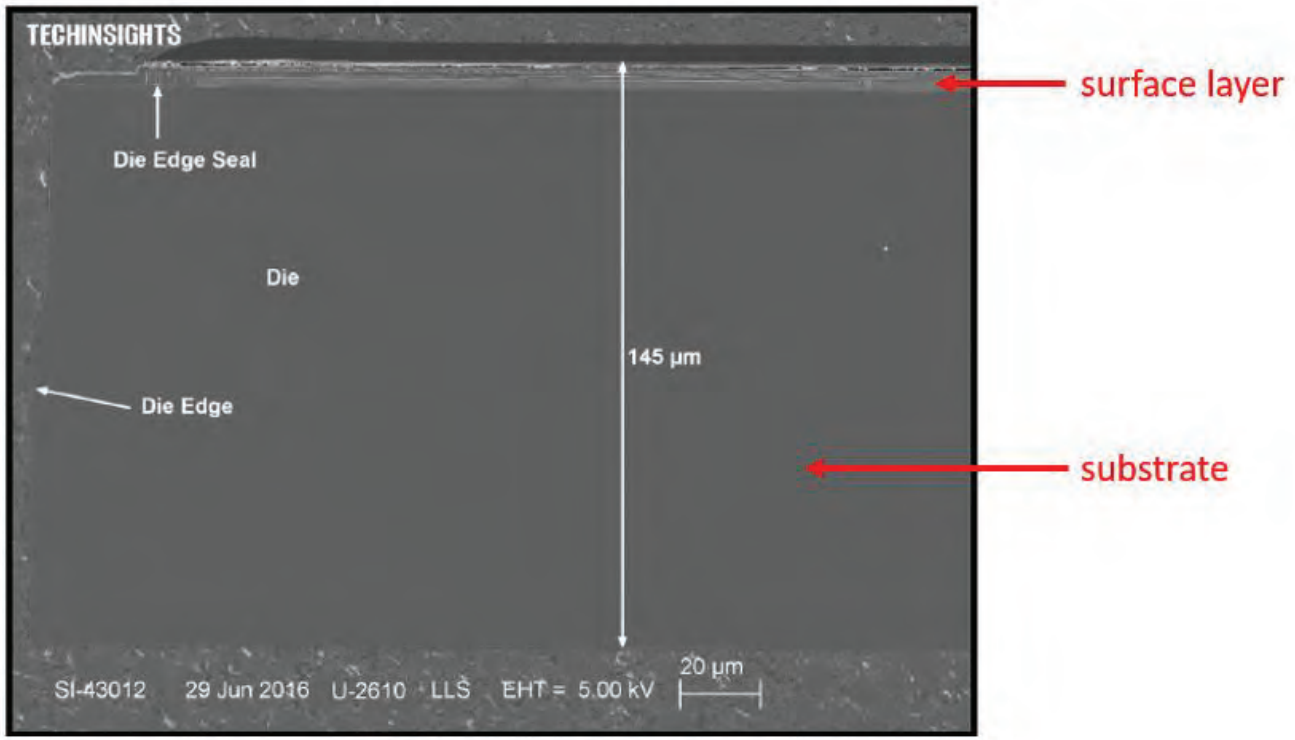
U.S. Patent No. 11,121,222	Accused Products
	 Figure 2.1.1: Spreading resistance profile of a peripheral p-well
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 39, Element 2.

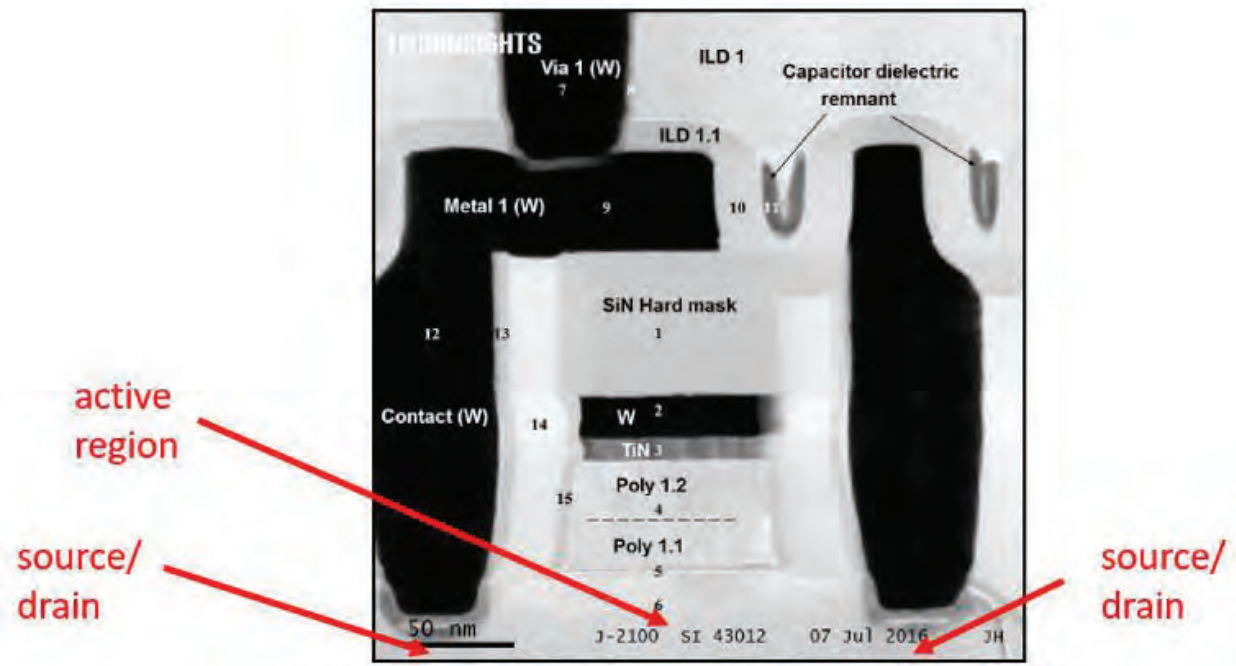
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[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Micron-DRAM Accused Products meet this limitation. SRP analysis (*see* Exhibit E-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a CMOS Semiconductor device. *See* Exhibit E-1, Claim 1, Preamble; Exhibit E-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 21, Element 1.

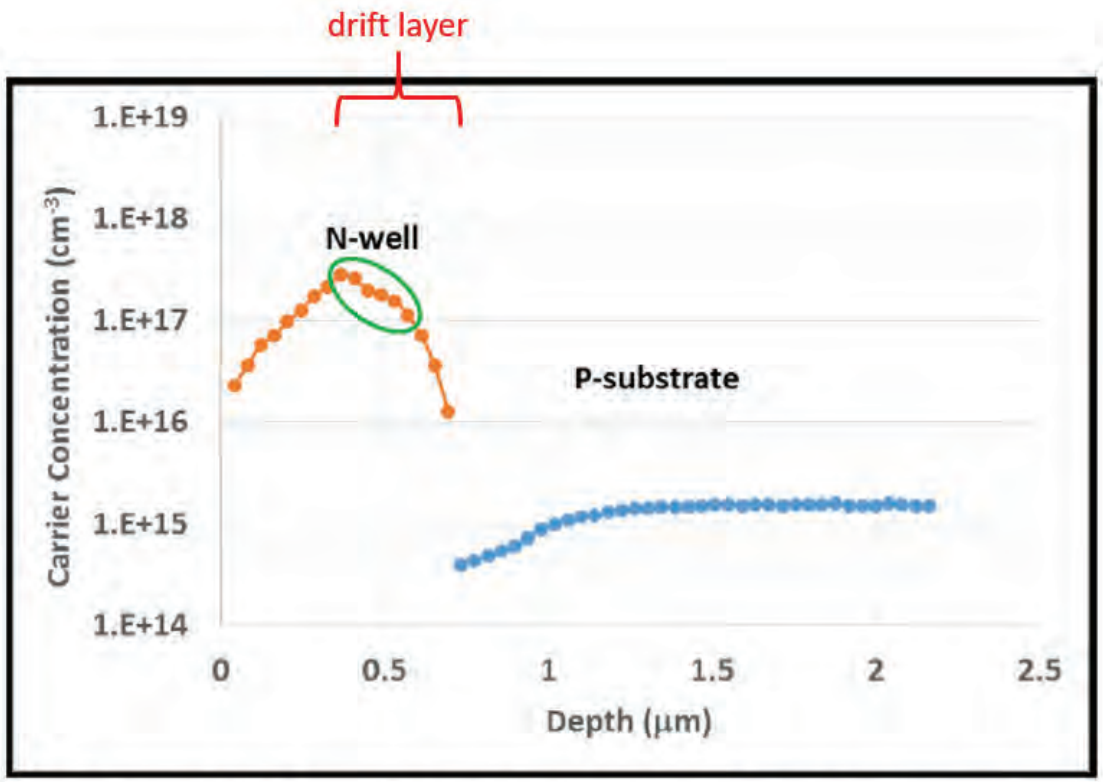
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	 Figure 1.2.5: Die thickness (SEM)
[Claim 44, Element 2] a substrate;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 44, Element 1.

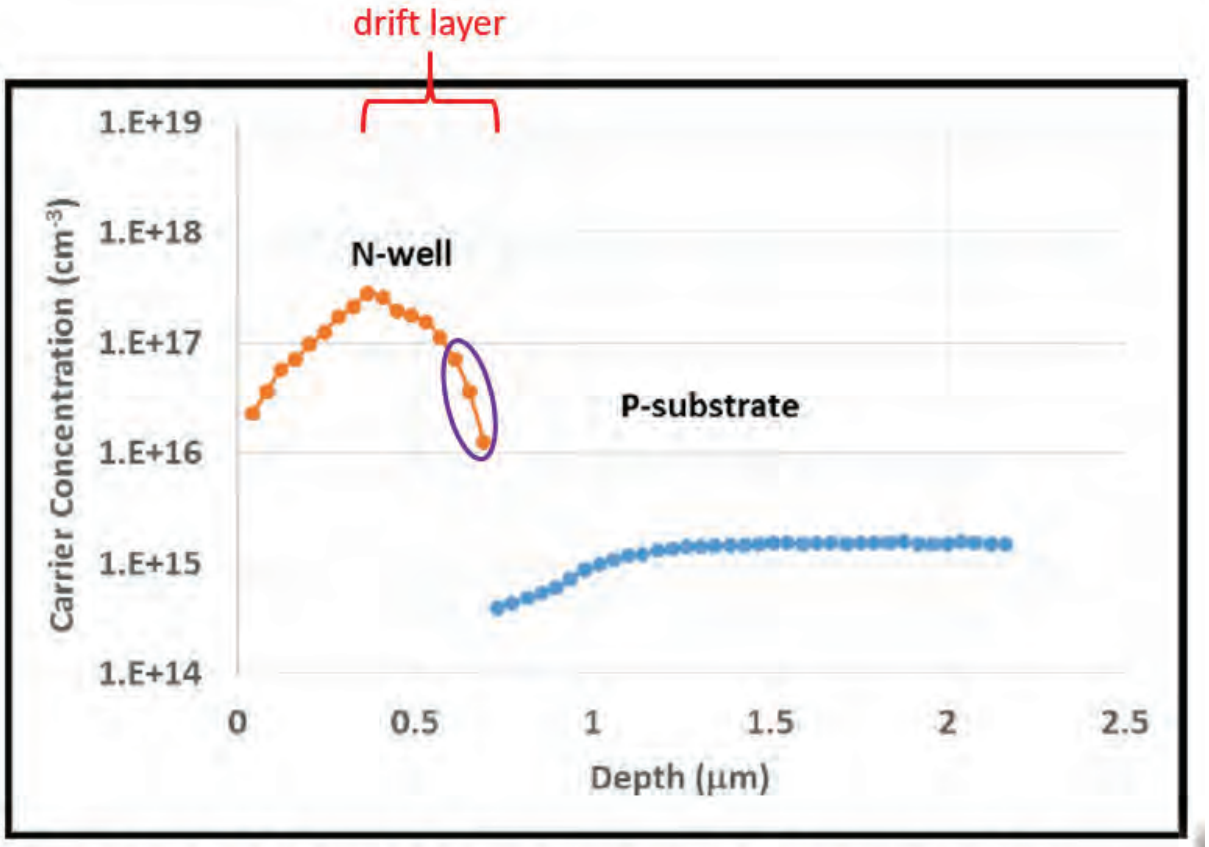
U.S. Patent No. 11,121,222	Accused Products
	 Figure 1.2.5: Die thickness (SEM)
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Element 3. For example, the SEM image below of the peripheral area of the Micron DRAM shows that the Micron DRAM includes an active region including a source and a drain disposed on one surface of the surface layer (e.g., as shown in the SEM image above for Claim 44, Element 2, the surface layer includes one surface facing away from the substrate (the active region is disposed on this surface) and another surface facing towards the substrate).

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	 Figure 2.3.6: TEM-EDS analysis locations in LV peripheral transistor area (BF-TEM)
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 21, Element 5. For example, SRP analysis shows that the Micron DRAM includes a single drift layer having a graded concentration (annotated with green oval below) as claimed:

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	 Figure 2.1.2: Spreading resistance profile of a peripheral n-well Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants (annotated with purple oval below to indicate a region of relatively steeper slope in concentration, compared to the shallower region discussed for Claim 44, Element 4).  Figure 2.1.2: Spreading resistance profile of a peripheral n-well Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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Exhibit E-4 to Greenthread's Amended Infringement Contentions (1/23/2023)

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a CMOS semiconductor device. *See* Exhibit E-3, Claim 44, Preamble. The Micron MT58K256M32JA-100:A GDDR5X DRAM referenced in Exhibit E-1 is discussed in this claim chart and other infringement contention claim charts as an example of a DRAM representative of the Dell-Micron-DRAM Accused Products. Upon information and belief, such a Micron DRAM is representative of DRAMs used in the Dell-Micron-DRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other DRAMs used in Dell-Micron-DRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, other DRAMs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Therefore, upon information and belief, other DRAMs used in Dell-Micron-DRAM Accused Products contain similar features as the Micron MT58K256M32JA-100:A GDDR5X DRAM, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 44, Element 4. Upon information and belief, the drift layer (*see* Exhibit E-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 5] at least one well region disposed in said single	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Dell Defendants and are expected to be

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Exhibit E-4 to Greenthread's Amended Infringement Contentions (1/23/2023)

U.S. Patent No. 8,421,195	Accused Products
drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	obtained through discovery. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The Dell-Micron-DRAM Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 4; Exhibit E-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Elements 1, 5.

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Exhibit E-5 to Greenthread's Amended Infringement Contentions (1/23/2023)

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include a semiconductor device. *See* Exhibit E-4, Claim 1, Preamble. The Micron MT58K256M32JA-100:A GDDR5X DRAM referenced in Exhibit E-1 is discussed in this claim chart and other infringement contention claim charts as an example of a DRAM representative of the Dell-Micron-DRAM Accused Products. Upon information and belief, such a Micron DRAM is representative of DRAMs used in the Dell-Micron-DRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other DRAMs used in Dell-Micron-DRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, other DRAMs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Therefore, upon information and belief, other DRAMs used in Dell-Micron-DRAM Accused Products contain similar features as the Micron MT58K256M32JA-100:A GDDR5X DRAM, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-4, Claim 1, Element 4. The graded concentration of dopants observed via SRP analysis (*see* Exhibit E-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-4, Claim 1, Element 5. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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Exhibit E-5 to Greenthread's Amended Infringement Contentions (1/23/2023)

U.S. Patent No. 9,190,502	Accused Products
unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The Dell-Micron-DRAM Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Dell Defendants and are expected to be obtained through discovery. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
11. The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-2, Claim 16.

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Exhibit E-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include an electronic system. *See* Exhibit E-1, Claim 1, Preamble; Exhibit E-4, Claim 1, Preamble. Each Dell-Micron-DRAM Accused Product is an electronic system, because a computer is an electronic system. The Micron MT58K256M32JA-100:A GDDR5X DRAM referenced in Exhibit E-1 is discussed in this claim chart and other infringement contention claim charts as an example of a DRAM representative of the Dell-Micron-DRAM Accused Products. Upon information and belief, such a Micron DRAM is representative of flash memory devices used in the Dell-Micron-DRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other DRAMs used in Dell-Micron-DRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, other DRAMs would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Therefore, upon information and belief, other DRAMs used in Dell-Micron-DRAM Accused Products contain similar features as the Micron MT58K256M32JA-100:A GDDR5X DRAM, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 1, Element 2; Exhibit E-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 1, Element 3; Exhibit E-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 1, Element 4.

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Exhibit E-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 1, Element 5. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 1, Element 6; Exhibit E-3, Claim 21, Element *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.6.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 2.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 5.

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Exhibit E-6 to Greenthread's Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 15.
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 16.

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U.S. Patent No. 11,316,014	Accused Products
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 17.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-Micron-DRAM Accused Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit E-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit E-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit E-1, Claim 9, Element 5. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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area of the substrate where there are no active regions; and	
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit E-3, Claim 21, Element 6. *See also* SRP analysis reproduced at Exhibit E-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 26.
27. The system of Claim 21, wherein the first active region and second active region of the at least	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 27.

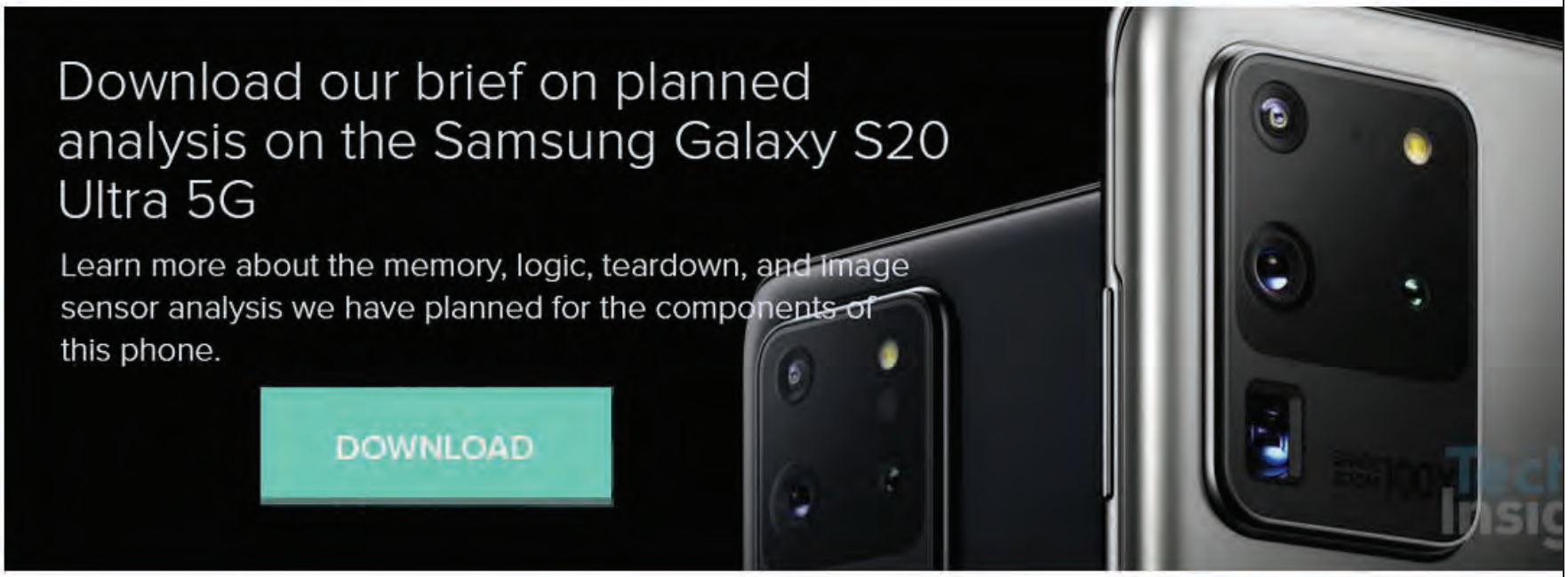
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one semiconductor device are each separated by at least one isolation region.	
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-Micron-DRAM Accused Products meet this limitation. *See* Exhibit E-3, Claim 28.

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Exhibits F-1 to F-6
Sony Accused
Transistor Products

Exhibit F-1 to Greenthread's Further Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products constitute and are incorporated into semiconductor devices. This chart includes exemplary information regarding a representative example of a Sony Accused Transistor Product found in the Sony IMX516 640x480 Resolution 5 µm pixel image sensor used in the Samsung Galaxy S20 Ultra 5G phone as analyzed in the below referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed in Exhibits F-1 through F-6. Selected pages are reproduced herein to aid in understanding. As shown in Exhibits D-1, D-2, D-3, and D-6, the Sony image sensors themselves infringe. However, Sony image sensors and other devices also include peripheral transistors that are exemplary of Sony Accused Transistors. Exhibits F-1 through F-6 analyze the peripheral transistors and other components in the Sony IMX516 which are exemplary of the transistors and components in other Sony Products. 

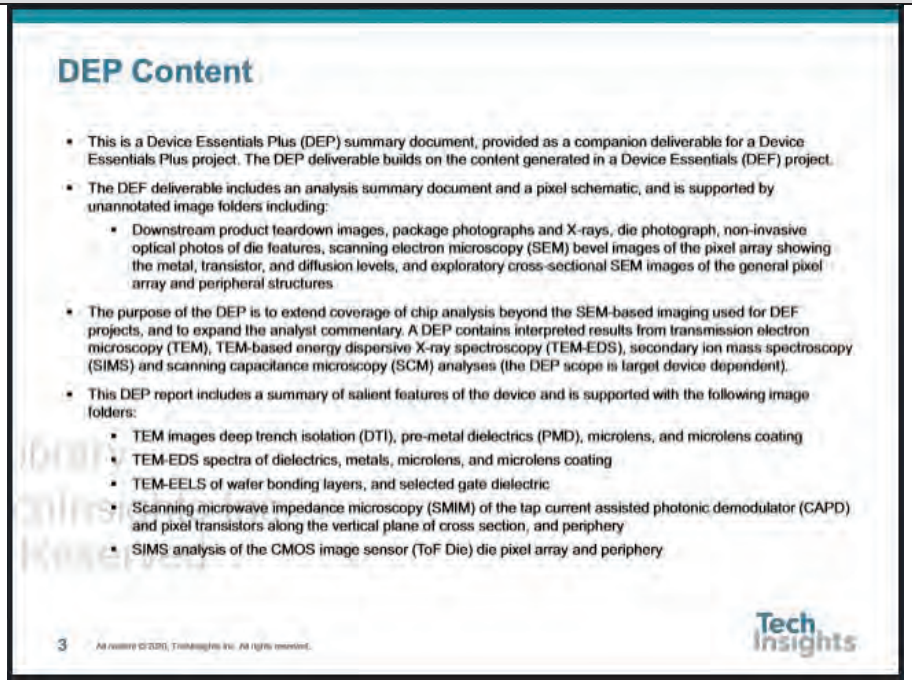
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Exhibit F-1 to Greenthread's Further Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products



DEP Content

- This is a Device Essentials Plus (DEP) summary document, provided as a companion deliverable for a Device Essentials Plus project. The DEP deliverable builds on the content generated in a Device Essentials (DEF) project.
- The DEF deliverable includes an analysis summary document and a pixel schematic, and is supported by unannotated image folders including:
  - Downstream product teardown images, package photographs and X-rays, die photograph, non-invasive optical photos of die features, scanning electron microscopy (SEM) bevel images of the pixel array showing the metal, transistor, and diffusion levels, and exploratory cross-sectional SEM images of the general pixel array and peripheral structures
- The purpose of the DEP is to extend coverage of chip analysis beyond the SEM-based imaging used for DEF projects, and to expand the analyst commentary. A DEP contains interpreted results from transmission electron microscopy (TEM), TEM-based energy dispersive X-ray spectroscopy (TEM-EDS), secondary ion mass spectroscopy (SIMS) and scanning capacitance microscopy (SCM) analyses (the DEP scope is target device dependent).
- This DEP report includes a summary of salient features of the device and is supported with the following image folders:
  - TEM images deep trench isolation (DTI), pre-metal dielectrics (PMD), microlens, and microlens coating
  - TEM-EDS spectra of dielectrics, metals, microlens, and microlens coating
  - TEM-EELS of wafer bonding layers, and selected gate dielectric
  - Scanning microwave impedance microscopy (SMIM) of the tap current assisted photonic demodulator (CAPD) and pixel transistors along the vertical plane of cross section, and periphery
  - SIMS analysis of the CMOS image sensor (ToF Die) die pixel array and periphery

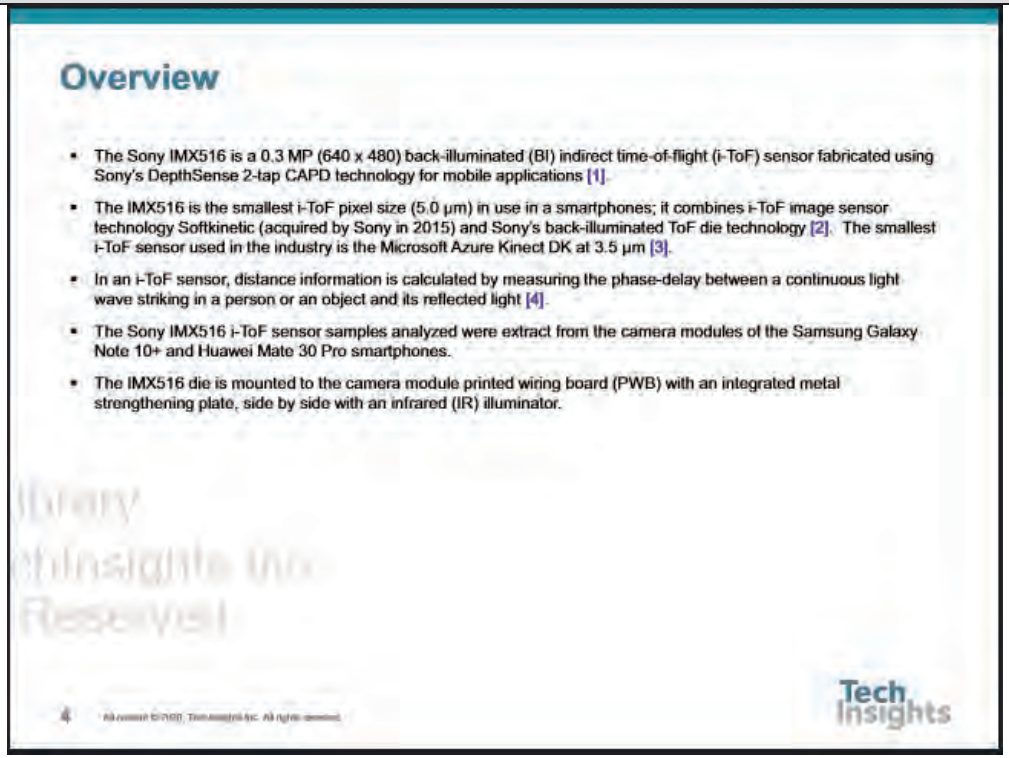
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Exhibit F-1 to Greenthread's Further Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,510,842	Accused Products



Overview

- The Sony IMX516 is a 0.3 MP (640 x 480) back-illuminated (BI) indirect time-of-flight (i-ToF) sensor fabricated using Sony's DepthSense 2-tap CAPD technology for mobile applications [1].
- The IMX516 is the smallest i-ToF pixel size (5.0 µm) in use in a smartphones; it combines i-ToF image sensor technology Softkinetic (acquired by Sony in 2015) and Sony's back-illuminated ToF die technology [2]. The smallest i-ToF sensor used in the industry is the Microsoft Azure Kinect DK at 3.5 µm [3].
- In an i-ToF sensor, distance information is calculated by measuring the phase-delay between a continuous light wave striking in a person or an object and its reflected light [4].
- The Sony IMX516 i-ToF sensor samples analyzed were extract from the camera modules of the Samsung Galaxy Note 10+ and Huawei Mate 30 Pro smartphones.
- The IMX516 die is mounted to the camera module printed wiring board (PWB) with an integrated metal strengthening plate, side by side with an infrared (IR) illuminator.

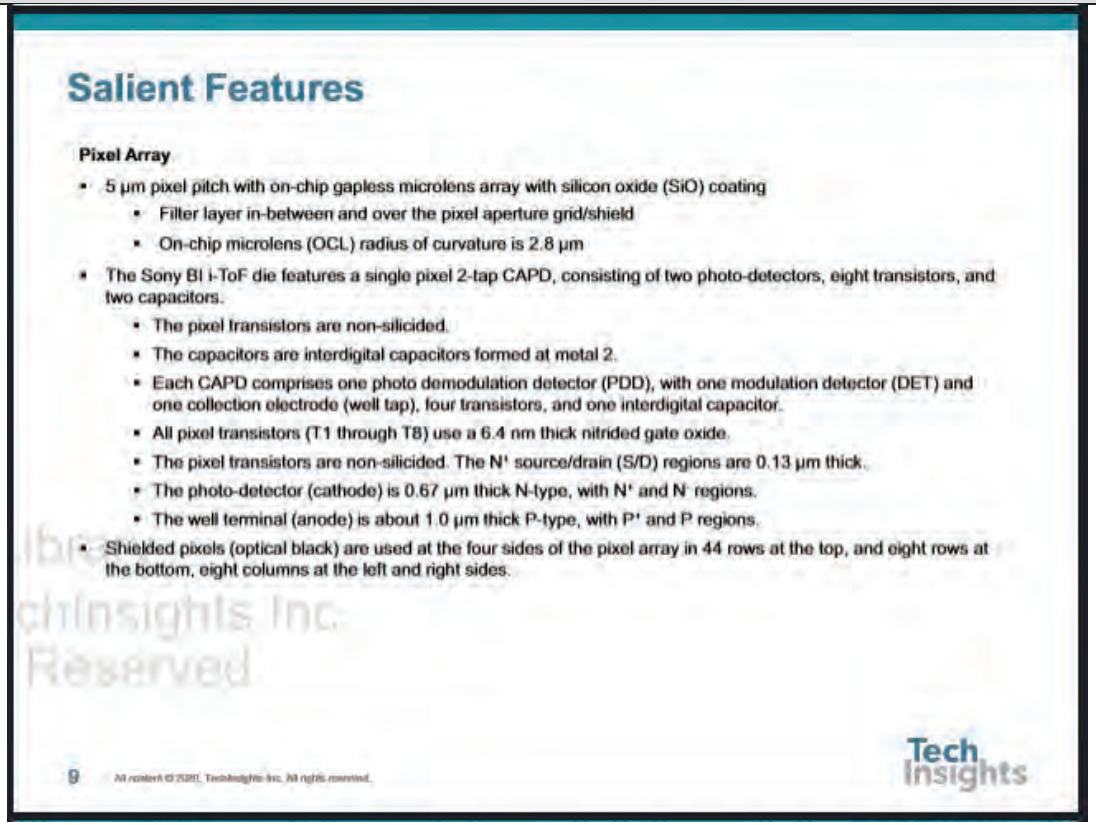
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Salient Features

Pixel Array

- 5 µm pixel pitch with on-chip gapless microlens array with silicon oxide (SiO) coating
  - Filter layer in-between and over the pixel aperture grid/shield
  - On-chip microlens (OCL) radius of curvature is 2.8 µm
- The Sony BI i-ToF die features a single pixel 2-tap CAPD, consisting of two photo-detectors, eight transistors, and two capacitors.
  - The pixel transistors are non-silicided.
  - The capacitors are interdigital capacitors formed at metal 2.
  - Each CAPD comprises one photo demodulation detector (PDD), with one modulation detector (DET) and one collection electrode (well tap), four transistors, and one interdigital capacitor.
  - All pixel transistors (T1 through T8) use a 6.4 nm thick nitrided gate oxide.
  - The pixel transistors are non-silicided. The N⁺ source/drain (S/D) regions are 0.13 µm thick.
  - The photo-detector (cathode) is 0.67 µm thick N-type, with N⁺ and N⁻ regions.
  - The well terminal (anode) is about 1.0 µm thick P-type, with P⁺ and P⁻ regions.
- Shielded pixels (optical black) are used at the four sides of the pixel array in 44 rows at the top, and eight rows at the bottom, eight columns at the left and right sides.

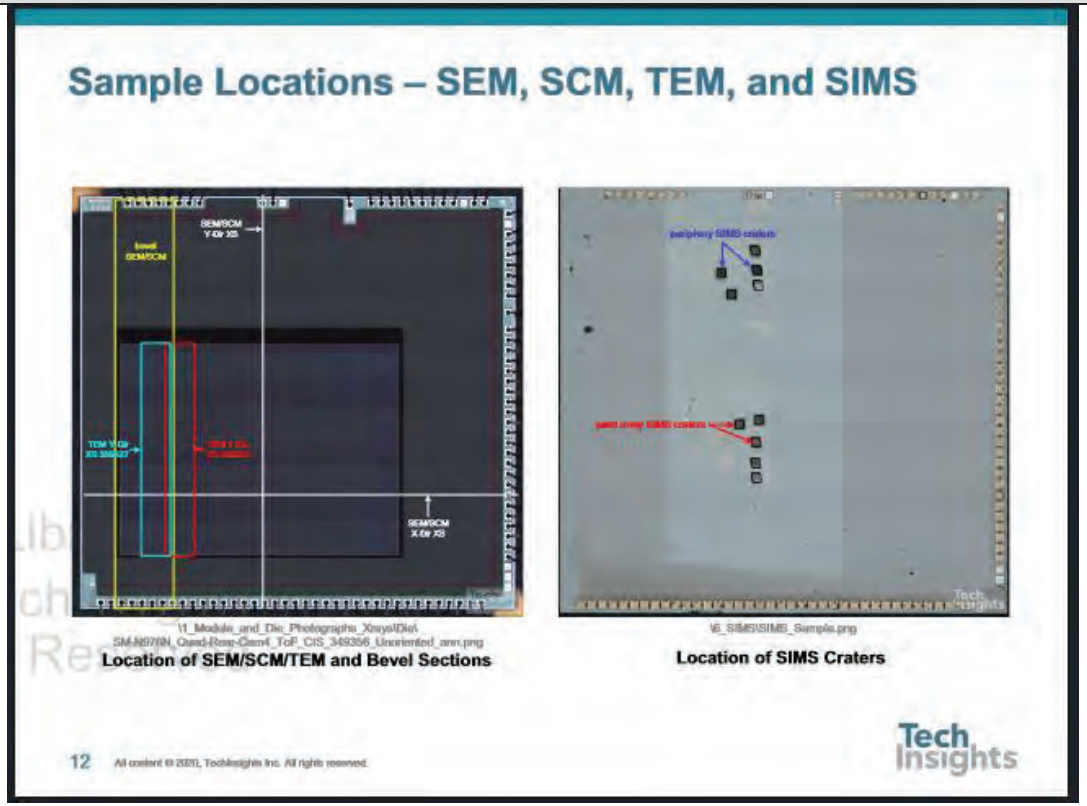
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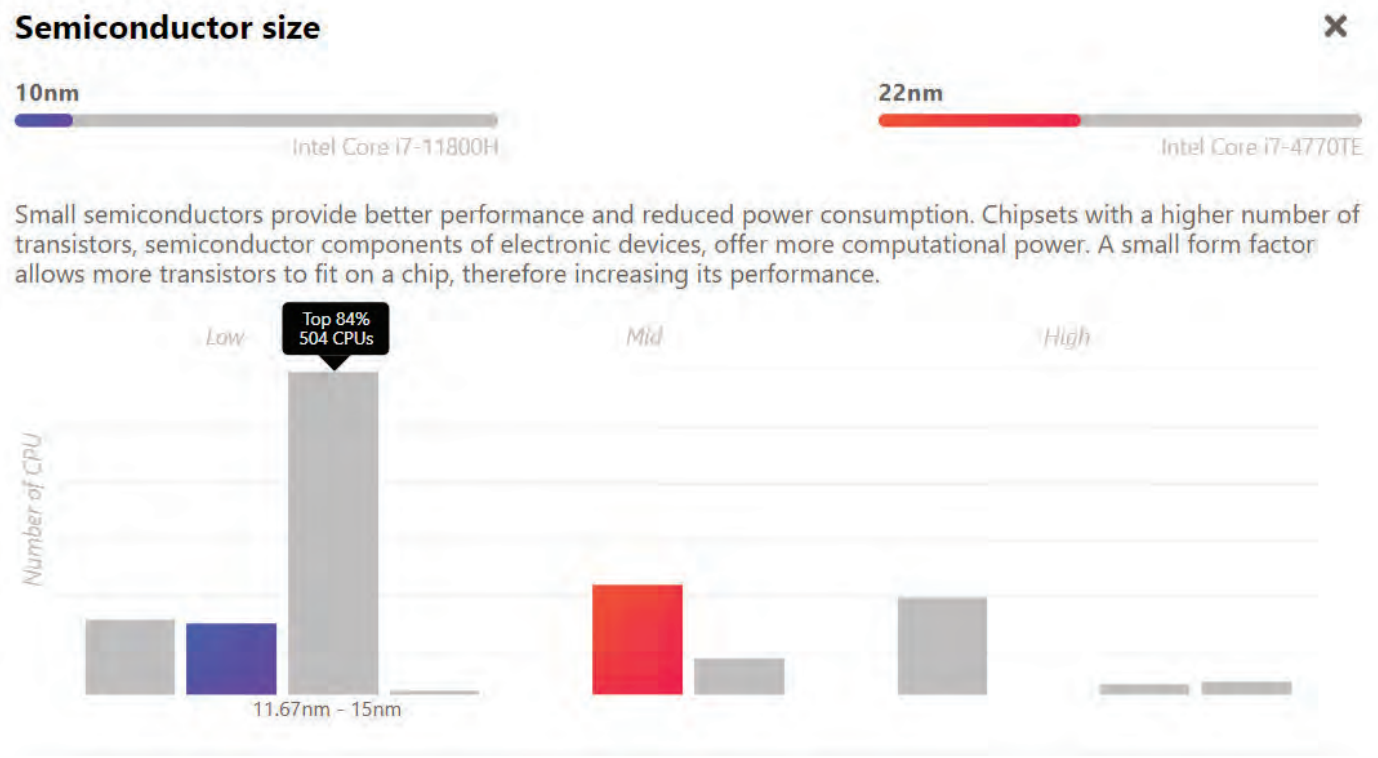
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The peripheral transistors in the Sony IMX516 are representative of the Sony Accused Transistor Products for purposes of Exhibits F-1 through F-6, and all Sony Accused Products, because IMX516 includes a transistor that is similar in structure and design to other Sony transistors. The Sony IMX516 transistor is representative of the Sony Accused Transistor Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Sony Accused Transistor Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other Sony Accused Transistor Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Similarly, the other Sony Accused Transistor Products (including Dell-Sony Accused Products) would have been designed in a similar manner as the Sony IMX516 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other Sony Accused Transistor Products contain similar features as the Sony IMX516 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Sony Accused Transistor Products contain similar features as the Sony IMX516, and function in a similar way with respect to the features claimed in the asserted claims.

This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained

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	through discovery. *See* https://www.techinsights.com/blog/samsung-galaxy-s20-ultra-5g-camera-teardown. The Sony Accused Transistor Products, of which Sony IMX516 is one example, are semiconductor devices.  *See* https://versus.com/en/intel-core-i7-11800h-vs-intel-core-i7-4770te
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Sony Accused Transistor Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary Sony Accused Transistor Product (the Sony IMX516 discussed above) incorporated into an exemplary Sony image sensor reveals the presence of such a substrate. For example, the Sony IMX516 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis.

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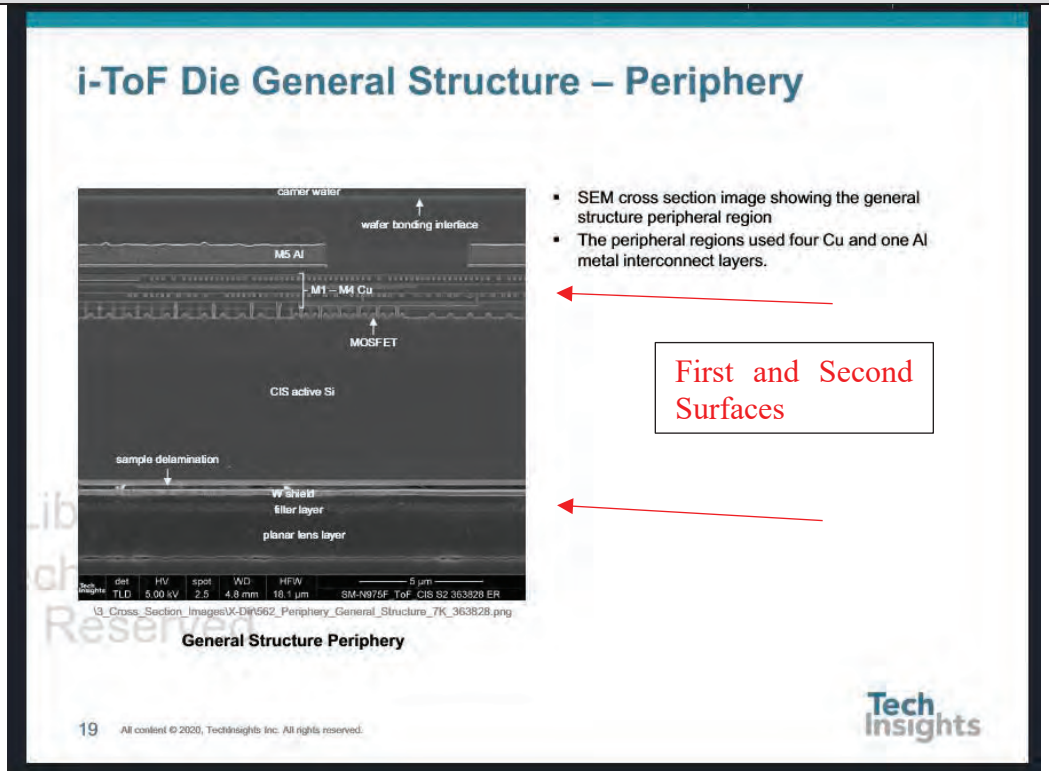


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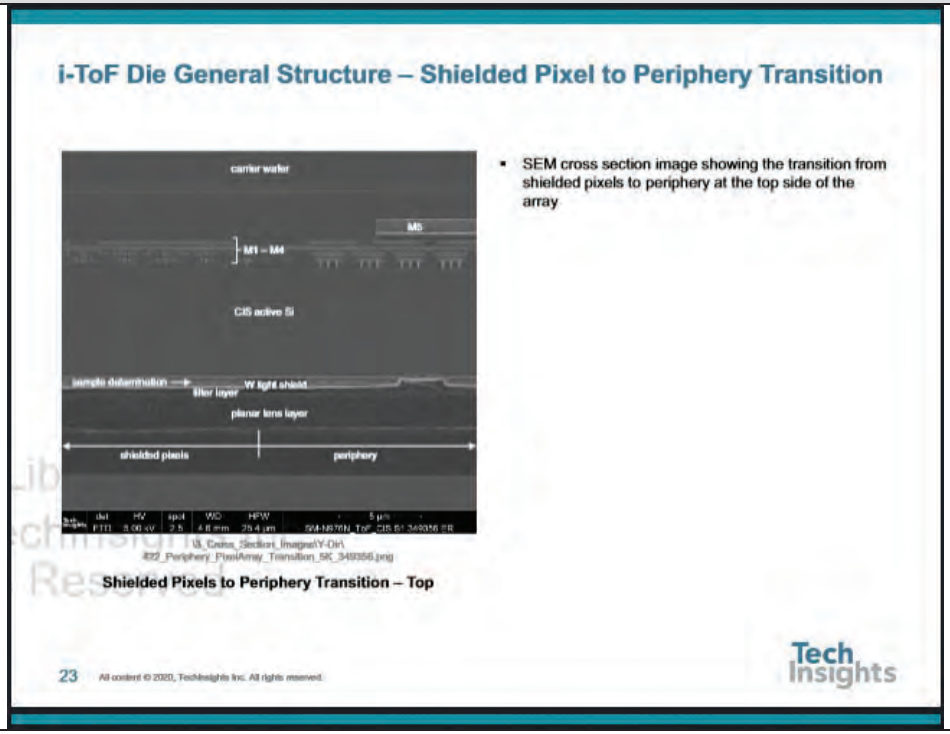
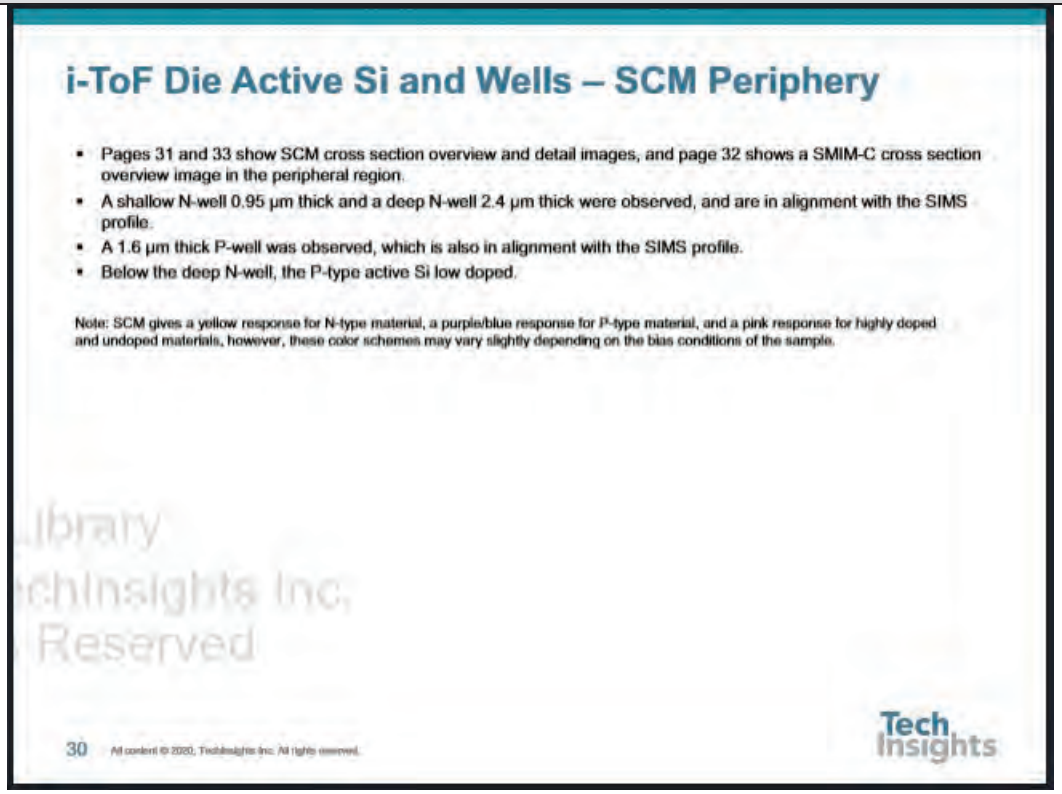
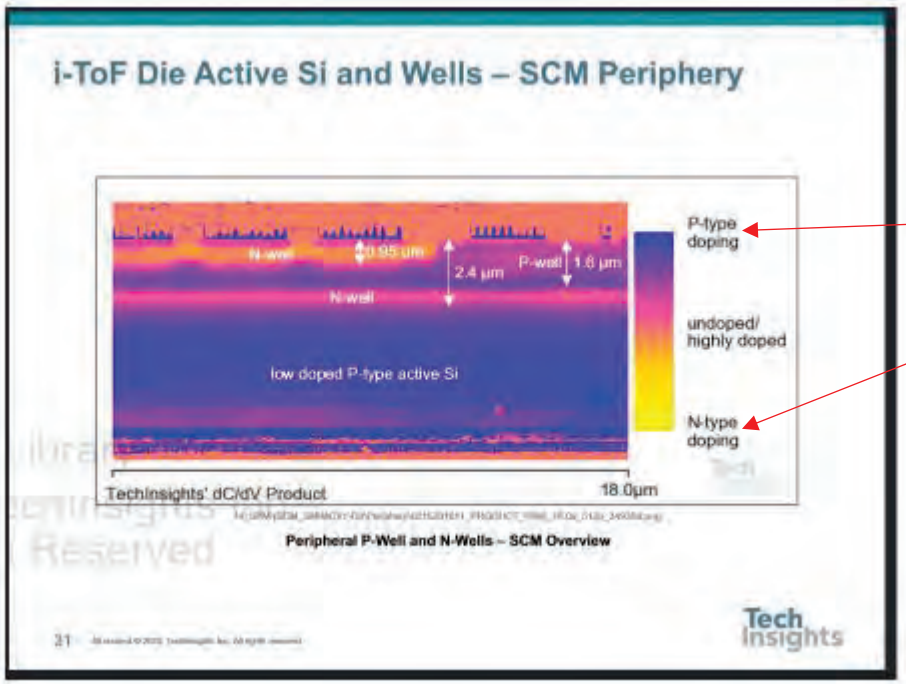
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First and Second Doping Types

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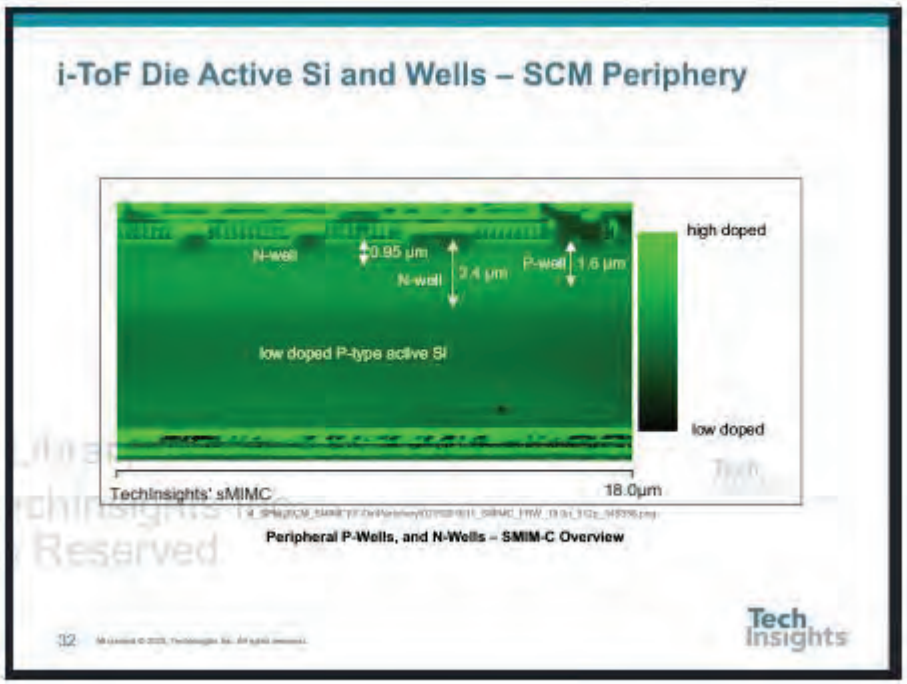
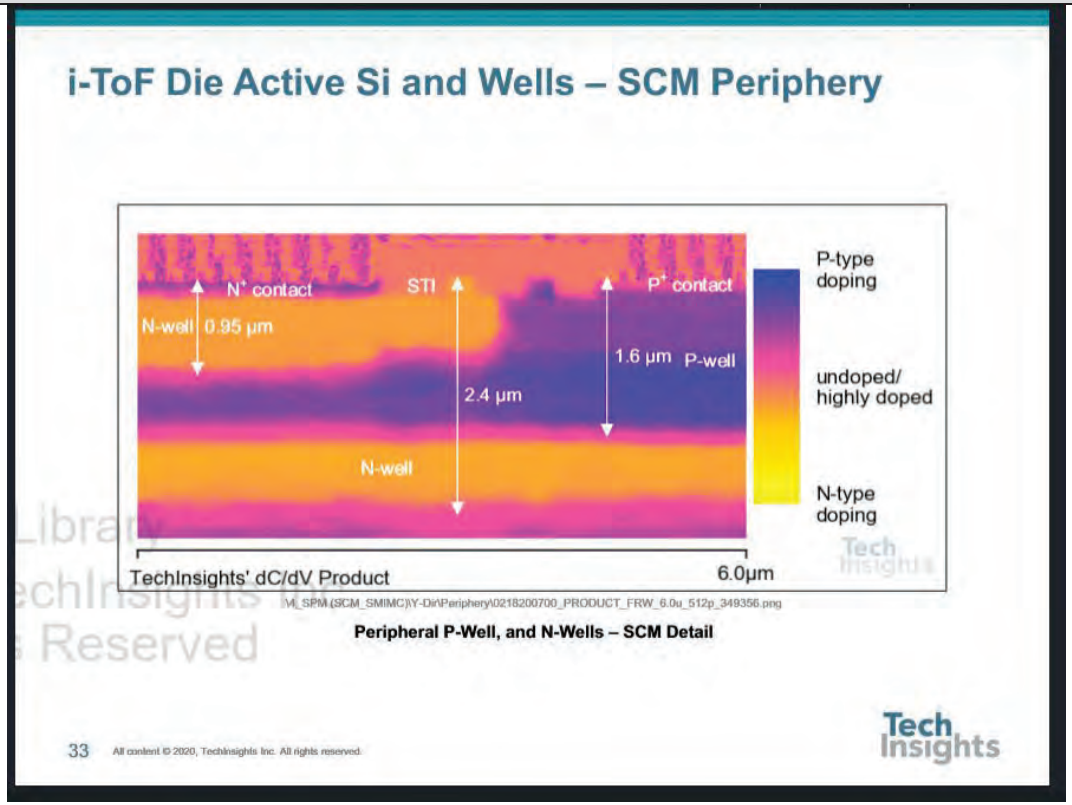
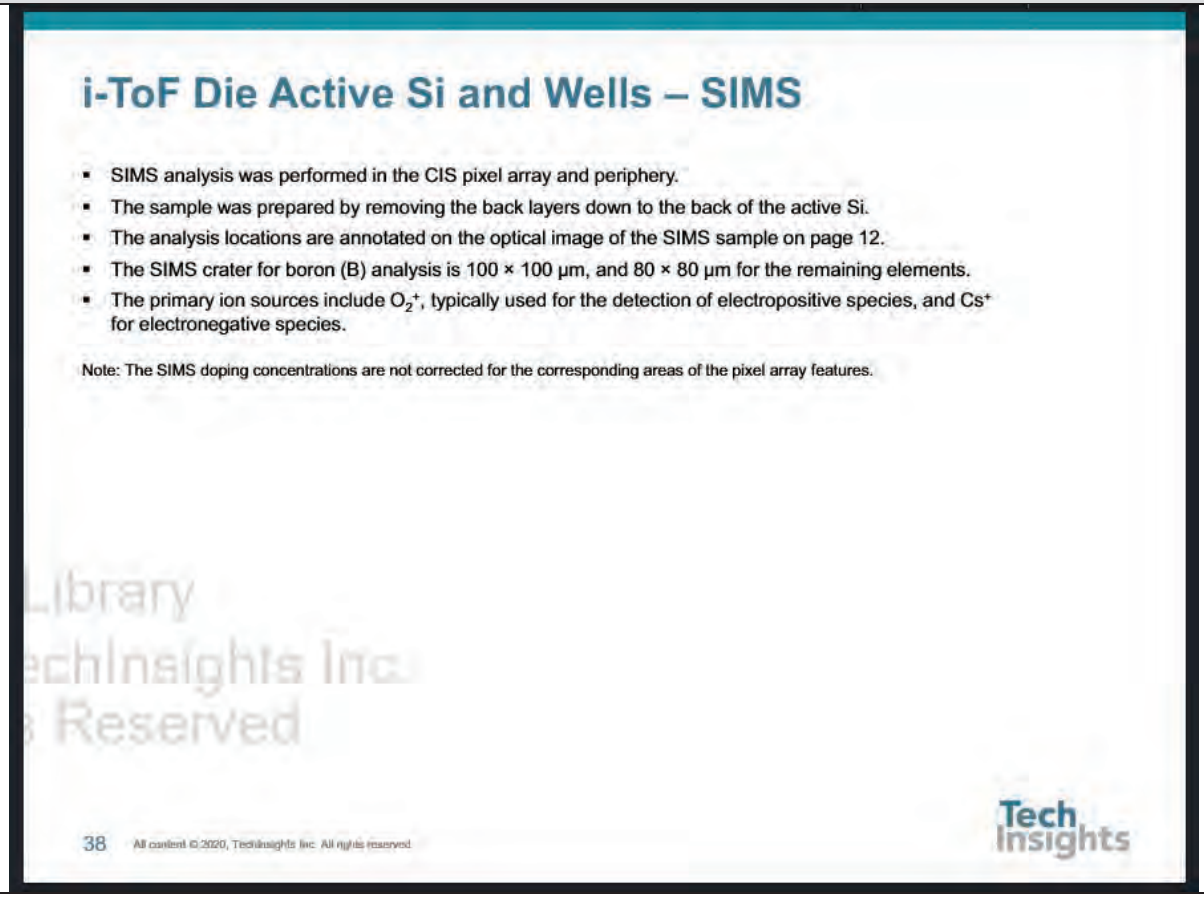
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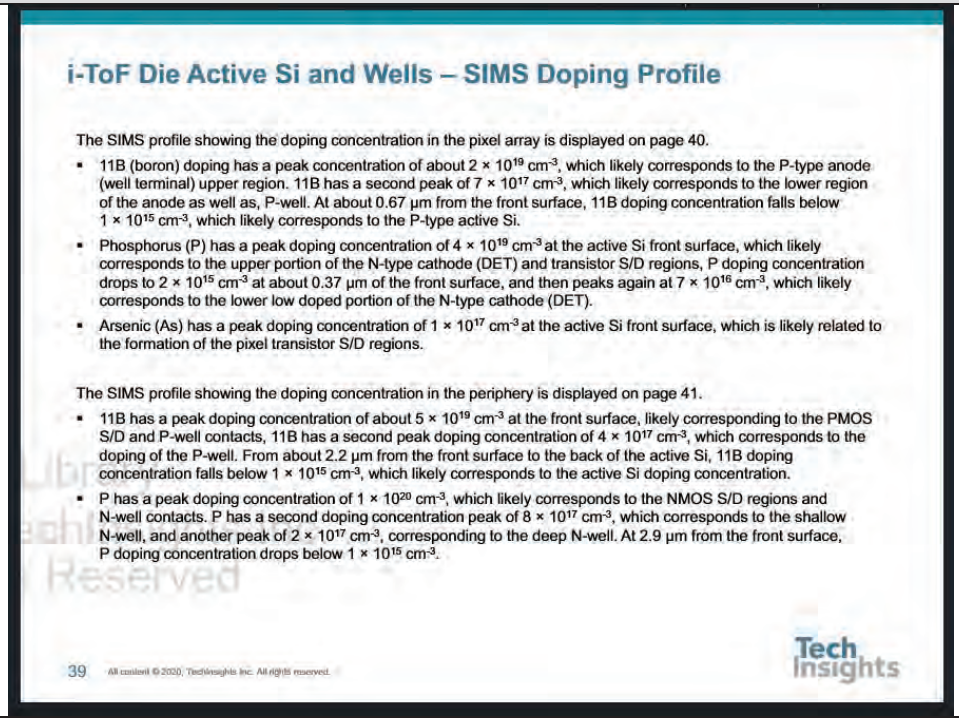
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i-ToF Die Active Si and Wells – SIMS Doping Profile

The SIMS profile showing the doping concentration in the pixel array is displayed on page 40.

- 11B (boron) doping has a peak concentration of about 2×10^{19} cm^{-3}, which likely corresponds to the P-type anode (well terminal) upper region. 11B has a second peak of 7×10^{17} cm^{-3}, which likely corresponds to the lower region of the anode as well as, P-well. At about 0.67 µm from the front surface, 11B doping concentration falls below 1×10^{15} cm^{-3}, which likely corresponds to the P-type active Si.
- Phosphorus (P) has a peak doping concentration of 4×10^{19} cm^{-3} at the active Si front surface, which likely corresponds to the upper portion of the N-type cathode (DET) and transistor S/D regions, P doping concentration drops to 2×10^{15} cm^{-3} at about 0.37 µm of the front surface, and then peaks again at 7×10^{16} cm^{-3}, which likely corresponds to the lower low doped portion of the N-type cathode (DET).
- Arsenic (As) has a peak doping concentration of 1×10^{17} cm^{-3} at the active Si front surface, which is likely related to the formation of the pixel transistor S/D regions.

The SIMS profile showing the doping concentration in the periphery is displayed on page 41.

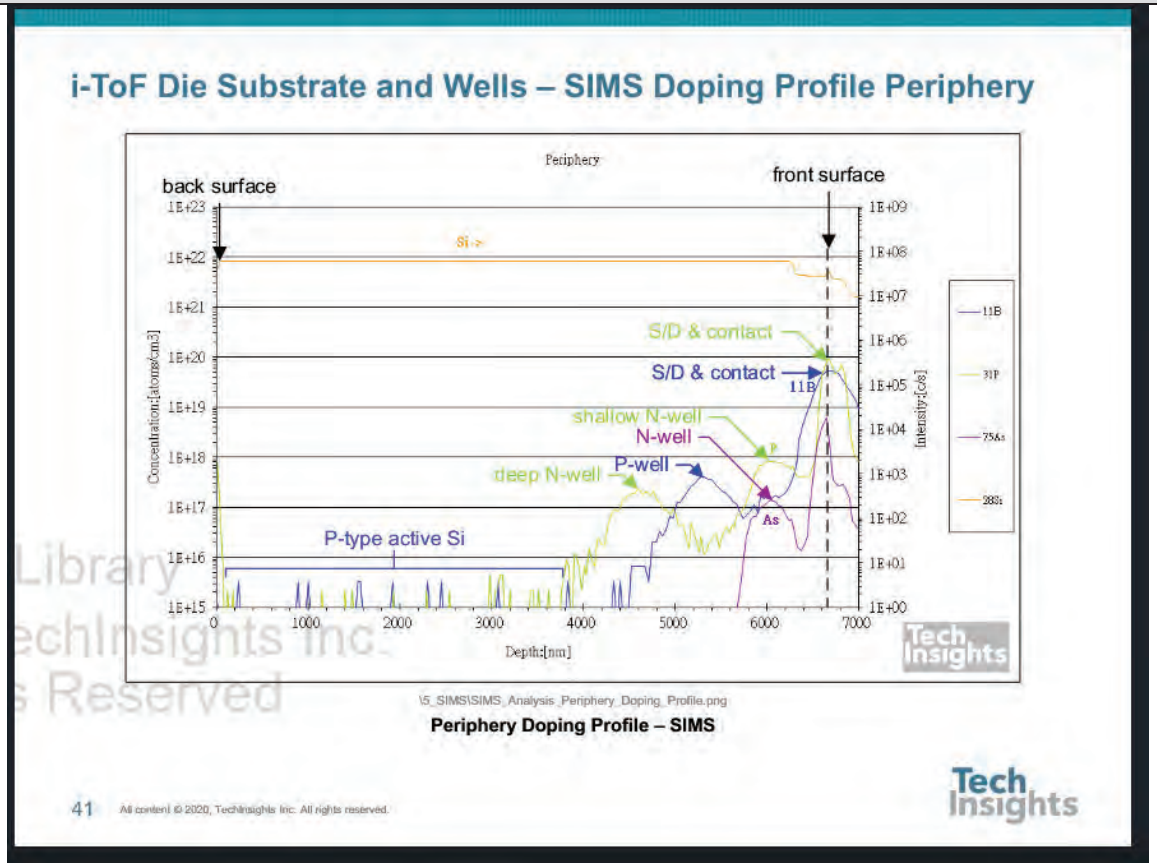
- 11B has a peak doping concentration of about 5×10^{19} cm^{-3} at the front surface, likely corresponding to the PMOS S/D and P-well contacts, 11B has a second peak doping concentration of 4×10^{17} cm^{-3}, which corresponds to the doping of the P-well. From about 2.2 µm from the front surface to the back of the active Si, 11B doping concentration falls below 1×10^{15} cm^{-3}, which likely corresponds to the active Si doping concentration.
- P has a peak doping concentration of 1×10^{20} cm^{-3}, which likely corresponds to the NMOS S/D regions and N-well contacts. P has a second doping concentration peak of 8×10^{17} cm^{-3}, which corresponds to the shallow N-well, and another peak of 2×10^{17} cm^{-3}, corresponding to the deep N-well. At 2.9 µm from the front surface, P doping concentration drops below 1×10^{15} cm^{-3}.

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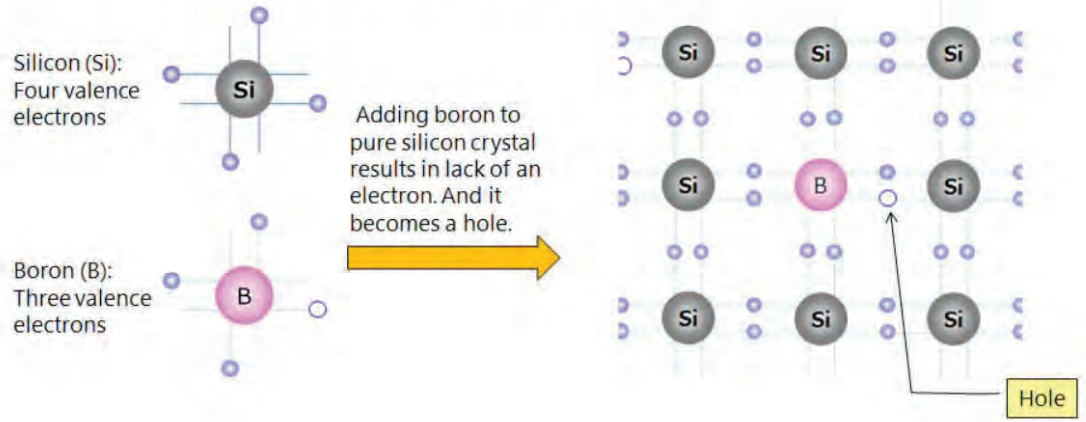
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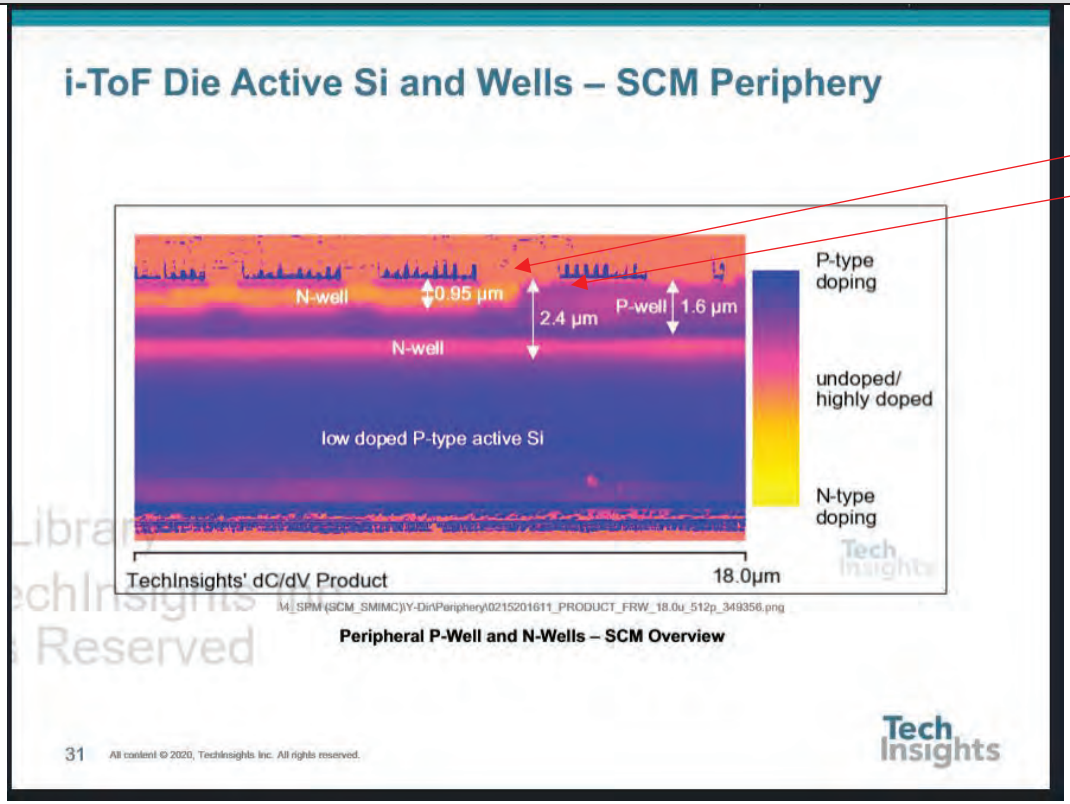


Boron (having chemical symbol B) has three valence electrons and is a p-type dopant.

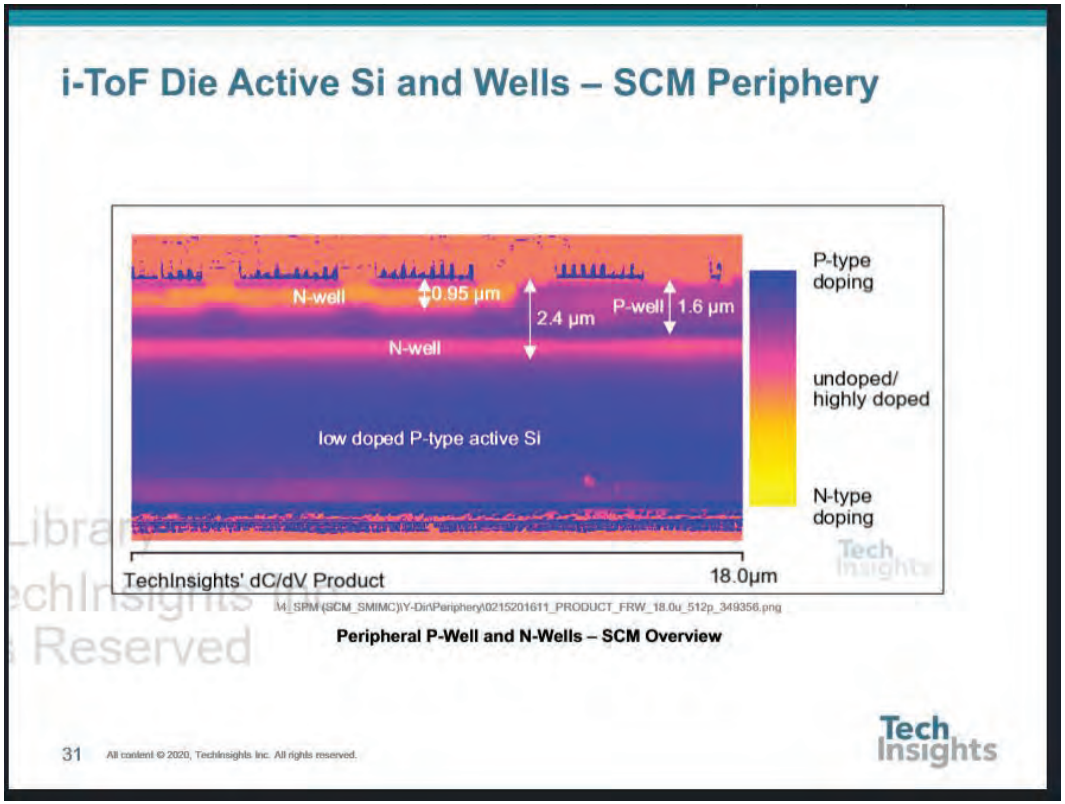
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	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons. Thus, the SIMS graph above shows the concentration of boron, which is a p-type (first doping type) dopant, at a first doping level.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second	The Sony Accused Transistor Products, and products incorporating them, include/Comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary Sony IMX516 scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. Active regions in the adjacent P-Wells and N-Wells shown in the Tech Insights Report are of opposite conductivity. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1. *See* annotation to Tech Insights Report page 31 at F-1 Claim 1 Element 2.

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doping type opposite in conductivity to the first doping type and within which transistors can be formed;	
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Sony Accused Transistor Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, as shown in the SCM image below, a second active region separate from the first active region is disposed adjacent to the first active region. Transistors are formed within the N-Wells and P-Wells shown below said transistors having active regions. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1.

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[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Sony Accused Transistor Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at Preamble, Elements 2-3, including Tech Insights Report pg. 3 (discussing "transistors").

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[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The Sony Accused Transistor Products meet this limitation. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1. For example, this is shown by the SIMS and scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis. SCM/SMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/SMIM maps taken from Sony Accused Transistor Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. The graded dopant concentration is also observed from the SIMS analysis discussed above. For more detail regarding SIMS testing, see Chart A-1. *See also* Dkt. Nos. 68 and 69 (further explaining the how to understand data from SCM, SIMS and SMIM).
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The substrate of the semiconductor device of the Sony Accused Transistor Products is a p-type substance, as discussed above and shown in SCM/SMIM, and SIMS analysis above.
4. The semiconductor device of claim 1, wherein the substrate has epitaxial	The substrate of the semiconductor device of the Sony Accused Transistor Products has epitaxial silicon on top of a nonepitaxial substrate. Upon information and belief, the substrate used in the Sony Accused Transistor Products is a single-crystal silicon wafer.

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silicon on top of a nonepitaxial substrate.	
5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Sony Accused Transistor Products meet this limitation. As discussed above for element 2 of claim 1, the first active region has n-type doping. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1. The first active region accordingly contains p-channel devices. The second active region also has n-type doping and contains p-channel devices. Thus, the first active region and second active region contain p-channel devices, which are located at the light-shaded regions out of the alternating light- and dark-shaded regions of the image below. 
6. The semiconductor device of claim 1,	The Sony Accused Transistor Products meet this limitation. The first active region and second active region have n-type dopant and contain p-channel devices in n-wells and n-channel devices in p-wells. *See* Claim 5 above. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1.

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wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the first active region and second active region are each separated by at least one isolation region. For example, isolation regions are annotated in the images discussed above for Claim 1, Element 2. Information about the fabrication process for the Sony Accused Transistor Products including usage of isolation regions, which are commonly used in semiconductor processing, is in the possession of Defendants and is expected to be obtained through discovery. *See, e.g.*, Tech Insights Report at pg. 33 annotating "STI."
8. The semiconductor device of claim 1, wherein the graded dopant is	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Sony Accused Transistor Products. Information about the fabrication process for the Sony Accused Transistor Products, including usage of an ion implantation process, is in the possession of Defendants and is expected to be obtained through discovery.

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fabricated with an ion implantation process.	
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include/comprise a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

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which transistors can be formed in the surface thereof;	
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5]	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 5.

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at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	
10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 2.
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 4.

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13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 6.
15. The	Upon information and belief, the Sony Accused Transistor Products meet this limitation. *See* above at Claim 7.

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semiconductor or device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	
16. The semiconductor or device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Sony Accused Transistor Products meet this limitation. *See* above at Claim 8.
17. The semiconductor or device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Elements 2 and 3.

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substrate.	
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The Sony Accused Transistor Products meet this limitation. *See* https://www.sony.com/en/SonyInfo/News/Press/201807/18-060E/ (describing the Sony IMX586 as a CMOS device) As discussed above for Claim 1, the Sony Accused Transistor Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery.

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[Claim 1, Preamble] A semiconductor device, comprising:	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Preamble.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 4.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 5.

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[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Sony Accused Transistor Products meet this limitation. As shown in the SIMS SCM and SIMMS analysis in the Tech Insights Report (see chart F-1 for discussion of SCM and SIMMS) the well regions adjacent to the active regions associated with the peripheral transistors have graded dopant regions to aid carrier movement from the furst surface to the second surface of the substrate. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 2.
3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 4.
4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 5.
5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 6.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 7.
7. The semiconductor device of claim 1, wherein the graded dopant	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 8.

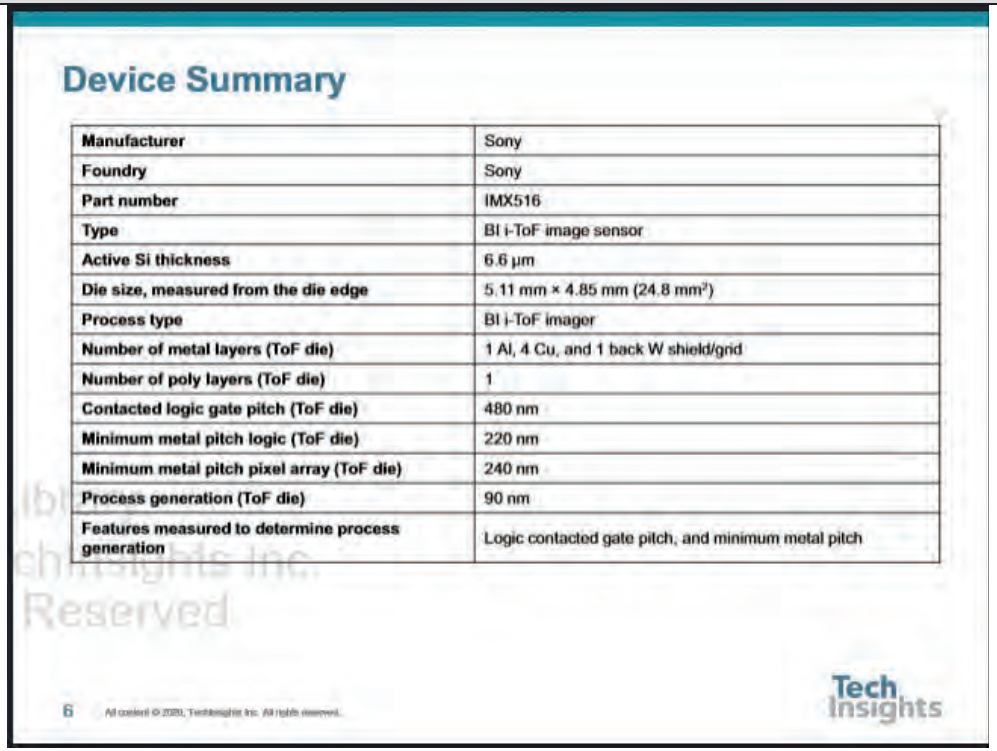
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U.S. Patent No. 10,734,481	Accused Products
is fabricated with an ion implantation process.	
8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Elements 1-3.
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Sony Accused Transistor Products meet this limitation. Dopant composition is revealed by the SIMS graph (*see* Exhibit F-1, regarding the SIMS analysis), where boron-11 is a p-type dopant and phosphorus-31 is an n-type dopant. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1.
13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 18.
15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 4 (regarding nonepitaxial substrate), Exhibit F-1 Claim 18 (regarding CMOS).
17. The semiconductor device of claim 1, wherein the device is a logic device.	The Sony Accused Transistor Products meet this limitation. The transistors described above form part of the logic associated with the Sony Accused Image Sensor products. https://www.sony.com/en/SonyInfo/News/Press/201807/18-060E/ (describing IMX586 as having "built-in, original signal processing function"). See further below regarding "Logic Regions."

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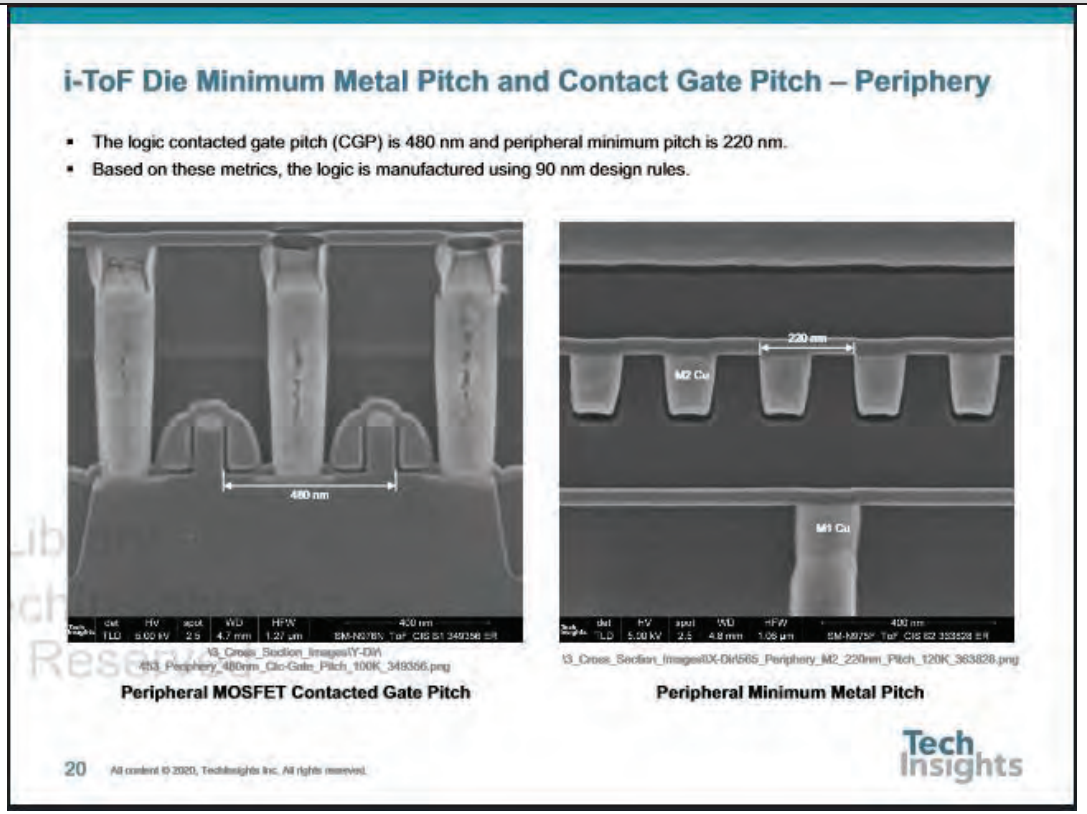
Device Summary

Manufacturer	Sony
Foundry	Sony
Part number	IMX516
Type	BI i-ToF image sensor
Active Si thickness	6.6 µm
Die size, measured from the die edge	5.11 mm × 4.85 mm (24.8 mm²)
Process type	BI i-ToF imager
Number of metal layers (ToF die)	1 Al, 4 Cu, and 1 back W shield/grid
Number of poly layers (ToF die)	1
Contacted logic gate pitch (ToF die)	480 nm
Minimum metal pitch logic (ToF die)	220 nm
Minimum metal pitch pixel array (ToF die)	240 nm
Process generation (ToF die)	90 nm
Features measured to determine process generation	Logic contacted gate pitch, and minimum metal pitch

Reserved

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Tech Insights

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19. The semiconductor device of claim 1, wherein the device is an image sensor.	See Exhibit F-1, Preamble.
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include/comprise a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 9, Element 2.

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U.S. Patent No. 10,734,481	Accused Products
surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 9, Element 3.
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 6, Element 1.
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 2.
23. The semiconductor device of claim 20, wherein the substrate has	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 4.

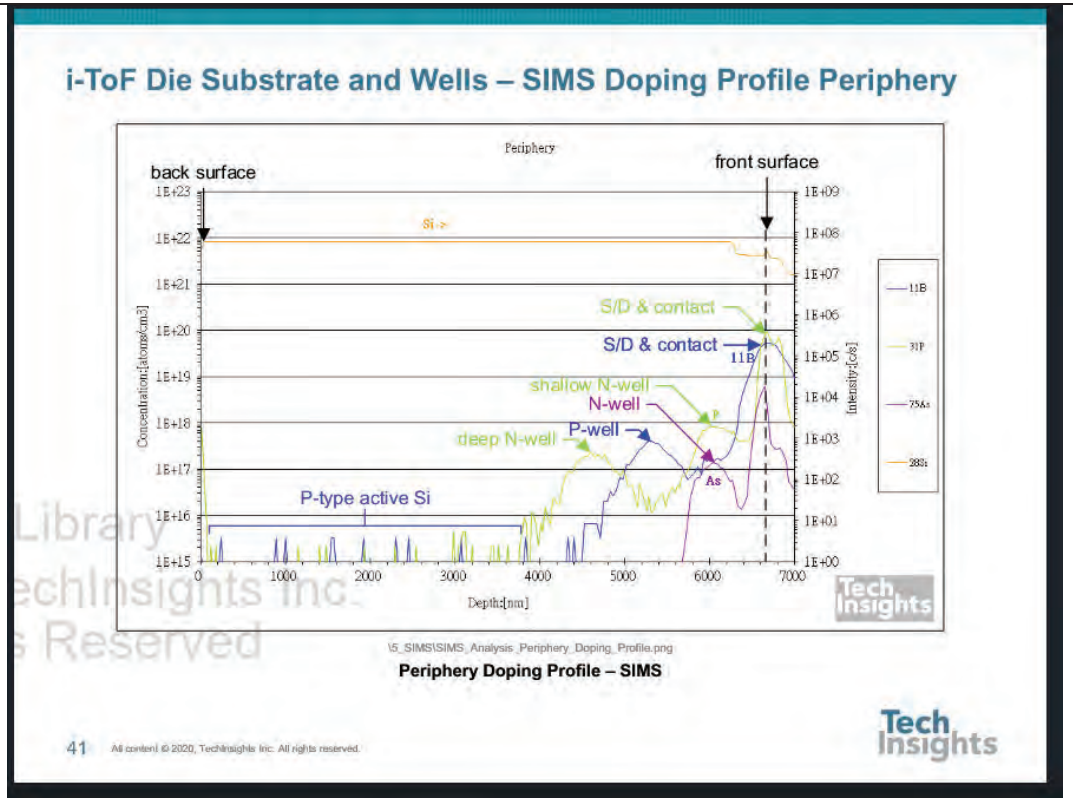
U.S. Patent No. 10,734,481	Accused Products
epitaxial silicon on top of a nonepitaxial substrate.	
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 5.
25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 6.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 7.
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 8.
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 15.

Exhibit F-2 to Greenthread's Further Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 10,734,481	Accused Products
34. The semiconductor device of claim 20, wherein the device is a logic device.	The Sony Accused Transistor Products meet this limitation. On information and belief, the transistors described above form part of the logic associated with the Sony Accused Image Sensor products. *See* above at Claim 19.
36. The semiconductor device of claim 20, wherein the device is an image sensor.	The Sony Accused Transistor Products meet this limitation. *See* Chart F-1 Claim 1 Preamble.

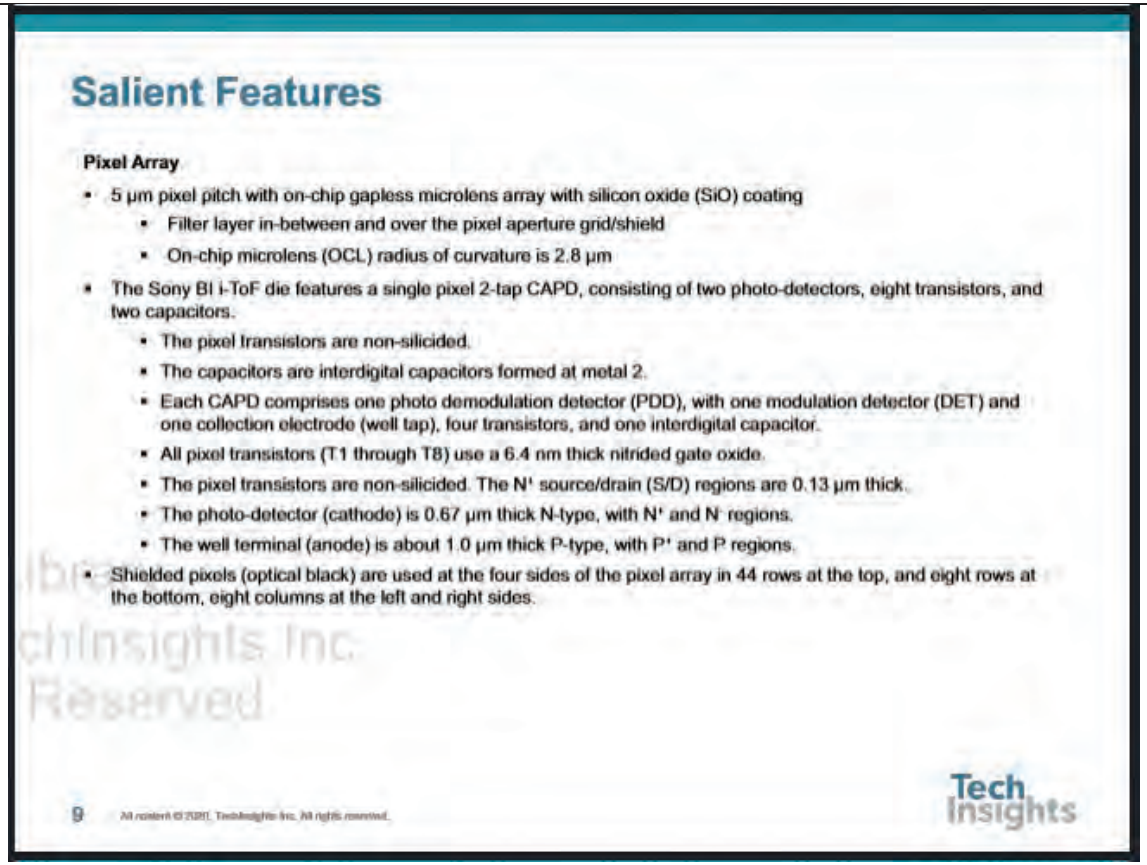
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U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include/comprise a VLSI semiconductor device. Each Sony Accused Product has millions of transistors, and is a VLSI semiconductor device. *See* https://www.dictionary.com/browse/vlsi *See* https://www.sony.com/en/SonyInfo/News/Press/201807/18-060E/ (describing the Sony IMX586 as having 48 megapixels)
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 4.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 5. As shown below, the areas within the N- and P-wells corresponding to the active regions (i.e. closer to the "front surface" than the areas annotated as "N-Well" or "P-Well") contain at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions. This is confirmed by other testing as well. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1.

area of the substrate where there are no active regions; and	
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-2, Claim 1, Element 6; Exhibit F-2, Claim 17 (digital logic). *See also* Claim 1 Element 5 above.

2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 2.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 6; Exhibit F-2, Claim 5; Exhibit F-2, Claim 17.
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Elements 1-3.

9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-2, Claim 13.
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-2, Claim 15.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The Sony Accused Transistor Products meet this limitation. For logic limitation see Exhibit F-2, Claim 17. The Sony IMX516 also include capacitors see below.

	
19. The VLSI semiconductor device of claim 1, wherein the device is an image sensor.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-2, Claim 19.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The Sony Accused Transistor Products meet this limitation. As shown by SEM imaging (see Exhibit F-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include a semiconductor device. *See* above at Claim 1, Preamble.

[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 9, Element 2.
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-2, Claim 1, Element 6. As shown by SIMS analysis, the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SIMS plot. *See* Tech Insights Report pg. 31-33, 41 reproduced at F-1 Claim 1, Element 1 (annotating well regions). *See also* Exhibit F-1, Claim 1, Element 5 showing carrier movement.

active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 2.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 5.
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-2, Claim 9.

region are either p-type or n-type.	
32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 8.
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 15.
35. The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-2, Claim 17 (regarding logic device); *see* above at Claim 17 (regarding capacitors). Upon information and belief, the capacitors are in at least some of the first or second active regions, because capacitors are commonly formed in active regions of semiconductor devices.
37. The VLSI semiconductor device of claim 21, wherein the device is an image sensor.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, preamble.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 20.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include a semiconductor device. *See* above at Claim 1, Preamble; Exhibit F-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 2; *see also* Exhibit F-1, Claim 1, Element 2.

type and within which transistors can be formed;	
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 6; Exhibit F-1, Claims 6, 14.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1.

[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 5. SIMS analysis (*see* Exhibit F-1, Claim 1, Element 1) reveals at least one graded dopant acceptor concentration (e.g., concentration of boron-11) as claimed. *See also* Exhibit F-1, Claim 1, Element 5 (showing carrier movement).
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 39, Element 2.

type and within which transistors can be formed;	
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 39, Element 5. SIMS analysis (*see* Exhibit F-1, Claim 1, Element 1) reveals at least one graded donor dopant concentration (e.g., concentration of phosphorus-31) as claimed. Exhibit F-1, Claim 1, Element 5 (showing carrier movement).

Exhibit F-6 to Greenthread's Further Amended Preliminary Infringement Contentions (1/23/2023)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include an electronic system. *See* Exhibit F-1, Claim 1, Preamble.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 1, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 1, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 1, Element 4.
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 1, Element 5. *See also* Exhibit F-1, Claim 1, Element 5 (showing carrier movement).
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 1, Element 6. *See also* Exhibit F-1, Claim 1, Element 5 (showing carrier movement).

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U.S. Patent No. 11,316,014	Accused Products
movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 2.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 5.
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 8.

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device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 15.
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 17.
19. The system of Claim 1, wherein the at least one semiconductor device is an image sensor.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 19.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Sony Accused Transistor Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1a.

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Exhibit F-6 to Greenthread's Further Amended Preliminary Infringement Contentions (1/23/2023)

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[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit F-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit F-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit F-1, Claim 9, Element 5. *See also* Exhibit F-1, Claim 1, Element 5 (showing carrier movement).
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Sony Accused Transistor Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit F-3, Claim 21, Element 6. *See also* Exhibit F-1, Claim 1, Element 5 (showing carrier movement).

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23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 26.
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Sony Accused Transistor Products meet this limitation. *See* Exhibit F-3, Claim 28.

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