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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
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Title of Invention

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	2783	FILED BY	Joselyn Rodriguez
PATENT CENTER #	66616031	FILING DATE	04/25/2022
CUSTOMER #	25883	FIRST NAMED INVENTOR	G.R. MOHAN RAO
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	William Howison

Documents

TOTAL DOCUMENTS: 4

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
GRTD60-35367 RSP AMD.pdf		16	-	259 KB
GRTD60-35367 RSP AMD-A....pdf	(1-1)	1	Amendment/Request for Reconsideration-After Non-Final Rejection	92 KB
GRTD60-35367 RSP AMD-CLM.pdf	(2-7)	6	Claims	123 KB
GRTD60-35367 RSP AMD-REM.pdf	(8-16)	9	Applicant Arguments/Remarks Made in an Amendment	217 KB
GRTD60-35367 Declaration		11	Affidavit-traversing rejections or	250 KB

of Douglas Holberg under 37 USC Section 1.132.pdf | objections rule 132

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
GRTD60-35367 RSP AMD.pdf	9FF9C637B6F76CF5A422D510CD1A4225D2FCA68CC8074D271DF05CADC11755AE9601AD23F38F59FE41F728E2DBF63927FC41B03925174E2B34633B1AC490395E
GRTD60-35367 RSP AMD-A....pdf	3F4963344780AC58169C19CF1987EF9792E6A8CD1919CC57E0FE7E3ECCD42F2EB2C1F5B701E70A5198115EC23807DBD033AC8527F5B8366A5ABFDF057CB3C066
GRTD60-35367 RSP AMD-CLM.pdf	101425CD3B9D92A4A25FC2F1434C258DC34AB560E1C91B2304798134FBF58332F0C378BEEF32B17739413E6C97D4E8EF263FCE5B111713CFFE696BC132BBF1B0
GRTD60-35367 RSP AMD-REM.pdf	BF882987F34A046BB26DCE1D49D30EA2A5E289A5D5CAA722A2112F61BC92265E6F7A323F984D428F3DD9810D4F0515424F8B8BE9A15702361C5D36B60A1D9A6F
GRTD60-35367 Declaration of Douglas Holberg under 37 USC Section 1.132.pdf	E06C2A1A31500497D2FC3462998E9D2ECDC9A30D00F85AC0C1C48B6D2019CE3E212F0C04AC7829898E460C6950080581AE869AE6E1BD5D5B048C6AB111A8B9A5

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If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G.R. MOHAN RAO
Serial No.:	17/728,588
Confirmation No.:	2783
Filed:	April 25, 2022
Group:	2892
Examiner:	Ajay ARORA
For:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
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Dear Sir:

AMENDMENT AND RESPONSE TO OFFICE ACTION

This communication is responsive to the Examiner's Office Action dated July 18, 2024. Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper. **Remarks/Arguments** begin on page 8 of this paper.

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In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electronic system, the system comprising:

at least one semiconductor device, the at least one semiconductor device including:

a substrate of a first doping type at a first doping level having a surface;

a first well region disposed proximate the surface with a second doping type opposite in conductivity to the first doping type and extending downward into the substrate and having a bottom surface, and having a first active region within which at least one transistor can be formed;

a second well region separate from the first well region and adjoining the first well region and extending downward into the substrate and having a bottom surface, and having a second active region within which at least one transistor can be formed;

at least one transistor formed in at least one of the first active region or second active region, the at least one transistor having a channel region in which a conductive channel can be formed;

at least one of the first and second well regions having at least one graded dopant concentration having a slope throughout the respective region creating a suitable aiding drift electric field to aid minority carrier movement from the at least one of the first or second active regions having the at least one transistor formed therein ~~towards the respective bottom thereof and~~ deep into the substrate in a direction towards an area of the substrate where there are no active regions; and

at least one subterranean well region adjoining the bottom surface of the first or second well regions and having a bottom surface diametrically opposite the adjoined one of the first or second well regions and containing at least one graded dopant concentration and the at least one subterranean well region separating the first and second well regions with the respective first and second active regions from the area of the substrate where there are no active regions, the graded dopant concentration having a relative slope throughout the respective region creating a

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suitable aiding drift electric field to aid minority carrier movement from the bottom of the at least one of the first and second active regions ~~towards the bottom surface of the at least one subterranean well region~~ deep into the substrate, to aid minority carrier movement from the at least a portion of at least one of the first and second active regions having at least one graded dopant concentration towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.

2. (Original) The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.

3. (Original) The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.

4. (Original) The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.

5. (Original) The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. (Original) The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.

7. (Original) The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. (Previously Presented) The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the surface of the substrate of the at least one semiconductor device.

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9. (Original) The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.

10-11. (Cancelled)

12. (Previously Presented) The system of Claim 1, wherein dopants of the graded dopant region in the at least one well region of the at least one semiconductor device are one of either p-type or n-type.

13. (Previously Presented) The system of claim 1, wherein the at least one transistor which can be formed in the first or second active regions of the at least one semiconductor device is a CMOS digital logic transistor requiring at least a source, a drain, a gate and a channel.

14. (Original) The system of Claim 1, wherein the at least one semiconductor device is a dynamic random access memory (DRAM).

15. (Original) The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. (Original) The system of Claim 1, wherein the at least one semiconductor device is a flash memory.

17. (Original) The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.

18. (Original) The system of Claim 1, wherein the at least one semiconductor device is a central processing unit.

19. (Original) The system of Claim 1, wherein the at least one semiconductor device is an image sensor.

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20. (Original) The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.

21. (Currently Amended) An electronic system, comprising:

at least one semiconductor device, the at least one semiconductor device including:

a substrate of a first doping type at a first doping level having a surface;

a first well region disposed proximate the surface of the substrate with a second doping type opposite in conductivity to the first doping type and extending downward into the substrate and having a bottom surface, and having a first active region within which at least one transistor can be formed in the surface thereof;

a second well region separate from the first well region and adjoining the first well region and extending downward into the substrate and having a bottom surface, and having a second active region within which at least one transistor can be formed in the surface thereof;

at least one transistor formed in at least one of the first active region or second active region, the at least one transistor having a channel region in which a conductive channel can be formed;

at least one of the first and second well regions having at least one graded dopant concentration having a slope throughout the respective region creating a suitable aiding drift electric field to aid minority carrier movement from the surface ~~towards the respective bottom thereof and~~ deep into the substrate in a direction to an area of the substrate where there are no active regions; and

at least one subterranean well region adjoining the bottom surface of the first or second well regions and having a bottom surface diametrically opposite the adjoined one of the first or second well regions and containing at least one graded dopant concentration and the at least one subterranean well region separating the first and second well regions with the respective first and second active regions from the area of the substrate where there are no active regions, the graded dopant concentration having a ~~relative~~ slope throughout the respective region creating a suitable aiding drift electric field to aid minority carrier movement from the bottom of the at least one of the first and second well regions ~~towards the bottom surface~~

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~~of the at least one subterranean well region~~ deep into the substrate, to aid minority carrier movement from the at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

22. (Previously Presented) The system of Claim 21, wherein the substrate of the at least one semiconductor device is an n-type substrate.

23. (Previously Presented) The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.

24. (Previously Presented) The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.

25. (Previously Presented) The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.

26. (Cancelled)

27. (Previously Presented) The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.

28-31. (Cancelled)

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32. (Previously Presented) The system of Claim 1, wherein the carriers are either holes or electrons.

33. (Cancelled)

34. (Previously Presented) The electronic system of Claim 21, wherein the carriers are either holes or electrons.

35. (Previously Presented) The system of Claim 1, wherein the conductive channel is oriented in a vertical direction to the surface of the substrate for conduction in a vertical direction.

36. (Previously Presented) The system of Claim 1, wherein the conductive channel is oriented in a planar direction to the surface of the substrate for conduction in a planar direction.

REMARKS

Applicant has carefully reviewed the Office Action dated July 18, 2024. Applicant has amended Claims 1 and 21 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

35 USC § 112(a) Rejection

Claims 1 – 9, 12 – 25, 27, 32 and 34 – 36 name rejected and the 35 U.S.C. §112 (a). This rejection is respectfully traversed.

The Examiner has taken the position that the claims contained subject matter which was not described in the Specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or joint inventor had possession of the claimed invention of the base claims 1 and 21. The specific language (pre-Amendment) the Examiner is addressing is as follows:

"at least one of the first and second well regions having at least one graded dopant concentration having a slope throughout the respective region creating a suitable aiding drift electric field to aid carrier movement from the at least one of the first or second active regions having the at least one transistor formed therein towards the respective bottom thereof and in a direction towards an area of the substrate where there are no active regions"

"at least one subterranean well adjoining the bottom surface of the first or second well regions and having a bottom surface diametrically opposite the adjoined one of the first or second well regions and containing at least one graded dopant concentration" and "the graded dopant concentration having a slope throughout the respective region creating a suitable aiding drift electric field to aid carrier movement from the bottom of the at least one of the first and second well regions towards a bottom surface of the at least one subterranean well region to aid carrier movement from the at least a portion of at least one of the first and second active regions ..... " (Emphasis from Office Action)

In order to describe how the term "gradient" is utilized and described and supported in the Specification, Applicant will try to step through how such as introduced and utilized in the Specification. In addition, the declaration under 37 CFR 1.132 of Douglas Holberg as an expert is filed herewith as support for this discussion. Applicant additionally notes that although the below arguments address the Examiner's arguments pertaining to the pre-Amendment claims, Applicant's arguments also apply to the claims as amended herein.

In ¶[0011], a description of a p-n-p transistor is set forth specifically with respect to Figure 1:

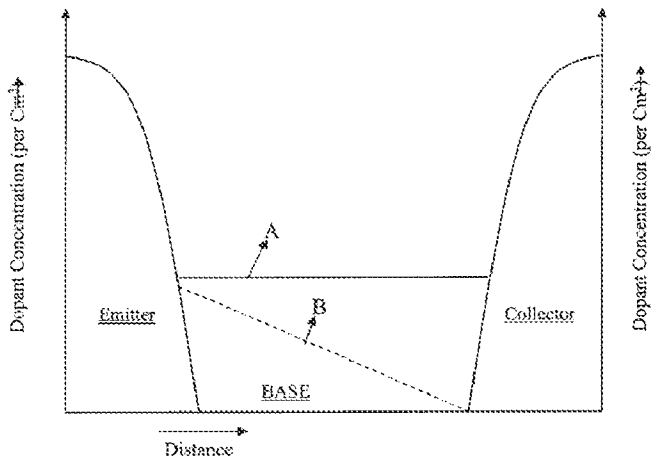

Figure 1 Prior Art

The structure of this transistor is described as having a base region that has a donor dopant concentration gradient that is high at the emitter-base junction and low at the base-collector injunction. This corresponds to the label "B" in Figure 1. This is defined as a "relative slope" which means nothing more than the fact that one-side is relatively lower than the other side. This slope is defined "throughout" the base to create "a suitable aiding drift electric field, to help the holes (p-n-p transistor) traverse from the emitter to collector. In an n-type material, the holes are "minority" carriers. This particular structure is noted as being Prior Art and the minority carriers

are injected as a result of placing a voltage across the transistor. It is also noted that this is "applicable" to n-p-n transistors. Of course, in an n-p-n transistor, p-type minority carriers are transitioning across a p-type base and the minority carries for the p-type material are electrons. Thus, this ¶[0011] describes a gradient for aiding the movement of minority carriers from one point to another through a region. In order to do such, a drift electric field is created via the gradient. The purpose is not to assist movement of the minority carriers "partially" through the region but, rather, from one border to the other.

In the embodiment related to the claims, that with respect to Figures 5A, 5B and 5C in ¶ [0013], the Specification at ¶0013] describes the use of the "donor gradient" as being of a benefit to very large scale integrated circuits. The purposes stated are a desire to remove minority carriers at the surface that are spuriously generated by clock switching, which can discharge various "actively held high" nodes. The use of the gradient dopant profile is noted as a "novel technique" that "creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible." It is also stated that the creation of "subterranean" recombination centers underneath the wells "is not practical for VLSI circuits." Thus, this statement teaches against impeding movement of minority carriers downward within any layer. The embodiment initially refers to a subterranean n^- layer as having a graded donor concentration (an n-type material) to sweep the minority carriers (holes) "deep into the substrate." Since this is an n-type material, it is a "donor" type material and would have a slope resulting in a drift field that would aid in moving minority carriers (holes in an n-type material) in a direction away from the active circuitry and "into the substrate." In a p-type material, the minority carriers would be electrons.

Applicant believes that a POSITA would recognize that the description of a donor dopant concentration for creating a drift electric field that aids movement of minority carriers within a region from one boundary of that region to the other boundary thereof in any embodiment in the Specification would necessarily define that gradient as to all embodiments. The function of the graded dopant concentration in the embodiment of Figure 1 (¶[0011]) is identical to the function of the graded dopant concentration described with respect to the embodiments of Figures5A, 5B

and 5C. It is to create an electric field to aid in movement of minority carriers from one boundary to the other of any region.

The Examiner has stated with respect to how the donor gradient is described with respect to the description of ¶[0011] (Figure 1) as follows: "[t]hus, the disclosure of the graded dopant or 'relative slope' or 'donor concentration throughout the base' are only with respect to base of a p-n-p transistor." Applicant disagrees with this position. The description of the base and the concentration thereof is a description of a region having a boundary. This region is a region through which carriers are transmitted from one side to the other. The gradient therethrough is described with respect to a donor region, i.e., an n-type region, that just happens to be utilized as the base of a transistor in the disclosed embodiment. But it is still nothing more than a region through which carriers are transmitted and the function of that gradient is to create "a suitable aiding drift electric field, to help the holes (minority carriers in a p-n-p transistor) traverse from emitter to collector." The emitter is just one boundary with the base and the collector is the other boundary with the base, but the base is just a region disposed therebetween through which holes (minority carriers for a p-n-p transistor or electrons as minority carriers for an n-p-n transistor) can traverse. The gradient just affects the function of that traversal within the particular region, which region just happens to be a base. But that function is not restricted only to a transistor; rather, it just describes a function of that region.

The Examiner's assertion that the term "throughout" is only relevant to the function of the base of a transistor is incorrect. In the embodiment of ¶ [0011], the Specification refers to the benefits of using a "donor gradient" as "also" providing a benefit. This benefit is defined as creating "a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate …" This language is consistent with the function of the donor gradient in the base of the transistor in the embodiment of ¶[0011]. This function cannot happen unless the gradient extends from one side of a region to the other. If not, then the minority carriers would be swept into some middle portion of a region and not "into the substrate." A POSITA would, from the reading of the embodiment of ¶[0013] understand that the donor gradient has a profile that is decreasing from one side to the other such that an electric drift field is created to aid movement of minority carriers from one side of the region (or well) to the other side thereof. The Examiner's

assertion that the description of the transistor base in the embodiment of ¶[0011] with respect to the functionality thereof is only applicable to the transistor embodiment is believed to be incorrect. It seems that the Examiner is taking the position that a description of one embodiment, that of ¶[0011] and the description that the gradient profile extends from one side to the other, i.e., "throughout," is such that it only applies to the description with respect to the transistor and cannot be extended to any other embodiment. However, a POSITA would understand that the functionality provided by that doping profile and gradient relative to the operation of a transistor is the same functionality that is described with respect to the embodiment of ¶[0013] in that the minority carriers are moved from one area to another deep into the substrate with the gradient providing the same function i.e., creating an electric drift field to aid the movement of carriers. Additionally, it would be unreasonable to not consider that the gradient extends all the way through the region or well because the specification specifically says that creation of "subterranean" recombination centers underneath the wells "is not practical for VLSI circuits." If the gradient does not extend all the way through the region, there is no way for the carriers to move into the substrate, as they would recombine within the region.

Thus, Applicant respectfully requests withdrawal of the 35 U.S.C. § 112 rejection with respect to Claims 1 – 9, 12 – 25, 27, 32 and 34 – 36.

<u>35 USC § 103 Rejection</u>

Claims 1 – 19, 12 – 13, 15, 20, 32, 34 and 36 stand rejected under 35 U.S.C. §103 as being unpatentable over *Yamashita* in view of *Kawagoe*. This rejection is respectfully traversed in view of the claims as currently amended.

The Examiner is utilizing the specification of *Yamashita* as disclosing the limitation of a gradient that creates an electric field to aid movement of minority carriers from one side of a region to another side of a region. The Examiner refers to the disclosure at Col. 24, line 64 to Col. 25, line 5 as supporting this. However, this language merely states that any electrons created "in the substrate" are prevented from moving upward because of the retrograde well. There is no dopant concentration having a gradient that extends from one side of a well to the other side thereof that creates an electric field that actually aids movement to the substrate. Rather, all this structure does

is prevent electrons that are created by α-rays from leaving the substrate and moving upwards across the layer. Since this is a retrograde junction, there is a peak that actually prevents or prohibits electron movement "from the substrate." This does not disclose any gradient across the layer that would in any way create an electric field for the purpose of aiding movement down into the substrate from the upper side of the substrate. Electrons are actually moving in the opposite direction away from a higher concentration, i.e., they exist below the high concentration and are not moved away from that high concentration and into the substrate.

The Examiner also refers to the disclosure of Figure 66 and Figure 71 as describing different graded dopant concentration profiles. These figures illustrate nothing more than a number of layers having retrograde dopant profiles for the peak profile concentration in the middle of the layer. These peaks prevent movement across the layer and do not suggest any operation that would create an electric field that would aid movement of minority carriers from one side of the region to the other side of the region.

The Examiner then utilizes the disclosure of *Kawagoe* as teaching a solution of a similar problem, that is "to counter the influenced caused to carriers due to α-rays, citing Col. 16, lines 2 – 7. This portion of the specification to set forth as follows:

> …. and the p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration NW) of the epitaxial layer 2E. Thus, the impurity concentration of the p-well 6p is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient **and prevented from entering the p-well 6p so that the soft errors can be reduced** in case the MIS memory of the DRAM or the like is formed in the p-well 6p. (Col. 15, line 66 to Col. 16, line 11) (Emphasis added).

Here, *Kawagoe* discloses a system that has a specific purpose of preventing any stray electrons from leaving the substrate and entering the P well 6p. There is no disclosure for creating a drift field for aiding movement of minority carriers from the upper surface to the substrate, since the free electrons are already in the substrate. This function is not described in *Kawagoe*, as that

is not the purpose of *Kawagoe*. The purpose is to prevent movement from the substrate of minority carriers, and this is also the precise purpose of *Yamashita*. Thus, *Kawagoe* and *Yamashita* both failed to disclose any creation of an electric drift field for the purpose of aiding movement of minority carriers from the surface substrate beneath or proximate an active region deep into the substrate. Just the existence of an active region above the P-well does not mean there are any minority carriers or undesired electrons requiring movement toward or into the substrate. The stray electrons are ones that are generated in the substrate and the purpose of both *Yamashita* and *Kawagoe* is to prevent the stray electrons from moving upward into the well, i.e., they are prevented from moving upward.

The Examiner's position is that the doping profile of *Yamashita* for both adjacent p-type layers can be replaced with the doping profile of *Kawagoe* and Figure 66. The primary question presented is why would a POSITA be motivated in any way to make such a substitution. The purpose of the doping profile and Yamashita is to prevent free electrons from moving from the substrate up to the surface and causing soft errors in the p-well. Each one of the peak doping profiles in the center would achieve such a result. In Kawagoe, the doping profile, from the perspective that the substrate, is an increasing doping profile. It is not necessary for the doping profile to increase from the bottom for the substrate to the surface of the active circuitry would exist. It is only necessary to have some upward slope toward the surface in order to prevent electrons removing from the substrate to the surface. Thus, there is no disclosure or benefit noted in Kawagoe for having the sloping service of the doping profile extend to the service in order to achieve the result of Kawagoe, that is, to prevent electrons employing from the substrate up to the p well. Thus, there would be no benefit provided to the noted problem in Yamashita, i.e., from any electrons from moving upward from the substrate to the p-well by incorporating the doping profile of Kawagoe. In the current claim invention, the purpose for having the gradient extend "throughout" the region is to move free electrons from one border of the region to another border of the region. Neither Yamashita nor Kawagoe have this requirement. Therefore, there would be no reason to substitute the doping profile of Kawagoe for the doping profile of Yamashita in both regions, as it does not in any way improve Yamashita, as both doping profiles do exactly the same thing at the substrate. Thus, a POSITA would not be motivated to substitute the doping profile of Kawagoe the doping profile of Yamashita.

Based upon the above, Applicant respectfully requests withdrawal of the 35 USC §103 rejection with respect to Claims 1 – 19, 12 – 13, 15, 20, 32, 34 and 36 because there is no reason set forth by the Examiner as to why the doping from of *Kawagoe* would be substituted for the 2 doping profiles of *Yamashita*.

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *whowison@munckwilson.com*.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 50-0208/GRTD60-35367.

Respectfully submitted,
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/728,588	Filing Date 04/25/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	08/01/2024	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 28	Minus	** 36	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/APRIL L. WALKER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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