

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION**

GREENTHREAD, LLC

Plaintiff,

vs.

CIRRUS LOGIC, INC.

Defendant.

Civil Action No. 1:23-cv-00369-DC

JURY TRIAL DEMANDED

GREENTHREAD'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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TABLE OF EXHIBITS¹

Exhibit	Description
1	Declaration of Dr. Alexander Glew (“Glew declaration”)
2	U.S. Patent No. 8,421,195 to G.R. Mohan Rao (GT-WDTX-CL_0000001-14) (“195 patent”)
3	U.S. Patent No. 9,190,502 to G.R. Mohan Rao (GT-WDTX-CL_0000015-28) (“502 patent”)
4	U.S. Patent No. 10,510,842 to G.R. Mohan Rao (GT-WDTX-CL_0000029-43) (“842 patent”)
5	Excerpts from Chen, J. Y., CMOS Devices and Technology for VLSI, Prentice-Hall (1990) (GT-WDTX-CL_0088908-88954) (“Chen”)
6	<i>Greenthread, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00147-JRG, Dkt. 67 (Claim Construction Memorandum Opinion and Order), E.D. Tex. Apr. 20, 2020 (GT-WDTX-CL_0065233-65264) (“EDTX <i>Markman</i> Order”)
7	<i>Greenthread, LLC v. Intel Corp.</i> , No. 6:22-cv-00105-ADA (email from Dr. Yi dated Dec. 21, 2022 in WDTX Greenthread case), D. Or. Feb. 8, 2023 (GT-WDTX-CL_0065441-65445) (“WDTX Preliminary Constructions”)
8	<i>Greenthread, LLC v. Intel Corp.</i> , No. 3:22-cv-02001-JR, Dkt. 44, D. Or. Mar. 16, 2023 (GT-WDTX-CL_0065365-65373) (“D. Or. Findings and Recommendation”)
9	<i>Samsung Elecs. Co., Ltd. v. Greenthread, LLC</i> , IPR2020-00289, Ex. 1003 (Apr. 14, 2020)) (GT-WDTX-CL_0050327-50417) (“Smith declaration”)
10	The American Heritage Dictionary of the English Language, Third Edition (2002), at 1792 (defining “substrate”) (GT-WDTX-CL_0020230-20234)
11	Excerpts from Webster’s Third New International Dictionary of the English Language Unabridged, Merriam-Webster, Inc. (2002) (GT-WDTX-CL_0020235-20245; GT-WDTX-CL_0065298-65314)
12	Excerpts from Baker, R. J., CMOS Circuit Design, Layout, and Simulation, IEEE (1998) (GT-WDTX-CL_0065146-65187) (“Baker”)

¹ When possible, Greenthread has cited to the exhibits previously attached to Cirrus’ Opening Claim Construction Brief (Dkt. 35). Unless otherwise indicated, all docket numbers refer to the present case, *Greenthread, LLC v. Cirrus Logic Inc.*, No. 1:23-cv-369-DC-DTG (W.D. Tex.), and all citations to page numbers of CM/ECF documents refer to the page number at the top of the page in the CM/ECF header.

Because many of the terms were previously at issue before this Court in *Greenthread, LLC v. Intel Corp.*, No. 6:22-cv-00105-ADA (W.D. Tex.), Greenthread includes some citations to the docket from that case, with the indication “*Intel* Dkt.”

13	File History of U.S. Patent No. 10,510,842 (GT-WDTX-CL_0000651-849) (“842 file history”)
14	Excerpts from Howe, R. T., <i>Microelectronics: An Integrated Approach</i> , Prentice-Hall (1997)) (GT-WDTX-CL_0065265-65285) (“Howe”)
15	Excerpts from Wolf S., <i>Silicon Processing for the VLSI Era Volume 2: Process Integration</i> , Lattice Press (1990) (GT-WDTX-CL_0020508-20521)
16	Excerpts from Wolf S., <i>Silicon Processing for the VLSI Era Volume 3: The Submicron MOSFET</i> , Lattice Press (1995) (GT-WDTX-CL_0065358-65364)
17	Excerpts from Webster’s Third New International Dictionary of the English Language Unabridged, Merriam-Webster, Inc. (2002) (GT-WDTX-CL_0088611-88614)
18	<i>Intel Corp. v. Greenthread, LLC</i> , IPR2023-00548, Paper 1 (Intel 195 Petition) (Jan. 30, 2023) (GT-WDTX-CL_0042466-42570)
19	<i>Intel Corp. v. Greenthread, LLC</i> , IPR2023-00548, Ex. 1003 (Blalock Declaration) (Jan. 30, 2023) (GT-WDTX-CL_0043021-43137)
20	<i>Cirrus Logic, Inc. et al. v. Greenthread, LLC</i> , IPR2024-00017, Paper 1 (Cirrus 195 Petition) (Oct. 18, 2023) (GT-WDTX-CL_0088793-88907)
21	<i>Cirrus Logic, Inc. et al. v. Greenthread, LLC</i> , IPR2024-00017, Ex. 1003 (Banerjee Declaration) (Oct. 18, 2023) (GT-WDTX-CL_0088615-88760)
22	U.S. Patent Publication No. 2020/0006551 (“Warrick”) (GT-WDTX-CL_0088781-88792)
23	U.S. Patent Publication No. 2003/0042511 (“Rhodes”) (GT-WDTX-CL_0018646-18667)
24	U.S. Patent Publication No. 2002/0093281 (“Cathey”) (GT-WDTX-CL_0088774-88780)
25	U.S. Patent No. 6,831,292 (“Currie”) (GT-WDTX-CL_0088761-88773)
26	<i>Dell Techs. Inc., et al. v. Greenthread LLC</i> , IPR2023-00506, Paper 1 (Dell 842 Petition) (GT-WDTX-CL_0002147-2235)
27	<i>Dell Techs. Inc., et al. v. Greenthread LLC</i> , IPR2023-00506, Ex. 1003 (Blalock Declaration) (GT-WDTX-CL_0002497-2599)
28	<i>Sony Group Corp. v. Greenthread, LLC</i> , IPR2023-00376, Paper 1 (Sony 842 Petition) (GT-WDTX-CL_0063539-63619)
29	<i>Sony Group Corp. v. Greenthread, LLC</i> , IPR2023-00376, 1002 (Guidash Declaration) (GT-WDTX-CL_0063681-63796)

EXEMPLARY CLAIMS 195:1 & 5

Term	U.S. Patent No. 8,421,195, Claim 1 (195:1)
	A CMOS Semiconductor device comprising: a <u>surface layer</u> ;
	a <u>substrate</u> ;
	an <u>active region</u> including a source and a drain, disposed on one surface of said surface layer;
  	a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a <u>graded concentration of dopants</u> extending between said surface layer and said substrate, said drift layer further having a first static <u>unidirectional electric drift field</u> <u>to aid the movement of minority carriers from said surface layer to said substrate</u> ; and
	at least one <u>well region</u> disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Term	U.S. Patent No. 8,421,195, Claim 5 (195:5)
	The CMOS Semiconductor device of claim 1, wherein <u>said graded concentration</u> follows a quasi-linear gradient.

EXEMPLARY CLAIM 502:8

Term	U.S. Patent No. 9,190,502, Claim 8 (502:8)
9	7. A semiconductor device comprising: - a surface layer; - a substrate; - an active region including a source and a drain, disposed on one surface of said surface layer; - a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and - at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. 8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in <u>respective active regions</u>.

EXEMPLARY CLAIMS 842:1 & 9

Term	U.S. Patent No. 10,510,842, Claim 1 (842:1)
10	A semiconductor device, comprising: - a substrate of a first doping type at a first doping level having first and second surfaces; - a first <u>active region</u> disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and <u>within which transistors can be formed</u>; - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; - transistors formed in at least one of the first active region or second active region; and - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

Term	U.S. Patent No. 10,510,842, Claim 9 (842:9)
11 12	A semiconductor device, comprising: - a substrate of a first doping type at a first doping level having first and second surfaces; - a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in <u>the surface thereof</u>; - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; - transistors formed in at least one of the first active region or second active region; and - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to <u>aid carrier movement from the surface to the substrate</u>.

DISPUTED CLAIM CONSTRUCTIONS

#	Claim(s)	Terms ²	Previous Constructions ³	Greenthread	Cirrus
1	195:1 502:7 222:44	“surface layer”	Not indefinite. Plain and ordinary meaning.	Not indefinite. Plain and ordinary meaning, where the plain and ordinary meaning is “a layer at the surface”	Indefinite
2	195:1 502:7 842: 1-2, 4, 9-10, 12, 17 481: 1-3, 8, 15, 20, 22-23, 32 222:1-3, 8, 15, 21, 23-24, 33, 39-42, 44 014: 1-3, 8, 15, 21, 23-24	“substrate”	Plain and ordinary meaning	Not indefinite. Plain and ordinary meaning, where the plain and ordinary meaning is an “underlying layer”	Indefinite
3	195:1 502:7, 8 842: 1, 5-7, 9, 13-15, 17, 18 481: 1, 4-6, 8, 9, 13, 20, 24-27 222: 1, 4-6, 8, 9, 13, 20, 21, 25-28, 35, 39, 40, 41, 42, 44 014: 1, 4-6, 8, 9, 13, 20, 21, 25-28	“active region”	Plain and ordinary meaning	Plain and ordinary meaning	“region that forms current path of a device”
4	195:1, 5, 6 502:7 842:1, 6, 8-9, 14, 16 481:1, 5, 7, 9, 20, 25, 27, 31 222:1, 5, 7, 9, 21, 26, 28, 32, 39-42, 44	“graded concentration of dopants” and other “graded” terms	Related to #s 5 and 6	Not indefinite. Plain and ordinary meaning, where the plain and ordinary meaning is a graded (or varying) concentration of dopants.	Indefinite

² All 12 terms were identified by Defendant.

³ Ex. 7 (WDTX Preliminary Constructions); Ex. 8 (D. Or. Findings and Recommendation) (“[T]he WDTX’s preliminary constructions and summary judgment ruling should govern this case.”).

DISPUTED CLAIM CONSTRUCTIONS (continued)

#	Claim(s)	Terms	Previous Constructions	Greenthread	Cirrus
5	195:1 502:7 222:44	“said [drift layer further/well region...] having a [first/second] static unidirectional electric drift field”	Plain and ordinary meaning	Plain and ordinary meaning	“said [drift layer further/well region...] having a [first/second] static electric drift field that is unidirectional over the extent of the [drift layer/well region]”
		“said [drift layer further/well region] having a graded concentration of dopants generating a [first/second] static unidirectional electric drift field”			“said [drift layer/well region] having a graded concentration of dopants generating a [first/second] static electric drift field that is unidirectional over the extent of the [drift layer/well region]”
6	195:1 502:7 842:1, 9 481:1, 20 222:1, 21, 39, 41-42, 44 014:1, 21	“to aid the movement of minority carriers from...to...”	Not indefinite. Plain and ordinary meaning.	Plain and ordinary meaning	“to aid the movement of minority carriers starting from...and reaching...”
		“to aid the movement of carriers from...to...”			“to aid the movement of carriers starting from...and reaching...”
		“to aid carrier movement from...to ...”			“to aid carrier movement starting from...and reaching...”
		“to aid carrier movement from...towards...”			“to aid carrier movement starting from...towards...”
		“to aid carrier thereof movement from...to...”			“to aid carrier thereof movement starting from...and reaching...”
7	195:1 502:7 842:1, 9 481:1, 20 222:1, 21, 39, 41-42, 44 014:1, 21	“well region”	Plain and ordinary meaning. Note not for jury: portions of a well are not well regions	Plain and ordinary meaning. Note not for jury: portions of a well are not well regions	“A well, whether formed by single or multiple implants. Portions of a well are not well regions.”

DISPUTED CLAIM CONSTRUCTIONS (continued)

#	Claim(s)	Terms	Previous Constructions	Greenthread	Cirrus
8	195:5, 6 481: 7, 31 222: 7, 32 014: 7	“said graded concentration” “the graded dopant”	Related to #4	Not indefinite. Plain and ordinary meaning.	Indefinite
9	502:8	“respective active regions”	Related to #3	Not indefinite. Plain and ordinary meaning.	Indefinite
10	842:1, 9 481:1, 20 222:1, 21, 39, 41-42 014:1, 21	“active region... within which transistors can be formed”	Not indefinite. Plain and ordinary meaning.	Not indefinite. Plain and ordinary meaning.	Indefinite
11	842:9 481:20 222:21 014:21	“the surface thereof” “the surface”	Related to #10	Not indefinite. Plain and ordinary meaning.	Indefinite
12	842:9 481:20	“aid carrier movement from the surface to the substrate”	Related to #6	Not indefinite. Plain and ordinary meaning.	Indefinite

I. INTRODUCTION

Greenthread’s complaint asserts six patents that improve the performance of semiconductor devices. All six patents claim priority to an application filed by Dr. Mohan Rao on September 3, 2004. Dr. Rao is one of the pioneers in the semiconductor industry. He is an award-winning inventor, and his inventions are featured in the Smithsonian museum. When he filed his application in 2004, he used terms that those skilled in the art would readily understand. He did not coin any new terms, and he did not disclaim the full scope of the plain meaning. Therefore, it is not surprising that plain meaning is the proper construction for all twelve disputed claim terms.

Greenthread has briefed the twelve terms in accordance with Judge Counts’ Standing Order Governing Patent Proceedings in the order that the terms first appear in the asserted patents and claims. Cirrus Logic (“Cirrus”) used an order that does not follow Judge Counts’ rules.

Terms 1-3, 5-7, and 10 were previously at issue in *Greenthread v. Intel*. In that litigation, this Court issued preliminary constructions (Ex. 7), siding with Greenthread on all seven terms. After Intel was transferred to the District of Oregon, Magistrate Judge Russo reviewed the claim construction briefing and issued a recommendation that the WDTX constructions should govern (Ex. 8, 8). Now Cirrus wants to rehash arguments that have been rejected not once, but *twice*.

For term 4, Cirrus takes a “Hail Mary” approach that the “graded dopant” terms in *all* of the asserted claims are indefinite. It is telling that defendants in the *Intel* case (i.e., Intel, Dell, and Sony) never argued that these terms are indefinite. Instead each of them and their technical experts consistently took the position that these terms are readily understood. Even Cirrus filed IPRs demonstrating that Cirrus and its expert understood what these terms mean.

For the remaining terms 8-9 and 11-12, Cirrus makes hyper-technical arguments that these terms are also indefinite. In doing so, Cirrus misapplies the law. The test is not whether the term alone would have been confusing, or whether the antecedent basis for a dependent claim is *exactly*

the same. Rather, the test is whether one of ordinary skill in the art reading the specification, file history, and surrounding claim language would have understood with reasonable certainty what was meant. When the law is properly applied, there is no question these terms are not indefinite.

II. BACKGROUND

A. Dopants

Silicon is an example of a semiconductor. In its pure form it is typically an insulator but it can become an electrical conductor when impurities called “dopants” are added into the silicon crystal. These dopants are usually phosphorous or boron atoms that have one more or one less valence electron than a silicon atom. If the dopant has one less valence electron, then it creates what is called a “hole,” which is a positive unit of charge. The extra electrons or holes disturb the local charge equilibrium in the silicon and can become mobile in response to electric fields. Thus, the electrons and holes are called “charge carriers.” Ex. 1 (Glew declaration), ¶26; *id.*, ¶¶1-25.

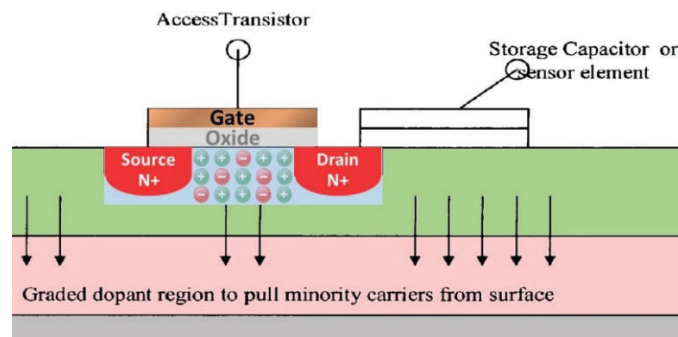
These dopants can also change the net electrical charge distribution in the surrounding silicon, which can influence the motion of other charge carriers passing by. When the dopant concentration is graded in a particular direction, other charge carriers will move in the gradient direction (or opposite direction) depending on the charge carrier’s polarity. This phenomenon is called “carrier drift.” *Id.*, ¶27.

B. Overview of Dr. Rao’s Invention

At the time of Dr. Rao’s invention, most semiconductor devices relied on uniform concentrations of dopants. Ex. 2 (195 patent), Abstract; 1:36-40, 50-51. Dr. Rao recognized, however, that graded concentrations of dopants can be used to improve the performance of transistors and other semiconductor devices. *Id.*, Abstract; 3:3-13, 33-35. His invention is clearly disclosed in Figs. 5B-C of his patents, and the corresponding parts of the specification. Ex. 1, ¶28.

A surface-channel MOSFET is a common type of transistor capable of controlling current

flow at or along the surface of the semiconductor substrate. Ex. 5 (Chen), 27 (“carriers propagate at the semiconductor surface”). Figure 5B shows an n-channel MOS (NMOS)⁴ transistor that is formed in a p-type surface layer. The transistor comprises (1) a gate; (2) a thin oxide separating the gate from the surface layer; and (3) two doped regions called the source and drain (shaded red). Ex. 2, 3:10-11 (“electrons can be swept from source to drain”); 3:42-43 (“accelerate majority carriers towards the drain”). In Fig. 5B, the N⁺ means these regions are heavily doped with an n-type dopant that creates a surplus of negative carriers (*i.e.*, electrons).⁵ The specification explains that the NMOS transistor in Fig. 5B can be a surface-channel MOSFET. Ex. 1, ¶¶29-32.



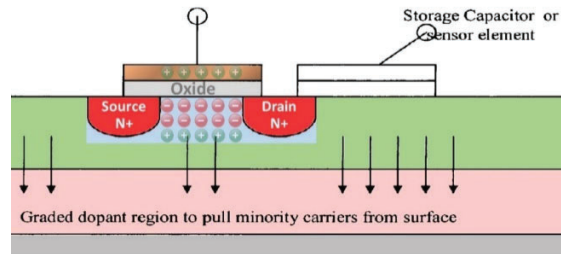
Ex. 1, ¶32 (explaining Fig. 5B above); Ex. 2, 3:41-43. Meanwhile, the p-type silicon between the source and drain (shaded blue) has an abundance of positively charged holes (green circles). When the holes separate the source’s electrons from the drain’s electrons, current cannot flow through the transistor, and the transistor is in an “off” state. Ex. 1, ¶¶32-33.

When a positive voltage is applied to the gate, an electric field forms in the oxide. *Id.* This electric field repels the holes downwards, while the electrons (red circles) are attracted to move into the blue surface layer. When enough electrons have accumulated in the surface layer below the oxide, they form a conductive channel between the source and the drain, and current can begin

⁴ MOS stands for “metal oxide semiconductor.” Ex. 1, ¶32 n.4.

⁵ An “N” region or layer has more electrons, and thus a “negative charge.” A “P” layer has more holes, and a “positive charge.” A “+” or “-” means heavily or lightly doped. Ex. 1, ¶32 n.5.

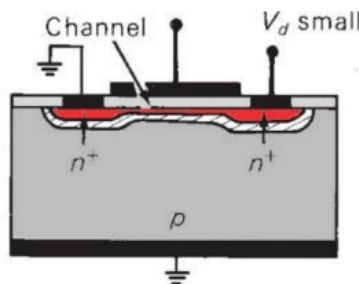
to flow through the transistor.



Ex. 1, ¶33.⁶ In order to turn the transistor “off,” the positive voltage is removed from the gate and the channel disappears as the holes return to the surface layer. *Id.*

POSITAs normally use the term “well region” to describe the doped silicon that surrounds the source and drain. *Id.*, ¶34. Dr. Rao recognized that by using graded concentrations of dopants in the well region and a drift layer (shaded pink), it is possible to “pull” carriers from the silicon’s surface. Ex. 2, Fig. 5B (annotated above). In this example, pulling the holes from the surface layer when a positive voltage is applied to the gate, allows the transistor to turn “on” more quickly. This improves the speed and performance of the transistor. Ex. 1, ¶35; Ex. 2, 3:8-13.

As its name suggests, the channel in a surface channel MOSFET forms along the surface. But it is slightly more complicated than that. The figure below shows that the n-channel starts at the source (left) and expands towards the drain (right) as the voltage applied to the gate increases. There is a thin layer below the surface (shaded red) where the channel actually forms. Ex. 1, ¶36.



Ex. 1, ¶36; Ex. 5, 19 (shaded). The cross-hatched region underneath is known as the depletion

⁶ Because the channel is formed by electrons with a negative charge, the MOSFET is referred to as an n-channel MOSFET, and the “minority carriers” are holes. Ex. 1, ¶33 n.6.

region. As shown above, the n-channel does not actually form on the surface but rather in the layer just below the surface (*i.e.*, the surface layer). Ex. 1, ¶36.

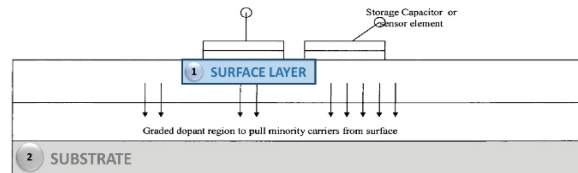
C. Exemplary Claims 195:1 & 5

Seven of the twelve disputed claim terms can be found in exemplary claim 195:1. These seven claim terms are numbered and color coded below.

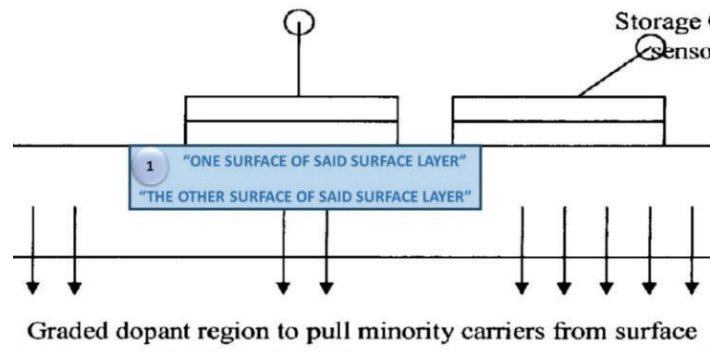
Term	U.S. Patent No. 8,421,195, Claim 1 (195:1)
1	A CMOS Semiconductor device comprising: a <u>surface layer</u> ;
2	a <u>substrate</u> ;
3	an <u>active region</u> including a source and a drain, disposed on one surface of said surface layer;
4	a single drift layer disposed between the other surface of said surface layer and said substrate,
5	said drift layer having a <u>graded concentration of dopants</u> extending between said surface
6	layer and said substrate, said drift layer further having a first static <u>unidirectional electric drift field</u> <u>to aid the movement of minority carriers from said surface layer to said substrate</u> ; and
7	at least one <u>well region</u> disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Far from being indefinite, claim 195:1 lines up exactly with Fig. 5B and the corresponding parts of the specification. Ex. 1, ¶¶37-38. Fig. 5B confirms exactly what is meant by each claim term. As the preamble states, Fig. 5B illustrates a CMOS device with metal and oxide layers on a silicon substrate. Ex. 2, 2:27-31; 3:41-43. The specification specifically mentions that the device may be a surface channel MOSFET. *Id.*, 3:41-43; *see also* 1:43-45.

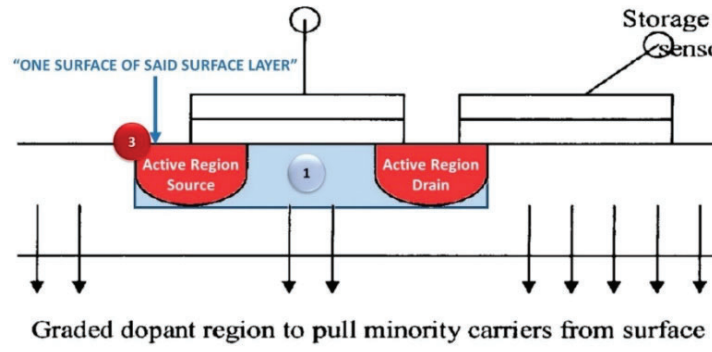
As seen below, the CMOS device comprises a surface layer (blue) and a substrate (gray). *Id.*, 3:30-45. The substrate is lightly doped with holes (P-), and the surface layer is a layer at the surface of the silicon. As explained below, the invention is concerned with moving minority carriers away from this surface layer. Ex. 1, ¶39.



Ex. 1, ¶39.⁷ The surface layer has at least two surfaces, which claim 195:1 refers to as the “one surface of said surface layer” and “the other surface of said surface layer.”

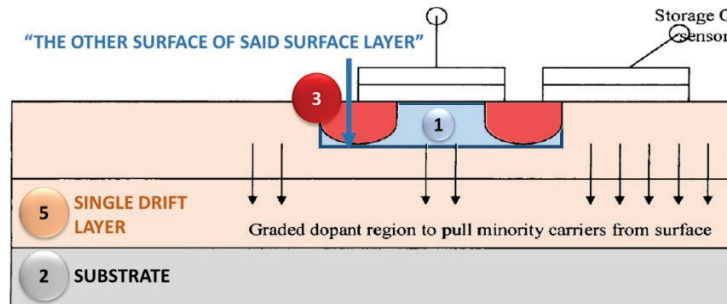


Ex. 1, ¶40; Ex. 2, 4:16-19. Next, the claim specifies an active region with a source and drain. Ex. 2, 4:16-17. Fig. 5B shows how the active region is “disposed on one surface of said surface layer.”

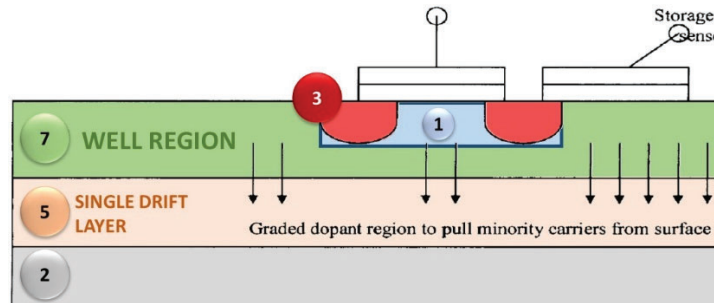


Ex. 1, ¶41. The “active region” is a doped region where a transistor can be formed. *Id.*, ¶42; Ex. 2, 1:61-63; 2:18-23; 3:1-3, 30-33. Next, the claim specifies there is a single drift layer disposed between “the other surface of said surface layer” and the substrate. The single drift layer has a graded concentration of dopants. Ex. 1, ¶43.

⁷ As explained below, “substrate” is a relative term, and Dr. Rao used it to refer to both the bottom layer, and the wells that are underneath the surface layer and active region. In each instance, Dr. Rao consistently used the term “substrate” to mean an “underlying layer.” Ex. 1, ¶39 n.7.



The graded dopants create an electric field that aids the movement of minority carriers (i.e., holes) from the surface layer to the substrate. Ex. 1, ¶44; Ex. 2, 3:17-20, 30-37. Finally, the claim specifies there is a well region disposed in the single drift layer, and this well region creates a second electric field that also aids the movement of minority carriers. Ex. 1, ¶45.



Ex. 1, ¶45; Ex. 2, 2:27-28; 3:37-40. Dependent claim 5 further specifies that “said graded concentration follow a quasi-linear gradient.” Ex. 2, 4:36-37.

D. Exemplary Claim 502:8

Like claim 195:1, base claim 502:7 is directed to a semiconductor device comprising a surface layer, substrate, an active region with a source and a drain, and a well region. Ex. 3, 4:53-67. Dependent claim 502:8 refers to an embodiment with multiple active regions, and specifies that electric fields are adapted to aid the movement of carriers in respective active regions. Thus, the grading of dopants can be different in different active regions. Ex. 3, 5:1-4; Ex. 1, ¶46.

E. Exemplary Claims 842:1 & 9

In claim 195:1, the “active region” includes the heavily doped regions called the “source” and the “drain.” Exemplary claim 842:1 sheds additional light on the “active region” when it

specifies the “active region” is a region “within which transistors can be formed.”

Term	U.S. Patent No. 10,510,842, Claim 1 (842:1)
10	A semiconductor device, comprising: a substrate of a first doping type at a first doping level having first and second surfaces; a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and <u>within which transistors can be formed;</u> a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; transistors formed in at least one of the first active region or second active region; and at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

In claim 842:1, there may be multiple active regions (*i.e.*, the first and second active regions), where a transistor is formed in at least one of them (*i.e.*, transistors formed in at least one of the active regions). Ex. 1, ¶¶47-48; Ex. 4, 4:48-56. Claim 842:9 is similar to claim 842:1 but specifies that within each of the active regions, transistors can be formed in the surface thereof, *i.e.*, in the surface of the first/second active regions. Ex. 4, 5:14-29. Claim 842:9 also specifies that at least one of the active regions has at least one graded dopant concentration to aid carrier movement from the surface (*i.e.*, of the active regions, because they have the graded dopant concentration) to the substrate. Ex. 4, 5:26-29; Ex. 1, ¶48.

III. DISPUTED CLAIM TERMS

For terms 1, 2, 4, and 8-12, Cirrus’ indefiniteness arguments ignore the specification and misapply the law. When the specification is properly read through the eyes of a POSITA⁸, Cirrus cannot meet its heavy burden of proving the terms are indefinite. In fact, Cirrus filed IPRs allegedly mapping these terms to the prior art, and Cirrus’ expert opined regarding the meaning of

⁸ Dr. Glew explains the qualifications for a POSITA. Ex. 1, ¶¶21-25. When Dr. Rao conceived his inventions, he had not one, but two Ph.D.s and had been working in the industry for more than forty years. Dkt. 1, ¶¶23-24.

some of the terms in a way that shows he understood them.

For terms 3 and 5-7, Cirrus ignores the well-accepted plain and ordinary meaning of the terms. The terms—active region, unidirectional, the preposition “to,” and well region—are simple terms that don’t need construction. Instead of giving them the full scope of their plain meaning, Cirrus seeks to add self-serving limitations that are inconsistent with the intrinsic record.

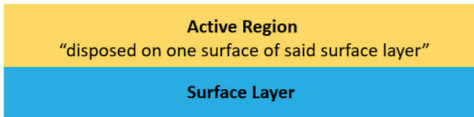
A. Claim Terms Found in Exemplary Claims 195:1 & 5

1. “surface layer” (195:1; 502:7; 222:44)

Previous Constructions	Greenthread	Cirrus
Not indefinite. Plain and ordinary meaning	Not indefinite. Plain and ordinary meaning, where the plain and ordinary meaning is “a layer at the surface”	Indefinite

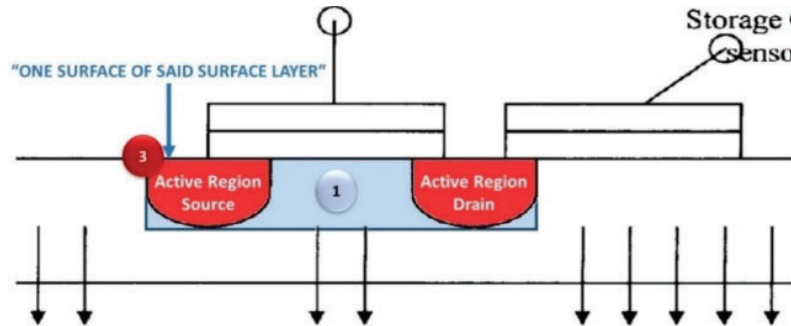
This Court and the District of Oregon already determined that “surface layer” is not indefinite, and it should be given its plain and ordinary meaning. Far from being indefinite, “surface layer” is a lay term that is understood by skilled artisans and lay people alike. Ex. 1, ¶¶58-65. Whether it is the surface layer of the ocean, skin, soil in a backyard garden, or a semiconductor device, it is referring to the same thing: a layer at the surface.

Nonetheless, Cirrus insists that the surface layer is *under* the active layer. That is, the surface layer is not at the surface. Not only would this contradict the plain meaning of surface layer, but it would exclude Dr. Rao’s invention and the preferred embodiment shown in Fig. 5. Like Intel did, Cirrus uses the following figure as the lynchpin for its argument. The only difference is that Cirrus changed the coloring from red-and-blue to yellow-and-blue.

Intel’s Argument (<i>Intel</i> Dkt. 82, 14)	Cirrus’ Argument (Dkt. 35, 18)
	

The Court already considered this argument and sided with Greenthread. Ex. 7, 2. As explained in the previous case, the claim specifies that the “surface layer” has two surfaces and the “active

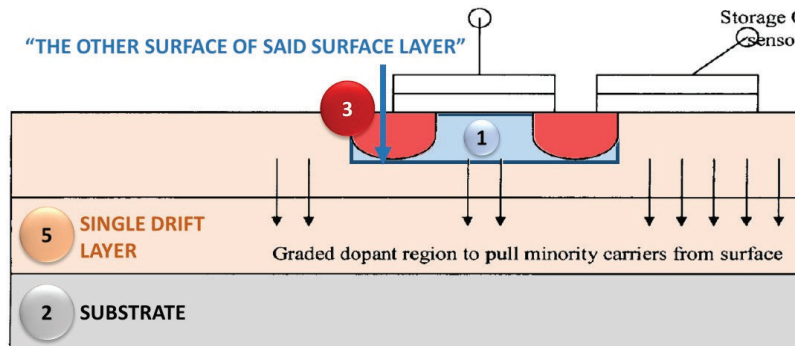
region” is disposed on one surface of the said surface layer.”



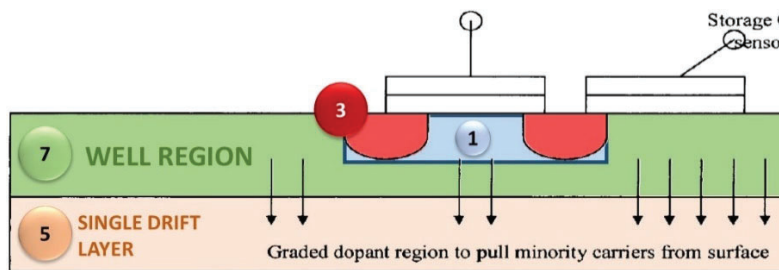
Ex. 2, Fig. 5B (annotated); Ex. 1, ¶59. When the claim says the “active region” is “disposed on one surface of said layer,” it is not saying it is a separate layer on top of the “surface layer.” Rather it is specifying where in the “surface layer” the “active region” is located. Instead of being anywhere in the surface layer, the “active region” is disposed on the top surface of the surface layer, as shown above. Ex. 1, ¶60. By analogy, if a room has two surfaces—a floor and a ceiling—and a ceiling fan is disposed on the ceiling of the room, it does not mean the ceiling fan is spinning around like a propeller on the roof of the house.⁹ Instead it means that the ceiling fan is hanging from the ceiling *inside* the room. The same is true about the active region and the surface layer. *Id.*, ¶60. When the claim says the active region is “disposed on one surface of the surface layer,” it means the active region is located on the “ceiling” of the silicon *inside* the silicon.

Cirrus arguments about “disposed on,” “disposed between” and “disposed in” support Greenthread, *not* Cirrus. When the claim language is read correctly, it lines up exactly with the preferred embodiment in Fig. 5B. As shown above, the active region is “disposed on” *one* surface of the surface layer. As shown below, the single drift layer is “disposed between” the *other* surface of the surface layer and the substrate. Ex. 1, ¶61.

⁹ Cirrus refers to this analogy as “absurd” because semiconductor devices don’t have “ceilings.” Dkt. 35, 13. Cirrus misses the point of an analogy. Cirrus does not dispute that a semiconductor has a top surface (*i.e.* the “ceiling of the room”) and that dopants penetrate this top surface to create the active region within the silicon (*i.e.*, the dopants are “inside” the room).



Ex. 2, Fig. 5B (annotated); Ex. 1, ¶61. And the well region is “disposed in” the single drift layer.



Ex. 2, Fig. 5B (annotated); Ex. 1, ¶62. The Federal Circuit has made it clear that the claims should be read to include the preferred embodiment, and that “[a] claim construction that ‘excludes the preferred embodiment is rarely, if ever, correct and would require highly persuasive evidentiary support.’” *SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1378-79 (Fed. Cir. 2013) (quoting *Adams Respiratory Therapeutics, Inc. v. Perrigo Co.*, 616 F.3d 1283, 1290 (Fed. Cir. 2010)).

The remainder of Cirrus’ brief regurgitates arguments that Intel already made and lost. ***First, the specification confirms that the “surface layer” is a layer at the surface.*** The test is not whether the words “surface layer” literally appear in the specification, but whether a POSITA would have known what was meant by the term after reading the intrinsic record. “Surface layer” is readily understood by POSITAs to mean the surface of the silicon where the source and drain are located. Ex. 1, ¶63. This is how the term “surface” is consistently used throughout the specification and figures. See Ex. 2, 1:43-45 (explaining MOS devices are majority carrier devices and “the channel can be a surface in one plane in planar devices”); 3:30-33 (explaining how Dr.

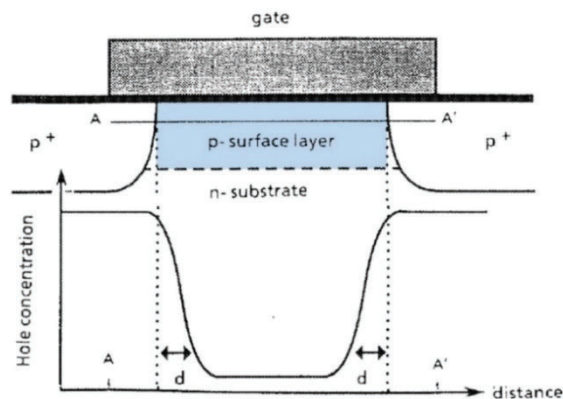
Rao's invention sweeps unwanted minority carriers "from the active circuitry at the surface"); 3:38-43 (explaining how graded dopants "sweep those carriers away from the surface" and may be used "in surface channel MOS devices to accelerate majority carriers towards the drain"); 3:43-45 (when programming devices, "carriers should be accelerated towards the surface"); 3:53-55 ("minority carriers can be channeled to the surface"); Fig. 5A ("Graded dopant region to pull minority carriers from surface"); and Fig. 5B ("Graded dopant region [a]ccelerates carriers towards surface during programming"). In each instance, the specification is referring to the surface layer at the surface of the semiconductor device where the active region is located. Ex. 1, ¶63.

A POSITA would have known that the carriers-of-interest are actually in the thin layer of silicon just below the silicon's surface (*i.e.*, the "surface layer"). *Id.*, ¶64. Armed with this knowledge, "surface" is frequently used as a shorthand for "surface layer." *Id.* While POSITAs know what is meant by carriers "at the surface," it is actually more precise to refer to them as carriers "in the surface layer." *Id.*; Dkt. 35-15, 109; Dkt. 35-16, 30, 33. Turning back to Fig. 5B, we know from the surrounding claim language that the source and drain are disposed on "one surface of the surface layer." When the specification refers to a surface channel MOSFET, the channel forms along the upper surface of this blue region. Furthermore, when the specification refers to "pull[ing] minority carriers from surface" or "accelerat[ing] minority carriers towards the surface," it refers to this same blue area. Thus, the specification consistently confirms that the "surface layer" is a layer at the surface of the semiconductor device. Ex. 1, ¶64.

Second, the prosecution history further confirms that the surface layer is the top layer of the silicon. During 195 prosecution, Applicant elected claims directed to the embodiment shown in Figs. 5B-C. Dkt. 35-7 (195 file history), 49. These claims, which were part of the original priority application, referred to the "active surface regions." *Id.*, 9. Applicant

subsequently amended the claims to change “surface region” to “surface layer,” and specified that the “active region” is “disposed on one surface of said surface layer.” *Id.*, 165. In the next Office action, the Examiner asserted that reference 23 in Fig. 2 of Kamins is a “surface layer.” *Id.*, 183; Dkt. 35-9 (Kamins), 3. Notably, the Examiner identified the layer at the surface of the silicon as the “surface layer,” and not the oxide layer on top of the silicon. This confirms that the Examiner understood the “surface layer” to be a layer at the surface of the silicon.

Third, “surface layer” has a plain meaning as used in the claims. A POSITA would readily understand that a “surface layer” is a layer at the surface of the semiconductor device. *Id.*, ¶65. This is because it is customary to refer to layers by their relative position. For example, a “bottom layer” is at the bottom; “middle layer” at the middle; and “surface layer” at the surface. Cirrus does not contend that it is unclear what is meant by the “surface” of a CMOS device. It is the doped silicon where the active region is located, and where the channel forms in a surface-channel MOSFET. Therefore, it should go without saying that a “surface layer” is a layer at the surface of the semiconductor device. The Wolf textbooks cited by Cirrus also confirm that a “surface layer” is a layer at the surface where the active region is located. *Id.*, ¶65.



Ex. 1, ¶65; Dkt. 35-15 (Wolf Vol. 3), 109 (describing MOSFET with source and drain); Dkt. 35-16 (Wolf Vol. 4), 30, 33 (describing “surface layer” of MOSFET as doped silicon near surface). The fact that the textbooks may use the term differently in other contexts does not alter the fact

that in the context of MOSFETs, “surface layer” means a “layer at the surface.” When, as here, a term may have multiple plain meanings, the one that is most consistent with the asserted patent’s context should be used. *Renishaw PLC v. Marposs S.p.A.*, 158 F.3d 1243, 1250 (Fed. Cir. 1998) (“Thus, where there are several common meanings for a claim term, the patent disclosure serves to point away from the improper meanings and toward the proper meaning.”).

2. “substrate” (195:1; 502:7; 842:1-2, 4, 9-10, 12, 17; 481:1-3, 8, 15, 20, 22-23, 32; 222:1-3, 8, 15, 21, 23-24, 33, 39-42, 44; 014:1-3, 8, 15, 21, 23-24)

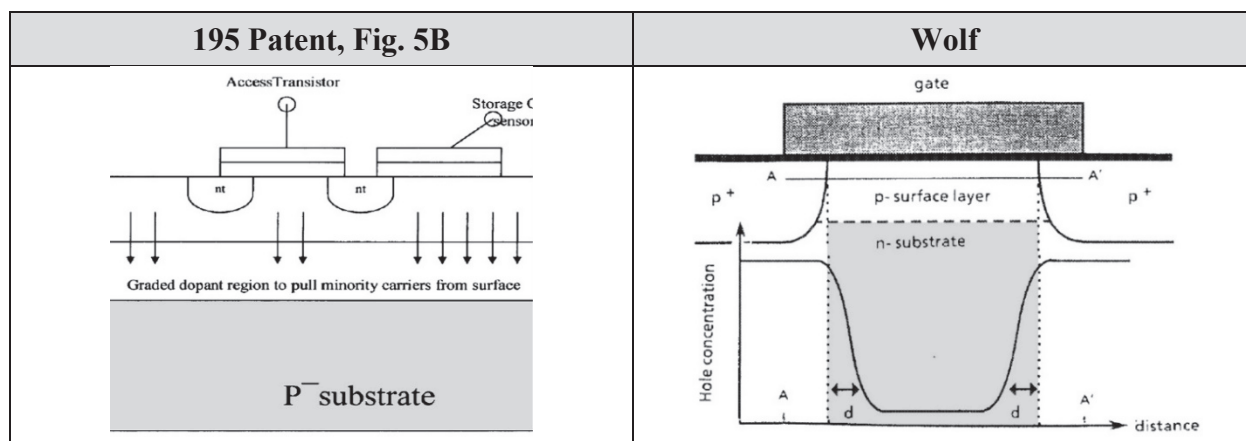
Previous Constructions	Greenthread	Cirrus
Plain and ordinary meaning	Not indefinite. Plain and ordinary meaning, where the plain and ordinary meaning is “a layer at the surface”	Indefinite

Intel previously argued “substrate” means “the intial material within which or on which the semiconductor device is fabriacted.” Instead this Court and the District of Orgeon determined that it should be given its plain and ordinary meaning. In the previous litigations, not one defendant has ever argued that the term “substrate” is indefinite. Nonetheless Cirrus now argues that because the exact physical location of the “substrate” might change, the term is indefinite. The mere fact that a “substrate” might be in one location in one claim, and in another location in another claim, does not make it indefinite. Cirrus’ indefiniteness arguments misapply the law, and would invalidate tens of thousands patent claims, including Cirrus’ own.

“Substrate” is a term that is readily understood by POSITAs. Ex. 1, ¶¶66-68. A substrate is an “underlying layer.” *See* Ex. 10 (American Heritage Dict.) (defining “substrate” as “an underlying layer”); Ex. 11 (Webster’s Dict.) (explaining “substrate” is synomous with its latin origin “substratum,” which means “underlying structure, layer, or part”). This is how the term is consistently used in the claims, specification, and prosecution history. Ex. 1, ¶66. The term is not indefinite, and it should be given the full scope of its plain meaning. *Id.*

In Fig. 5B, the “P- substrate” (shaded gray) is an “underlying layer.” In the Wolf textbook,

the “n- substrate” (shaded gray) is also an “underlying layer.” Dkt. 35-15, 109 (p.295). This is how the term “substrate” is ordinarily used in the art. Ex. 1, ¶67.



Id. There is nothing in the intrinsic record that departs from the term’s plain meaning. Every time “substrate” is used, it refers to an “underlying layer.” *Id.*; Ex. 2, 1:50, 62 (“twin well substrate”); 2:18-23, 27-28 (“a MOS silicon substrate with two wells, and, an underlying layer”); 3:31-32 (“sweep these unwanted minority carriers into the substrate”); 3:35 (“deep into the substrate”); Figs. 2, 3A-D, 4, 5A-C (all showing substrate as an underlying layer).

Cirrus makes a mockery of indefiniteness law, when it argues that the precise meaning of “substrate” may be context specific, and “substrate” may mean different regions of a semiconductor in different claims. Dkt. 35, 26. To suggest this makes “substrate” indefinite is illogical. In semiconductor patents, it is common to refer to layers by their relative location to other layers. The fact that the exact physical location of the “substrate” may change does *not* make it indefinite. In each instance, the “substrate” is still an “underlying layer.” This is how the term is ordinarily used in the art, and how it is consistently used in *all* of the asserted claims.

Greenthread never said the asserted claims use the term “substrate” inconsistently, as Cirrus falsely alleges in its brief. Rather Greenthread explained “substrate” is a relative term, and Dr. Rao correctly used it to refer to both the bottom layer, and the wells that are underneath the

surface layer and active region. Both the bottom layer and the wells are “underlying layers.” Furthermore, Dr. Rao consistently used the term “substrate” in all of the asserted claims to mean the same thing—an underlying layer. The mere fact that the same term can be used to refer to different physical locations does not make it indefinite. “[B]readth is not indefiniteness.” *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1367 (Fed. Cir. 2017) (citation omitted). That the term “substrate” can encompass both (or either) a bottom layer and wells does not make it indefinite. In *BASF*, the Federal Circuit criticized and reversed a district court that held a term indefinite because “a practically limitless number of materials” could meet the limitation. *Id.*

3. “active region” (195:1; 502:7-8; 842:1, 5-7, 9, 13-15, 17-18; 481:1, 4-6, 8-9, 13, 20, 24-27; 222:1, 4-6, 8-9, 13, 20-21, 25-28, 35, 39-42, 44; 014:1, 4-6, 8-9, 13, 20-21, 25-28)

Previous Constructions/Greenthread	Cirrus
Plain and ordinary meaning	“region that forms current path of a device”

Intel argued “active region” means “region that forms the current path of a device.” *Intel* Dkt. 82, 18. Instead this Court and the District of Oregon determined that it should be given its plain and ordinary meaning.” Cirrus is remaking the same argument that has already been rejected.

“Active region” is a term that POSITAs readily understand and can easily explain to jurors. A POSITA reading the claims and intrinsic record would understand that an active region is a doped silicon region at the surface of a semiconductor device where a transistor can be formed. Ex. 1, ¶¶69-73. This is how the term is used in the relevant claims and throughout the intrinsic record. *Id.*, ¶69. There is no need to construe the term, and to do so would only introduce ambiguity where there is none. *Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 805 (Fed. Cir. 2007).

As explained in the previous case, the term “active region” appears in both claims 195:1 and 842:1, and the term *must* be given the same meaning in both claims. *See NTP, Inc. v. Research in Motion, Ltd.*, 418 F.3d 1282, 1293 (Fed. Cir. 2005) (“Because [plaintiff’s] patents all derive

from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents.”).

Claim 842:1 requires two active regions and that transistors are formed in at least one of them. Ex. 3, 4:48-56. This means some, but not necessarily all, of the active regions will form a transistor. If the active region does not form a transistor, then the active region will not necessarily form the current path of a device. Ex. 1, ¶70. This means Cirrus’ construction cannot be correct.

To form, for example, a CMOS transistor in an active region, terminals must be connected to the source, drain, and gate, and a sufficient voltage must be applied to the gate to turn the transistor “on.” Ex. 1, ¶71. Dr. Rao contemplated that the transistors may be formed later. Ex. 2, 1:61-63; 2:18-23 (“subsequently fabricated”); 3:1-3 (“for eventual device fabrication”). Therefore, Cirrus’ construction would exclude a preferred embodiment. Ex. 1, ¶71.

Cirrus cites to extrinsic evidence where “active region” is used to refer to a region that forms the current path of a device. Dkt. 35, 18-20. In some contexts, this may be true. But there are plenty of other references where “active region” is used to refer to the source and drain of a MOSFET, and the silicon between the source and drain, regardless of whether current flows between them. In fact, Baker explains how a MOSFET transistor is built in the active region. Ex. 12, 65 (“The active layers are used to make the source and drain regions.”). Similarly, Chen describes forming the source and drain as forming the “active region.” Ex. 5, 239 (“Active channel regions are first defined by etching windows in a thick field oxide...The boron impurities in the active regions are counter doped...”). This is how active region is used in the claims-at-issue and the intrinsic record. Therefore, in the context of Dr. Rao’s inventions, it is more accurate to refer to an active region as a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed. Ex. 1, ¶72. When,

as here, a term may have multiple plain meanings, the one that is most consistent with the asserted patent's context should be used. *Renishaw*, 158 F.3d at 1250.

Cirrus' argues Greenthread's plain meaning construction conflates "active region" with "well region." Dkt. 35, 17. This is not true. In all of the claims where "active region" appears, the claim specifies additional limitations. These additional limitations differentiate the "active region" from the "well region" or other regions of the semiconductor device. Ex. 1, ¶73.

4. "graded concentration of dopants" and "graded" terms(195:1, 5, 6; 502:7; 842:1, 6, 8, 9, 14, 16; 481:1, 5, 7, 9, 20, 25, 27, 31; 222:1, 5, 7, 9, 21, 26, 28, 32, 39–42, 44)

Greenthread	Cirrus
Not indefinite. Plain and ordinary meaning, where the plain and ordinary meaning is a graded (or varying) concentration of dopants.	Indefinite

In the *Intel* litigation, "graded dopant concentration" was part of the "unidirectional" term that is addressed in the next section. As seen in claim 195:1, the well region has "a *graded concentration of dopants* and a second static unidirectional electric drift field. Ex. 2, 4:26-28. The *Intel* defendants did not dispute the meaning of "graded concentration of dopants," and this Court and the District of Oregon determined that the entire term (including the graded portion) should be given its plain and ordinary meaning. Exs. 7-8.

Not one of the *Intel* defendants argued that any of the "graded" terms are indefinite. In fact, they consistently took the position that these terms are readily understood and should be given their plain meaning. *See, e.g.*, Ex. 18, 6, 17, 19, 53-57; Ex. 19, ¶¶61-62, 89, 156-163; Ex. 26, 9, 26-32, 52-56; Ex. 27, ¶¶54, 89-94, 141-145; Ex. 28, 9, 25-30, 51-56, 75; Ex. 29, ¶¶100-103, 150-154, 192. Even Cirrus' own IPRs demonstrate that Cirrus and its experts understood what these terms mean. *See, e.g.*, Ex. 20, 8; Ex. 21, ¶¶58, 61. When applying prior art in its IPR petition, Cirrus had no issues determining what it believed to constitute graded dopants. Ex. 20, 19-21, 59-

66; Ex. 21, ¶¶88-93, 156-167. To now argue the term is indefinite is rather hypocritical.

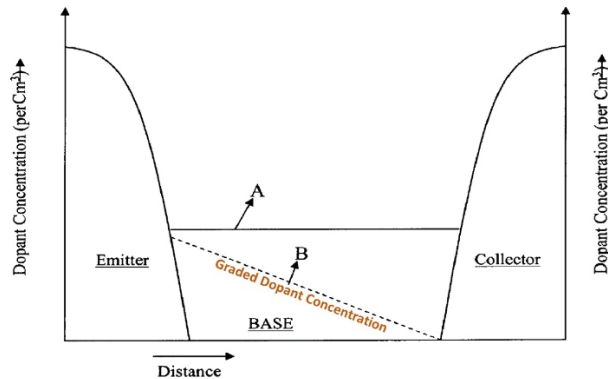
Far from being indefinite, “graded dopant concentration” is a term POSITAs readily understand and can easily explain to jurors. Ex. 1, ¶¶74-80. A POSITA reading the claims and intrinsic record would understand a “graded dopant concentration” is a graded (or varying) concentration of dopants. This is how “graded” is used in the relevant claims and throughout the intrinsic record. *Id.*, ¶75. It is also how it is used in Wolf, Dkt. 35-13, 64, p. 373 (“graded junctions”), and even in Cirrus’ own patent filings, Ex. 22, [0004] (“The dopant distribution...may be formed by lateral diffusion of dopants...which forms a laterally graded channel region 104.”).

The test for indefiniteness is whether the claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty. *Nautilus, Inc. v. Biosig Instruments*, 572 U.S. 898, 910 (2014). A POSITA reading the claims in light of the specification and prosecution history would have readily understood that a “graded dopant concentration” is a graded (or varying) concentration of dopants. Ex. 1, ¶76.

The claim language confirms that a “graded concentration of dopants” is a graded (or varying) concentration of dopants. The asserted claims specify that the graded dopants generate a “first static unidirectional electric field” that “aids the movement of minority carriers.” When the dopants are graded (or varied) in a particular direction, other charge carriers will move in the gradient direction (or opposite direction) depending on the charge carrier’s polarity. Therefore, the surrounding claim language would have informed a POSITA that a “graded dopant concentration” is a graded (or varying) concentration of dopants. *Id.*

The specification further confirms that a “graded dopant concentration” is a graded (or varying) concentration of dopants. To the extent there is any doubt from the face of the claims what is meant by “graded dopant concentration,” Fig. 1 and the corresponding portions of the

written description disclose a specific example of a graded dopant concentration. Ex. 1, ¶77.



Ex. 2, Fig. 1. The X axis measures “Distance” and the Y axis measures “Dopant Concentration (per Cm³)”. *Id.*; Ex. 1, ¶77. The solid line labelled “A” shows a uniform dopant concentration in the base region of a bipolar junction transistor (BJT). *Id.*; Ex. 2, 2:35-38. In contrast, the dashed line labelled “B” shows a graded dopant concentration. Ex. 1, ¶77. As seen above, there is a graded (or varying) concentration of dopants in the relevant portion of the BJT. *Id.*

In the specification, Dr. Rao explained that “[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier’s speed from emitter to collector.” Ex. 2, 1:55-57. Therefore, a POSITA would have readily understood that the graded dopants generate the electric field that aids movement of the carriers. Ex. 1, ¶78.

When describing the prior art in Figure 2, Dr. Rao made it clear that the “n-dopant concentration is uniform.” Ex. 2, Fig. 2, 2:39-40. In contrast, Fig. 4 shows an embodiment of Dr. Rao’s invention where the “n-dopant concentration is graded.” Ex. 2, Fig. 4, 2:51-53. The specification explains in more detail that the graded dopant concentration can be used to significantly decrease the amount of time it takes to turn the transistor “on” and “off.” Ex. 1, ¶79. Similarly, Fig. 5A shows a “graded dopant n-layer”; Fig. 5B shows a “graded dopant region to pull minority carriers from surface”; and Fig. 5C shows a “graded dopant region” that “accelerates carriers towards surface during programming.” Ex. 2, Figs. 5A-C. Dr. Rao explained in more

detail that n and p wells can “be graded or retrograded in dopants to sweep those carriers away from the surface,” and graded dopants can be used “in surface channel MOS devices to accelerate majority carrier towards the drain.” *Id.*, 4:3-7. Dr. Rao also explained that graded dopants can be used to accelerate carriers towards the surface when programming memory cells. *Id.*, 4:7-10. Additionally, Dr. Rao disclosed that graded dopants can be used to improve Junction Field-Effect transistors by using “a graded channel instead of a uniformly doped channel.” *Id.*, 4:10-13.

The prosecution history further confirms a “graded dopant concentration” is a graded (or varying) concentration of dopants. During prosecution, the Examiner pointed to regions 160, 170, and 180 of Rhodes (Ex. 23) as disclosing “graded doped regions.” Dkt. 35-7, 56. The office action demonstrates that he understood what the term “graded dopant concentration” meant. Ex. 1, ¶80. Similarly, the Examiner pointed to Fig. 2 of Cathey (Ex. 24) as showing a graded dopant concentration. Dkt. 35-7, 57. Again, this demonstrates he understood the term. Later, the Examiner pointed to cols. 5-6 of Currie (Ex. 25) as disclosing a graded dopant concentration. Dkt. 35-7, 113. This further demonstrates he understood the term.

In its Opening Brief, Cirrus makes much ado about certain statements during the Intel litigation regarding Kamins. Dkt. 35, 14-15. Fig. 3 of Kamins (which is replicated on page 14 of Cirrus’ opening brief) shows that layers 23 and 19 of Fig. 2 (also replicated on page 14) contain a uniform dopant concentration. Dkt. 35-9, Figs. 2-3. Any implication by Greenthread that all three layers (i.e., layers 19, 21, and 23) contain uniform dopants was based on an inadvertent error, and Greenthread does not contend here or anywhere else in the present litigation that layer 21 contains a uniform concentration of dopants. Rather than focus on the merits, Cirrus would rather focus on a misstatement in the previous *Intel* litigation.

When, as here, it is clear from the face of the claims what was meant by “graded dopant

concentration”; Dr. Rao provided specific examples in his specification, and even illustrated a graded dopant concentration in Figure 2; and the file history provides additional examples of what was meant by “graded dopant concentration”; Cirrus cannot possibly meet its burden of proving by clear and convincing evidence that any of the “graded” terms are indefinite. *Enzo Biochem, Inc. v. Applera Corp.*, 599 F.3d 1325, 1336 (Fed. Cir. 2010) (holding not indefinite because POSITA could use “the examples in the specification”).

5. “unidirectional electric drift field” terms (195:1; 502:7; 222:44)

Previous Constructions/ Greenthread	Cirrus
Plain and ordinary meaning	“said [drift layer further/well region...] having a [first/second] static electric drift field that is unidirectional over the extent of the [drift layer/well region]” “said [drift layer/well region] having a graded concentration of dopants generating a [first/second] static electric drift field that is unidirectional over the extent of the [drift layer/well region]”

Intel previously argued that “said drift layer further having a first static unidirectional electric drift field” means “said drift layer further having a first static electric drift field that is unidirectional *over the drift layer.*” Instead this Court and the District of Oregon determined that it should be given its plain and ordinary meaning. Cirrus is remaking the same claim construction argument that has already been rejected.

For this term, Cirrus contends there was prosecution disclaimer where there was none. Cirrus does not contend that “electric drift field” or “unidirectional” need to be construed. Instead, Cirrus contends the straight-forward language should be rewritten to add the extraneous limitation “over the extent of the drift layer.” Dkt. 35, 20. Cirrus makes a similar argument for the “well region.” *Id.* There is no justification for rewriting the claim to say the electric field is “unidirectional *over the extent of the drift layer.*”

There was no clear disavowal, and Cirrus cannot possibly meet the high bar for prosecution disclaimer. *Cordis Corp. v. Boston Sci. Corp.*, 561 F. 3d 1319, 1329 (Fed. Cir. 2009) (“A

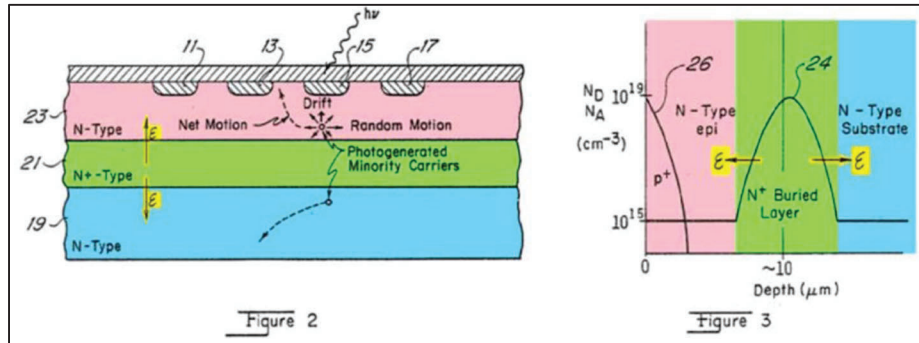
disclaimer must be ‘clear and unmistakable,’ and unclear prosecution history cannot be used to limit claims”). There is no justification to limit the terms like Cirrus suggests. Ex. 1, ¶¶81-86.

To begin, Cirrus argues the “claim language itself *implies* a single unidirectional field over the *extent* of the layer or region.” Dkt. 35, 32 (emphasis added). First, the claim says “single drift layer,” not “single unidirectional field.” There is nothing in the claim preventing additional electric fields. Ex. 1, ¶82. Second, Cirrus admits with the word “implies” that the claim does not expressly require the field to be unidirectional over the entire drift layer. Dr. Rao could have certainly added this language. The fact that he did not is compelling evidence he did not intend it to be a limitation. Instead he merely said the drift layer has a unidirectional field. The fact that the field may stop before the end of the layer does not mean that the drift layer does not have a unidirectional field.

Next, Cirrus grossly misrepresents the specification and figures. Cirrus cites to several instances where the specification mentions that a graded concentration of dopants creates an electric field. But nothing in the specification says there is only one field per layer, much less that the field must continue across the entire layer or region. Ex. 1, ¶83. These are fictions that Intel created, and the Court has already considered. *Compare Intel* Dkt. 82, 22 *with* Dkt. 35, 32 (both citing to the following); Ex. 2, 1:34-36 (merely says “aiding drift field” without any mention of a layer, direction of the field, or the total number of fields); 2:13-15 (merely says “doping profiles” without *any* mention of a field); 2:35-47 (discussing how a graded dopant concentration “creates a suitable aiding drift electric field” without any mention of a layer, direction of field, or the total number of fields); 3:30-35 (discussing how the graded dopants create a drift field to sweep the minority carriers into the substrate without any mention of the location or duration of the drift field or the total number of fields); Fig. 1 and 5A (no field at all). Cirrus also cites Figs. 5B-C, which support Greenthread, not Cirrus. These figures show multiple fields that traverse only part of the

well region and drift layer. Cirrus' construction would exclude both preferred embodiments.

Finally, Cirrus argues prosecution disclaimer where there was none. All of Cirrus' arguments turn entirely on Kamins' layer 21 in the annotated figures below.



Dkt. 35, 33; Ex. 1, ¶84. As explained by Greenthread in its surreply in the *Intel* case, the fact that Kamins' layer 21 may contain graded dopants that create two fields, does **not** change the end result that there was **no** prosecution disclaimer. *Intel* Dkt. 102, 10-11. This is because Dr. Rao distinguished Kamins on the basis there was no “single drift layer” that aids movement of “minority carriers **from** said surface layer to the substrate.” During prosecution, the Examiner identified the “surface layer” as the top pink layer 23 and the “drift layer” as the middle green layer 21. Dkt. 35-7, 223 (“a surface layer (23)” and “a drift layer (21)”). As Dr. Rao pointed out, the middle green layer cannot be the claimed “single drift layer” because it does not move minority carriers **from** the surface layer to the substrate. *Id.*, 238. Instead, the middle green layer either accelerates minority carriers to the surface, or merely moves them deeper into the substrate. *Id.* Thus, no layer moves minority carriers from the surface layer to the substrate. Ex. 1, ¶85.

Fig. 2 above refers to “photogenerated” carriers in the green layer 21. Dkt. 35-9, 2:11-20. These carriers include electrons and holes with the latter being the minority carriers in the Kamins device. *Id.* There are only two possible scenarios for “aid[ing] the movement” of the minority carriers. In the first scenario, the minority carrier will move from the green buried layer to the cross hatched surface of the pink layer (see dashed line labeled “Net Motion”). This is certainly

not movement from the surface layer to the substrate. In the second scenario, the minority carriers will move from the green buried layer to the blue underlying layer. Again this is not movement from the pink surface layer to the substrate. Ex. 1, ¶86. Thus, Dr. Rao’s claims were clearly patentable over Kamins for these reasons alone. There is no logical reason that Dr. Rao would have limited his claims to require the electric field to be unidirectional over the entire drift layer, or disclaimed multiple electric fields in any of the layers. It was not necessary to overcome the prior art. When, as here, there is another explanation for the amendment (*e.g.*, to clarify that the movement is from the surface layer to the substrate), Cirrus cannot meet the high bar for prosecution disclaimer. *Baxalta Inc. v. Genentech, Inc.*, 972 F.3d 1341, 1348-49 (Fed. Cir. 2020) (finding the patentee’s claim amendment did “not clearly establish disclaimer” where another “plausible” explanation for the introduction of the amendment was presented).

Finally, Cirrus strangely points to Greenthread’s preliminary infringement contentions as an alleged basis for narrowing the claim scope. Cirrus alleges that because Greenthread’s infringement against previous defendants Micron and Western Digital happened to identify electric drift fields pointing multiple directions, and Greenthread’s preliminary infringement contentions against Cirrus happened to identify an electric drift field pointing in a single direction, that this means the Court should limit the scope of Dr. Rao’s claims. Obviously this is not a legitimate reason for reading limitation into the claims.

6. “to aid the movement” terms (195:1; 502:7; 842:1, 9; 481:1, 20; 222:1, 21, 39, 41-42, 44; 014:1, 21)

Previous Constructions	Greenthread	Cirrus
Not indefinite. Plain and ordinary meaning	Plain and ordinary meaning	“to aid the movement of minority carriers starting from...and reaching...” and variations thereof

Intel previously argued these terms are indefinite. This Court and the District of Oregon disagreed and determined these terms should be given their plain meaning. Now Cirrus goes a

different route and attempts to read new limitations into the claims terms.

Exemplary Claim 195:1	Cirrus' Proposed Construction
"to aid the movement of minority carriers from said surface layer to said substrate"	"to aid the movement of minority carriers <u>starting</u> from said surface layer ~~to~~ <u>and reaching</u> said substrate"

Cirrus' proposed construction contains *three* egregious re-writes. Cirrus has not identified any prosecution disclaimer, specification disclaimer, or any other form of disclaimer that would justify such a dramatic change to the claim language. The preposition "to" does not need construction, and the jury can determine for itself what Dr. Rao meant by the word "to." Ex. 1, ¶¶87-89. The fact that some claims may use the preposition "to" and some claims may use the word "towards" is not a legitimate basis for replacing the word "to" with "and reaching." To do so, would insert extraneous limitations that limit the scope of Dr. Rao's invention. To make matters worse, Cirrus provides *no* justification for the insertion of the additional limitation "starting."

When citing to the specification, Cirrus erroneously cites to statements about accelerating electrons from an emitter to a collector, or from a source to drain. These statements have little, if any, relevance to the claim language above about aiding the movement of minority carriers from the surface layer. Ex. 1, ¶89. When citing to the prosecution history, Cirrus admits, as it must, that the pending claims did not even include the claim language above. Without something more, there is no justification for Cirrus' proposed construction.

7. "well region" (195:1; 502:7; 842:1, 9; 481:1, 20; 222:1, 21, 39, 41, 42, 44; 014:1, 21)

Previous Constructions/Greenthread	Cirrus
Plain and ordinary meaning. Note not for jury: portions of a well are not well regions	"A well, whether formed by single or multiple implants. Portions of a well are not well regions."

Intel proposed the same "single or multiple implant" language. Instead this Court and the District of Oregon determined that it should be given its plain meaning." Greenthread agrees with this Court's determination that the "well region" portion is best handled as a "note not for jury."

As explained in the *Intel* litigation, “well region” is a term that is readily understood by POSITAs and easy to explain to jurors. The term is commonly used to refer to a doped region that surrounds the active region of a semiconductor device. Ex. 1, ¶90 (citing Dkt. 35-14, 106-108). This is how the term is consistently used in the claims, specification, and prosecution history. This term does not require construction, and it should be given the full scope of its plain meaning.

There are two parts to Cirrus’ proposed construction. The first part is unnecessary and introduces ambiguity where there is none. The parties appear to agree that the “well region” is a doped region. But to construe the term to mean the well is “formed by single or multiple implants” is unnecessary and just begs the question what is meant by “single or multiple implants.” In cases, like this one, it is better to leave the claim untouched. *See W. Union Co. v. MoneyGram Int’l, Inc.*, 2008 U.S. Dist. LEXIS 108129, at *15-16 (W.D. Tex. Nov. 6, 2008) (citing *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008)) (“A Court may refuse to construe a commonly understood term if the proposed construction would create ambiguity or confuse the jury.”) (cleaned up). Greenthread agrees with the second part of Cirrus’ construction that “[p]ortions of a well are not well regions,” but like the Court did before, this is best handled as a note not for the jury.

8. “said graded concentration”/“the graded dopant” (195:5-6; 481:7, 31; 222:7, 32; 014:7)

Greenthread	Cirrus
Not indefinite. Plain and ordinary meaning.	Indefinite

Cirrus makes the hyper-technical argument that because the antecedent basis appears twice in the independent claims, the dependent claims must be indefinite. To the contrary, it is abundantly clear from the face of the claims and the intrinsic record what is meant by the dependent claims. Ex. 1, ¶¶91-92. Exemplary independent claim 195:1 requires both a drift layer and a well

region having “a graded concentration of dopants.” Ex. 2, 4:18-29. Then dependent claim 195:5 specifies that “said graded concentration of dopants follows an exponential gradient.” Ex. 2, 4:36-39. The fact that the independent claim uses the exact same language—“a graded concentration of dopants”—for both the drift layer and the well region, and then specifies it follows an exponential gradient, makes it abundantly clear that the additional limitation applies to both the drift layer and the well region. Similarly, the additional limitations in the other dependent claims would apply to both antecedent bases in the independent claim. Ex. 1, ¶92. To the extent there is any doubt from the face of the claims, a POSITA would read the specification to understand it does not limit the gradient to a particular location. Ex. 2, 2:40-41 (“The gradient can be ... quasi linear [or] exponential...”). Therefore, a POSITA would understand it applies to **both** of the antecedent bases in the independent claim. Ex. 1, ¶¶91-92. When, as here, a POSITA can determine that the limitation applies to both of the antecedent bases, the claim is not indefinite. *Summit 6 LLC v. HTC Corp.*, No. 7:14-CV-00014-O, 2015 WL 11117868, at *17 (N.D. Tex. Mar. 21, 2015) (determining that “said identification” in dependent claim applied to **both** uses of the word “identification” in the independent claim); *Gen. Atomics v. Axis-Shield*, No. C 05-04074 SI, 2006 WL 2792428, at *6-8 (N.D. Cal. Sept. 27, 2006) (determining “said analyte” applied to **both** uses of the “analyte”).

B. Claim Term Found in Claim 502:8

9. “respective active regions” (502:8)

Greenthread	Cirrus
Not indefinite. Plain and ordinary meaning.	Indefinite

For this term, Cirrus makes another hyper-technical antecedent basis argument. Once again, Cirrus ignores that patent claims are not read in a vacuum. Rather, they are read in light of the specification through the eyes of one skilled in the art. *Nautilus*, 572 U.S. at 910.

For this term, Cirrus argues that because independent claim 502:7 specifies “an active region” and dependent claim 502:8 references “respective active regions,” the dependent claim must be indefinite. In doing so, Cirrus overlooks the obvious. There may be multiple transistors, as shown in Fig. 5C of the 502 patent, where there is an active region for each transistor. Dependent claim 502:8 clearly contemplates that the active region in independent claim 502:7 comprises multiple active regions. A POSITA reading claim 502:8 would readily understand that the electric fields are adapted to each of the active regions. Ex. 1, ¶93.

C. Claim Terms Found in Exemplary Claims 842:1 & 9

10. “active region...within which transistors can be formed” (842:1, 9; 481:1, 20; 222:1, 21, 39, 41-42; 014:1, 21)

Previous Constructions/Greenthread	Cirrus
Not indefinite. Plain and ordinary meaning.	Indefinite

This Court and the District of Oregon already determined that this term is not indefinite, and it should be given its plain and ordinary meaning. Cirrus is merely rehashing arguments that have already been rejected. In fact, Cirrus essentially copied Intel’s opening brief *verbatim*, including Intel’s misleading use of ellipsis and brackets to hide the real story. *Compare* Dkt. 35-40 *with Intel* Dkt. 82, 36-42. Cirrus did, however, delete the portions of the specification that support Greenthread’s claim construction. *See Intel* Dkt. 82, 37 n. 18.

A POSITA reading the claims and intrinsic record would understand this term means exactly what it says: an active region (*i.e.*, a doped region at the surface of a semiconductor device, *see* term #3 above) where a transistor can be formed. Ex. 1, ¶¶94-105. Intel’s indefiniteness arguments (now Cirrus’s arguments) start with the unsupported premise that an active region is where current flows. Next, Cirrus mistakenly argues that the specification and prosecution history for the earlier 195 and 502 patents say the same, while the prosecution history for the later patents

conflate the “active region” with the surrounding “well region.” This is *not* true. In the specification and entire prosecution history, Dr. Rao consistently used “active region” to refer to the doped regions at the surface of a semiconductor device (*e.g.*, the source and drain) where, for example, a MOSFET transistor is built or can be built. As Dr. Glew explains in his declaration, the term “well region” can be used to refer to the doped silicon that surrounds the “active region” where the source and drain are formed. Cirrus, on the other hand, confuses the two. While the active region may be “located within” or “surrounded by” the well region, Dr. Rao made it clear that the active region is where the transistors are built or may be built. When the term “active region...within which transistors can be formed” is properly viewed in this context through the eyes of a POSITA, there is nothing indefinite about it. Ex. 1, ¶95.

An “active region” does not require current flow. Cirrus baldly asserts without any support that “a region is ‘active’ when an existing device is formed there causing electrical current to flow.” Dkt. 35, 40. This is not true. An active region does not have to be “electrified” to form a channel between a source and drain in order to qualify as an active region. Ex. 1, ¶96. For example, in order for a channel to form in a MOSFET, terminals must be attached to the source, drain, and gate, and a voltage must be applied to the gate to repel the minority carriers away from the surface layer. The fact that the transistor is not “electrically active” such that current is not flowing through the transistor does not mean that an active region does not exist. *Id.*

The specification confirms that an “active region” is a doped region at the surface of a semiconductor device where a transistor can be built. *Id.*, ¶97. While Cirrus essentially copied Intel’s opening brief, it deleted the following citations, which Greenthread relied on in the previous case to show that the specification supports Greenthread’s construction. *See Intel* Dkt. 82, 37 n. 18 (citing the following); Abstract (referring to “active region” without mention of current flow);

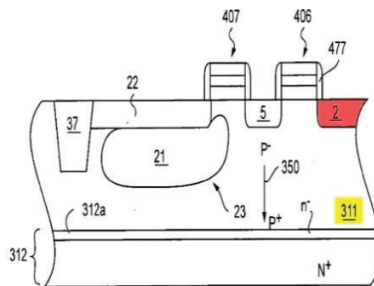
2:16-18 (referring to “active devices,” not “active regions”); 2:25-26 (referring to Figs. 3B-D, where the “active regions” are shown as doped regions at the surface where transistors are built; none of the figures show a current flow); 3:62-63 (referring to “active circuitry,” not “active regions”); Fig. 3A, 5A (referring to “active devices,” not “active regions”); Figs. 3C, 5B-C (all showing active regions has doped regions at the surface where transistors are built); claim 5 (merely saying a particular type of transistor can be built in the active regions); claim 7 (merely saying the active regions are separated by an isolation regions; claim 18 (merely saying the transistor that can be built in the active region is a typical MOSFET).

Completely ignoring Greenthread’s responsive brief in the *Intel* case, Cirrus repeats Intel’s failed argument that the specification never describes a regions that is both an “active region,” and a “region...within which transistors can be formed.” Dkt. 35, 41. Cirrus’ argument (which it copied from Intel) misses the obvious. The 842 patent repeatedly describes active regions where transistors *are* built. Ex. 2, 2:24-27, 3:10-13; Fig. 3C, 5B-5C. This is proof that these “active regions” are “regions...within which transistors can be formed.” Ex. 1, ¶¶98. Cirrus’ argument is like arguing that real estate zoned for commercial use (*i.e.*, real estate where commercial property can be built), is no longer commercial real estate once a commercial building is built there.

The earlier prosecution history confirms that “active region” is a doped region where a transistor can be built. *Id.*, ¶¶99-105. Cirrus falsely asserts that Greenthread referred to the claimed “active region” as the current path of an existing transistor. Dkt. 35, 41. This is not true. Cirrus’ citations to the prosecution history actually support Greenthread, not Cirrus. ***First***, Cirrus cites to where Applicant mentions “active and well regions,” and then states an “active element” (*i.e.*, a pair of transistors) “can be active when a voltage (or current) is applied.” This statement confirms that an “active region” is an “active region” regardless of whether the “active element”

is turned “on.” *Second*, Cirrus cites to a prior art reference’s use of the term “electrically active.” *Id.* (citing Dkt. 35-11 (Rhodes)). But “electrically active” (as opposed to “active”) confirms that an “active region” does *not* have to have an electrical current. If an “active region” necessarily required an electrical current, then it would be redundant to say “electrically active.” *Finally*, as Cirrus correctly notes, Applicant has identified the “active region” as the doped region at the surface where the transistor is built. Dkt. 35, 43. Ex. 1, ¶¶99-101.

The later prosecution history also confirms that “active region” is a doped region at the surface where a transistor can be built. Any confusion was created by the Examiner, not Dr. Rao. To compound the confusion, Cirrus has falsely accused Dr. Rao of agreeing with the Examiner’s incorrect positions. This is not true. Rather Dr. Rao was merely explaining that even under the Examiner’s incorrect construction, his invention is still patentable over the prior art. During prosecution, the Examiner relied on Fig. 4D from Hong to reject then-pending claim 1.



Ex. 1, ¶102; Ex. 13 (842 file history), 101-110; Dkt. 35-12 (Hong), 6 (Fig. 4D). Hong makes clear that 311 is the substrate, *id.*, [0030]; and 2 is the “source/drain region,” *id.*, [0040]. Ex. 1, ¶103. Nonetheless, the Examiner took the position that “311, which includes wells such as 21, 22, 5, 2” could be the “first active region”; and “source/drain region 2” could be the “second active region.” Ex. 13, 113. Obviously this rejection was flawed. But this is the rejection that Dr. Rao was responding to. *Id.*, 111-117. In doing so, Dr. Rao *never* said that numeral 311 was an active region, as Cirrus wrongly suggests. Rather Dr. Rao was merely explaining that even under the

Examiner's incorrect rejection Figure 4B did not meet the limitations of the pending claim. This is why he wrote:

The Examiner has referred to the first active region as the region 311, but has referred to the regions 21, 22, 5 and 2 as "wells." As discussed in the prior Response, there is no support for such a construction, as the term "wells" in semiconductor technology typically refers to a region formed in a substrate within which active components are formed. The Examiner has referred to the second active region as being that defined by the source/drain region 2 or the regions 2 or 5 or 22 of the pixel cell.

Id., 108-109 (highlighting added). With the use of suspect bracketing and ellipses, Cirrus omitted the highlighted portions to hide that Dr. Rao did not agree with the Examiner's construction for the "first active region." Meanwhile, he did not dispute that a source/drain region could be an active region. Thus, the prosecution history supports Greenthread, not Cirrus. Ex. 1, ¶¶104-105.

11. "the surface thereof"/"the surface" (842:9; 481:20; 222:21; 014:21)

Greenthread	Cirrus
Not indefinite. Plain and ordinary meaning.	Indefinite

This term is related to the previous term. As discussed above, independent claim 842:1 requires an active region "within which transistors can be formed." Similarly independent claim 842:9 requires an active region "within which transistors can be formed in the surface thereof." Ex. 4, 5:17-23. POSITAs and lay persons alike know what "thereof" means, and it is readily apparent from the face of the claim that in claim 842:9, the transistor can be formed in the surface of the active region. Ex. 1, ¶106; Ex. 17, 1296. This is exactly what is shown in the preferred embodiment in Fig. 5C, where there is a source and drain at the surface of the active region.

Once again, Cirrus is making a hyper-technical antecedent basis argument that ignores the law. Patent claims are not read in a vacuum; they are read in light of the intrinsic record through the eyes of one skilled in the art. *Nautilus*, 572 U.S. at 910. In its brief, Cirrus feigns ignorance, but then states the obvious: "The word 'thereof' suggests that 'the surface thereof' may refer to a

surface of the active regions.” Dkt. 35, 45. A POSITA reading the claim would have readily understood exactly that. Ex. 1, ¶106. Cirrus’ own brief is proof that this term is not indefinite. When, as here, a later term (“the surface thereof”) is referring to an inherent part (“surface”) of the antecedent basis (“first active region”), it is entirely proper to use “the” as Dr. Rao did when he referred to “the surface thereof.” *Bose Corp. v. JBL, Inc.*, 274 F.3d 1354, 1359 (Fed. Cir. 2001) (““Inherent components of elements recited have antecedent basis in the recitation of the components themselves.”) (quoting MPEP § 2173.05(e)).

12. “aid carrier movement from the surface to the substrate” (842:9; 481:20)

Greenthread	Cirrus
Not indefinite. Plain and ordinary meaning.	Indefinite

Once again, Cirrus makes a hyper-technical antecedent basis argument that ignores the obvious. As explained for the previous term, claim 842:9 requires an active region where transistors can be formed in the surface of the active region (*i.e.*, active region...within which transistors can be formed in the surface thereof”). The last clause of claim 842:9 specifies that this active region has a graded dopant concentration to “aid carrier movement from the surface to the substrate.” A POSITA reading the claim in light of the specification would have readily understood that the graded dopant concentration is aiding carrier movement from the surface *of the active region* to the substrate. Ex. 1, ¶¶107-108. This is exactly what is shown in the preferred embodiment in Fig. 5C. *Id.*

Cirrus makes two flawed arguments that rely on the same “nonsensical” premise (Cirrus’ own word choice). **First**, Cirrus argues that it is unclear whether the term is referring to either the first or second surface *of the substrate*. The answer is neither. It is clear from the face of the claim that (1) the active region has a surface, and (2) the graded dopants are in the active region. Ex. 1,

¶107. Therefore, the graded dopants are aiding carrier movement from the surface *of the active region* to the substrate. *Id.* It makes no sense to say that the graded dopants would aid movement from the surface *of the substrate* to the substrate. *Id.*

Yet this is exactly Cirrus’ ***second*** argument. Cirrus states “it is nonsensical for carriers to move from the substrate to the substrate itself.” Dkt. 35, 44-45. This statement and the use of the word “nonsensical” is further proof that Greenthread’s reading of the claim is correct. When this term is properly read in light of the specification through the eyes of a POSITA, there is nothing indefinite about this term.

IV. CONCLUSION

For the reasons above, terms 1, 2, 4, and 8-12 are not indefinite, and all of the terms should be given their plain and ordinary meaning.

Dated: December 14, 2023

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the above and foregoing document has been served on all counsel of record via the Court's ECF system on December 14, 2023.

/s/ Alan L. Whitehurst
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