Doc Code: PET.POA.WDRW
Document Description: Petition to withdraw attorney or agent (SB83)

PTO/AIA/83 (04-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	13/059,336, Patent No. 8,525,446
Filing Date	September 17, 2009
First Named Inventor	David Tikkanen
Art Unit	2819
Examiner Name	Jason Crawford
Practitioner Docket Number	6008.012

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please withdraw me as attorney or agent for the above-identified patent application, and

☐ all the practitioners of record;

☐ the practitioners (with registration numbers) of record listed on the attached paper(s); or

☒ the practitioners of record associated with Customer Number: 30589

NOTE: The immediately preceding box should only be marked when the practitioners were appointed using the listed Customer Number.

The reason(s) for this request are those described in 37 CFR:

☐ 11.116(a)(1) ☐ 11.116(a)(2) ☒ 11.116(a)(3)
☒ 11.116(b)(1) ☐ 11.116(b)(2) ☐ 11.116(b)(3)
☐ 11.116(b)(4) ☐ 11.116(b)(5) ☐ 11.116(b)(6)
☐ 11. 116(b)(7) Please explain below:

Certifications

Check each box below that is factually correct. WARNING: If a box is left unchecked, the request will likely not be approved.

1. ☒ I/We have given reasonable notice to the client, prior to the expiration of the response period, that the practitioner(s) intend to withdraw from employment.

2. ☒ I/We have delivered to the client or a duly authorized representative of the client all papers and property (including funds) to which the client is entitled.

3. ☒ I/We have notified the client of any responses that may be due and the time frame within which the client must respond.

Please provide an explanation, if necessary:

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/83 (04-13)
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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Complete the following section only when the correspondence address will change. *Changes of address will only be accepted to an applicant.*

Change the correspondence address and direct all future correspondence to:

A. ☐ The address of the applicant associated with Customer Number: _____

OR

B. ☒ Applicant

Address 219 W. Wilshire Blvd. Suite 104D

City	State	Zip	Country
Oklahoma City	OK	73116	US

Telephone 405-520-9220 Email Jenn@onyxtheater.com

I am authorized to sign on behalf of myself and all withdrawing practitioners.

Signature /Ann M. Robl/

Name Ann M. Robl Registration No. 71541

Address 609 W. Sheridan

City	State	Zip	Country
Oklahoma City	OK	73102	US

Date April 28, 2021 Telephone No. 405-607-8600

NOTE: Withdrawal is effective when approved rather than when received.

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	42581110
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	30589
Filer:	Ann M. Robl/Bradley Thompson
Filer Authorized By:	Ann M. Robl
Attorney Docket Number:	6008.012
Receipt Date:	28-APR-2021
Filing Date:	22-MAR-2011
Time Stamp:	16:07:23
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	6008012_SB21Transmittal_04282021.pdf	165938 63ad5ad821c7ed61bf23e76c250acc80d8a19bcc	no	1

Warnings:

Information:					
2	Petition to withdraw attorney or agent (SB83)	6008012_AIA83Withdrawal_04282021.pdf	133972 7b13e8bd5ff7f7df7e5f0336b7685c2046e8862f	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	299910	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: TRAN.LET

Document Description: Transmittal Letter

PTO/SB/21 (07-09)
Approved for use through 12/31/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	13/059,336, Patent No. 8,525,446
Filing Date	September 17, 2009
First Named Inventor	David Tikkanen
Art Unit	2819
Examiner Name	Jason Crawford
Attorney Docket Number	6008.012

Total Number of Pages in This Submission: 3

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☑ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please identify below):

Remarks

Electronically Transmitted:

1) sb21 Transmittal (1 page); and,
2) aia83 Request for Withdrawal as Attorney or Agent and Change of Correspondence Address (2 pages)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Dunlap Codding, P.C.		
Signature	/Ann M. Robl/		
Printed name	Ann M. Robl		
Date	April 28, 2021	Reg. No.	71,541

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	/Ann M. Robl/		
Typed or printed name	Ann M. Robl	Date	April 28, 2021

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
13/059,336	03/22/2011	David Tikkanen	6008.012	129954

Acknowledgement of Change to Small Entity Status

The entity status change request below filed through Private PAIR on 01/21/2021 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant asserting small entity status. See 37 CFR 1.27.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Ann M. Robl/
Name:	Ann M. Robl
Registration Number:	71541

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/059,336	03/22/2011	David Tikkanen	K8001064WOUS

CONFIRMATION NO. 9207

POWER OF ATTORNEY NOTICE

34236
GOWLING WLG (CANADA) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

OC000000122532123

Date Mailed: 01/11/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/04/2021.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/zabraha/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/059,336	03/22/2011	David Tikkanen	K8001064WOUS

CONFIRMATION NO. 9207

30589
DUNLAP CODDING, P.C.
PO BOX 16370
OKLAHOMA CITY, OK 73113

POA ACCEPTANCE LETTER

OC000000122532136

Date Mailed: 01/11/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/04/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/zabraha/

PTO/AIA/80 (07-17)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

[X] Practitioners associated with Customer Number: 30589

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

[X] The address associated with Customer Number: 30589

OR

[ ]

Firm or individual name		
Address		
City	State	Zip
Country		
Telephone	Email	

Assignee name and address: Mate, LLC
219 W. Wilshire Blvd, Suite 104D
Oklahoma City, Oklahoma 73116

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature Jon Upton	Date 12/20/20
Name Jon Upton	Telephone 405-520-9220
Title Manager, Mate. LLC	

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Lumastream Canada ULC

Application No./Patent No.: 8,525,446 Filed/Issue Date: 09/03/2013

Titled: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

Mate. LLC, a limited liability corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: David Tikkanen, Jason Neudorf, Steven Lyons, Todd Scott, Kyle Hathaway, and David Jansen To: Electronic Craftsmen Corporation

   The document was recorded in the United States Patent and Trademark Office at
   Reel 025818, Frame 0970, or for which a copy thereof is attached.

2. From: Electronic Craftsmen Corporation To: E Craftsmen Corporation

   The document was recorded in the United States Patent and Trademark Office at
   Reel 025819, Frame 0023, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: E Craftsmen Corporation To: Lumastream Canada ULC

The document was recorded in the United States Patent and Trademark Office at
Reel 026192, Frame 0220, or for which a copy thereof is attached.

4. From: Lumastream Canada ULC To: Lumastream, Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 054134, Frame 0089, or for which a copy thereof is attached.

5. From: Lumastream, Inc. To: E Craftsmen Corporation

The document was recorded in the United States Patent and Trademark Office at
Reel 054134, Frame 0330, or for which a copy thereof is attached.

6. From: E Craftsmen Corporation To: Mate. LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 054709, Frame 0940, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Ann M. Robl/	January 4, 2021
Signature	Date
Ann M. Robl	71,541
Printed or Typed Name	Title or Registration Number

Electronic Acknowledgement Receipt

EFS ID:	41542298
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	34236
Filer:	Ann M. Robl/Anne Burns
Filer Authorized By:	Ann M. Robl
Attorney Docket Number:	K8001064WOUS
Receipt Date:	04-JAN-2021
Filing Date:	22-MAR-2011
Time Stamp:	13:16:19
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	6008012_sb21_Transmittal_01042021.pdf	170600 ee984ac22f72a450cb8eff63e70cfbf818443c0e	no	1

Warnings:

Information:					
2	Power of Attorney	6008012_AIA80_POA_01042021.pdf	109212 51bba786d365b2e28ea4d732dcb464118fe6b1ec	no	1
Warnings:					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73	6008012_AIA96_Statement_01042021.pdf	82222 d900385d756542732082bc498167cf1cce4c30ca	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	362034	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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Doc Code: TRAN.LET

Document Description: Transmittal Letter

PTO/SB/21 (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	13/059,336
Filing Date	March 22, 2011
First Named Inventor	David Tikkanen
Art Unit	2819 (conf. 9207)
Examiner Name	Jason Crawford
Attorney Docket Number	6008.012

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☑ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please identify below):

  See Remarks

Remarks

Electronically Transmitted: January 4, 2021

1) sb21 Transmittal (1 page);
2) AIA60 Power of Attorney (1 page); and
3) AIA96 Statement Under 37 CFR 3.73(c) (2 pages).

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	DUNLAP CODDING, P.C.		
Signature	/Ann M. Robl/		
Printed name	Ann M. Robl		
Date	January 4, 2021	Reg. No.	71,541

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being electronically transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	/Ann M. Robl/		
Typed or printed name	Ann M. Robl	Date	January 4, 2021

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/059,336	03/22/2011	David Tikkanen	K8001064WOUS

CONFIRMATION NO. 9207

34236
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

POA ACCEPTANCE LETTER

OC000000078803135

Date Mailed: 11/23/2015

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/17/2015.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmturner myles/

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/059,336	03/22/2011	David Tikkanen	K8001064WOUS

CONFIRMATION NO. 9207

POWER OF ATTORNEY NOTICE



26123
BORDEN LADNER GERVAIS LLP (Ottawa)
Shin Hung
WORLD EXCHANGE PLAZA
100 QUEEN STREET SUITE 1300
OTTAWA, ON K1P 1J9
CANADA

Date Mailed: 11/23/2015

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/17/2015.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmturner myles/

PTO/SB/81A (12-08)
Approved for use through 11/30/2011. OMB 0651-0035
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PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	8,525,446
Issue Date	2013-09-03
First Named Inventor	TIKKANEN, David
Title	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
Attorney Docket Number	K8001064WOUS

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 34236

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Inventor, having ownership of the patent.

OR

☒ Patent owner.
Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____

SIGNATURE of Inventor or Patent Owner

Signature		Date	Aug 21/2014
Name	David TIKKANEN	Telephone	819 744-5677
Title and Company	Vice President, Lumastream Canada ULC		

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	24110060
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	26123
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	17-NOV-2015
Filing Date:	22-MAR-2011
Time Stamp:	16:12:56
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		20151117160629861.pdf	305690 aab6d397d2b2b84bc92aa99531b9a80143feb9d4	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Assignee showing of ownership per 37 CFR 3.73	1	1
	Power of Attorney	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	305690	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Lumastream Canada ULC

Application No./Patent No.: 8,525,446 Filed/Issue Date: 2013-09-03

Titled:

Lumastream Canada ULC , a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: TIKKANEN, David; NEUDORF, Jason; LYONS, Steven; SCOTT, Todd William; HATHAWAY, Kyle Grahame; JANSEN, David Wainesworth To: ELECTRONIC CRAFTSMEN CORPORATION

The document was recorded in the United States Patent and Trademark Office at Reel 025818, Frame 0970, or for which a copy thereof is attached.

2. From: ELECTRONIC CRAFTSMEN CORPORATION To: E CRAFTSMEN CORPORATION

The document was recorded in the United States Patent and Trademark Office at Reel 025819, Frame 0023, or for which a copy thereof is attached.

3. From: E CRAFTSMEN CORPORATION To: LUMASTREAM CANADA ULC

The document was recorded in the United States Patent and Trademark Office at Reel 026192, Frame 0220, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jeffrey W. Wong/ 2015-11-17

Signature Date

Jeffrey W. Wong Agent, Reg. No. 46414

Printed or Typed Name Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/96 (07-09)
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Lumastream Canada ULC

Application No./Patent No.: 8,525,446 Filed/Issue Date: 2013-09-03

Titled: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

Lumastream Canada ULC , a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: TIKKANEN, David; NEUDORF, Jason; LYONS, Steven; SCOTT, Todd William; HATHAWAY, Kyle; JANSEN, David Wainesworth To: ELECTRONIC CRAFTSMEN CORPORATION

The document was recorded in the United States Patent and Trademark Office at Reel 025818 , Frame 0970 , or for which a copy thereof is attached.

2. From: ELECTRONIC CRAFTSMEN CORPORATION To: E CRAFTSMEN CORPORATION

The document was recorded in the United States Patent and Trademark Office at Reel 025819 , Frame 0023 , or for which a copy thereof is attached.

3. From: E CRAFTSMEN CORPORATION To: LUMASTREAM CANADA ULC

The document was recorded in the United States Patent and Trademark Office at Reel 026192 , Frame 0220 , or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jeffrey W. Wong/ 2014-10-14

Signature Date

Jeffrey W. Wong Agent, Reg. No. 46414

Printed or Typed Name Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/81A (12-08)
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PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	8,525,446
Issue Date	2013-09-03
First Named Inventor	TIKKANEN, David
Title	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
Attorney Docket Number	K8001064WOUS

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 34236

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Inventor, having ownership of the patent.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____.

SIGNATURE of Inventor or Patent Owner

Signature		Date	Aug 21/2014
Name	David TIKKANEN	Telephone	519 744-5677
Title and Company	Vice President, Lumastream Canada ULC		

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	20406137
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	26123
Filer:	Jeffrey Wong
Filer Authorized By:	
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	14-OCT-2014
Filing Date:	22-MAR-2011
Time Stamp:	12:33:06
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	K8001064WOUS-POA.pdf	315744 5b66e87366ec8d21eae3b36099a10110e225b643	no	2

Warnings:	
Information:	

Total Files Size (in bytes):	315744

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/059,336	09/03/2013	8525446	PAT 67545W-2	9207

26123 7590 08/14/2013

BORDEN LADNER GERVAIS LLP
Anne Kinsman
WORLD EXCHANGE PLAZA
100 QUEEN STREET SUITE 1100
OTTAWA, ON K1P 1J9
CANADA

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 246 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

David Tikkanen, Waterloo, CANADA;
Jason Neudorf, Kitchener, CANADA;
Steven Lyons, Kitchener, ON, CANADA;
Todd William Scott, Waterloo, ON, CANADA;
Kyle Grahame Hathaway, Kitchener, ON, CANADA;
David Wainesworth Jansen, Waterloo, ON, CANADA;

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Change(s) applied to document, /S.W./ 5/20/2013

Please replace the 6th paragraph, starting at ~~line 20~~ line 25, on page 9 with the following amended paragraph:

The current source 92 preferably includes ancillary circuitry for operation and comprises a buck topology power stage with hysteretic control. The current sense 94 provides a digital feedback loop for each current source 92. In the preferred embodiment, the current source 92 is a buck circuit topology however other embodiments can include topologies such as boost, buck-boost, or single ended primary ~~redactor~~ inductor converter ~~converter~~ (SEPIC).

Please replace the 2nd paragraph, starting at ~~line 3~~ line 6, on page 14 with the following amended paragraph:

Furthermore, the communication interface 74 can be adapted to have one or more 0 - 10 Vdc signal voltages control an associated group of one or more output current drivers in ~~zone~~ zonal dimming applications. An optional master 0 - 10 Vdc signal voltage could be able to simultaneously control all of the individual groups of output current drivers.

instance, the dimmer 10 can also include an EMI filter and a bridge rectifier. With respect to connections, it will be understood that the primary digital controller 58 can also be connected to the PFC boost 44, the inrush current limit 40 and the DC/DC ~~controller~~ converter 46 while the secondary digital controller 64 can be connected to the output voltage bus 48, the power limit 50 and the output current drivers 52.

line 26

Please replace the 4th paragraph, starting at ~~line 20~~, on page 6 with the following amended paragraph:

Change(s) applied to document, /S.W./ 5/20/2013

In operation, the PFC Boost 44 and DC/DC Converter 46 are controlled by the primary side digital controller 58 while the secondary digital controller 64 monitors the output voltage bus 48 and provides digital feedback control information via isolated communication bus ~~66~~ 61 to regulate the output voltage bus 48. Secondary digital controller 64 also translates dimming and/or color mixing information from the external transmitter 76 into LED control information for the output current drivers 52. The primary 58 and secondary 64 digital controllers and output current drivers 52 have an associated programming port for further configuring the LED dimmer 10.

line 15

Please replace the 3rd paragraph, starting at ~~line 9~~, on page 7 with the following amended paragraph:

Turning to Figure 5, an embodiment of an improved inrush current limit 40 is shown. An EMI filter 82 is connected between the power supply and the current limit 40 and is connected directly to the PFC boost 44 and via the current limit 40. The current limit 40 includes a thermistor 84, a relay or relay contact ~~coil~~ 86 and a switch 59. The relay ~~coil~~ contact 86 is connected in parallel with the thermistor 84. A typical relay coil requires greater energy to close the contacts than is required with the currently described limiter 40 to maintain the contacts in a closed position since less holding force is required. After the relay contacts have been closed by applying a voltage of 12 Vdc, modulation of the relay coil voltage can be initiated by the primary controller 58 to effectively reduce the average voltage across the coil to approximately 5 volts versus a DC voltage of 12V, reducing power consumption. It should be noted that the pulse duty cycle and frequency can also be changed to improve or optimize performance.

Amendments to the Specification

Please replace the 4th paragraph, starting at ~~line 18~~ line 24, on page 5 with the following amended paragraph:

Change(s) applied to document, /S.W./ 5/20/2013

Turning to Figure 3, a block diagram of another embodiment of the LED dimmer is shown. The LED dimmer 10 includes an inrush current limit 40, or inrush current limit circuit, which receives power from an AC power source or supply 42, located external to the dimmer 10. The inrush circuit 40 is connected to a Power Factor Correction (PFC) Boost 44 which, in turn, is connected to a DC/DC Converter 46, or power conversion stage. The converter 46 is connected to an Output Voltage ~~Base~~ bus 48 which is connected to a power limiter 50. The inrush circuit 40, the PFC boost 44, the DC/DC converter 46, the Output Voltage Base bus 48 and the power limit 50 can be seen as a power circuit 47. Although only one power limit 50 is shown, it will be understood that there could be multiple power limits. The power limiter 50 is connected to a set of output current drivers 52, whereby each of the output current drivers 52 has an associated in-circuit serial programming (ICSP) port 54. The output of the output current drivers 52 is connected to individual Organic Light-Emitting Diodes (OLED)/Light-Emitting Diodes (LED) loads 56, further referred to as LED loads.

Please replace the 1st paragraph, starting at ~~line 1~~ line 7, on page 6 with the following amended paragraph:

Along with the above-identified components and circuitry, the dimmer 10 further includes a primary digital controller 58 which is connected to an auxiliary power source 60 and an ICSP Port 62. The primary digital controller 58 is further connected, via an isolated communication bus ~~66~~ 61 to a secondary digital controller 64, which receives power from the auxiliary power source 60. An ICSP port 68 is also connected to the secondary digital controller 64.

Please replace the 3rd paragraph, starting at ~~line 13~~ line 19, on page 6 with the following amended paragraph:

As will be understood, not all of the components or connections of the LED dimmer 10 required for operation are shown as they will be understood by one skilled in the art. For

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13059336
Filing Date	2011-02-16
First Named Inventor	David TIKKANEN
Art Unit	2821
Examiner Name	
Attorney Docket Number	PAT 67545W-2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/JC/	1	5420780		1995-05-30	Bernstein et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
Change(s) applied to document. /JC/ /A.E.M./ 6/18/2013	1	20020047642		2002-04-25	Miyagawa ~~ROHM CO., LTD.~~	Figs. 6, 7
	2	20080018261		2008-01-24	Kastner	Fig. 20; Para. 102
	3	20090179594		2009-07-16	Yang	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/JC/	1	2009039112	WO		2009-03-26	EXCLARA, INC.	Figs. 1, 10	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

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26123 7590 05/09/2013
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Anne Kinsman
WORLD EXCHANGE PLAZA
100 QUEEN STREET SUITE 1100
OTTAWA, ON K1P 1J9
CANADA

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/059,336	03/22/2011	David Tikkanen	PAT 67545W-2	9207

TITLE OF INVENTION: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	08/09/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JASON	2819	315-312000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Jeffrey W. Wong
2 Borden Ladner Gervais LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Lumastream Canada ULC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Calgary, Alberta, CANADA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies .....

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- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 501593 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Jeffrey W. Wong/ Date July 30, 2013

Typed or printed name Jeffrey W. Wong Registration No. 46414

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal

Application Number:	13059336
Filing Date:	22-Mar-2011
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Filer:	Jeffrey Wong/Tara Charbonneau
Attorney Docket Number:	PAT 67545W-2

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2080**

Electronic Acknowledgement Receipt

EFS ID:	16450145
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	26123
Filer:	Jeffrey Wong/Tara Charbonneau
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	30-JUL-2013
Filing Date:	22-MAR-2011
Time Stamp:	11:22:18
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2080
RAM confirmation Number	10240
Deposit Account	501593
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	PAT67545W-2_Fee_Trans.pdf	320922 21961015c7d48858f270ea4ae51e7efa72e2f993	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32416 49db3b965687d73911023fcc1533042f1e1c7e6e	no	2
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

26123 7590 05/09/2013

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Anne Kinsman
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OTTAWA, ON K1P 1J9
CANADA

EXAMINER
CRAWFORD, JASON

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/09/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/059,336	03/22/2011	David Tikkanen	PAT 67545W-2	9207

TITLE OF INVENTION: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	08/09/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

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For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/059,336	03/22/2011	David Tikkanen	PAT 67545W-2	9207

TITLE OF INVENTION: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	08/09/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JASON	2819	315-312000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
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3 _____

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(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

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4a. The following fee(s) are submitted:
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5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

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Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/059,336	03/22/2011	David Tikkanen	PAT 67545W-2	9207

26123 7590 05/09/2013

BORDEN LADNER GERVAIS LLP
Anne Kinsman
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OTTAWA, ON K1P 1J9
CANADA

EXAMINER	
CRAWFORD, JASON	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/09/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 246 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 246 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/059,336	Applicant(s) TIKKANEN ET AL.	
	Examiner Jason M. Crawford	Art Unit 2819	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/12/13*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1,3,4 and 6-23*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

   Interim copies:

   a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 2/16/11,8/31/12,10/2/12
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Jason M. Crawford/
Primary Examiner, Art Unit 2819

DETAILED ACTION

Drawings

The drawings were received on 4/12/2013. These drawings are accepted by the Examiner.

Miscellaneous

The Applicant has cancelled claims 2, 5 and added new claims 21-23; therefore only claims 1, 3-4 and 6-23 remain for this Office Action.

Allowable Subject Matter

Claims 1, 3-4 and 6-23 are allowed. The following is an examiner's statement of reasons for allowance:

In regards to claim 1, the prior art discloses of the claimed subject matter with the exception of the configurable light emitting diode (LED) driver/dimmer further comprising a power circuit including: *an inrush current limit; a DC/DC converter; a power factor correction (PFC) boost connected to the inrush current limit and the DC/DC converter; a regulated output voltage bus connected to the DC/DC converter; and at least one power limit connected to the output voltage bus*, nor would it have been obvious to one of ordinary skill in the art to do so. Claims 3-4 and 6-22 are also allowed as being dependent on claim 1.

In regards to claim 23, the prior art does not disclose of a power circuit for a configurable light-emitted diode (LED) driver, the power circuit comprising: *an inrush*

current limit; a DC/DC converter; a power factor correction (PFC) boost connected to the inrush current limit and the DC/DC converter; an output voltage bus connected to the DC/DC converter; and at least one power limit connected to the output voltage bus, nor would it have been obvious to one of ordinary skill in the art to do so.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Crawford whose telephone number is (571)272-6004. The examiner can normally be reached on Mon-Fri 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shawki Ismail can be reached on (571) 272-3985. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M. Crawford/
Primary Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 13/059,336	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.	
	Examiner Jason M. Crawford	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0018261	01-2008	Kastner, Mark Allen	315/192
*	B	US-2008/0025028	01-2008	Gloisten et al.	362/294
*	C	US-2002/0047642	04-2002	Miyagawa, Shozo	315/307
*	D	US-2010/0164403	07-2010	Liu, Da	315/297
*	E	US-2005/0218838	10-2005	Lys, Ihor A.	315/291
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S121	10	S120 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:37
S120	23	(ICSP (in adj circuit adj serial adj program$4)) and (DMX512 RDM zigbee)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:37
S119	1	(PFC (power adj factor)) and S118	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:36
S118	12	("20070267978" | "20090322234" | "20100164403").PN. OR ("7880400").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/04/18 07:36
S117	6	S116 and (DC adj DC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:36
S116	13	S115 and (LED (light adj emit$4 adj diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:36
S115	30	S114 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:36
S114	229	("315"/$.ccls. "361"/$.ccls.) and S113	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:36
S113	1644	S112 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:36
S112	2677	(PFC (power adj factor)) and (heatsink$3 (heat adj sink$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:36
S111	6	("315"/$.ccls. "361"/$.ccls.) and (ICSP (in adj circuit adj serial adj program$4)) and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35
S110	22	S109 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35

S109	34	((u adj shap$3) with (heatsink$3 (heat adj sink$3) fins)) and (LED adj2 control$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35
S108	10	S106 not S107	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35
S107	2	S106 and (thermistor and coil)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35
S106	12	S105 and (heatsink$3 (heat adj sink$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35
S105	29	(PFC (power adj factor)) and S104	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35
S104	152	S103 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35
S103	206	((inrush (in adj rush)) adj2 limit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:35
S102	4	S100 not S101	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:34
S101	6	S100 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:34
S100	10	S98 not S99	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:34
S99	2	S98 and (PFC (power adj factor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:34
S98	12	("315"/$.ccls. "361"/$.ccls.) and (ICSP (in adj circuit adj serial adj program$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:34
S97	0	S96 and (power adj limit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:27
S96	10	S95 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:26
S95	13	(inrush adj current) same (PFC (power adj factor$3 adj control$4)) same (DC adj DC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/04/18 07:26

JC

			IBM_TDB			
S94	102	S93 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:26
S93	146	(inrush adj current) and (PFC (power adj factor$3 adj control$4)) and (DC adj DC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 07:26

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S126	2	(ICSP (in adj circuit adj serial adj program$4)) and S125	US-PGPUB; USPAT; UPAD	OR	ON	2013/04/18 07:37
S125	2	S123 and (light$3 illuminat$3)	US-PGPUB; USPAT; UPAD	OR	ON	2013/04/18 07:37
S124	2	S123 and (light$3 illuminat$3)	US-PGPUB; USPAT; UPAD	OR	ON	2013/04/18 07:36
S123	4	S122 and @ad<"20080918"	US-PGPUB; USPAT; UPAD	OR	ON	2013/04/18 07:36
S122	7	(ICSP (in adj circuit adj serial adj program$4)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2013/04/18 07:36

4/18/2013 1:03:40 PM
H:\EAST\Workspaces\13059336.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13059336	TIKKANEN ET AL.
	Examiner	Art Unit
	JASON M CRAWFORD	2819

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
315	247,291,294,297,302,307,312	4/18/2013	JC

SEARCH NOTES		
Search Notes	Date	Examiner
See attached search	4/18/2013	JC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
All	see text search	4/18/2013	JC

	/JASON M CRAWFORD/ Primary Examiner.Art Unit 2819

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BIB DATA SHEET

CONFIRMATION NO. 9207

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/059,336	03/22/2011 RULE	315	2819	PAT 67545W-2

APPLICANTS

David Tikkanen, Waterloo, CANADA;
Jason Neudorf, Kitchener, CANADA;
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Todd William Scott, Waterloo, ON, CANADA;
Kyle Grahame Hathaway, Kitchener, ON, CANADA;
David Wainesworth Jansen, Waterloo, ON, CANADA;

**** CONTINUING DATA ***************************

This application is a 371 of PCT/CA09/01295 09/17/2009 JC
which claims benefit of 61/097,963 09/18/2008 JC

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

04/14/2011

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/JASON CRAWFORD/ Examiner's Signature	☐ JC Initials	CANADA	12	20	1

ADDRESS

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OTTAWA, ON K1P 1J9
CANADA

TITLE

CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

FILING FEE RECEIVED		
1110	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13059336
Filing Date	2011-02-16
First Named Inventor	David TIKKANEN
Art Unit	2821
Examiner Name	
Attorney Docket Number	PAT 67545W-2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/JC/	1	5420780		1995-05-30	Bernstein et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/JC/	1	20020047642		2002-04-25	ROHM CO., LTD.	Figs. 6, 7
	2	20080018261		2008-01-24	Kastner	Fig. 20; Para. 102
	3	20090179594		2009-07-16	Yang	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/JC/	1	2009039112	WO		2009-03-26	EXCLARA, INC.	Figs. 1, 10	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/

Receipt date: 10/02/2012	Application Number	13059336 13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2011-02-16
	First Named Inventor	David TIKKANEN
	Art Unit	2821
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/JC/	1	UKIPO (Examiner HUNT), SEARCH AND EXAMINATION REPORT UNDER SECTIONS 17 & 18(3), Patent Application No. GB1102782.8, 2012-09-06	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Jason Crawford/ (04/17/2013)	Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/

Receipt date: 10/02/2012	Application Number	13059336 13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2011-02-16
	First Named Inventor	David TIKKANEN
	Art Unit	2821
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2012-10-02
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13059336
Filing Date	2011-02-16
First Named Inventor	TIKKANEN, David
Art Unit	2821
Examiner Name	
Attorney Docket Number	PAT 67545W-2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/JC/	1	8197079		2012-06-12	RUUD ET AL	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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Receipt date: 08/31/2012	Application Number	13059336 13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2011-02-16
	First Named Inventor	TIKKANEN, David
	Art Unit	2821
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

	1		☐

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EXAMINER SIGNATURE

Examiner Signature	/Jason Crawford/ (04/17/2013)	Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Receipt date: 08/31/2012	Application Number	13059336	13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2011-02-16	
	First Named Inventor	TIKKANEN, David	
	Art Unit	2821	
	Examiner Name		
	Attorney Docket Number	PAT 67545W-2	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2012-08-31
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	TIKKANEN, David, ET AL.
Art Unit	
Examiner Name	
Attorney Docket Number	PAT 67545W-2

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/JC/	1	20050289279		2005-12-29	FAILS ET AL.	
	2	20050218838		2005-10-06	LYS	
	3	20080018261		2008-01-24	KASTNER	

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/JC/	1	2008052293	WO		2008-05-08	QUICK ET AL.		☐

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Receipt date: 02/16/2011	Application Number	13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	
	First Named Inventor	TIKKANEN, David, ET AL.
	Art Unit	
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	Attorney Docket Number	PAT 67545W-2

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/JC/	1	ERICSSON AB, Power Supplies Goes Digital White Paper, October 2006	☐
	2	SKANDA; MICROCHIP TECHNOLOGY INC., Power Factor Correction in Power Conversion Applications using the dsPIC® DSC", AN1106, June 2007	☐
	3	TRAXON TECHNOLOGIES, LED Engine XB 3W-108 Technical Specifications and User Manual Version 1.1, 2007	☐
	4	PENWELL CORPORATION, Dialight Lumidrives Launches Colurdriver XP for High-Power LEDs, LEDs MAGAZINE, downloaded from http://www.ledsmagazine.com/press/15469, 2007-09-25	☐
	5	Colourdriver XP data sheet, 2008-07-30	☐
	6	US-TECH ONLINE, Dialight: New High Power LED Driver, downloaded from http://www.us-tech.com, October 2007	☐
	7	IST LTD., iDrive™ 1000 The Intelligent 210W LED Driver User Manual, v. 1.7, 2008-06-20	☐
	8	ROAL ELECTRONICS, S.P.A, Programmable RGB LED Driver 200 Watts Model RHPS180 Product Details, Rev. 2, 2007-10	☐
	9	INTERNATIONAL SEARCHING AUTHORITY (CA), International Search Report and Written Opinion for International Patent Application No. PCT/CA2009/001295, 2010-01-13	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	
	First Named Inventor	TIKKANEN, David, ET AL.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

EXAMINER SIGNATURE			
Examiner Signature	/Jason Crawford/ (04/17/2013)	Date Considered	

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Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2011-02-16
Name/Print	Jeffrey W. Wong	Registration Number	46414

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Issue Classification	Application/Control No. 13059336	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.
	Examiner JASON M CRAWFORD	Art Unit 2819

CPC				
Symbol			Type	Version
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CPC Combination Sets							
Symbol			Type	Set	Ranking	Version
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		/				

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION					
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED
315	312	H	0	5	B	37 / 00 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
315	291				

NONE (Assistant Examiner) (Date)	Total Claims Allowed: 21	
/JASON M CRAWFORD/ Primary Examiner.Art Unit 2819 04/18/2013 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 8

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13059336	TIKKANEN ET AL.
	Examiner	**Art Unit**
	JASON M CRAWFORD	2819

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	21	
/JASON M CRAWFORD/ Primary Examiner.Art Unit 2819	04/18/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	**Art Unit**
	JASON M CRAWFORD	2819

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	20	17												
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6	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	21	
/JASON M CRAWFORD/ Primary Examiner.Art Unit 2819	04/18/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13059336	TIKKANEN ET AL.
	Examiner	Art Unit
	JASON M CRAWFORD	2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/07/2013	04/18/2013							
1	1	✓	=							
-	2	O	-							
2	3	✓	=							
16	4	✓	=							
-	5	✓	-							
1	6	✓	=							
4	7	✓	=							
7	8	✓	=							
8	9	✓	=							
9	10	✓	=							
10	11	✓	=							
11	12	✓	=							
5	13	✓	=							
12	14	O	=							
13	15	✓	=							
6	16	O	=							
20	17	O	=							
17	18	O	=							
18	19	✓	=							
19	20	✓	=							
14	21		=							
15	22		=							
21	23		=							

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	TIKKANEN, David; NEUDORF, Jason; LYONS, Steven; SCOTT, Todd, William; HATHAWAY, Kyle, Grahame; JANSEN, David, Wainesworth
Serial No.:	13/059,336
Filed:	September 17, 2009
Title:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
Group:	2819
Examiner:	CRAWFORD, Jason
Attorney Ref.:	PAT 67545W-2 US

April 12, 2013

Mail Stop Amendment
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria VA 22314-1450
USA

AMENDMENT

In response to the Office Action of January 23, 2013, please amend the above-identified-application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Amendments to the Drawings begin on page 6 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks/Arguments begin on page 7 of this paper.

An **Appendix** including amended drawing figures is attached following page 8 of this paper.

Amendments to the Specification

Please replace paragraph **[0009]** with the following amended paragraph:

[0009] In another aspect of the present disclosure, there is provided a ~~configurable~~ power circuit ~~source~~ that can provide[[s]] a plurality of output channels, such as 6, 8, 9, or 12, to color change or dim OLED or LED loads. In color changing applications, the number of available channels is a multiple of three or four to accommodate either red/green/blue LED loads or red/green/blue/amber or white LED loads. The number of output channels and available output power is increased or maximized based on the LED current requirements. The output channels are programmable by means of in circuit serial programming (ICSP) ports and calibrated by a secondary digital controller to the required output current and other parameters such as dimming frequency range.

Please replace paragraph **[0070]** with the following amended paragraph:

[0070] Figure 8 is a schematic diagram of an alternate embodiment of a configurable LED dimmer 10. As shown, individual current sources 114 and current senses 116 are mounted in the light fixture containing the LED load 56, and power and data signals are provided to each output current source 114 by the multi conductor cable 22. In this embodiment, the current sources 114 are configured to regulate to a predetermined peak current. The load controller 110 ~~64~~ transmits the data signal containing the output current information encoded within the three variables of on time, off time, and period whereby no three variables are held constant.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads comprising:

a power circuit including:

an inrush current limit;

a DC/DC converter;

a power factor correction (PFC) boost connected to the inrush current limit and the DC/DC converter;

a regulated output voltage bus connected to the DC/DC converter; and

at least one power limit connected to the output voltage bus;

a primary ~~digital~~ controller for controlling the power circuit;

a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load;

a secondary ~~digital~~ controller for controlling the set of output current drivers;

wherein the secondary controller transmits LED control information to control outputs of the set of output current drivers~~; and~~

~~wherein the secondary digital controller provides digital feedback control information to the primary digital controller~~.

2. (Cancelled)

3. (Currently Amended) The LED driver/dimmer of Claim 1 further comprising:

a set of in-circuit serial programming (ICSP) ports, each of the set of ICSP ports associated with one of the set of output current drivers for ~~dynamic control of the~~ configuration of output current drivers.

4. (Currently Amended) The LED driver/dimmer of Claim [[1]]22 further comprising an in-circuit serial programming (ICSP) port connected to the ~~primary~~ digital controllers.

5. (Cancelled)

6. (Currently Amended) The LED driver/dimmer of Claim 1 further comprising a communication interface for receiving data from an external transmitter and for transmitting the data to the secondary ~~digital~~ controller.

7. (Currently Amended) The LED driver/dimmer of Claim [[1]]6 further including an isolation barrier for separating the secondary ~~digital~~ controller and the communication interface.

8. (Original) The LED driver/dimmer of Claim 1 further comprising a housing portion for housing the components of the driver.

9. (Original) The LED driver/dimmer of Claim 8 wherein the housing portion comprises:
an aluminum heatsink; and
a U-shaped chassis.

10. (Original) The LED driver/dimmer of Claim 9 wherein the heatsink comprises a plurality of fins.

11. (Original) The LED driver/dimmer of Claim 10 wherein heatsink acts to cool the driver/dimmer via convection cooling.

12. (Original) The LED driver/dimmer of Claim 9 further comprising a thermally conductive electrically isolated material for coupling the power circuit to the chassis to further improve heat dissipation. .

13. (Original) The LED driver/dimmer of Claim 6 wherein the communication interface is either DMX512A, 0-10Vdc analog control, Zigbee wireless or Remote Device Management (RDM) compatible.

14. (Currently Amended) The LED driver/dimmer of Claim [[2]]1 wherein the inrush current limit comprises:
a switch;
a relay coil, connected to the switch; and
a thermistor;

wherein the relay coil and the thermistor are in parallel with each other.

15. (Currently Amended) The LED driver/dimmer of Claim 1 wherein the light fixture load is one of an Organic LED (OLED) load or an LED load.

16. (Currently Amended) The LED driver/dimmer of Claim [[2]]6 comprising an auxiliary flyback converter to provide power to the primary ~~digital~~ controller, secondary ~~digital~~ controller, and communication interface

17. (Currently Amended) The LED driver/dimmer of Claim 22 wherein the primary digital controller can disable the PFC boost and DC/DC Converter at zero light intensity state.

18. (Currently Amended) The LED driver/dimmer of Claim 4[[5]] comprising a means to map output current drivers to various DMX512 addresses.

19. (Currently Amended) The LED driver/dimmer of Claim 4[[5]] comprising a means to map output current drivers to various dimming zones for 0-10 Vdc control.

20. (Currently Amended) The LED driver/dimmer of Claim 4[[5]] further comprising an isolated communication bus to transmit the digital feedback control into the primary controller~~PDC~~.

21. (New) The LED driver/dimmer of Claim 1 wherein the secondary controller provides feedback control information to the primary controller.

22. (New) The LED driver/dimmer of Claim 1 wherein the primary and secondary controllers are digital controllers.

23. (New) A power circuit for a configurable light-emitted diode (LED) driver, the power circuit comprising:

an inrush current limit;

a DC/DC converter;

a power factor correction (PFC) boost connected to the inrush current limit and the DC/DC converter;

an output voltage bus connected to the DC/DC converter; and

at least one power limit connected to the output voltage bus.

Amendments to the Drawings

The attached sheet(s) of drawings includes changes to Figure 8. The sheet, which includes Figure 8, replaces the original sheet including Figure 8.

Attachment: Replacement sheet (1)

Remarks/Arguments

Claims 1, 3 to 4 and 6 to 23 are pending in the current application. Claims 1, 3, 4, 6, 7, 14, 15, 16 and 17 are amended, Claims 21 to 23 are new and Claims 2 and 5 cancelled.

Claim 1 has been amended to include the subject matter of original Claim 2 and to remove the phrase "wherein the secondary controller provides feedback control information to the primary controller" which is now added as new Claim 21. Claim 3 has been amended to replace the expression "dynamic control of the" with the expression "configuration of". Claims 4, 6, 7 and 16 have been amended to remove the word "digital". Claims 4, 14,16 and 17 have been amended to change their claim dependency. New independent Claim 23 is directed at the subject matter of original Claim 2.

The amendments to the specification and figures are to correct clear errors. No new subject matter has been added as a result of these amendments.

Claims 1, 6 to 8, 13 and 15 are rejected under 35 U.S.C. 102(a) as being anticipated by US Patent Publication No. 2008/0018261 to Kastner. Applicant has amended Claim 1 to include the subject matter of original Claim 2 which has been deemed patentable in the Office Action by the Examiner. It is respectfully submitted that independent Claim 1 and each of its independent claims are now patentable over the cited art. Retraction of Examiner's rejection of Claims 1, 6 to 8, 13 and 15 is respectfully requested.

Claims 3 to 5, 9 to 12 and 19 to 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kastner in view of US Patent Publication No. 2008/0025028 to Gloisten et al. Applicant respectfully submits that the Examiner's rejection is now moot in view of the amendments outlined above. Retraction of Examiner's rejection of Claims 3 to 5, 9 to 12 and 19 to 20 is respectfully requested.

For the above reasons, it is respectfully submitted that the application is now in condition for allowance, which is requested. If there are any outstanding issues, the Examiner is invited to contact the undersigned to discuss this matter further.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments, to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

Tikkanen, Dave, et al.

By: /Jeffrey W. Wong/
Jeffrey W. Wong
Registration No. 46,414
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100 Queen Street
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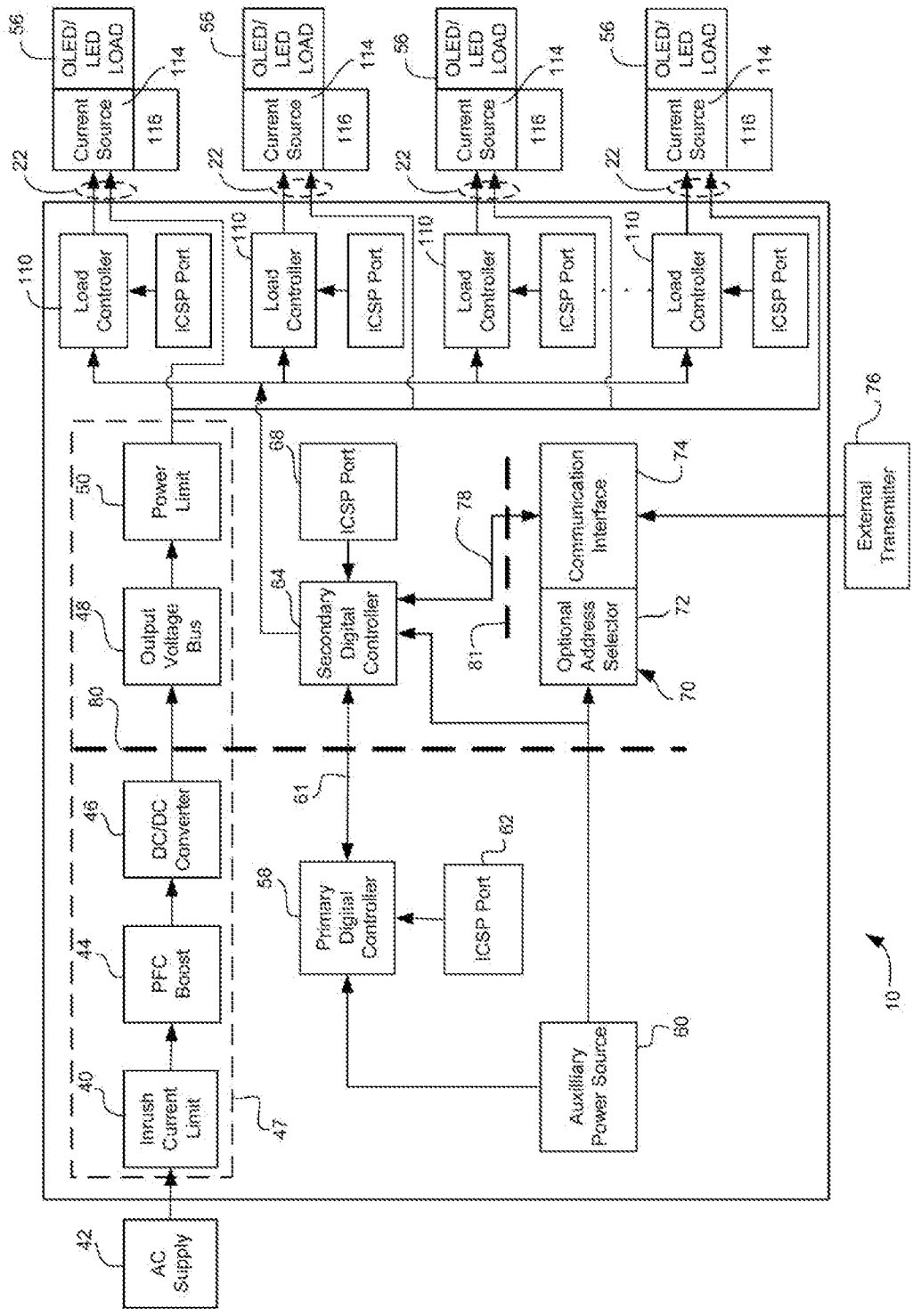

OLED/ LED LOAD
Current Source
116
114
56
22
110
Load Controller
ICSP Port
Power Limit
50
Output Voltage Bus
48
DC/DC Converter
46
PFC Boost
44
Inrush Current Limit
40
47
AC Supply
42
Secondary Digital Controller
64
Primary Digital Controller
58
61
ICSP Port
62
68
78
81
Communication Interface
74
Optional Address Selector
72
70
External Transmitter
76
Auxiliary Power Source
60
80
10

FIGURE 8

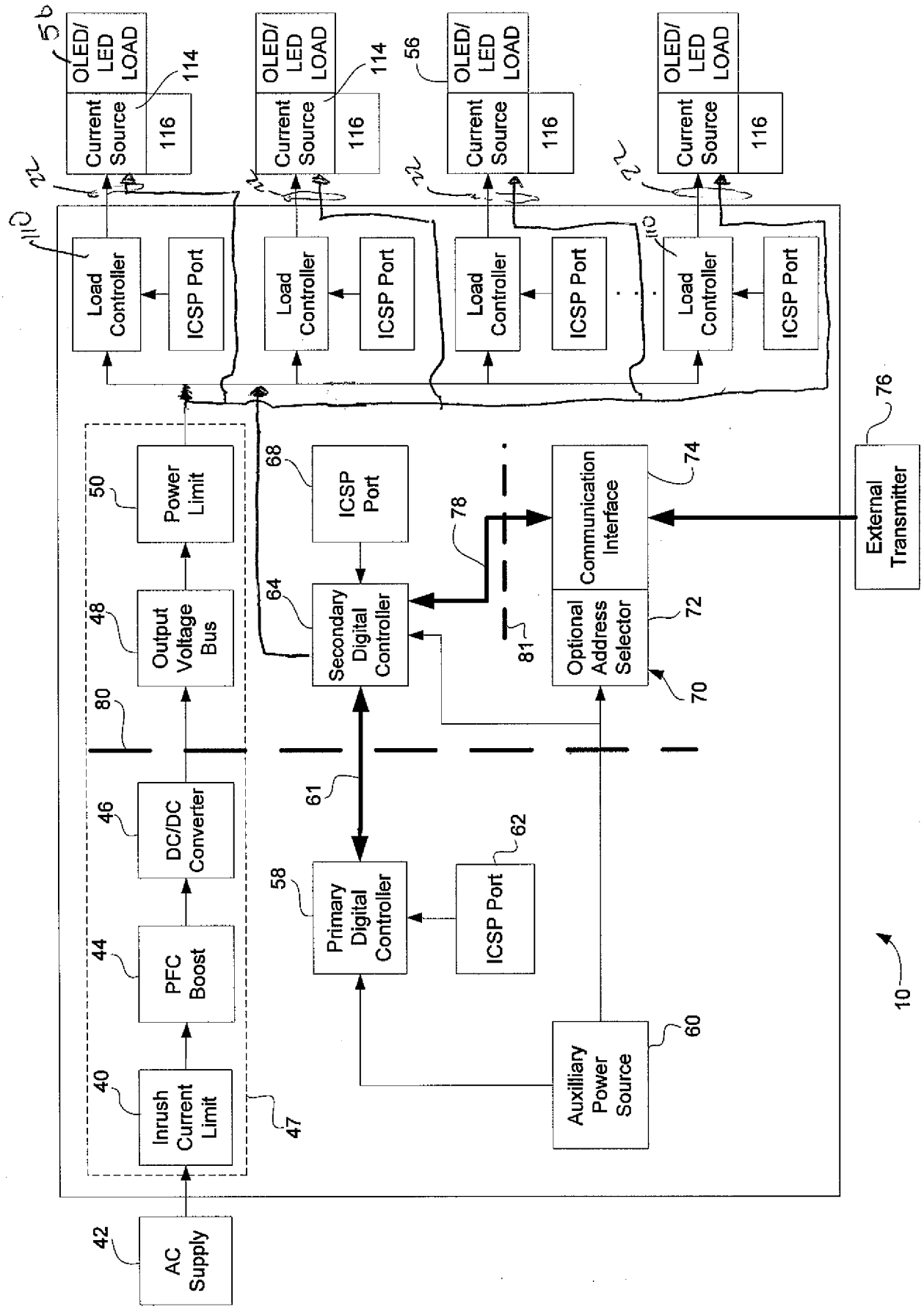


FIGURE 8

AMENDED MARKED-UP DRAWINGS

Electronic Acknowledgement Receipt

EFS ID:	15505218
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	26123
Filer:	Jeffrey Wong/Tara Charbonneau
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	12-APR-2013
Filing Date:	22-MAR-2011
Time Stamp:	14:58:58
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PAT67545W-2_Response.pdf	141679 bdcf2e9068a431278826c21e52d5739181b58395	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	2
	Claims	3	6
	Applicant Arguments/Remarks Made in an Amendment	7	9

Warnings:					
Information:					
2	Drawings-only black and white line drawings	PAT67545W-2_Replacement_Sheet_Fig8.pdf	433037 9560565d64200ec11dd98947815fc308903b59b5	no	1
Warnings:					
Information:					
3	Drawings-only black and white line drawings	PAT67545W-2_Marked-Up_Fig8.pdf	23742 3034a2ee60ba14f63d8e69cdbe08e47ff17087dd	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	598458		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
13/059,336	03/22/2011	

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **04/12/2013**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 21	Minus	** 20	= 1	X $80 =	80
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**80**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LASHAWN MARKS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/059,336	03/22/2011	David Tikkanen	PAT 67545W-2	9207

26123 7590 01/23/2013

BORDEN LADNER GERVAIS LLP
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OTTAWA, ON K1P 1J9
CANADA

EXAMINER	
CRAWFORD, JASON	
ART UNIT	**PAPER NUMBER**
2819	

NOTIFICATION DATE	DELIVERY MODE
01/23/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipinfo@blg.com

Office Action Summary	Application No.	Applicant(s)	
	13/059,336	TIKKANEN ET AL.	
	Examiner	Art Unit	
	Jason M. Crawford	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,3-13,15,19 and 20* is/are rejected.

8)☒ Claim(s) *2,14 and 16-18* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/16/11,8/31/12,10/2/12*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

1. Claims 1, 6-8, 13 and 15 are rejected under 35 U.S.C. 102(a) as being anticipated by Kastner (US 2008/0018261).

In regards to claim 1, Kastner discloses of a configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads (see Fig 20D) comprising: a power circuit (Figs 20A-B); a primary digital controller (U1, Fig 20B) for controlling the power circuit; a set of output current drivers (in Fig 20D), each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load (see Fig 20D); a secondary digital controller (U4, Fig 20C) for controlling the set of output current drivers (Fig 20D); wherein the secondary controller (U4, Fig 20C) transmits LED control information to control outputs of the set of output current drivers (Fig 20D); and wherein the secondary digital controller (Fig 20C) provides digital feedback (VFB) control information to the primary digital controller (U1, see Figs 20, 20A-D).

In regards to claim 6, Kastner discloses of the LED driver/dimmer of Claim 1 further comprising a communication interface for receiving data from an external

transmitter (see Paragraph 0105) and for transmitting the data to the secondary digital controller (U4).

In regards to claim 7, Kastner discloses of the LED driver/dimmer of Claim 1 further including an isolation barrier for separating the secondary digital controller (U4) and the communication interface (see Fig 20C and Paragraph 0105).

In regards to claim 8, Kastner discloses of the LED driver/dimmer of Claim 1 further comprising a housing portion for housing the components of the driver (see Fig 20, 20A-D,. parts of an IC which is housed).

In regards to claim 13, Kastner discloses of the LED driver/dimmer of Claim 6 wherein the communication interface is either DMX512A, 0-10Vdc analog control, Zigbee wireless or Remote Device Management (RDM) compatible (see Paragraph 0105 and Claim 7, dimming function controlled from a dimming circuit remotely located from the driver).

In regards to claim 15, Kastner discloses of the LED driver/dimmer of Claim 1 wherein the light fixture load is one of an Organic LED (OLED) load or an LED load (LED, see Fig 20D).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3-5, 9-12 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kastner (US 2008/0018261) in view of Gloisten et al. (US 2008/0025028).

In regards to claims 3-5, Kastner discloses of the LED driver/dimmer of Claim 1 as found within the explanation above.

However, Kastner does not disclose of the LED driver/dimmer further comprising: a set of in-circuit serial programming (ICSP) ports, each of the set of ICSP ports associated with one of the set of output current drivers for dynamic control of the output current drivers, and the in-circuit serial programming (ICSP) port connected to the primary and secondary digital controllers.

Gloisten discloses of a configurable light emitting diode (LED) driver/dimmer) for controlling a set of light fixture loads (within 240) comprising a set of in-circuit serial programming (ICSP) ports (see Paragraph 0033) connected to and associated with digital controllers (275) and current drivers respectively, for control of the light fixture loads.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to utilize a set of in-circuit serial programming (ICSP) ports as taught by Gloisten for utilizing known standards for loading and programming of firmware to achieve the desired control characteristics.

In regards to claim 9, Kastner discloses of the LED driver/dimmer of Claim 8 as found within the explanation above.

However, Kastner does not disclose of wherein the housing portion comprises: an aluminum heatsink; and a U-shaped chassis.

Gloisten discloses of a configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads (within 240) comprising a set of in-circuit serial programming (ICSP) ports (see Paragraph 0033) connected to and associated with digital controllers (275) and current drivers respectively, for control of the light fixture loads, wherein the LED driver/dimmer comprises a housing (280), such that the housing portion comprises an aluminum heatsink (see Paragraph 0027).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have an aluminum heatsink housing as taught by Gloisten for utilizing the properties of aluminum for the proper amount of heat exchange to achieve optimum temperature reduction.

Furthermore, at the time of the invention, it would readily apparent and obvious to one having ordinary skill in the that the shape of the chassis is an obvious matter of design choice to accommodate a desired shape or the presented shape of the device.

In regards to claim 10, Kastner in view of Gloisten disclose of the LED driver/dimmer of Claim 9 wherein the heatsink comprises a plurality of fins (see Gloisten 140, 200B, 200 and 280 of Figs 1-2, 2C and 3 respectively).

In regards to claim 11, Kastner in view of Gloisten disclose of the LED driver/dimmer of Claim 10 wherein heatsink (140, 200B, 200, 280 of Gloisten) acts to cool the driver/dimmer via convection cooling (see Paragraphs 0003 and 0023-0028 of Gloisten).

In regards to claim 12, Kastner in view of Gloisten disclose of the LED driver/dimmer of Claim 9 further comprising a thermally conductive electrically isolated material (160, 250 of Gloisten) for coupling the power circuit (150) to the chassis (140, 280) to further improve heat dissipation (see Gloisten Paragraph 0003).

In regards to claim 19, Kastner in view of Gloisten disclose of the LED driver/dimmer of Claim 5 comprising a means to map output current drivers (Fig 20D of Kastner) to various dimming zones for 0-10 Vdc control (see Kastner Figs 20, 20A-D, 0 Vdc for shut off of load).

In regards to claim 20, Kastner in view of Gloisten disclose of the LED driver/dimmer of Claim 5 further comprising an isolated communication bus to transmit the digital feedback control (VFB of Kastner) into the PDC (U1, see Kastner Figs 20B-C).

Allowable Subject Matter

3. Claims 2, 14 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to claim 2, the prior art discloses of the claimed subject matter with the exception of the LED driver/dimmer of Claim 1 further comprising *wherein the power circuit comprises: an inrush current limit; a power factor conversion (PFC) boost; a*

DC/DC converter; an output voltage bus; and at least one power limit, nor would it have been obvious to one of ordinary skill in the art to do so. Claims 14 and 16-17 are also objected to as being dependent on claim 2.

In regards to claim 18, the prior art does not disclose of the LED driver/dimmer of Claim 5 further comprising *means to map output current drivers to various DMX512 addresses*, nor would it have been obvious to one of ordinary skill in the art to do so.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Crawford whose telephone number is (571)272-6004. The examiner can normally be reached on Mon-Fri 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shawki Ismail can be reached on (571) 272-3985. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M. Crawford/
Primary Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 13/059,336	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.	
	Examiner Jason M. Crawford	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0018261	01-2008	Kastner, Mark Allen	315/192
*	B	US-2008/0025028	01-2008	Gloisten et al.	362/294
*	C	US-2002/0047642	04-2002	Miyagawa, Shozo	315/307
*	D	US-2010/0164403	07-2010	Liu, Da	315/297
*	E	US-2005/0218838	10-2005	Lys, Ihor A.	315/291
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13059336	TIKKANEN ET AL.
	Examiner	**Art Unit**
	JASON M CRAWFORD	2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/07/2013								
	1	✓								
	2	O								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	O								
	15	✓								
	16	O								
	17	O								
	18	O								
	19	✓								
	20	✓								

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13059336
Filing Date	2011-02-16
First Named Inventor	David TIKKANEN
Art Unit	2821
Examiner Name	
Attorney Docket Number	PAT 67545W-2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/JC/	1	5420780		1995-05-30	Bernstein et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/JC/	1	20020047642		2002-04-25	ROHM CO., LTD.	Figs. 6, 7
	2	20080018261		2008-01-24	Kastner	Fig. 20; Para. 102
	3	20090179594		2009-07-16	Yang	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/JC/	1	2009039112	WO		2009-03-26	EXCLARA, INC.	Figs. 1, 10	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/

Receipt date: 10/02/2012	Application Number	13059336 13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2011-02-16
	First Named Inventor	David TIKKANEN
	Art Unit	2821
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/JC/	1	UKIPO (Examiner HUNT), SEARCH AND EXAMINATION REPORT UNDER SECTIONS 17 & 18(3), Patent Application No. GB1102782.8, 2012-09-06	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Jason Crawford/ (01/02/2013)	Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/

Receipt date: 10/02/2012	Application Number	13059336 13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2011-02-16
	First Named Inventor	David TIKKANEN
	Art Unit	2821
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2012-10-02
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"20110204820".did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/02 14:09
S2	7	("20050218838" | "20050289279" | "20020047642" | "20080018261" | "20080018261" | "8197079" | "20090179594" | "5420780").PN.	US-PGPUB; USPAT	OR	ON	2013/01/02 14:09
S3	6	S2 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/02 14:09
S4	1	S2 not S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/02 14:14
S5	7	("20050218838" | "20050289279" | "20020047642" | "20080018261" | "20080018261" | "8197079" | "20090179594" | "5420780").PN.	US-PGPUB; USPAT	OR	ON	2013/01/03 11:00
S6	0	(11/796940).APP.	USPAT; USOCR	OR	ON	2013/01/03 11:04
S7	10086	(primary and secondary) adj2 control$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:04
S8	82	S7 and @ad<"20080918" and "315"/$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:04
S9	34	S8 and (LED (light adj emit$4 adj diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/01/03 11:05

JC

			DERWENT; IBM_TDB			
S10	7968	315/247,291,294,297,302,307,312.ccls. and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:09
S11	20	((primary and secondary) adj2 control$4) and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:09
S12	6	S11 and (PFC (power adj factor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:09
S13	0	S12 and ICSP	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:10
S14	1	S12 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:10
S15	0	S5 and S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:10
S16	0	S5 and ICSP	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:10
S17	1	((primary and secondary) adj2 control$4) and 361/709.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:13
S18	76	((primary and secondary) adj2 control$4) and ("315"/$,ccls. "361"/$.ccls.) and @ad<"20080918"	US-PGPUB; USPAT; USOCR;	OR	ON	2013/01/03 11:13

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S19	1	(11/079928).APP.	USPAT; USOCR	OR	ON	2013/01/03 11:15
S20	160	("20020038157" | "20020044066" | "20020048169" | "20020070688" | "20020074559" | "20020078221" | "20020106540" | "20020130627" | "20020145394" | "20020145869" | "20020152045" | "20020154525" | "20020158583" | "20020176259" | "20030011538" | "20030028260" | "20030057884" | "20030057887" | "20030076281" | "20030085749" | "20030100837" | "20030133292" | "20030169014" | "20030222587" | "20030222603" | "20040036006" | "20040052076" | "20040090191" | "20040090787" | "20040095185" | "20040105261" | "20040113568" | "20040116039" | "20040130909" | "20040145320" | "20040178751" | "20040212320" | "20040212321" | "20040212993" | "20050029527" | "20050099824" | "20050116667" | "20050122065" | "20050151489" | "20050156583" | "20050213352" | "20050213353" | "20050218838" | "20050218870" | "20050219872" | "20050231133" | "20050236029" | "20050236998" | "20050253533" | "20050275626" | "20050276053" | "20060002110" | "20060087298" | "4536631" | "5640061" | "5786992" | "6016038" | "6091614" | "6150774" | "6166496" | "6211626" | "6285139" | "6292901" | "6304464" | "6340868" | "6369525" | "6441558" | "6459919" | "6495964" | "6510995" | "6528954" | "6548967" | "6577080" | "6586890" | "6608453" | "6618031" | "6624597" | "6639198" | "6667583" | "6717376" | "6720745" | "6734639" | "6768047" | "6774584" | "6777891" | "6781329" | "6788011" | "6801003" | "6806659" | "6807202" | "6836081" | "6853150" | "6869204" | "6883929" | "6888322" | "6888383" | "6888529" | "6897624" | "6930452" | "6930893").PN. OR ("6936978" | "6943504" | "6965205" | "6967448" | "6969954" | "6975079" | "7009348" | "7015654" | "7030572").PN. OR ("7233115").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/01/03 11:15
S21	0	(09/968775).APP.	USPAT; USOCR	OR	ON	2013/01/03 11:16
S22	12	("20050024877" | "7141941" | "20050105311" | "4492899" | "20060001381" | "7276861" | "5661645" | "7489086" | "3176204" | "6507159" | "6274987" | "7129652").PN.	US-PGPUB; USPAT	OR	ON	2013/01/03 11:17

S23	1215	(inrush (in adj rush)) and (PFC (power adj factor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:18
S24	2	S23 and ICSP	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:18
S25	7	("20050218838" | "20050289279" | "20020047642" | "20080018261" | "20080018261" | "8197079" | "20090179594" | "5420780").PN.	US-PGPUB; USPAT	OR	ON	2013/01/03 11:20
S26	0	S25 not S5	US-PGPUB; USPAT	OR	ON	2013/01/03 11:21
S27	6	"315"/$.ccls. and ICSP	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:28
S28	7	"315"/$.ccls. and (ICSP (in adj circuit adj serial adj program$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:29
S29	12	("315"/$.ccls. "361"/$.ccls.) and (ICSP (in adj circuit adj serial adj program$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:29
S30	2	S29 and (PFC (power adj factor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:29
S31	10	S29 not S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:29
S32	6	S31 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/01/03 11:30

			IBM_TDB			
S33	4	S31 not S32	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:30
S34	0	S33 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 11:31
S35	5	(PFC (power adj factor)) and (ICSP (in adj circuit adj serial adj program$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 12:59
S36	3	S35 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 12:59
S37	0	S36 and (heatsink$3 (heat adj sink$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 12:59
S38	2598	(PFC (power adj factor)) and (heatsink$3 (heat adj sink$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:00
S39	1637	S38 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:00
S40	229	("315"/$.ccls. "361"/$.ccls.) and S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:00
S41	30	S40 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2013/01/03 13:00

			EPO; JPO; DERWENT; IBM_TDB			
S42	13	S41 and (LED (light adj emit$4 adj diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:00
S43	6	S42 and (DC adj DC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:00
S44	9	("20070267978" | "20090322234" | "20100164403").PN. OR ("7880400").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/01/03 13:04
S45	1	(12/317977).APP.	USPAT; USOCR	OR	ON	2013/01/03 13:07
S46	11	("20080088346" | "20080116818" | "20080203946" | "20090322234" | "6369525" | "6847169" | "7116086" | "7408308" | "7710049" | "7804256").PN. OR ("8044609").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/01/03 13:07
S47	0	S44 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:08
S48	1	(PFC (power adj factor)) and S44	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:08
S49	77755	14and (DC adj DC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:08
S50	1	S48 and (DC adj DC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:08
S51	10	S46 not S44	US-PGPUB; USPAT; USOCR	OR	ON	2013/01/03 13:08
S52	0	S51 and (inrush (in adj rush))	US-PGPUB; USPAT;	OR	ON	2013/01/03 13:10

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S53	3	(PFC (power adj factor)) and S51	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:10
S54	790	(u adj shap$3) with (heatsink$3 (heat adj sink$3)) and fins	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:25
S55	384	("315"/$.ccls. "361"/$.ccls.) and S54	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:25
S56	2	S55 and (ICSP (in adj circuit adj serial adj program$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:25
S57	327	S55 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:26
S58	0	S57 and (serial adj programm$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:26
S59	0	S57 and (serial adj program$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:26
S60	0	S57 and (serial$2 adj2 program$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:26

S61	0	S57 and (serial$2 adj2 port)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:26
S62	4	(PFC (power adj factor)) and S57	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:26
S63	34	((u adj shap$3) with (heatsink$3 (heat adj sink$3) fins)) and (LED adj2 control$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:29
S64	22	S63 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:29
S65	6	("315"/$.ccls. "361"/$.ccls.) and (ICSP (in adj circuit adj serial adj program$4)) and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:37
S66	6	S65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:41
S67	445	(ICSP (in adj circuit adj serial adj program$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:43
S68	277	S67 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:43
S69	103	S68 and (light$3 illuminat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/01/03 13:43

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			DERWENT; IBM_TDB			
S70	8	S69 and (heatsink$3 (heat adj sink$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:44
S71	401	("315"/$.ccls. "361"/$.ccls.) and zigbee	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:54
S72	135	S71 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:54
S73	0	(ICSP (in adj circuit adj serial adj program$4)) and S72	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:54
S74	49	("315"/$.ccls. "361"/$.ccls.) and RDM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:55
S75	2	(ICSP (in adj circuit adj serial adj program$4)) and S74	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:55
S76	0	S75 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:55
S77	23	(ICSP (in adj circuit adj serial adj program$4)) and (DMX512 RDM zigbee)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 13:56
S78	10	S77 and @ad<"20080918"	US-PGPUB; USPAT; USOCR;	OR	ON	2013/01/03 13:56

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S79	201	((inrush (in adj rush)) adj2 limit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 14:07
S80	152	S79 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 14:07
S81	29	(PFC (power adj factor)) and S80	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 14:07
S82	12	S81 and (heatsink$3 (heat adj sink$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 14:08
S83	0	(ICSP (in adj circuit adj serial adj program$4)) and S82	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 14:08
S84	2	S82 and (thermistor and coil)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 14:08
S85	10	S82 not S84	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/03 14:10
S86	418957	"4" and (heatsink$3 (heat adj sink$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/04 07:40

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S87	7	(ICSP (in adj circuit adj serial adj program$4)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2013/01/04 07:33
S88	4	S87 and @ad<"20080918"	US-PGPUB; USPAT; UPAD	OR	ON	2013/01/04 07:39
S89	2	S88 and (light$3 illuminat$3)	US-PGPUB; USPAT; UPAD	OR	ON	2013/01/04 07:39
S90	2	(ICSP (in adj circuit adj serial adj program$4)) and S89	US-PGPUB; USPAT; UPAD	OR	ON	2013/01/04 07:40
S91	0	S90 and (heatsink$3 (heat adj sink$3) fins)	US-PGPUB; USPAT; UPAD	OR	ON	2013/01/04 07:40
S92	0	(PFC (power adj factor)) and S90	US-PGPUB; USPAT; UPAD	OR	ON	2013/01/04 07:40

1/7/2013 10:54:42 AM
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CONFIRMATION NO. 9207

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/059,336	03/22/2011	315	2819	PAT 67545W-2

APPLICANTS

David Tikkanen, Waterloo, CANADA;
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Todd William Scott, Waterloo, ON, CANADA;
Kyle Grahame Hathaway, Kitchener, ON, CANADA;
David Wainesworth Jansen, Waterloo, ON, CANADA;

**** CONTINUING DATA ***************************

This application is a 371 of PCT/CA09/01295 09/17/2009 JC
which claims benefit of 61/097,963 09/18/2008 JC

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

04/14/2011

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /JASON CRAWFORD/ Examiner's Signature	☐ Met after Allowance JC Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CANADA	12	20	1

ADDRESS

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OTTAWA, ON K1P 1J9
CANADA

TITLE

CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

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Receipt date: 02/16/2011
Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

13059336 - GAU: 2819
PTO/SB/08a (01-10)
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Application Number	
Filing Date	
First Named Inventor	TIKKANEN, David, ET AL.
Art Unit	
Examiner Name	
Attorney Docket Number	PAT 67545W-2

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/JC/	1	20050289279		2005-12-29	FAILS ET AL.	
	2	20050218838		2005-10-06	LYS	
	3	20080018261		2008-01-24	KASTNER	

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/JC/	1	2008052293	WO		2008-05-08	QUICK ET AL.		☐

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Receipt date: 02/16/2011	Application Number	13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	
	First Named Inventor	TIKKANEN, David, ET AL.
	Art Unit	
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/JC/	1	ERICSSON AB, Power Supplies Goes Digital White Paper, October 2006	☐
	2	SKANDA; MICROCHIP TECHNOLOGY INC., Power Factor Correction in Power Conversion Applications using the dsPIC® DSC", AN1106, June 2007	☐
	3	TRAXON TECHNOLOGIES, LED Engine XB 3W-108 Technical Specifications and User Manual Version 1.1, 2007	☐
	4	PENWELL CORPORATION, Dialight Lumidrives Launches Colurdriver XP for High-Power LEDs, LEDs MAGAZINE, downloaded from http://www.ledsmagazine.com/press/15469, 2007-09-25	☐
	5	Colourdriver XP data sheet, 2008-07-30	☐
	6	US-TECH ONLINE, Dialight: New High Power LED Driver, downloaded from http://www.us-tech.com, October 2007	☐
	7	IST LTD., iDrive™ 1000 The Intelligent 210W LED Driver User Manual, v. 1.7, 2008-06-20	☐
	8	ROAL ELECTRONICS, S.P.A, Programmable RGB LED Driver 200 Watts Model RHPS180 Product Details, Rev. 2, 2007-10	☐
	9	INTERNATIONAL SEARCHING AUTHORITY (CA), International Search Report and Written Opinion for International Patent Application No. PCT/CA2009/001295, 2010-01-13	☐

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Receipt date: 02/16/2011	Application Number	13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	
	First Named Inventor	TIKKANEN, David, ET AL.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

EXAMINER SIGNATURE			
Examiner Signature	/Jason Crawford/ (01/02/2013)	Date Considered	

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Receipt date: 02/16/2011	Application Number	13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	
	First Named Inventor	TIKKANEN, David, ET AL.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2011-02-16
Name/Print	Jeffrey W. Wong	Registration Number	46414

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Receipt date: 08/31/2012

13059336 - GAU: 2819

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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(Not for submission under 37 CFR 1.99)

Application Number	13059336
Filing Date	2011-02-16
First Named Inventor	TIKKANEN, David
Art Unit	2821
Examiner Name	
Attorney Docket Number	PAT 67545W-2

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Receipt date: 08/31/2012	Application Number	13059336 13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2011-02-16
	First Named Inventor	TIKKANEN, David
	Art Unit	2821
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

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Receipt date: 08/31/2012	Application Number	13059336	13059336 - GAU: 2819
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2011-02-16	
	First Named Inventor	TIKKANEN, David	
	Art Unit	2821	
	Examiner Name		
	Attorney Docket Number	PAT 67545W-2	

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☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2012-08-31
Name/Print	Jeffrey W. Wong	Registration Number	46414

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13059336	TIKKANEN ET AL.
	Examiner	Art Unit
	JASON M CRAWFORD	2819

SEARCHED			
Class	Subclass	Date	Examiner
315	247,291,294,297,302,307,312	1/7/2013	JC

SEARCH NOTES		
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See attached search	1/7/2013	JC

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Art Unit	2821
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	2	20080018261		2008-01-24	Kastner	Fig. 20; Para. 102
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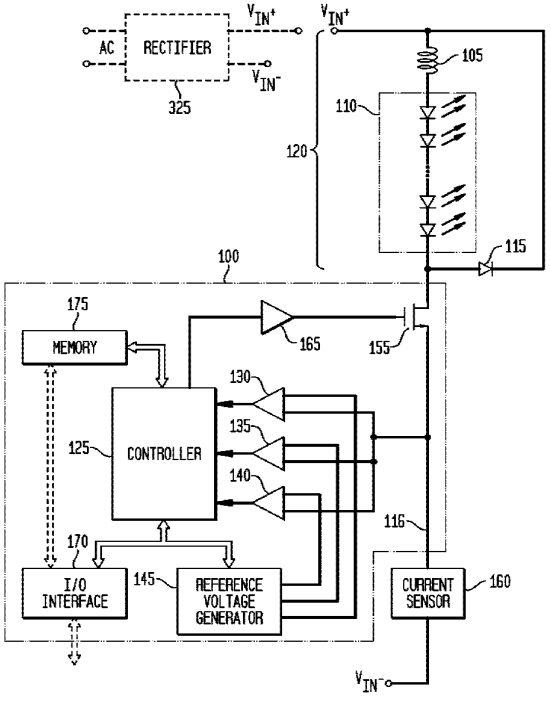
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(54) Title: DIGITAL DRIVER APPARATUS, METHOD AND SYSTEM FOR SOLID STATE LIGHTING

FIG. 1



(57) Abstract: An apparatus, method and system are provided for controlling the solid state lighting, such as LEDs An exemplary apparatus comprises a switch for switching electrical current through the LEDs, a current sensor, a first comparator adapted to determine a switch current first predetermined threshold, a second comparator determining the switch current reached an average level, controller adapted to turn the switch into on/off states, determine a first on time period as a duration between either second predetermined threshold detection or the turning the switch into the on state, and the detection of the predetermined average current level, determine a second on time period as a duration between predetermined average current level and first predetermined threshold detection, determine an on time switch penod as proportional to first and second on time periods Additionally, utilize a difference between first and second on time periods to generate an error signal.

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GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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DIGITAL DRIVER APPARATUS, METHOD AND SYSTEM FOR SOLID STATE LIGHTING

FIELD OF THE INVENTION

The present invention in general is related to supplying and controlling power to solid state lighting devices, and more particularly, to digitally controlling the current of solid state lighting devices such as light emitting diodes utilized in lighting and other applications.

BACKGROUND OF THE INVENTION

Arrays of light emitting diodes ("LEDs") are utilized for a wide variety of applications, including for general lighting and multicolored lighting. Because emitted light intensity is proportional to the average current through an LED (or through a plurality of LEDs connected in series), adjusting the average current through the LED(s) is one typical method of regulating the intensity or the color of the illumination source. Solid state lighting, such as LEDs, are typically coupled to a converter as a power source.

A step-down (Buck) converter can be controlled either in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). Typically DCM is suitable only for low power processing, while CCM mode is utilized for higher power conversion, such as for high brightness LEDs.

In the prior art, a technique referred to as "current programming mode" ("CPM") is utilized in an attempt to simplify compensator designs for the Buck converter, *see, e.g.*, U.S. Patent Nos. 6,034,517; 4,975,820; 4,672,518; 4,674,020; and 4,717,994. Prior art circuits for this CPM mode typically regulate the inductor current in CCM mode around a set point within the Buck converter. This set point is further manipulated by an outer compensating loop. For a Buck converter implemented with CPM mode, the outer compensating loop can be a single pole network.

A CPM implementation, however, cannot simply utilize a controller for a Buck converter, but must also be accompanied with a circuit implementing DCM. One challenge facing this CCM implementation is that the control system needs to transition between DCM and CCM modes in both directions. Many prior art control

systems will oscillate around these two modes, which causes LED current to fluctuate, and which may be visually apparent as flicker, for example. When the outer compensator bandwidth may be low, another problem with this CCM technique is that the LED current may also fluctuate, particularly when the input voltage to the Buck converter contains a high ripple percentage.

Most prior art LED control systems also utilize a "high side sensing" technique, in which the output current of a Buck converter is sensed by a sensing resistor in series with the inductor (see, e.g., U.S. Patent Nos. 6,853,174; 6,166,528; and 5,600,234). With high side sensing, output current can be regulated accurately, and high side sensing can also be utilized with CPM techniques. In order to overcome the various stability problems and other disadvantages mentioned above, the prior art has utilized various controllers to implement hysteretic (or so called "bang-bang") control to regulate this inductor current.

The high side sensing technique works well when the controller integrated circuit ("IC") can tolerate the Buck converter input voltage range. This is typically not the case for an LED driver, however, which involves input voltages which are much higher than what a controller IC is capable of tolerating or specified to tolerate and, accordingly, such a high side sensing technique cannot be utilized with typical controller ICs.

Various techniques for "low side sensing" are also found in the prior art, in which the sense resistor is in between the main converter switching element (MOSFET) and ground, *see, e.g.*, U.S. Patent Nos. 6,580,258 and 5,912,552. The low side sensing technique is usually associated with a control method called "constant off time" (U.S. Patent Nos. 6,580,258 and 5,912,552). Detailed analysis of this constant off time method shows that while it may be suitable for controlling Buck converter output voltage, it exhibits a very large error if it is used for controlling output current, due to converter component and environmental variations (*e.g.*, manufacturing variations, component aging or life span, and environmental conditions such as temperature).

A need remains, therefore, for a control method, apparatus and system, using low side sensing and suitable for IC implementation, that can regulate output current accurately while eliminating those drawbacks caused by existing techniques.

Such an apparatus, method and system should provide a simpler controller compared to CPM techniques, and further provide excellent accuracy and not exhibiting the problems associated with prior art techniques such as CPM technique. Such an apparatus, system and method should also control the intensity (brightness) of light emissions for solid state devices such as LEDs, while simultaneously providing for substantial stability of perceived color emission and control over wavelength shifting, over both a range of intensities and a range of LED junction temperatures. Such an apparatus, system and method should be capable of being implemented with few components, and without requiring extensive feedback systems.

SUMMARY OF THE INVENTION

The exemplary embodiments of the present invention provide numerous advantages for providing power to solid state lighting, such as light emitting diodes. The exemplary embodiments allow for energizing one or more LEDs, using digital control and low side sensing, enabling low voltage IC implementations. The exemplary apparatus and system embodiments may be implemented with either fixed or variable frequency switching, and may be implemented with either AC or DC power sources. As a digital implementation, the exemplary embodiments may also be implemented at a reduced cost. The exemplary embodiments also provide for precise current control, within any selected tolerance levels. In addition, the exemplary embodiments also eliminate the required RC filtering of the prior art.

Further advantages of the exemplary embodiments further provide for controlling the intensity of light emissions for solid state devices such as LEDs, while simultaneously providing for substantial stability of perceived color emission, over both a range of intensities and also over a range of LED junction temperatures. The exemplary embodiments provide digital control, without requiring external compensation. The exemplary embodiments do not utilize significant resistive impedances in the current path to the LEDs, resulting in appreciably lower power losses and increased efficiency. The exemplary current regulator embodiments also utilize comparatively fewer components, providing reduced cost and size, while simultaneously increasing efficiency and enabling longer battery life when used in portable devices, for example.

An exemplary embodiment provides a method of controlling solid state lighting, with the solid state lighting coupled to a switch providing an electrical current path, and the solid state lighting having an electrical current. The exemplary method comprises: turning the switch into an on state; detecting when the electrical current has reached a predetermined average current level; detecting when the electrical current has reached a first predetermined current threshold; determining a first on time period as a duration between detection of a second predetermined current level or turning the switch into the on state and the detection of the predetermined average current level; determining a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; and determining an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period. When the on time period has elapsed, the exemplary also provides for turning the switch into an off state. The exemplary method may also provide for detecting when the electrical current has reached the second predetermined current threshold.

The exemplary embodiments may operate in a fixed or variable frequency switching mode. For the fixed frequency switching, subsequent to turning the switch into the off state, when a fixed time period has elapsed from having turned the switch into the on state, the exemplary method again turns the switch into an on state and repeats the detection and determination steps. For this exemplary embodiment, the method also provides for generating an error signal as a difference between the second on time period and the first on time period, and adjusting the on time period proportionally to the error signal.

For variable frequency switching, when a current off time period has elapsed, the exemplary method provides for determining the current off time period of the switch as a function of the first on time period and the second on time period, and more particularly, determining the current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period. In an exemplary embodiment, the current off time period of the switch may be determined as:

$T_{OFF}(K+1) \approx \frac{2 \bullet T_{ON2}(K) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$, in which $T_{OFF}(K+1)$ is the current off time period, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period. In another exemplary embodiment, the current off time period of the switch may be determined as:

$T_{OFF}(K+1) \approx \frac{(T_{ON1}(K)_A + T_{ON2}(K)) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$, in which $T_{OFF}(K+1)$ is the current off time period, $T_{ON1}(K)_A$ is a previous first on time period determined using the detection of the second predetermined current level, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period. In another exemplary embodiment, the current off time period of the switch may be determined as a function of a current first on time period, a previous second on time period, and a previous off time period, or as a function of a current first on time period, a previous first on time period, a previous second on time period, and a previous off time period.

In another exemplary embodiment, the method includes adjusting the current off time period to provide that the first on time period is substantially equal to the second on time period. In addition, the exemplary method also provides for decreasing the current off time period proportionally to a driving gate rising edge time period, or decreasing the on time period proportionally to a driving gate falling edge time period and a comparator falling edge time period. In another variation, the exemplary method may include adjusting the second on time period proportionally to a driving gate falling edge time period, or decreasing the second on time period proportionally to a driving gate falling edge time period and a comparator falling edge time period.

The exemplary method also provides for determining a blanking time interval following turning the switch into the on state. During the blanking time interval, the exemplary method provides for ignoring the detection of the second predetermined current threshold, the detection of the predetermined average current level, or the detection of the first predetermined current threshold. The blanking time interval may be determined as proportional to a gate rising edge time period and a

transient current time period, or as proportional to a gate rising edge time period and detection of the predetermined average current level, for example.

In another exemplary embodiment, the exemplary method includes adjusting a brightness level of the solid state lighting by using at least two different and opposing electrical biasing techniques. In addition, the method of adjusting a brightness level of the solid state lighting may include using a hysteresis of at least two electrical current amplitude levels and at least two electrical current duty cycle ratios.

In an exemplary embodiment, the solid state lighting comprises at least one light emitting diode which has a comparatively high voltage node and a comparatively low voltage node, and wherein the detection of the second predetermined current threshold, the detection of the predetermined average current level, and the detection of the first predetermined current threshold occur at the comparatively low voltage node.

In another exemplary embodiment, the solid state lighting comprises a plurality of arrays of a plurality of series-connected light emitting diodes, and each array of the plurality of arrays further coupled to a corresponding switch providing an electrical current path. The exemplary method may also include separately determining a corresponding first on time period, a corresponding second on time period, and a corresponding on time period as substantially proportional to the sum of the corresponding first on time period and the corresponding second on time period for each array of the plurality of arrays; when the corresponding on time period has elapsed, separately turning the corresponding switch into an off state; and separately determining a corresponding off time period for each array of the plurality of arrays. In addition, the exemplary method may also include interleaving the corresponding on time periods of the corresponding switches of the plurality of arrays, such as by successively switching electrical current to each array of the plurality of arrays for the corresponding on time period.

Another exemplary embodiment provides an apparatus for controlling solid state lighting, with the apparatus comprising: a switch couplable to the solid state lighting; a first comparator adapted to determine when a switch electrical current has reached a first predetermined current threshold; a second comparator adapted to determine when the switch electrical current has reached a predetermined average

current level; and a controller coupled to the first comparator and to the second comparator. In an exemplary embodiment, the controller is adapted to turn the switch into an on state and an off state, to determine a first on time period as a duration between either a detection of a second predetermined current threshold or the turning the switch into the on state, and the detection of the predetermined average current level; to determine a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; and to determine an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period. The controller is further adapted to perform the methodology discussed above.

In an exemplary embodiment, the apparatus also includes a gate driver circuit coupled between the controller and the switch, and wherein the controller is adapted to turn the switch on and to turn the switch off by generating a corresponding signal to the gate driver circuit. The exemplary apparatus may also include a third comparator adapted to determine when the electrical current has reached the second predetermined current threshold; a reference voltage generator adapted to provide reference voltages respectively corresponding to the first and second predetermined current thresholds and to the predetermined average current level; an input-output interface coupled to the controller and adapted to receive an input control signal; and a current sensor coupled to the first and second comparators and to the switch. An exemplary current sensor is embodied as a resistive circuit element.

When the solid state lighting comprises a plurality of arrays of a plurality of series-connected light emitting diodes, with each array of the plurality of arrays is further coupled to a corresponding switch, the controller is further adapted to turn each corresponding switch into an on state and an off state; to separately determine a corresponding first on time period, a corresponding second on time period, and a corresponding on time period as substantially proportional to the sum of the corresponding first on time period and the corresponding second on time period for each array of the plurality of arrays; when the corresponding on time period has elapsed, to separately turn the corresponding switch into an off state; to separately determine a corresponding off time period for each array of the plurality of arrays; and to interleave the corresponding on time periods of the corresponding switches of the

plurality of arrays, such as by successively turn into an on state each corresponding switch for each array of the plurality of arrays for the corresponding on time period.

The exemplary embodiments also provide a solid state lighting system, the system couplable to a power source, with the system comprising: a plurality of arrays of series-connected light emitting diodes; a plurality of switches, a corresponding switch of the plurality of switches coupled to each the array of the plurality of arrays of light emitting diodes; at least one corresponding first comparator adapted to determine when a corresponding switch electrical current has reached a corresponding first predetermined current threshold; at least one corresponding second comparator adapted to determine when the corresponding switch electrical current has reached a corresponding predetermined average current level; and at least one controller coupled to the corresponding first comparator and to the corresponding second comparator, the controller adapted to turn the corresponding switch into an on state and an off state, to determine a corresponding first on time period as a duration between either a detection of a corresponding second predetermined current threshold or the turning the corresponding switch into the on state, and the detection of the corresponding predetermined average current level; to determine a corresponding second on time period as a duration between the detection of the corresponding predetermined average current level and the detection of the corresponding first predetermined current threshold; and to determine a corresponding on time period of the corresponding switch as substantially proportional to a sum of the corresponding first on time period and the corresponding second on time period. The exemplary controller is also adapted to separately perform the methodology of the invention for each array, including the interleaving and the other features discussed above and below.

In addition, in the exemplary system, the exemplary apparatus may be coupled to a DC-DC power converter receiving a DC input voltage or coupled to AC-DC power converter receiving a rectified AC input voltage. When the power source provides a rectified AC input voltage, an electrical current through a corresponding switch is substantially zero when the rectified AC input voltage is below a selected or predetermined threshold. In addition, when the power source provides a rectified AC input voltage, the at least one controller is in an off state when the rectified AC input voltage is below a selected or predetermined threshold.

Another exemplary embodiment includes an apparatus for controlling solid state lighting, with the apparatus comprising: a switch couplable to the solid state lighting; a current sensor coupled to the switch; a first comparator adapted to determine when a switch electrical current has reached a first predetermined current threshold; a second comparator adapted to determine when the switch electrical current has reached a predetermined average current level; a third comparator adapted to determine when the switch electrical current has reached a second predetermined current threshold; a reference voltage generator coupled to the first, second and third comparators and adapted to provide reference voltages respectively corresponding to the first predetermined current threshold, the second predetermined current threshold; and to the predetermined average current level; an input-output interface adapted to receive an input control signal; and a controller coupled to the first, second and third comparators and to the input-output interface, the controller adapted to turn the switch into an on state and an off state, to determine a first on time period as a duration between either the detection of a second predetermined current threshold or the turning the switch into the on state, and the detection of the predetermined average current level; to determine a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; to determine an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period; to turn the switch into an off state when the on time period has elapsed; and to determine a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period.

Numerous other advantages and features of the present invention will become readily apparent from the following detailed description of the invention and the embodiments thereof, from the claims and from the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention will be more readily appreciated upon reference to the following disclosure when considered in conjunction with the accompanying drawings, wherein like reference numerals are used to identify identical components in the various views, and wherein reference numerals

with alphabetic characters are utilized to identify additional types, instantiations or variations of a selected component embodiment in the various views, in which:

Figure (or "FIG.") 1 is a block and circuit diagram of an exemplary first system embodiment and first apparatus embodiment in accordance with the teachings of the present invention.

Figure (or "FIG.") 2, divided into FIGs. 2A and 2B, are graphical diagrams illustrating a first exemplary current waveform through the solid state lighting and through a switch, respectively, in accordance with the teachings of the present invention.

Figure (or "FIG.") 3 is a graphical diagram illustrating an exemplary current waveform of a solid state lighting current overshoot, in accordance with the teachings of the present invention.

Figure (or "FIG.") 4 is a graphical diagram illustrating an exemplary current waveform of a solid state lighting current undershoot, in accordance with the teachings of the present invention.

Figure (or "FIG.") 5 is a graphical diagram of an inrush current and a blanking time interval in accordance with the teachings of the present invention.

Figure (or "FIG.") 6 is a graphical diagram illustrating combined pulse width modulation ("PWM") and amplitude modulation for brightness adjustment in accordance with the teachings of the invention.

Figure (or "FIG.") 7 is a graphical diagram illustrating hysteresis between two amplitude levels and duty cycle ratios for brightness adjustment in accordance with the teachings of the invention.

Figure (or "FIG.") 8 is a block and circuit diagram of an exemplary second system embodiment and second apparatus embodiment in accordance with the teachings of the present invention.

Figure (or "FIG.") 9 is a graphical diagrams illustrating a second exemplary current waveform through the solid state lighting and a rectified AC current in accordance with the teachings of the present invention.

Figure (or "FIG.") 10 is a block and circuit diagram of an exemplary third system embodiment in accordance with the teachings of the present invention.

Figure (or "FIG.") 11 is a timing diagram illustrating exemplary multiphase switching of the exemplary third system embodiment in accordance with the teachings of the present invention.

Figure (or "FIG.") 12 is a flow diagram of an exemplary method embodiment in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

While the present invention is susceptible of embodiment in many different forms, there are shown in the drawings and will be described herein in detail specific exemplary embodiments thereof, with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention and is not intended to limit the invention to the specific embodiments illustrated. In this respect, before explaining at least one embodiment consistent with the present invention in detail, it is to be understood that the invention is not limited in its application to the details of construction and to the arrangements of components set forth above and below, illustrated in the drawings, or as described in the examples. Methods and apparatuses consistent with the present invention are capable of other embodiments and of being practiced and carried out in various ways. Also, it is to be understood that the phraseology and terminology employed herein, as well as the abstract included below, are for the purposes of description and should not be regarded as limiting.

As mentioned above, exemplary embodiments of the present invention provide numerous advantages for providing power to solid state lighting, such as light emitting diodes. The exemplary embodiments allow for energizing one or more LEDs, using digital control and low side sensing, enabling low voltage IC implementations. The exemplary apparatus and system embodiments may be implemented with either fixed or variable frequency switching, and may be implemented with either AC or DC power sources. As a digital implementation, the exemplary embodiments may also be implemented at a reduced cost. The exemplary embodiments also provide for precise current control, within any selected tolerance levels. In addition, the exemplary embodiments also eliminate the required RC filtering of the prior art. Further advantages are discussed below.

Figure 1 is a block and circuit diagram of an exemplary first system 150 embodiment and first apparatus 100 embodiment in accordance with the teachings of the present invention, for a single channel of LEDs 110. As illustrated in Figure 1, the system 150 comprises an apparatus 100, a converter 120 with an array of LEDs 110 (as an exemplary type of solid state lighting), and a current sensor 160 (illustrated in Figure 8 as implemented using a resistor 160_A). The illustrated configuration for the converter 120 is a Buck converter, although many other configurations and types of converters may be utilized equivalently, requiring only the capability for "low side" (node 116) current sensing, *i.e.*, current sensor 160 is on the comparatively low side (*e.g.*, at node 116) of the power converter 120, as described in greater detail below. The converter 120 comprises an inductor 105 and a diode 115, with the inductor 105 having a series connection with the LEDs 110. The switch 155 may be considered part of the apparatus 100 or part of the converter 120. As known in the art, other components may also be included within the converter 120, and are also within the scope of the present invention.

The apparatus 100, also referred to as a "digital LED driver", comprises a controller 125, a plurality of comparators 130, 135, 140, and a reference voltage generator 145. The comparators 130, 135, 140 and reference voltage generator 145 may be implemented as known or becomes known in the electronic arts. Optionally, the apparatus 100 may also include an input-output ("I/O") interface 170, to receive (and/or transmit) various signals, such as on, off, brightness (dimming) information, or other control information (such as from a building control system), and may communicate using any protocol, as described below. The apparatus 100 also may include a memory 175, such as to store settings, values, and other parameters which may be used by the controller 125, and which also may have a connection to the I/O interface 170, for input or modification of such parameters. Various implementations of the controller 125 (and other controller 225 embodiments), the I/O interface 170, and the memory 175 are described in greater detail below. A switch 155, typically implemented as a field effect transistor ("FET") or any other type of transistor or switching device, may be considered to be part of either the apparatus 100, the converter 120, or the system 150, and is controlled by the controller 125, typically through an optional gate driver (buffer) 165. The current sensor 160 also may be

considered to be part of either the apparatus 100 or the system 150. Those of skill in the art will recognize that the current sensor 160 may be implemented in innumerable ways, in addition to the illustrated resistor (Figure 8), and any and all of which are considered equivalent and within the scope of the invention. Not separately illustrated in Figure 1 are the typical power (Vdd and/or V_{IN}), ground, and clock (oscillator) inputs and connections for the apparatus 100. In addition, either terminal illustrated as V_{IN}^- or V_{IN}^+ may also be a ground (GND) connection (*e.g.*, V_{IN}^+ and GND, or GND and V_{IN}^-). Also as illustrated, V_{IN}^+ and V_{IN}^- may be a DC voltage or a rectified AC (AC line voltage), using an optional rectifier 325. Exemplary current waveforms for an AC implementation are illustrated and discussed below with reference to Figure 9.

As mentioned above, the apparatus 100 implements "low-side" sensing, such that voltages are detected on the "low" side of LEDs 110, compared to prior art "high-side" sensing of inductor 105 (or LED 110) current. Accordingly, the apparatus 100 is not required to tolerate high voltages which would be necessary with high-side sensing. The apparatus 100 operates by detecting various LED 110 current levels when the switch 155 is on and conducting, and by the controller 125 calculating and predicting optimal switch 155 "on time" durations ("T_{ON}") (divided into first and second portions) and switch 155 "off time" durations ("T_{OFF}"). By controlling the on and off durations of the switch 155, the controller 125 thereby regulates the current through the LEDs 110, with current increasing during the on time, and decreasing during the off time (and flowing through diode 115, rather than the switch 155), as illustrated in Figure 2A. In addition, for these first system and apparatus embodiments, because the combined duration (arithmetic sum) of the on (T_{ON}) and off (T_{OFF}) times for the LEDs 110 is not constant, but is variable, the system 150 has a variable switching frequency (a constant switching frequency is discussed below with reference to Figure 8). The LED 110 current levels are detected as corresponding voltage levels across the current sensor 160 during the on time, and compared by the plurality of comparators 130, 135, 140, to corresponding reference voltages generated by reference voltage generator 145. When the switch 155 is off and not conducting, however, it should be noted that no current flow through or otherwise will be available to the current sensor 160 (switch 155 current falls to zero during T_{OFF}, as illustrated in Figure 2B), and as a consequence, the comparators 130, 135, 140, will not have corresponding

voltage input and will therefore have a low (binary zero) output. Described another way, during the off time of the switch 155, the comparators 130, 135, 140 are not providing any (valid) information concerning the LED 110 current levels.

In accordance with the present invention, the controller 125 will determine various "on" times of the switch 155 to provide a selected or predetermined average current level through the LEDs 110, which current is further less than a selected or predetermined first, high threshold level and greater than a selected or predetermined second, low threshold level, thereby regulating average current through the LEDs 110 with a predetermined current ripple level. A first comparator 130 is utilized to detect the first, high threshold ("HT") level, typically as a voltage across the current sensor 160, by comparing the voltage level across the current sensor 160 with a first reference voltage level provided by the reference voltage generator 145. A second comparator 135 is utilized to detect the second, low threshold ("LT") level, by comparing the voltage level across the current sensor 160 with a second reference voltage level provided by the reference voltage generator 145, and a third comparator 140 is utilized to detect the third, average level, by comparing the voltage level across the current sensor 160 with a third (*e.g.*, average ("AV")) reference voltage level provided by the reference voltage generator 145. Based upon those detected levels, the controller 125 will determine the accurate (and optimal) on time durations for the switch 155. Using those switch 155 on time durations, and a current "off" time duration (which at initial start up may be a default value), the controller 125 will calculate a next off time duration. Quite rapidly and within very few on and off cycles of the switch 155, the controller 125 will cause the on and off durations of the switch 155 to converge to accurate (and optimal) values, and further, to provide any corrections within very few clock cycles, such as due to potentially fluctuating input voltage levels (V_{IN}^{+} and/or V_{IN}^{-}).

Figure 2, divided into FIGs. 2A and 2B, are graphical diagrams illustrating a first exemplary current waveform through the solid state lighting (LEDs 110) (and being equal to the current through the inductor 105) and through the switch 155, respectively, in accordance with the teachings of the present invention. As illustrated in Figure 2A, during initial start up, the switch 155 is on ($T_{ON1}(1)$, interval 214), and the current through the LEDs 110 will increase (180). During this time

period, as the current increases and the voltage across the current sensor 160 increases, the voltage level across the current sensor 160 will be compared by the comparators 130, 135, 140. As the various threshold levels are reached, the comparators 130, 135, 140 will provide corresponding signals to the controller 125, and the controller 125, in turn, is adapted to determine the corresponding time intervals (durations) for the current to increase, for example, either from when the switch 155 has been turned on to the third, average current level (signal from the third comparator 140) ($T_{ON1}(K)$), or from the second, low threshold (signal from second comparator 135) to the third, average current level (also a signal from the third comparator 140) ($T_{ON1}(K)_A$), and then from the third, average current level to the first, high threshold level (T_{ON2}) (signal from the first comparator 130). Upon reaching the first, high threshold, the first comparator 130 will provide a corresponding signal to the controller 125, which will then turn off the switch 155, typically via the gate driver 165, and the current through the LEDs 110 will begin to decrease (181). During initial start up ($T_{ON1}(1)$), the $T_{ON1}(1)$ interval is not utilized (*e.g.*, insufficiently accurate, due to the start up time), and a default off time is implemented ($T_{OFF}(1)$), such that following the default interval, the switch 155 will be turned on again (187).

In accordance with the exemplary embodiments, the on time of the switch 155 is divided into two intervals, $T_{ON1}(K)$ and $T_{ON2}(K)$, indexed for each switching cycle "K" of the switch 155, with consecutive cycles referred to as "K" and "K+1", with $T_{ON1}(K)$ being the time interval commencing with turning on the switch 155 and ending with the LED 110 current reaching the third, average current level (I_{AV}), and with $T_{ON2}(K)$ being the time interval commencing with the current having reached the third, average current level (I_{AV}) and ending with the LED 110 current reaching the first, high threshold current level (I_{HT}). In addition, to accommodate various input (V_{IN}^{+}) and output (V_O) voltage levels, another T_{ON1} time interval is utilized, illustrated in Figure 2A as $T_{ON1}(K)_A$ (177) and $T_{ON1}(K+1)_A$ (198), which is the time interval commencing with the LED 110 current reaching the second, low threshold current level (I_{LT}) and ending with the LED 110 current reaching the third, average current level (I_{AV}). The $T_{ON1}(K)_A$ and $T_{ON1}(K+1)_A$ time periods are utilized for the non-linear rising of the inductor 105 current, illustrated as curves 183, 186 in Figure 2A. The alternative first on time, $T_{ON1}(K)_A$, from the second, low threshold (I_{LT}) to the

third, average current level (I_{AV}), also may be utilized generally when valid second, low threshold (I_{LT}) information is obtainable (depending upon whether the low threshold has already been reached when the blanking time interval has elapsed, as discussed below). Also in accordance with the exemplary embodiments, as the apparatus 100 has a few cycles of operation, the time at which the switch 155 is turned on will be at about the second, low threshold current level (I_{LT}).

When the switch 155 is turned on again (187), depending on the input (V_{IN}^{+}) and output (V_O) voltage levels, the increase in current through LEDs 110 may be comparatively linear (182, 185), typically for the input voltage V_{IN}^{+} being significantly greater than the output voltage V_O, or may be nonlinear (183, 186), typically for the input voltage V_{IN}^{+} being comparatively close in value to the output voltage V_O. The exemplary embodiments of the present invention provide current control for and regardless of either the linear or the nonlinear situation. As the current increases, based upon the input from the comparators 130, 135, 140, the controller 125 will determine the time intervals (durations) $T_{ON1}(K)$ and $T_{ON2}(K)$. When the first, high threshold has been reached, the controller 125 will again turn off the switch 155 (189, 199), and will calculate the next off duration for the switch 155 (to be utilized currently), such that the LED current level is generally kept above the second, low threshold (188), and does not have undershoot (or has insignificant undershoot) (as may have occurred previously (187) during initial start up, as illustrated).

The controller 125, generally, will determine a current off time of the switch 155 as a function of the on time and the previous off time. More specifically, the controller 125 will determine a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period. Even more specifically, the controller 125 will determine a current off time period of the switch as a function of a current first on time period, a previous second on time period, and a previous off time period. In another alternative, and also more specifically, the controller 125 will determine a current off time period of the switch as a function of a current first on time period, a previous first on time period, a previous second on time period, and a previous off time period. In addition, current and previous should be understood in their relative sense, which are also pair-wise equivalent to the relative terms next and current (respectively, as a pair), so that any

reference or claim to current and previous should be understood to mean and include next and current, respectively.

During any given cycle, at the point of turning off the switch 155 (189, 199), the current values (or parameters) for $T_{ON1}(K+1)$, $T_{ON2}(K+1)$ and the previous values (or parameters) for $T_{ON1}(K)$, $T_{ON2}(K)$, and $T_{OFF}(K)$ are known. In accordance with the exemplary embodiments, the next off time ($T_{OFF}(K+1)$) which will be utilized in the current cycle (K+1) will be calculated or otherwise determined by the controller 125 using the previous off time ($T_{OFF}(K)$), and the various on times, such as the previous second on time $T_{ON2}(K)$ and the current first on time $T_{ON1}(K+1)$, or the previous second on time $T_{ON2}(K)$, the current first on time $T_{ON1}(K+1)$ and the previous first on time $T_{ON1}(K)_A$. More specifically, in accordance with the invention, the switch 155 off time ($T_{OFF}(K)$) is adjusted such that the first and second on times are generally about or substantially equal to each other, $T_{ON1}(K) \approx T_{ON2}(K)$, which then provides the desired current regulation, maintaining the average current level (I_{AV}), while generally maintaining the current below the first, high threshold (I_{HT}) and above the second, low threshold (I_{LT}), depending upon the allowed or tolerated current ripple level.

When V_{IN} is significantly higher than V_O, the inductor 105 current rise slope generally is substantially linear (182, 185). We may assume that the converter 120 input and output voltages V_{IN} and V_O do not vary between consecutive cycles. For a Buck converter, the current rising slope is defined by (Equation 1):

$$current\_rising\_slope = \frac{V_{IN} - V_o}{L},$$

such that the current rising slope does not vary appreciably between consecutive cycles. Since comparators 130, 135, 140 are comparing against fixed thresholds I_{HT}, I_{LT} and I_{AV}, T_{ON2} should remain the same across the consecutive cycles, *i.e.*, (Equation 2):

$$T_{ON2}(K+1) = T_{ON2}(K),$$

such that any calculation using a current second on time $T_{ON2}(K+1)$ is equivalent to and includes using a previous second on time period $T_{ON2}(K)$, and vice versa. By the time $T_{ON1}(K+1)$ elapses, the controller 125 knows $T_{OFF}(K)$, $T_{ON2}(K)$ and $T_{ON1}(K+1)$. Since $T_{OFF}(K)$, $T_{ON1}(K+1)$, and $T_{ON2}(K+1)$ (which equals $T_{ON2}(K)$ from Equation 2) share the same peak (I_{HT})and valley (I_{LT})currents, then (Equation 3)

$$\Delta I = \frac{V_o}{L} T_{OFF}(K) = \frac{V_{in} - V_o}{L} \{T_{ON1}(K+1) + T_{ON2}(K+1)\}$$
$$\approx \frac{V_{in} - V_o}{L} \{T_{ON1}(K+1) + T_{ON2}(K)\}$$

Because an average current of I_{AV} and equal halves (time intervals) for of peak (I_{HT})and valley (I_{LT}) currents are desired, then (Equation 4):

$$T_{ON1}(K+1) = T_{ON2}(K).$$

The desired T_{OFF} (K+1) can be formulated as (Equation 5):

$$\Delta I_{desired} = \frac{V_o}{L} T_{OFF}(K+1) = \frac{V_{IN} - V_o}{L} \{2 \bullet T_{ON2}(K)\}.$$

Dividing Equation 5 by Equation 3 (i.e., Equation 5 over Equation 3) to remove a dependence over V_{IN}, V_O and L, yields (Equation 6):

$$\frac{T_{OFF}(K+1)}{T_{OFF}(K)} = \frac{2 \bullet T_{ON2}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}.$$

Thus, for an exemplary embodiment, the next T_{OFF} (K+1) should be generated by the controller 125 as (Equation 7):

$$T_{OFF}(K+1) = \frac{2 \bullet T_{ON2}(K) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}.$$

Implementation of Equation 7 requires one multiply, one shift, one addition and one divide operation per converter 120 switching cycle. The performance of the apparatus 100, therefore, is about two switching cycles to converge to its target values or parameters for I_{AV}, I_{HT}, and I_{LT}. In addition, the requirement of one multiply and divide per converter 120 switching cycle can be relaxed if the converter 120 switching frequency is much higher than normal ripple found in V_{IN} and V_O. As mentioned above, however, when the current first on time $T_{ON1}(K+1)_A$ or previous first on time $T_{ON1}(K)_A$ are available (*i.e.*, may be measured after the blanking interval described below), these measurements may be utilized instead of the current first on time $T_{ON1}(K+1)$ or previous first on time $T_{ON1}(K)$.

When V_{IN} is not much higher than V_O, the rising slope of the inductor 105 current is no longer linear (183, 186 in Figure 2A). Typically, the initial slope during the $T_{ON1}(K)$ interval is steeper than the $T_{ON2}(K)$ interval. Because in this case Equation 7 may yield a much lower valley (I_{LT}) current than the desired average current I_{AV}, Equation 7 can be modified as (Equation 8):

$$T_{OFF}(K+1) = \frac{(T_{ON1}(K)_A + T_{ON2}(K)) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)} \quad .$$

As mentioned above, $T_{ON1}(K)_A$ is the time interval from I_{LT} to I_{AV}, and may be determined along curves 183, 186 or the curves 182, 185. As discussed in greater detail below, however, because the controller 125 of various exemplary embodiments does not utilize any output of comparators 130, 135, 140 during a "blanking" interval following turning on the switch 155, it is possible that the output of the second comparator 135 (I_{LT}) may be already high when the blanking interval has elapsed and, in which case, Equation 7 is utilized to calculate T_{OFF} (K+1) as well, rather than Equation 8.

Referring again to Figure 1, the thresholds (peak (I_{HT}), valley (I_{LT}) and average (I_{AV}) currents used by comparators 130, 135, 140 are set (predetermined) within the apparatus 100, such as by inputting values using the I/O interface 170, and storing those values as parameters or values in memory 175. For example, for an allowable or selectable 20% ripple in LED 110 current regulation, peak (I_{HT}), average (I_{AV}) and valley (I_{LT}) currents can be set to be apart by 10% intervals. Typical values for peak (I_{HT}), average (I_{AV}) and valley (I_{LT}) currents are represented by corresponding voltages across the current sensor 160, *e.g.*, at around 0.3 Volts (and can be lower when using an IC). The current sensor 160 is selected based upon the desired application; for example, when implemented as a resistor, a value is selected to pass a desired average current.

For even more fine-grained current regulation, the exemplary embodiments of the invention also account for rise and fall delays of the various switching elements, such as the rising and falling time delays of the switch 155, the gate driver 165, and the comparators 130, 135, 140, with any propagation delays included within any such rising and falling time delays. Figure 3 is a graphical diagram illustrating an exemplary current waveform of a solid state lighting current overshoot, in accordance with the teachings of the present invention, illustrating in greater detail section 215 from Figure 2. Figure 4 is a graphical diagram illustrating an exemplary current waveform of a solid state lighting current undershoot, in accordance with the teachings of the present invention, illustrating in greater detail section 210 from Figure 2.

Referring to Figure 3, when the LED 110 current reaches the first, high threshold (I_{HT}) at time t_1, there is a rise time associated with the first (peak) comparator 130 (interval 201), such that the controller 125 does not receive the corresponding information until time t_2. At time t_2, the controller 125 will turn off the gate driver 165 to turn off the switch 155, resulting in a fall time associated with the gate driver 165 and the switch 155 (interval 202), such that the switch 155 has stopped conducting at time t_3. As the current through the LEDs 110 (and switch 155) decreases, there is another fall time associated with the first (peak) comparator 130 (interval 203), such that the controller 125 does not receive the corresponding information until time t_4. Because of these rising and falling time delays, unless the delays are accounted for, there can be an overshoot of the LED 110 current, with the LED 110 current being higher than the selected first, high threshold. Accordingly, the controller 125 receives the corresponding comparator (130) rising and falling edge information at t_2 and t_4.

Similarly, referring to Figure 4, when the LED 110 current decreases to the second, low threshold (I_{LT}) during an off time period, no current is flowing through the switch 155 (Figure 2B), so no information is available to the controller 125. At time t_6, the end of the off time period, the controller 125 will turn on the gate driver 165 to turn on the switch 155, resulting in a rise time associated with the gate driver 165 and the switch 155 (interval 205), such that the switch 155 will start conducting at time t_7. As the current through the LEDs 110 (and switch 155) increases to the low threshold (t_8), there is a rise time associated with the second (valley) comparator 135 (interval 206), such that the controller 125 does not receive the corresponding information until time t_9. Because of these rising and falling time delays, unless the delays are accounted for, there can be an undershoot of the LED 110 current, with the LED 110 current being lower than the selected second, low threshold. Accordingly, the controller 125 receives the corresponding comparator (135) rising edge information at t_9.

The exemplary embodiments of the invention may be implemented to account the various delays associated with the rising and falling times of the first (peak) comparator 130, the gate driver 165 and the switch 155, and the second (valley) comparator 135. By making the rising and falling delay times equal (symmetrical) for each comparator 130, 135, then the time interval during which the controller 125

receives the corresponding comparator (130, 135) rising and falling edge information (*e.g.*, at t_2 and t_4) is equal to the actual overshoot time interval (of t_1 to t_3). Accordingly, the overshoot time may be measured from the first comparator 130 rising edge (t_2) (also coincident with the falling edge of the off command/signal to the gate driver 165) to the first (peak) comparator 130 falling edge (t_4), resulting in (Equation 9):

$$T_{overshoot} \approx T_{p\_gate\_drive\_fall} + T_{pk\_comp\_fall} .$$

Accordingly, for finer-grained control, the overshoot time is subtracted from T_{ON2} by the controller 125, such that the actual LED 110 current would barely reach the first, high threshold I_{HT}.

Because the second comparator 135 is not receiving comparable information during T_{OFF}, a different approach may be utilized, as an option, for determining an undershoot time interval or duration. Accordingly, by also making the first comparator 130 and second comparator 135 to be similar, such that each effectively having the same rising and falling time intervals as the other (symmetrical), then the undershoot time may be considered to be substantially equal or otherwise comparable to the overshoot time. Assuming such symmetry between comparators 130, 135, results in (Equation 10):

$$T_{undershoot} \approx T_{overshoot},$$

such that the interval from t_2 to t_4 in turn also would be equal to the undershoot time interval (of t_5 to t_7). In this instance, the undershoot time is subtracted from T_{OFF} by the controller 125, such that the actual LED 110 current would barely decrease to the second, low threshold I_{LT}. In both overshoot and undershoot circumstances, the measurements of these intervals may be completed during the initial system 150 start up, and treated as constants during subsequent switching cycles or, alternatively, the overshoot and undershoot time intervals may be calibrated whenever the corresponding first (peak) comparator 130 has valid information. In addition, because the undershoot and overshoot time periods may be symmetrical, when the gate driver 165 and switch 155 have symmetrical rise and fall times, and when the various comparators have symmetrical rise and fall times, then the measurement of one (overshoot) also may be used for the other (undershoot).

In another variation, when the second comparator 135 does not provide valid information during an on time interval (*e.g.*, the second comparator 135 has already indicated that the low threshold of current has been reached when the blanking time has elapsed), then the relevant undershoot time may be considered to be only the rise time of the gate driver 165 and switch 155 which, given the symmetrical rise and fall times, would be equal to the fall time of the gate driver 165 and switch 155. This may be determined as described below, or as another alternative, the overshoot time (which also includes first comparator 130 rise or fall time) may be utilized as a sufficiently accurate estimation.

In addition, in exemplary embodiments, depending upon selected tolerance levels, the undershoot compensation may be omitted, as lower current levels are not harmful to the LEDs 110, and if the undershoot is not large, may not be visually apparent. Alternatively, the first, high threshold I_{HT} and the second, low threshold I_{LT} may also be adjusted in advance, to provide tighter regulation, such as spacing them apart by 5% of 7.5% intervals, rather than 10% intervals, for example.

Both of the overshoot and undershoot controls, however, generally should be implemented such that both the first (peak) comparator 130 and the second (valley) comparator 135 periodically trip, to avoid the LED 110 current from deviating down or up without notice. Accordingly, in accordance with the exemplary embodiments, the controller 125 will periodically allow the LED 110 current to rise and fall sufficiently to trip the first (peak) comparator 130 and the second (valley) comparator 135, respectively.

Conversely, if the specification for LED 110 current ripple allow current overshoot (*e.g.*, allowing the LED 110 current envelope to follow V_{IN} ripple), then the overshoot and undershoot may be made symmetrical as well, such as by increasing the off time T_{OFF} by the undershoot (or symmetrical overshoot) interval. By doing so, the LED 110 average current would remain constant.

Figure 5 is a graphical diagram of an inrush current through the switch 155 when it is turned on and a "blanking" time interval in accordance with the teachings of the present invention. In the prior art, such an inrush (transient) current would be filtered using an additional capacitor and resistor (RC filter) in parallel with the current sensor 160; in the exemplary embodiments, the use of such an RC filter is

not required, and a blanking time interval is utilized instead, as mentioned above and as described below. Initially the controller 125 issues a command to the gate driver 165 (and thereby switch 155) to turn on, at time t_{10}. After the gate driver 165 and switch 155 rise time (interval 211) (combined as "Tp_gate_drive_rise" time), the switch 155 current exhibits a transient spike, referred to as an "inrush", starting at time t_{11}, typically caused by its terminal capacitance and the reverse recovery of diode 115, which lasts for interval 212 (through time t_{12}). This inrush current through the switch 155 may be higher than the average current (I_{AV}) and potentially even higher than the first, high threshold (I_{HT}), causing their respective comparators 140, 130 to trip (and provide corresponding logic high signals to the controller 125). In accordance with the exemplary embodiments, the controller 125 disregards this information by establishing or setting a "blanking" time interval (216) ("Tblank"), during which the outputs of the comparators 130, 135, and 140 are ignored. The blanking time interval commences when the controller 125 generates the command to turn on the gate driver 165 (and switch 155) (t_{10}), and extends until the transient inrush current has settled (t_{13}), resulting in (Equation 10): $T_{blank} > T_{P\_gate\_drive\_rise} + T_{inrush}$.

The transient, inrush time interval (212) is generally a function of switch 155 terminal capacitance, diode 115 reverse recovery charge, and the sense resistance value (when current sensor 160 is implemented as a resistor). If the inrush current is higher than the average current (I_{AV}), it is possible for the controller 125 to determine the inrush time and adjust the blanking time appropriately.

Ideally, Equation 4 provides that T_{ON1} should be equal to T_{ON2}. The controller 125, however, as mentioned above, should turn on the gate driver 165 and switch 155 earlier by an amount equal to their combined rise time (Tp_gate_drive_rise time). In a system where the gate driver 165 is designed such that its rise time is close to the overshoot time (*e.g.*, the gate driver 165 and switch 155 have symmetrical rising and falling times and comparator delay time is not significant), then the overshoot time can be utilized to decrease T_{OFF}.

Yet another method of determine the rise time of the gate driver 165 and switch 155 (Tp_gate_drive_rise) is through the third, average current (I_{AV}) comparator 140. Although the moment when the switch 155 inrush current trips the third, average current (I_{AV}) comparator 140 should not be used as an indicator of the actual inductor

105 average current, it can be used to indicate the time when the switch 155 actually starts to conduct. Accordingly, the rise time of the gate driver 165 and switch 155 and the rise time of the third, average current (I_{AV}) comparator 140 ("Tav_comp_rise ") (Tp_gate_drive_rise + Tav_comp_rise) can be measured from the time the controller 125 issues the turn on command until the third, average current (I_{AV}) comparator 140 trips. Then the third, average current (I_{AV}) comparator 140 rise time (Tav_comp_rise) is subtracted from the measurement in order to obtain the rise time of the gate driver 165 and switch 155 (Tp_gate_drive_rise). In an exemplary embodiment, the third, average current (I_{AV}) comparator 140 rise time (Tav_comp_rise) is a known design parameter or is significantly smaller than the rise and fall times of the gate driver 165 and switch 155 (Tp_gate_drive_rise and Tp_gate_drive_fall).

The rise times of the various comparators 130, 135 and 140 may also affect the measurements of T_{ON1} and T_{ON2}. As mentioned above, T_{ON1} is the interval from the time the current reaches the low threshold current level (I_{LT}), as determined by the second (I_{LT}) comparator 135 (or from the time when the switch 155 actually conducts) to the time the current reaches the average current level (I_{AV}), as determined by the third, average current (I_{AV}) comparator 140. T_{ON2} is the time interval from the average current level to the first, high (peak) current level, namely, as determined by the third, average current (I_{AV}) comparator 140 and the first (I_{HT}) comparator 130, respectively. In the exemplary embodiments, therefore, the first (I_{HT}) comparator 130 and the third, average current (I_{AV}) comparator 140 are designed or implemented to have the same or substantially similar delay times (*i.e.*, $T_{av\_comp\_rise} = T_{pk\_comp\_rise}$). With the rise times of the first (I_{HT}) comparator 130 and the third, average current (I_{AV}) comparator 140 being substantially the same, then T_{ON2} can be measured by the interval from when the controller 125 receives the rising edge of the third, average current (I_{AV}) comparator 140 to when the controller 125 receives the rising edge of the first (I_{HT}) comparator 130. It should be noted, as mentioned above, that this measurement does not apply during the blanking time interval, or when the controller 125 does not receive a valid rising edge of the first (I_{HT}) comparator 130 (*e.g.*, due to overshoot compensation, in which case T_{ON2} may be adjusted occasionally in order for the first (I_{HT}) comparator 130 to trip and provide information at these various intervals).

As indicated above, T_{ON1} may be measured from the interval beginning with the controller 125 receiving the rising edge of the second (I_{LT}) comparator 135 (when available (*i.e.* when the rising edge did not occur during the blanking interval)) until the controller 125 receives the rising edge of the third, average current (I_{AV}) comparator 140, or beginning with the controller 125 generating the turn on command for the gate driver 165 and switch 155) until the controller 125 receives the rising edge of the third, average current (I_{AV}) comparator 140 (T_{ON1} measured). For the former case, given the symmetry of the comparators, no additional compensation is needed for determining T_{ON1} measured. In the latter case however, when the rising edge of the second (I_{LT}) comparator 135 does not provide valid information (during the blanking interval, or due to undershoot compensation), then for this measurement, the rise time of the gate driver 165 and switch 155 should then be subtracted, to provide the actual value of T_{ON1} ($T_{ON1} \approx T_{ON1}$ measured - Tav_comp_rise). T_{ON1} may also be measured using the transient current spike (inrush current), if the inrush current is sufficiently high to trip the third, average current (I_{AV}) comparator 140, indicating a start of the conduction by the switch 155. T_{ON1} is then the interval between the controller 125 receiving the first rising edge of the third, average current (I_{AV}) comparator 140 due to the inrush current and receiving the second rising edge of the third, average current (I_{AV}) comparator 140 (after the transient has settled). Knowing both T_{ON1} and T_{ON2}, the controller 125 may then determine T_{OFF}.

In the event that during initial start up, the third, average current (I_{AV}) comparator 140 stays high after the transient current spike (inrush current) has settled, indicating that the current is already too high, there is no need to measure T_{ON1} and T_{ON2}. Rather, TOFF is extended, to allow current to decrease, with valid measurements for T_{ON1} and T_{ON2} obtainable in the next cycle.

Figure 6 is a graphical diagram illustrating combined pulse width modulation ("PWM") and amplitude modulation for brightness adjustment in accordance with the teachings of the invention. The exemplary embodiments implement brightness control (dimming) using a combination of at least two different electrical biasing techniques across the LEDs 110, such as PWM and amplitude modulation (or constant current regulation ("CCR"). A first electrical biasing technique, by itself, will tend to produce a first wavelength shift (higher or lower) in

response to a change in intensity, such as in response to a change in duty cycle for PWM, while a second electrical biasing technique, by itself, will tend to produce a second, opposite or opposing wavelength shift (lower or higher, respectively) in response to the change in intensity, such as in response to a change in amplitude for analog regulation or CCR. In accordance with the exemplary embodiments, any resulting wavelength shift is minimized or maintained within a selected tolerance level by utilizing at least two different and opposing electrical biasing techniques (such that the opposing wavelength shifts effectively "cancel" each other). Additional discussion of that methodology is in one or more related patent applications. To decrease brightness, for PWM, the duty cycle is decreased (*e.g.*, from D1 to D2), and for amplitude modulation (CCR), the amplitude of the LED current is decreased (*e.g.*, from ILED1 to ILED2), as illustrated in Figure 6. In accordance with the exemplary embodiments, the controller 125 implements dimming by using both PWM and amplitude modulation, either alternating them in successive modulation intervals or combining them during the same modulation interval, with the latter illustrated in Figure 6. This inventive combination of at least two different electrical biasing techniques having opposing effects on wavelength emission allows for both regulating the intensity of the emitted light while controlling the wavelength emission shift, from either or both the LED response to intensity variation (dimming technique) and due to p-n junction temperatures changes, and also to produce dynamic lighting and color effects.

Figure 7 is a graphical diagram illustrating hysteresis between two amplitude levels (ILED1, ILED2) and duty cycle ratios (D1L, D2L, D1H, D2H) for brightness adjustment in accordance with the teachings of the invention. In order to prevent jitter, a hysteresis is implemented as illustrated in Figure 7. The operating points (ILED1, D1L) have the same brightness (color) to (ILED2, D2L), and the same brightness applies to (ILED1, D1H) and (ILED2, D2H). When D1 comes from high brightness down to D1L, ILED1 is changed to ILED2 and D2L is used instead. When D2 comes up from low brightness to D2H, ILED2 is switched to ILED1 and D1H is used.

Figure 8 is a block and circuit diagram of an exemplary second system 250 embodiment and second apparatus 200 embodiment, for fixed frequency switching

operation, in accordance with the teachings of the present invention. The second system 250 and second apparatus 200 differ from the first system 150 and first apparatus 100 insofar as: (1) the combined duration (arithmetic sum) of the on (T_{ON}) and off (T_{OFF}) times for the LEDs 110 is constant, not variable, such that the second system 250 has a fixed or constant switching frequency (rather than the variable switching frequency previously discussed); and (2) the controller 225 is adapted to provide current control when the commencement or initiation of the on time of the switch 155 is at a fixed, regular frequency. In addition, as an illustrated alternative, the controller 225 is coupled directly to the switch 155, rather than via a gate driver (165). It should be understood, however, that the second system 250 and second apparatus 200 may also include such a gate driver circuit 165, such as a buffer.

For the second system 250 and second apparatus 200, the controller 225 includes an error generator 260, a compensator 255, and a control block 251 for determining the respective on (T_{ON}) and off (T_{OFF}) durations for the switch 155. In this embodiment, the controller 225 also provides that T_{ON1} is substantially equal to T_{ON2}, with the error generator 260 generating an error signal substantially equal or proportional to the difference between T_{ON1} and T_{ON2} (error = T_{ON2} - T_{ON1}, error $\approx$ T_{ON2} - T_{ON1}, or error $\approx c \cdot (T_{ON2} - T_{ON1})$, where "c" is a constant of proportionality). The error signal is provided to the compensator 255, which then adjusts the on time (T_{ON}) of the switch 155, which is then correspondingly switched on and off by the control block 251. It should be noted, because the switch 155 is switched on at a fixed frequency, adjusting the on time (T_{ON}) of the switch 155 automatically changes the off time (T_{OFF}) of the switch 155 (*e.g.*, increasing the on time T_{ON} decreases the off time T_{OFF}, and vice versa).

Figure 9 is a graphical diagrams illustrating a second exemplary current waveform through the solid state lighting and a rectified AC current in accordance with the teachings of the present invention. Such a rectified AC current 301 (or voltage) may be provided by a rectifier 325 to provide a voltage input V_{IN} (illustrated as V_{IN}^{+} and V_{IN}^{-}) having a DC average value, from an AC line voltage (AC mains), for example, and may be utilized with either the first or second system 150, 250 and first or second apparatus 100, 200, and also may be utilized with the third system 350 discussed below. When the rectified AC current 301 is below a selected (or

predetermined) threshold, illustrated as intervals 303, there is generally no switch 155 current, and the apparatus 100, 200 will typically be off during these AC zero crossing intervals. As illustrated, the switch 155 is turned on, above the selected (or predetermined) threshold, the LED 110 current 302 will initially track the rectified AC current 301, increasing to the second, low threshold (I_{LT}), reaching the average current level (I_{AV}) and then the first, high threshold (I_{HT}), followed by turning the switch 155 off for its calculated duration, and followed by successive on and off cycles, as described above, using the measurements and calculations described above for T_{ON1}, T_{ON2}, and T_{OFF}, or using the error signal (*e.g.*, error $\approx T_{ON2} - T_{ON1}$) described above, for either variable or fixed frequency embodiments. Such an apparatus and system can be built directly into an Edison socket, and further, can provide power factor correction ("PFC"). In order to achieve PFC operation, the controller 125 or compensator 255 is comparatively slow with respect to a V_{IN} ripple frequency of 120Hz (or 100Hz). For example and without limitation, for each half of the AC cycle, the T_{ON} determined and outputted by the compensator 255 can be regarded as a constant, and is adjusted during successive half-cycles.

It should be noted that the first system 150, first apparatus 100, the second system 250 and second apparatus 200, and their versions including an AC rectifier 325, may be scaled or extended to multiple channels of LEDs 110. In one such implementation, the first or second apparatus 100, 200 is instantiated in its entirety for each separate channel of LEDs 110.

In another such implementation, discussed below with reference to Figure 10, the comparators 130, 135, 140 are instantiated separately for each separate or independent channel of LEDs 110, such that the LED 110 current through each channel is separately monitored. In this scaled embodiment, the controller 125, 225 then has multiple outputs, one to each to each gate driver 165 (which in turn is coupled to a corresponding switch 155 for each separate or independent channel of LEDs 110). The controller 125, 225 separately computes the various on (T_{ON1} and T_{ON2}) durations for the switch 155, and for apparatus 100, the controller 125 also computes the off (T_{OFF}) duration, for each separate (or independent) channel of LEDs 110, and separately controls each gate driver 165 to each switch 155 for each separate channel of

LEDs 110 to provide the current regulation through each such channel of LEDs 110 as discussed above and as discussed below.

Figure 10 is a block and circuit diagram of an exemplary third system 350 embodiment, for multichannel operation, in accordance with the teachings of the present invention. As mentioned above, the various first and second apparatus 100, 200 may be extended to control current through a plurality of separate arrays 310 (also referred to equivalently as channels or strings) of LEDs 110, illustrated as array 310_1 having LEDs 110_1, array 310_2 having LEDs 110_2, through array 310_n having LEDs 110_n. Each such array or channel 310 includes at least one LED 110 or a plurality of LEDs 110 connected in series. In contrast with the prior art, the plurality of LEDs 110 of each array are not required to be identical or from the same manufacturing bin; instead, because of the separate control and regulation provided by the exemplary embodiments, there may be significant variation among the LEDs 110, for a considerable cost savings.

With the separate current control for each LED array 310, the regulated current can be matched to each separate LED array 310. Accordingly, various LED arrays 310 are not subject to excessive current levels, that would be caused in the prior art systems from some LED arrays having a higher impedance and drawing less current than expected. As a consequence, the exemplary third system 350 enables increased durability, improved system lifetime, decreased heat generated (also enabling a corresponding decrease in the size of heat sinks for the LEDs 110), a decrease in the number of LEDs 110 required for the same optical output, and overall increased system efficiency and efficacy.

As illustrated for the third system 350, each array 310 has a corresponding switch 155, illustrated as switch 155_1, switch 155_2, through switch 155_n, which are controlled by respective gate driver circuits (buffers) 165 (illustrated collectively, for ease of discussion), under the control of at least one controller 125, 225. The comparators 130, 135, 140 are instantiated separately for each separate or independent array or channel 310 of LEDs 110, such that the LED 110 current through each array (channel) 310 (via corresponding current sensors 160_1, 160_2, through 160_n) is separately monitored and separately controlled, as described above for the first and second systems 100, 200. At least one reference voltage generator 145 provides the

corresponding reference voltages (corresponding to the first (high) threshold, average, and second (low) threshold) for each current through each separate array 310. It should be noted that the various average, first and second threshold currents may be either the same or different across the various arrays 310, such that any selected array 310 may have its own set average and threshold current levels, separate from the average and threshold currents of the other arrays 310.

In this scaled, third system 350 embodiment, the controller 125, 225 then has multiple outputs, one to each to each gate driver 165, to turn on or off a corresponding switch 155 for each separate array 310 of LEDs 110. The controller 125, 225 separately determines the various on (T_{ON1} and T_{ON2}) durations for each corresponding switch 155_1, switch 155_2, through switch 155_n, and for variable frequency operation, the controller 125 also computes the off (T_{OFF}) duration, for each separate (or independent) array 310 of LEDs 110. The controller 125, 225 separately controls each gate driver 165 to each switch 155_1, switch 155_2, through switch 155_n, for each separate array 310 of LEDs 110, to provide separate current regulation through each separate channel of LEDs 110 in accordance with the exemplary embodiments of the invention.

Accordingly, for each separate array 310 of LEDs 110, for variable frequency switching, the controller 125 will determine T_{ON1} and T_{ON2}, and a corresponding T_{OFF}, as previously described above for the first system 150 and first apparatus 100, to provide regulated current control, for each array 310, and for fixed frequency switching, the controller 225 will determine T_{ON1} and T_{ON2}, as previously described above for the second system 250 and second apparatus 200, to provide regulated current control, for each array 310.

While the exemplary third system 350 provides separate control to each LED array 310, such control may be independent, controlling each LED array 310 completely independently of all the other LED arrays 310, or such control may include any type of coordinated, joint or dependent regulation, for any selected lighting or color effect, as may be necessary or desirable for any selected application. In addition, such independent or dependent regulation may be implemented for any type of LEDs 110, such as separate or independent control of red, blue, and green LEDs 110, or coordinated control of such red, blue, and green LEDs 110, such as to produce various

lighting effects having a selected hue, for example. Also for example, lighting effects such as output intensity, color output, color temperature, etc. may be regulated independently or in a coordinated manner for each LED array 310. Importantly, the exemplary third system 350 is capable of providing completely separate and independent current regulation of each LED array 310, with any such independence selectively implemented or not, for example, by the end user of the exemplary third system 350. Also importantly, the exemplary third system 350 is capable of providing any type of coordinated current regulation of each LED array 310, with any such coordination selectively implemented or not, for example, by the end user of the exemplary third system 350.

As an example of one form of coordinated control, in the exemplary third system 350, interleaving of switch 155 on (T_{ON}) durations may be implemented, providing a multiphase control, such that only selected arrays 310 are switched on and are conducting current during a given time interval. Figure 11 is a timing diagram illustrating exemplary multiphase switching of the exemplary third system embodiment, for "n" arrays 310 of LEDs 110, in accordance with the teachings of the present invention. As illustrated, each T_{ON} "pulse" 370 represents the on duration (T_{ON}) of a switch 155 of an array 310; while illustrated as a square wave, it may have any waveform, and merely represents a signal from the controller 125, 225 to turn on (and keep on for the selected on time duration) the corresponding switch 155 (via a corresponding gate driver 165). Also as illustrated, the timing of each such T_{ON} pulse 370 differs across the "n" arrays, with T_{ON} pulses 370_1, 370_{n-3}, and 370_{n-2} occurring during time interval t_A for LED arrays 310_1, 310_{n-3}, and 310_{n-2}, respectively; T_{ON} pulses 370_1, 370_2, 370_{n-2} and 370_{n-1} occurring during time interval t_B for LED arrays 310_1, 310_2, 310_{n-2} and 310_{n-1}, respectively; T_{ON} pulses 370_2, 370_3, 370_{n-1} and 370_n occurring during time interval t_C for LED arrays 310_2, 310_3, 310_{n-1} and 310_n, respectively; and so on. The various on durations may be selected to be separate (*e.g.*, T_{ON} pulses 370_1 and 370_4) or to overlap (*e.g.*, T_{ON} pulses 370_1 and 370_2), as may be necessary or desirable.

Because of this interleaving, multiphase control, not all LED arrays 310 are receiving current at the same time. This enables a much smoother AC input current, which minimizes any requirement on input electromagnetic interference (EMI)

filter size, further enabling a reduction in the input filter capacitor size, and reduced component costs. It is also expected to work well with a thyristor-type dimming.

It should be noted that the controllers 125, 225 may be implemented the same, and configured or otherwise programmed for operation as part of any of the systems 150, 250, and 350.

Figure 12 is a flow diagram of an exemplary method embodiment, in accordance with the teachings of the present invention, for controlling the energizing of solid state lighting, such as LEDs 110, and provides a useful summary. As discussed above, the solid state lighting is coupled to a switch (155) providing an electrical current path (*e.g.*, through current sensor 160), and with the solid state lighting having an electrical current. The method begins, start step 400, with turning the switch 155 into an on state, step 405. The method then detects when the electrical current has reached a predetermined average current level, step 410, and detects when the electrical current has reached a first predetermined (*e.g.*, high) current threshold, step 415. When available (*i.e.*, not during the blanking interval), and prior to detecting the average current level, step 410 may also include detecting when the electrical current has reached a second predetermined (*e.g.*, low) current threshold. The method then determines a first on time period (T_{ON1}) as a duration between the detection of the second predetermined (*e.g.*, low) current threshold (or turning the switch into the on state) and the detection of the predetermined average current level, step 420, and determines a second on time period (T_{ON2}) as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold, step 425. An on time period (T_{ON}) of the switch is then determined as substantially equal or proportional to the sum of the first on time period and the second on time period ($T_{ON} \approx T_{ON1} + T_{ON2}$), step 430. When the on time period has elapsed, the switch is turned off, step 435. For a first embodiment, the exemplary method also determines a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period (Equations 7 and 8), step 440. When the method continues, step 445, then following expiration of the off time period, step 450, the method returns to step 405 to turn the switch on, and the method iterates. When the method does not continue in step 445, the method may end, return step 455.

Not separately illustrated, the method may also include: adjusting the current off time period to provide that the first on time period is substantially equal to the second on time period (($T_{ON1} \approx T_{ON2}$); or decreasing the current off time period proportionally to a driving gate rising edge time period. In addition, the determination of the current off time period of the switch may be a further function, more specifically, of previous first and second on times and one or more current first on times.

The exemplary method may also provide for determining a blanking time interval following turning the switch into the on state, and ignoring the detection of the second predetermined current threshold, the detection of the predetermined average current level or the detection of the first predetermined current threshold during the blanking time interval. The blanking time interval may be determined as proportional to a gate rising edge time period and a transient current time period, or as proportional to a gate rising edge time period and detection of the predetermined average current level.

The exemplary method may also provide for adjusting a brightness level of the solid state lighting by using at least two electrical biasing techniques, and for example, adjusting a brightness level of the solid state lighting by using a hysteresis of at least two electrical current amplitude levels and at least two electrical current duty cycle ratios.

The method may also provide for current overshoot protection, by adjusting the second on time period proportionally to a driving gate falling edge time period, and more particularly, such as by decreasing the second on time period proportionally to a driving gate falling edge time period and a comparator falling edge time period.

The method may also provide for current undershoot protection by adjusting the first on time period proportionally to a driving gate rising edge time period, such as by increasing the first on time period proportionally to a driving gate rising edge time period. Such undershoot protection may be provided equivalently by decreasing the current off time period proportionally to a driving gate rising edge time period, such as by decreasing the current off time period proportionally to a driving gate rising edge time period.

In another exemplary embodiment, the method may include generating an error signal as a difference between the second on time period and the first on time period, and then adjusting the on time period proportionally to the error signal.

Referring to Figures 1, 8 and 10, as mentioned above, the I/O interface 170 is utilized for input/output communication, providing appropriate connection to a relevant channel, network or bus; for example, and the interface 170 may provide additional functionality, such as impedance matching, drivers and other functions for a wireline interface, may provide demodulation and analog to digital conversion for a wireless interface, and may provide a physical interface for the memory 175 and controller 125, 225 with other devices. In general, the interface 170 is used to receive and transmit data, depending upon the selected embodiment, such as to receive intensity level selection data, temperature data, and to provide or transmit control signals for current regulation (for controlling an LED driver), and other pertinent information. For example and without limitation, the interface 170 may implement communication protocols such as DMX 512, DALI, I^2C, SPI, etc.

Also as mentioned above, a controller 125, 225 (or, equivalently, a "processor") may be any type of controller or processor, and may be embodied as one or more controllers 125, 225, adapted to perform the functionality discussed herein. As the term controller or processor is used herein, a controller 125, 225 may include use of a single integrated circuit ("IC"), or may include use of a plurality of integrated circuits or other components connected, arranged or grouped together, such as controllers, microprocessors, digital signal processors ("DSPs"), parallel processors, multiple core processors, custom ICs, application specific integrated circuits ("ASICs"), field programmable gate arrays ("FPGAs"), adaptive computing ICs, associated memory (such as RAM, DRAM and ROM), and other ICs and components. As a consequence, as used herein, the term controller (or processor) should be understood to equivalently mean and include a single IC, or arrangement of custom ICs, ASICs, processors, microprocessors, controllers, FPGAs, adaptive computing ICs, or some other grouping of integrated circuits which perform the functions discussed below, with associated memory, such as microprocessor memory or additional RAM, DRAM, SDRAM, SRAM, MRAM, ROM, FLASH, EPROM or E^2PROM. A controller (or processor) (such as controller 125, 225), with its associated memory, may be adapted or

configured (via programming, FPGA interconnection, or hard-wiring) to perform the methodology of the invention, as discussed above and below. For example, the methodology may be programmed and stored, in a controller 125, 225 with its associated memory (and/or memory 175) and other equivalent components, as a set of program instructions or other code (or equivalent configuration or other program) for subsequent execution when the processor is operative (*i.e.,* powered on and functioning). Equivalently, when the controller 125, 225 may implemented in whole or part as FPGAs, custom ICs and/or ASICs, the FPGAs, custom ICs or ASICs also may be designed, configured and/or hard-wired to implement the methodology of the invention. For example, the controller 125, 225 may be implemented as an arrangement of controllers, microprocessors, DSPs and/or ASICs, collectively referred to as a "controller", which are respectively programmed, designed, adapted or configured to implement the methodology of the invention, in conjunction with a memory 175.

The memory 175, which may include a data repository (or database), may be embodied in any number of forms, including within any computer or other machine-readable data storage medium, memory device or other storage or communication device for storage or communication of information, currently known or which becomes available in the future, including, but not limited to, a memory integrated circuit ("IC"), or memory portion of an integrated circuit (such as the resident memory within a controller 125, 225 or processor IC), whether volatile or non-volatile, whether removable or non-removable, including without limitation RAM, FLASH, DRAM, SDRAM, SRAM, MRAM, FeRAM, ROM, EPROM or E^2PROM, or any other form of memory device, such as a magnetic hard drive, an optical drive, a magnetic disk or tape drive, a hard disk drive, other machine-readable storage or memory media such as a floppy disk, a CDROM, a CD-RW, digital versatile disk (DVD) or other optical memory, or any other type of memory, storage medium, or data storage apparatus or circuit, which is known or which becomes known, depending upon the selected embodiment. In addition, such computer readable media includes any form of communication media which embodies computer readable instructions, data structures, program modules or other data in a data signal or modulated signal, such as an electromagnetic or optical carrier wave or other transport mechanism, including any

information delivery media, which may encode data or other information in a signal, wired or wirelessly, including electromagnetic, optical, acoustic, RF or infrared signals, and so on. The memory 175 may be adapted to store various look up tables, parameters, coefficients, other information and data, programs or instructions (of the software of the present invention), and other types of tables such as database tables.

As indicated above, the controller 125, 225 is programmed, using software and data structures of the invention, for example, to perform the methodology of the present invention. As a consequence, the system and method of the present invention may be embodied as software which provides such programming or other instructions, such as a set of instructions and/or metadata embodied within a computer readable medium, discussed above. In addition, metadata may also be utilized to define the various data structures of a look up table or a database. Such software may be in the form of source or object code, by way of example and without limitation. Source code further may be compiled into some form of instructions or object code (including assembly language instructions or configuration information). The software, source code or metadata of the present invention may be embodied as any type of code, such as C, C++, SystemC, LISA, XML, Java, Brew, SQL and its variations (*e.g.*, SQL 99 or proprietary versions of SQL), DB2, Oracle, or any other type of programming language which performs the functionality discussed herein, including various hardware definition or hardware modeling languages (*e.g.,* Verilog, VHDL, RTL) and resulting database files (*e.g.,* GDSII). As a consequence, a "construct", "program construct", "software construct" or "software", as used equivalently herein, means and refers to any programming language, of any kind, with any syntax or signatures, which provides or can be interpreted to provide the associated functionality or methodology specified (when instantiated or loaded into a processor or computer and executed, including the controller 125, 225, for example).

The software, metadata, or other source code of the present invention and any resulting bit file (object code, database, or look up table) may be embodied within any tangible storage medium, such as any of the computer or other machine-readable data storage media, as computer-readable instructions, data structures, program modules or other data, such as discussed above with respect to the memory 175, *e.g.*, a floppy disk, a CDROM, a CD-RW, a DVD, a magnetic hard drive, an

optical drive, or any other type of data storage apparatus or medium, as mentioned above.

Numerous advantages of the present invention for providing power to solid state lighting, such as light emitting diodes, are readily apparent. The exemplary embodiments allow for energizing one or more LEDs, using digital control and low side sensing, enabling low voltage IC implementations. The exemplary apparatus and system embodiments may be implemented with either fixed or variable frequency switching, and may be implemented with either AC or DC power sources. As a digital implementation, the exemplary embodiments may also be implemented at a reduced cost. The exemplary embodiments also provide for precise current control, within any selected tolerance levels. In addition, the exemplary embodiments also eliminate the required RC filtering of the prior art.

For changes in brightness levels, a combination of forward biasing techniques are implemented, which allow for both regulating the intensity of the emitted light while controlling the wavelength emission shift, from either or both the LED response to intensity variation (dimming technique) and due to p-n junction temperatures changes. In addition, the exemplary embodiments of the invention also provide for varying intensity while simultaneously reducing the EMI produced by prior art lighting systems, especially because current steps in the pulse modulation are dramatically reduced or eliminated completely. The exemplary LED controllers are also backwards-compatible with legacy LED control systems, frees the legacy host computer for other tasks, and allows such host computers to be utilized for other types of system regulation. The exemplary current regulator embodiments provide digital control, without requiring external compensation. The exemplary current regulator embodiments also utilize comparatively fewer components, providing reduced cost and size, while simultaneously providing increased efficiency and enabling longer battery life when used in portable devices.

Although the invention has been described with respect to specific embodiments thereof, these embodiments are merely illustrative and not restrictive of the invention. In the description herein, numerous specific details are provided, such as examples of electronic components, electronic and structural connections, materials, and structural variations, to provide a thorough understanding of embodiments of the

present invention. One skilled in the relevant art will recognize, however, that an embodiment of the invention can be practiced without one or more of the specific details, or with other apparatus, systems, assemblies, components, materials, parts, etc. In other instances, well-known structures, materials, or operations are not specifically shown or described in detail to avoid obscuring aspects of embodiments of the present invention. In addition, the various Figures are not drawn to scale and should not be regarded as limiting.

Reference throughout this specification to "one embodiment", "an embodiment", or a specific "embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention and not necessarily in all embodiments, and further, are not necessarily referring to the same embodiment. Furthermore, the particular features, structures, or characteristics of any specific embodiment of the present invention may be combined in any suitable manner and in any suitable combination with one or more other embodiments, including the use of selected features without corresponding use of other features. In addition, many modifications may be made to adapt a particular application, situation or material to the essential scope and spirit of the present invention. It is to be understood that other variations and modifications of the embodiments of the present invention described and illustrated herein are possible in light of the teachings herein and are to be considered part of the spirit and scope of the present invention.

It will also be appreciated that one or more of the elements depicted in the Figures can also be implemented in a more separate or integrated manner, or even removed or rendered inoperable in certain cases, as may be useful in accordance with a particular application. Integrally formed combinations of components are also within the scope of the invention, particularly for embodiments in which a separation or combination of discrete components is unclear or indiscernible. In addition, use of the term "coupled" herein, including in its various forms such as "coupling" or "couplable", means and includes any direct or indirect electrical, structural or magnetic coupling, connection or attachment, or adaptation or capability for such a direct or indirect electrical, structural or magnetic coupling, connection or attachment, including

integrally formed components and components which are coupled via or through another component.

As used herein for purposes of the present invention, the term "LED" and its plural form "LEDs" should be understood to include any electroluminescent diode or other type of carrier injection- or junction-based system which is capable of generating radiation in response to an electrical signal, including without limitation, various semiconductor- or carbon-based structures which emit light in response to a current or voltage, light emitting polymers, organic LEDs, and so on, including within the visible spectrum, or other spectra such as ultraviolet or infrared, of any bandwidth, or of any color or color temperature.

Furthermore, any signal arrows in the drawings/Figures should be considered only exemplary, and not limiting, unless otherwise specifically noted. Combinations of components of steps will also be considered within the scope of the present invention, particularly where the ability to separate or combine is unclear or foreseeable. The disjunctive term "or", as used herein and throughout the claims that follow, is generally intended to mean "and/or", having both conjunctive and disjunctive meanings (and is not confined to an "exclusive or" meaning), unless otherwise indicated. As used in the description herein and throughout the claims that follow, "a", "an", and "the" include plural references unless the context clearly dictates otherwise. Also as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

The foregoing description of illustrated embodiments of the present invention, including what is described in the summary or in the abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed herein. From the foregoing, it will be observed that numerous variations, modifications and substitutions are intended and may be effected without departing from the spirit and scope of the novel concept of the invention. It is to be understood that no limitation with respect to the specific methods and apparatus illustrated herein is intended or should be inferred. It is, of course, intended to cover by the appended claims all such modifications as fall within the scope of the claims.

It is claimed:

1. A method of controlling solid state lighting, the solid state lighting coupled to a switch providing an electrical current path, and the solid state lighting having an electrical current, the method comprising:

turning the switch into an on state;

detecting when the electrical current has reached a predetermined average current level;

detecting when the electrical current has reached a first predetermined current threshold;

determining a first on time period as a duration between detection of a second predetermined current level or turning the switch into the on state and the detection of the predetermined average current level;

determining a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; and

determining an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period.

2. The method of claim 1, further comprising:

when the on time period has elapsed, turning the switch into an off state.

3. The method of claim 2, further comprising:

subsequent to turning the switch into the off state, when a fixed time period has elapsed from having turned the switch into the on state, again turning the switch into the on state and repeating the detection and determination steps.

4. The method of claim 3, further comprising:

generating an error signal as a difference between the second on time period and the first on time period.

5. The method of claim 5, further comprising:

adjusting the on time period proportionally to the error signal.

6. The method of claim 2, further comprising:

when a current off time period has elapsed, turning the switch into the on state and repeating the detection and determination steps.

7. The method of claim 6, further comprising:

determining the current off time period of the switch as a function of the first on time period and the second on time period.

8. The method of claim 6, further comprising:

determining the current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period.

9. The method of claim 6, further comprising:

determining the current off time period of the switch as:

$T_{OFF}(K+1) \approx \frac{2 \bullet T_{ON2}(K) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$, in which $T_{OFF}(K+1)$ is the current off time period, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period.

10. The method of claim 6, further comprising:

determining the current off time period of the switch as:

$T_{OFF}(K+1) \approx \frac{(T_{ON1}(K)_A + T_{ON2}(K)) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$, in which $T_{OFF}(K+1)$ is the current off time period, $T_{ON1}(K)_A$ is a previous first on time period determined using the detection of the second predetermined current level, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period.

11. The method of claim 6, further comprising:

determining the current off time period of the switch as a function of a current first on time period, a previous second on time period, and a previous off time period.

12. The method of claim 6, further comprising:

determining the current off time period of the switch as a function of a current first on time period, a previous first on time period, a previous second on time period, and a previous off time period.

13. The method of claim 6, further comprising:

adjusting the current off time period to provide that the first on time period is substantially equal to the second on time period.

14. The method of claim 6, further comprising:

decreasing the current off time period proportionally to a driving gate rising edge time period.

15. The method of claim 1, further comprising:

decreasing the on time period proportionally to a driving gate falling edge time period and a comparator falling edge time period.

16. The method of claim 1, further comprising:

determining a blanking time interval following turning the switch into the on state.

17. The method of claim 16, further comprising:

ignoring the detection of the second predetermined current threshold, the detection of the predetermined average current level, or the detection of the first predetermined current threshold during the blanking time interval.

18. The method of claim 16, further comprising:

determining the blanking time interval as proportional to a gate rising edge time period and a transient current time period.

19. The method of claim 16, further comprising:

determining the blanking time interval as proportional to a gate rising edge time period and detection of the predetermined average current level.

20. The method of claim 1, further comprising:

adjusting a brightness level of the solid state lighting by using at least two different and opposing electrical biasing techniques.

21. The method of claim 1, further comprising:

adjusting a brightness level of the solid state lighting by using a hysteresis of at least two electrical current amplitude levels and at least two electrical current duty cycle ratios.

22. The method of claim 1, further comprising:

adjusting the second on time period proportionally to a driving gate falling edge time period.

23. The method of claim 1, further comprising:

decreasing the second on time period proportionally to a driving gate falling edge time period and a comparator falling edge time period.

24. The method of claim 1, further comprising:

detecting when the electrical current has reached the second predetermined current threshold.

25. The method of claim 1, wherein the solid state lighting comprises at least one light emitting diode.

26. The method of claim 25, wherein the at least one light emitting diode is coupled to a power converter, and wherein the electrical current detections occur at a comparatively low side of the power converter.

27. The method of claim 1, wherein the solid state lighting comprises a plurality of arrays of a plurality of series-connected light emitting diodes, and each array of the plurality of arrays further coupled to a corresponding switch providing an electrical current path.

28. The method of claim 27, further comprising:

separately determining a corresponding first on time period, a corresponding second on time period, and a corresponding on time period as substantially proportional to the sum of the corresponding first on time period and the corresponding second on time period for each array of the plurality of arrays.

29. The method of claim 28, further comprising:

when the corresponding on time period has elapsed, separately turning the corresponding switch into the off state.

30. The method of claim 29, further comprising:

separately determining a corresponding off time period for each array of the plurality of arrays.

31. The method of claim 29, further comprising:

interleaving the corresponding on time periods of the corresponding switches of the plurality of arrays.

32. The method of claim 27, further comprising:

successively switching electrical current to each array of the plurality of arrays for the corresponding on time period.

33. An apparatus for controlling solid state lighting, the apparatus comprising:

a switch couplable to the solid state lighting;

a first comparator adapted to determine when a switch electrical current has reached a first predetermined current threshold;

a second comparator adapted to determine when the switch electrical current has reached a predetermined average current level; and

a controller coupled to the first comparator and to the second comparator, the controller adapted to turn the switch into an on state and an off state, to determine a first on time period as a duration between either a detection of a second predetermined current threshold or the turning the switch into the on state, and the detection of the predetermined average current level; to determine a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; and to determine an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period.

34. The apparatus of claim 33, wherein the controller is further adapted, when the on time period has elapsed, to turn the switch into an off state.

35. The apparatus of claim 34, wherein the controller is further adapted, subsequent to turning the switch into the off state and when a fixed time period has elapsed from having turned the switch into the on state, to turn the switch into the on state.

36. The apparatus of claim 35, wherein the controller is further adapted to generate an error signal as a difference between the second on time period and the first on time period.

37. The apparatus of claim 36, wherein the controller is further adapted to adjust the on time period proportionally to the error signal.

38. The apparatus of claim 34, wherein the controller is further adapted to determine a current off time period of the switch as a function of the first on time period and the second on time period.

39. The apparatus of claim 34, wherein the controller is further adapted to determine a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period.

40. The apparatus of claim 34, wherein the controller is further adapted to determine a current off time period of the switch as:

$T_{OFF}(K+1) \approx \frac{2 \bullet T_{ON2}(K) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$, in which $T_{OFF}(K+1)$ is the current off time period, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period.

41. The apparatus of claim 34, wherein the controller is further adapted to determine a current off time period of the switch as a function of a current first on time period, a previous second on time period, and a previous off time period.

42. The apparatus of claim 34, wherein the controller is further adapted to determine a current off time period of the switch as a function of a current first on time period, a previous first on time period, a previous second on time period, and a previous off time period.

43. The apparatus of claim 34, wherein the controller is further adapted to adjust a current off time period to provide that the first on time period is substantially equal to the second on time period.

44. The apparatus of claim 33, further comprising:

a gate driver circuit coupled between the controller and the switch, and wherein the controller is adapted to turn the switch on and to turn the switch off by generating a corresponding signal to the gate driver circuit.

45. The apparatus of claim 44, wherein the controller is further adapted to decrease a current off time period proportionally to a rising edge time period of the gate driver circuit.

46. The apparatus of claim 44, wherein the controller is further adapted to decrease the on time period proportionally to a falling edge time period of the gate driver circuit and a falling edge time period of the first comparator.

47. The apparatus of claim 44, wherein the controller is further adapted to adjust the second on time period proportionally to a falling edge time period of the gate driver circuit.

48. The apparatus of claim 44, wherein the controller is further adapted to decrease the second on time period proportionally to a falling edge time period of the gate driver circuit and a falling edge time period of the first comparator.

49. The apparatus of claim 44, wherein the controller is further adapted to determine a blanking time interval following turning the switch into the on state.

50. The apparatus of claim 49, further comprising:

a third comparator adapted to determine when the electrical current has reached the second predetermined current threshold.

51. The apparatus of claim 50, further comprising:

a current sensor coupled to the first, second and third comparators and to the switch.

52. The apparatus of claim 51, wherein the current sensor is embodied as a resistive circuit element.

53. The apparatus of claim 50, wherein the controller is further adapted to determine a current off time period of the switch as:

$$T_{OFF}(K+1) \approx \frac{(T_{ON1}(K)_A + T_{ON2}(K)) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$$, in which $T_{OFF}(K+1)$ is the current off time period, $T_{ON1}(K)_A$ is a previous first on time period determined using the detection of the second predetermined current level, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period.

54. The apparatus of claim 50, wherein the controller is further adapted to ignore the detection of the second predetermined current threshold, the detection of the predetermined average current level, or the detection of the first predetermined current threshold during the blanking time interval.

55. The apparatus of claim 50, wherein the controller is further adapted to determine the blanking time interval as proportional to a rising edge time period of the gate driver circuit and a transient current time period.

56. The apparatus of claim 50, wherein the controller is further adapted to determine the blanking time interval as proportional to a rising edge time period of the gate driver circuit and detection of the predetermined average current level.

57. The apparatus of claim 33, wherein the controller is further adapted to adjust a brightness level of the solid state lighting by generating control signals to a driver circuit for using at least two different and opposing electrical biasing techniques.

58. The apparatus of claim 33, wherein the controller is further adapted to adjust a brightness level of the solid state lighting by generating control signals to a driver circuit to use a hysteresis of at least two electrical current amplitude levels and at least two electrical current duty cycle ratios.

59. The apparatus of claim 33, wherein the solid state lighting comprises at least one light emitting diode.

60. The apparatus of claim 59, wherein the at least one light emitting diode is coupled to a power converter, and wherein the first and second comparators are coupled to a current sensor at a comparatively low side of the power converter.

61. The apparatus of claim 33, wherein the solid state lighting comprises a plurality of arrays of a plurality of series-connected light emitting diodes, each array of the plurality of arrays is further coupled to a corresponding switch, and wherein the controller is further adapted to turn each corresponding switch into an on state and an off state.

62. The apparatus of claim 61, wherein the controller is further adapted to separately determine a corresponding first on time period, a corresponding second on time period, and a corresponding on time period as substantially proportional to the sum of the corresponding first on time period and the corresponding second on time period for each array of the plurality of arrays.

63. The apparatus of claim 62, wherein the controller is further adapted, when the corresponding on time period has elapsed, to separately turn the corresponding switch into an off state.

64. The apparatus of claim 62, wherein the controller is further adapted to separately determine a corresponding off time period for each array of the plurality of arrays.

65. The apparatus of claim 62, wherein the controller is further adapted to interleave the corresponding on time periods of the corresponding switches of the plurality of arrays.

66. The apparatus of claim 62, wherein the controller is further adapted to successively turn into an on state each corresponding switch for each array of the plurality of arrays for the corresponding on time period.

67. The apparatus of claim 33, further comprising:

a reference voltage generator coupled to the first and second comparators and adapted to provide reference voltages respectively corresponding to the first predetermined current threshold and to the predetermined average current level.

68. The apparatus of claim 33, further comprising:

an input-output interface coupled to the controller and adapted to receive an input control signal.

69. The apparatus of claim 33, wherein the apparatus is coupled to a DC-DC power converter receiving a DC input voltage or coupled to AC-DC power converter receiving a rectified AC input voltage.

70. A solid state lighting system, the system couplable to a power source, the system comprising:

a plurality of arrays of series-connected light emitting diodes;

a plurality of switches, a corresponding switch of the plurality of switches coupled to each the array of the plurality of arrays of light emitting diodes;

at least one corresponding first comparator adapted to determine when a corresponding switch electrical current has reached a corresponding first predetermined current threshold;

at least one corresponding second comparator adapted to determine when the corresponding switch electrical current has reached a corresponding predetermined average current level; and

at least one controller coupled to the corresponding first comparator and to the corresponding second comparator, the controller adapted to turn the corresponding switch into an on state and an off state, to determine a corresponding first on time period as a duration between either a detection of a corresponding second predetermined current threshold or the turning the corresponding switch into the on state, and the detection of the corresponding predetermined average current level; to determine a corresponding second on time period as a duration between the detection of the corresponding predetermined average current level and the detection of the corresponding first predetermined current threshold; and to determine a corresponding on time period of the corresponding switch as substantially proportional to a sum of the corresponding first on time period and the corresponding second on time period.

71. The system of claim 70, wherein the at least one controller is further adapted, when the corresponding on time period has elapsed, to turn the corresponding switch into an off state.

72. The system of claim 70, wherein the at least one controller is further adapted, subsequent to turning the corresponding switch into the off state and when a fixed time period has elapsed from having turned the corresponding switch into the on state, to turn the corresponding switch into the on state.

73. The system of claim 72, wherein the at least one controller is further adapted to generate a corresponding error signal as a difference between the corresponding second on time period and the corresponding first on time period.

74. The system of claim 73, wherein the at least one controller is further adapted to adjust the corresponding on time period proportionally to the corresponding error signal.

75. The system of claim 70, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as a function of the corresponding first on time period and the corresponding second on time period.

76. The system of claim 70, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as a function of the corresponding first on time period, the corresponding second on time period, and a corresponding previous off time period.

77. The system of claim 70, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as:

$T_{OFF}(K+1) \approx \frac{2 \bullet T_{ON2}(K) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$, in which $T_{OFF}(K+1)$ is the corresponding current off time period, $T_{ON2}(K)$ is a corresponding previous second on time period, $T_{OFF}(K)$ is a corresponding previous off time period, and $T_{ON1}(K+1)$ is a corresponding current first on time period.

78. The system of claim 70, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as a function of a corresponding current first on time period, a corresponding previous second on time period, and a corresponding previous off time period.

79. The system of claim 70, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as a function of a corresponding current first on time period, a corresponding previous first on time period, a corresponding previous second on time period, and a corresponding previous off time period.

80. The system of claim 70, wherein the at least one controller is further adapted to adjust a corresponding current off time period to provide that the corresponding first on time period is substantially equal to the corresponding second on time period.

81. The system of claim 70, further comprising:

at least one corresponding gate driver circuit coupled between the at least one controller and the corresponding switch, and wherein the at least one controller is adapted to turn the corresponding switch on and to turn the corresponding switch off by generating a corresponding signal to the corresponding gate driver circuit.

82. The system of claim 81, wherein the at least one controller is further adapted to decrease a corresponding current off time period proportionally to a rising edge time period of the at least one corresponding gate driver circuit.

83. The system of claim 81, wherein the at least one controller is further adapted to decrease the corresponding on time period proportionally to a falling edge time period of the at least one corresponding gate driver circuit and a falling edge time period of the at least one first comparator.

84. The system of claim 81, wherein the at least one controller is further adapted to adjust the corresponding second on time period proportionally to a falling edge time period of the at least one corresponding gate driver circuit.

85. The system of claim 81, wherein the at least one controller is further adapted to decrease the corresponding second on time period proportionally to a falling edge time period of the at least one corresponding gate driver circuit and a falling edge time period of the at least one first comparator.

86. The system of claim 81, wherein the at least one controller is further adapted to determine a corresponding blanking time interval following turning the corresponding switch into the on state.

87. The system of claim 86, further comprising:

at least one corresponding third comparator adapted to determine when the corresponding electrical current has reached the corresponding second predetermined current threshold.

88. The system of claim 87, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as:

$$T_{OFF}(K+1) \approx \frac{(T_{ON1}(K)_A + T_{ON2}(K)) \bullet T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$$, in which $T_{OFF}(K+1)$ is the corresponding current off time period, $T_{ON1}(K)_A$ is a corresponding previous first on time period determined using the detection of the second predetermined current level, $T_{ON2}(K)$ is a corresponding previous second on time period, $T_{OFF}(K)$ is a corresponding previous off time period, and $T_{ON1}(K+1)$ is a corresponding current first on time period.

89. The system of claim 87, wherein the at least one controller is further adapted to ignore the detection of the corresponding second predetermined current threshold, the detection of the corresponding predetermined average current level, or the detection of the corresponding first predetermined current threshold during the corresponding blanking time interval.

90. The system of claim 87, wherein the at least one controller is further adapted to determine the corresponding blanking time interval as proportional to a rising edge time period of the at least one corresponding gate driver circuit and a corresponding transient current time period.

91. The system of claim 87, wherein the at least one controller is further adapted to determine the corresponding blanking time interval as proportional to a rising edge time period of the at least one corresponding gate driver circuit and detection of the corresponding predetermined average current level.

92. The system of claim 70, wherein the at least one controller is further adapted to adjust a brightness level of at least one array of the plurality of arrays of light emitting diodes by generating control signals to a driver circuit for the at least one array for using at least two different and opposing electrical biasing techniques.

93. The system of claim 70, wherein the at least one controller is further adapted to adjust a brightness level of at least one array of the plurality of arrays of light emitting diodes by generating control signals to a driver circuit for the at least one array to use a hysteresis of at least two electrical current amplitude levels and at least two electrical current duty cycle ratios.

94. The system of claim 70, wherein each corresponding array of the plurality of arrays of light emitting diodes has a comparatively high voltage node and a comparatively low voltage node, and wherein the at least one first and second comparators are coupled via the corresponding switch to the comparatively low voltage node.

95. The system of claim 70, wherein the at least one controller is further adapted to interleave the corresponding on time periods of the corresponding switches of the plurality of arrays.

96. The system of claim 70, wherein the at least one controller is further adapted to successively turn into an on state each corresponding switch for each array of the plurality of arrays for the corresponding on time period.

97. The system of claim 70, further comprising:

at least one reference voltage generator coupled to the at least one corresponding first and second comparators and adapted to provide corresponding reference voltages respectively for the corresponding first predetermined current threshold and the corresponding predetermined average current level.

98. The system of claim 70, further comprising:

an input-output interface coupled to the at least one controller and adapted to receive an input control signal.

99. The system of claim 70, further comprising:

at least one rectifier couplable to the power source.

100. The system of claim 70, wherein the power source provides a DC input voltage or a rectified AC input voltage.

101. The system of claim 70, wherein when the power source provides a rectified AC input voltage, an electrical current through a corresponding switch is substantially zero when the rectified AC input voltage is below a selected or predetermined threshold.

102. The system of claim 70, wherein when the power source provides a rectified AC input voltage, the at least one controller is in an off state when the rectified AC input voltage is below a selected or predetermined threshold.

103. An apparatus for controlling solid state lighting, the apparatus comprising:

a switch couplable to the solid state lighting;

a current sensor coupled to the switch;

a first comparator adapted to determine when a switch electrical current has reached a first predetermined current threshold;

a second comparator adapted to determine when the switch electrical current has reached a predetermined average current level;

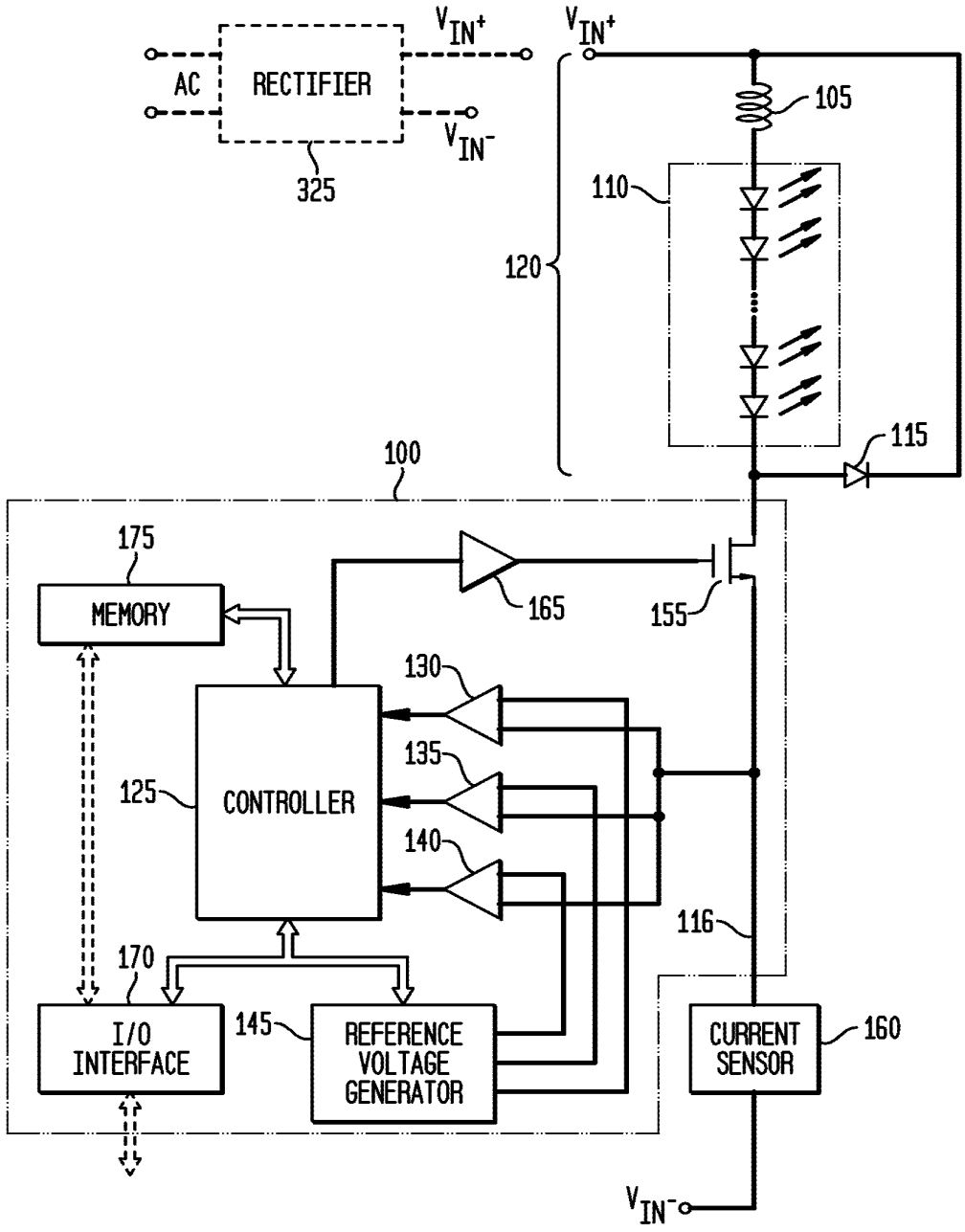
a third comparator adapted to determine when the switch electrical current has reached a second predetermined current threshold;

a reference voltage generator coupled to the first, second and third comparators and adapted to provide reference voltages respectively corresponding to the first predetermined current threshold, the second predetermined current threshold; and to the predetermined average current level;

an input-output interface adapted to receive an input control signal; and

a controller coupled to the first, second and third comparators and to the input-output interface, the controller adapted to turn the switch into an on state and an off state, to determine a first on time period as a duration between either the detection of a second predetermined current threshold or the turning the switch into the on state, and the detection of the predetermined average current level; to determine a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; to determine an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period; to turn the switch into an off state when the on time period has elapsed; and to determine a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period.

FIG. 1


150
AC
RECTIFIER
325
V_{IN}^+
V_{IN}^-
V_{IN}^+
105
110
120
115
100
175
MEMORY
165
155
130
135
140
125
CONTROLLER
116
170
I/O INTERFACE
145
REFERENCE VOLTAGE GENERATOR
CURRENT SENSOR
160
V_{IN}^-

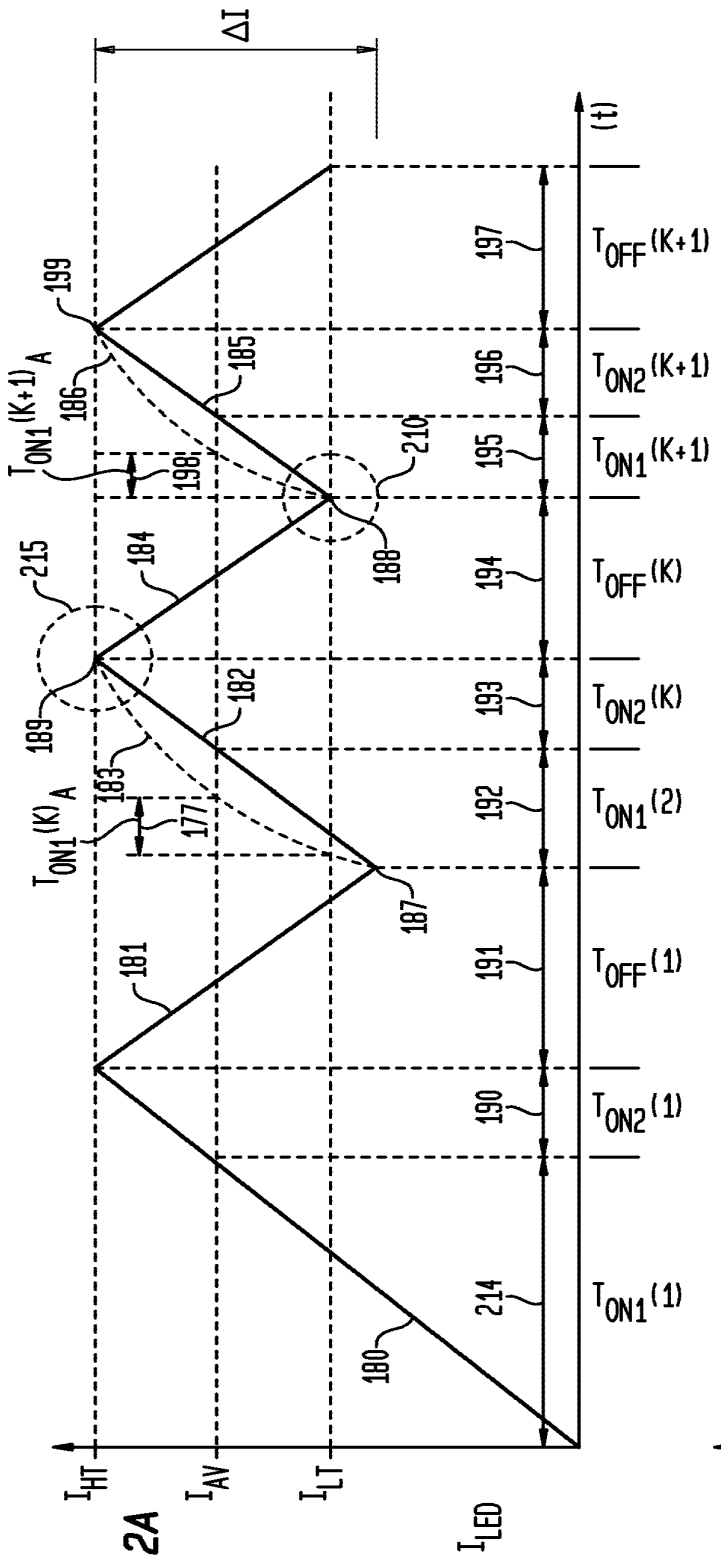

ΔI
(t)
199
185
186
$T_{ON1}^{(K+1)}$ A
198
210
188
215
184
189
182
183
177
$T_{ON1}^{(K)}$ A
187
181
180
214
197
196
195
194
193
192
191
190
$T_{OFF}(K+1)$
$T_{ON2}(K+1)$
$T_{ON1}(K+1)$
$T_{OFF}(K)$
$T_{ON2}(K)$
$T_{ON1}(2)$
$T_{OFF}(1)$
$T_{ON2}(1)$
$T_{ON1}(1)$
I_{HT}
I_{AV}
I_{LT}
I_{LED}

FIG. 2A

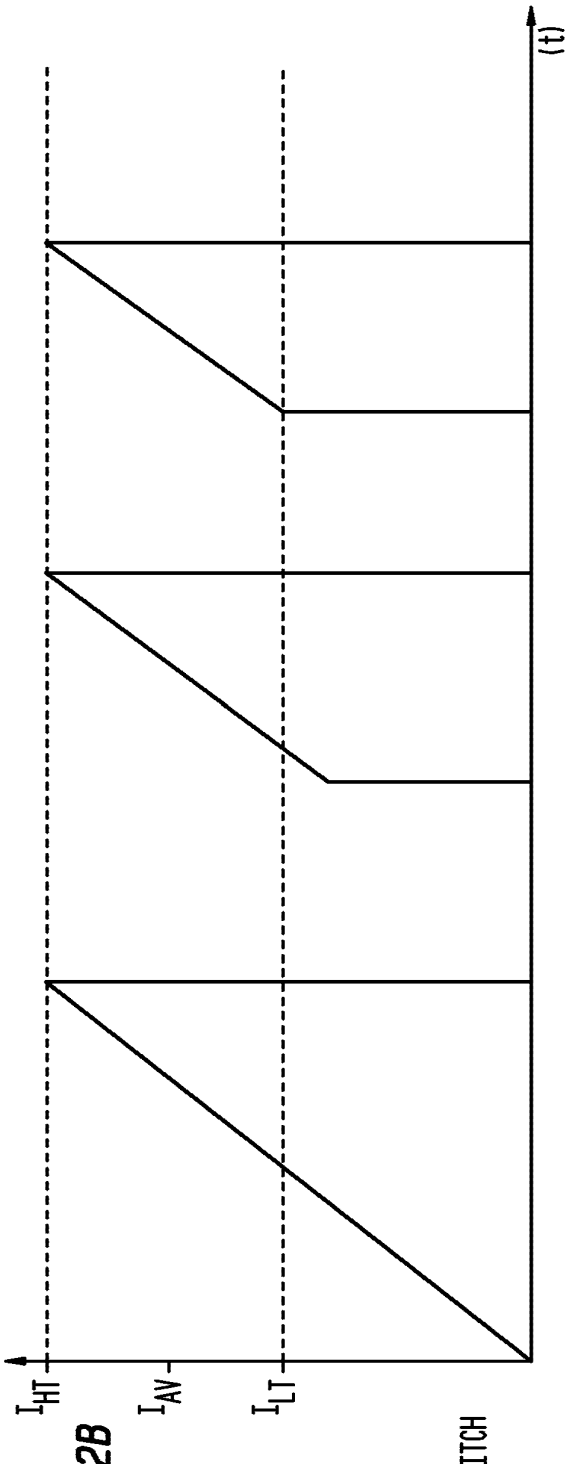

(t)
I_{HT}
I_{AV}
I_{LT}
I_{SWITCH}

FIG. 2B

FIG. 3

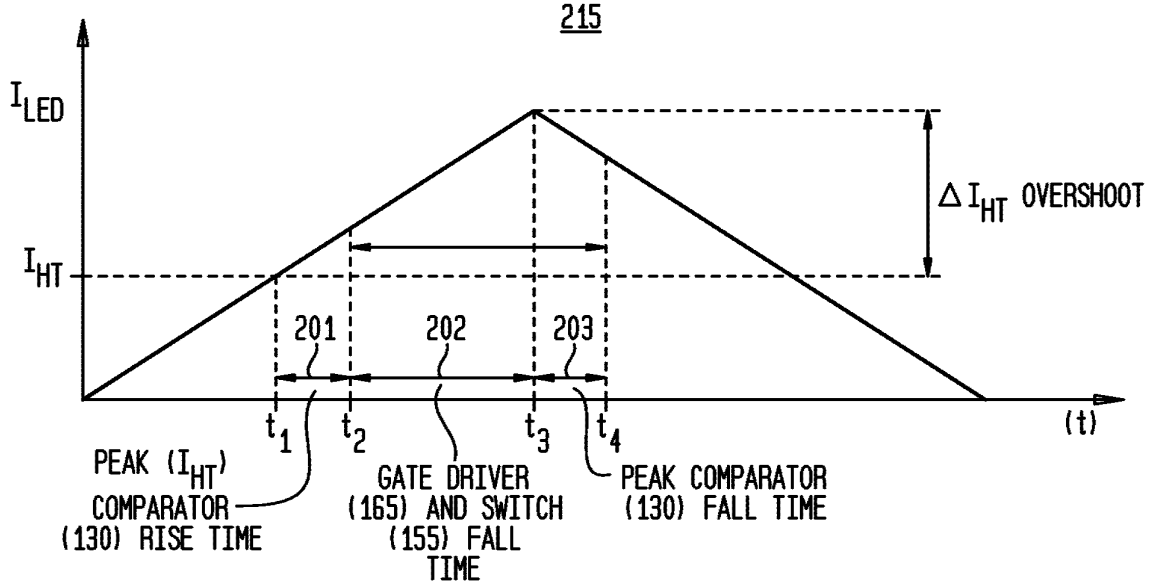

215
I_{LED}
I_{HT}
ΔI_{HT} OVERSHOOT
201
202
203
t_1
t_2
t_3
t_4
(t)
PEAK (I_{HT}) COMPARATOR (130) RISE TIME
GATE DRIVER (165) AND SWITCH (155) FALL TIME
PEAK COMPARATOR (130) FALL TIME

FIG. 4

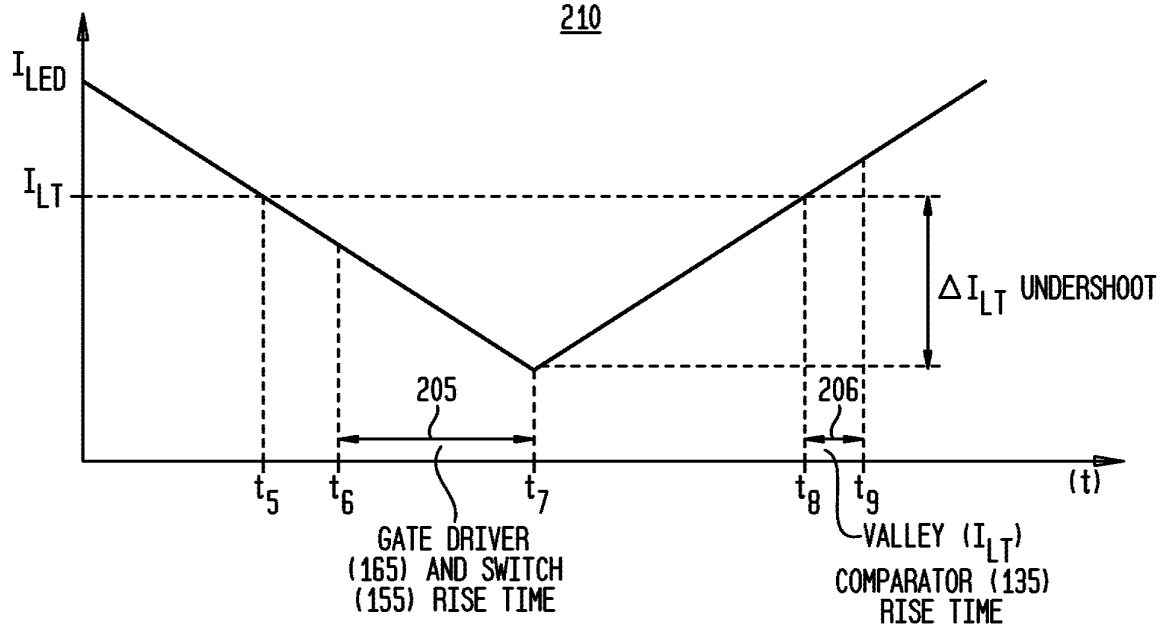

210
I_{LED}
I_{LT}
ΔI_{LT} UNDERSHOOT
205
206
t_5
t_6
t_7
t_8
t_9
(t)
GATE DRIVER (165) AND SWITCH (155) RISE TIME
VALLEY (I_{LT}) COMPARATOR (135) RISE TIME

FIG. 5

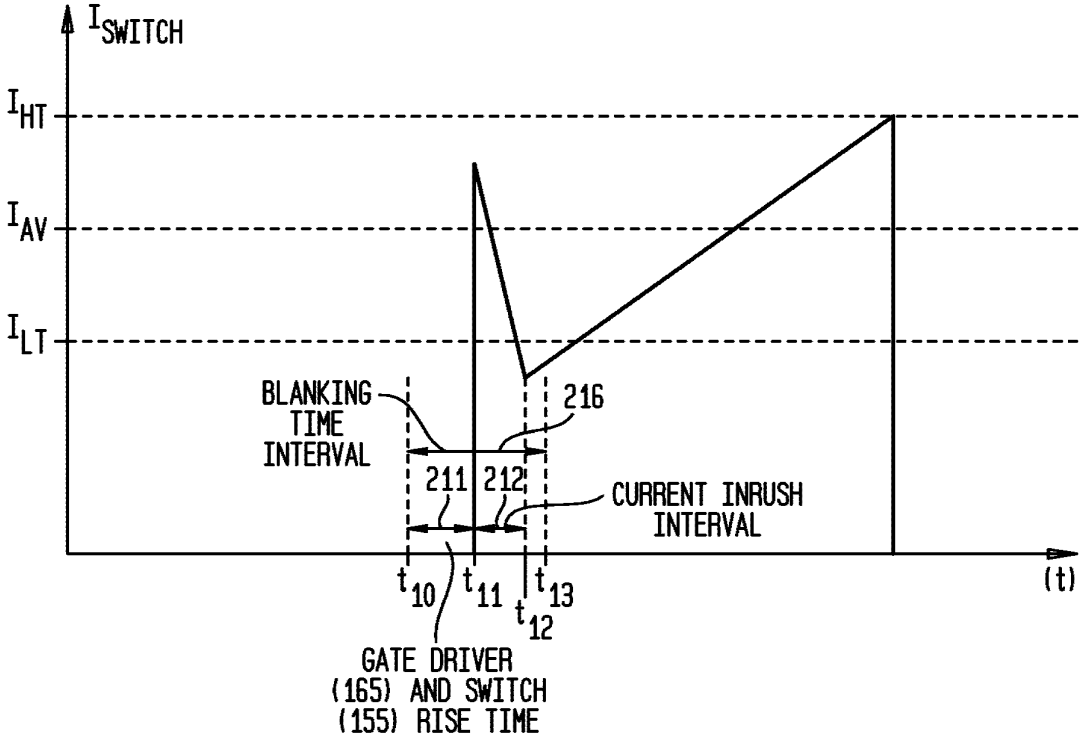

I_SWITCH
I_HT
I_AV
I_LT
BLANKING TIME INTERVAL
216
211
212
CURRENT INRUSH INTERVAL
t_10
t_11
t_12
t_13
(t)
GATE DRIVER (165) AND SWITCH (155) RISE TIME

FIG. 6

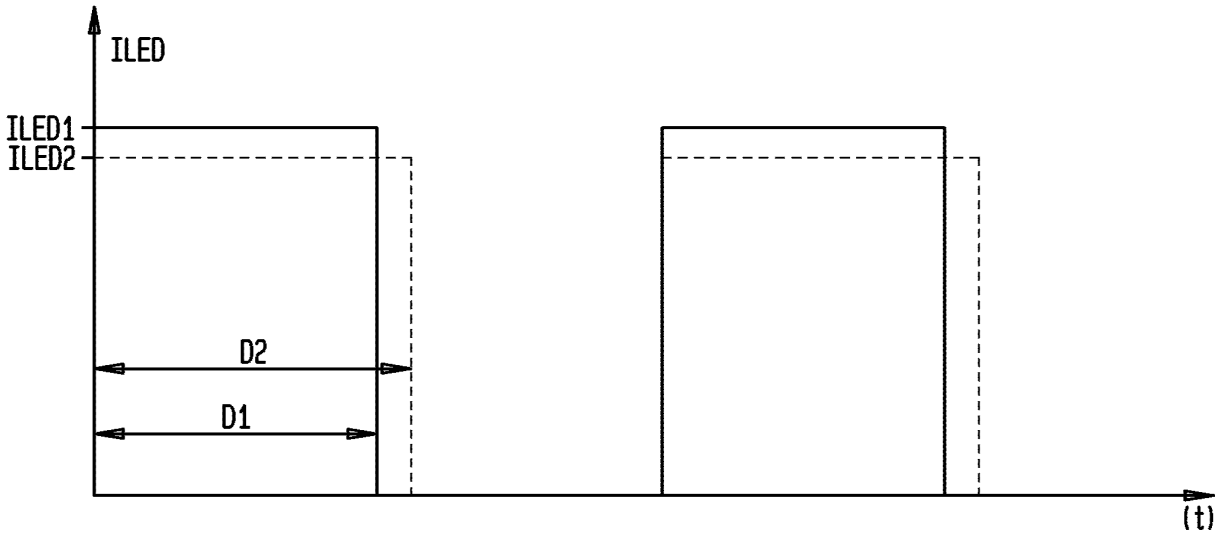

ILED
ILED1
ILED2
D2
D1
(t)

FIG. 7

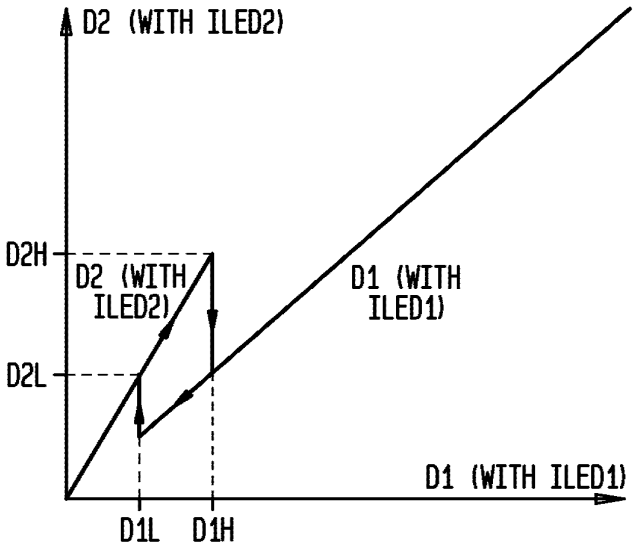

D2 (WITH ILED2)
D2H
D2 (WITH ILED2)
D1 (WITH ILED1)
D2L
D1 (WITH ILED1)
D1L
D1H

FIG. 8

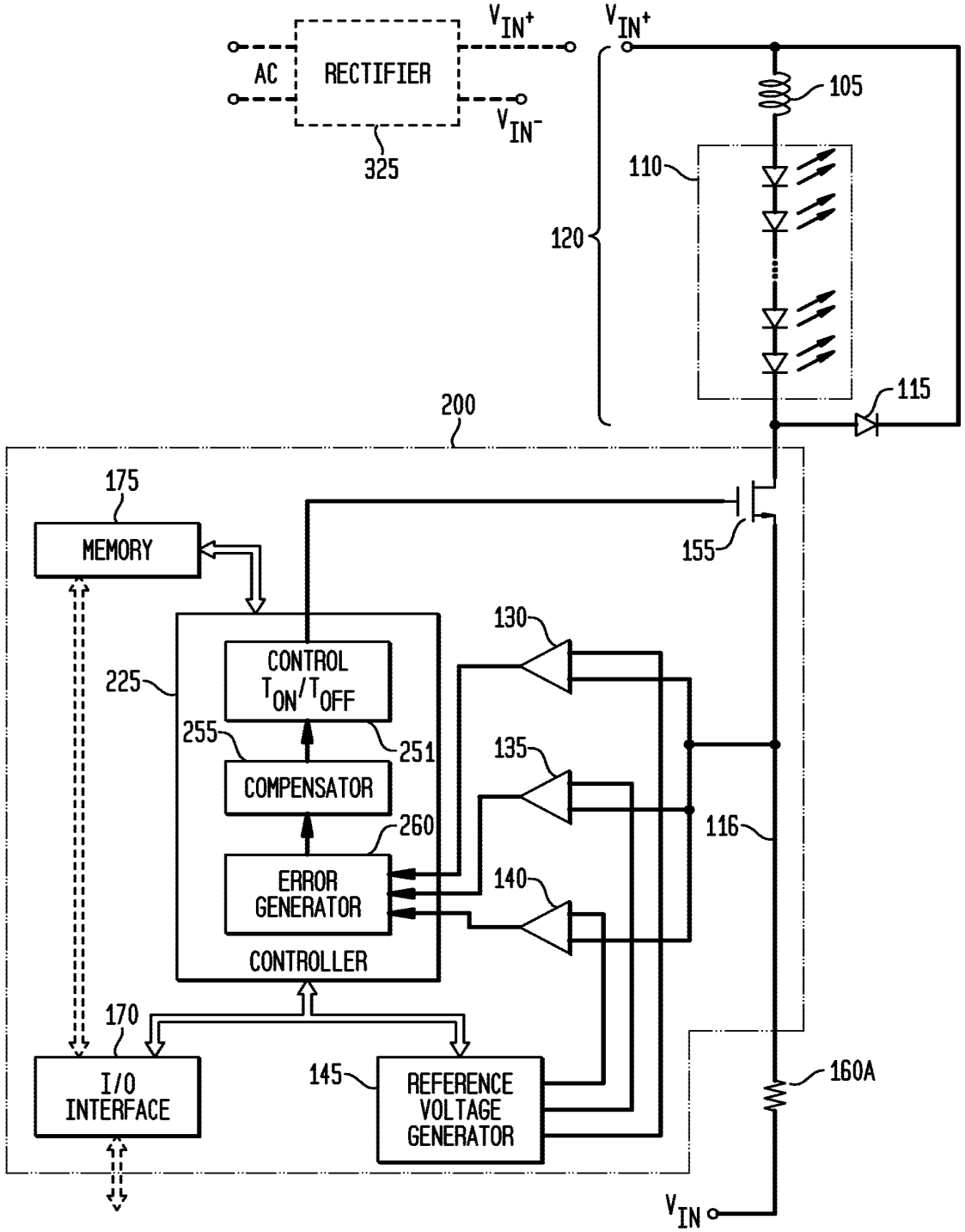

250
AC
RECTIFIER
V_{IN}^+
V_{IN}^-
325
V_{IN}^+
105
110
120
115
200
175
MEMORY
155
130
225
CONTROL
T_{ON}/T_{OFF}
255
251
135
COMPENSATOR
116
260
ERROR
GENERATOR
140
CONTROLLER
170
I/O
INTERFACE
145
REFERENCE
VOLTAGE
GENERATOR
160A
V_{IN}

FIG. 9

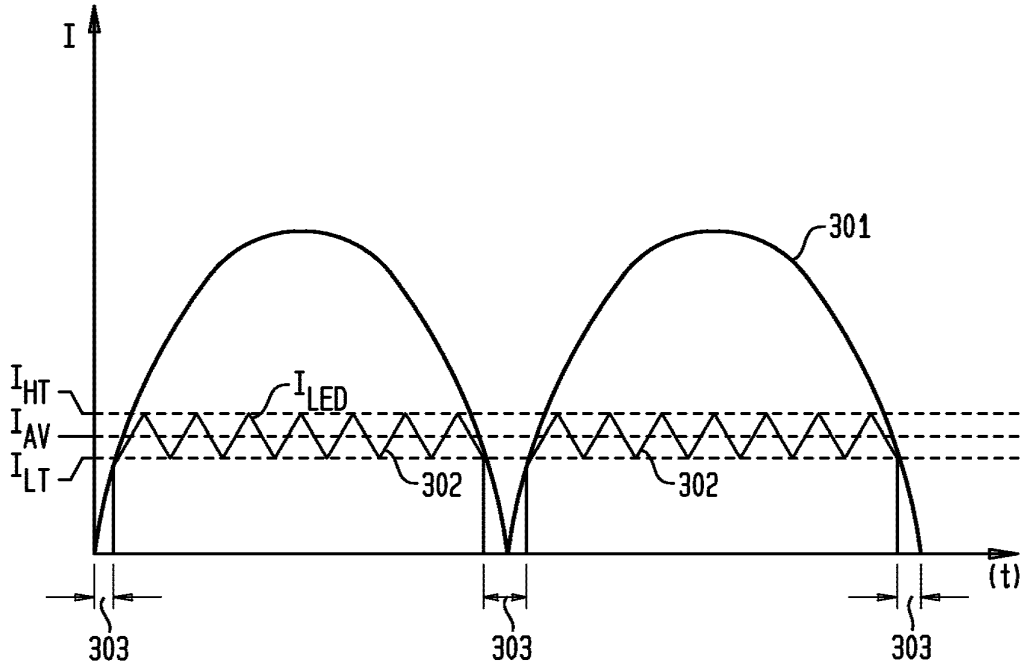


FIG. 10

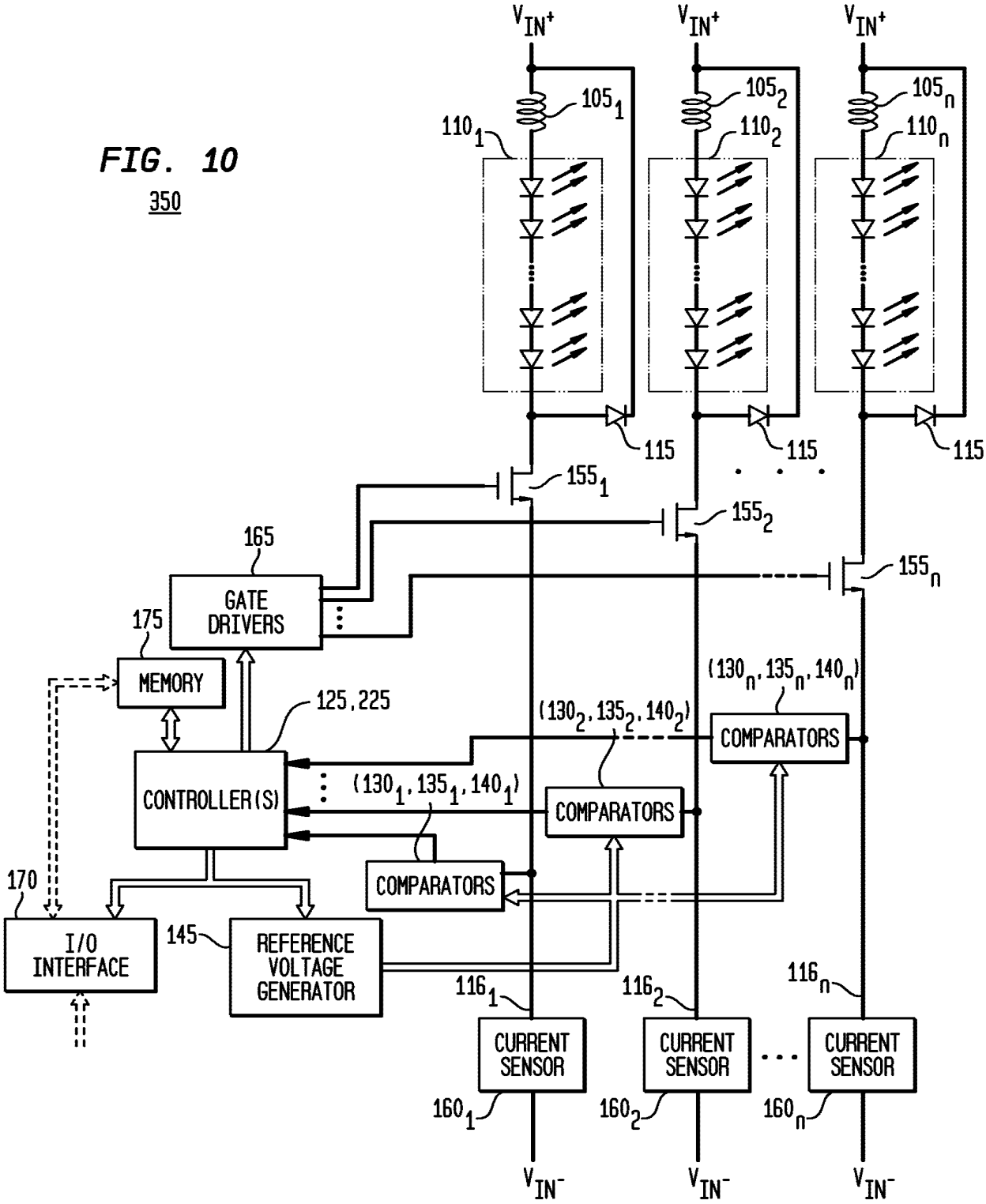

350
V_{IN}^+
105_1
110_1
105_2
110_2
105_n
110_n
115
155_1
155_2
155_n
165
GATE DRIVERS
175
MEMORY
125,225
CONTROLLER(S)
$(130_1, 135_1, 140_1)$
$(130_2, 135_2, 140_2)$
$(130_n, 135_n, 140_n)$
COMPARATORS
170
I/O INTERFACE
145
REFERENCE VOLTAGE GENERATOR
116_1
116_2
116_n
CURRENT SENSOR
160_1
160_2
160_n
V_{IN}^-

FIG. 11

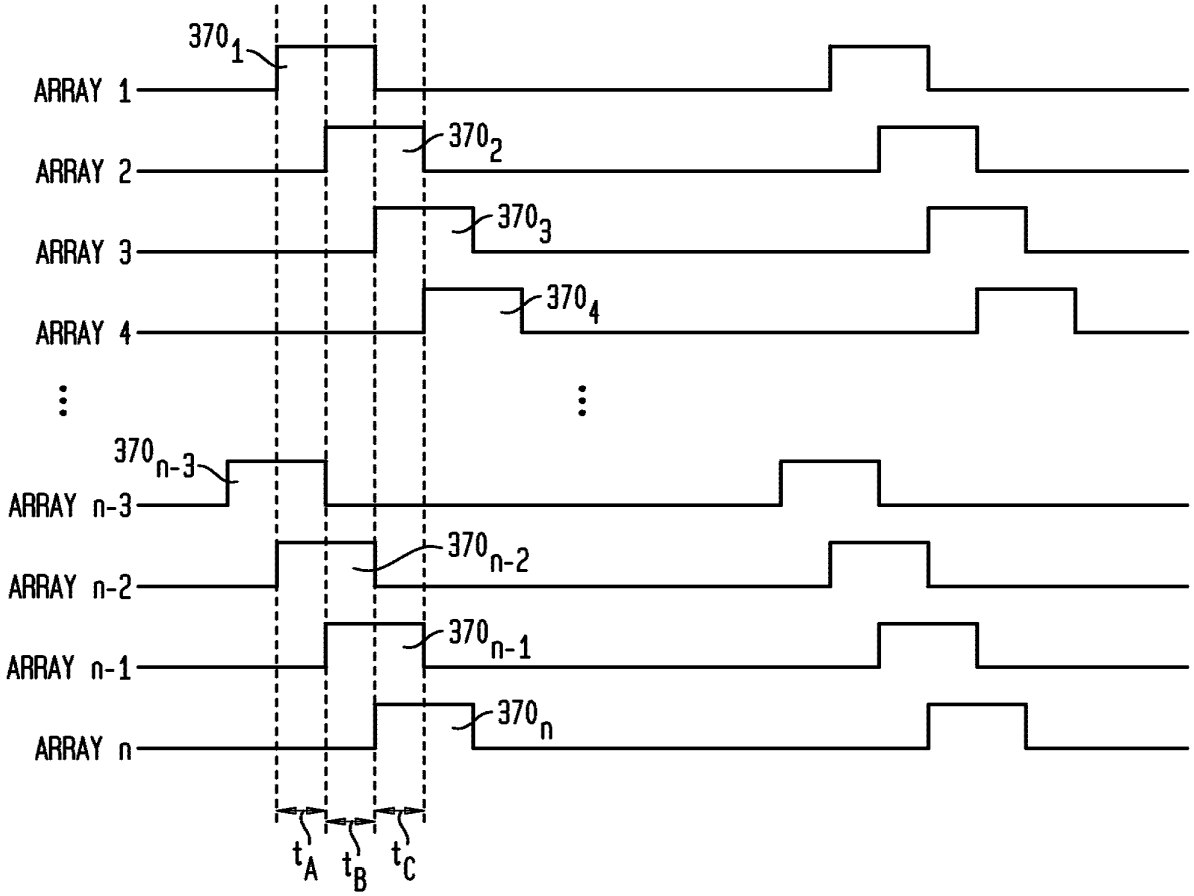
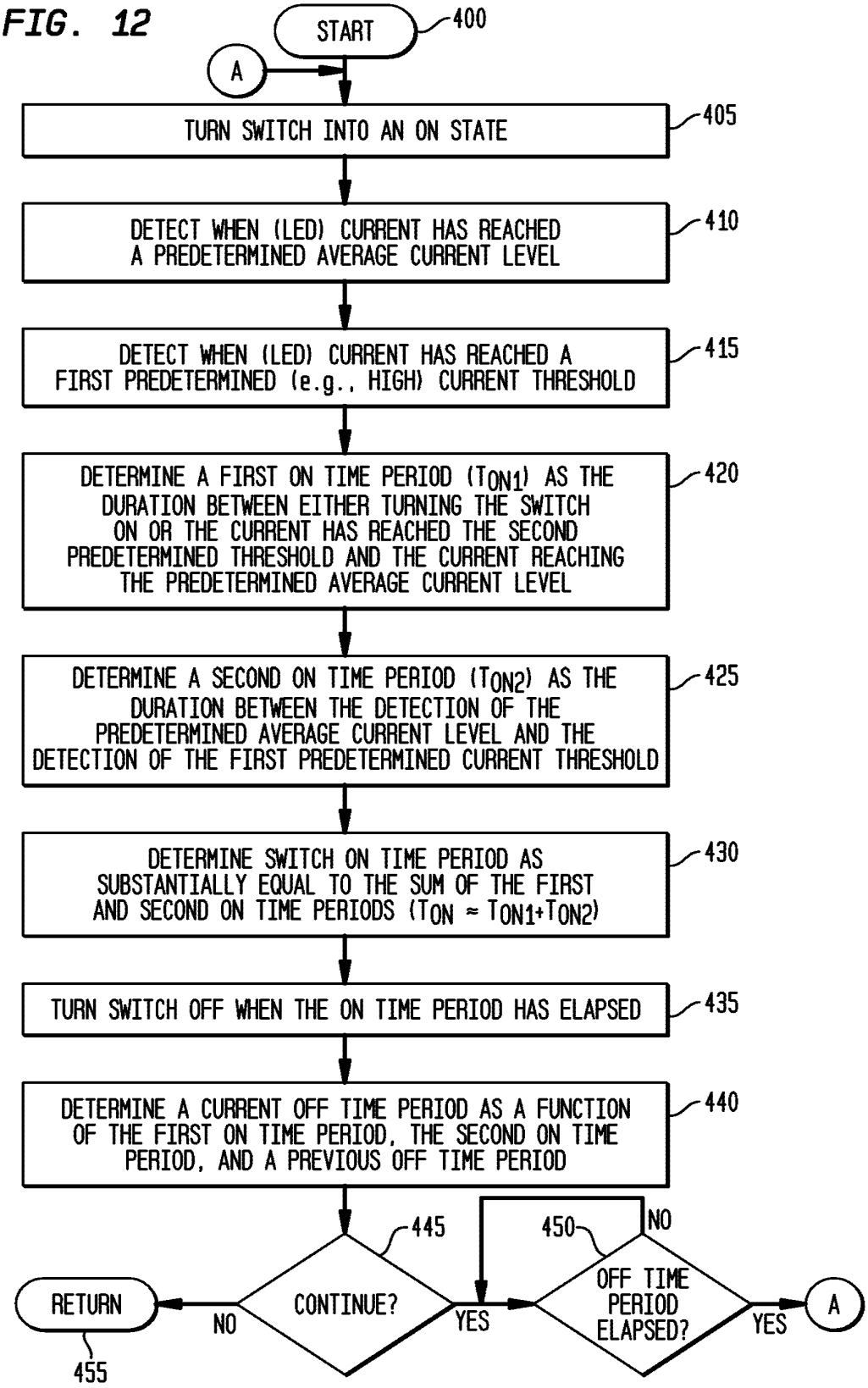

370 1
ARRAY 1
370 2
ARRAY 2
370 3
ARRAY 3
370 4
ARRAY 4
370 n-3
ARRAY n-3
370 n-2
ARRAY n-2
370 n-1
ARRAY n-1
370 n
ARRAY n
t A
t B
t C

FIG. 12


START
400
A
TURN SWITCH INTO AN ON STATE
405
DETECT WHEN (LED) CURRENT HAS REACHED A PREDETERMINED AVERAGE CURRENT LEVEL
410
DETECT WHEN (LED) CURRENT HAS REACHED A FIRST PREDETERMINED (e.g., HIGH) CURRENT THRESHOLD
415
DETERMINE A FIRST ON TIME PERIOD (T_{ON1}) AS THE DURATION BETWEEN EITHER TURNING THE SWITCH ON OR THE CURRENT HAS REACHED THE SECOND PREDETERMINED THRESHOLD AND THE CURRENT REACHING THE PREDETERMINED AVERAGE CURRENT LEVEL
420
DETERMINE A SECOND ON TIME PERIOD (T_{ON2}) AS THE DURATION BETWEEN THE DETECTION OF THE PREDETERMINED AVERAGE CURRENT LEVEL AND THE DETECTION OF THE FIRST PREDETERMINED CURRENT THRESHOLD
425
DETERMINE SWITCH ON TIME PERIOD AS SUBSTANTIALLY EQUAL TO THE SUM OF THE FIRST AND SECOND ON TIME PERIODS ($T_{ON} \approx T_{ON1}+T_{ON2}$)
430
TURN SWITCH OFF WHEN THE ON TIME PERIOD HAS ELAPSED
435
DETERMINE A CURRENT OFF TIME PERIOD AS A FUNCTION OF THE FIRST ON TIME PERIOD, THE SECOND ON TIME PERIOD, AND A PREVIOUS OFF TIME PERIOD
440
445
CONTINUE?
NO
YES
RETURN
455
450
OFF TIME PERIOD ELAPSED?
NO
YES
A

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/76552

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G05F 1/00 (2008.04)
USPC - 315/291
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 315/291

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 368/189, 315/291,149,150,156,159

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO WEST (PGPB, USPT, EPAB, JPAB); Google Scholar;
Search Terms Used: predetermined, current level, light control, controlling, LED, array, detect, current, period, time, phase, duration, interval, on time, circuit.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/0024213 A1 (Shteynberg et al.) 1 February 2007 Especially (para [0007]-[0009],[0012],[0013],[0017]-[0019],[0047]-[0049],[0052],[0053],[0057]-[0059], [0065],[0066], [0072],[0075], para [0081] - Fig. 14, Fig. 2)	1-103
A	US 2007/0194210 A1 (Lee et al.) 23 August 2007	1-103
A	US 7081722 B1 (Huynh et al.) 25 July 2006	1-103
A	US 6731079 B2 (Anderson et al.) 4 May 2004 (04.05.2004)	1-103

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 November 2008 (05.11.2008)	19 NOV 2008

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)

Electronic Acknowledgement Receipt

EFS ID:	13893414
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	26123
Filer:	Jeffrey Wong/Tara Charbonneau
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	02-OCT-2012
Filing Date:	22-MAR-2011
Time Stamp:	16:06:35
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PAT_67545W-2_IDS.PDF	612770 9ffb5e084334d27fb3b9beea7b82818ec874d953	no	4

Warnings:	
Information:	

2	Non Patent Literature	PAT_67545W-2_NPL_1.pdf	522150 ed66fe6d169dbf8a7b0356f11320536c3e06f167	no	3
Warnings:					
Information:					
3	Foreign Reference	WO2009039112.pdf	3122535 6f012efcdc88fdc607f362f1f2f8decf6649ae89	no	70
Warnings:					
Information:					
			Total Files Size (in bytes):	4257455	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13059336
Filing Date	2011-02-16
First Named Inventor	TIKKANEN, David
Art Unit	2821
Examiner Name	
Attorney Docket Number	PAT 67545W-2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8197079		2012-06-12	RUUD ET AL	

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13059336
	Filing Date	2011-02-16
	First Named Inventor	TIKKANEN, David
	Art Unit	2821
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13059336
Filing Date	2011-02-16
First Named Inventor	TIKKANEN, David
Art Unit	2821
Examiner Name	
Attorney Docket Number	PAT 67545W-2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2012-08-31
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	13634167
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	26123
Filer:	Jeffrey Wong/Stacy Duke
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	31-AUG-2012
Filing Date:	22-MAR-2011
Time Stamp:	10:04:30
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PAT-67545W-2-IDS-form.PDF	761973 2affbc15f07e436efe92c2c1fc44834ca6e85b69	no	4

Warnings:	
Information:	

Total Files Size (in bytes):	761973

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	TIKKANEN, David; NEUDORF, Jason; LYONS, Steven; SCOTT, Todd, William; HATHAWAY, Kyle, Grahame; JANSEN, David, Wainesworth
Serial No.:	13/059,336
Filed:	September 17, 2009
Title:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
Group:	2821
Examiner:	
Attorney Ref.:	PAT 67545W-2

August 3, 2012

MAIL STOP AMENDMENT

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22314-1450
U.S.A.

Dear Sir:

PRELIMINARY AMENDMENT

Please amend the above identified application as follows:

Amendments to the Specification begin on page **2** of this paper.

Amendments to the Drawings begin on page **5** of this paper and include the attached replacement sheets.

Remarks/Arguments begin on page **6** of this paper.

Amendments to the Specification

Please replace the 4th paragraph, starting at line 18, on page 5 with the following amended paragraph:

Turning to Figure 3, a block diagram of another embodiment of the LED dimmer is shown. The LED dimmer 10 includes an inrush current limit 40, or inrush current limit circuit, which receives power from an AC power source or supply 42, located external to the dimmer 10. The inrush circuit 40 is connected to a Power Factor Correction (PFC) Boost 44 which, in turn, is connected to a DC/DC Converter 46, or power conversion stage. The converter 46 is connected to an Output Voltage ~~Base~~ bus 48 which is connected to a power limiter 50. The inrush circuit 40, the PFC boost 44, the DC/DC converter 46, the Output Voltage Base bus 48 and the power limit 50 can be seen as a power circuit 47. Although only one power limit 50 is shown, it will be understood that there could be multiple power limits. The power limiter 50 is connected to a set of output current drivers 52, whereby each of the output current drivers 52 has an associated in-circuit serial programming (ICSP) port 54. The output of the output current drivers 52 is connected to individual Organic Light-Emitting Diodes (OLED)/Light-Emitting Diodes (LED) loads 56, further referred to as LED loads.

Please replace the 1st paragraph, starting at line 1, on page 6 with the following amended paragraph:

Along with the above-identified components and circuitry, the dimmer 10 further includes a primary digital controller 58 which is connected to an auxiliary power source 60 and an ICSP Port 62. The primary digital controller 58 is further connected, via an isolated communication bus ~~66~~ 61 to a secondary digital controller 64, which receives power from the auxiliary power source 60. An ICSP port 68 is also connected to the secondary digital controller 64.

Please replace the 3rd paragraph, starting at line 13, on page 6 with the following amended paragraph:

As will be understood, not all of the components or connections of the LED dimmer 10 required for operation are shown as they will be understood by one skilled in the art. For

instance, the dimmer 10 can also include an EMI filter and a bridge rectifier. With respect to connections, it will be understood that the primary digital controller 58 can also be connected to the PFC boost 44, the inrush current limit 40 and the DC/DC ~~controller~~ converter 46 while the secondary digital controller 64 can be connected to the output voltage bus 48, the power limit 50 and the output current drivers 52.

Please replace the 4th paragraph, starting at line 20, on page 6 with the following amended paragraph:

In operation, the PFC Boost 44 and DC/DC Converter 46 are controlled by the primary side digital controller 58 while the secondary digital controller 64 monitors the output voltage bus 48 and provides digital feedback control information via isolated communication bus ~~66~~ 61 to regulate the output voltage bus 48. Secondary digital controller 64 also translates dimming and/or color mixing information from the external transmitter 76 into LED control information for the output current drivers 52. The primary 58 and secondary 64 digital controllers and output current drivers 52 have an associated programming port for further configuring the LED dimmer 10.

Please replace the 3rd paragraph, starting at line 9, on page 7 with the following amended paragraph:

Turning to Figure 5, an embodiment of an improved inrush current limit 40 is shown. An EMI filter 82 is connected between the power supply and the current limit 40 and is connected directly to the PFC boost 44 and via the current limit 40. The current limit 40 includes a thermistor 84, a relay or relay contact ~~coil~~ 86 and a switch 59. The relay ~~coil~~ contact 86 is connected in parallel with the thermistor 84. A typical relay coil requires greater energy to close the contacts than is required with the currently described limiter 40 to maintain the contacts in a closed position since less holding force is required. After the relay contacts have been closed by applying a voltage of 12 Vdc, modulation of the relay coil voltage can be initiated by the primary controller 58 to effectively reduce the average voltage across the coil to approximately 5 volts versus a DC voltage of 12V, reducing power consumption. It should be noted that the pulse duty cycle and frequency can also be changed to improve or optimize performance.

Please replace the 6th paragraph, starting at line 20, on page 9 with the following amended paragraph:

The current source 92 preferably includes ancillary circuitry for operation and comprises a buck topology power stage with hysteretic control. The current sense 94 provides a digital feedback loop for each current source 92. In the preferred embodiment, the current source 92 is a buck circuit topology however other embodiments can include topologies such as boost, buck-boost, or single ended primary ~~redactor~~ inductor converter ~~converter~~ (SEPIC).

Please replace the 2nd paragraph, starting at line 3, on page 14 with the following amended paragraph:

Furthermore, the communication interface 74 can be adapted to have one or more 0 - 10 Vdc signal voltages control an associated group of one or more output current drivers in ~~zone~~ zonal dimming applications. An optional master 0 - 10 Vdc signal voltage could be able to simultaneously control all of the individual groups of output current drivers.

Amendments to the Drawings

The attached sheets of drawings includes changes to Figs. 9 - 11. The sheets, which include Figs. 9 - 11, replace the original sheets including Figs. 9 – 11.

REMARKS / ARGUMENTS

The figures and description have been amended to correct typographical errors. No new matter has been added.

For the above reasons, it is respectfully submitted that the application is now in condition for allowance, which is requested. If there are any outstanding issues, the Examiner is invited to contact the undersigned to discuss this matter further.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments, to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,
TIKKANEN, David et al.

By: /Jeffrey W. Wong/
Jeffrey W. Wong
Registration No. 46,414
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Electronic Acknowledgement Receipt

EFS ID:	13415409
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	26123
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	03-AUG-2012
Filing Date:	22-MAR-2011
Time Stamp:	15:34:18
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Drawings-only black and white line drawings	pat-67545w-2-drawings.pdf	36767 7655d16dd01b9ad4f6d19b7a2c7de27323d907c6	no	3

Warnings:	
Information:	

2		pat-67545w-2-pa.pdf	89325 76bf52219608e64761b0aee01056ee14d1b442d0	yes	6

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Preliminary Amendment	1	1
Specification	2	4
Drawings-only black and white line drawings	5	5
Applicant Arguments/Remarks Made in an Amendment	6	6

Warnings:

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Total Files Size (in bytes):	126092

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

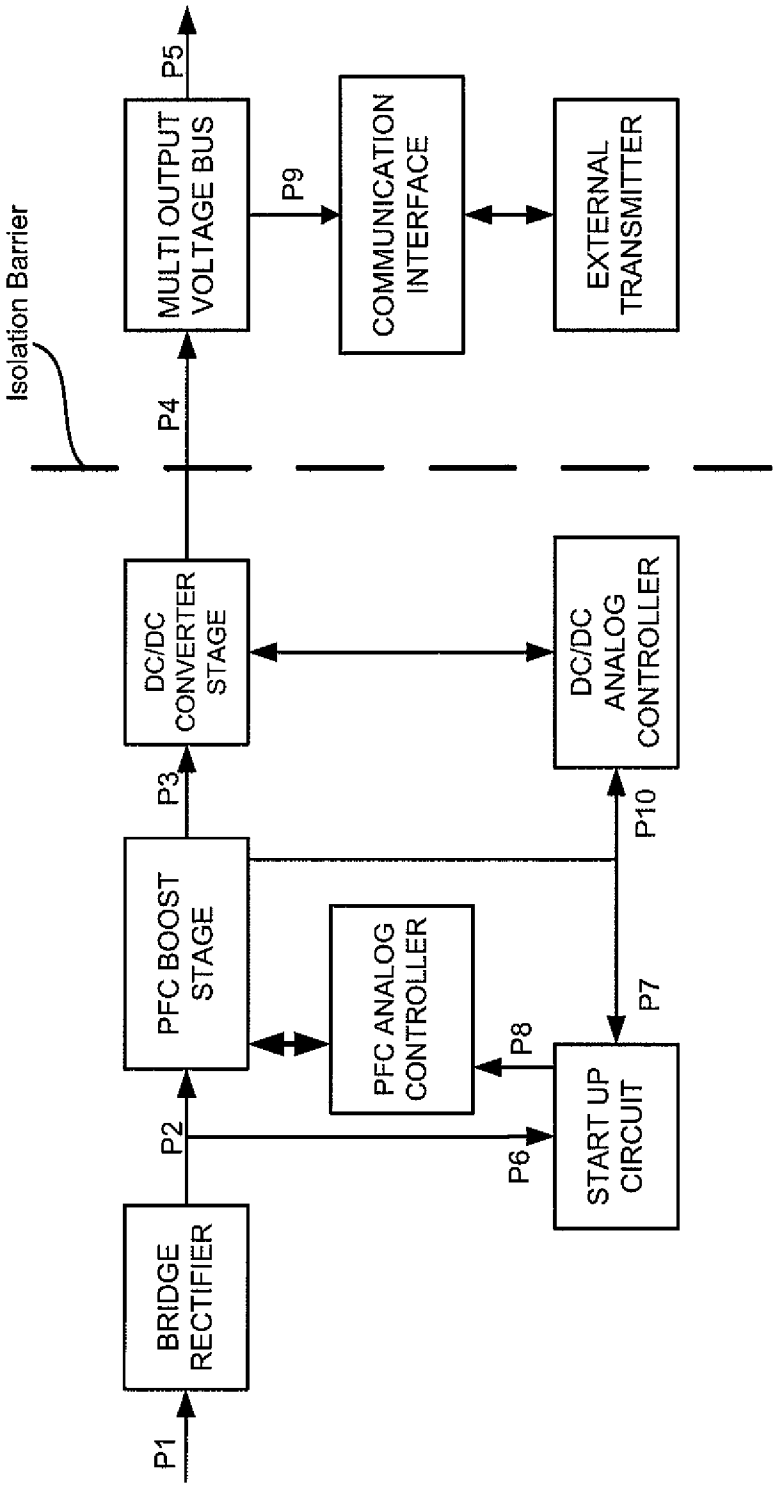


FIGURE 9 (PRIOR ART)

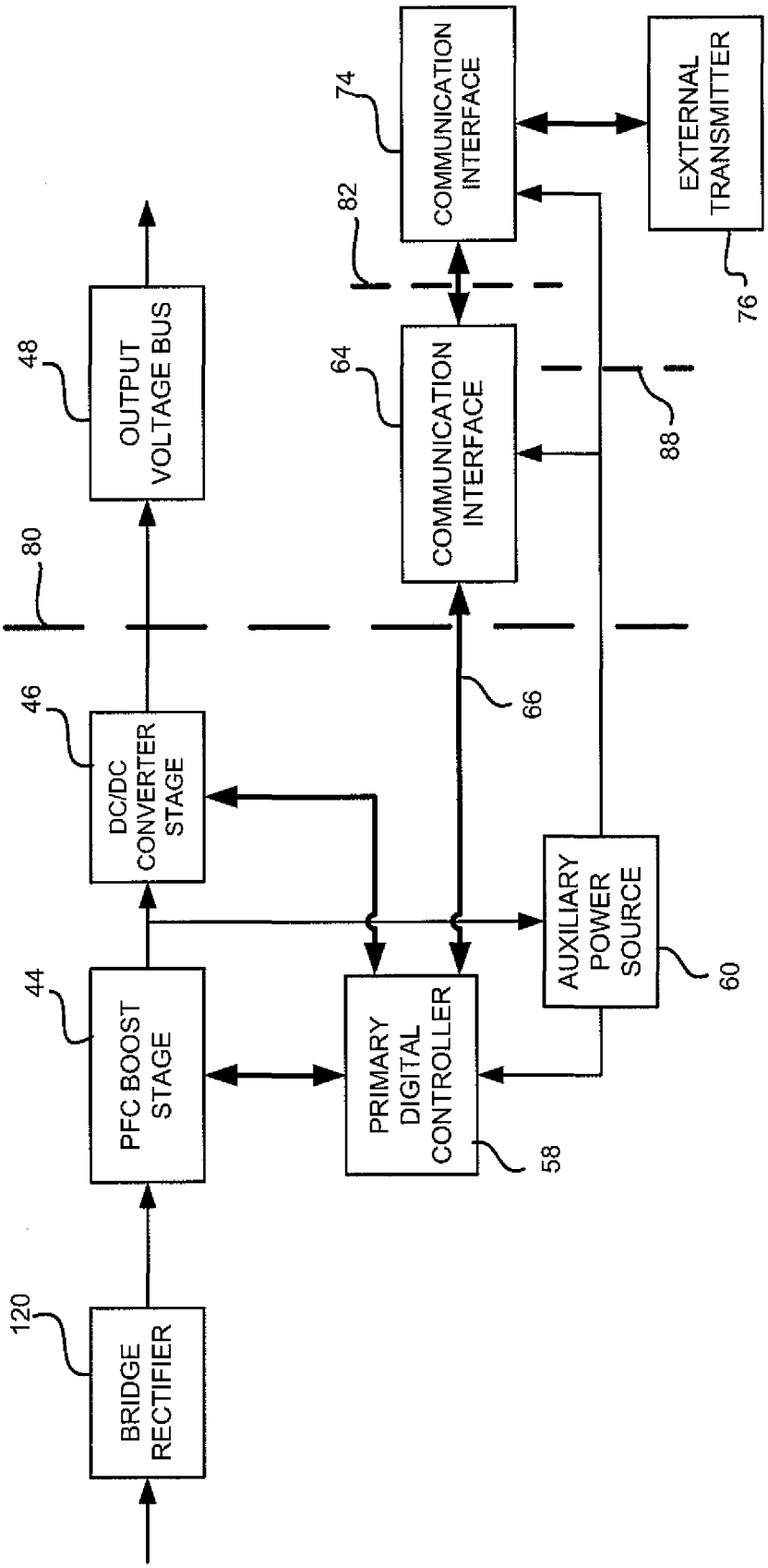

BRIDGE RECTIFIER
120
PFC BOOST STAGE
44
DC/DC CONVERTER STAGE
46
OUTPUT VOLTAGE BUS
48
80
PRIMARY DIGITAL CONTROLLER
58
AUXILIARY POWER SOURCE
60
66
COMMUNICATION INTERFACE
64
82
88
COMMUNICATION INTERFACE
74
EXTERNAL TRANSMITTER
76

FIGURE 10

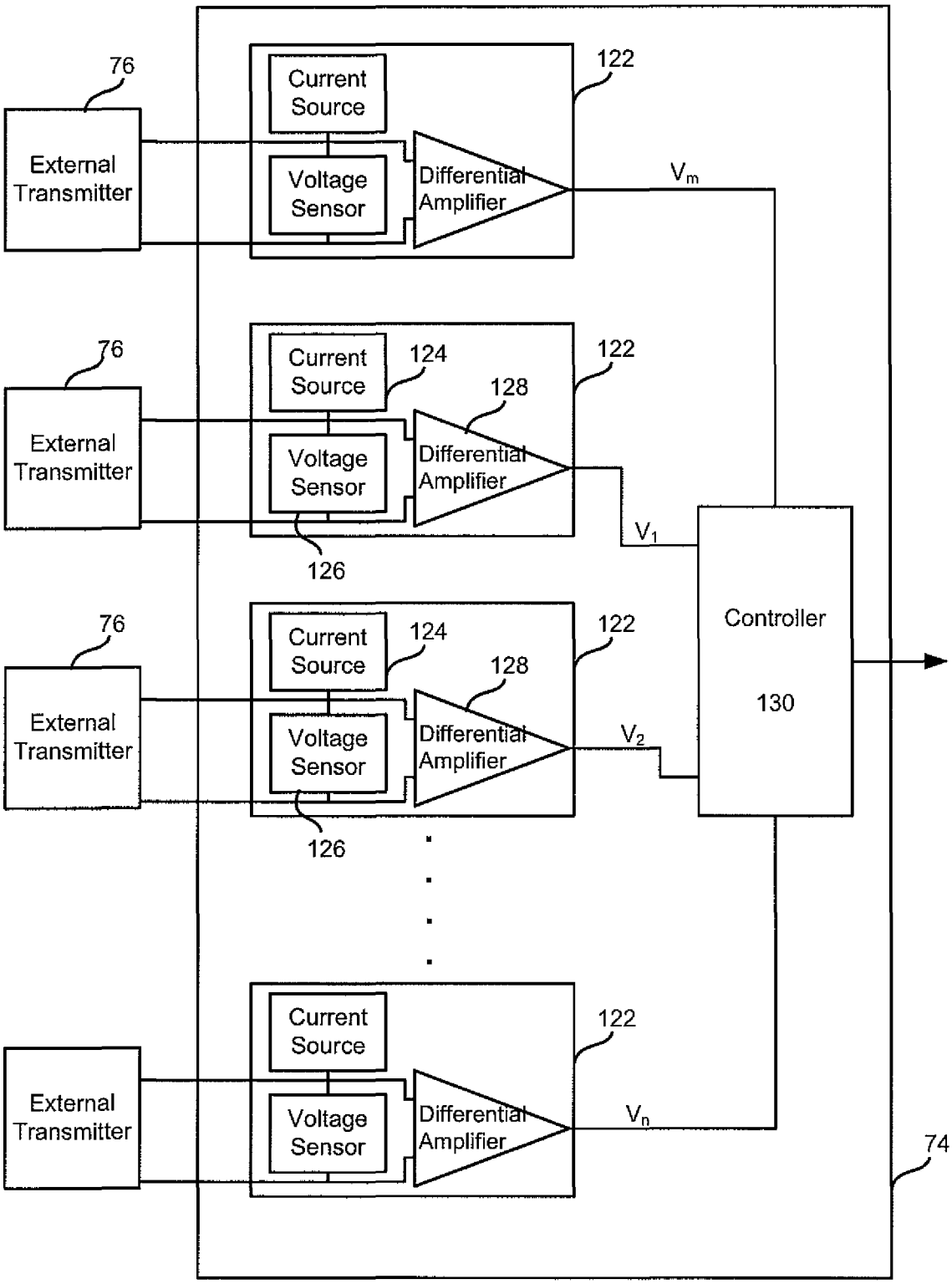

76
External Transmitter
Current Source
Voltage Sensor
Differential Amplifier
122
V_m
124
128
126
V_1
V_2
V_n
Controller
130
74

FIGURE 11

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
13/059,336	03/22/2011	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 08/03/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $60=	0
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/MINNIE JACKSON/

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/059,336	03/22/2011	David Tikkanen	PAT 67545W-2

CONFIRMATION NO. 9207

PUBLICATION NOTICE

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BORDEN LADNER GERVAIS LLP
Anne Kinsman
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OTTAWA, ON K1P 1J9
CANADA

OC000000049499833

Title:CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

Publication No.US-2011-0204820-A1
Publication Date:08/25/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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Substitute for Form PTO-875

Application or Docket Number: 13/059,336

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	430
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 52 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 220 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	980

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
13/059,336	David Tikkanen	PAT 67545W-2

26123
BORDEN LADNER GERVAIS LLP
Anne Kinsman
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INTERNATIONAL APPLICATION NO.	
PCT/CA09/01295	
I.A. FILING DATE	PRIORITY DATE
09/17/2009	09/18/2008

CONFIRMATION NO. 9207
371 ACCEPTANCE LETTER

OC000000047166513

Date Mailed: 05/16/2011

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

03/22/2011	03/22/2011
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 02/16/2011
- Copy of the International Search Report filed on 02/16/2011
- Preliminary Amendments filed on 02/16/2011
- Information Disclosure Statements filed on 02/16/2011
- Oath or Declaration filed on 03/22/2011
- U.S. Basic National Fees filed on 02/16/2011
- Priority Documents filed on 02/16/2011

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

NADINE V CLARK

Telephone: (571) 272-8662

FORM PCT/DO/EO/903 (371 Acceptance Notice)

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United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/059,336	03/22/2011	2821	1110	PAT 67545W-2	20	1

CONFIRMATION NO. 9207

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OTTAWA, ON K1P 1J9
CANADA

FILING RECEIPT



Date Mailed: 05/16/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

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Assignment For Published Patent Application

E CRAFTSMEN CORPORATION, Waterloo, ON, CA

Power of Attorney: The patent practitioners associated with Customer Number 26123

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/CA09/01295 09/17/2009
which claims benefit of 61/097,963 09/18/2008

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 04/14/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/059,336**

Projected Publication Date: 08/25/2011

Non-Publication Request: No

Early Publication Request: No

Title

CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

Preliminary Class

315

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set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

PTO/SB/81 (01-09)
Approved for use through 11/30/2011. OMB 0651-0035
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POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	13/059,336
Filing Date	2011-02-16
First Named Inventor	TIKKANEN, David
Title	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID ST
Art Unit	
Examiner Name	
Attorney Docket Number	PAT 67545W-2

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

26123

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/Inventor.

OR

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Assignee of Record

Signature	David Tikkanen	Date	April 15/2011
Name	David Tikkanen	Telephone	519-744-5677
Title and Company	Vice President - E Craftsmen Corporation		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: TIKKANEN, David, ET AL.

Application No./Patent No.: 13/059,336 Filed/Issue Date: 2011-02-16

Titled: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

E CRAFTSMEN CORPORATION , a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: All inventors (TIKKANEN, David, ET AL.) To: ELECTRONIC CRAFTSMEN CORPORATION

The document was recorded in the United States Patent and Trademark Office at
Reel 025818, Frame 0970, or for which a copy thereof is attached.

2. From: ELECTRONIC CRAFTSMEN CORPORATION To: E CRAFTSMEN CORPORATION

The document was recorded in the United States Patent and Trademark Office at
Reel 025819, Frame 0023, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jeffrey W. Wong/ 2011-04-19

Signature Date

Jeffrey W. Wong Agent, Reg. No. 46414

Printed or Typed Name Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	9907302
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David Tikkanen
Customer Number:	26123
Filer:	Jeffrey Wong
Filer Authorized By:	
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	19-APR-2011
Filing Date:	22-MAR-2011
Time Stamp:	11:36:49
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	pat-67545w-2-poa.pdf	72138 28063884ef5b6636c17d8b72413c3cd6b7a1b3fb	no	1

Warnings:	
Information:	

2	Assignee showing of ownership per 37 CFR 3.73(b).	pat-67545w-2-statement.pdf	176748 44479154b6f468b134b7c11dbf00a82e8df85e46	no	1

Warnings:	
Information:	
Total Files Size (in bytes):	248886

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
13/059,336	David Tikkanen	PAT 67545W-2

26123
BORDEN LADNER GERVAIS LLP
Anne Kinsman
WORLD EXCHANGE PLAZA
100 QUEEN STREET SUITE 1100
OTTAWA, ON K1P 1J9
CANADA

INTERNATIONAL APPLICATION NO.	
PCT/CA09/01295	
I.A. FILING DATE	PRIORITY DATE
09/17/2009	09/18/2008

CONFIRMATION NO. 9207
371 ACCEPTANCE LETTER

OC000000047166513

Date Mailed: 04/18/2011

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

03/22/2011	03/22/2011
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 02/16/2011
- Copy of the International Search Report filed on 02/16/2011
- Preliminary Amendments filed on 02/16/2011
- Information Disclosure Statements filed on 02/16/2011
- Oath or Declaration filed on 03/22/2011
- U.S. Basic National Fees filed on 02/16/2011
- Priority Documents filed on 02/16/2011

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

NADINE V CLARK

Telephone: (571) 272-8662

FORM PCT/DO/EO/903 (371 Acceptance Notice)

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/059,336

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	430
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 52 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 220 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	980

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/059,336	03/22/2011		1110	PAT 67545W-2	20	1

CONFIRMATION NO. 9207

26123
BORDEN LADNER GERVAIS LLP
Anne Kinsman
WORLD EXCHANGE PLAZA
100 QUEEN STREET SUITE 1100
OTTAWA, ON K1P 1J9
CANADA

FILING RECEIPT



Date Mailed: 04/18/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

David Tikkanen, Waterloo, CANADA;
Jason Neudorf, Kitchener, CANADA;
Steven Lyons, Kitchener, ON, CANADA;
Todd William Scott, Waterloo, ON, CANADA;
Kyle Grahame Hathaway, Kitchener, ON, CANADA;
David Wainesworth Jansen, Waterloo, ON, CANADA;

Assignment For Published Patent Application

E CRAFTSMEN CORPORATION, Waterloo, ON, CA

Power of Attorney: The patent practitioners associated with Customer Number 26123

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/CA09/01295 09/17/2009
which claims benefit of 61/097,963 09/18/2008

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 04/14/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/059,336**

Projected Publication Date: 371 Perfected

Non-Publication Request: No

Early Publication Request: No

Title

CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

Preliminary Class

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier

license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	TIKKANEN, David; NEUDORF, Jason; LYONS, Steven; SCOTT, Todd, William; HATHAWAY, Kyle, Grahame; JANSEN, David, Wainesworth
Serial No.:	13/059,336
Filed:	September 17, 2009
Title:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
Examiner:	
Attorney Ref.:	PAT 67545W-2

March 22, 2011

MAIL STOP MISSING PARTS
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22314-1450
U.S.A.

Dear Sir:

RESPONSE TO NOTIFICATION OF MISSING REQUIREMENTS

In response to the Notification of Missing Requirements Under 35 U.S.C. 371, dated March 14, 2011, Applicant submits a copy of the originally-submitted Declaration with all alterations initialled by the appropriate inventors.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,
TIKKANEN, David, et al.

By: /Jeffrey W. Wong/

Jeffrey W. Wong
Reg. No. 46414
Borden Ladner Gervais LLP
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100 Queen Street, Suite 1100
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CANADA
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JWW/cgk

PTO/SB/01A (01-09)
Approved for use through 09/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☑ United States application or PCT international application number PCT/CA2009/001295
  filed on 2009-09-17
  - ☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: David TIKKANEN Date: Jan 24, 2011

Signature: [signature] Citizen of: Canada

Inventor two: Jason NEUDORF Date: 2011 Jan 24

Signature: [signature] Citizen of: Canada

☑ Additional inventors or a legal representative are being named on 2 additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/02A (07-07)
Approved for use through 09/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Steven	LYONS

Inventor's Signature: Steven Lyons — Date: JAN 24/11

Residence: City	State	Country	Citizenship
~~Wallenstein~~ KITCHENER	ON	CA	CA

Mailing Address: ~~7800 Rd, 45 Glen Allan~~ 1011 QUEENS BLVD

City	State	Zip	Country
~~Wallenstein~~ KITCHENER	ON	~~N0B 2S0~~ N2M 1B8	CA

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Todd William	SCOTT

Inventor's Signature: Todd Scott — Date: JAN 24/2011

Residence: City	State	Country	Citizenship
Waterloo	ON	CA	CA

Mailing Address: 581 Drummerhill Crescent

City	State	Zip	Country
Waterloo	ON	N2T 1G3	CA

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Kyle Grahame MA	HATHAWAY

Inventor's Signature: Kyle Hathaway — Date: Jan. 24 '11

Residence: City	State	Country	Citizenship
Kitchener	ON	CA	CA

Mailing Address: 5 Norbert Place

City	State	Zip	Country
Kitchener	ON	N2K 1E5	CA

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
David Wainesworth	JANSEN		
Inventor's Signature			Date JAN 24/2011
Waterloo Residence: City	ON State	CA Country	CA Citizenship
333A Mayview Crescent Mailing Address			
Waterloo City	ON State	N2V 1P9 Zip	CA Country

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

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PTO/SB/02B (07-07)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION – Supplemental Priority Data Sheet

Foreign applications:

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
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			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	9711533
Application Number:	13059336
International Application Number:	
Confirmation Number:	9207
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	26123
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 67545W-2
Receipt Date:	22-MAR-2011
Filing Date:	
Time Stamp:	15:06:01
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	pat-67545w-2-response.pdf	78978 c947a53b8f166b1f5991dbc8ff7d85158b092a8a	no	1

Warnings:	
Information:	

2	Oath or Declaration filed	pat-67545w-2-declaration.pdf	210371 ee426b9e9ac97d19a5c0a5fb4190c4af42a2a27d	no	5

Warnings:	
Information:	
Total Files Size (in bytes):	289349

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/059,336

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	430
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 52 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 220 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	980

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
13/059,336	David TIKKANEN	PAT 67545W-2

26123
BORDEN LADNER GERVAIS LLP
Anne Kinsman
WORLD EXCHANGE PLAZA
100 QUEEN STREET SUITE 1100
OTTAWA, ON K1P 1J9
CANADA

INTERNATIONAL APPLICATION NO.	
PCT/CA09/01295	
I.A. FILING DATE	PRIORITY DATE
09/17/2009	09/18/2008

CONFIRMATION NO. 9207
371 FORMALITIES LETTER

OC000000046500303

Date Mailed: 03/14/2011

NOTIFICATION OF MISSING REQUIREMENTS UNDER 35 U.S.C. 371 IN THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

The following items have been submitted by the applicant or the IB to the United States Patent and Trademark Office as an Elected Office (37 CFR 1.495):

- Priority Document
- Copy of the International Application filed on 02/16/2011
- Copy of the International Search Report filed on 02/16/2011
- Preliminary Amendments filed on 02/16/2011
- Information Disclosure Statements filed on 02/16/2011
- Oath or Declaration filed on 02/16/2011
- U.S. Basic National Fees filed on 02/16/2011
- Priority Documents filed on 02/16/2011

The following items **MUST** be furnished within the period set forth below in order to complete the requirements for acceptance under 35 U.S.C. 371:

- Oath or declaration of the inventors, in compliance with 37 CFR 1.497(a) and (b), identifying the application by the International application number and international filing date. The current oath or declaration does not comply with 37 CFR 1.497(a) and (b) in that it:
  - alterations should be initialed

ALL OF THE ITEMS SET FORTH ABOVE MUST BE SUBMITTED WITHIN TWO (2) MONTHS FROM THE DATE OF THIS NOTICE OR BY 32 MONTHS FROM THE PRIORITY DATE FOR THE APPLICATION, WHICHEVER IS LATER. FAILURE TO PROPERLY RESPOND WILL RESULT IN ABANDONMENT.

The time period set above may be extended by filing a petition and fee for extension of time under the provisions of 37 CFR 1.136(a).

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

NADINE V CLARK

Telephone: (571) 272-8662

PTO-1390 (Rev. 09-08)
Approved for use through 3/31/2010. OMB 0651-0021
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
PAT 67545W-2	
U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/CA2009/001295	2009-09-17	2008-09-18

TITLE OF INVENTION
CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

APPLICANT(S) FOR DO/EO/US
TIKKANEN, David, ET AL.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☑ This is a **FIRST** submission of items concerning a submission under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a submission under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☑ The US has been elected (Article 31).
5. ☑ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☑ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☑ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☑ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☑ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☑ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☑ A preliminary amendment.
14. ☑ An Application Data Sheet under 37 CFR 1.76.
15. ☐ A substitute specification.
16. ☐ A power of attorney and/or change of address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.3 and 37 CFR 1.821 - 1.825.
18. ☐ A second copy of the published International Application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).

This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
	PCT/CA2009/001295	PAT 67545W-2

20. Other items or information:

Front page of International Publication No. WO2010/031169

The following fees have been submitted	CALCULATIONS	PTO USE ONLY
21. ☑ Basic national fee (37 CFR 1.492(a)) $330	$ 330	
22. ☑ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... $0 All other situations $220	$ 220	
23. ☑ Search fee (37 CFR 1.492(b)) If the written opinion of the ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... $0 Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority ..... $100 International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB ..... $430 All other situations $540	$ 430	
TOTAL OF 21, 22 and 23 =	980	

☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)).
The fee is $270 for each additional 50 sheets of paper or fraction thereof.

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof (round up to a whole number)	RATE	
- 100 =	/50 =		x $270	$

Surcharge of $130.00 for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total claims	- 20 =		x $52	$	
Independent claims	- 3 =		x $220	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $390	$	
			TOTAL OF ABOVE CALCULATIONS =	$	
☐ Applicant claims small entity status. See 37 CFR 1.27. Fees above are reduced by ½.					
			SUBTOTAL =	$	
Processing fee of $130.00 for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). +				$	
			TOTAL NATIONAL FEE =	$ 980	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$	
			TOTAL FEES ENCLOSED =	$ 980	
			Amount to be refunded:	$	
			Amount to be charged	$	

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☑ Please charge my Deposit Account No. 501593 in the amount of $ 980 to cover the above fees.

c. ☑ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 501593.

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SEND ALL CORRESPONDENCE TO:

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/Jeffrey W. Wong/
SIGNATURE

Jeffrey W. Wong
NAME

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(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **TIKKANEN, David** [CA/CA]; 194 Silverwood Place, Waterloo, Ontario N2T 2R9 (CA). **NEUDORF, Jason** [CA/CA]; 306-30 Bridge Street West, Kitchener, Ontario N2K 1K4 (CA). **LYONS, Steven** [CA/CA]; 1011 Queen's Boulevard, Kitchener, Ontario N2M 1B8 (CA). **SCOTT, Todd, William** [CA/CA]; 581 Drummerhill Crescent, Waterloo, Ontario N2T 1G3 (CA). **HATHAWAY, Kyle** [CA/CA]; 5 Norbert Place, Kitchener, Ontario N2K 1E5 (CA). **JANSEN, David, Wainesworth** [CA/CA]; 333A Mayview Crescent, Waterloo, Ontario N2V 1P9 (CA).

(74) Agents: **WONG, Jeffrey W.** et al.; BORDEN LADNER GERVAIS LLP, World Exchange Plaza, 100 Queen Street, Suite 1100, Ottawa, Ontario K1P 1J9 (CA).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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[Continued on next page]

(54) Title: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

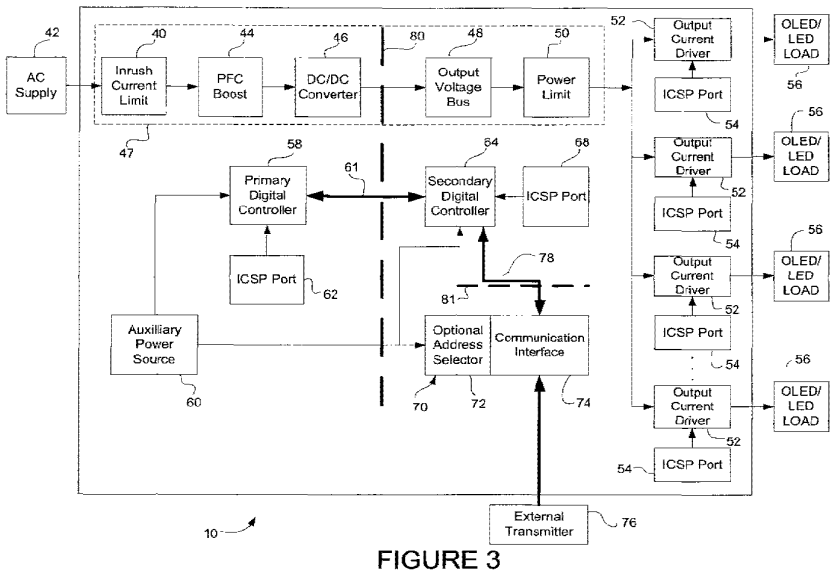


FIGURE 3

(57) Abstract: The disclosure is directed at a configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads comprising: a power circuit; a primary digital controller for controlling the power circuit; a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load; a secondary digital controller for controlling the set of output current drivers; wherein the secondary controller transmits LED control information to control outputs of the set of output current drivers; and wherein the secondary digital controller provides digital feedback control information to the primary digital controller.

WO 2010/031169 A1

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Filer:	Jeffrey Wong/Christopher Kreider
Attorney Docket Number:	PAT 67545W-2

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
National Stage Fee	1631	1	330	330
Natl Stage Search Fee - Report provided	1642	1	430	430
National Stage Exam - all other cases	1633	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
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Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	26123
Filer:	Jeffrey Wong/Christopher Kreider
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Attorney Docket Number:	PAT 67545W-2
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	OTT01-4353008-v1-PAT_67545W-2_ADS.PDF	1559272 880beea8c933fa31233828a055974538d05d3e1f	no	6
Warnings:					
Information:					
2	Oath or Declaration filed	OTT01-4357504-v1-PAT_67545W-2_Executed_Declaration.PDF	349963 7526333c6be10c2f06cbcd8e568a4e14acdc6a30	no	5
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3	Information Disclosure Statement (IDS) Filed (SB/08)	OTT01-4390066-v1-PAT_67545W-2_IDS.PDF	847968 2bc56b9a30995978fa8ac07bf9b354f321a72755	no	5
Warnings:					
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4	NPL Documents	pat-67545-NPL-colourdriver.pdf	448516 c74034a90fb0bb124f9af491b19fefd5aa307f99	no	2
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5	NPL Documents	pat-67545-NPL-Ericsson.pdf	639361 939c3714399146 43b859c6dd22287f08d1b7cb1c	no	16
Warnings:					
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10	NPL Documents	pat-67545-NPL-Traxon.pdf	886115 9abd3fea119d8268687c8f88995d88b480e17f20	no	17
Warnings:					
Information:					
11	NPL Documents	pat-67545-NPL-US-Tech-Online.pdf	583597 7341b5a13c73ea228e787f882335fd0051e44f08	no	1
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12	Foreign Reference	pat-67545w-2-fr-wo08052293.pdf	1350482 9402523c2371b7d079fd8ce1029715af90b9d40b	no	34
Warnings:					
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13	NPL Documents	pat-67545w-2-npl-isr.pdf	458937 75aeb5e679c05fc70d119364cd1ba3c45e8425de	no	12
Warnings:					
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14		pat-67545w-2-preliminary-amendment.pdf	81089 b0ac98db5779ba6465bd7e446f61f7a4037c5f8e	yes	3

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Specification	2	2
Applicant Arguments/Remarks Made in an Amendment	3	3

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15	Transmittal of New Application	pat-67545w-2-transmittal.pdf	391699 e650779c8e260a7b4ed0b38c6e8fc4591adbfe98	no	3
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16	Documents submitted with 371 Applications	pat-67545w-2-wo-cover.pdf	1424335 038b7faad28b2b97f9e013587697bc2c99c64b33	no	2
Warnings:					
Information:					
17	Fee Worksheet (PTO-875)	fee-info.pdf	33376 ec56e6150f5aafc760192265f8f4ebe55a10be7a	no	2
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 67545W-2
	Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

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Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	David		TIKKANEN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Waterloo	Country Of Residence[i]	CA
Citizenship under 37 CFR 1.41(b)[i]	CA		

Mailing Address of Applicant:

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City	Waterloo	State/Province	ON
Postal Code	N2T 2R9	Country[i]	CA

Applicant 2 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jason		NEUDORF	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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Citizenship under 37 CFR 1.41(b)[i]	CA		

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Postal Code	N2K 1K4	Country[i]	CA

Applicant 3 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Steven		LYONS	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Kitchener	Country Of Residence[i]	CA

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 67545W-2
	Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

Citizenship under 37 CFR 1.41(b) i	CA		
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Address 1	1011 Queen's Boulevard		
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Applicant 4 Remove

Applicant Authority (•) Inventor ( ) Legal Representative under 35 U.S.C. 117 ( ) Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Todd	William	SCOTT	

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City	Waterloo	**Country Of Residence**i	CA
Citizenship under 37 CFR 1.41(b) i	CA		
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Address 2			
City	Waterloo	**State/Province**	ON
Postal Code	N2T 1G3	**Country**i	CA

Applicant 5 Remove

Applicant Authority (•) Inventor ( ) Legal Representative under 35 U.S.C. 117 ( ) Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kyle	Grahame	HATHAWAY	

Residence Information (Select One) ( ) US Residency (•) Non US Residency ( ) Active US Military Service

City	Kitchener	**Country Of Residence**i	CA
Citizenship under 37 CFR 1.41(b) i	CA		
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Address 2			
City	Kitchener	**State/Province**	ON
Postal Code	N2K 1E5	**Country**i	CA

Applicant 6 Remove

Applicant Authority (•) Inventor ( ) Legal Representative under 35 U.S.C. 117 ( ) Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	David	Wainesworth	JANSEN	

Residence Information (Select One) ( ) US Residency (•) Non US Residency ( ) Active US Military Service

City	Waterloo	**Country Of Residence**i	CA
Citizenship under 37 CFR 1.41(b) i	CA		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 67545W-2
	Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

Mailing Address of Applicant:			
Address 1	333A Mayview Crescent		
Address 2			
City	Waterloo	**State/Province**	ON
Postal Code	N2V 1P9	**Country**[i]	CA

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	26123		
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Application Information:

Title of the Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		
Attorney Docket Number	PAT 67545W-2	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	14	**Suggested Figure for Publication (if any)**	1a

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 67545W-2
	Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	CA2009/001295	2009-09-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
CA2009/001295	non provisional of	61097963	2008-09-18

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Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			◉ Yes ○ No

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Assignee Information:

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Assignee 1 Remove

If the Assignee is an Organization check here. ☒			
Organization Name	E CRAFTSMEN CORPORATION		
Mailing Address Information:			
Address 1	73 Schaefer Street		
Address 2			
City	Waterloo	**State/Province**	ON
Country [i] CA		Postal Code	N2L 4C4
Phone Number		Fax Number	
Email Address			

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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 67545W-2
	Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

Signature	/Jeffrey W. Wong/			Date (YYYY-MM-DD)	2011-02-16
First Name	Jeffrey W.	Last Name	Wong	Registration Number	46414

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/01A (01-09)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☑ United States application or PCT international application number PCT/CA2009/001295 filed on 2009-09-17
- ☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: David TIKKANEN Date: Jan 24, 2011

Signature: [signature] Citizen of: Canada

Inventor two: Jason NEUDORF Date: 2011 Jan 24

Signature: [signature] Citizen of: Canada

☑ Additional inventors or a legal representative are being named on 2 additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Steven	LYONS		
Inventor's Signature			Date: JAN 24/11
Wallenstein ~~Residence:~~ City KITCHENER	ON State	CA Country	CA Citizenship
~~7800 Rd, 45 Glen Allan~~ 1011 QUEENS BVLD Mailing Address			
~~Wallenstein~~ City KITCHENER	ON State	~~N2M 1B8~~ N0B 2S0 Zip	CA Country

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Todd William	SCOTT		
Inventor's Signature			Date: JAN 24/2011
Waterloo Residence: City	ON State	CA Country	CA Citizenship
581 Drummerhill Crescent Mailing Address			
Waterloo City	ON State	N2T 1G3 Zip	CA Country

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Kyle Grahame	HATHAWAY		
Inventor's Signature			Date: Jan. 24 '11
Kitchener Residence: City	ON State	CA Country	CA Citizenship
5 Norbert Place Mailing Address			
Kitchener City	ON State	N2K 1E5 Zip	CA Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
David Wainesworth	JANSEN		
Inventor's Signature			Date JAN 24/2011
Waterloo Residence: City	ON State	CA Country	CA Citizenship
333A Mayview Crescent Mailing Address			
Waterloo City	ON State	N2V 1P9 Zip	CA Country

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

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DECLARATION – Supplemental Priority Data Sheet

Foreign applications:

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	TIKKANEN, David, ET AL.
Art Unit	
Examiner Name	
Attorney Docket Number	PAT 67545W-2

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	1	20050289279		2005-12-29	FAILS ET AL.	
	2	20050218838		2005-10-06	LYS	
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	1	2008052293	WO		2008-05-08	QUICK ET AL.		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	TIKKANEN, David, ET AL.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	ERICSSON AB, Power Supplies Goes Digital White Paper, October 2006	☐
	2	SKANDA; MICROCHIP TECHNOLOGY INC., Power Factor Correction in Power Conversion Applications using the dsPIC® DSC", AN1106, June 2007	☐
	3	TRAXON TECHNOLOGIES, LED Engine XB 3W-108 Technical Specifications and User Manual Version 1.1, 2007	☐
	4	PENWELL CORPORATION, Dialight Lumidrives Launches Colurdriver XP for High-Power LEDs, LEDs MAGAZINE, downloaded from http://www.ledsmagazine.com/press/15469, 2007-09-25	☐
	5	Colourdriver XP data sheet, 2008-07-30	☐
	6	US-TECH ONLINE, Dialight: New High Power LED Driver, downloaded from http://www.us-tech.com, October 2007	☐
	7	IST LTD., iDrive™ 1000 The Intelligent 210W LED Driver User Manual, v. 1.7, 2008-06-20	☐
	8	ROAL ELECTRONICS, S.P.A, Programmable RGB LED Driver 200 Watts Model RHPS180 Product Details, Rev. 2, 2007-10	☐
	9	INTERNATIONAL SEARCHING AUTHORITY (CA), International Search Report and Written Opinion for International Patent Application No. PCT/CA2009/001295, 2010-01-13	☐

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	Application Number	
	Filing Date	
	First Named Inventor	TIKKANEN, David, ET AL.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

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	Application Number	
	Filing Date	
	First Named Inventor	TIKKANEN, David, ET AL.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	PAT 67545W-2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2011-02-16
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

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8 May 2008 (08.05.2008)

PCT

(10) International Publication Number
WO 2008/052293 A1

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(22) International Filing Date:
5 November 2007 (05.11.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
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(71) Applicant *(for all designated States except US)*: **CLIPSAL AUSTRALIA PTY LTD** [AU/AU]; 12 Park Terrace, Bowden, S.A. 5007 (AU).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **QUICK, Ashleigh, Glen** [AU/AU]; 12 Park Terrace, Bowden, S.A. 5007 (AU). **NEWMAN, Andrew** [AU/AU]; 12 Park Terrace, Bowden, S.A. 5007 (AU).

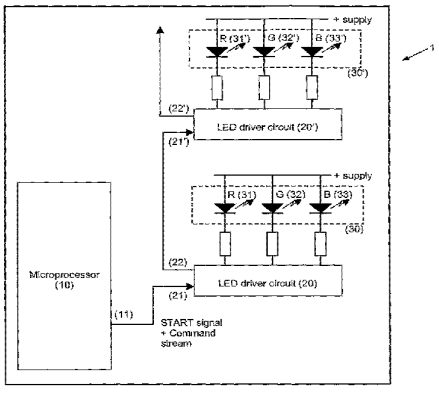
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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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(54) **Title:** LIGHT EMITTING DIODE DRIVER AND METHOD



(57) **Abstract:** Disclosed is a method and apparatus for controlling a plurality of Light Emitting Diodes (LEDs). A communications protocol is also provided, which comprises a START code, a first Command packet and at least one subsequent Command packet. An LED driver receives a signal according to the protocol, and separates the first Command packet from the signal and controls an LED associated with the LED driver in accordance with instructions in the first Command packet. The LED driver then outputs the remaining signal for use by one or more subsequent LED drivers.

WO 2008/052293 A1

LIGHT EMITTING DIODE DRIVER AND METHOD

TECHNICAL FIELD

This invention relates to Light Emitting Diodes and to apparatus and methods for their control.

PRIORITY

The present application claims priority from Australian Provisional Patent Application No. 2006906139 entitled "Light Emitting Diode Driver and Method".

The entire content of this provisional application is hereby incorporated by reference.

BACKGROUND

A common requirement for electronic equipment is to have a visual indication on a control device. Such a control device could be a button, lever, knob, or similar, and the visual indication is often used to show the state of whatever is controlled – for example an electrical load being turned on or off, or a door open or closed.

In modern electronic equipment, the visual indication is readily provided by a light emitting diode (LED) which has the advantages of being small, cheap, and a long operating life. Multiple colours may be achieved by making use of several LEDs of different colour – these can even be mounted in the same physical package.

By separate dimming of each component colour, a dual-colour combination LED can be used to mix the two component colours to create additional colours, as perceived by a human observer. More recently, three colour combination LEDs have become available, and some of these include elemental components that emit in the colours Red, Green and Blue. By selective dimming of these components, any colour, including white, can be obtained.

In order to produce any resultant colour, an RGB combination LED needs each of the colour components to have a separate dimmable drive. Whilst LED dimming is

straightforward using the well-established method of pulse-width modulation, such a typical combination LED will usually have at least 4 terminals: a common point and a drive input for each of the three colour elements.

Using a single three colour RGB combination LED with a common point and 3 drive inputs is relatively easy to drive to obtain any desired human-perceived colour. For example, a small micro-processor can use 3 separate pulse-width modulated outputs to drive such an indicator. An exemplary arrangement of this application is shown in prior art figure 1. In figure 1, there is shown microprocessor 10 driving two LEDs 30 and 30'. Each LED has respective colour components of red (31), green (32) and blue (33). Respective resistors 34, 35 and 36 are also provided to limit the current applied to the LED components.

In operation, microprocessor 10 generates and transmits control signals to each LED 30 and corresponding colour component 31, 32 and 33 to control the operation of each LED in accordance with a sequence of instructions programmed into microprocessor 10 as will be understood by the person skilled in the art.

As can be seen from Figure 1, driving 2 LEDs requires 6 drive signals 11, 12, 13, 14 ,15 and 16, one for each LED component, or three for each LED in the case of a three-colour LED.

It will be appreciated however, that when many such combination LEDs need to be driven (irrespective of the number and nature of the coloured elements) – potentially all showing separate information (for example colour and brightness) the number of drive signals rapidly increases. For example to drive 10 such RGB combination LEDs would require 30 drive signals. As the number of multi-colour combination LEDs in a product increases, the complexity of wiring these to a controller device increases, as does the complexity of the controlling device. For example, a large number of wiring paths might be needed on a printed circuit board, and a large number of pulse width modulated outputs might be needed on a microprocessor.

LED controller devices are currently available that make use of serial data buses - the most notable being the Philips inter-integrated circuit (I2C) bus. Such LED controllers allow a 2-wire control output from a microprocessor to be connected to a LED driver IC, which in turn is connected to one or more combination LEDs. By sending appropriate commands to the I2C driver IC, a suitable colour and brightness can be obtained from the combination LED(s). If the combination LED contains red, green and blue elements, then by appropriate selection of brightness of the elements, any colour can be obtained.

Whilst being an improvement on directly connecting LEDs to a microprocessor, systems using these approaches have a number of deficiencies. These deficiencies include the high cost of the LED driver ICs, the limited addressing range of these bus systems, and the additional need to route power and / or ground separately to the LEDs and the driver IC's - increasing circuit board layout complexity and potentially cost, through the need for multi-layer PCBs. Whilst this limited addressing can be overcome by the use of I2C bridges, this adds extra devices and cost to such an arrangement.

It is therefore an object of the present invention to provide an alternative to existing LED control systems.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention, there is provided a communications protocol for use in controlling a plurality of Light Emitting Diodes (LEDs) associated with respective LED drivers, the communications protocol comprising a first Command packet containing at least one instruction for controlling a first of the plurality of LEDs, and at least one subsequent Command packet containing instructions for controlling at least one subsequent LED, connected in series with the first LED.

In one form, the protocol further comprises a START code prior to the first Command packet.

In one form, the respective START codes are provided prior to each subsequent Command packets.

In one form, at least one of the first and subsequent Command packets contains instructions for controlling a plurality of elements within a respective LED.

According to a second aspect of the present invention, there is provided a Light Emitting Diode (LED) driver comprising:

an input for receiving a signal according to the communications protocol as claimed in any one of claims 1 to 4;

means for controlling an associated LED in accordance with the at least one instruction in the first Command packet; and

an output for outputting the at least one subsequent Command packet.

In one form, the LED further comprises means for separating the first Command packet from the signal.

According to a third aspect of the present invention, there is provided a Light Emitting Diode (LED) comprising an LED driver according to the second form of the present invention.

According to a fourth aspect of the present invention, there is provided a device for controlling a plurality of LEDs, the device comprising:

means for generating and outputting a signal comprising a START code, a first Command packet and at least one subsequent Command packet;

first means for receiving the signal and controlling an LED associated with the first means in accordance with instructions in the first Command packet;

first means for separating the first Command packet from the signal to provide a remaining signal; and

means for outputting the remaining signal.

In one form, the means for generating is a microprocessor.

In one form, the first means for receiving and controlling, the first means for separating and the means for outputting comprise an LED driver.

In one form, the LED driver is a microprocessor.

In one form, there is at least one subsequent driver associated with at least one subsequent LED.

According to a fifth aspect of the present invention, there is provided an electronic device comprising:

a plurality of Light Emitting Diodes (LEDs);

a plurality of LED drivers as claimed in claim 5 for controlling a respective one of the plurality of Light Emitting Diodes; and

a microprocessor for generating and outputting a signal according to the communications protocol as claimed in any one of claims 1 to 4 to a first of the plurality of LED drivers.

According to a sixth aspect of the present invention, there is provided a method for controlling a plurality of LEDs, the method comprising:

generating and outputting a signal comprising a START code, a first Command packet and at least one subsequent Command packet;

receiving the signal and controlling an LED in accordance with instructions in the first Command packet;

separating the first Command packet from the signal to provide a remaining signal; and

outputting the remaining signal.

According to a seventh aspect of the present invention, there is provided a machine readable medium containing machine executable instructions to perform the method of the sixth aspect of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 - shows a prior art arrangement with 2 RGB combination LEDs connected to a microcontroller;

Figure 2 - shows a first exemplary implementation of an aspect of the present invention in which several LED driver circuits are connected to a single microprocessor output;

Figure 3 - shows an exemplary timing diagram and command sequence that could be applied to the arrangement of Figure 2;

Figure 4 – shows an alternative exemplary timing diagram and command sequence that could be applied to the arrangement of Figure 2;

Figure 5 - shows a second exemplary implementation according to an aspect of the present invention, in which two LED driver circuits are connected to 2 microprocessor outputs;

Figure 6 - shows an exemplary timing diagram and command sequence that could be applied to the arrangement of Figure 5;

Figure 7 – shows a block diagram of an LED driver as shown in Figure 2;

Figure 8 – shows a reference circuit diagram of the LED driver of Figure 2;

Figure 9 – shows a block diagram of an LED driver as shown in Figure 5.

Figure 10 – shows a circuit diagram of an exemplary embodiment of the master section of the arrangement shown in Figure 2; and

Figure 11 – shows a circuit diagram of an exemplary embodiment of the driver section of the arrangement shown in Figure 2.

DETAILED DESCRIPTION

Figure 2 shows an electronic device 1 showing an exemplary arrangement of components according to a first aspect of the present invention. In Figure 2 there is

shown a microprocessor 10 with a single output signal 11 connected to LED driver circuit constructed according to another aspect of the present invention. Details of the operation of LED driver circuit 20 will be discussed in more detail further below. LED driver 20 drives LED 30.

Figure 2 also shows a second LED 30', driven by a second LED driver 20'.

Microprocessor 10 can be any microprocessor, from any manufacturer, that is capable of transmitting a data stream out of a single output – a technique commonly referred to as "bit bashing". Such microprocessors are readily available from many manufacturers, in an almost infinite variant of capability variations. Suitable microprocessors are available from manufacturers including Atmel, Texas Instruments, Zilog, Freescale, ST, and many others.

According to an aspect of the present invention, microprocessor 10 generates a control signal and transmits this along output 11 to an input 21 of the LED driver 20.

As will be described in more detail further below, the signal generated by microprocessor 10 consists of a series of Command packets, each intended for one of the LEDs needed to be controlled by microcontroller 10. Driver 20 accepts the signal, and strips off (or separates) the first Command packet in the signal or data stream, and outputs the remainder of the signal or data stream via output 22. The remainder of the signal is then input into the input 21' of the next LED driver 20', which then strips off the next Command packet and outputs the remainder of the signal via output 22'. The signal continues to travel from one LED driver to the next, until all Command packets have been stripped off or separated.

The Command packet for each LED contains information to allow each LED driver 20 to drive each of the red (31), green (32) and blue (33) light components of respective LEDs.

In one form, the communication protocol includes a START code indication, followed by one or more subsequent Command packets. The first Command packet is applied to the first LED driver circuit that the signals reach after the controlling device, and is removed from the stream. Everything after the first Command packet is then passed out of the first LED driver circuit to the second LED driver circuit and so on, as described above. Each LED driver circuit knows to expect a new Command packet when it sees the START code. To ensure that the START code is passed along, each LED driver circuit can either re-generate the START code, as shown in Figure 3, or can simply pass it out when it is received, as shown in Figure 4.

In one form, the LED driver circuit 20 has the function of accepting in its Command packet a setting of the brightness of each of the colour elements of its attached combination LED.

By placing the LED driver circuits in a sequential cascade arrangement, there is no need to address information to each circuit – instead, addressing will be achieved by the order of the electrical interconnection. Thus, for example, the first Command packet will be accepted by the first LED driver circuit (and subsequent Command packets are simply passed out to the next one in the line). Similarly the second LED driver circuit, not seeing the Command packet that was removed by the first LED driver circuit, will accept the second Command packet transmitted, and pass on any that follow. This process is repeated until the last LED driver circuit is reached.

Figures 3 and 4 show an exemplary structure of such a signal, containing multiple Command packets. Figure 3 shows the case where the START code is regenerated, while Figure 4 shows the case where the START code is copied instead of being regenerated. The first row (A) of Figures 3 and 4 show the signal as generated by the microprocessor 10. This signal is input to the input 21 of the first LED driver device 20 (for example as seen in Figure 2). In one form, the signal may include a START code 110 at the beginning of the signal. In one form, the START code 110 comprises a pattern that is distinguishable from the Command packet information. When a LED

driver circuit recognises the sequence comprising the START code, it knows that the Command packet that follows is for its use, and subsequent commands are to be relayed out to a subsequent device.

One suitable method of generating the START code is to encode the Command portions using "bit-stuffing", and use a coding violation as the START code - a technique which is well established in the prior art. Another possible method is to transmit the Command portion as a stream of asynchronous serial data bits, and to transmit a "Break" symbol as the START code. Whilst these are two suitable methods, there are many others that provide the same behaviour.

Following the START code 110, when present, is the first Command 120. This Command contains control information for the first LED driver 20 to control the various elements of the LED 30 to which it is connected (see Figure 2). Upon receiving the signal, LED driver 20 strips off, or otherwise "switches off" the first Command so as to be not present, or ignored by subsequent LED drivers, and retransmits or otherwise forwards the signal from its output 22 to the next LED driver 20' in the series.

The signal may contain as many Commands as there are LED drivers, or may contain more or less, depending upon the required function of the LEDs to be controlled. For example, if there are more Commands than LEDs, the extra Commands could be simply ignored. If there are fewer Commands than LEDs, either the extra LEDs may not be provided instructions, or the extra LEDs may perform the same function as the last LED which had a specific Command, or could be otherwise connected to previous LEDs to perform the same function as those.

In line B of Figures 3 and 4, the signal can be seen to have had the first Command 120 removed, with subsequent Commands 130 and 140 remaining. This is the structure of the signal on the output 22 of LED driver 20 and the input 21' of LED driver 20' in Figure 2. In row C, the signal can be seen to have had first and second Commands removed, to have remaining the last Command for the last LED required to be

controlled. In the case of Figure 2, this signal structure will appear on the output 22' of LED driver 20', for input into the next LED driver (not shown).

The structure of each Command will be tailored for the required operation of each individual LED 30. In one example, the structure of the Command can be a set of binary coded brightness levels for each individual LED. For RGB LEDs, the Command might comprise typically between 4 and 8 bits to encode the brightness levels of the Red, Green, and Blue component LEDs. Any precise ordering or encoding of these brightness levels is unimportant, provided it is applied consistently between the microprocessor 10 and all LED driver circuits.

In this manner, a single microprocessor could drive a single combination LED, or any other number, without additional hardware interconnections being required to the microprocessor. In another form, this arrangement could be used to drive two or more LEDs having only one colour component, or having any number of colour components. In some forms, the LEDs driven could have varying numbers of colour or other control components, for example, the microprocessor might set a flash pattern on a LED, or combination LED, by setting a flash rate, or setting periods of time for a LED or LED components are to be switched on and off.

For example, a system may have 10 LEDs, 5 of which may be single colour components, 2 may be 2-colour components and 3 may be 3-colour components. Of course the number of controllable components within an LED need not be restricted to 3, but could be any number as may be required for the particular application.

One example of a structure of a Start bit used as the Start code, is 1440us wide, with a low for 960us and a high pulse for 480us. A data bit definition for the Command packets could be "Bit 0" having 60 us width with a 20us low and a 40us high pulse. The "Bit 1" definition could have a 60us width with 40us low and 20us high pulse. Such coding is known as Manchester coding and is well known to the person skilled in the art. Of course, any other form of suitable coding may also be used.

In generating a signal according to this aspect of the invention, the microprocessor does so in accordance with a software program. An example of a suitable program for controlling five LEDs, 2 of a single colour component and 3 of 3 colour components is shown in the following pseudo-code:

Assumptions:

A single Command comprises brightness for Red, Green and Blue, in that order

A single colour LED has its brightness set by the Red component of a Command only

A suitable coding system has been chosen for the Commands and the START code

The two single colour LEDs are wired closest to the microprocessor, followed by the 3, 3 colour LEDs

Pseudo-code:

Send the START code

Send the Command for the first single colour LED comprising the set (First brightness, anything, anything)

Send the Command for the second single colour LED comprising the set (Second brightness, anything, anything)

Send the Command for the third LED comprising the set (Third Red, third Green, Third Blue)

Send the Command for the fourth LED comprising the set (Fourth Red, Fourth Green, Fourth Blue)

Send the Command for the fifth LED comprising the set (Fifth Red, Fifth Green, Fifth Blue)

In an alternative form of the present invention, the signal generated by the microprocessor 10 need not have a START code embedded therein. In this case, two microprocessor outputs may be used, the first such output being used to signal the start of a new command stream, and the second such output being used to encode

the stream of Commands being sent to each of the driver circuits in turn. Such an encoding of the Commands could comprise digital data, typically as a stream of binary digits (bits).

Figure 5 shows an arrangement according to this aspect of the invention, in which like elements are numbered accordingly. In this arrangement, microprocessor 10 has two outputs, 11 and 12. Output 11 functions as previously described with reference to Figure 2, but output 12 now provides the START information to inform each LED driver 20, 20′ ... when a new Command stream is being transmitted, in place of the START code being present in the signal.

In this arrangement, LED drivers 20, 20′... will have a third input 23, for receiving the START code from microprocessor 10.

Figure 6 shows an exemplary structure of the control signals generated by microprocessor 10 in the arrangement as shown in Figure 5. In row A of Figure 6, a START code is provided on output 12 of microprocessor 10 and input to each of the LED drivers 20 via respective inputs 23. Row B shows the structure of the signal generated by microprocessor 10 and output on output 11, to be received by each LED driver 20 in turn. It will be noted that no START code is present in this structure as it is being provided by output 12. Rows B, C and D of Figure 6 correspond to rows A, B and C of Figures 3 and 4 and function in the same way.

Figure 7 shows an exemplary system block diagram of an LED driver circuit for an LED driver as shown in Figure 2 that has a single input for receiving a START code and Command packets. In this arrangement, the START code and Command packets enter driver 20 at data input 21. The START code is detected at block 24 and the Command packet is received at block 26, decoded and passed to pulse width modulation (PWM) channels block 27 for application to the components of the LED (not shown) via an optional current limiting block 29. Oscillator/clock generator 28 provides the timing for block PWM block 27.

From block 26, the remaining Command packets are passed through to data output 22. If the START code is to be regenerated and passed through to subsequent drivers, this is done at block 35 and provided to output 22 with the remaining Command codes from block 26.

Figure 8 shows a reference circuit diagram of the arrangement of Figure 7. This reference circuit uses a small, low-cost microprocessor as the main element of the LED driver circuit, with all major functions implemented in software. Suitable microprocessors are available from Texas Instruments, Freescale, and other manufacturers. Naturally, such an arrangement can be replaced by any other functionally equivalent circuit, whether using software or not.

Figure 9 shows an exemplary system block diagram of an LED driver circuit for an LED driver as shown in Figure 5 that has a single input for receiving a START code and Command packets. This is an alternative arrangement for driver 20 to that of Figure 7. In this arrangement, the Command packets enter driver 20 at data input 21. The START code that is generated separately at a second output of microprocessor 10 (as described previously with reference to Figure 5) enters driver 20 at second input 23. The Command packets and START code are received at block 26. The Command packets are decoded and passed to pulse width modulation (PWM) channels block 27 for application to the components of the LED (not shown) via an optional current limiting block 29. Oscillator/clock generator 28 provides the timing for block PWM block 27.

The START code and remaining Command packets are then sent to subsequent drivers via output 22.

The arrangement of Figure 9 can equally be implemented as a single microprocessor having programmed thereon instructions to carry out the functions of the arrangement of Figure 9. This would be as shown in Figure 8.

Figure 10 shows an alternative embodiment of the LED controller master section, showing microprocessor 10, which in this example is a PIC16F73. The particular layout and function of the surrounding circuitry will be apparent to the person skilled in the art and will not be described in detail herein.

Figure 11 shows an implementation of an LED driver 20 and associated LED 30 with individually-drivable colour components 31 (Red), 32 (Green) and 33 (Blue). In this example, the microprocessor used for the driver 20 is an EM78P153S available from ELAN Microelectronics Corporation in Taiwan. Again, the layout and function of the surrounding circuitry will be apparent to the person skilled in the art and will not be described in detail herein.

In use, a circuit will be built up using a plurality of drivers 20 as shown in Figure 11, cascaded in daisy-chain style. Each LED 30, 30', 30'' e.t.c. would be associated with its own driver 20, 20', 20'' e.t.c.

In another aspect of the invention, there is provided a method of controlling a plurality of LEDs. The first aspect of the method provides for the generation of a signal or data stream according to the protocol described above. In particular, the method includes generating the signal or data stream by generating a Start code, generating a first Command packet, generating at least one subsequent Command packet and then outputting the signal. A further aspect of the method includes receiving the data stream or signal, separating the first Command packet from the data stream or signal to provide a remaining data stream or signal, controlling a first LED in accordance with instructions in the first command packet and outputting the remaining data stream or signal. The remaining data stream or signal is then processed in the same way with respect to the at least one subsequent Command packet.

In another aspect, the present invention provides computer executable instructions which cause a computer to perform the various steps of the methods described herein. In particular, the computer executable instructions cause the computer (such

as microprocessor 10) to execute the steps of generating a first Command packet containing at least one instruction for controlling a first of the plurality of LEDs, and generating at least one subsequent Command packet containing instructions for controlling at least one subsequent LED, connected in series with the first LED. In another form, the computer executable instructions cause the computer to also generate a START code and insert this in a data stream in front of the Command and subsequent Command packets. In another form, the computer executable instructions cause the computer to generate separate START codes prior to each of the Command and subsequent Command packets.

In another aspect, the computer executable instructions also cause a computer to perform the steps performed by the driver 20. As described with reference to Figure 8, the computer could also be a microprocessor. In this aspect, the computer executable instructions cause the computer to execute the steps of receiving a data stream including a first Command packet and at least one subsequent Command packet, separating the first Command packet from the data stream, controlling an LED associated with the computer in accordance with instructions in the first Command packet, and outputting the at least one subsequent Command packet for use by another driver.

In one form, the computer executable instructions may also cause the computer to detect a START code in the data stream, and either pass that START code through and output it with the at least one subsequent Command packet or generate a new START code and output that with the at least one Command packet.

In another aspect of the invention, there is also provided a machine readable medium containing the machine executable instructions described above. Such a machine readable medium includes the memory on the microprocessor 10, or other, separate memory medium, including a CD, a DVD, a Flash drive or other portable memory medium.

In one embodiment, the LED driver circuit could be implemented as an integrated circuit, using a suitable semiconductor technology such as but not limited to silicon. A variation of this embodiment would be to attach and integrate the circuit with an LED device. In one example, this could be an LED with 3 primary colour LED elements. In such an embodiment the current limit resistors may be integrated, or replaced by a transistor based current limiting arrangement, both techniques being well established.

In such an embodiment, which made use of a single control signal from a microprocessor, the completed packaged integrated driver circuit and LEDs would have four electrical connections comprising a power input, a power return (or ground), a data in signal, and a data out signal. An embodiment making use of two outputs from microprocessor would include a fifth electrical connection used to indicate the start of a new stream of Commands.

In one form the microprocessor 10 would transmit the Command stream at a rate of at least 100,000 bits/second. Such a rate would allow the colour and brightness of 10 RBG LEDs to be completely updated in less than 3 milliseconds. Naturally, operation at even faster speeds would be straightforward and yield commensurately lower update times. Naturally, where rapid update or only a small number of LEDs is to be controlled, a lower rate would also be suitable

This arrangement has the advantages that it allows any number of combination LEDs to be driven without need for special expansion devices when an addressing range is exceeded; it allows a small number of drive signals from the controlling device; and it offers the benefit of integrating such a LED driver circuit into the same component package as the combination LED. Integration of the driver circuit into the LED package minimises the overall cost, and dramatically reduces the number of electrical interconnections between the driver IC and the colour elements of the combination LED.

The various aspects of the present invention may be used in any number of electronic devices that have LEDs as part of their circuitry. This includes entertainment devices such as televisions, digital set-top boxes, sound systems, DVD players, CD players, remote control units. It also includes computers and computer peripherals, and displays for vehicles and other devices. The various aspects of the present invention can also be applied to electronic devices that have not yet been invented at the time of filing the present application.

It will be understood that the above has been described with reference to particular embodiments and that many variations and modifications may be made within the scopes of the different aspects of the present invention.

Throughout the specification and the claims that follow, unless the context requires otherwise, the words "comprise" and "include" and variations such as "comprising" and "including" will be understood to imply the inclusion of a stated integer or group of integers, but not the exclusion of any other integer or group of integers.

The reference to any prior art in this specification is not, and should not be taken as, an acknowledgement of any form of suggestion that such prior art forms part of the common general knowledge.

THE CLAIMS:

1. A communications protocol for use in controlling a plurality of Light Emitting Diodes (LEDs) associated with respective LED drivers, the communications protocol comprising a first Command packet containing at least one instruction for controlling a first of the plurality of LEDs, and at least one subsequent Command packet containing instructions for controlling at least one subsequent LED, connected in series with the first LED.

2. A communications protocol as claimed in claim 1 further comprising a START code prior to the first Command packet.

3. A communications protocol as claimed in claim 2 wherein respective START codes are provided prior to each subsequent Command packet.

4. A communications protocol as claimed in claim 1 wherein at least one of the first and subsequent Command packets contains instructions for controlling a plurality of elements within a respective LED.

5. A Light Emitting Diode (LED) driver comprising:

an input for receiving a signal according to the communications protocol as claimed in any one of claims 1 to 4;

means for controlling an associated LED in accordance with the at least one instruction in the first Command packet; and

an output for outputting the at least one subsequent Command packet.

6. A Light Emitting Diode (LED) driver as claimed in claim 5 further comprising means for separating the first Command packet from the signal.

7. A Light Emitting Diode (LED) comprising an LED driver as claimed in claim 5.

8. A device for controlling a plurality of LEDs, the device comprising:

means for generating and outputting a signal comprising a START code, a first Command packet and at least one subsequent Command packet;

first means for receiving the signal and controlling an LED associated with the first means in accordance with instructions in the first Command packet;

first means for separating the first Command packet from the signal to provide a remaining signal; and

means for outputting the remaining signal.

9. A device as claimed in claim 8 wherein the means for generating is a microprocessor.

10. A device as claimed in claim 9 wherein the first means for receiving and controlling, the first means for separating and the means for outputting comprise an LED driver.

11. A device as claimed in claim 10 wherein the LED driver is a microprocessor.

12. A device as claimed in claims 10 to 11 further comprising at least one subsequent driver associated with at least one subsequent LED.

13. An electronic device comprising:

a plurality of Light Emitting Diodes (LEDs);

a plurality of LED drivers as claimed in claim 5 for controlling a respective one of the plurality of Light Emitting Diodes; and

a microprocessor for generating and outputting a signal according to the communications protocol as claimed in any one of claims 1 to 4 to a first of the plurality of LED drivers.

14. A method for controlling a plurality of LEDs, the method comprising:

generating and outputting a signal comprising a START code, a first Command packet and at least one subsequent Command packet;

receiving the signal and controlling an LED in accordance with instructions in the first Command packet;

separating the first Command packet from the signal to provide a remaining signal; and

outputting the remaining signal.

15. A machine readable medium containing machine executable instructions to perform the method of claim 14.

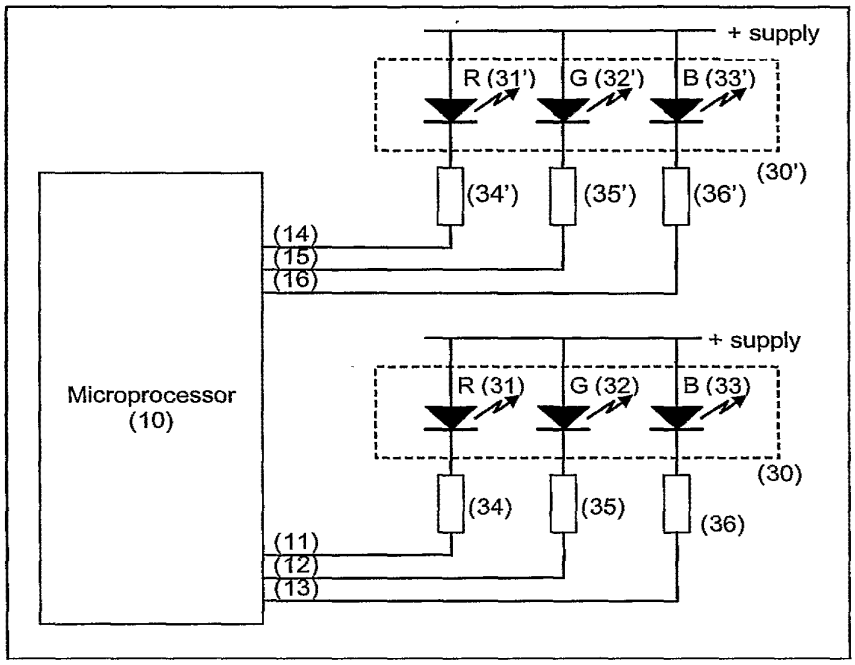


Figure 1

Prior Art

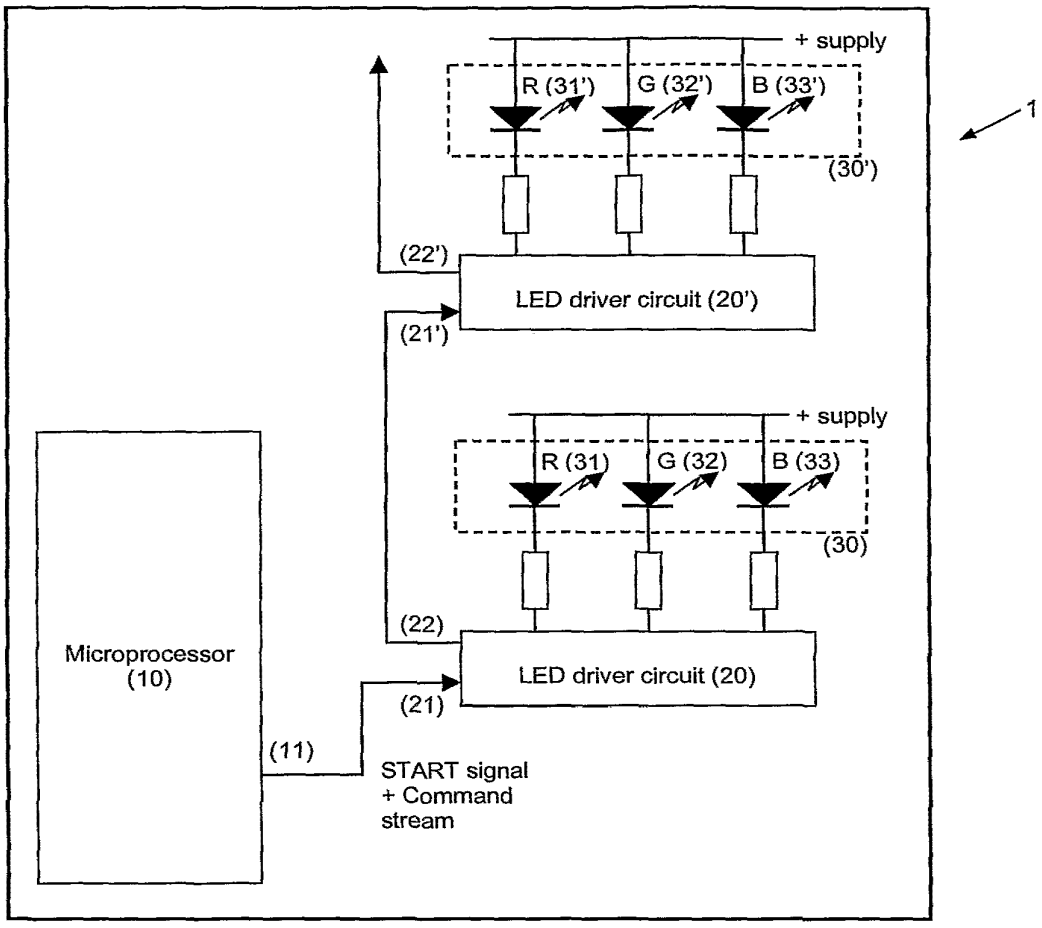

+ supply
R (31')
G (32')
B (33')
(30')
1
(22')
LED driver circuit (20')
(21')
+ supply
R (31)
G (32)
B (33)
(30)
(22)
Microprocessor
(10)
LED driver circuit (20)
(21)
(11)
START signal
+ Command
stream

Figure 2

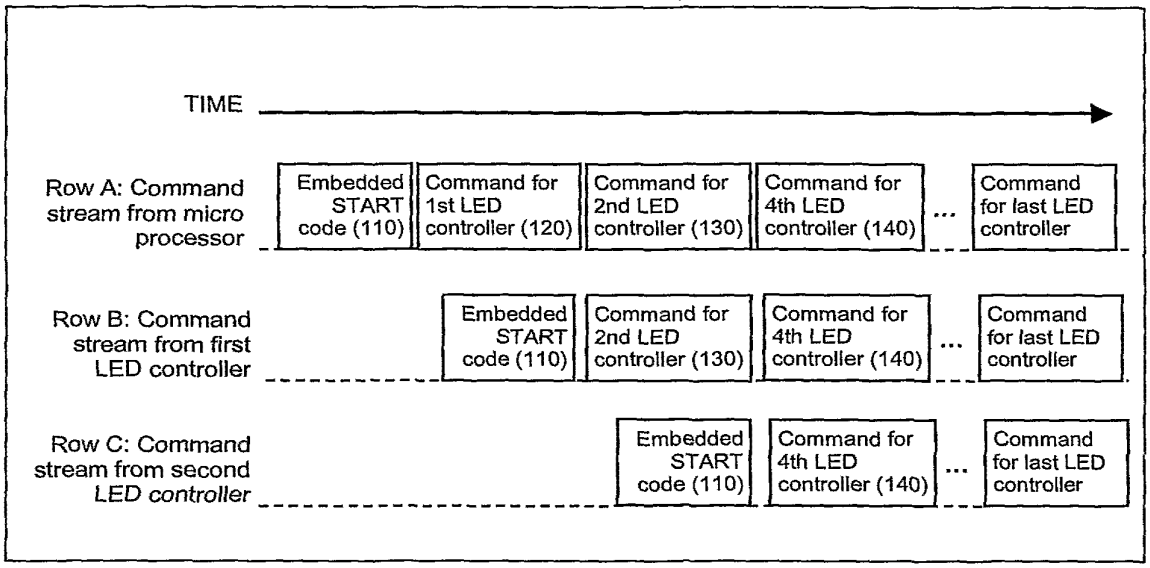


Figure 3

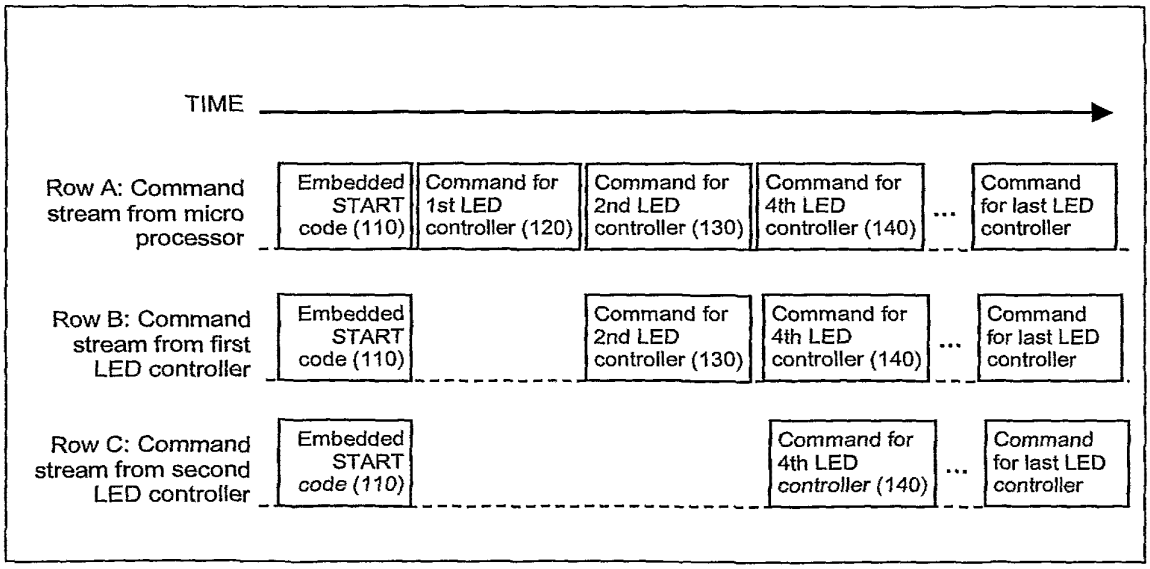


Figure 4

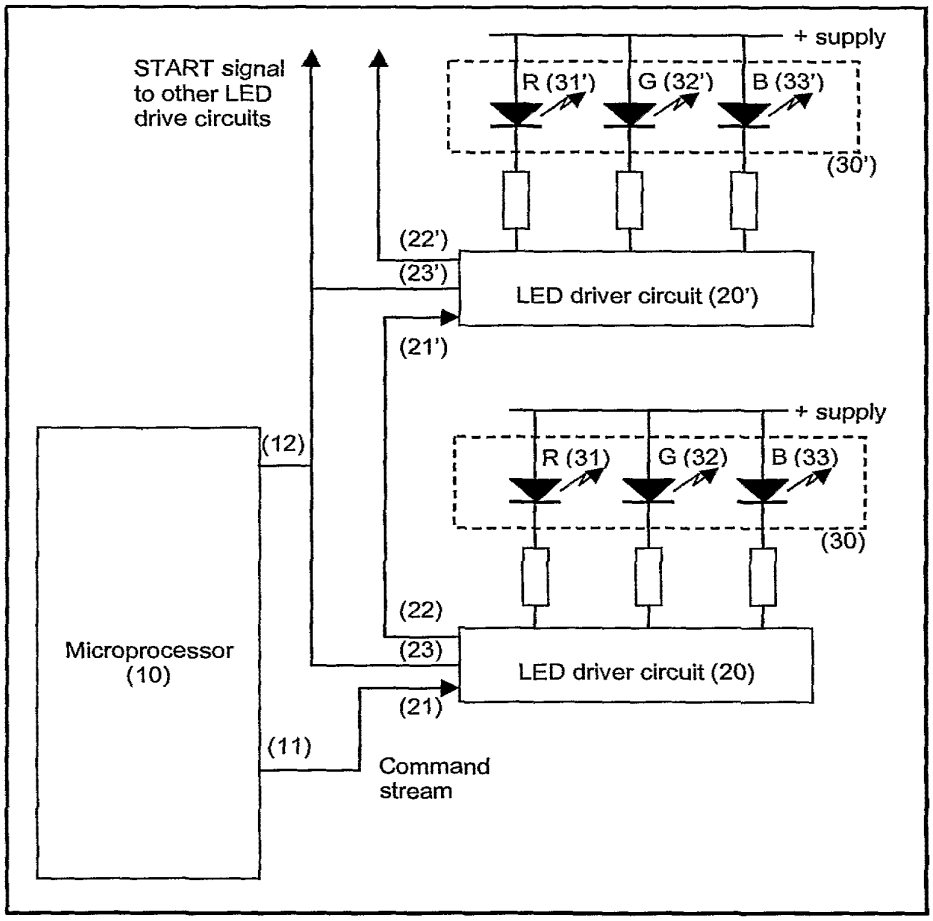

START signal
to other LED
drive circuits
+ supply
R (31')
G (32')
B (33')
(30')
(22')
(23')
LED driver circuit (20')
(21')
+ supply
R (31)
G (32)
B (33)
(30)
(12)
(22)
(23)
LED driver circuit (20)
(21)
Microprocessor
(10)
(11)
Command
stream

Figure 5

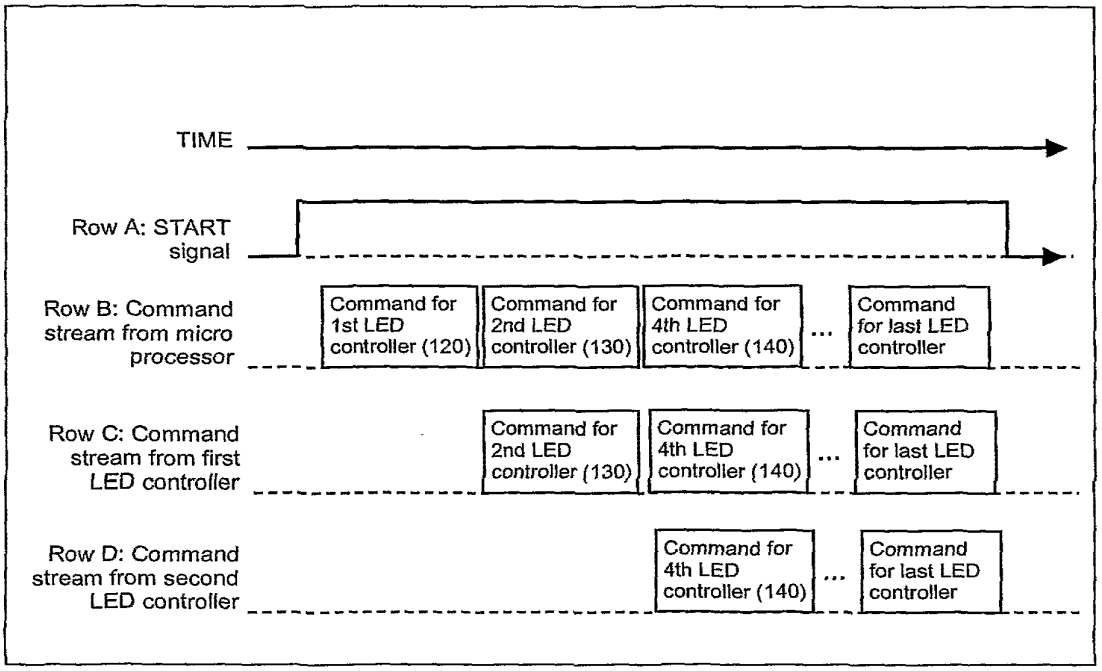

TIME
Row A: START signal
Row B: Command stream from micro processor
Command for 1st LED controller (120)
Command for 2nd LED controller (130)
Command for 4th LED controller (140)
...
Command for last LED controller
Row C: Command stream from first LED controller
Command for 2nd LED controller (130)
Command for 4th LED controller (140)
...
Command for last LED controller
Row D: Command stream from second LED controller
Command for 4th LED controller (140)
...
Command for last LED controller

Figure 6

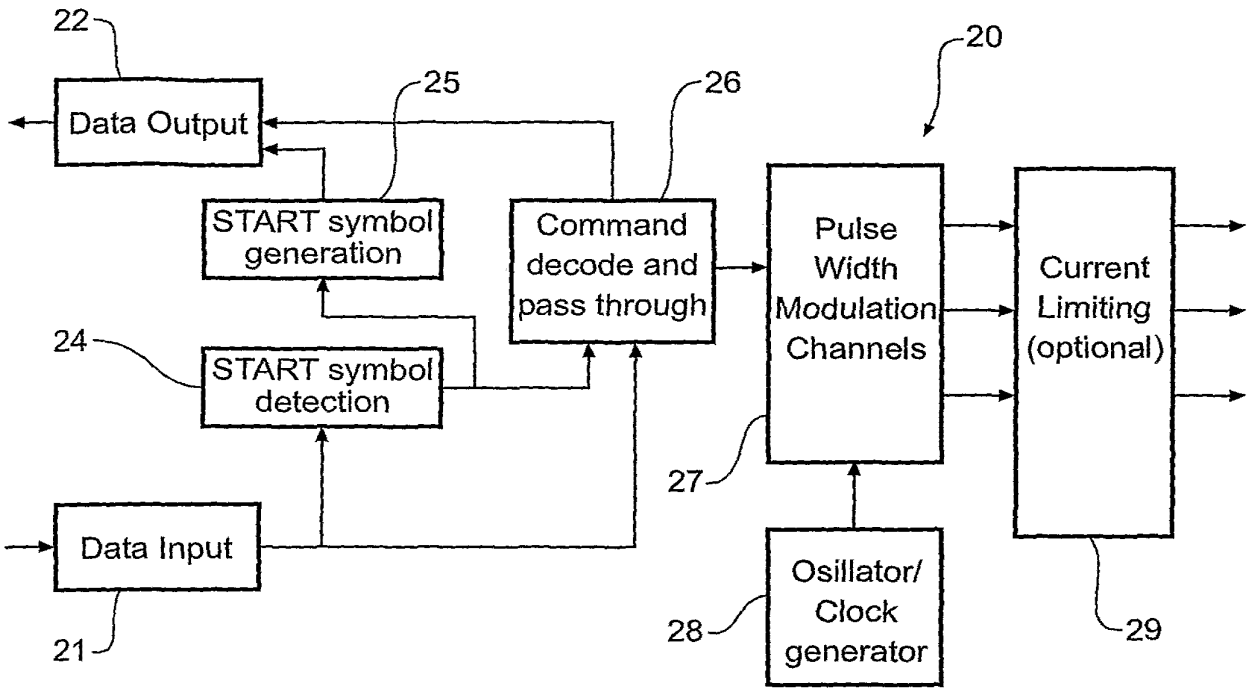


Figure 7

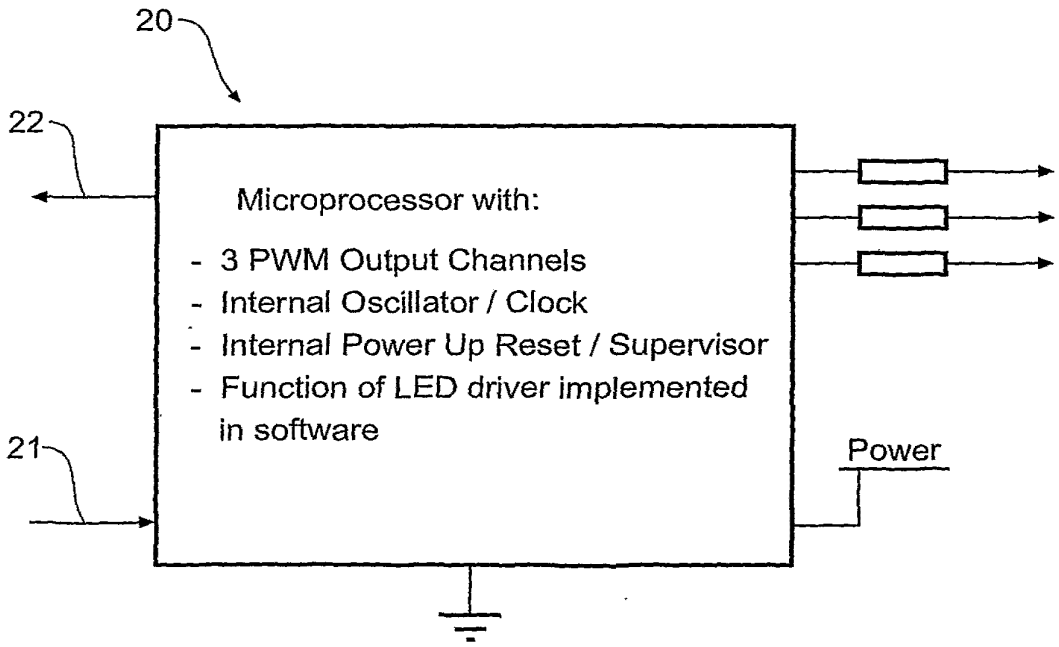


Figure 8

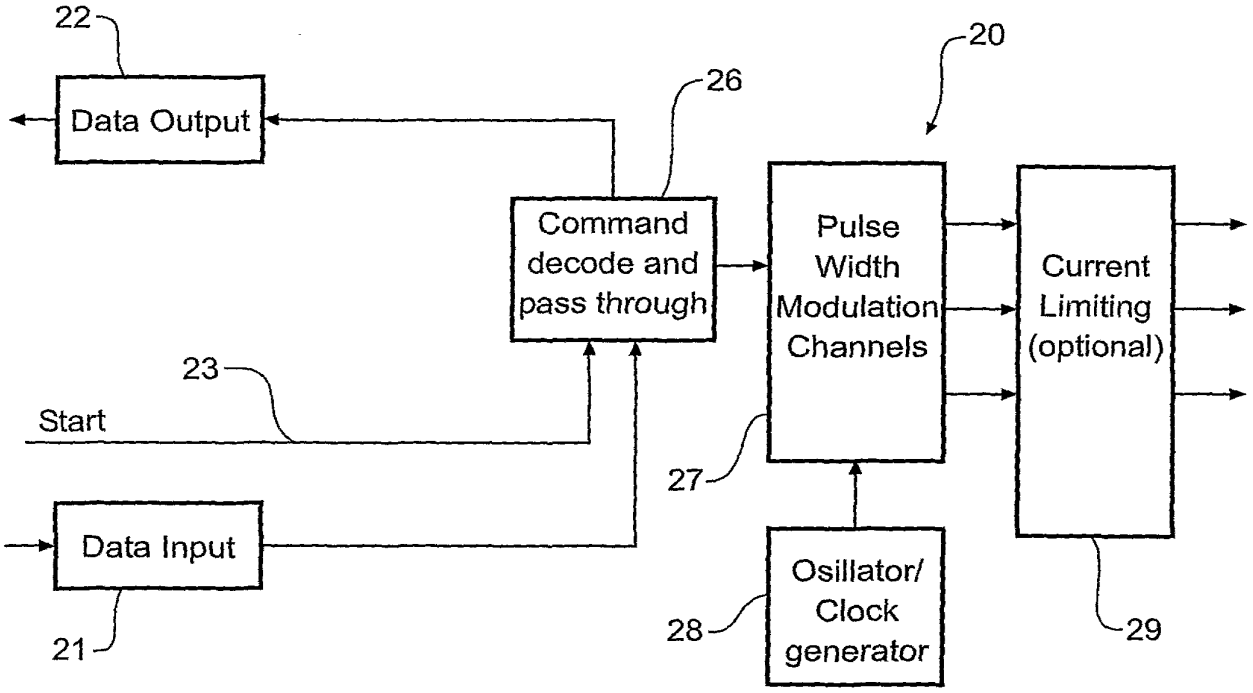

22
Data Output
26
20
Command decode and pass through
Pulse Width Modulation Channels
Current Limiting (optional)
23
Start
27
Data Input
21
Osillator/ Clock generator
28
29

Figure 9

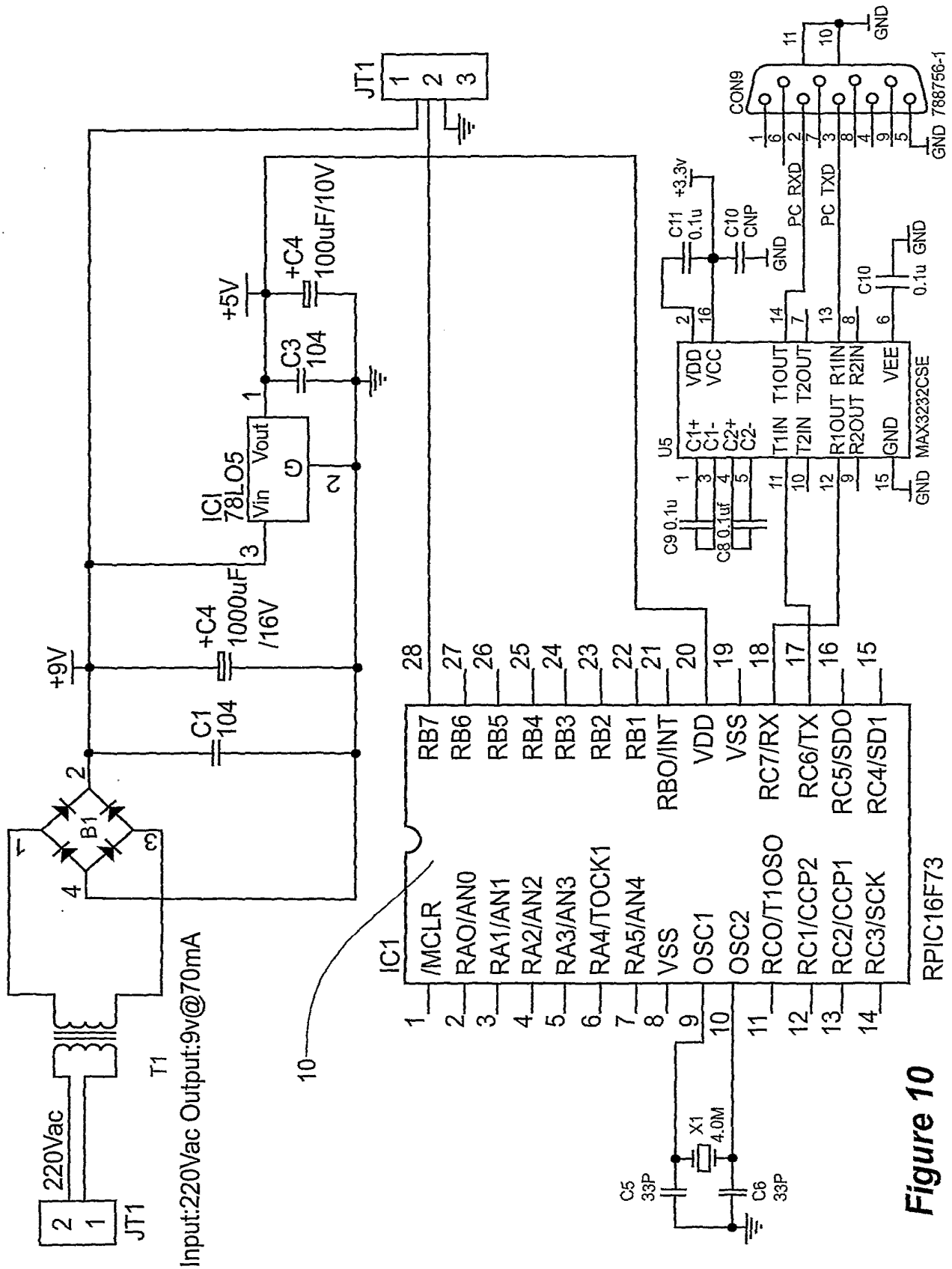

JT1
220Vac
Input:220Vac Output:9v@70mA
T1
B1
C1
104
+9V
+C4
1000uF
/16V
IC1
78L05
Vin
Vout
C3
104
+5V
+C4
100uF/10V
JT1
IC1
/MCLR
RA0/AN0
RA1/AN1
RA2/AN2
RA3/AN3
RA4/TOCK1
RA5/AN4
VSS
OSC1
OSC2
RC0/T1OSO
RC1/CCP2
RC2/CCP1
RC3/SCK
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0/INT
VDD
VSS
RC7/RX
RC6/TX
RC5/SDO
RC4/SD1
RPIC16F73
X1
4.0M
C5
33P
C6
33P
U5
MAX3232CSE
C8 0.1uf
C9 0.1u
C11 +3.3v
0.1u
C10
CNP
GND
PC RXD
PC TXD
CON9
788756-1

Figure 10

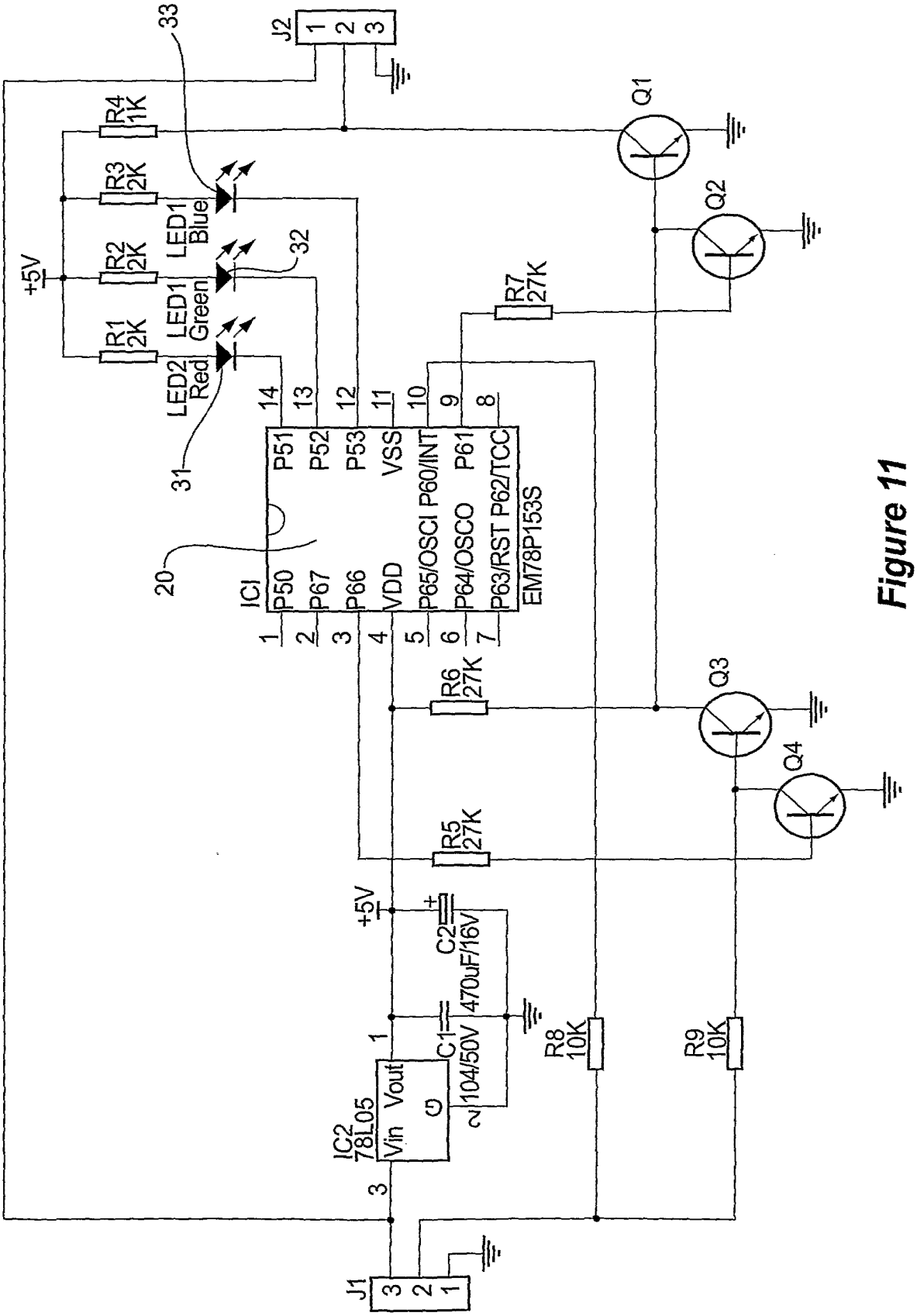

J2
1 2 3
33
R4 1K
R3 2K
LED1 Blue
R2 2K
LED1 Green
32
+5V
R1 2K
LED2 Red
31
20
Q1
Q2
R7 27K
14 13 12 11 10 9 8
P51 P52 P53 VSS P60/INT P61 P62/TCC
P50 P67 P66 VDD P65/OSCI P64/OSCO P63/RST
EM78P153S
ICI
1 2 3 4 5 6 7
R6 27K
Q3
Q4
R5 27K
+5V
C2 470uF/16V
C1 104/50V
IC2 78L05
Vin Vout
R8 10K
R9 10K
J1
3 2 1

Figure 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2007/001697

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H05B 37/02 (2006.01) ***G09G 3/14*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT: led control, driver, packets and similar terms
USPTO: controlling led, packets

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0257007 A1 (LYS et al.) 23 December 2004 Page 1 Para [0005]-Page 8 Para [0111]	1-15
A	US 2003/0057887 A1 (DOWLING et al.) 27 March 2003 Abstract	1-15

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 January 2008	10 JAN 2008
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **JUZER KHANBHAI** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No: (02) 6283 2176

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/AU2007/001697

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Member					
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	CA	2591205	CN	1809867	EP	1016062
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WO	2006069002	WO	2006069117	WO	2006071628

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	TIKKANEN, David; NEUDORF, Jason; LYONS, Steven; SCOTT, Todd, William; HATHAWAY, Kyle; JANSEN, David, Wainesworth
Serial No.:	
Filed:	September 17, 2009
Title:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
Group:	
Examiner:	
Attorney Ref.:	PAT 67545W-2

February 16, 2011

MAIL STOP AMENDMENT
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22314-1450
U.S.A.

Dear Sir:

Preliminary Amendment

Please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

Amendments to the Specification:

Please replace the first paragraph on page 1 of the specification, under the section heading "CROSS-REFERENCE TO RELATED APPLICATIONS", with the following amended paragraph:

This application is a national stage filing under 35 U.S.C. 371 of International Patent Application PCT/CA2009/001295, filed on September 17, 2009, which claims the benefit of priority of U.S. Provisional Application No. ~~61/097,063~~ 61/097,963, filed September 18, 2008, both of which ~~is~~ are incorporated herein by reference.

REMARKS

The cross reference to related applications has been amended to reflect the national stage application, and to correct a typographical error in the priority claim.

Entrance of this amendment is respectfully requested.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments, to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP

Respectfully submitted,
TIKKANEN, David et al.

By: /Jeffrey W. Wong/
Jeffrey W. Wong
Registration No. 46,414
Agent for Applicant

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
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(43) International Publication Date
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(10) International Publication Number
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PCT/CA2009/001295

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17 September 2009 (17.09.2009)

(25) Filing Language: English

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(30) Priority Data:
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(71) Applicant *(for all designated States except US)*: **E CRAFTSMEN CORPORATION** [CA/CA]; 73 Schaefer Street, Waterloo, Ontario N2L 4C4 (CA).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **TIKKANEN, David** [CA/CA]; 194 Silverwood Place, Waterloo, Ontario N2T 2R9 (CA). **NEUDORF, Jason** [CA/CA]; 306-30 Bridge Street West, Kitchener, Ontario N2K 1K4 (CA). **LYONS, Steven** [CA/CA]; 1011 Queen's Boulevard, Kitchener, Ontario N2M 1B8 (CA). **SCOTT, Todd, William** [CA/CA]; 581 Drummerhill Crescent, Waterloo, Ontario N2T 1G3 (CA). **HATHAWAY, Kyle** [CA/CA]; 5 Norbert Place, Kitchener, Ontario N2K 1E5 (CA). **JANSEN, David, Wainesworth** [CA/CA]; 333A Mayview Crescent, Waterloo, Ontario N2V 1P9 (CA).

(74) Agents: **WONG, Jeffrey W.** et al.; BORDEN LADNER GERVAIS LLP, World Exchange Plaza, 100 Queen Street, Suite 1100, Ottawa, Ontario K1P 1J9 (CA).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

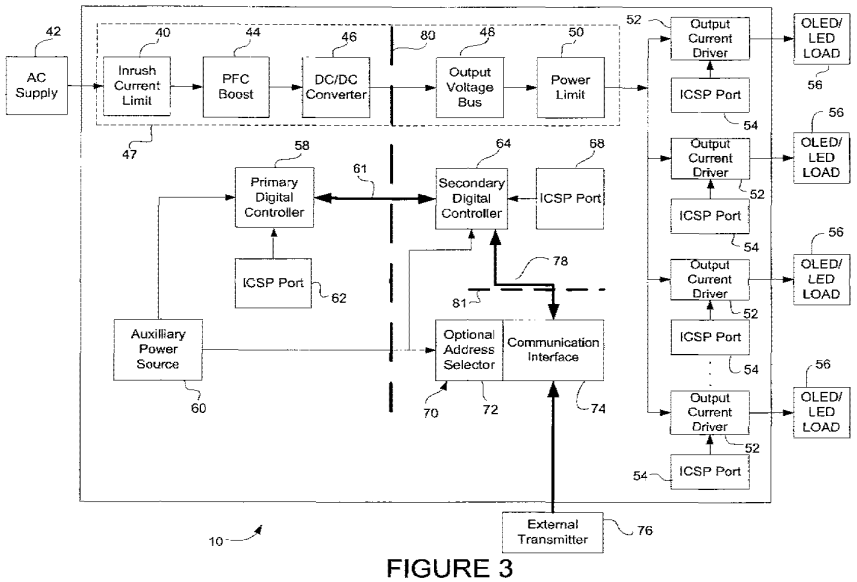


FIGURE 3

(57) Abstract: The disclosure is directed at a configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads comprising: a power circuit; a primary digital controller for controlling the power circuit; a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load; a secondary digital controller for controlling the set of output current drivers; wherein the secondary controller transmits LED control information to control outputs of the set of output current drivers; and wherein the secondary digital controller provides digital feedback control information to the primary digital controller.

WO 2010/031169 A1

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 61/097,063 September 18, 2008, which is incorporated herein by reference.

BACKGROUND OF THE DISCLOSURE

With the rapid increase in light emitting diode (LED) efficacies for high powered LEDs, the latest technologies have exceeded incandescent and halogen sources and are now starting to compete with fluorescent, mercury vapour, metal halide and sodium lighting. In addition to better energy usage, LEDs also have considerable advantages over traditional light sources such as long life, better durability and improved color generating abilities. The advancement of LED technology by various manufacturers has produced high power LEDs with various recommended drive currents such as 350 mA, 500mA, 700mA, 1000mA, and 1400mA or higher.

In recent years, controllable power sources for Solid State Lighting (SSL) applications have entered the market with integrated features. In addition, digital controllers within power sources have enabled the development of configurable options to provide a wider flexibility of solutions for Solid State Lighting applications. The ability to dim the light output of LEDs is also important to reduce energy consumption.

However, lighting companies are faced with considerable challenges in adopting SSL technology due to their unfamiliarity and lack of expertise in the driving and dimming requirements for LEDs.

Therefore, there is provided a novel LED Driver/dimmer for solid state lighting applications.

SUMMARY OF THE DISCLOSURE

With the wide variety of communication interface options and LED drive currents available for numerous architectural and entertainment Solid State Lighting applications, the configurable LED Driver/dimmer of the current disclosure includes at least one of the

following advantages: configurable output current options that maximize the available power in the "front end" PFC and isolated power conversion converter stage; multiple drive current options for the multiple LED drive current options for various LEDs; elimination of a cooling fan which can present issues with audible noise and flexibility in where the power source is located, relatively low standby power consumption during "black out" lighting conditions, where "black out" refers to no load operation on the output of the dimmer/driver; multiple communication interface options; the ability to map output current sources/channels to different DMX512A addresses and the ability to configure multiple groups of output current sources/channels such that each group is controlled by one 0 - 10 Vdc analog signal.

Some embodiments of the present disclosure are directed to a highly efficient enclosed, configurable power source, controllable by various external communication interfaces and a method for driving and dimming LEDs or OLEDs in lighting fixtures such as used for architectural or entertainment lighting applications. Such applications can include, but are not limited to, theater, convention centers, cruise ships, architectural building features, amusement parks, museums, and hospitality lighting in restaurants and bars.

In one aspect of the present disclosure, there is provided a configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads comprising: a power circuit; a primary digital controller for controlling the power circuit; a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load; a secondary digital controller for controlling the set of output current drivers; wherein the secondary controller transmits LED control information to control outputs of the set of output current drivers; and wherein the secondary digital controller provides digital feedback control information to the primary digital controller.

In another aspect of the present disclosure, there is provided a configurable power source that provides a plurality of output channels, such as 6, 8, 9, or 12, to color change or dim OLED or LED loads. In color changing applications, the number of available channels is a multiple of three or four to accommodate either red/green/blue LED loads or red/green/blue/amber or white LED loads. The number of output channels and available

output power is increased or maximized based on the LED current requirements. The output channels are programmable by means of in circuit serial programming (ICSP) ports and calibrated by a secondary digital controller to the required output current and other parameters such as dimming frequency range.

In another embodiment, the dimming of multiple monochromatic color or white LED loads (output channels) utilizing a single 0 - 10 Vdc analog control signal, or the control of groups of LED loads (output channels) with an associated 0 - 10 Vdc analog control signal for each group is contemplated.

In another aspect of the present disclosure, the output channels are digitally controlled current sources configurable for various peak currents to power and control a variety of LEDs. The LED average current is encoded within the three variables of on-time, off-time, and period whereby no three variables are held constant. Depending on the output drive currents of the LED loads, the number of available output channels is maximized based on the maximum output power available from the power factor and isolated DC/DC converter stages.

In another aspect of the present disclosure, the configurable power source is housed in a rectangular enclosure with a monolithic aluminum extrusion and a U shaped aluminum chassis and metal end plates. Various electrical components are thermally coupled to the heatsink to increase or maximize heat transfer to the outside surface of the enclosure.

In another aspect of the present disclosure, the power source includes a digital controller to decrease power consumption of a relay coil as part of an inrush current limit circuit to reduce power consumption and improve efficiency.

In another aspect of the present disclosure, the power source utilizes an independent efficient auxiliary power source and one or more digital controllers to provide power to the communication interface. A digital controller disables various electrical circuits during black out lighting conditions to reduce no load power consumption and improve efficiency.

BRIEF DESCRIPTION OF DRAWINGS

Embodiments of the present disclosure will now be described, by way of example only, with reference to the attached Figures, wherein:

Figure 1 is a perspective view of a configurable LED Driver/dimmer;

Figures 2a and 2b are cross-sectional views of the configurable LED Driver/dimmer;

Figure 2c is a schematic view of an internal layout of the LED Driver/dimmer;

Figure 3 is a schematic block diagram of the configurable LED Driver/dimmer;

Figure 4 is a schematic diagram of a prior art inrush current limit circuit;

Figure 5 is a schematic diagram of an embodiment of a novel inrush current limit circuit for use with the configurable LED Driver/dimmer;

Figure 6 is a schematic diagram of an embodiment of an output current driver;

Figure 7 is a schematic diagram of another embodiment of the output current driver;

Figure 8 is a schematic block diagram of another embodiment of the configurable LED Driver/dimmer;

Figure 9 is a schematic diagram of a prior art multistage power source;

Figure 10 is a schematic diagram of an embodiment of a novel multistage power source; and

Figure 11 is a schematic diagram of a communication interface for use with the configurable LED Driver/dimmer.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

In general, the present disclosure is directed at a method and apparatus for providing a configurable LED Driver/dimmer. In the current description, the Driver/dimmer will be referred to as a dimmer, however, it will be understood that the configurable apparatus can function as either a driver, a dimmer or both. In the preferred embodiment, the dimmer is used for Solid State Lighting (SSL) applications.

Turning to Figure 1, a perspective view of an LED dimmer is shown. The LED dimmer 10 includes a body portion 12, or housing, which includes a monolithic aluminum

heatsink 14 and a U-shaped chassis 16. Cross-sectional views of the dimmer 10 are provided in Figures 2a and 2b.

The dimmer 10 further includes a front plate 18 which includes a plurality of ports 20 along with a set of conductor cables 22. The front plate 18 is fastened to the body portion 12 via a set of fasteners 24, such as screws. In this embodiment, as conductor cables are used to provide output power to LED/OLED loads, the space requirement for the front plate 18 is reduced with respect to other known connection means such as terminal blocks.

Turning to Figures 2a and 2b, a pair of cross-sectional views of the LED dimmer are provided. Figure 2c is a schematic view of one embodiment of an internal layout of the dimmer 10. The cross-sectional views for Figures 2a and 2b are taken along lines A-A and B-B of Figure 2c respectively.

As shown, the heatsink 14 includes a receptacle portion 26 for receiving the ends of the chassis 16. In order to increase, or optimize, the heat dissipation capability of the configurable dimmer 10 at full output power, the extruded aluminum heatsink 14 includes fins 28 to increase the surface area for heat dissipation. The heatsink 14 also has a mounting platform 30 for receiving power components, or semiconductors 32, such as a bridge rectifier, MOSFETs, and/or diodes to efficiently transfer heat to the outside surface of the heatsink 14. These components will be discussed in more detail below with respect to Figure 3. A power factor inductor and main isolation transformer pair 34 are thermally coupled to the chassis 16 by a thermally conductive, electrically isolated material 36 to further improve heat dissipation of these components. A circuit board 38 is also mounted to the heatsink 14.

Turning to Figure 3, a block diagram of another embodiment of the LED dimmer is shown. The LED dimmer 10 includes an inrush current limit 40, or inrush current limit circuit, which receives power from an AC power source or supply 42, located external to the dimmer 10. The inrush circuit 40 is connected to a Power Factor Correction (PFC) Boost 44 which, in turn, is connected to a DC/DC Converter 46, or power conversion stage. The converter 46 is connected to an Output Voltage bus 48 which is connected to a power limiter 50. The inrush circuit 40, the PFC boost 44, the DC/DC converter 46, the Output Voltage Base 48 and the power limit 50 can be seen as a power circuit 47.

Although only one power limit 50 is shown, it will be understood that there could be multiple power limits. The power limiter 50 is connected to a set of output current drivers 52, whereby each of the output current drivers 52 has an associated in-circuit serial programming (ICSP) port 54. The output of the output current drivers 52 is connected to individual Organic Light-Emitting Diodes (OLED)/Light-Emitting Diodes (LED) loads 56, further referred to as LED loads.

Along with the above-identified components and circuitry, the dimmer 10 further includes a primary digital controller 58 which is connected to an auxiliary power source 60 and an ICSP Port 62. The primary digital controller 58 is further connected, via an isolated communication bus 66 to a secondary digital controller 64, which receives power from the auxiliary power source 60. An ICSP port 68 is also connected to the secondary digital controller 64.

The auxiliary power source 60 is also used to power an interface component 70 which includes an optional address selector 72 and a communication interface 74. The communication interface 74 receives inputs from an external transmitter 76 and communicates via an isolated serial communication bus 78 with the secondary digital controller 64. A set of isolation barriers 80 and 81 are located within the dimmer 10, each barrier separating various components of the dimmer 10 from each other.

As will be understood, not all of the components or connections of the LED dimmer 10 required for operation are shown as they will be understood by one skilled in the art. For instance, the dimmer 10 can also include an EMI filter and a bridge rectifier. With respect to connections, it will be understood that the primary digital controller 58 can also be connected to the PFC boost 44, the inrush current limit 40 and the DC/DC controller 46 while the secondary digital controller 64 can be connected to the output voltage bus 48, the power limit 50 and the output current drivers 52.

In operation, the PFC Boost 44 and DC/DC Converter 46 are controlled by the primary side digital controller 58 while the secondary digital controller 64 monitors the output voltage bus 48 and provides digital feedback control information via isolated communication bus 66 to regulate the output voltage bus 48. Secondary digital controller 64 also translates dimming and/or color mixing information from the external transmitter 76 into LED control information for the output current drivers 52. The primary 58 and

secondary 64 digital controllers and output current drivers 52 have an associated programming port for further configuring the LED dimmer 10.

Turning to Figure 4, a prior art inrush current limit is shown. In order to limit inrush current limit during initial start up of the power source, one approach is to utilize a negative temperature coefficient thermistor (NTC) in parallel with a relay contact. During initial turn on of the power source, the NTC thermistor limits the inrush current. When the PFC boost stage bulk capacitor is charged, and before the PFC stage is enabled by the primary controller, the primary controller closes the relay contact to bypass the NTC thermistor. This is accomplished by applying a DC voltage via a switch across the coil in the relay.

A limitation of this approach is the power consumption of the relay coil when a continuous DC voltage is applied. This power consumption becomes significant in terms of Energy Star requirements during no load or standby operation such as when a "black out" or minimum light intensity state is received by the communication interface.

Turning to Figure 5, an embodiment of an improved inrush current limit 40 is shown. An EMI filter 82 is connected between the power supply and the current limit 40 and is connected directly to the PFC boost 44 and via the current limit 40. The current limit 40 includes a thermistor 84, a relay coil 86 and a switch 59. The relay coil 86 is connected in parallel with the thermistor 84. A typical relay coil requires greater energy to close the contacts than is required with the currently described limiter 40 to maintain the contacts in a closed position since less holding force is required. After the relay contacts have been closed by applying a voltage of 12 Vdc, modulation of the relay coil voltage can be initiated by the primary controller 58 to effectively reduce the average voltage across the coil to approximately 5 volts versus a DC voltage of 12V, reducing power consumption. It should be noted that the pulse duty cycle and frequency can also be changed to improve or optimize performance.

In one embodiment, the primary controller 58 pulses the DC voltage across the relay coil via the switch 59 to reduce power consumption.

In one embodiment, for the PFC boost 44, as shown in Figure 3, the PFC Boost 44 utilizes a boost topology with an input AC voltage mains range of 103 Vac to 300 Vac from the AC supply 42. Energy stored in an inductor within the PFC boost 44 is

transferred and stored in the bulk capacitor on a cycle by cycle switching basis at a loosely regulated 430V DC over the input range. The energy is controlled in a manner that forces AC input current to be sinusoidal and in phase with the AC line voltage. By drawing current in phase with the input mains voltage 42, the amount of harmonic currents of the fundamental AC mains frequency being introduced into the power line is reduced.

For the DC/DC convertor 46 and the output voltage bus 48, the preferred embodiment for the DC/DC converter 46 is derived from the isolated buck converter topology and comprises a galvanically isolated full bridge converter employing a primary side phase modulation technique with a secondary side current doubler rectifier circuit.

The full bridge converter parasitic circuit elements in conjunction with primary magnetization current and reflected inductor ripple current cause resonant edge switching transitions on the MOSFET switch thus forcing zero voltage across the MOSFET switching device before turn on. The result is higher efficiency due to the elimination of Coss (drain to source MOSFET Capacitance) switching losses, reduction of gate charge across the Miller capacitance and minimized power loss during switching transitions when voltage and current are changing simultaneously.

Since the output of the DC/DC converter is a tightly regulated DC bus 48, the set of power limit circuits 50 are coupled to either one or more current drivers 52 to limit the power output of each of the output current drivers. 52 The power limit circuits 50 each include a current sensor that is monitored by the secondary controller 64. In the event of a single component failure within the output current driver module, the power limit circuits 50 limit the energy to the loads in accordance with the UL standard 1310 Class 2. Supplementary protection to the power limit circuits can also include one or more fuses.

For the primary digital controller 44, the controller 44 provides digital feedback control for the PFC Boost 44 and DC/DC Converter 46. The digital feedback method for the PFC Boost 44 utilizes average current mode control with duty cycle feed forward for the inner current loop and voltage mode control for the outer control loop. The DC/DC Converter 46 utilizes voltage mode control for the digital control loop.

The primary digital controller 44 also controls the inrush current limit circuit 40, provides primary current limit protection, and over voltage protection for the output of the

PFC Boost 44. The primary digital controller 44 also disables the PFC Boost 44 and the DC/DC Converter 46 during black out or no load conditions to reduce power dissipation.

With respect to the output current drivers 52, configuring the required number of outputs and required output current is accomplished by populating the appropriate sections of a single printed circuit board with the appropriate electrical components and programming the output current driver via the in-circuit serial programming (ICSP) ports 54.

Turning to Figure 6, which is an embodiment of an output current driver, the output current driver 52 comprises a load controller 90, a current source 92, and current sense 94. Although only one current driver 52 is shown, it will be understood that multiple are present as reflected in Figure 3.

The output current driver utilizes the dimming/color mixing techniques for LEDs described in detail in US Patent Publication No. 2007/0103086, which is hereby incorporated by reference, wherein the LED average current is encoded within the three variables of on time, off time, and period where by no three variables are held constant.

The secondary controller 64 receives dimming or color mixing information in the form of a serial data stream from the external transmitter 76 via the communication interface 74 and then translates the data stream into LED control information. The LED control information is transmitted to the load controller 90 in the form of instructions to generate a digital signal 98 and an analog signal 100.

The load controller 90 further comprises a signal generator 102 which transmits the digital signal 98 and the analog signal 100 to the current source 92. The digital control signal 98 and the analog signal 100 are preferably generated via a digital control algorithm and 1 Bit algorithm, respectively.

The current source 92 preferably includes ancillary circuitry for operation and comprises a buck topology power stage with hysteretic control. The current sense 94 provides a digital feedback loop for each current source 92. In the preferred embodiment, the current source 92 is a buck circuit topology however other embodiments can include topologies such as boost, buck-boost, or single ended primary redactor convertor (SEPIC).

Output 104 of the current driver 52 provides a current pulse via current source 92 to the LED Load 56 whereby on times, off times, and period are not held constant.

Each output current driver 52, has an associated in-circuit serial programming (ICSP) port 54. The ICSP port 54 provides access to the load controller 90 such that firmware updates are possible to permit the configuration of the output current drivers 52. The ICSP port(s) 54 for the output current driver(s) 52 can be located on the printed circuit board assembly of the apparatus or they can be located on the outside of the enclosure.

The configuration options include, but are not limited to, such parameters as the adjustment of the frequency range of the dimming current pulse for the range of light intensity output or the set point adjustment of the peak on time output current.

For example, it might be necessary to increase the frequency range of the dimming current pulse in video recording applications where the dimming current pulse frequency can be programmed for a 2000Hz to 2500Hz range. This would negate a visible beat frequency effect that would other wise be noticeable on recorded video. There can be other applications where the adjustment of the dimming current frequency range is required to reduce EMI effects.

The default peak output current set point is programmed via the ICSP port 54 which provides flexibility in the number of possible LEDs types that can be driven and is typically dependent on the recommended operating current specified by the manufacturer such as 350mA, 700mA, etc. The set point current is preferably programmed to within 4% of the manufacturer's specification. The peak output current set point can then be precisely calibrated to within typically 1% via the secondary controller 64 during factory calibration.

An alternate embodiment of an output current driver 52 is shown in Figure 7. In this embodiment, the output current driver 52 comprises a load controller 110 including a signal generator 112. A current source 114 and a current sense 116 are located within an apparatus 118, such as a light fixture. The light fixture 118 also includes the LED load 56. After receiving the LED control information from the secondary controller 64, the signal generator 112 provides a data signal to the light fixture 118 to operate the LED load 56 via the current source 114 and the current sense 116. This is also schematically shown in Figure 8.

Figure 8 is a schematic diagram of an alternate embodiment of a configurable LED dimmer 10. As shown, individual current sources 114 and current senses 116 are mounted

in the light fixture containing the LED load 56, and power and data signals are provided to each output current source 114 by the multi conductor cable 22. In this embodiment, the current sources 114 are configured to regulate to a predetermined peak current. The load controller 64 transmits the data signal containing the output current information encoded within the three variables of on time, off time, and period whereby no three variables are held constant.

Turning to Figure 9, a known application of internal auxiliary power requirements in a multistage power source is shown and illustrates how auxiliary power is provided to the various blocks of a multistage power source. P1, P2...P10 represents the various power and voltage transfer requirements for each functional block. For simplicity, the various voltage regulator and filter circuits required for each of the power outputs have been omitted.

In operation, the bridge rectifier converts the AC mains voltage P1 to a rectified voltage P2. A portion of power P6 from the output of the bridge rectifier P2 is supplied to the start up circuit. The start up circuit is comprised of a power transistor or MOSFET and is intended to provide power P8 to the PFC analog controller for only a short duration of a few seconds. Power P8 to the PFC analog controller will allow the PFC Boost stage to begin switching, providing power P10 to the DC/DC controller, and power P3 to the DC/DC converter power stage. Since the start up circuit dissipates an excessive amount of power, it is turned off by the voltage component of P7 supplied by the PFC boost stage. The P7 power is permitted to 'flow through' the start up circuit to continue to supply power P8 to the PFC analog controller.

The output of the DC/DC Analog Converter provides power P4 to the multi output voltage bus, power P9 to the Communication Interface, and the Output Current Drivers by means of P5.

In this implementation, the PFC and DC/DC Controllers are typically analog controllers. It should be noted that in this implementation, in order for the communication interface to continually receive dimming information from an external transmitter, the DC/DC Converter stage must remain turned on. Similarly, in order for the DC/DC converter stage to provide power P4, the PFC Boost stage must remain on.

In a 'black out' state, the communication interface may receive a "0" intensity value out of 255 intensity levels for all of its output current drivers via the external transmitter such as a DMX512A or RDM controller interface, or it may receive an analog voltage of between 0 to 1V via a controller compliant to ESTA E1.3-2001 or IEC60929 as one of many communication interface options. In this 'black out' state, the DC/DC Converter and PFC Boost Stage continue to dissipate an excessive amount of power.

Figure 10 is directed at an embodiment of an improved internal auxiliary power distribution in a multistage power source for providing auxiliary power to the various blocks of a multistage power source. For simplicity, the various voltage regulator and filter circuits required for each of the power outputs have been omitted. The transfer of power from AC mains to the Output Current Drivers (52) is unchanged. This embodiment shows an improved implementation of an independent auxiliary power source providing power to the primary digital controller 58, the secondary digital controller 64, and the communication interface 74. The auxiliary power source 60 comprises an efficient isolated flyback topology with a wide input voltage range and pulse skipping capability to minimize its power dissipation at light loads or no load conditions. In other words power can be provided to the primary digital controller 58, the secondary digital controller 64, and the communication interface 74 via an auxiliary flyback converter.

A 'black out' state received from the external transmitter 76 to the communication interface 74 is communicated to the secondary digital controller 64 and then the primary digital controller 58 via the isolated communication bus 66. The primary digital controller 58 then disables the PFC Boost Stage 44 and DC/DC Converter Stage 46 reducing overall power dissipation of the configurable power source.

It should be noted that even when the PFC Boost 44 is disabled, power can continue to be supplied to the auxiliary power source 60 since rectified voltage from a bridge rectifier 120 can continue to peak charge the PFC boost 44 through an internal capacitor via the boost diode.

The auxiliary power source 60 continues to provide power to the primary digital controller 58, secondary digital controller 64, and communication interface 74 in order to be able to 'listen' for or sense a change in light intensity state that may be communicated by the external transmitter 76.

Alternate embodiments can include additional ancillary circuits that can be powered by the independent auxiliary power source that can be disabled by a controller to reduce over all power dissipation in black out or no load conditions.

With respect to the communication interface 74, the communication interface 74 comprises a removable and interchangeable module with each module adapted for different control options such as DMX512A, RDM, 0 - 10 Vdc and Zigbee. Operation of the communication interface with such control options will be understood by one skilled in the art.

The communication interface module receives lighting control information via the external transmitter 76 and converts the various protocols into a serial data stream. It then transmits this data by means of a Universal Asynchronous Receiver Transmitter (UART) to the secondary digital controller 64 via the isolated serial communication bus 78. The isolated serial communication bus 78 is comprised of a isolation barrier 82 to "float" the communication interface and prevent ground loops.

Turning to Figure 11, an embodiment of the communication interface is shown. In this embodiment, an analog interface module adapted for 0 - 10 Vdc IEC60929 or ESTA E1.3-2001 dimming methods as the communication interface 74 is shown. The analog interface module can be adapted to receive one or more analog control voltages from one or more associated external transmitters 76. The external transmitter 76 is preferably an electronic resistor or potentiometer that sinks current from the current source located on the analog interface module and outputs a variable 0 - 10 Vdc control voltage proportional to the required light intensity.

Individual external transmitters 76 supply signals to various controls 122 within the communication interface 74. Each control 122 is representative of an area or group of LED loads 56. Within each control 122 is a current source 124, a voltage sensor 126 and a differential amplifier 128. The differential amplifier 128 senses a voltage across the voltage sensor 126 and converts this into a correlated voltage (Vm,V1,V2...Vn) supplied to a controller 130. The controller 130 converts this analog voltage into a serial data stream for transmission to the secondary digital controller 64 via the isolated serial communication bus 78.

The communication interface 74 can be configured to have one 0 – 10 Vdc control voltage simultaneously control via the secondary digital controller 64, all output current drivers 52 and LED loads 56. This application is beneficial in monochromatic color or white lighting applications since only one control signal and associated wiring is required to control multiple light loads.

Furthermore, the communication interface 74 can be adapted to have one or more 0 - 10 Vdc signal voltages control an associated group of one or more output current drivers in zone dimming applications. An optional master 0 - 10 Vdc signal voltage could be able to simultaneously control all of the individual groups of output current drivers.

In applications not requiring the complexity of DMX512A, these analog control options are beneficial in red/green/blue or red/green/blue/amber color changing or monochromatic color or white light applications whereby the addressability and corresponding control of individual LED light loads is not required.

With respect to the secondary digital controller 64, the controller 64 monitors and transmits digital output voltage bus information (feedback loop) via the two way isolated serial communication bus 78, decodes the serial data from the communication interface 74, and transmits control information to the output current drivers 52. As a protection feature, the secondary controller 64 also monitors output currents from the power limit stages 50 supplied to the output current drivers 52

The secondary digital controller 64 includes the ICSP port 68 to program and calibrate the output voltage bus 48 to the required voltage. In DMX512A applications, the ICSP port 68 also allows for the mapping of each of the output channels to a wide variety of addresses. Similarly, in 0 - 10 Vdc analog control applications, the secondary digital controller ICSP port allows for the mapping of output channels into groups for each associated 0 - 10Vdc control signal.

This mapping capability is particularly useful in addressable-networked lighting systems using a DMX512A control protocol where different lighting zones are required to respond to different illumination information. For example, in a 12 channel output configuration, the first 6 channels could be mapped to the DMX base address of the power source (ie DMX01) and the last 6 channels could be mapped to DMX address +1 (i.e. DMX02).

This mapping capability is also useful in zone dimming applications using 0 - 10 Vdc analog controls as the communication interface. For example, a 12 channel output LED dimmer configuration can have 7 output channels grouped for a first associated 0 - 10 Vdc signal, the next 3 channels can be grouped to a second associated 0 - 10 Vdc control signal, and the last 2 channels can be grouped to a third associated control signal.

Embodiments of the disclosure can be represented as a software product stored in a machine-readable medium (also referred to as a computer-readable medium, a processor-readable medium, or a computer usable medium having a computer-readable program code embodied therein). The machine-readable medium can be any suitable tangible medium, including magnetic, optical, or electrical storage medium including a diskette, compact disk read only memory (CD-ROM), memory device (volatile or non-volatile), or similar storage mechanism. The machine-readable medium can contain various sets of instructions, code sequences, configuration information, or other data, which, when executed, cause a processor to perform steps in a method according to an embodiment of the disclosure. Those of ordinary skill in the art will appreciate that other instructions and operations necessary to implement the described disclosure can also be stored on the machine-readable medium. Software running from the machine-readable medium can interface with circuitry to perform the described tasks.

The above-described embodiments of the disclosure are intended to be examples only. Alterations, modifications and variations can be effected to the particular embodiments by those of skill in the art without departing from the scope of the disclosure, which is defined solely by the claims appended hereto.

What is claimed is:

1. A configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads comprising:

a power circuit;

a primary digital controller for controlling the power circuit;

a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load;

a secondary digital controller for controlling the set of output current drivers;

wherein the secondary controller transmits LED control information to control outputs of the set of output current drivers; and

wherein the secondary digital controller provides digital feedback control information to the primary digital controller.

2. The LED driver/dimmer of Claim 1 wherein the power circuit comprises:

an inrush current limit;

a power factor conversion (PFC) boost;

a DC/DC converter;

an output voltage bus; and

at least one power limit.

3. The LED driver/dimmer of Claim 1 further comprising:

a set of in-circuit serial programming (ICSP) ports, each of the set of ICSP ports associated with one of the set of output current drivers for dynamic control of the output current drivers.

4. The LED driver/dimmer of Claim 1 further comprising an in-circuit serial programming (ICSP) port connected to the primary digital controller.

5. The LED driver/dimmer of Claim 1 further comprising an in-circuit serial programming (ICSP) port connected to the secondary digital controller.

6. The LED driver/dimmer of Claim 1 further comprising a communication interface for receiving data from an external transmitter and for transmitting the data to the secondary digital controller.

7. The LED driver/dimmer of Claim 1 further including an isolation barrier for separating the secondary digital controller and the communication interface.

8. The LED driver/dimmer of Claim 1 further comprising a housing portion for housing the components of the driver.

9. The LED driver/dimmer of Claim 8 wherein the housing portion comprises:
an aluminum heatsink; and
a U-shaped chassis.

10. The LED driver/dimmer of Claim 9 wherein the heatsink comprises a plurality of fins.

11. The LED driver/dimmer of Claim 10 wherein heatsink acts to cool the driver/dimmer via convection cooling.

12. The LED driver/dimmer of Claim 9 further comprising a thermally conductive electrically isolated material for coupling the power circuit to the chassis to further improve heat dissipation. .

13. The LED driver/dimmer of Claim 6 wherein the communication interface is either DMX512A, 0-10Vdc analog control, Zigbee wireless or Remote Device Management (RDM) compatible.

14. The LED driver/dimmer of Claim 2 wherein the inrush current limit comprises:
a switch;

a relay coil, connected to the switch; and

a thermistor;

wherein the relay coil and the thermistor are in parallel with each other.

15. The LED driver/dimmer of Claim 1 wherein the light fixture load is one of an Organic LED (OLED) load or an LED load.

16. The LED driver/dimmer of Claim 2 comprising an auxiliary flyback converter to provide power to the primary digital controller, secondary digital controller, and communication interface

17. The LED driver/dimmer of Claim 2 wherein the primary digital controller can disable the PFC boost and DC/DC Converter at zero light intensity state.

18. The LED driver/dimmer of Claim 5 comprising a means to map output current drivers to various DMX512 addresses.

19. The LED driver/dimmer of Claim 5 comprising a means to map output current drivers to various dimming zones for 0-10 Vdc control.

20. The LED driver/dimmer of Claim 5 further comprising an isolated communication bus to transmit the digital feedback control into the PDC.

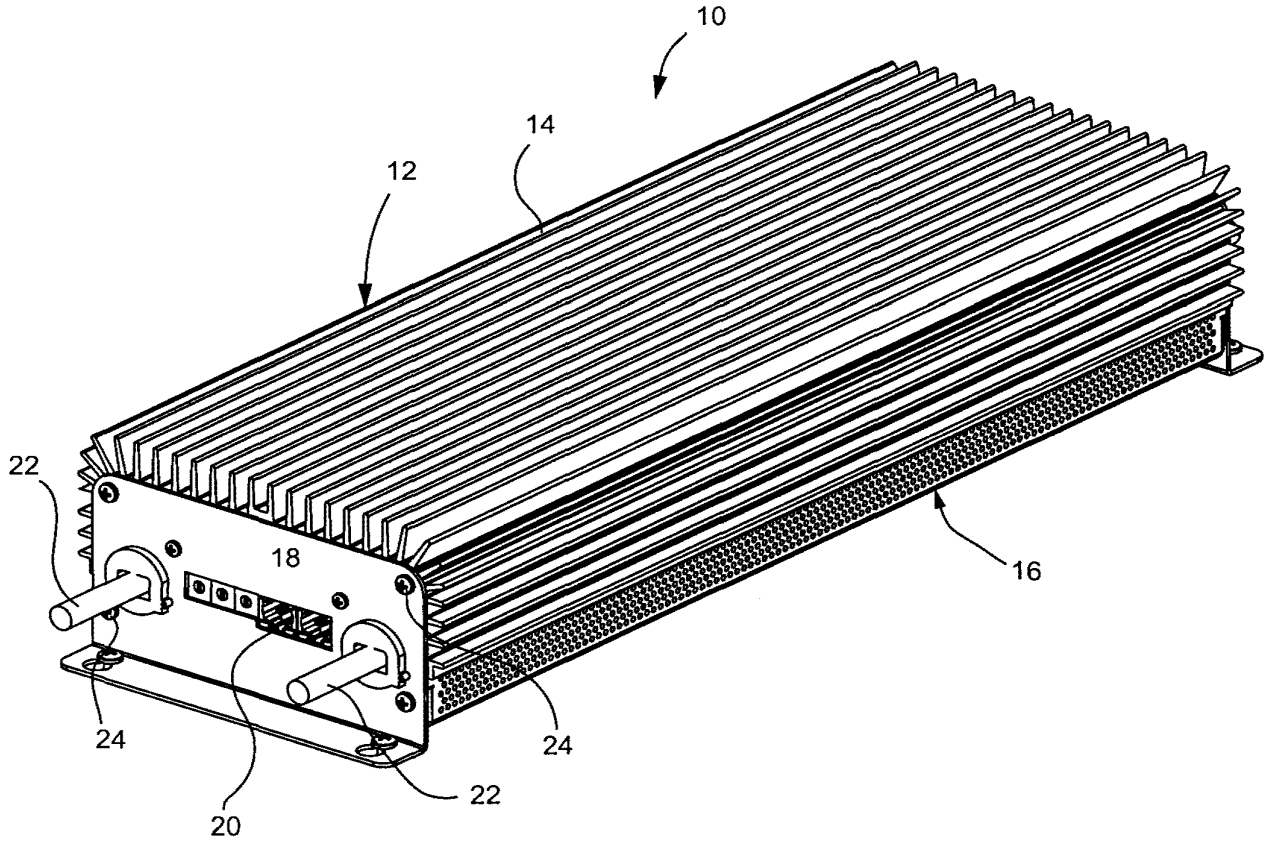


FIGURE 1

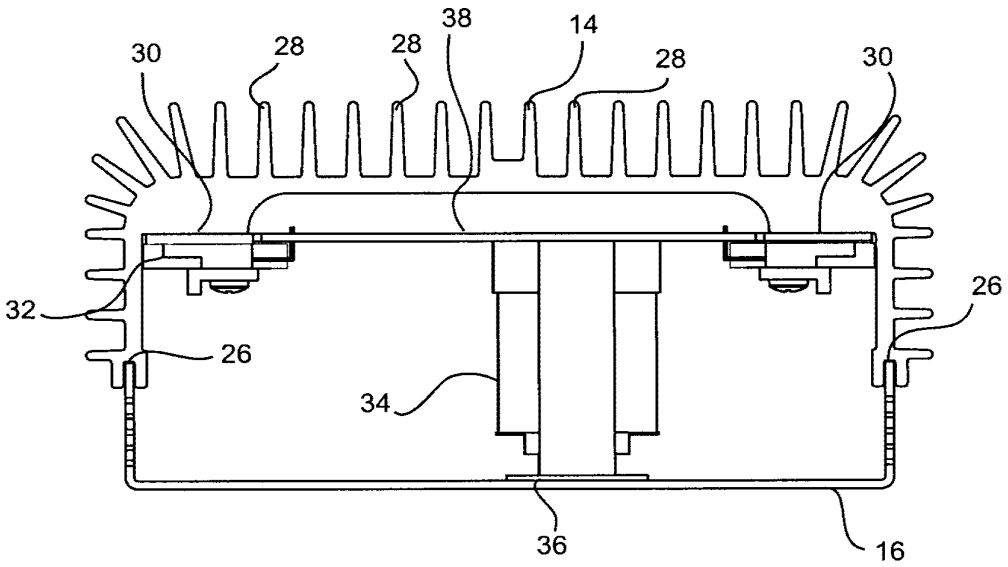


FIGURE 2a

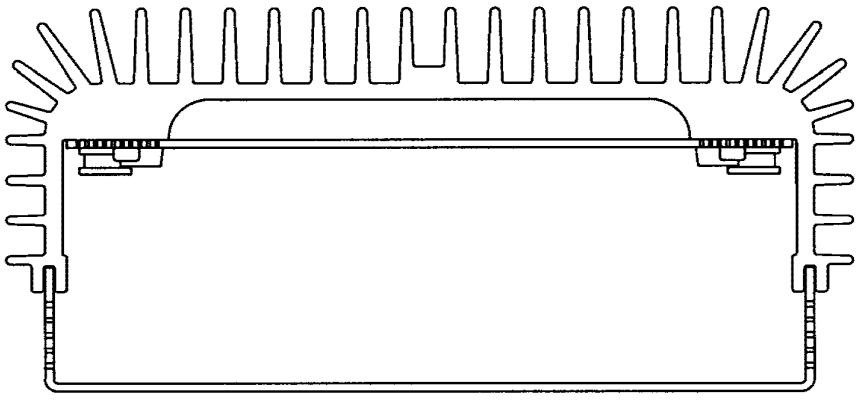


FIGURE 2b

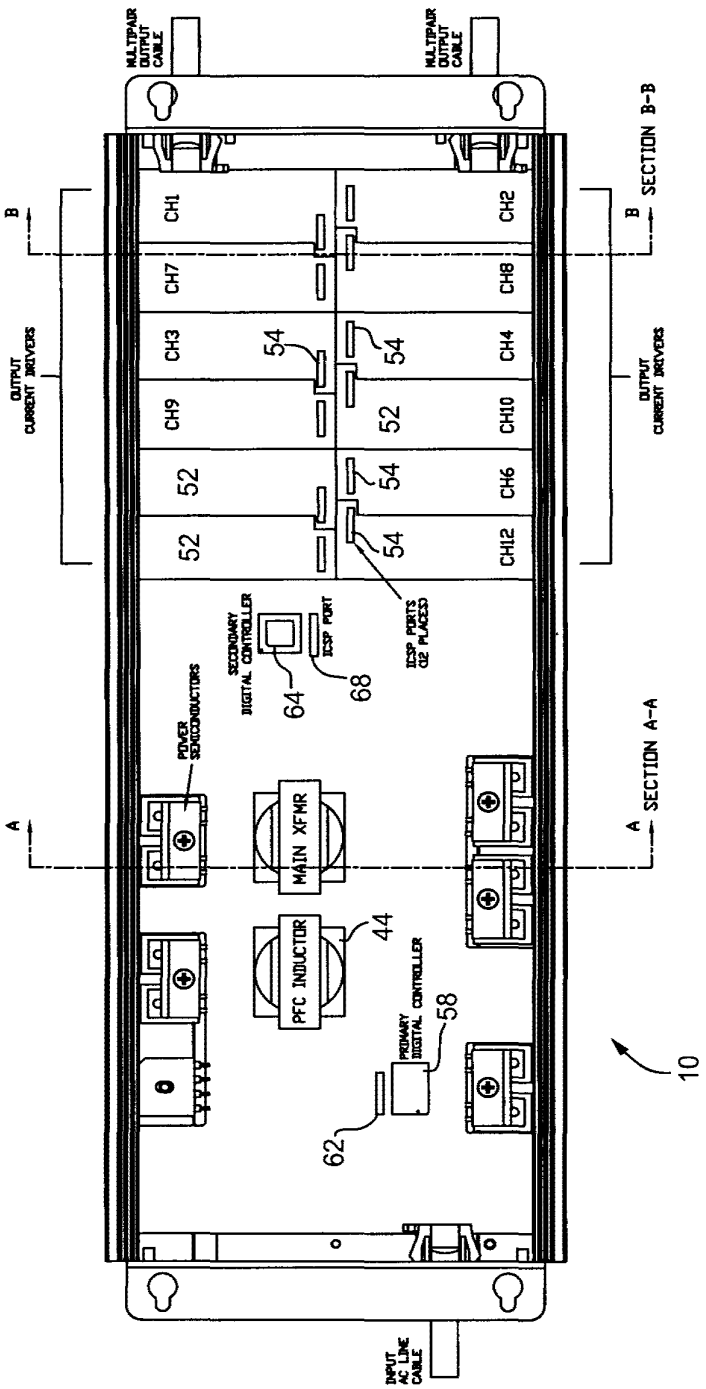

MULTIPAIR OUTPUT CABLE
MULTIPAIR OUTPUT CABLE
SECTION B-B
B
B
CH1
CH2
CH7
CH8
CH3
CH4
CH9
CH10
CH6
CH12
54
52
OUTPUT CURRENT DRIVERS
OUTPUT CURRENT DRIVERS
SECONDARY DIGITAL CONTROLLER
ICSP PORT
ICSP PORTS OE PLACED
64
68
POWER SEMICONDUCTORS
MAIN XFMR
SECTION A-A
A
A
PFC INDUCTOR
44
PRIMARY DIGITAL CONTROLLER
58
62
10
INPUT AC LINE CABLE

FIGURE 2c

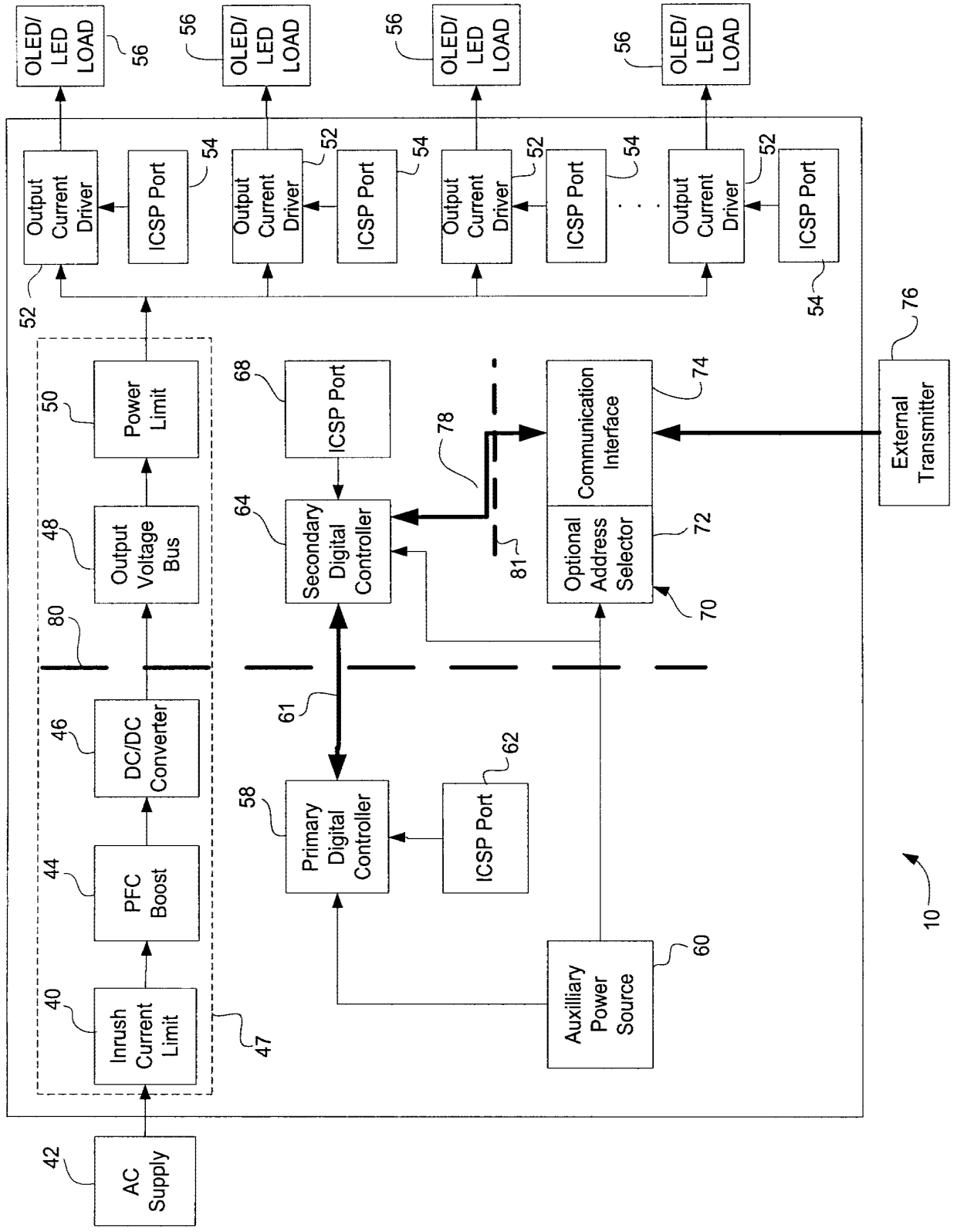

OLED/ LED LOAD
56
Output Current Driver
52
ICSP Port
54
Power Limit
50
Output Voltage Bus
48
DC/DC Converter
46
PFC Boost
44
Inrush Current Limit
40
47
80
AC Supply
42
ICSP Port
68
Secondary Digital Controller
64
78
81
Communication Interface
74
Optional Address Selector
72
70
External Transmitter
76
61
Primary Digital Controller
58
ICSP Port
62
Auxilliary Power Source
60
10

FIGURE 3

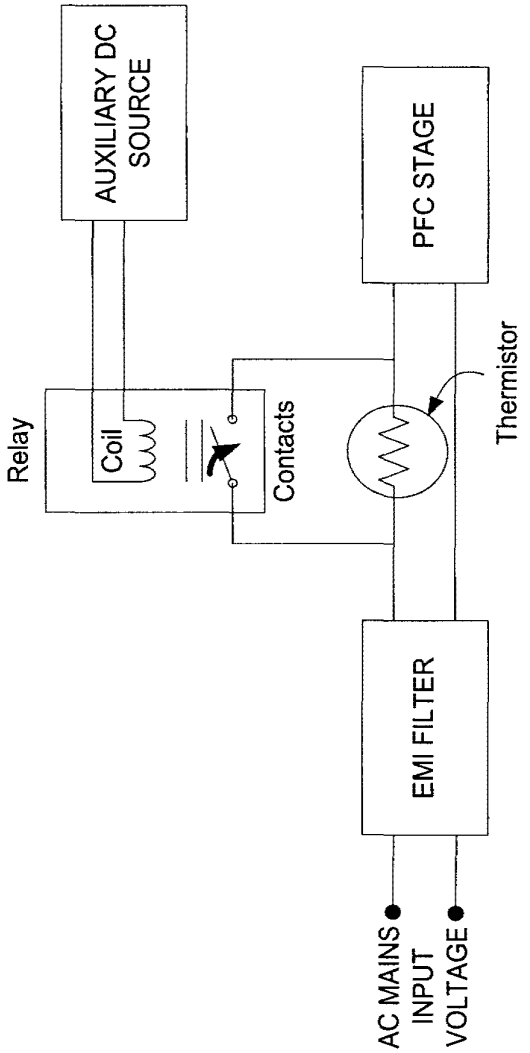


FIGURE 4 (PRIOR ART)

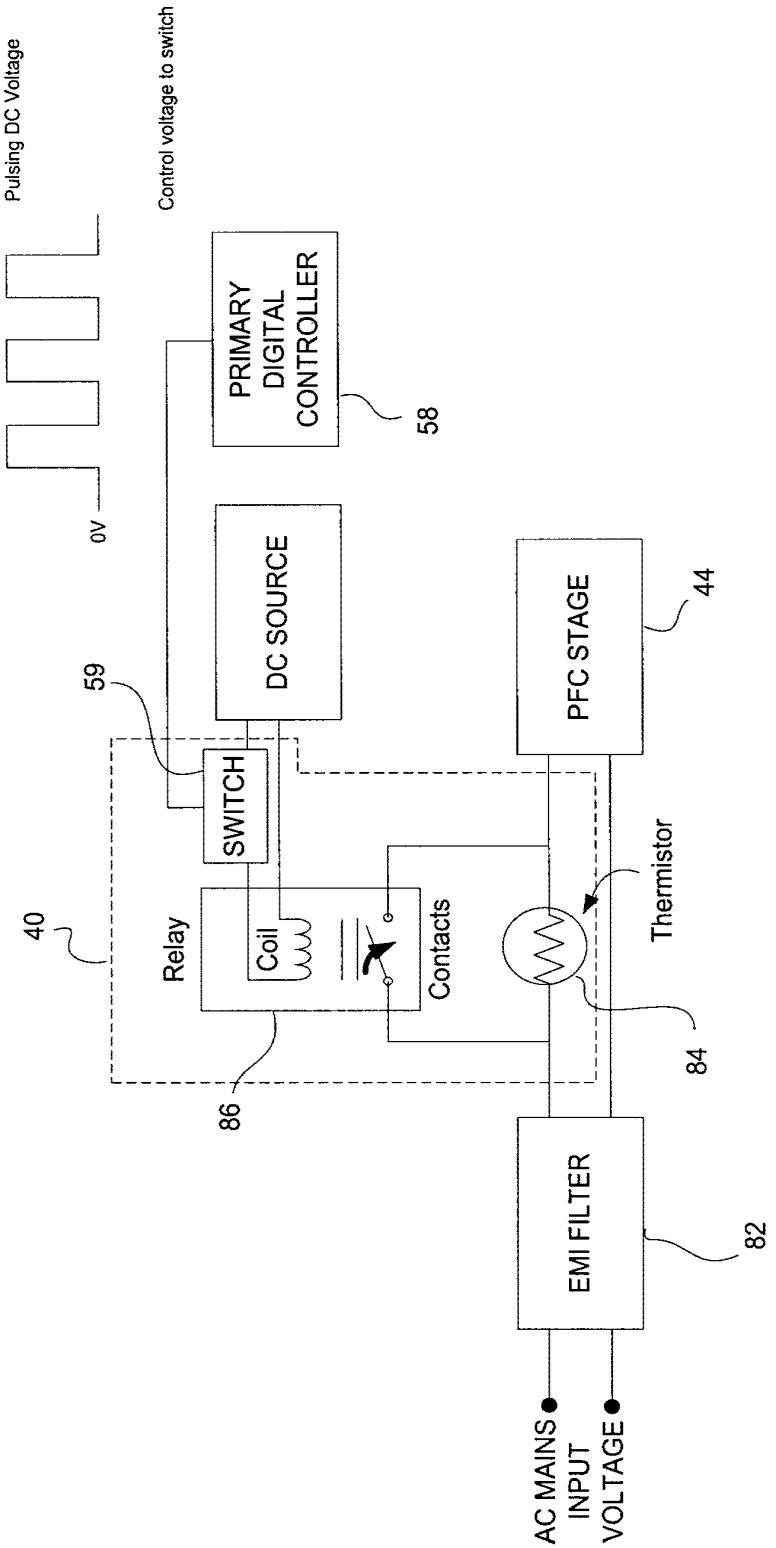

Pulsing DC Voltage
0V
Control voltage to switch
PRIMARY DIGITAL CONTROLLER
58
DC SOURCE
59
SWITCH
40
Relay
Coil
Contacts
86
PFC STAGE
44
Thermistor
84
EMI FILTER
82
AC MAINS INPUT VOLTAGE

FIGURE 5

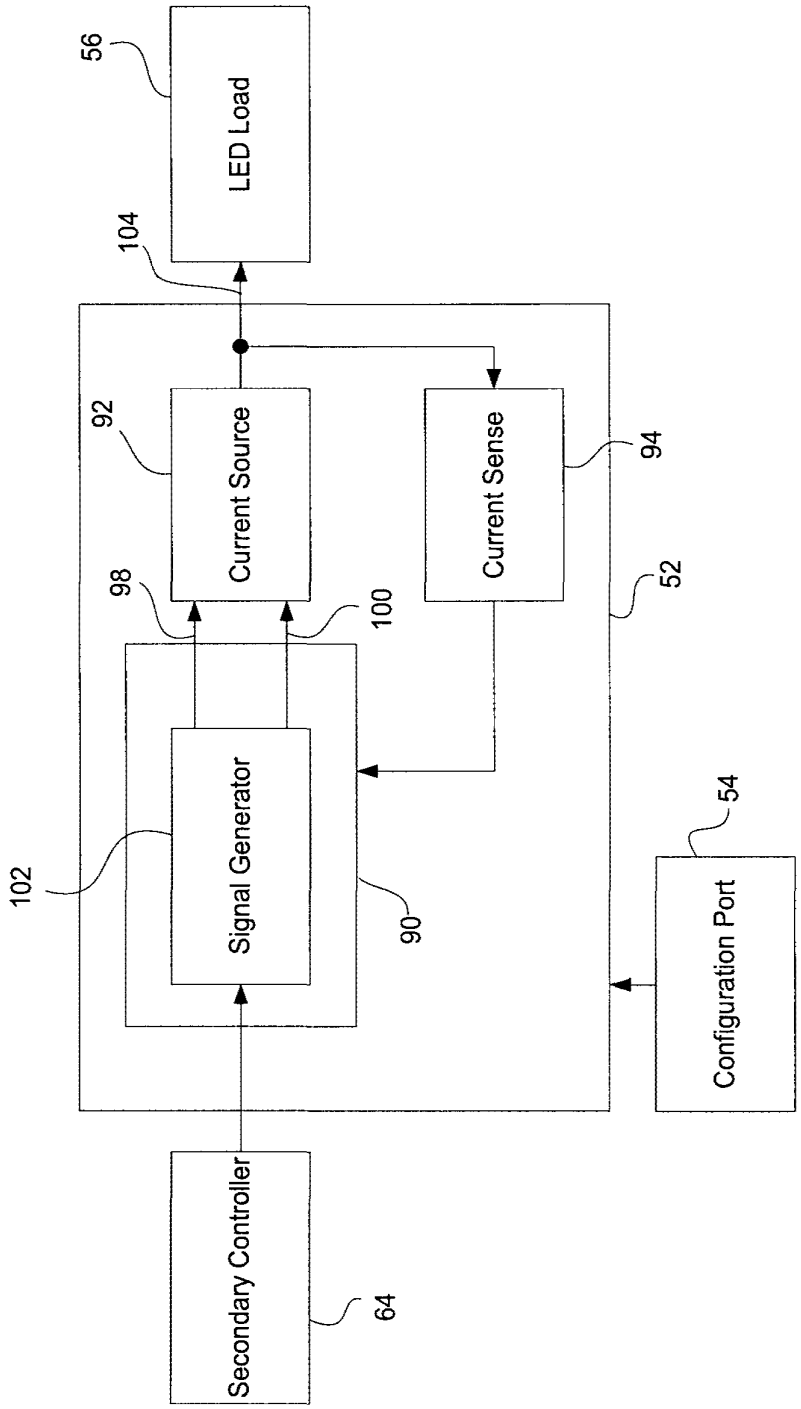

56
LED Load
104
92
Current Source
Current Sense
94
98
100
52
Signal Generator
102
90
54
Configuration Port
Secondary Controller
64

FIGURE 6

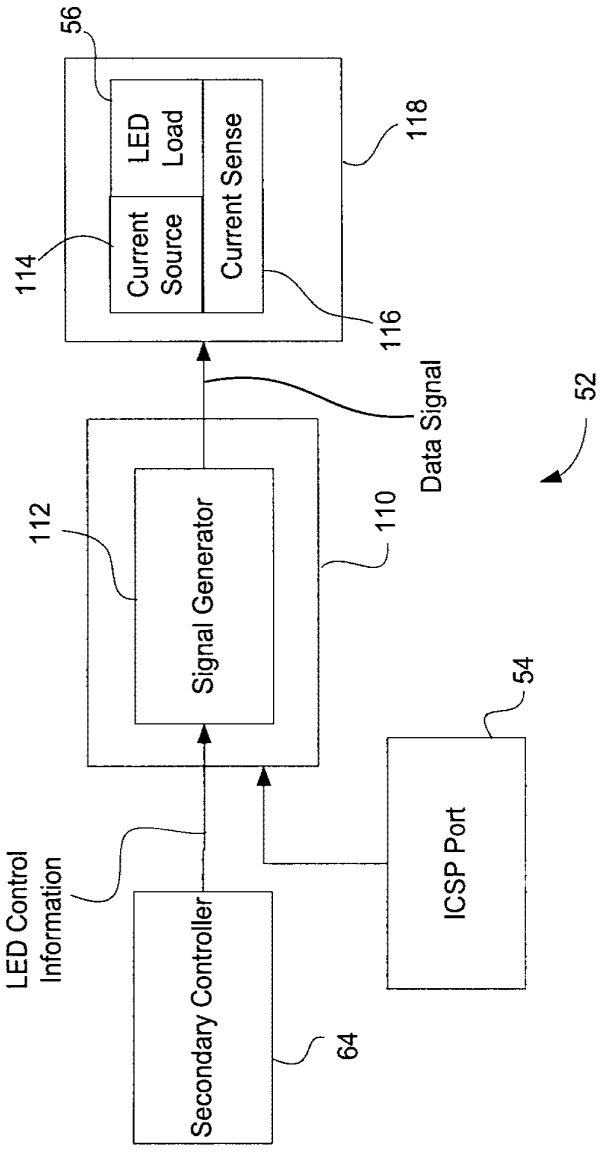

56
LED Load
Current Source
Current Sense
118
114
116
Data Signal
52
112
Signal Generator
110
54
ICSP Port
LED Control Information
Secondary Controller
64

FIGURE 7

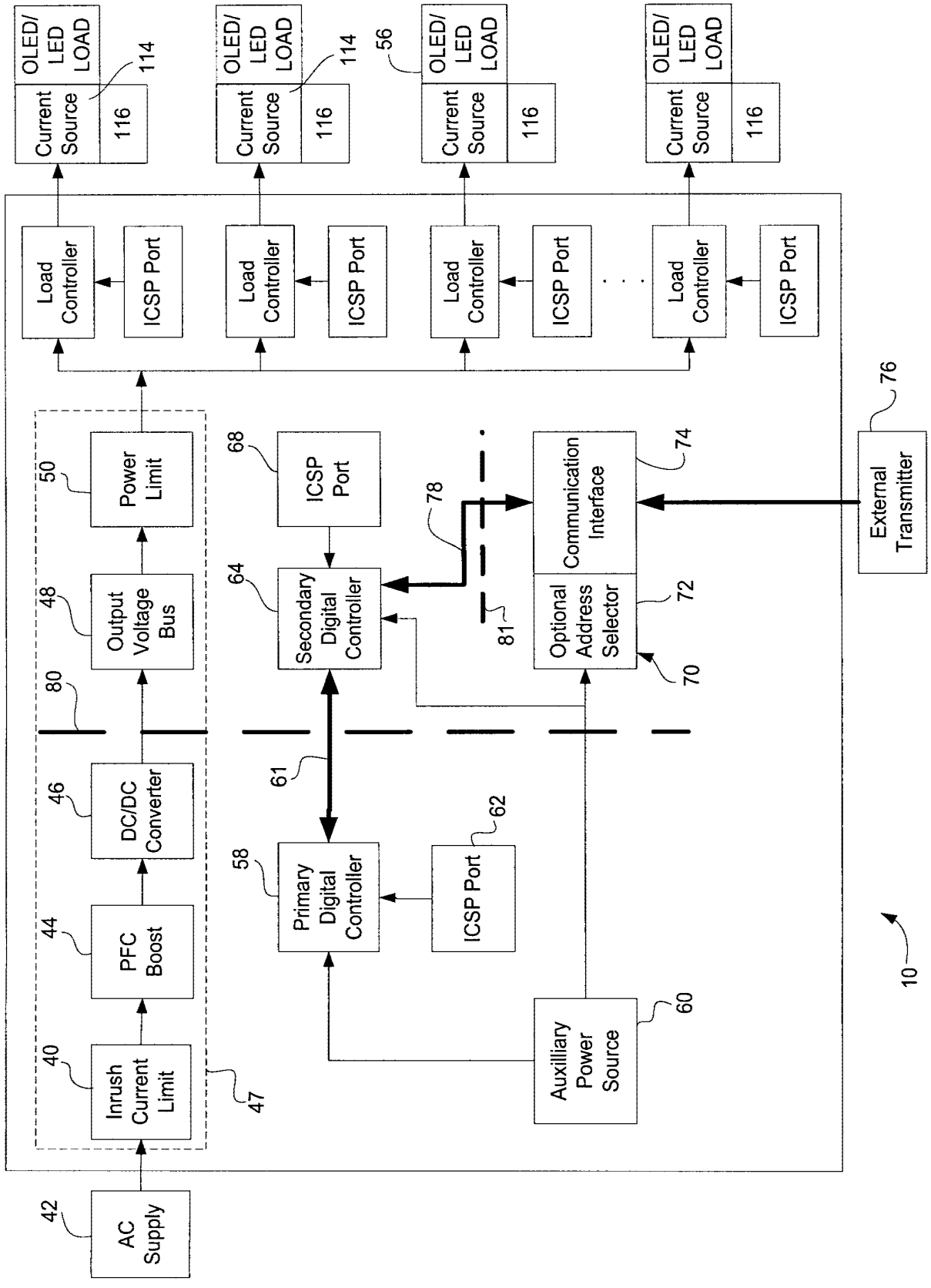

OLED/ LED LOAD
Current Source
116
114
56
Load Controller
ICSP Port
Power Limit
50
Output Voltage Bus
48
DC/DC Converter
46
PFC Boost
44
Inrush Current Limit
40
47
80
AC Supply
42
ICSP Port
68
Secondary Digital Controller
64
Primary Digital Controller
58
ICSP Port
62
61
78
81
Communication Interface
74
Optional Address Selector
72
70
External Transmitter
76
Auxilliary Power Source
60
10

FIGURE 8

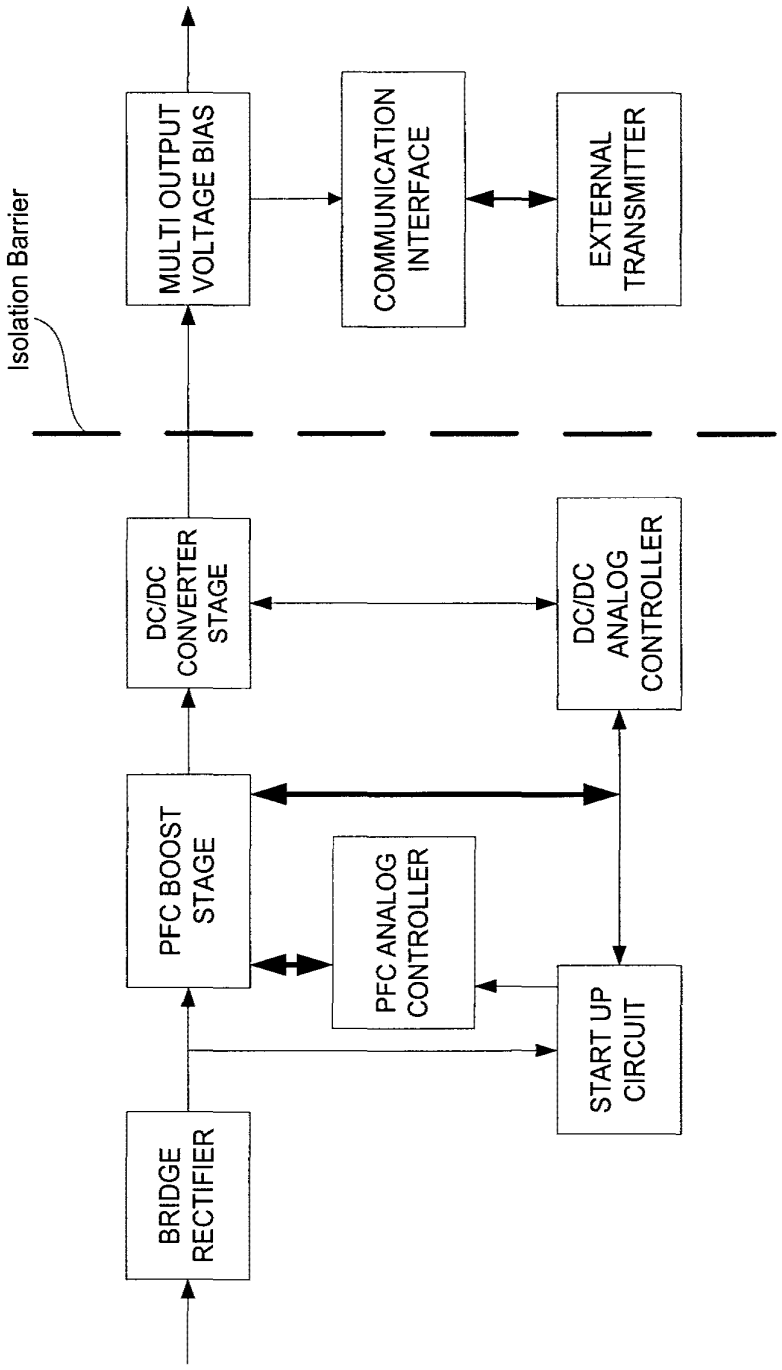


FIGURE 9 (PRIOR ART)

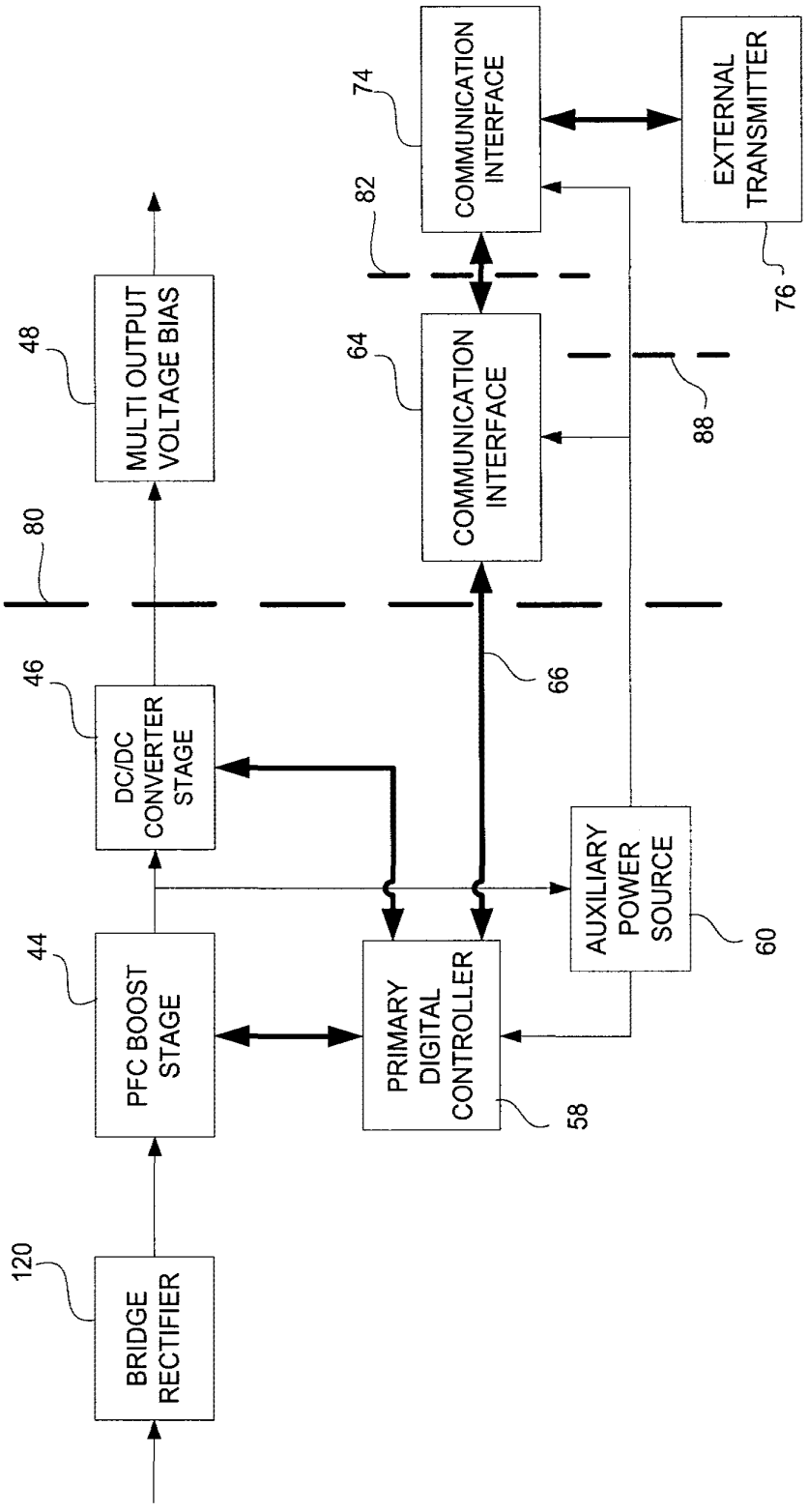

BRIDGE RECTIFIER
120
PFC BOOST STAGE
44
DC/DC CONVERTER STAGE
46
MULTI OUTPUT VOLTAGE BIAS
48
80
PRIMARY DIGITAL CONTROLLER
58
AUXILIARY POWER SOURCE
60
66
COMMUNICATION INTERFACE
64
88
82
COMMUNICATION INTERFACE
74
EXTERNAL TRANSMITTER
76

FIGURE 10

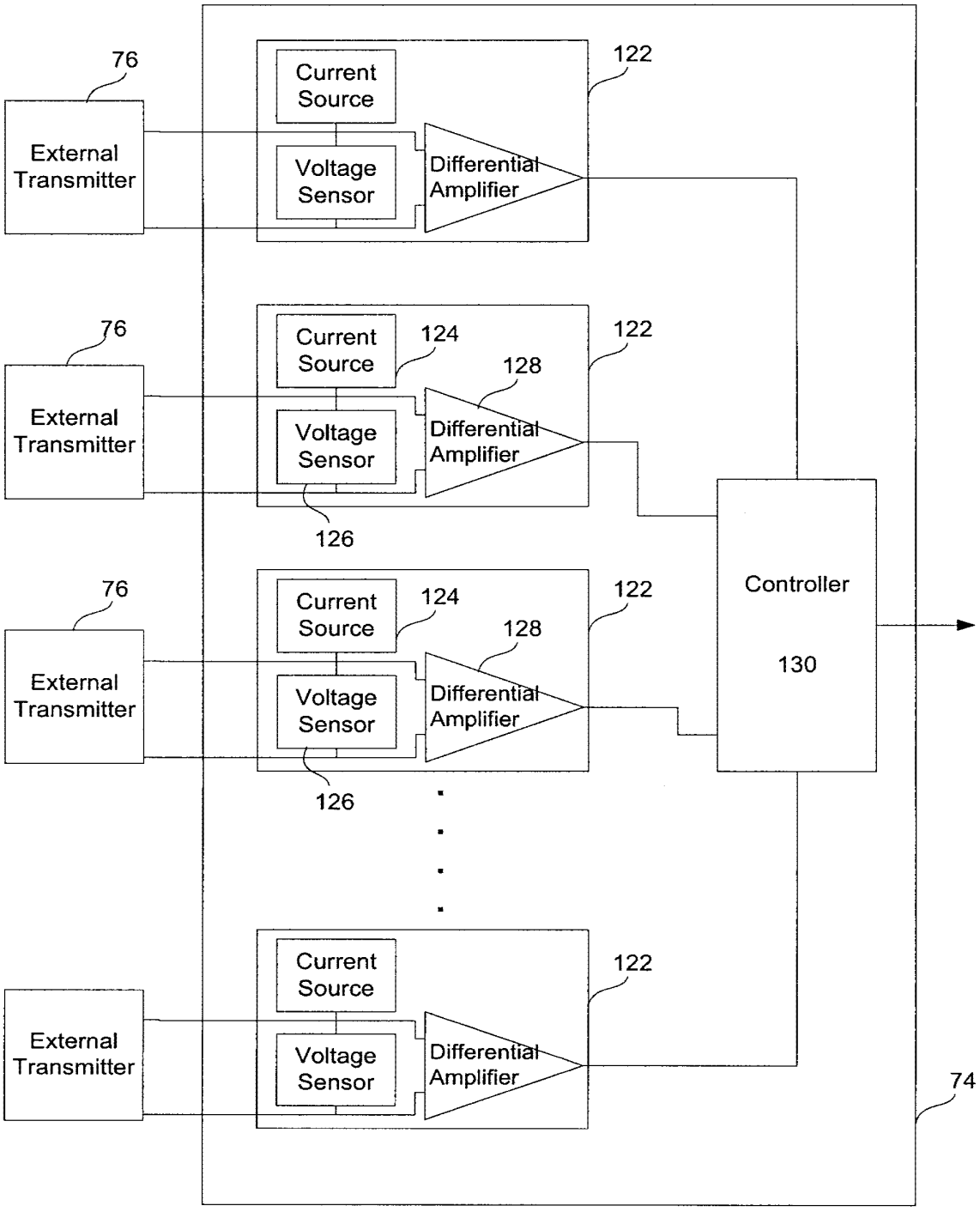

76
External Transmitter
Current Source
Voltage Sensor
Differential Amplifier
122
124
128
126
Controller
130
74

FIGURE 11

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EFS ID:	3964841
Application Number:	61097963
International Application Number:	
Confirmation Number:	1241
Title of Invention:	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	26123
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 67545P-2
Receipt Date:	18-SEP-2008
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RAM confirmation Number	10225
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1	Transmittal of New Application	PAT-67545P-2-Cover.pdf	763155 8db1746d4310f9431e342ef981e2589505af4231	no	4
Warnings:					
Information:					
2	Application Data Sheet	PAT-67545P-2-ADS.pdf	1675861 1478cad3b9e87cf32d513e6b188ec79eb6f20168	no	6
Warnings:					
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3		PAT-67545P-2-Spec.pdf	108012 14c9924f9b4e9b3ad4ab0e54309b3d181c51f3e5	yes	17

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	16
Claims	17	17

Warnings:					
Information:					
4	Drawings-only black and white line drawings	67545_d2.PDF	526763 560503837c63c41cb35a44d895ca0345d83cc2d9	no	13
Warnings:					
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5	Fee Worksheet (PTO-06)	fee-info.pdf	29658 e9097238466ac898719c04b3acc343dce141e864	no	2
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Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

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Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

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Title of Invention	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
Attorney Docket Number (if applicable)	PAT 67545P-2

Correspondence Address

Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

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Entity Status

Applicant claims small entity status under 37 CFR 1.27

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Signature	/Jeffrey W. Wong/			Date (YYYY-MM-DD)	2008-09-18
First Name	Jeffrey W.	Last Name	Wong	Registration Number (If appropriate)	46414

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A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

BACKGROUND OF INVENTION

LED TECHNOLOGY

[0001] With the rapid increase in Light Emitting Diode (LED) efficacies for high powered LEDs compared to common light sources, the latest LED technologies have exceeded incandescent and halogen sources and are now starting to compete with fluorescent, mercury vapour, metal halide and sodium lighting.

[0002] In addition to better energy usage, LEDs also have considerable advantages over traditional light sources such as long life, better durability, and improved color generating abilities.

[0003] The advancement of LED technology by various manufacturers such as Lumileds, Osram Sylvania, and Nichia has produced high power LEDs with various recommended drive currents such as 350 mA, 500mA, 700mA, 1000mA, and 1400mA or higher.

COMMUNICATION OPTIONS

[0004] The ability to dim the light output of LEDs is also important to reduce energy consumption and a number of different interfaces are available such as DMX512A, 0-10Vdc analog control, Zigbee wireless, and Remote Device Management (RDM). A brief description of each interface is as follows;

[0005] DMX512A (Digital Multiplex or DMX) is an EIA-485 based unidirectional communications protocol that is used for entertainment lighting control. A DMX controller is connected to lighting systems incorporating the appropriate DMX receiver interface in a daisy chain link. DMX512A data is sent serially at 250 Kbit/s using RS-485 voltage levels and cabling practices and is grouped into packets of up to 513 bytes, with the first byte being the start code byte. The remaining 512 bytes are 8 bit values, between 0 and 255 corresponding to a light intensity level. One DMX universe comprises 512 addresses with each address associated with a function within a device or load that can be independently controlled by the corresponding 8 bit value within the DMX packet.

[0006] RDM is an extension of the DMX512A protocol that incorporates bidirectional communication between the lighting controller and lighting fixtures. RDM allows for diagnostic feedback and remote addressing capabilities for a lighting system.

[0007] 0-10 Vdc analog control can be implemented by various means such as the ESTA E1.3-2001 "Lighting Control Systems 0-10 Vdc Analog Control Specification" for Entertainment Technology or IEC60929 "AC supplied electronic ballasts for tubular fluorescent lamps".

[0008] E1.3 based lighting controllers (transmitter) provide a current source output to a dimmer (receiver). The output is intended to vary between 0 and 10 volts and be linear. Minimum light output is represented by about 0 volts and full light output is represented by about 10 volts. IEC60929 based dimming methods have a current source within the lighting ballast to provide a 0 to 10 Vdc voltage to the control interface.

[0009] Zigbee is a wireless mesh networking communication protocol based on the IEEE 802.15.4 standard. It is targeted at wireless control applications that require low data rates, low power consumption and secure networking. Its applications include home automation and commercial building automation.

INTENSITY CONTROL FOR LEDS

[0010] It should be understood that the terms intensity control, dimming, and color mixing control are terms that can be used interchangeably. Color mixing controls the intensity of more than one LED color.

[0011] The light intensity of an LED as seen by the human eye can be varied by various modulation techniques that change the average current through an LED.

[0012] Pulse Width Modulation (PWM) is the most common technique used to vary the intensity of light. It uses a fixed frequency with a variable duty cycle or on time. The duty cycle determines the intensity of the LEDs.

[0013] Pulse Amplitude Modulation (PAM) is another known technique. In PAM, the system creates a PAM signal, which encodes the required LED current in the amplitude of a series of pulses of constant duration and frequency.

[0014] Bit Angle Modulation (BAM) utilizes a binary pulse train that contains the light intensity value. Each bit of the pulse train is stretched proportionally to the binary significance

of each bit of the binary word and therefore allocated a fixed range of phase angles within the drive cycle.

[0015] Pulse Frequency Modulation (PFM) is a method using a constant pulse width. Intensity control is achieved by varying the repetition rate of the pulses and therefore the frequency of the signal.

DIGITAL CONTROL IN POWER SUPPLIES

[0016] In switch mode power supply applications, analog control techniques have been the main approach for feedback control. The use of microcontrollers in power supplies has typically been limited to monitoring functions such as temperature, over current, and over voltage and under voltage protection as well as other housekeeping functions.

ENERGY EFFICIENCY

[0017] Solid State Lighting (SSL) systems that incorporate LEDs or OLEDs have the potential to generate energy savings if the power sources used to power them are energy efficient as well.

[0018] The California Energy Commission (CEC), Environmental Protection Agency (EPA) and Department of Energy (DOE) have developed energy efficiency standards for consumer products including external power supplies and lighting fixtures. The Energy Star Program created by the EPA in 1992, has recently established industry wide requirements for Solid State Lighting (SSL) products. The principle energy efficiency metric used is the luminaire efficacy whereby luminaire efficacy is defined as net light output from the fixture divided by input power.

[0019] The Energy Star program and CEC have also established standards for external power supplies. For example, the principle energy efficiency metrics used include the average efficiency of the power supply over various load ranges such as 25%, 50%, 75% and 100% and the standby power consumption at no load of less than 0.5 Watts.

NEED FOR ENERGY EFFICIENT CONFIGURABLE LED DRIVER

[0020] Lighting companies are faced with considerable challenges in adopting SSL technology due to their unfamiliarity and lack of expertise in the driving and dimming requirements for LEDs. In order for lighting companies to develop energy efficient SSL

systems, they must either source or design, then integrate the various elements of AC to DC power conversion, interface control for dimming requirements, and constant current drivers with the various LEDs available. Thermal management and power efficiency is a key consideration for the SSL system.

[0021] The specific LED drive currents, the number of LEDs required (and therefore the total power requirement), as well as the color or colors of the LEDs, and the dimming method all depend on the end application.

[0022] This has created a need in the market place for efficient, configurable, controllable power sources in order to utilize the full benefits of LEDs.

BRIEF DESCRIPTION OF DRAWINGS

[0023] Embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

Figure 1: Preferred Embodiment -Block Diagram of Configurable LED Driver/Dimmer

Figure 2: Preferred Embodiment-Mechanical Configuration of LED Driver/Dimmer

Figure 3: Preferred Embodiment-Mechanical Cross Section of LED Driver Dimmer

Figure 4: Prior Art-Inrush Current Limit Circuit

Figure 5: Preferred Embodiment-Inrush Current Limit Circuit

Figure 6: Internal Layout of Configurable LED Driver/Dimmer

Figure 7: Preferred Embodiment-Output Current Driver

Figure 7A: Alternate Embodiment-Output Current Driver

Figure 8: Alternate Embodiment- Electrical Block Diagram of LED Driver/Dimmer

Figure 9: Prior Art-Typical Application of Internal Auxiliary Power Distribution in a Multistage Power Source

Figure 10: Preferred Embodiment-Internal Auxiliary Power Distribution in a Multistage Power Source

Figure 11: 0-10 Vdc Analog Control Communication Interface

SUMMARY OF INVENTION

[0024] In recent years, controllable power sources greater than 150 watts of output power for Solid State Lighting applications have entered the market with integrated features

such as power factor correction (PFC), an isolated power conversion stage, a communication interface such as DMX512A, and multiple current sources incorporated into a single module or enclosure.

[0025] With the wide variety of communication interface options and LED drive currents available for numerous architectural and entertainment Solid State Lighting applications, the current invention includes one or more of the following advantages:

-configurable output current options that maximize the available power in the "front end" PFC and isolated power conversion converter stage,

-multiple drive current options given that there are multiple LED drive current options for various LEDs.

-no need for a cooling fan which may present issues with audible noise and flexibility in where the power source may be located,

-relatively low standby power consumption at "black out" lighting conditions, where "black out" refers to no load operation on the output of the dimmer/driver.

-multiple communication interface options available

-the ability to map output current sources/channels to different DMX512A addresses

-the ability to configure multiple groups of output current sources/channels such that each group is controlled by one 0-10Vdc analog signal.

[0026] Recently, there has been significant growth in the implementation of digital feedback control as better digital controllers become available at lower cost. Digital control has considerable benefits over analog control solutions that include; flexibility to control parameters for nonlinear control loops to improve stability and responsiveness, better energy efficiency by optimizing switching characteristics, and EMI reduction.

[0027] In addition, digital controllers within power sources have enabled the development of configurable options to provide a wider flexibility of solutions for Solid State Lighting applications.

[0028] Some embodiments of the present invention are directed to a highly efficient enclosed, configurable power source, controllable by means of various external communication interfaces and a method for driving and dimming LEDs or OLEDs in lighting fixtures used for architectural or entertainment lighting applications. Such applications can

include theater, convention centers, cruise ships, architectural building features, amusement parks, museums, and hospitality lighting in restaurants and bars.

[0029] One aspect of the present invention is a configurable power source that provides a plurality of output channels (6, 8, 9, or 12) to color change or dim OLED or LED loads. In color changing applications, the number of available channels is a multiple of 3 or 4 to accommodate either red/green/blue LED loads or red/green/blue/amber or white LED loads. The number of output channels and available output power is maximized based on the LED current requirements. The output channels are programmable by means of in circuit serial programming (ICSP) ports and calibrated by means of their secondary digital controllers [see figure 7] to the required output current and other parameters such as frequency range.

[0030] In another embodiment the dimming of multiple monochromatic color or white LED loads (output channels) utilizing a single 0-10 Vdc analog control signal, or the control of groups of LED loads (output channels) with an associated 0-10 Vdc analog control signal for each group is contemplated.

[0031] In another aspect of the present invention, the output channels are digitally controlled current sources configurable for various peak currents to power and control a variety of LEDs. The LED average current is encoded within the three variables of on-time, off-time, and period whereby no three variables are held constant. Depending on the output drive currents of the LED loads, the number of available output channels is maximized based on the maximum output power available from the power factor and isolated DC/DC converter stages.

[0032] In another aspect of the present invention, the configurable power source is mechanically packaged in a rectangular enclosure with a monolithic aluminum extrusion and a U shaped aluminum chassis and metal end plates. Various electrical components are thermally coupled to the heatsink to maximize heat transfer to the outside surface of the enclosure. The output connection means to the LED loads comprises multipair cable or cables to decrease space requirements on the end plate.

[0033] In another aspect of the present invention, the power source utilizes a digital controller to decrease power consumption of a relay coil as part of an inrush current limit circuit to reduce power consumption and improve efficiency.

[0034] In another aspect of the present invention, the power source utilizes an independent efficient auxiliary power source and one or more digital controllers to provide

power to the communication interface. A digital controller disables various electrical circuits during black out lighting conditions to reduce no load power consumption and improve efficiency.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

[0035] **Figure 1** is a high level block diagram depicting a configurable LED Driver/Dimmer. The system generally comprises a PFC Boost and DC/DC Converter power conversion stage with an electrical isolation barrier, output current drivers, an independent auxiliary power source, and communication interface. The PFC Boost and DC/DC Converter stages are controlled by a primary side digital controller and the secondary digital controller translates dimming and/or color mixing information from the external transmitter into LED control information for the output current drivers. The primary and secondary digital controllers and output current drivers have an associated programming port for configuring the LED Driver/Dimmer.

[0036] A perspective view of an embodiment of a configurable led driver/dimmer for solid state lighting applications is shown in **Figure 2: Mechanical Configuration of LED Driver/Dimmer**. The device is contained within a rectangular shaped housing. The power output connection apparatus, or means, from the output current drivers comprises multi-pair conductors within one or more cables that exit the end plate of the configurable power source. This approach reduces the space, surface area requirements for the end plate compared to other connection means such as terminal blocks or connectors.

[0037] The housing as shown in **Figure 3: Mechanical Cross Section of LED Driver Dimmer** comprises a monolithic aluminum extrusion heatsink and a U shaped aluminum chassis. To optimize the heat dissipation capability of the configurable power source at full output power, the extruded aluminum heatsink incorporates fins to maximize the surface area. The heatsink also has a mounting platform for the power semiconductors such as the bridge rectifier, MOSFETs, and diodes to efficiently transfer heat to the outside surface of the heatsink. The power factor inductor and main isolation transformer are thermally coupled to the U frame chassis by means of a thermally conductive, electrically isolated material to further improve heat dissipation of these components.

INRUSH CURRENT LIMIT

[0038] To limit inrush current limit during initial start up of the power source, a typical approach is to utilize a negative temperature coefficient thermistor (NTC) in parallel with a relay contact as shown in **Figure 4**, which is a Prior Art -Inrush Current Limit Circuit. During initial turn on of the power source, the NTC thermistor limits the inrush current. When the PFC boost stage bulk capacitor is charged, and before the PFC stage is enabled by the primary controller, the primary controller closes the relay contact to bypass the NTC thermistor. This is accomplished by applying a DC voltage via a switch across the coil in the relay. This approach is typically used to eliminate power dissipation in the NTC thermistor during normal load operation.

[0039] A limitation of this approach is the power consumption of the relay coil when a continuous DC voltage is applied. This power consumption becomes significant in terms of Energy Star requirements during no load or standby operation such as when a "black out" or minimum light intensity state is received by the communication interface.

[0040] An improvement to this approach is to have the primary controller pulse the DC voltage across the relay coil via a switch to reduce power consumption, such as shown in **Figure 5: Preferred Embodiment-Inrush Current Limit Circuit,** A typical relay coil requires greater energy to close the contacts than is required to maintain the contacts in a closed position since less holding force is required. After the relay contacts have been closed by applying a voltage of 12VDC, modulation of the relay coil voltage can be initiated by the primary controller to effectively reduce the average voltage across the coil to approximately 5 volts versus a DC voltage of 12V, reducing power consumption. It should be noted that the pulse duty cycle and frequency can be changed to optimize performance.

PFC BOOST STAGE

[0041] Referencing **Figure 1** in the preferred embodiment, the PFC Boost Stage utilizes a boost topology with an input AC voltage mains range of 103 Vac to 300 Vac.. Energy stored in the PFC boost inductor is transferred and stored in the bulk capacitor on a cycle by cycle switching basis at a loosely regulated 430V DC over the input range. The energy is controlled in a manner that forces AC input current to be sinusoidal and in phase with the AC line voltage. By drawing current in phase with the input mains voltage, it reduces the amount

of harmonic currents of the fundamental AC mains frequency from being introduced into the power line.

DC/DC CONVERTER AND OUTPUT VOLTAGE BUS

[0042] The preferred implementation for the DC/DC converter stage is derived from the isolated buck converter topology and comprises a galvanically isolated full bridge converter employing a primary side phase modulation technique with a secondary side current doubler rectifier circuit.

[0043] The full bridge converter parasitic circuit elements in conjunction with primary magnetization current and reflected inductor ripple current cause resonant edge switching transitions on the MOSFET switch thus forcing zero voltage across the MOSFET switching device before turn on. The result is higher efficiency due to the elimination of Coss (drain to source MOSFET Capacitance) switching losses, reduction of gate charge across the Miller capacitiance and minimized power loss during switching transitions when voltage and current are changing simultaneously.

[0044] The output of the DC/DC converter is a tightly regulated DC bus. To limit the power output of each of the output current drivers, a set of power limit circuits coupled to either one or more current drivers are used to power a plurality of LEDs or OLEDs. The power limit circuits each include a current sensor that is monitored by the secondary side controller. In the event of a single component failure within the output current driver module, the power limit circuits limit the energy to the loads in accordance with the UL standard 1310 Class 2.

[0045] Supplementary protection to the power limit circuits can also include one or more fuses.

PRIMARY DIGITAL CONTROLLER

[0046] The primary digital controller provides digital feedback control for the PFC Boost and DC/DC Converter stages.

[0047] The digital feedback method for the PFC Boost Stage utilizes average current mode control with duty cycle feed forward for the inner current loop and voltage mode control for the outer control loop. The DC/DC Converter stage utilizes voltage mode control for the digital control loop.

[0048] The primary digital controller also controls the inrush current limit circuit, provides primary current limit protection, and over voltage protection for the PFC Boost Stage output. The primary digital controller also disables the PFC Boost stage and DC/DC Converter stage during black out or no load conditions to reduce power dissipation.

OUTPUT CURRENT DRIVERS

[0049] Referring to **Figure 6:** In the preferred embodiment, the output current drivers are a monolithic part of the apparatus. Configuring the required number of outputs and required output current is accomplished by populating the appropriate sections of a single printed circuit board with the appropriate electrical components and programming the output current driver via the in-circuit serial programming (ICSP) port.

[0050] Referencing **Figure 7**, which is a preferred embodiment of an output current driver, the output current drivers **40**, comprise a load controller **30**, a current source **20**, and current sense **28**. Although only one current driver **40** is shown, it will be understood that multiple are present.

[0051] The output current drivers utilize the dimming/color mixing techniques for LEDs described in detail in provisional patents 60/796,550 and 60/735,220 wherein the LED average current is encoded within the three variables of on time, off time, and period where by no three variables are held constant.

[0052] The secondary controller **12** receives dimming and/or color mixing information in the form of a serial data stream from the external transmitter via the communication interface and secondary controller and translates this into LED control information. The LED control information is transmitted to the load controller **30** in the form of instructions to generate the digital signal **22** and the analog signal **24**.

[0053] The load controller **30**, further comprises a signal generator **18**, which transmits a digital signal **22** and an analog signal **24** to the current source **20**. The digital control signal **22** and the analog signal **24** are preferably generated via a digital control algorithm and 1 Bit algorithm, respectively.

[0054] The current source **20** preferably includes ancillary circuitry for operation and comprises a buck topology power stage with hysteretic control. The current sense **28** provides a digital feedback loop for each current source **20**. The current source **20** is a buck

circuit topology however other embodiments may include topologies such as boost, buck-boost, or SEPIC.

[0055] The output **42** of the current driver **40n** provides a current pulse via current source **20** to the LED Load **26n** whereby on times, off times, and period are not held constant.

[0056] Each output current driver **40**, has an associated in-circuit serial programming (ICSP) port **60**. The ICSP port **60** provides access to the load controller **30** such that firmware updates are possible to permit the configuration of the output current drivers **40n**. The ICSP port(s) **60** for the output current driver(s) **60** can be located on the printed circuit board assembly of the apparatus or they can be located on the outside of the enclosure.

[0057] The configuration options include but are not limited to such parameters as the adjustment of the frequency range of the dimming current pulse for the range of light intensity output or the set point adjustment of the peak on time output current.

[0058] For example, it might be necessary to increase the frequency range of the dimming current pulse in video recording applications where the dimming current pulse frequency may be programmed for a 2000Hz to 2500Hz range. This would negate a visible beat frequency effect that would other wise be noticeable on recorded video. There can be other applications where the adjustment of the dimming current frequency range is required to reduce Electromagnetic Interference (EMI) effects.

[0059] The default peak output current set point is programmed via the ICSP port **60** which provides flexibility in the number of possible LEDs types that can be driven and is typically dependent on the recommended operating current specified by the manufacturer such as 350mA, 700mA, etc. The set point current is preferably programmed to within 4% of the manufacturer's specification. The peak output current set point can then be precisely calibrated to within typically 1% by the secondary controller **12** during factory calibration.

[0060] An alternate embodiment has the current sources **20** and current sense **28** remotely mounted from the PFC and DC/DC Converter stages as shown in **Figure 7A: Alternate Embodiment of Output Current Driver** and **Figure 8: Alternate Embodiment-Configurable LED Driver/Dimmer**. The current source and current sense may be mounted in the light fixture containing the LED load, and power and data signals are provided to each output current source by means of a multi conductor cable. In this embodiment, the current sources are configured to regulate to a predetermined peak current for example 700mA. The load controller transmits the data signal containing the output current information encoded

within the three variables of on time, off time, and period whereby no three variables are held constant.

[0061] Alternate embodiments of the present invention for light intensity control include pulse width modulation (PWM), pulse amplitude modulation (PAM), Bit Angle Modulation (BAM), and pulse frequency modulation (PFM).

AUXILIARY POWER SUPPLY

[0062] Referencing **Figure 9**, which shows a typical application of internal auxiliary power requirements in a multistage power source, a typical approach is shown of how auxiliary power is provided to the various blocks of a multistage power source. **P1, P2...P10** represents the various power and voltage transfer requirements for each functional block. For simplicity, the various voltage regulator and filter circuits required for each of the power outputs have been omitted. A brief description for initial startup and continuous operation of the auxiliary power source is as follows;

[0063] The bridge rectifier converts the AC mains voltage **P1** to a rectified voltage **P2**. A portion of power **P6** from the output of the bridge rectifier **P2** is supplied to the start up circuit. The start up circuit is comprised of a power transistor or MOSFET and is intended to provide power **P8** to the PFC analog controller for only a short duration of a few seconds. Power **P8** to the PFC analog controller will allow the PFC Boost stage to begin switching, providing power **P10** to the DC/DC controller, and power **P3** to the DC/DC converter power stage. Since the start up circuit dissipates an excessive amount of power, it is turned off by the voltage component of **P7** supplied by the PFC boost stage. The **P7** power is permitted to 'flow through' the start up circuit to continue to supply power **P8** to the PFC analog controller.

[0064] The output of the DC/DC Analog Converter provides power **P4** to the multi output voltage bus, power **P9** to the Communication Interface, and the Output Current Drivers by means of **P5**.

[0065] In this implementation, the PFC and DC/DC Controllers are typically analog controllers. It should be noted that in this implementation, in order for the communication interface to continually receive dimming information from an external transmitter, the DC/DC Converter stage must remain turned on. Similarly, in order for the DC/DC converter stage to provide power **P4**, the PFC Boost stage must remain on.

[0066] In a 'black out' state, the communication interface may receive a "0" intensity value out of 255 intensity levels for all of its output current drivers via the external transmitter such as a DMX512A or RDM controller interface, or it may receive an analog voltage of between 0 to 1V via a controller compliant to ESTA E1.3-2001 or IEC60929 as one of many communication interface options. In this 'black out' state, the DC/DC Converter and PFC Boost Stage continue to dissipate an excessive amount of power.

[0067] **Figure 10: Preferred Embodiment-Internal Auxiliary Power Distribution in a Multistage Power Source** shows a preferred embodiment for providing auxiliary power to the various blocks of a multistage power source. **K1,K2...K10** represent the various power (voltage and current) transfer requirements for each functional block. For simplicity, the various voltage regulator and filter circuits required for each of the power outputs have been omitted. The transfer of power from AC mains to the Output Current Drivers (K1,K2,K3,K4,K5) is unchanged. This embodiment shows a novel implementation of an independent auxiliary power source providing power to the Primary Digital Controller **K7**, Secondary Digital Controller **K8,** and Communication Interface **K9**. Note that there is an isolation barrier between K8 and K9. The auxiliary power source is comprised of an efficient isolated flyback topology with a wide input voltage range and pulse skipping capability to minimize its power dissipation at light loads or no load conditions.

[0068] A 'black out' state received from the external transmitter to the communication interface is communicated to the secondary digital controller and then the primary digital controller via the isolated communication bus. The primary digital controller then disables the PFC Boost Stage and DC/DC Converter Stage reducing overall power dissipation of the configurable power source.

[0069] It should be noted that even when the PFC Boost Stage is disabled, power **K6** can continue to be supplied to the auxiliary power source since the rectified voltage **K2** from the bridge rectifier can continue to peak charge the PFC boost capacitor via the boost diode.

[0070] The auxiliary power source continues to provide power to the primary digital controller, secondary digital controller, and communication interface in order to be able to 'listen' for a change in light intensity state that may be communicated by the external transmitter.

[0071] Alternate embodiments may include additional ancillary circuits that may be powered by the independent auxiliary power source that can be disabled by a controller to reduce over all power dissipation in black out or no load conditions.

COMMUNICATION INTERFACE

[0072] The communication interface comprises a removable and interchangeable module with each module adapted for different control options such as DMX512A, RDM, 0-10Vdc and Zigbee.

[0073] The communication interface module receives lighting control information via an external transmitter and converts the various protocols into a serial data stream. It then transmits this data by means of a Universal Asynchronous Receiver Transmitter (UART) to the secondary digital controller via an isolated serial communication bus. The electrically isolated barrier between the secondary digital controller and the communication interface prevents ground loops.

[0074] One embodiment of the present invention utilizes a DMX512A module as the communication interface.

[0075] Referencing **Figure#11**, another embodiment of the present invention utilizes an analog interface module adapted for the 0-10 Vdc IEC60929 dimming method as the communication interface. The analog interface module can be adapted to receive one or more analog control voltages from one or more associated external transmitters. The external transmitter is preferably an electronic resistor or potentiometer that sinks current from the current source located on the analog interface module and outputs a variable 0-10Vdc control voltage proportional to the required light intensity.

[0076] The analog control module comprises one or more current sources and voltage sensors and controller. The differential amplifier senses a voltage across the voltage sensor and converts this into a correlated voltage (Vm,V1,V2...Vn) supplied to the controller. The controller converts this analog voltage into a serial data stream for transmission to the secondary digital controller via the isolated serial communication bus.

[0077] The analog control module may be configured to have one 0-10Vdc control voltage simultaneously control via the secondary digital controller, all output current drivers and multiple LED loads. This application is beneficial in monochromatic color or white lighting

applications since only one control signal and associated wiring is required to control multiple light loads.

[0078] As also shown in Figure 11, an alternate configuration can have the communication module adapted to have one or more 0-10Vdc signal voltages control an associated group of one or more output current drivers in zone dimming applications. An optional master 0-10Vdc signal voltage would be able to simultaneously control all of the individual groups of output current drivers.

[0079] In applications not requiring the complexity of DMX512A, these analog control options are beneficial in simple red/green/blue or red/green/blue/amber color changing or monochromatic color or white light applications whereby the addressability and corresponding control of individual LED light loads is not required.

SECONDARY DIGITAL CONTROLLER AND ISOLATED COMMUNICATION BUS

[0080] Referencing **Figure 1: Configurable LED Driver/Dimmer Block Diagram**, the secondary digital controller monitors and transmits output voltage bus information (feedback loop) via the two way isolated serial communication bus, decodes the serial data from the communication interface, and transmits control information to the output current drivers. As a protection feature, the secondary controller also monitors input currents in the power limit stages supplied to the output current drivers.

[0081] The secondary digital controller includes a ICSP port to program and calibrate the output voltage bus to the required voltage. In DMX512A applications, the ICSP port also permits the mapping of each of the output channels to a wide variety of addresses. Similarly, in 0-10Vdc analog control applications, the secondary digital controller ICSP port permits the mapping of output channels into groups for each associated 0-10Vdc control signal.

[0082] This mapping capability is particularly useful in addressable-networked lighting systems using a DMX512A control protocol where different lighting zones are required to respond to different illumination information. For example, in a 12 channel output configuration, the first 6 channels could be mapped to the DMX base address of the power source (ie DMX01) and the last 6 channels could be mapped to DMX address +1 (ie DMX02).

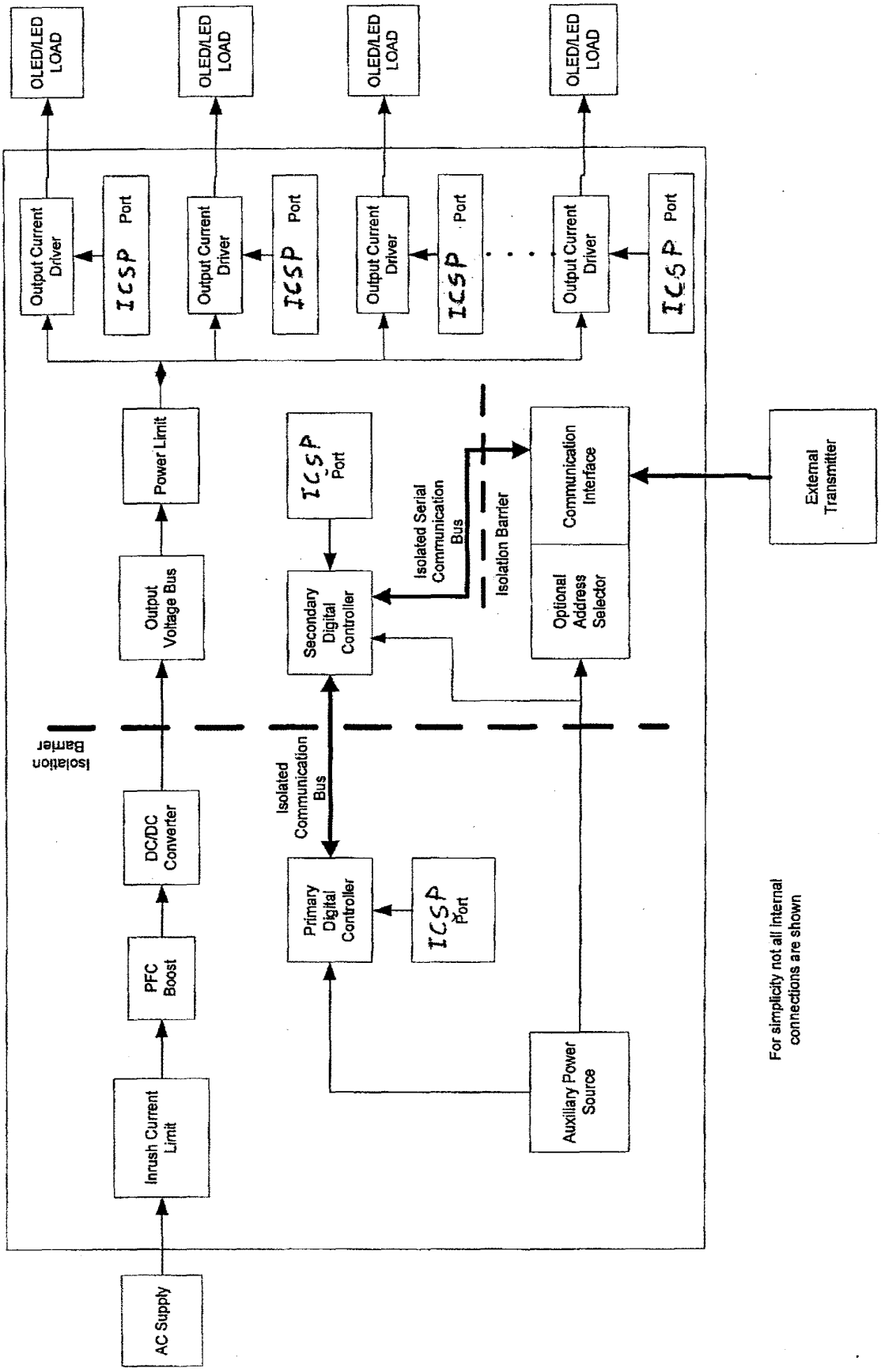
[0083] This mapping capability is also useful in zone dimming applications using 0-10Vdc analog controls as the communication interface. For example, a 12 channel output LED

Driver/Dimmer configuration can have 7 output channels grouped for a first associated 0-10Vdc signal, the next 3 channels can be grouped to a second associated 0-10Vdc control signal, and the last 2 channels can be grouped to a third associated control signal.

What is claimed is:

1. A configurable LED driver/dimmer for solid state lighting applications comprising a PFC Boost and DC/DC Converter power conversion stage with an electrical isolation barrier, output current drivers, an independent auxiliary power source, and communication interface wherein the PFC Boost and DC/DC Converter stages are controlled by a primary side digital controller and the secondary digital controller translates dimming and/or color mixing information from the external transmitter into LED control information for the output current drivers, and the primary and secondary digital controllers and output current drivers have an associated programming port for configuring the LED Driver/Dimmer.

FIGURE 1: Preferred Embodiment - Configurable LED Driver/Dimmer Block Diagram



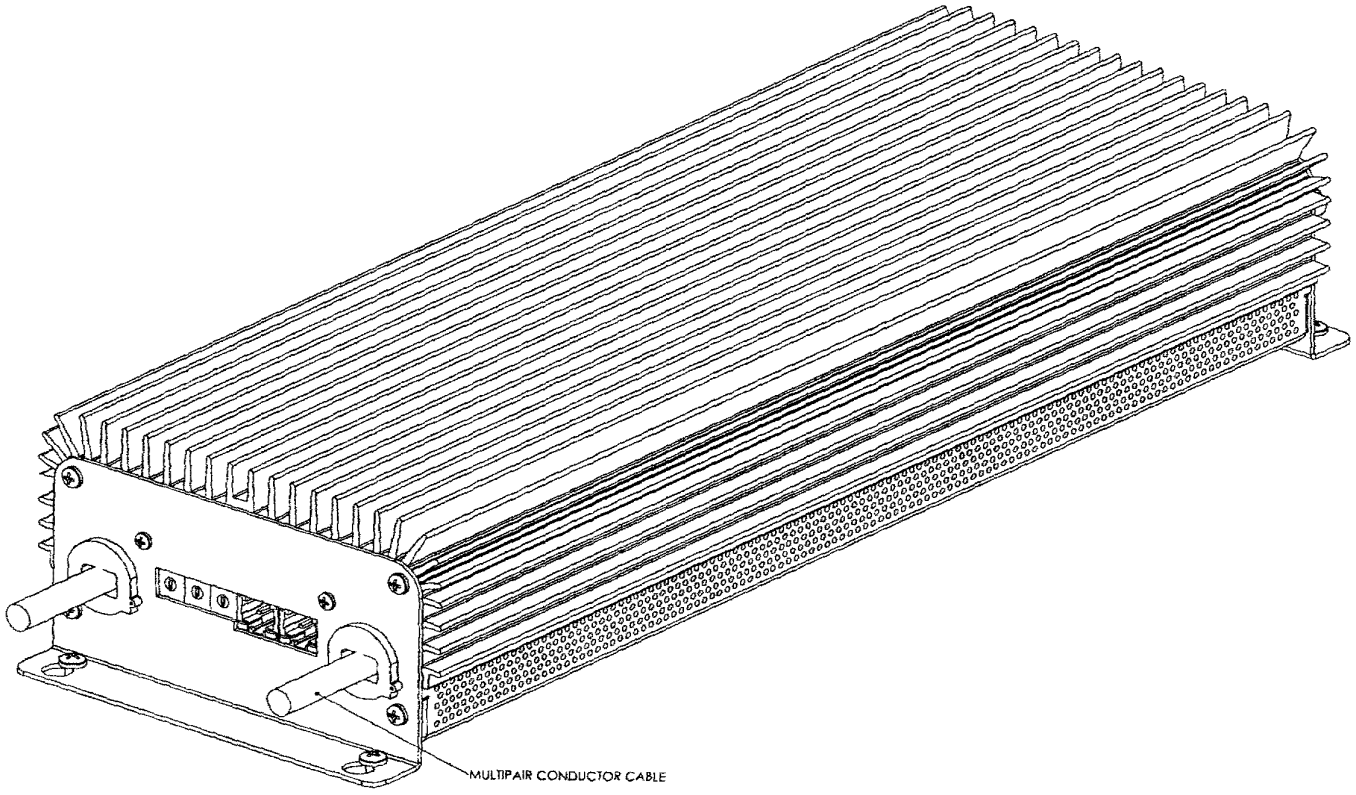
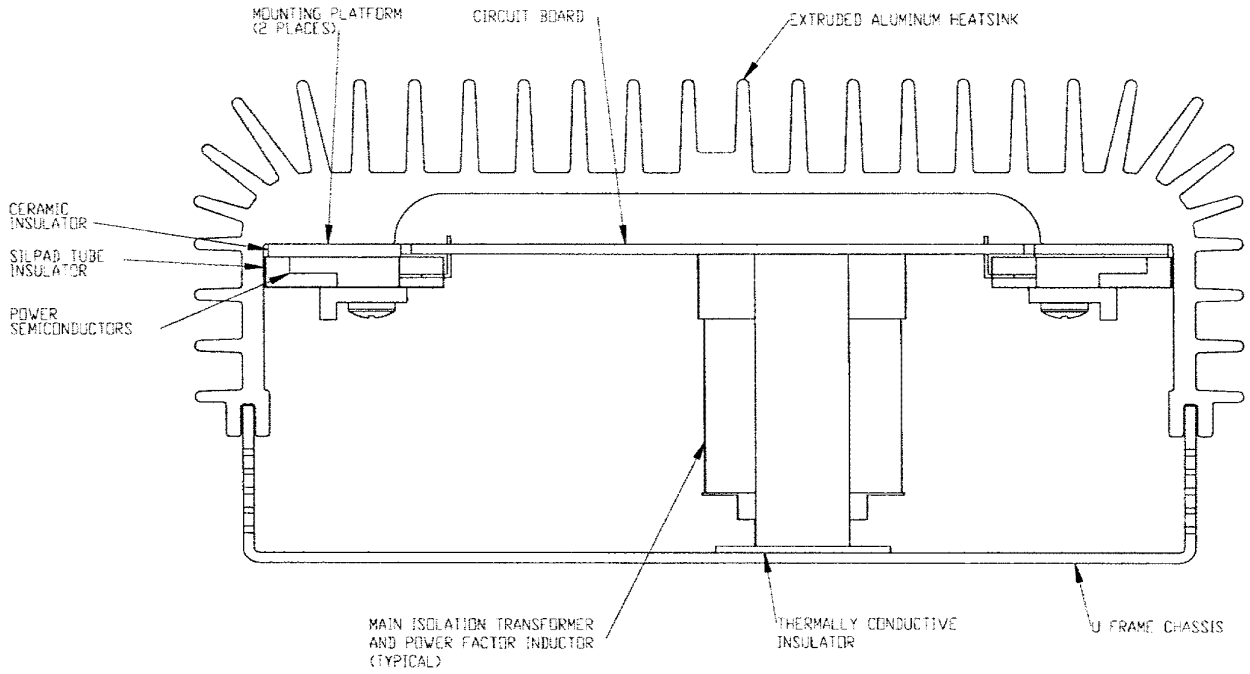
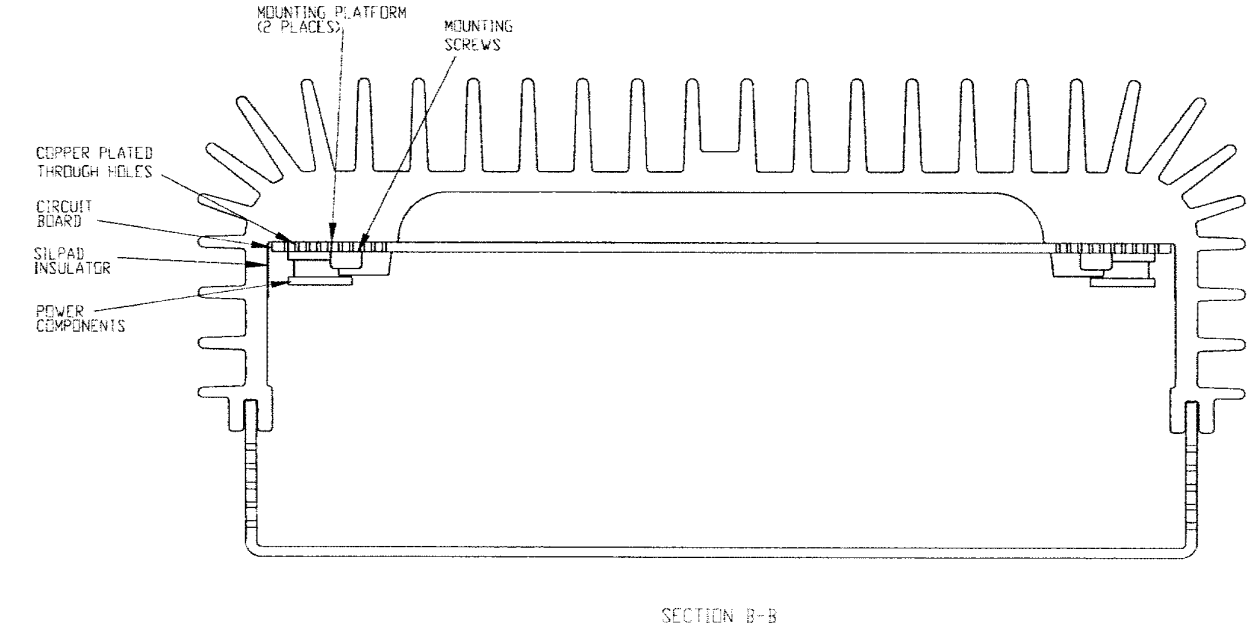


FIGURE 2: MECHANICAL CONFIGURATION OF LED DRIVER/DIMMER



SECTION A-A



SECTION B-B

FIGURE 3: MECHANICAL CROSS SECTION OF LED DRIVER DIMMER

PRIOR ART

FIGURE 4: Inrush Current Limit Circuit

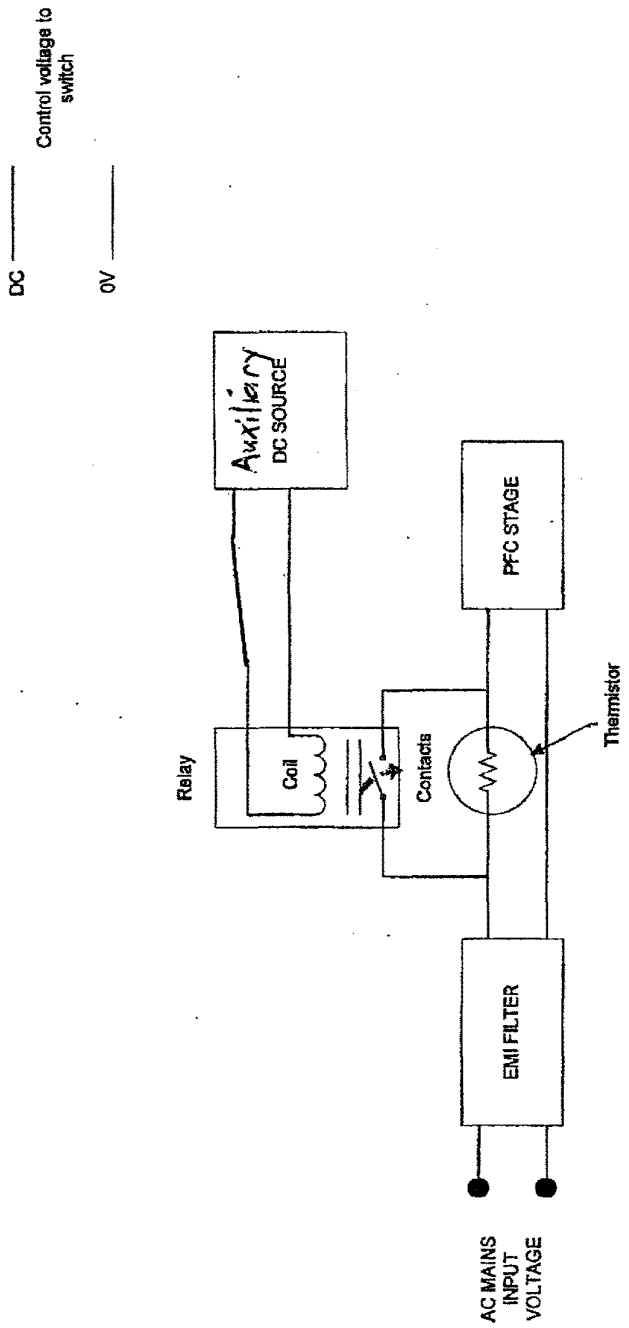
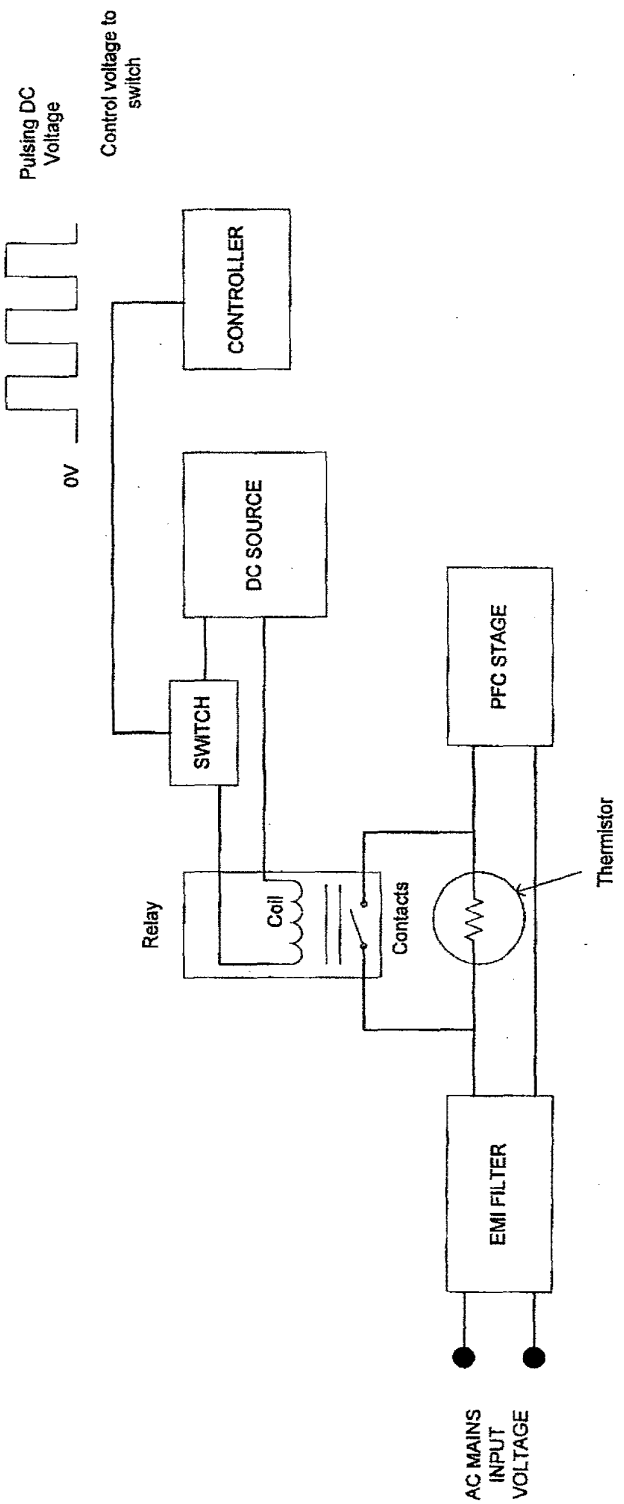


FIGURE 5: Preferred Embodiment
Inrush Current Limit Circuit



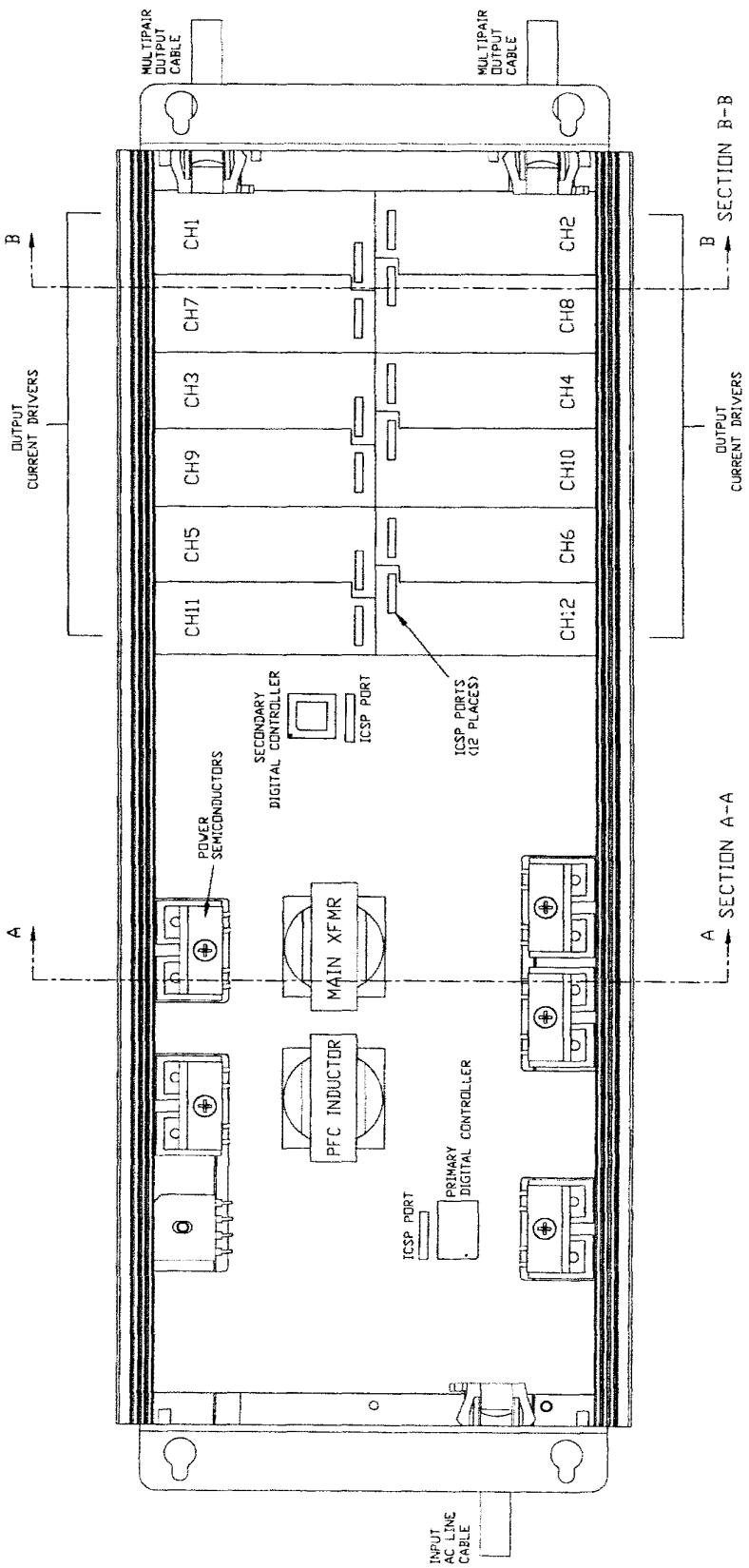


FIGURE 6: INTERNAL LAYOUT OF CONFIGURABLE LED DRIVER/DIMMER

Figure 7A - Alternate Embodiment of Output Current Driver

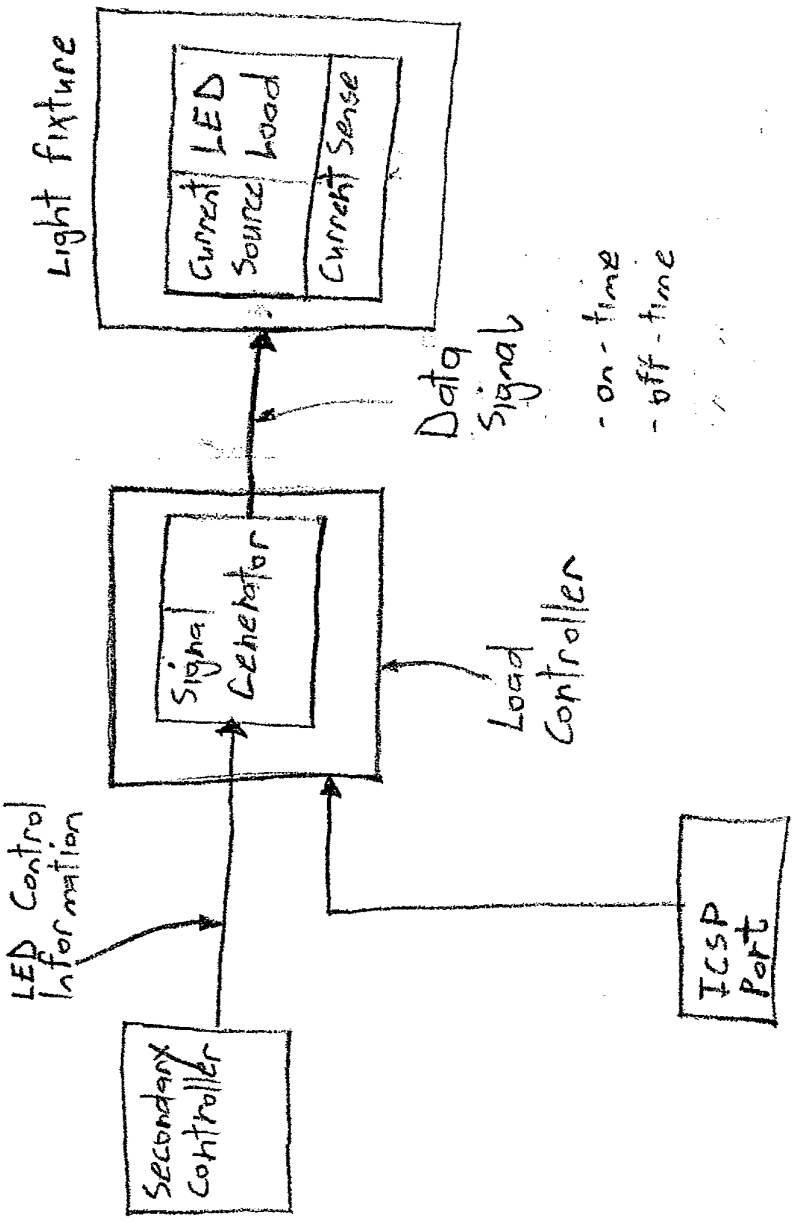


FIGURE 7: Output Current Driver
(Preferred Embodiment)

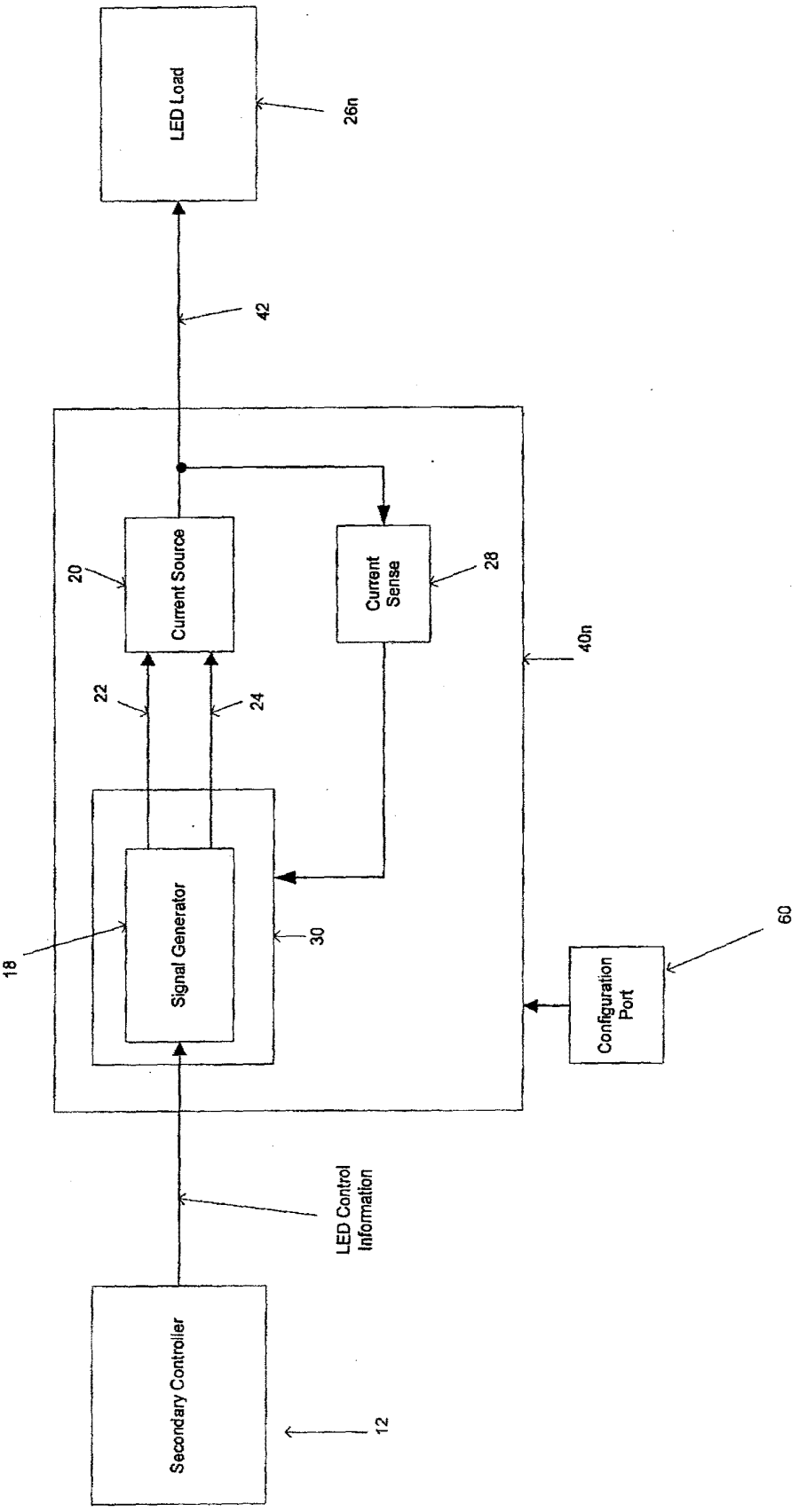
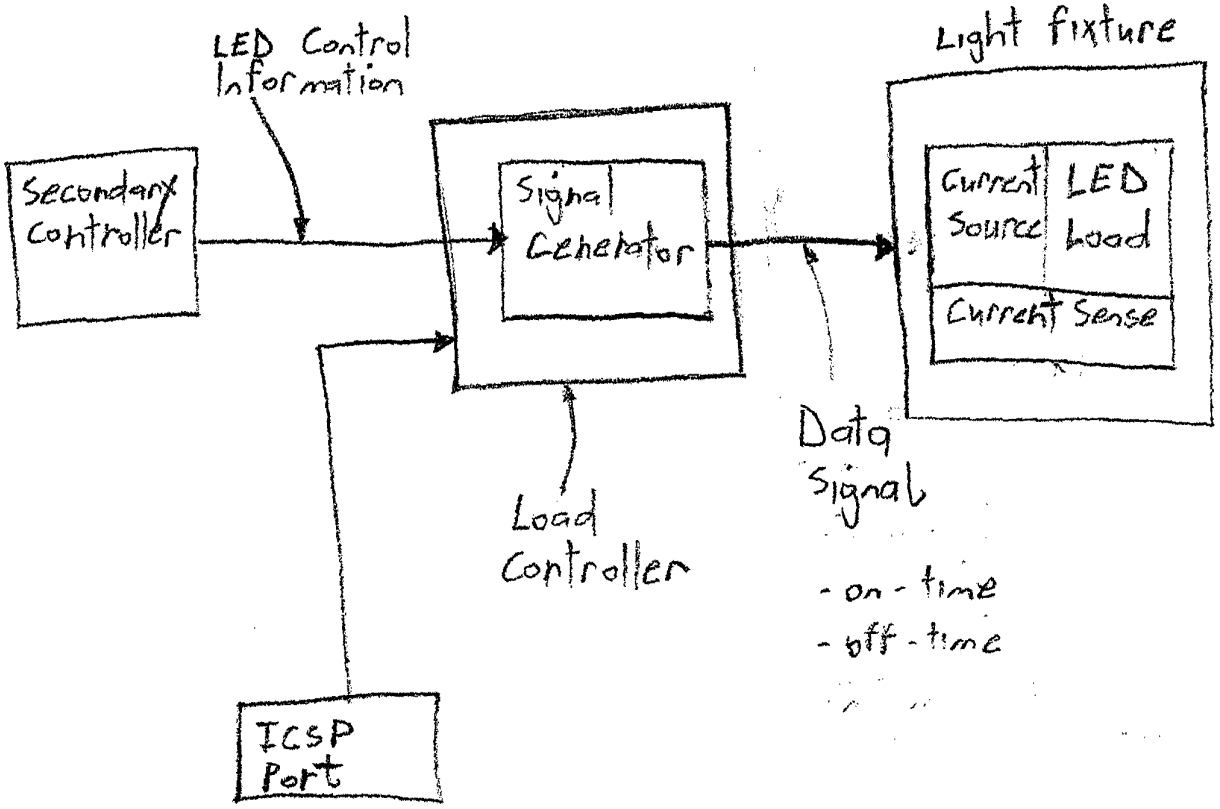


Figure 7A – Alternate Embodiment of Output Current Driver



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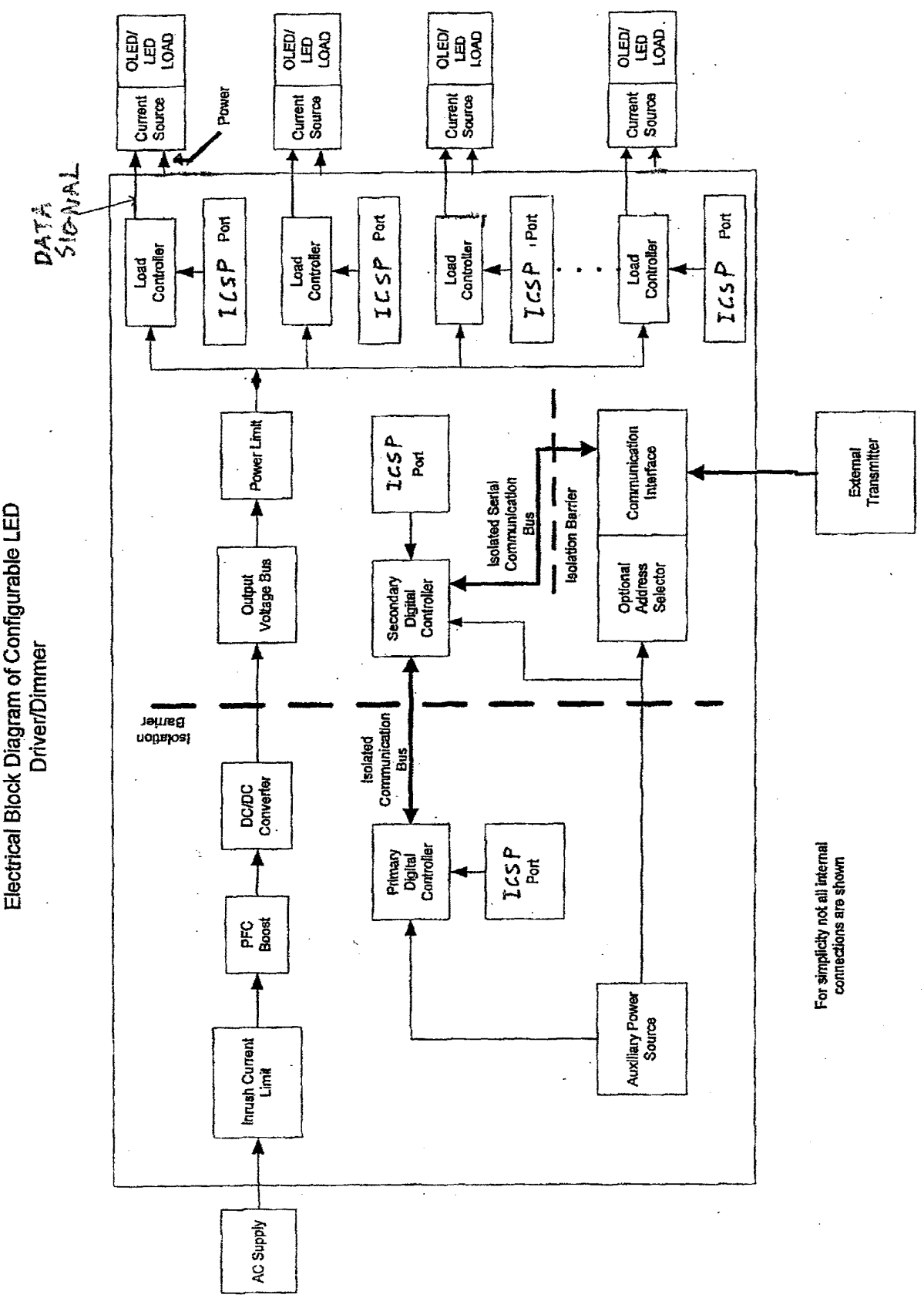


FIGURE 8: Alternate Embodiment
Electrical Block Diagram of Configurable LED Driver/Dimmer

FIGURE 9: Prior Art
Typical Application of Internal Auxiliary Power Distribution in a Multistage Power Source

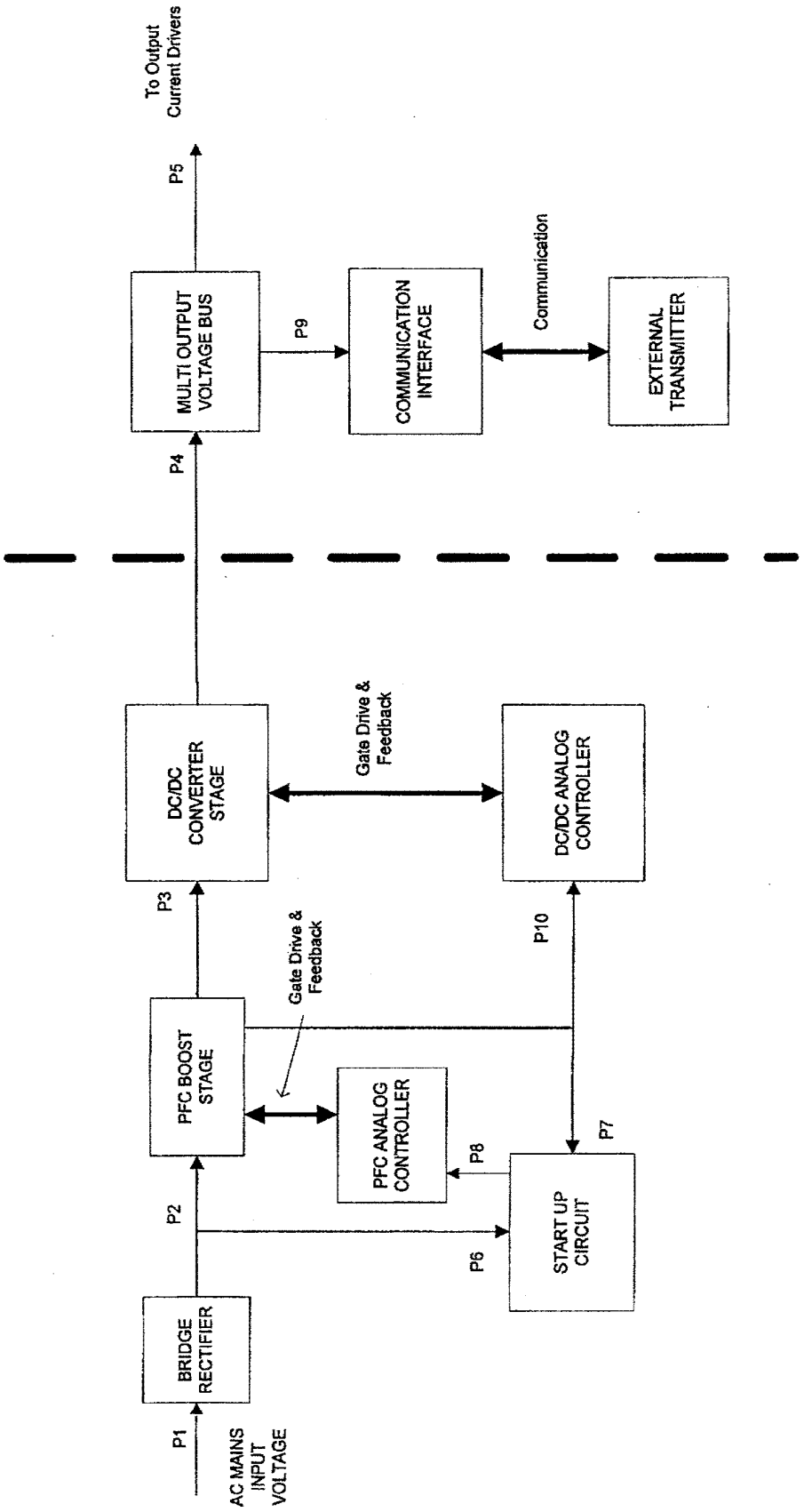


FIGURE 10:
Preferred Embodiment of Internal Auxiliary
Power Distribution in a Multistage Power Source

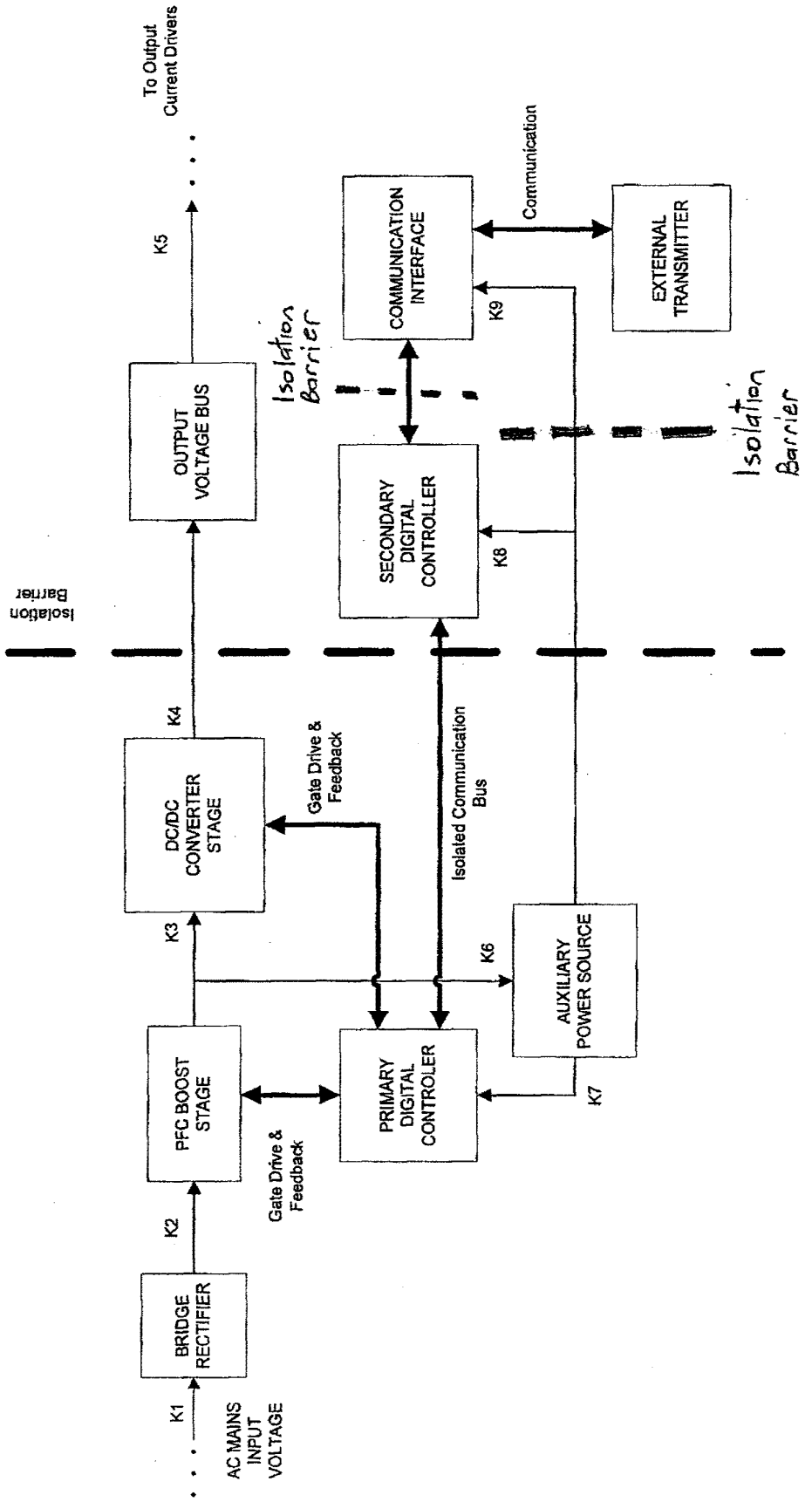
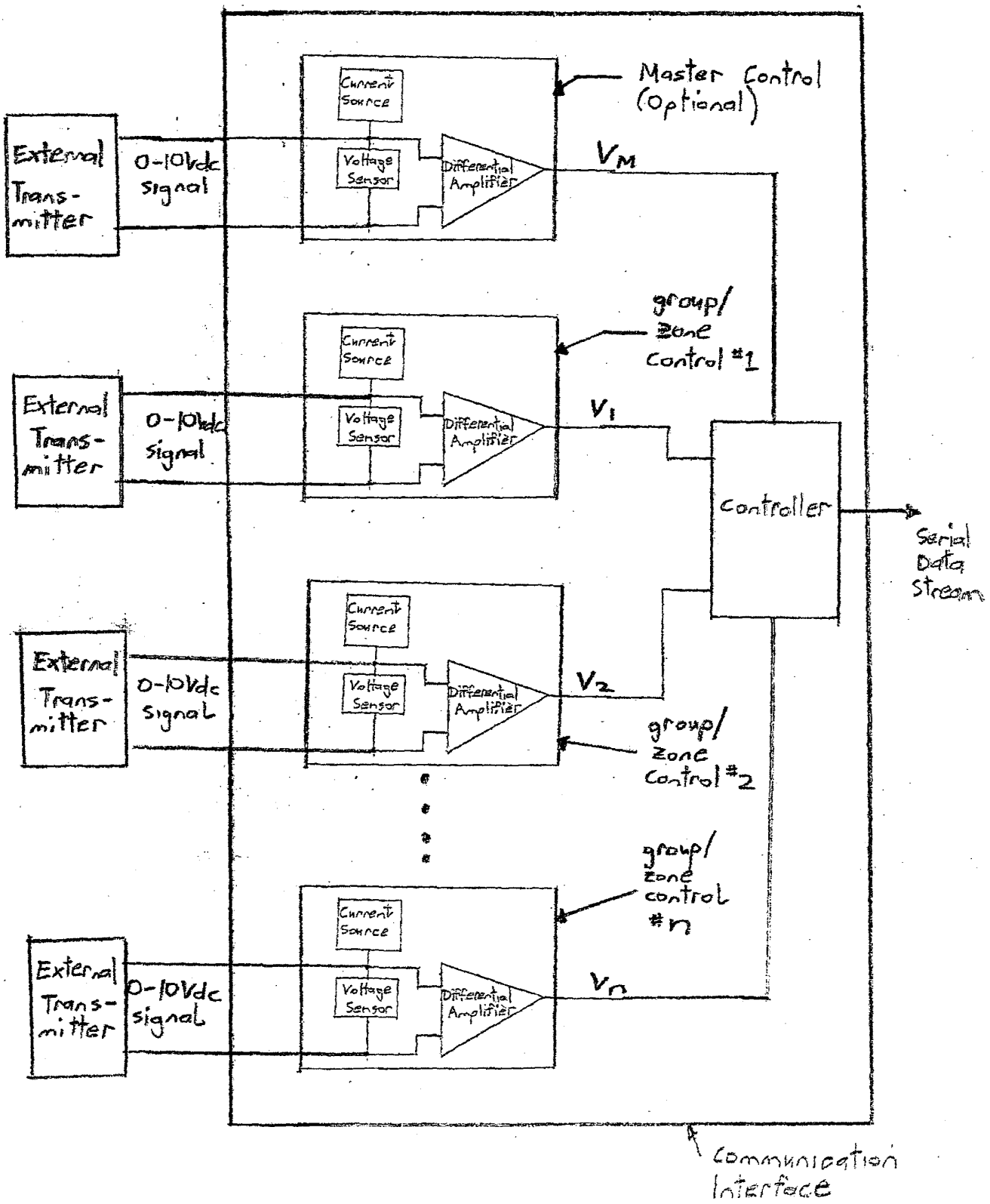


Figure #11: 0-10Vdc Analog Control Communication Interface



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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 67545P-2
	Application Number	
Title of Invention	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

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Postal Code	N2K 1E5	**Country**i	CA

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Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 67545P-2
	Application Number	
Title of Invention	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

Mailing Address of Applicant:			
Address 1	333A Mayview Crescent		
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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	26123		
Email Address	ipinfo@blgcanada.com	Add Email	Remove Email

Application Information:

Title of the Invention	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		
Attorney Docket Number	PAT 67545P-2	**Small Entity Status Claimed**	☐
Application Type	Provisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	26123		

PTO/SB/14 (07-07)
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Title of Invention	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			◉ Yes ○ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	ELECTRONIC CRAFTSMEN CORPORATION		
Mailing Address Information:			
Address 1	73 Schaefer Street		
Address 2			
City	Waterloo	**State/Province**	ON
Country [i] CA		Postal Code	N2L 4C4
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2008-09-18

PTO/SB/14 (07-07)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 67545P-2
	Application Number	
Title of Invention	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

First Name	Jeffrey W.	Last Name	Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
13/059,336	02/16/2011	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 02/16/2011

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/JUDY SWAYNE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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