Doc Code: PET.POA.WDRW
Document Description: Petition to withdraw attorney or agent (SB83)

PTO/AIA/83 (04-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	14/893,375, Patent No. 9,591,713
Filing Date	June 25, 2014
First Named Inventor	David Tikkanen
Art Unit	2844
Examiner Name	Vibol Tan
Practitioner Docket Number	6008.008

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please withdraw me as attorney or agent for the above-identified patent application, and

☐ all the practitioners of record;

☐ the practitioners (with registration numbers) of record listed on the attached paper(s); or

☒ the practitioners of record associated with Customer Number: 30589

NOTE: The immediately preceding box should only be marked when the practitioners were appointed using the listed Customer Number.

The reason(s) for this request are those described in 37 CFR:

☐ 11.116(a)(1) ☐ 11.116(a)(2) ☒ 11.116(a)(3)
☒ 11.116(b)(1) ☐ 11.116(b)(2) ☐ 11.116(b)(3)
☐ 11.116(b)(4) ☐ 11.116(b)(5) ☐ 11.116(b)(6)
☐ 11. 116(b)(7) Please explain below:

Certifications

Check each box below that is factually correct. WARNING: If a box is left unchecked, the request will likely not be approved.

1. ☒ I/We have given reasonable notice to the client, prior to the expiration of the response period, that the practitioner(s) intend to withdraw from employment.

2. ☒ I/We have delivered to the client or a duly authorized representative of the client all papers and property (including funds) to which the client is entitled.

3. ☒ I/We have notified the client of any responses that may be due and the time frame within which the client must respond.

Please provide an explanation, if necessary:

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/83 (04-13)
Approved for use through 03/31/2021. OMB 0651-0035
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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Complete the following section only when the correspondence address will change. *Changes of address will only be accepted to an applicant.*

Change the correspondence address and direct all future correspondence to:

A. ☐ The address of the applicant associated with Customer Number: _____

OR

B. ☒ Applicant

Address 219 W. Wilshire Blvd. Suite 104D

City	State	Zip	Country
Oklahoma City	Ok	73116	US

Telephone 405-520-9220 Email Jenn@onyxtheater.com

I am authorized to sign on behalf of myself and all withdrawing practitioners.

Signature /Ann M. Robl/

Name Ann M. Robl Registration No. 71541

Address 609 W. Sheridan

City	State	Zip	Country
Oklahoma City	OK	73102	US

Date April 28, 2021 Telephone No. 405-607-8600

NOTE: Withdrawal is effective when approved rather than when received.

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	42579615
Application Number:	14893375
International Application Number:	
Confirmation Number:	6653
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	30589
Filer:	Ann M. Robl/Bradley Thompson
Filer Authorized By:	Ann M. Robl
Attorney Docket Number:	6008.008
Receipt Date:	28-APR-2021
Filing Date:	23-NOV-2015
Time Stamp:	15:07:06
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	6008008_SB21Transmittal_04282021.pdf	205655 614fa3f474a06fadf8fa7c1afd51da42215a7cde	no	2

Warnings:

Information:					
2	Petition to withdraw attorney or agent (SB83)	6008008_AIA83Withdrawal_04282021.pdf	177092 f14fa78391ffa00424a24e05eff37e4d9c50afda	no	3
Warnings:					
Information:					
			Total Files Size (in bytes):	382747	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: TRAN.LET

Document Description: Transmittal Letter

PTO/SB/21 (07-09)
Approved for use through 12/31/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	14/893,375, Patent No. 9,591,713
Filing Date	June 25, 2014
First Named Inventor	David Tikkanen
Art Unit	2844
Examiner Name	Vibol Tan
Attorney Docket Number	6008.008

Total Number of Pages in This Submission: 3

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☑ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please identify below):

Remarks

Electronically Transmitted:

1) sb21 Transmittal (1 page); and,
2) aia83 Request for Withdrawal as Attorney or Agent and Change of Correspondence Address (2 pages)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Dunlap Codding, P.C.		
Signature	/Ann M. Robl/		
Printed name	Ann M. Robl		
Date	April 28, 2021	Reg. No.	71,541

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	/Ann M. Robl/		
Typed or printed name	Ann M. Robl	Date	April 28, 2021

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/893,375	11/23/2015	David TIKKANEN	K8001051WOUS

CONFIRMATION NO. 6653

POWER OF ATTORNEY NOTICE

34236
GOWLING WLG (CANADA) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

OC000000122415489

Date Mailed: 01/06/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/30/2020.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ltaba/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/893,375	11/23/2015	David TIKKANEN	6008.008

CONFIRMATION NO. 6653

POA ACCEPTANCE LETTER

30589
DUNLAP CODDING, P.C.
PO BOX 16370
OKLAHOMA CITY, OK 73113

OC000000122415526

Date Mailed: 01/06/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/30/2020.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ltaba/

PTO/AIA/80 (07-17)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

[X] Practitioners associated with Customer Number: 30589

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

[X] The address associated with Customer Number: 30589

OR

[ ]

Firm or individual name		
Address		
City	State	Zip
Country		
Telephone	Email	

Assignee name and address: Mate, LLC
219 W. Wilshire Blvd, Suite 104D
Oklahoma City, Oklahoma 73116

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature Jon Upton	Date 12/20/20
Name Jon Upton	Telephone 405-520-9220
Title Manager, Mate. LLC	

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Lumastream Canada ULC

Application No./Patent No.: 9,591,713 B2 Filed/Issue Date: March 7, 2017

Titled: APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

Mate. LLC, a limited liability corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: David Tikkanen and Kyle Hathaway To: Lumastream Canada ULC

   The document was recorded in the United States Patent and Trademark Office at Reel 032870, Frame 0291, or for which a copy thereof is attached.

2. From: Lumastream Canada ULC To: Lumastream, Inc.

   The document was recorded in the United States Patent and Trademark Office at Reel 054134, Frame 0089, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: Lumastream, Inc. To: E Craftsmen Corporation

The document was recorded in the United States Patent and Trademark Office at
Reel 054134, Frame 0330, or for which a copy thereof is attached.

4. From: E Craftsmen Corporation To: Mate. LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 054709, Frame 0940, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Ann M. Robl/	12/30/2020
Signature	Date
Ann M. Robl	71,541
Printed or Typed Name	Title or Registration Number

Electronic Acknowledgement Receipt

EFS ID:	41526085
Application Number:	14893375
International Application Number:	
Confirmation Number:	6653
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Ann M. Robl/Anne Burns
Filer Authorized By:	Ann M. Robl
Attorney Docket Number:	K8001051WOUS
Receipt Date:	30-DEC-2020
Filing Date:	23-NOV-2015
Time Stamp:	17:15:29
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	6008008_sb21_Transmittal_12302020.pdf	170466 bb9b6fd13d055a5d287a3e521e1c6cc49637092d	no	1

Warnings:

Information:					
2	Power of Attorney	6008008_AIA80_POA_12302020.pdf	109294 c60f338ba5264e1d2dc7f2111c5256ae3d4c1537	no	1
Warnings:					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73	6008008_AIA96_Statement_12302020.pdf	82062 0a98c63239fe10353ae7c014a782dbd27ef2a47c	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	361822	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: TRAN.LET

Document Description: Transmittal Letter

PTO/SB/21 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	14/893,375
Filing Date	November 23, 2015
First Named Inventor	David Tikkanen
Art Unit	2844 (conf. no. 6653)
Examiner Name	Vibol Tan
Attorney Docket Number	6008.008

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☑ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please identify below):

  See Remarks

Remarks

Electronically Transmitted: December ?, 2020

1) sb21 Transmittal (1 page);
2) AIA60 Power of Attorney (1 page); and
3) AIA96 Statement Under 37 CFR 3.73(c) (2 pages).

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	DUNLAP CODDING, P.C.		
Signature	/Ann M. Robl/		
Printed name	Ann M. Robl		
Date	December 30, 2020	Reg. No.	71,541

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being electronically transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	/Ann M. Robl/		
Typed or printed name	Ann M. Robl	Date	December 30, 2020

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/893,375	03/07/2017	9591713	K8001051WOUS	6653

34236 7590 02/15/2017

Gowling WLG (Canada) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

LUMASTREAM CANADA ULC, Calgary, AB, CANADA;
David TIKKANEN, Waterloo, ON, CANADA;
Kyle HATHAWAY, Kitchener, ON, CANADA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

34236 7590 11/10/2016
Gowling WLG (Canada) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/893,375	11/23/2015	David TIKKANEN	K8001051WOUS	6653

TITLE OF INVENTION: APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/10/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
TAN, VIBOL	2844	315-301000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Gowling WLG (Canada) LLP
2 Jeffrey W. Wong
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: LUMASTREAM CANADA ULC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Calgary, Alberta, Canada

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 501613 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jeffrey W. Wong/ Date January 24, 2017

Typed or printed name Jeffrey W. Wong Registration No. 46414

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	14893375
Filing Date:	23-Nov-2015
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Filer:	Jeffrey Wong/Ryan Waugh
Attorney Docket Number:	K8001051WOUS

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt

EFS ID:	28145556
Application Number:	14893375
International Application Number:	
Confirmation Number:	6653
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Ryan Waugh
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001051WOUS
Receipt Date:	24-JAN-2017
Filing Date:	23-NOV-2015
Time Stamp:	10:12:39
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$960
RAM confirmation Number	012417INTEFSW00009794501613
Deposit Account	501613
Authorized User	Jeffrey Wong

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

37 CFR 1.492 (National application filing, search, and examination fees)

37 CFR 1.492(a) (Basic national fee only)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	K8001051WOUS-Issue-Fee-Transmittal.pdf	228060 3786067f0f4b448876be33a573ca728bb4eb9eb1	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30770 4e895b00ace0180848a0abdd1c6561695ba61813	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	258830		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

34236 7590 11/10/2016

Gowling WLG (Canada) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2844	

DATE MAILED: 11/10/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/893,375	11/23/2015	David TIKKANEN	K8001051WOUS	6653

TITLE OF INVENTION: APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/10/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

34236 7590 11/10/2016
Gowling WLG (Canada) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/893,375	11/23/2015	David TIKKANEN	K8001051WOUS	6653

TITLE OF INVENTION: APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/10/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
TAN, VIBOL	2844	315-301000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/893,375	11/23/2015	David TIKKANEN	K8001051WOUS	6653

34236 7590 11/10/2016

Gowling WLG (Canada) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

EXAMINER	
TAN, VIBOL	
ART UNIT	**PAPER NUMBER**
2844	

DATE MAILED: 11/10/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/893,375	Applicant(s) TIKKANEN ET AL.	
	Examiner Vibol Tan	Art Unit 2844	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *after final amendment filed 10/27/16*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5,7-11 and 19-21*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach or suggest wherein if the load power exceeds the predetermined power limit, the power limit controller internally generates and transmits a signal to the current source controller to control the load power to the load, wherein the signal is based on internal controls, as required by amended claim 1.

3. Claims 1-5, 7-11, and 19-21 are now in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alex Taningco can be reached on (571) 272-8048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2844

Receipt date: 10/27/2016

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14893375
Filing Date	2015-11-23
First Named Inventor	TIKKANEN, David
Art Unit	2844
Examiner Name	TAN, Vibol
Attorney Docket Number	K8001051WOUS

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/V.T/	1	7804189		2010-09-28	KOEHLER ET AL.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Receipt date: 10/27/2016

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Filing Date	2015-11-23
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Art Unit	2844
Examiner Name	TAN, Vibol
Attorney Docket Number	K8001051WOUS

	1	

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature	/VIBOL TAN/	Date Considered	11/03/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Receipt date: 10/27/2016

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14893375
Filing Date	2015-11-23
First Named Inventor	TIKKANEN, David
Art Unit	2844
Examiner Name	TAN, Vibol
Attorney Docket Number	K8001051WOUS

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2016-10-27
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14893375	TIKKANEN ET AL.
	Examiner	**Art Unit**
	VIBOL TAN	2844

CPC							
Symbol						**Type**	**Version**
H05B		33	/	089		F	2013-01-01
H05B		33	/	0887		I	2013-01-01
H05B		33	/	0815		I	2013-01-01
H05B		33	/	0896		I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	13	
/VIBOL TAN/ Primary Examiner.Art Unit 2844	11/03/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1b

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14893375	TIKKANEN ET AL.
	Examiner	**Art Unit**
	VIBOL TAN	2844

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		H	0	5	B	33 / 08 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	13	
/VIBOL TAN/ Primary Examiner.Art Unit 2844	11/03/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1b

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14893375	TIKKANEN ET AL.
	Examiner	**Art Unit**
	VIBOL TAN	2844

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17												
2	2		18												
3	3	11	19												
4	4	12	20												
5	5	13	21												
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6	7														
7	8														
8	9														
9	10														
10	11														
	12														
	13														
	14														
	15														
	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 13	
/VIBOL TAN/ Primary Examiner.Art Unit 2844 (Primary Examiner)	11/03/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1b

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In The Matter of United States Patent Application:

Applicant	:	**Lumastream Canada ULC**
Application No.	:	**14/893,375**
Filed	:	**June 25, 2014**
Title	:	**APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES**
TC/A.U.	:	**2844**
Examiner	:	**TAN, Vibol**
Docket No.	:	**K8001051WOUS**
Conf Number	:	**6653**
Date	:	**October 27, 2016**

MAIL STOP AF

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

OK TO ENTER: /V.T/

AMENDMENT AND RESPONSE TO OFFICE ACTION

In response to the Office Action of September 6, 2016, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page **2** of this paper.

Remarks/Arguments begin on page **5** of this paper.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6653

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/893,375	11/23/2015	315	2844	K8001051WOUS

APPLICANTS

LUMASTREAM CANADA ULC, Calgary, AB, CANADA;

INVENTORS

David TIKKANEN, Waterloo, ON, CANADA;
Kyle HATHAWAY, Kitchener, ON, CANADA;

**** CONTINUING DATA ***************************

This application is a 371 of PCT/CA2014/050609 06/25/2014
which claims benefit of 61/838,965 06/25/2013

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

01/26/2016

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /VIBOL TAN/ Examiner's Signature	☐ Met after Allowance VTan Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		ON	9	21	2

ADDRESS

Gowling WLG (Canada) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

TITLE

APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

FILING FEE RECEIVED		
1560	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14893375	TIKKANEN ET AL.
	Examiner	Art Unit
	VIBOL TAN	2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B33/0815 H05B33/0818 H05B33/0827 H05B37/02 H05B37/029 H05B39/04 H05B41/36 H05B33/089 H05B33/0896 and text	4/4/2016	VTan

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
pct/ca2014/050609	4/4/2016	VTan
EAST text search	4/4/2016	VTan
EAST text update	8/30/2016	VTan
EAST text update	11/3/2016	VTan

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
uspgpub & upat	text	11/3/2016	VTan

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14893375	TIKKANEN ET AL.
	Examiner	Art Unit
	VIBOL TAN	2844

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/03/2016								
1	1	=								
2	2	=								
3	3	=								
4	4	=								
5	5	=								
	6	-								
6	7	=								
7	8	=								
8	9	=								
9	10	=								
10	11	=								
	12	-								
	13	-								
	14	-								
	15	-								
	16	-								
	17	-								
	18	-								
11	19	=								
12	20	=								
13	21	=								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	32	(US-20140192102-$ or US-20140160802-$ or US-20140055439-$ or US-20140015412-$ or US-20130221871-$ or US-20110316446-$ or US-20120126703-$ or US-20120032610-$ or US-20130300310-$ or US-20120194087-$ or US-20100026208-$ or US-20120200229-$ or US-20120280637-$ or US-20130300312-$ or US-20110204820-$ or US-20070103086-$ or US-20120313529-$ or US-20120313528-$).did. or (US-8525422-$ or US-8975825-$ or US-8638045-$ or US-8957601-$ or US-D662880-$ or US-8525446-$ or US-8299987-$ or US-9024541-$ or US-7719248-$ or US-7671571-$).did. or (US-20140055439-$ or US-20140160802-$ or US-20140192102-$ or US-20120126703-$).did.	US-PGPUB; USPAT; DERWENT	OR	OFF	2016/11/03 16:18
L2	28	TIKKANEN-David.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/11/03 16:20
L3	13	HATHAWAY-Kyle.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/11/03 16:21
L4	28	2 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/11/03 16:21
S1	326	(("2014205575") or ("2913239") or ("8957601") or ("9049759") or ("20120280637") or ("20130300312") or ("20150108912") or ("20150115839") or ("8525446") or ("9078310") or ("2010031169") or ("20110204820") or ("2734757") or ("2734757") or ("9013114") or ("20130214697") or ("2627155") or ("20080303456") or ("7626342") or ("102640570") or ("2008154069") or ("102754525") or ("2499220") or ("2013510388") or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/03/31 17:20

		("102577606") or ("102577606") or ("2497339") or ("2011055284") or ("2013509683") or ("20120223650") or ("102132628") or ("102132628") or ("8432108") or ("102573210") or ("102573210") or ("2491764") or ("2013072784") or ("20100117545") or ("2011049703") or ("2752089") or ("20140285103") or ("9301347") or ("5102257") or ("102598870") or ("20130038234") or ("2564668") or ("2011135505") or ("2014116100") or ("20140252992") or ("2749130") or ("2013054297") or ("2777512") or ("103918349") or ("2777512") or ("2013524472") or ("2014532274") or ("2014535146") or ("103947289") or ("6191568") or ("2014200450") or ("2010308455") or ("2259055") or ("2484179") or ("2010308455") or ("20120274216") or ("20160029446") or ("101686591") or ("2494852") or ("5773394") or ("20100045210") or ("2011051859")).PN.				
S2	7	(("8299987") or ("20130049634")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/04/01 14:30
S3	20411	(power adj converter) same controller same (abnormal or fault or (over adj threshold or current or power or voltage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:36
S4	1435	(power adj converter) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:38
S5	70	(power adj converter) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:40
S6	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (power adj limit$4) same driver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:50
S7	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or	US-PGPUB; USPAT;	OR	ON	2016/04/01 14:50

		((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (power adj limit$4) same driv$3	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S8	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:52
S9	1	(power adj (converter or circuit$2)) same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:53
S10	6	controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:53
S11	379	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 15:03
S12	0	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (power adj limit$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 15:03
S13	39	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (dim or dimmer or dimming)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 15:09
S14	43534	(H05B33/0815 H05B33/0818 H05B33/0827 H05B37/02 H05B37/029 H05B39/04 H05B41/36 H05B33/089 H05B33/0896).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:00
S15	4189	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2016/04/04 12:01

			IBM_TDB			
S16	3650	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:14
S17	2090	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and converter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:15
S18	558	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:15
S19	555	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2016/04/04 12:16
S20	59	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter) and (output near1 driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:17
S21	9	lumastream adj canada adj ulc.as.	US-PGPUB; USPAT	OR	ON	2016/04/04 14:27
S22	0	("20110204820").PN.	USPAT	OR	OFF	2016/04/04 14:37
S23	1	("20110204820").PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 14:37
S24	2	(("20110204820") or ("8525446")).PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 14:59
S25	1	("20070103086").PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 15:05
S26	2776	controller same (digital adj filter)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:39
S27	762	controller near5 (digital adj filter)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:39
S28	0	(controller near5 (digital adj filter)) same (output near1 driver)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:40
S29	1	(controller near5 (digital adj filter)) same (output near1 driver)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:40
S30	4	(power near1 controller near5 (digital adj filter))	US-PGPUB; USPAT	OR	ON	2016/04/05 10:42
S31	4	(power near1 controller) near5 (digital adj filter)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:43
S32	16	(power near1 controller) same (digital adj	US-PGPUB;	OR	ON	2016/04/05

		filter)	USPAT			10:44
S33	0	controller same (digital adj filter) same (electronic adj ballast)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:46
S34	16	controller same (digital adj filter) and (electronic adj ballast)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:46
S35	2641	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same ((fault$1 or abnormal) adj condition)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:41
S36	6	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same ((fault$1 or abnormal) adj condition) same (power adj limit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:43
S37	1	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (fault$1 or abnormal) same (power adj limit adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:56
S38	2	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (power adj limit adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:56
S39	3540	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (power near1 controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:57
S40	135	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (fault$1 or abnormal) same (power near1 controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:57
S41	12	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (fault$1 or abnormal) same (power near1 controller) same protect$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:58
S42	2096	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) and (fault$1 or abnormal) and (power near1 controller) and protect$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2016/08/30 13:59

			IBM_TDB			
S43	6	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) and ((fault$1 or abnormal) adj condition) and (power adj limit adj controller) and protect$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 14:00
S44	1	("7804189").PN.	US-PGPUB; USPAT	OR	OFF	2016/11/03 15:39

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	1	((power adj circuit) and (power adj limit adj controller) and (load adj power)).clm.	US-PGPUB; USPAT	OR	ON	2016/11/03 16:29

11/3/2016 4:30:19 PM
C:\Users\vtan\Documents\EAST\Workspaces\14893375.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In The Matter of United States Patent Application:

Applicant	:	**Lumastream Canada ULC**
Application No.	:	**14/893,375**
Filed	:	**June 25, 2014**
Title	:	**APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES**
TC/A.U.	:	**2844**
Examiner	:	**TAN, Vibol**
Docket No.	:	**K8001051WOUS**
Conf Number	:	**6653**
Date	:	**October 27, 2016**

MAIL STOP AF

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND RESPONSE TO OFFICE ACTION

In response to the Office Action of September 6, 2016, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page **2** of this paper.

Remarks/Arguments begin on page **5** of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) Apparatus for controlling power to a solid state lighting (SSL) device load comprising:

a power circuit for receiving power from an external source;

at least one power limit connected to the power circuit;

at least one output current driver for supplying a load power to the SSL device load, the at least one output current driver connected to the at least one power limit; and

a power limit controller;

wherein the power circuit transmits the power to the at least one power limit which, in turn, transmits a current to the at least one output current driver;

wherein the power limit controller directly or indirectly monitors a level of the load power and controls the at least one power limit to reduce the level of the load power for a predetermined period of time when the load power exceeds a predetermined power limit;

wherein if the load power exceeds the predetermined power limit, the power limit controller internally generates and transmits a signal to the current source controller to control the load power to the load;

wherein the signal is based on internal controls.

2. (Original) The apparatus of claim 1 wherein the at least one power limit is integrated within one of the at least one output current drivers.

3. (Original) The apparatus of claim 1 wherein the at least one power limit comprises:

the power limit controller;

a power monitor; and

a fault optocoupler,

wherein if the load power exceeds the predetermined power limit, the power limit controller transmits a signal to the fault optocoupler to control the load power.

4. (Original) The apparatus of claim 3 further comprising:

a power circuit controller;

wherein the fault optocoupler transmits a signal to the power circuit controller to control the power being supplied to the power limit.

5. (Original) The apparatus of claim 1 wherein the at least one output current driver comprises:

an output current source;

a current sense; and

a current source controller.

6. (Cancelled)

7. (Original) The apparatus of claim 1 wherein the power limit controller comprises a digital filter.

8. (Original) The apparatus of claim 7 wherein the power limit controller comprises at least one port.

9. (Original) The apparatus of claim 8 wherein the at least one port receives instructions to calibrate the at least one power limit to the predetermined power limit.

10. (Previously Presented) The apparatus of claim 3 wherein the power monitor comprises a current sense.

11. (Previously Presented) The apparatus of claim 1 wherein the at least one output current driver reduces the load power by a pulsing technique.

Claims 12–18. (Cancelled)

19. (Previously Presented) The apparatus of claim 2 wherein the at least one power limit comprises:

the power limit controller;

a power monitor; and

a fault optocoupler,

wherein if the load power exceeds the predetermined power limit, the current source controller transmits a signal to the fault optocoupler to control the load power.

20. (Previously Presented) The apparatus of claim 1 wherein the at least one output current driver reduces load power by a constant current reduction technique.

21. (Original) The apparatus of claim 1 wherein the SSL device load is one of an organic light emitting diode (OLED) load, a light emitting diode (LED) load or a LED array load.

REMARKS/ARGUMENTS

Claims 1 to 5, 7 to 11, and 19 to 21 remain in the current application. Claims 12 to 18 have been cancelled. Claim 6 was previously cancelled.

Claims 12 to 18 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by US Patent No. 7,671,571 to Burlak et al. ("Burlak"). Claims 12 to 18 have been cancelled. Applicant respectfully reserves the right to file the subject matter of the cancelled claims. Retraction of Examiner's rejection of claims 12 to 18 is respectfully requested.

For the above reasons, it is respectfully submitted that the application is now in condition for allowance, which is requested. If there are any outstanding issues, the Examiner is invited to contact the undersigned to discuss this matter further.

The Commissioner is hereby authorized to charge any additional fees, and credit any payments, to Deposit Account No. 501613, in the name of Gowling WLG (Canada) LLP.

Respectfully submitted,

By: /Jeffrey W. Wong/

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Electronic Patent Application Fee Transmittal

Application Number:	14893375
Filing Date:	23-Nov-2015
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Filer:	Jeffrey Wong/Christopher Kreider
Attorney Docket Number:	K8001051WOUS

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	27342804
Application Number:	14893375
International Application Number:	
Confirmation Number:	6653
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001051WOUS
Receipt Date:	27-OCT-2016
Filing Date:	23-NOV-2015
Time Stamp:	15:10:53
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$180
RAM confirmation Number	102816INTEFSW00001524501613
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	K8001051WOUS-IDS.pdf	1082206 22e20a2baadd614518554c362eef0b78ecea5e1b	no	4
Warnings:					
Information:					
2		K8001051WOUS-Response.pdf	60848 a686fe6521ca11cf9d82b5611489b4528ccb8a40	yes	5

Multipart Description/PDF files in .zip description

Document Description	Start	End
Response After Final Action	1	1
Claims	2	4
Applicant Arguments/Remarks Made in an Amendment	5	5

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30998 00e57efc1c5415b87644b4e059d36a722a7aecfa	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1174052		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14893375
Filing Date	2015-11-23
First Named Inventor	TIKKANEN, David
Art Unit	2844
Examiner Name	TAN, Vibol
Attorney Docket Number	K8001051WOUS

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7804189		2010-09-28	KOEHLER ET AL.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14893375
	Filing Date	2015-11-23
	First Named Inventor	TIKKANEN, David
	Art Unit	2844
	Examiner Name	TAN, Vibol
	Attorney Docket Number	K8001051WOUS

	1	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14893375
Filing Date	2015-11-23
First Named Inventor	TIKKANEN, David
Art Unit	2844
Examiner Name	TAN, Vibol
Attorney Docket Number	K8001051WOUS

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2016-10-27
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/06 (09-11)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/893,375	Filing Date 11/23/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **10/27/2016**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 16	Minus	** 21	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DAVID SASFAI/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/893,375	11/23/2015	David TIKKANEN	K8001051WOUS	6653

34236 7590 09/06/2016

Gowling WLG (Canada) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2844	

NOTIFICATION DATE	DELIVERY MODE
09/06/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

VAL.COTTRILL@GOWLINGWLG.COM
Waterloo.IP@gowlingwlg.com
JEFF.WONG@GOWLINGWLG.COM

Office Action Summary	Application No. 14/893,375	Applicant(s) TIKKANEN ET AL.	
	Examiner Vibol Tan	Art Unit 2844	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed 8/24/16*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-5 and 7-21* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *1-5,7-11 and 19-21* is/are allowed.

7)☒ Claim(s) *12-18* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *8/24/16* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

3. Claim(s) 12-18 is/are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Burlak et al. (U. S. PAT. 7,671,571).

In claim 12, Burlak teaches all claimed features in Figs. 1-2, a method of controlling power to a solid state lighting (SSL) device load (104 could represent a lamp; col. 2, line 65) comprising:

receiving an input power (110);

delivering load power (power signal 112 supplies power to the load 104; col. 2, line 52) to the SSL device load (104);

monitoring current level in load power (col. 5, line 2; 126 could also ensure that an excessive amount of current and/or power is not supplied to the load);

reducing load power (col. 4, line 67; output power device 102 allows the load 104 to pull a reduced amount of current or power from the output power device 102) to the SSL device for a predetermined period of time after a predetermined operational fault

condition (a reference temperature measurement of the output power device 102 is approaching a critical level; col. 4, lines 58-59) is met;

wherein if the load power exceeds (excessive amount of current and/or power) a predetermined power limit, transmitting an internally generated signal (from 126 to 124) to a current source controller (120) to control the load power to the SSL load (104); wherein the generated signal is based on internal controls (col. 5, lines 6-7; 126 includes any hardware, software, firmware, or any combination thereof read on the internal controls).

In claim 13, Burlak further teaches the method of claim 12 wherein the predetermined operational fault condition is one of a single component failure, an external light emitting diode (LED) fault and an overload condition (a passive short circuit condition; col. 9, line 35).

In claim 14, Burlak further teaches the method of claim 12 wherein monitoring current level in load power comprises: sensing current delivered by an output bus (interconnect between 120 and 126) to a power limit (126) or sensing current delivered to a load by an output current driver.

In claim 15, Burlak further teaches the method of claim 12 further comprising: gradually increasing load power (power signal 112) to a normal operational power level.

In claim 16, Burlak further teaches the method of claim 15 wherein the load power (power signal 112) is gradually increased at predetermined time intervals (inherent).

In claim 17, Burlak further teaches the method of claim 15 wherein the load power (power signal 112) is gradually increased in predetermined power increments (inherent).

In claim 18, Burlak further teaches the method of claim 12 wherein if a maximum power threshold is met, load power delivered to the load is disabled (col. 3, line 17; …causes output power device 102 to stop providing the power signal 112 to the load 104).

Allowable Subject Matter

4. Claims 1-5, 7-11 and 19-21 appear to comprise allowable subject matter.

Response to Arguments

5. Applicant's arguments with respect to claims 12-18 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alex Taningco can be reached on (571) 272-8048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2844

Notice of References Cited	Application/Control No. 14/893,375	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.	
	Examiner Vibol Tan	Art Unit 2844	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-7,671,571 B2	03-2010	Burlak; Gary J.	H02M1/32	323/275
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14893375	TIKKANEN ET AL.
	Examiner	Art Unit
	VIBOL TAN	2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B33/0815 H05B33/0818 H05B33/0827 H05B37/02 H05B37/029 H05B39/04 H05B41/36 H05B33/089 H05B33/0896 and text	4/4/2016	VTan

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
pct/ca2014/050609	4/4/2016	VTan
EAST text search	4/4/2016	VTan
EAST text update	8/30/2016	VTan

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	326	(("2014205575") or ("2913239") or ("8957601") or ("9049759") or ("20120280637") or ("20130300312") or ("20150108912") or ("20150115839") or ("8525446") or ("9078310") or ("2010031169") or ("20110204820") or ("2734757") or ("2734757") or ("9013114") or ("20130214697") or ("2627155") or ("20080303456") or ("7626342") or ("102640570") or ("2008154069") or ("102754525") or ("2499220") or ("2013510388") or ("102577606") or ("102577606") or ("2497339") or ("2011055284") or ("2013509683") or ("20120223650") or ("102132628") or ("102132628") or ("8432108") or ("102573210") or ("102573210") or ("2491764") or ("2013072784") or ("20100117545") or ("2011049703") or ("2752089") or ("20140285103") or ("9301347") or ("5102257") or ("102598870") or ("20130038234") or ("2564668") or ("2011135505") or ("2014116100") or ("20140252992") or ("2749130") or ("2013054297") or ("2777512") or ("103918349") or ("2777512") or ("2013524472") or ("2014532274") or ("2014535146") or ("103947289") or ("6191568") or ("2014200450") or ("2010308455") or ("2259055") or ("2484179") or ("2010308455") or ("20120274216") or ("20160029446") or ("101686591") or ("2494852") or ("5773394") or ("20100045210") or ("2011051859")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/03/31 17:20
S2	7	(("8299987") or ("20130049634")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/04/01 14:30
S3	20411	(power adj converter) same controller same (abnormal or fault or (over adj threshold or current or power or voltage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:36
S4	1435	(power adj converter) same controller same (abnormal or fault or ((over or	US-PGPUB; USPAT;	OR	ON	2016/04/01 14:38

		exceed$3) adj (threshold or current or power or voltage)))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S5	70	(power adj converter) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:40
S6	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (power adj limit$4) same driver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:50
S7	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (power adj limit$4) same driv$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:50
S8	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:52
S9	1	(power adj (converter or circuit$2)) same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:53
S10	6	controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:53
S11	379	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 15:03
S12	0	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/04/01 15:03

		adj state adj lighting) or ssl.u/c.) same (power adj limit$4)	DERWENT; IBM_TDB			
S13	39	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (dim or dimmer or dimming)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 15:09
S14	43534	(H05B33/0815 H05B33/0818 H05B33/0827 H05B37/02 H05B37/029 H05B39/04 H05B41/36 H05B33/089 H05B33/0896).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:00
S15	4189	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:01
S16	3650	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:14
S17	2090	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and converter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:15
S18	558	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:15
S19	555	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2016/04/04 12:16
S20	59	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter) and (output near1 driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:17
S21	9	lumastream adj canada adj ulc.as.	US-PGPUB; USPAT	OR	ON	2016/04/04 14:27
S22	0	("20110204820").PN.	USPAT	OR	OFF	2016/04/04

						14:37
S23	1	("20110204820").PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 14:37
S24	2	(("20110204820") or ("8525446")).PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 14:59
S25	1	("20070103086").PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 15:05
S26	2776	controller same (digital adj filter)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:39
S27	762	controller near5 (digital adj filter)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:39
S28	0	(controller near5 (digital adj filter)) same (output near1 driver)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:40
S29	1	(controller near5 (digital adj filter)) same (output near1 driver)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:40
S30	4	(power near1 controller near5 (digital adj filter))	US-PGPUB; USPAT	OR	ON	2016/04/05 10:42
S31	4	(power near1 controller) near5 (digital adj filter)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:43
S32	16	(power near1 controller) same (digital adj filter)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:44
S33	0	controller same (digital adj filter) same (electronic adj ballast)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:46
S34	16	controller same (digital adj filter) and (electronic adj ballast)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:46
S35	2641	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same ((fault$1 or abnormal) adj condition)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:41
S36	6	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same ((fault$1 or abnormal) adj condition) same (power adj limit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:43
S37	1	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (fault$1 or abnormal) same (power adj limit adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:56
S38	2	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (power adj limit adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:56
S39	3540	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (power near1 controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/08/30 13:57

			DERWENT; IBM_TDB			
S40	135	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (fault$1 or abnormal) same (power near1 controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:57
S41	12	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) same (fault$1 or abnormal) same (power near1 controller) same protect$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:58
S42	2096	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) and (fault$1 or abnormal) and (power near1 controller) and protect$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 13:59
S43	6	((solid adj state adj light$3) or ssl.u/c. or (light adj emiting adj (didode or element)) or led.u/c.) and ((fault$1 or abnormal) adj condition) and (power adj limit adj controller) and protect$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/08/30 14:00

EAST Search History (Interference)

<This search history is empty>

8/ 31/ 2016 7:19:09 AM
C:\ Users\ vtan\ Documents\ EAST\ Workspaces\ 14893375.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In The Matter of United States Patent Application:

Applicant	:	**Lumastream Canada ULC**
Application No.	:	**14/893,375**
Filed	:	**June 25, 2014**
Title	:	**APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES**
TC/A.U.	:	**2844**
Examiner	:	**TAN, Vibol**
Docket No.	:	**K8001051WOUS**
Conf Number	:	**6653**
Date	:	**August 24, 2016**

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND RESPONSE TO OFFICE ACTION

A petition for a one-month extension of time is submitted herewith. In response to the Office Action of April 27, 2016, please amend the above-identified application as follows:

Amendments to the Specification begin on page **2** of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page **5** of this paper.

Amendments to the Drawings begin on page **9** of this paper and include attached replacement sheets.

Remarks/Arguments begin on page **10** of this paper.

Amendments to the Specification:

Please replace the fifth paragraph on page 6 (lines 25-30) with the following amended paragraph:

> In operation, the secondary controller 38 includes an averaging digital filter 1 which takes a set, such as 1024, of readings for current over a period of time and then calculates an average value and compares this value to a predetermined power limit. In one embodiment, the predetermined power limit may be set at about 97 watts. If the power level is at or exceeds the predetermined limit, the secondary controller 38 will assert one or more power limit options.

Please replace the second paragraph on page 8 (lines 3-7) with the following amended paragraph:

> With further reference to output current driver 20, the current source controller 48 is further connected to the current source 44 and current sense 46 via control lines 56 and 58 respectively and also connected to port 50 for programming and calibrating various parameters. As shown in Figure [[1]] 1a, the voltage sense 52 is connected in parallel with the LED load 14, however, in other embodiments, the voltage sense 52 may be omitted.

Please preplace the fifth paragraph on page 8 (lines 23-26) with the following amended paragraph:

> Furthermore, the power from the output bus 28 is transferred to the output current source 44 of the output current ~~divider~~ driver 20 via the power limit 18. The power monitor 30 senses current or power (via the current sense 36) delivered from the output bus 28 and transmits this current information to the secondary controller 38.

Please preplace the sixth paragraph on page 8 (lines 27-29) with the following amended paragraph:

> In further aspects of operation, the current source 44 provides a constant current output 2 to the LED load 14 while the current sense 46 provides a feedback signal to current source controller 48 to regulate the current supplied to the LED load 14. The output voltage

Please preplace the third paragraph on page 11 (lines 6-10) with the following amended paragraph:

> When the power from the output bus 28 is transferred to the output current source 44 of the output current ~~divider~~ driver 20 via the power limit 18, the power monitor 30 senses current (via the current sense 36) delivered from the output bus 28 and may also sense voltage (via the voltage sense 34) across the output bus 28 and transmits this current and/or voltage information to the secondary controller 38.

Please preplace the fourth paragraph on page 11 (lines 11-16) with the following amended paragraph:

> Turning to Figures 2a to 2d, schematic graphs illustrating various examples of LED power source operation when an operational fault condition occurs is shown. In the following graphs, the Y-axis relates to the power level being supplied to or used by the LED power source while the X-axis is a reflection [[on]] of elapsed time. In the current figures, the power level reflected on the Y-axis is the power transmitted from output bus 28 to the input of output current source 44 ~~by the current sense 36 and the voltage sense 34 (where appropriate)~~.

Please preplace the second paragraph on page 14 (lines 7-14) with the following amended paragraph:

As will be understood, the secondary controller 38 may limit the power from the output bus in other scenarios, such as, but not limited to transmitting a signal through a data line to the current source controller 48 to reduce the average output current either gradually or stepwise to the LED load 14 and a subsequent or stepwise increase in average current after a period of time. Alternatively, the secondary controller 38 may complete a sequence of tasks attempting to reduce the output power to the LED load first and ~~them~~ then if it is determined that the power level being supplied still exceeds beyond a predetermined power limit, as sensed by the power monitor 32, assert a shutdown of the power circuit 16.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) Apparatus for controlling power to a solid state lighting (SSL) device load comprising:

a power circuit for receiving power from an external source;

at least one power limit connected to the power circuit;

at least one output current driver for supplying a load power to the SSL device load, the at least one output current driver connected to the at least one power limit; and

a power limit controller;

wherein the power circuit transmits the power to the at least one power limit which, in turn, transmits a current to the at least one output current driver;

wherein the power limit controller directly or indirectly monitors a level of the load power and controls the at least one power limit to reduce the level of the load power for a predetermined period of time when the load power exceeds a predetermined power limit;

wherein if the load power exceeds the predetermined power limit, the power limit controller internally generates and transmits a signal to the current source controller to control the load power to the load;

wherein the signal is based on internal controls.

2.(Original) The apparatus of claim 1 wherein the at least one power limit is integrated within one of the at least one output current drivers.

3. (Original) The apparatus of claim 1 wherein the at least one power limit comprises:

the power limit controller;

a power monitor; and

a fault optocoupler,

wherein if the load power exceeds the predetermined power limit, the power limit controller transmits a signal to the fault optocoupler to control the load power.

4. (Original) The apparatus of claim 3 further comprising:

a power circuit controller;

wherein the fault optocoupler transmits a signal to the power circuit controller to control the power being supplied to the power limit.

5. (Original) The apparatus of claim 1 wherein the at least one output current driver comprises:

an output current source;

a current sense; and

a current source controller.

6. (Cancelled)

7. (Original) The apparatus of claim 1 wherein the power limit controller comprises a digital filter.

8. (Original) The apparatus of claim 7 wherein the power limit controller comprises at least one port.

9. (Original) The apparatus of claim 8 wherein the at least one port receives instructions to calibrate the at least one power limit to the predetermined power limit.

10. (Currently Amended) The apparatus of claim [[2]]3 wherein the power monitor comprises a current sense.

11. (Currently Amended) The apparatus of claim [[6]]1 wherein the at least one output current driver reduces the load power by a pulsing ~~apparatus~~technique.

12. (Currently Amended) A method of controlling power to a solid state lighting (SSL) device load comprising:

receiving an input power;

delivering load power to the SSL device load;

monitoring current level in load power;

~~limiting~~reducing load power to the SSL device for a predetermined period of time after a predetermined operational fault condition is met;

wherein if the load power exceeds a predetermined power limit, transmitting an internally generated signal to a current source controller to control the load power to the SSL load;

wherein the signal is based on internal controls.

13. (Currently Amended) The method of claim 12 wherein the predetermined operational fault condition is one of a ~~single~~ component failure, an external light emitting diode (LED) fault and an overload condition.

14. (Original) The method of claim 12 wherein monitoring current level in load power comprises:

sensing current delivered by an output bus to a power limit or sensing current delivered to a load by an output current driver.

15. (Original) The method of claim 12 further comprising:

gradually increasing load power to a normal operational power level.

16. (Original) The method of claim 15 wherein the load power is gradually increased at predetermined time intervals.

17. (Original) The method of claim 15 wherein the load power is gradually increased in predetermined power increments.

18. (Original) The method of claim 12 wherein if a maximum power threshold is met, load power delivered to the load is disabled.

19. (Currently Amended) The apparatus of claim 2 wherein the at least one power limit comprises:

the power limit controller;

a power monitor; and

a fault optocoupler,

wherein if the load power exceeds the predetermined power limit, the ~~power limit~~ current source controller transmits a signal to the fault optocoupler to control the load power.

20.(Currently Amended) The apparatus of claim [[6]]1 wherein the at least one output current driver reduces load power by a constant current ~~apparatus~~reduction technique.

21. (Original) The apparatus of claim 1 wherein the SSL device load is one of an organic light emitting diode (OLED) load, a light emitting diode (LED) load or a LED array load.

Amendments to the Drawings:

The attached sheets of drawings includes changes to Figs. 1a, 1b, 4a and 4b. These sheet replace the original sheets including Figs. 1a, 1b, 4a and 4b.

Attachment: Replacement Sheets (4)

REMARKS/ARGUMENTS

Claims 1 to 5 and 7 to 21 remain in the current application. Claims 1, 10 to 13, 19 and 20 have been amended and Claim 6 cancelled.

Portions of the specification have been amended to correct typographical errors and to clarify the teachings of the specification.

The drawings have been objected to as not complying with 37 CFR 1.83(a). The Examiner has stated that the features of the power limit controller, the digital filter, the constant current apparatus and the pulsing apparatus must be shown in the figures.

Applicant has amended Figures 1a, 1b, 4a and 4b to replace the term "secondary controller" with the term "power limit controller" with respect to the item associated with reference number 38. Support for this amendment can be found in at least paragraph 30 of the published application which states "The power limit **18** includes a power monitor **32** (having a current sense **36**), a secondary, or power limit, controller **38**…..". Figures 1a, 1b, 4a and 4b have also been amended to include a digital filter **1** within the secondary, or power limit, controller **38**. Support for this amendment can be found in at least paragraph 33 of the published application which states "In operation, the secondary controller **38** includes an averaging digital filter". Paragraph 33 has also been amended to include the reference number "1" for the digital filter. With respect to the constant current apparatus, Claim 20 has been amended to replace the word "apparatus" with the word "reduction technique". Support for this amendment can be found in at least paragraphs 43, 44, 48 and 81 of the published application. Reference number "2" has been added to Figures 1a, 1b, 4a, 4b and paragraph 43 reflecting the constant current output.

With respect to the pulsing apparatus, Claim 11 has been amended to claim the load power being reduced by a pulsing technique. It is respectfully submitted that support for this amendment can be found in at least paragraph 44 of the published application. In paragraph 44, the specification states "The current source controller 48 regulates the output current provided to the LED load 14 and also provides apparatus for reducing the average current to

the LED load 14 via a gate pulse signal with a variable duty cycle through control line 56". Applicant respectfully submits that it can be seen that a pulsing technique is being used to reduce the average current to the LED load 14. Further support can be found in paragraph 48 which states "If an operational fault condition such as an over power event occurs, the current source controller 48 may reduce the average current (or power) to the LED load 14 by a dimming pulse including a variable duty cycle through control line 56 to the current source 44". In other words, a pulsing technique is being used to reduce the load power. Retraction of Examiner's objection to the drawings is respectfully requested.

Claims 1, 3, 4, 6 to 8, 11 and 19 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112(pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which is regarded as the invention. More specifically, the Examiner has suggested that the term "the power limit controller" is not supported by the specification. Applicant respectfully disagrees. Along with its mention on page 2 (as stated by the Examiner), the term "power limit controller" is also included in paragraph 30 of the published application as outlined above. As can be seen, the power limit controller may also be seen as the secondary controller. Applicant respectfully submits that the function of the power limit controller is fully supported by the specification when one looks at the description.

With respect to the pulsing apparatus, Claim 11 has been amended as outlined above. Claim 10 has been amended to correct its claim dependency from Claim 2 to Claim 3. Retraction of Examiner's rejection of Claims 1, 3, 4, 6 to 8, 11 and 19 is respectfully requested.

Claims 1, 2, 5, 6, 12 to 18 and 21 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by US Patent Publication No. 2011/0204820 to Tikkanen et al. ("Tikkanen"). The independent claims have been amended to include the subject matter of "wherein if the load power exceeds the predetermined power limit, the power limit controller internally generates and transmits a signal to the current source controller to control the load power to the load" and "wherein the signal is based on internal controls." Support for this amendment can be found in at least paragraph 36 of the published application.

In paragraph 36, the specification discloses various power limit options which may be performed if power limiting is required. As discussed in the specification, the system may transmit a change in light intensity command (in the form of control information) when power limiting is required. As such, control information is translated into on-time and off-time information and transmitted as a gate pulse to reduce the average output current when power limiting is required. As can be seen in Figures 1a, 1bv, 4a and 4b, there is no external transmitter connected to the system. In this manner, it will be understood that any power limiting signals are generated internally based on internal determinations. As discussed in paragraph 37, a shutdown command may be transmitted from the power limit controller over command line 43 to the fault optocoupler to disable the power circuit. Again, it can be seen that the signal is generated internally before being transmitted by the power limit controller based. The internal signal is generated based on signals from the internal power monitor within the system.

In Tikkanen, inputs are received by the secondary controller, which controls the power limit, from an external transmitter 76 (paragraph 35). These inputs include dimming or color mixing information in the form of a serial data stream (paragraph 51). Control of the claimed invention is via an internally generated signal. For at least these reasons, it is respectfully submitted that the independent claims are patentable over the cited art. Retraction of Examiner's rejection of Claims 1, 2, 5, 6, 12 to 18 and 21 is respectfully requested.

Claims 7 to 9 have been rejected under 35 U.S.C. 103 as being unpatentable over Tikkanen in view of US Patent No. 9,024,541 to Xie et al. ("Xie"). Notwithstanding the fact that Xie is not citable in the current application, it is respectfully submitted that Xie is silent with respect to the subject matter lacking in Tikkanen to obviate the independent claims. Retraction of Examiner's rejection of Claims 7 to 9 is respectfully requested.

For the above reasons, it is respectfully submitted that the application is now in condition for allowance, which is requested. If there are any outstanding issues, the Examiner is invited to contact the undersigned to discuss this matter further.

The Commissioner is hereby authorized to charge any additional fees, and credit any payments, to Deposit Account No. 501613, in the name of Gowling WLG (Canada) LLP.

Respectfully submitted,

By: /Jeffrey W. Wong/

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Electronic Patent Application Fee Transmittal

Application Number:	14893375
Filing Date:	23-Nov-2015
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Filer:	Jeffrey Wong/Christopher Kreider
Attorney Docket Number:	K8001051WOUS

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
			Total in USD ($)	**200**

Electronic Acknowledgement Receipt

EFS ID:	26735147
Application Number:	14893375
International Application Number:	
Confirmation Number:	6653
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001051WOUS
Receipt Date:	24-AUG-2016
Filing Date:	23-NOV-2015
Time Stamp:	14:36:30
Application Type:	U.S. National Stage under 35 USC 371

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Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$200
RAM confirmation Number	082516INTEFSW00000900501613
Deposit Account	501613
Authorized User	Jeffrey Wong

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	K8001051WOUS-EOT.pdf	238516 51a34c46871e541d4b7db1101c827b5b3cdfb1b4	no	1
Warnings:					
Information:					
2	Drawings-only black and white line drawings	K8001051WOUS-Drawings.pdf	303922 471bf247eec49c3c523e38c7ceba88262b3e1e26	no	4
Warnings:					
Information:					
3		K8001051WOUS-Response.pdf	121174 5a45dd4f4ccd461d6be53dac35ab7b606b754f9b	yes	13

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Specification	2	4
Claims	5	8
Drawings-only black and white line drawings	9	9
Applicant Arguments/Remarks Made in an Amendment	10	13

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30938 c2ccc3d8d0057b567a67618c30231d217ca3cc42	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	694550

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/22 (03-13)
Approved for use through 7/31/2016. OMB 0651-0031
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): K8001051WOUS

Application Number: 14/893,375

Filed: 2015-11-23

For: APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

Art Unit: 2844

Examiner: TAN, Vibol

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☑ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$ 200
☐ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☐ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number _____.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 46414.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Jeffrey W. Wong/ — Signature

2016-08-24 — Date

Jeffrey W. Wong — Typed or printed name

519-575-7543 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

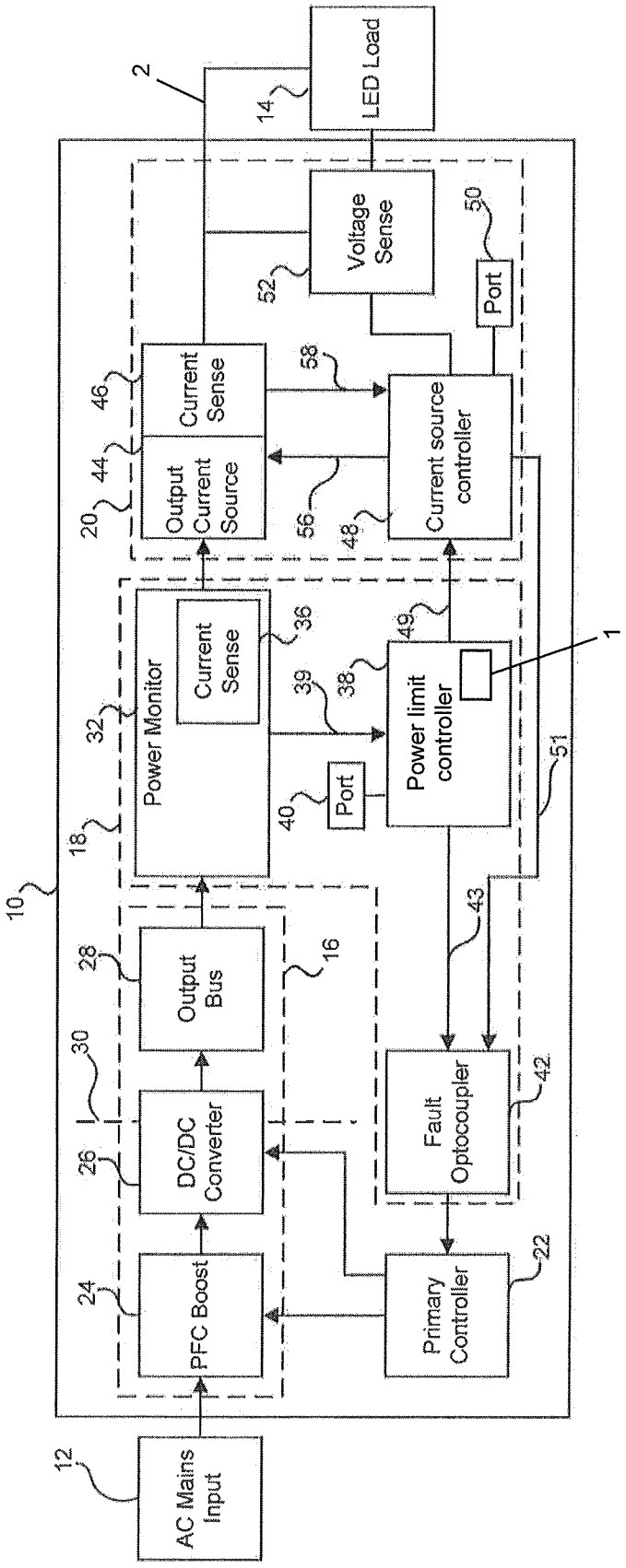

LED Load
14
2
Voltage Sense
52
Port
50
Current Sense
46
Output Current Source
44
20
58
56
48
Current source controller
Power Monitor
32
Current Sense
36
39
38
49
Power limit controller
1
Port
40
18
51
10
Output Bus
28
16
43
30
DC/DC Converter
26
Fault Optocoupler
42
PFC Boost
24
Primary Controller
22
AC Mains Input
12

FIGURE 1a

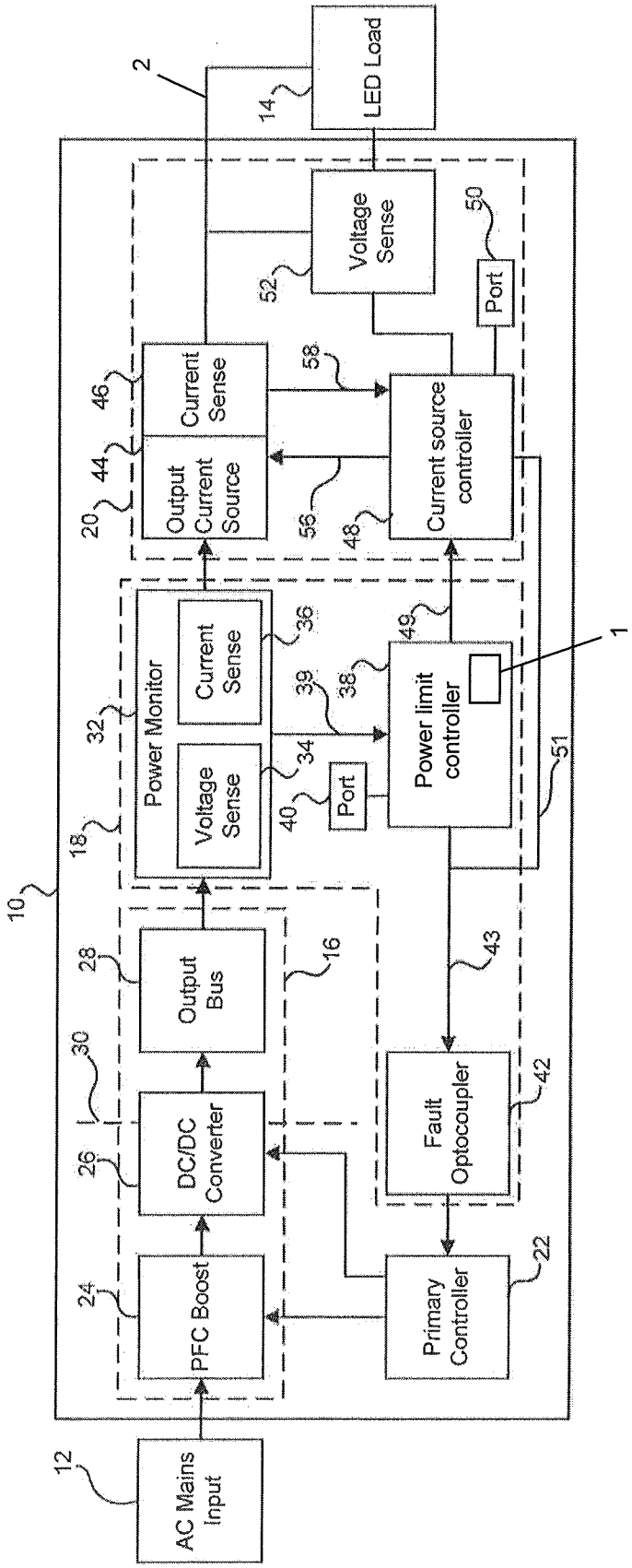

LED Load
14
2
Voltage Sense
52
Port
50
Current Sense
46
Output Current Source
44
20
58
56
48
Current source controller
Power Monitor
32
Current Sense
36
Voltage Sense
34
39
38
40
Port
Power limit controller
49
1
51
18
10
Output Bus
28
16
30
DC/DC Converter
26
43
Fault Optocoupler
42
PFC Boost
24
Primary Controller
22
12
AC Mains Input

FIGURE 1b

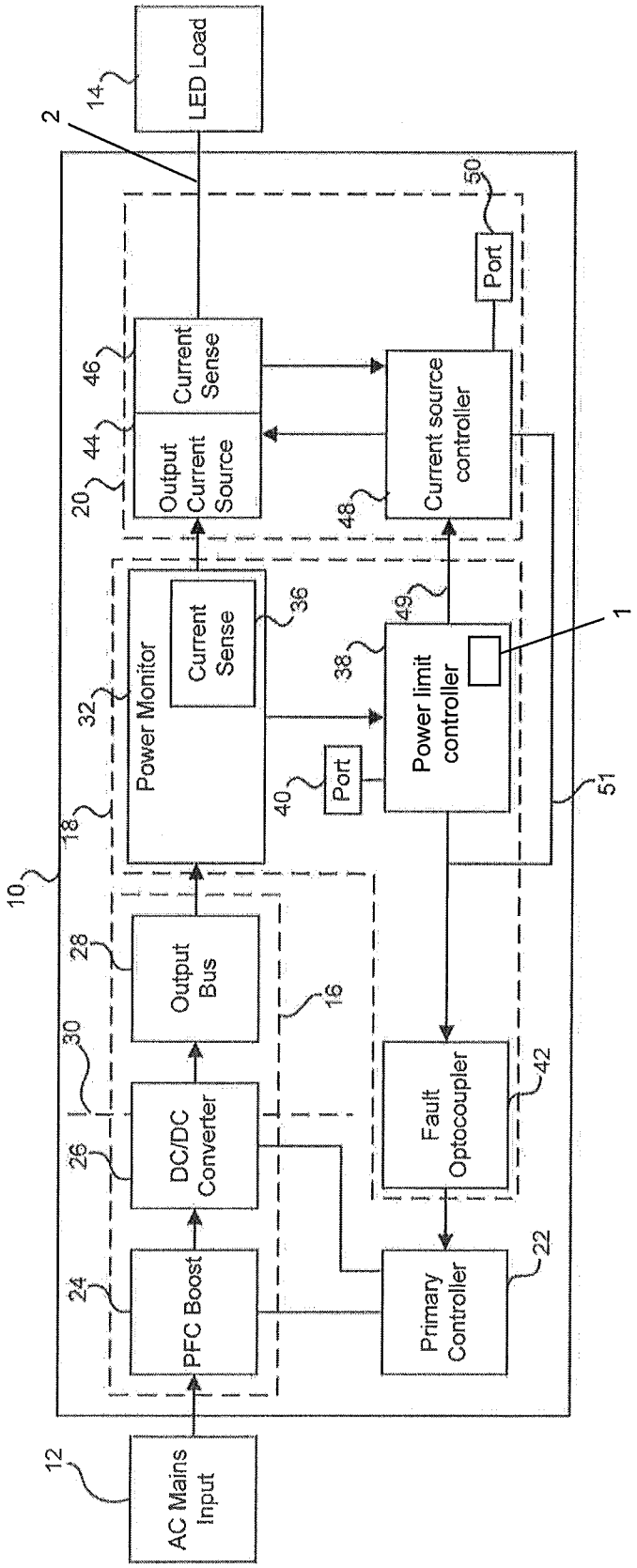

LED Load
14
2
50
Port
46
Current Sense
44
Output Current Source
20
48
Current source controller
Power Monitor
32
Current Sense
36
49
38
Power limit controller
1
40
Port
51
18
10
28
Output Bus
16
30
26
DC/DC Converter
Fault Optocoupler
42
24
PFC Boost
Primary Controller
22
12
AC Mains Input

FIGURE 4a

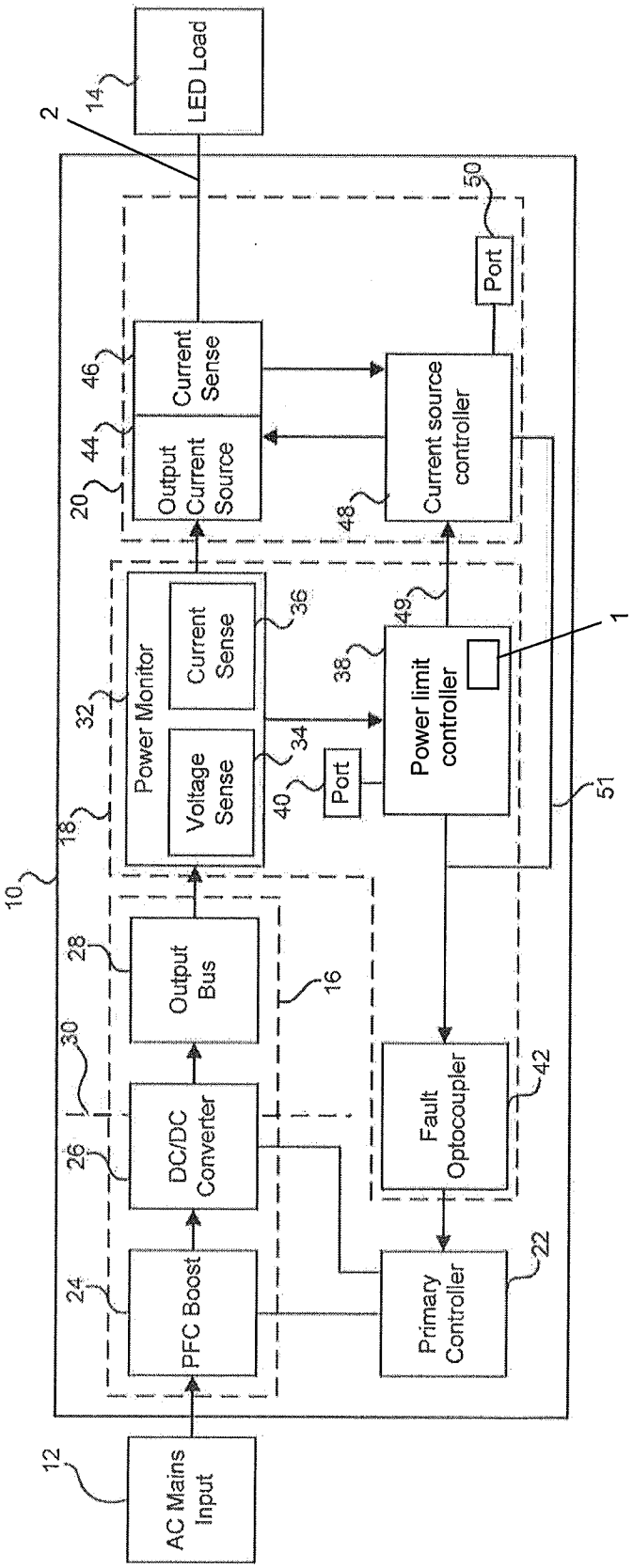

LED Load
14
2
Port
50
Current Sense
46
Output Current Source
44
20
Current source controller
48
Power Monitor
32
Current Sense
36
Voltage Sense
34
40
Port
Power limit controller
38
49
1
51
18
10
Output Bus
28
16
30
DC/DC Converter
26
Fault Optocoupler
42
PFC Boost
24
Primary Controller
22
AC Mains Input
12

FIGURE 4b

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
14/893,375	11/23/2015	

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	**280**
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	**280**

APPLICATION AS AMENDED – PART II

AMENDMENT **08/24/2016**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 16	Minus	** 21	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**0**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
GWENDOLYN MYERS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/893,375	11/23/2015	David TIKKANEN	K8001051WOUS

CONFIRMATION NO. 6653

34236
Gowling WLG (Canada) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

PUBLICATION NOTICE

OC00000082699621

Title:APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

Publication No.US-2016-0128144-A1
Publication Date:05/05/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/893,375	11/23/2015	David TIKKANEN	K8001051WOUS	6653

34236 7590 04/27/2016

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P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2844	

NOTIFICATION DATE	DELIVERY MODE
04/27/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

VAL.COTTRILL@GOWLINGWLG.COM
Waterloo.IP@gowlingwlg.com
JEFF.WONG@GOWLINGWLG.COM

Office Action Summary	Application No. 14/893,375	Applicant(s) TIKKANEN ET AL.	
	Examiner Vibol Tan	Art Unit 2844	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/23/15*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-21* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-21* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *11/23/15* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *2/24/16*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the power limit controller, the digital filter, the constant current apparatus, and the pulsing apparatus must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 3, 4, 6-8, 11, and 19 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

In claims 1, 3, 4, 6-8, and 19, it is unclear what part of the circuit in the drawings is the claimed “power limit controller” that is used to directly or indirectly monitor a level of the load power and controls the at least one power limit to reduce the level of the load power for a predetermined period of time when the load power exceeds a predetermined power limit. The “power limit controller" is recited in summary of the disclosure in page 2, lines 28 and 30; but not in the detailed description of the specification that would be sufficient to provide clear support for what being claimed.

In claim 11, it is not understood what being referred to as the pulsing apparatus because there is no support in the specification.

5. Claim 10 recites the limitation "the power monitor" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

7. Claims 1, 2, 5, 6, 12-18 and 21 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Tikkanen et al. (US 2011/0204820).

In claim 1, Tikkanen teaches all claimed features in Fig. 3, apparatus for controlling power to a solid state lighting (SSL) device load comprising:

a power circuit (47) for receiving power from an external source (42);

at least one power limit (50) connected to the power circuit (47);

at least one output current driver (52) for supplying a load power to the SSL device load (56), the at least one output current driver connected to the at least one power limit; and

a power limit controller (64);

wherein the power circuit (47) transmits the power to the at least one power limit which, in turn, transmits a current to the at least one output current driver (52);

wherein the power limit controller (64) directly or indirectly monitors ([0045]; monitored by controller 64) a level of the load power and controls the at least one power limit to reduce (the power limit circuits 50 limit the energy to the loads in accordance with the UL standard 1310 Class 2; [0045]) the level of the load power for a predetermined period of time when the load power exceeds a predetermined power limit (operating voltage).

In claim 2, Tikkanen further teaches the apparatus of Claim 1 wherein the at least one power limit (50) is integrated within one of the at least one output current drivers (52).

In claim 5, Tikkanen further teaches the apparatus of Claim 1 wherein the at least one output current driver (52 in Fig. 6) comprises:

an output current source (92);

a current sense (94); and

a current source controller (90).

In claim 6, Tikkanen further teaches the apparatus of Claim 5 wherein if the load power exceeds the predetermined power limit, the power limit controller (64) transmits a signal to the current source controller (90) to control the load power to the load (56).

In claim 12, Tikkanen teaches all claimed features in Fig. 3, a method of controlling power to a solid state lighting (SSL) device load (56) comprising:

receiving an input power (from 42);

delivering load power (by 50) to the SSL device load;

monitoring current level (monitored by controller 64) in load power;

limiting load power (the power limit circuits 50 limit the energy to the loads in accordance with the UL standard 1310 Class 2; [0045]) to the SSL device for a predetermined period of time after a predetermined operational fault condition (caused by component failure) is met.

In claim 13, Tikkanen further teaches the method of Claim 12 wherein the predetermined operational fault condition is one of a single component failure ([0045]; In the event of a single component failure within the output current driver module, the power limit circuits 50 limit the energy to the loads in accordance with the UL standard 1310 Class 2), an external light emitting diode (LED) fault and an overload condition.

In claim 14, Tikkanen further teaches the method of Claim 12 wherein monitoring current level in load power comprises: sensing current (92 in Fig. 6) delivered by an output bus (48 in Fig. 3) to a power limit (50) or sensing current delivered to a load by an output current driver.

In claim 15, Tikkanen further teaches the method of Claim 12 further comprising: gradually increasing load power to a normal operational power level (inherent).

In claim 16, Tikkanen further teaches the method of Claim 15 wherein the load power is gradually increased at predetermined time intervals (inherent).

In claim 17, Tikkanen further teaches the method of Claim 15 wherein the load power is gradually increased in predetermined power increments (inherent).

In claim 18, Tikkanen further teaches the method of Claim 12 wherein if a maximum power threshold is met, load power delivered to the load is disabled (inherent).

Claim 20 is rejected in the same manner as claim 6.

In claim 21, Tikkanen further teaches the apparatus of Claim 1 wherein the SSL device load (56) is one of an organic light emitting diode (OLED) load, a light emitting diode (LED) load or a LED array load.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 7-9 are rejected under 35 U.S.C. 103 as being unpatentable over Tikkanen et al. in view of Xie et al. (U.S. Pat. 9,024,541).

In claim 7, Tikkanen teaches the apparatus of Claim 1; with the exception of teaching wherein the power limit controller comprises a digital filter. However, in the same field of endeavor, Xie teaches in col. 5, line 49, the controller 202 includes a digital filter (not shown).

Therefore; it would have been obvious to one ordinary skill in the art before the effective filing date of the claimed invention to combine the teachings wherein the controller includes a digital filter in order to process the multiple resonant periods to obtain a single estimation of the resonant period, such as by averaging the multiple resonant periods to obtain an average resonant period.

In claim 8, Tikkanen further teaches the apparatus of Claim 7 wherein the power limit controller (64) comprises at least one port (68).

In claim 9, Tikkanen further teaches the apparatus of Claim 8 wherein the at least one port (68) receives instructions to calibrate ([0079]) the at least one power limit to the predetermined power limit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alex Taningco can be reached on (571) 272-8048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2844

Notice of References Cited	Application/Control No. 14/893,375	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.	
	Examiner Vibol Tan	Art Unit 2844	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2011/0204820 A1	08-2011	Tikkanen; David	H05B33/0815	315/294
*	B	US-8,299,987 B2	10-2012	Neudorf; Jason	H05B33/0818	315/169.3
*	C	US-8,975,825 B2	03-2015	Hu; Yuequan	H05B33/0854	315/239
*	D	US-8,638,045 B2	01-2014	Kunst; David	H05B33/0815	315/185S
*	E	US-8,957,601 B2	02-2015	Tikkanen; David	H05B33/0803	315/294
*	F	US-9,049,759 B2	06-2015	Tikkanen; David	H05B33/0815	1/1
*	G	US-8,525,446 B2	09-2013	Tikkanen; David	H05B33/0815	315/291
*	H	US-9,024,541 B2	05-2015	Xie; Yanhui	H02M3/33507	315/224
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

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Receipt date: 02/24/2016

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14893375
Filing Date	2015-11-23
First Named Inventor	TIKKANEN, David
Art Unit	2844
Examiner Name	V.Tan
Attorney Docket Number	K8001051WOUS

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/V.T./	1	2273324	CA		1998-04-30	NCON CORPORATION PTY LIMITED		
/V.T./	2	2742843	CA		2010-05-27	GENERAL ELECTRIC COMPANY		
/V.T./	3	2761294	CA		2010-11-18	ILUMISYS, INC.		

Receipt date: 02/24/2016

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/V.T./	1	CANADIAN INTELLECTUAL PROPERTY OFFICE AS INTERNATIONAL SEARCHING AUTHORITY, International Search Report and Written Opinion for International Patent App. No. PCT/CA2014/050609, 2014-10-07	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	326	(("2014205575") or ("2913239") or ("8957601") or ("9049759") or ("20120280637") or ("20130300312") or ("20150108912") or ("20150115839") or ("8525446") or ("9078310") or ("2010031169") or ("20110204820") or ("2734757") or ("2734757") or ("9013114") or ("20130214697") or ("2627155") or ("20080303456") or ("7626342") or ("102640570") or ("2008154069") or ("102754525") or ("2499220") or ("2013510388") or ("102577606") or ("102577606") or ("2497339") or ("2011055284") or ("2013509683") or ("20120223650") or ("102132628") or ("102132628") or ("8432108") or ("102573210") or ("102573210") or ("2491764") or ("2013072784") or ("20100117545") or ("2011049703") or ("2752089") or ("20140285103") or ("9301347") or ("5102257") or ("102598870") or ("20130038234") or ("2564668") or ("2011135505") or ("2014116100") or ("20140252992") or ("2749130") or ("2013054297") or ("2777512") or ("103918349") or ("2777512") or ("2013524472") or ("2014532274") or ("2014535146") or ("103947289") or ("6191568") or ("2014200450") or ("2010308455") or ("2259055") or ("2484179") or ("2010308455") or ("20120274216") or ("20160029446") or ("101686591") or ("2494852") or ("5773394") or ("20100045210") or ("2011051859")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/03/31 17:20
S2	7	(("8299987") or ("20130049634")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/04/01 14:30
S3	20411	(power adj converter) same controller same (abnormal or fault or (over adj threshold or current or power or voltage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:36
S4	1435	(power adj converter) same controller same (abnormal or fault or ((over or	US-PGPUB; USPAT;	OR	ON	2016/04/01 14:38

		exceed$3) adj (threshold or current or power or voltage)))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S5	70	(power adj converter) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:40
S6	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (power adj limit$4) same driver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:50
S7	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (power adj limit$4) same driv$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:50
S8	0	(power adj (converter or circuit$2)) same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:52
S9	1	(power adj (converter or circuit$2)) same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:53
S10	6	controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (output adj driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 14:53
S11	379	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 15:03
S12	0	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2016/04/01 15:03

		(diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (power adj limit$4)	EPO; JPO; DERWENT; IBM_TDB			
S13	39	converter same controller same (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) same ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) same (dim or dimmer or dimming)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/01 15:09
S14	43534	(H05B33/0815 H05B33/0818 H05B33/0827 H05B37/02 H05B37/029 H05B39/04 H05B41/36 H05B33/089 H05B33/0896).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:00
S15	4189	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:01
S16	3650	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:14
S17	2090	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and converter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:15
S18	558	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:15
S19	555	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2016/04/04 12:16
S20	59	S14 and (abnormal or fault or ((over or exceed$3) adj (threshold or current or power or voltage))) and ((light adj emitting adj (diode or element) or led.u/c.) or (solid adj state adj lighting) or ssl.u/c.) and (power adj converter) and (output near1 driver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/04 12:17
S21	9	lumastream adj canada adj ulc.as.	US-PGPUB; USPAT	OR	ON	2016/04/04 14:27

S22	0	("20110204820").PN.	USPAT	OR	OFF	2016/04/04 14:37
S23	1	("20110204820").PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 14:37
S24	2	(("20110204820") or ("8525446")).PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 14:59
S25	1	("20070103086").PN.	US-PGPUB; USPAT	OR	OFF	2016/04/04 15:05
S26	2776	controller same (digital adj filter)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:39
S27	762	controller near5 (digital adj filter)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:39
S28	0	(controller near5 (digital adj filter)) same (output near1 driver)	US-PGPUB; USPAT	OR	OFF	2016/04/05 10:40
S29	1	(controller near5 (digital adj filter)) same (output near1 driver)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:40
S30	4	(power near1 controller near5 (digital adj filter))	US-PGPUB; USPAT	OR	ON	2016/04/05 10:42
S31	4	(power near1 controller) near5 (digital adj filter)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:43
S32	16	(power near1 controller) same (digital adj filter)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:44
S33	0	controller same (digital adj filter) same (electronic adj ballast)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:46
S34	16	controller same (digital adj filter) and (electronic adj ballast)	US-PGPUB; USPAT	OR	ON	2016/04/05 10:46

EAST Search History (Interference)

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4/5/2016 3:10:59 PM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14893375	TIKKANEN ET AL.
	Examiner	Art Unit
	VIBOL TAN	2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B33/0815 H05B33/0818 H05B33/0827 H05B37/02 H05B37/029 H05B39/04 H05B41/36 H05B33/089 H05B33/0896 and text	4/4/2016	VTan

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
pct/ca2014/050609	4/4/2016	VTan
EAST text search	4/4/2016	VTan

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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Application Number	14893375
Filing Date	2015-11-23
First Named Inventor	TIKKANEN, David
Art Unit	
Examiner Name	
Attorney Docket Number	K8001051WOUS

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	1	2273324	CA		1998-04-30	NCON CORPORATION PTY LIMITED		
	2	2742843	CA		2010-05-27	GENERAL ELECTRIC COMPANY		
	3	2761294	CA		2010-11-18	ILUMISYS, INC.		

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	Art Unit	
	Examiner Name	
	Attorney Docket Number	K8001051WOUS

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	1	CANADIAN INTELLECTUAL PROPERTY OFFICE AS INTERNATIONAL SEARCHING AUTHORITY, International Search Report and Written Opinion for International Patent App. No. PCT/CA2014/050609, 2014-10-07	
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Art Unit	
Examiner Name	
Attorney Docket Number	K8001051WOUS

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2016-02-24
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PAT78496W-90	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below
International application No. **PCT/CA2014/050609**	International filing date *(day/month/year)* 25 June 2014 (25-06-2014)	(Earliest)Priority date *(day/month/year)* 25 June 2013 (25-06-2013)
Applicant LUMASTREAM CANADA ULC		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☑ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of:

   ☑ the international application in the language in which it was filed.

   ☐ a translation of the international application into which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

   ☑ the text is approved as submitted by the applicant.

   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

   ☑ the text is approved as submitted by the applicant.

   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may,within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

   a. the figure of the **drawings** to be published with the abstract is Figure No. 1a

   ☑ as suggested by the applicant.

   ☐ as selected by this Authority, because the applicant failed to suggest a figure.

   ☐ as selected by this Authority, because this figure better characterizes the invention.

   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2014/050609

A. CLASSIFICATION OF SUBJECT MATTER
IPC: ***H05B 37/02*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC *H05B* (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Canadian Patent Database and TotalPatent. Terms used: led, light, power, limit, exceed, threshold and others.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CA 2,273,324 A1, 30 April 1998 (30-04-1998) Figure 1; pages 1-5; claim 1	1, 12
A	CA 2,742,843 A1, 27 May 2010 (27-05-2010) abstract and figures	1, 12
A	CA 2,761,294 A1, 18 November 2010 (18-11-2010) whole document	1, 12

☐ Further documents are listed in the continuation of Box C.

☑ See patent family annex.

*	Special categories of cited documents:
"A"	document defining the general state of the art which is not considered to be of particular relevance
"E"	earlier application or patent but published on or after the international filing date
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O"	document referring to an oral disclosure, use, exhibition or other means
"P"	document published prior to the international filing date but later than the priority date claimed
"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&"	document member of the same patent family

Date of the actual completion of the international search 3 October 2014 (03-10-2014)	Date of mailing of the international search report 06 October 2014 (06-10-2014)
Name and mailing address of the ISA/CA Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	Authorized officer Andrew O'Malley (819) 953-5481

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2014/050609

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
CA2273324A1	30 April 1998 (30-04-1998)	CA2273324A1	30 April 1998 (30-04-1998)
		CA2273324C	29 March 2005 (29-03-2005)
		AT477703T	15 August 2010 (15-08-2010)
		AU7267096A	15 May 1998 (15-05-1998)
		AU744659B2	28 February 2002 (28-02-2002)
		BR9612783A	18 April 2000 (18-04-2000)
		CN1242136A	19 January 2000 (19-01-2000)
		CN1162055C	11 August 2004 (11-08-2004)
		DE69638232D1	23 September 2010 (23-09-2010)
		EP0934682A1	11 August 1999 (11-08-1999)
		EP0934682A4	02 February 2005 (02-02-2005)
		EP0934682B1	11 August 2010 (11-08-2010)
		ES2352644T3	22 February 2011 (22-02-2011)
		JP2001508228A	19 June 2001 (19-06-2001)
		JP3872820B2	24 January 2007 (24-01-2007)
		KR20000052799A	25 August 2000 (25-08-2000)
		KR100461504B1	13 December 2004 (13-12-2004)
		US6188182B1	13 February 2001 (13-02-2001)
		WO9818296A1	30 April 1998 (30-04-1998)
CA2742843A1	27 May 2010 (27-05-2010)	CA2742843A1	27 May 2010 (27-05-2010)
		CA2742843C	11 June 2013 (11-06-2013)
		CN102217418A	12 October 2011 (12-10-2011)
		CN102217418B	10 July 2013 (10-07-2013)
		EP2359666A1	24 August 2011 (24-08-2011)
		EP2359666B1	08 January 2014 (08-01-2014)
		JP2012509556A	19 April 2012 (19-04-2012)
		MX2011005204A	01 June 2011 (01-06-2011)
		US2010123404A1	20 May 2010 (20-05-2010)
		US7944155B2	17 May 2011 (17-05-2011)
		WO2010059411A1	27 May 2010 (27-05-2010)
CA2761294A1	18 Nov. 2010 (18-11-2010)	CA2761294A1	18 November 2010 (18-11-2010)
		EP2430888A2	21 March 2012 (21-03-2012)
		US2010289418A1	18 November 2010 (18-11-2010)
		US8330381B2	11 December 2012 (11-12-2012)
		US2013088162A1	11 April 2013 (11-04-2013)
		WO2010132625A2	18 November 2010 (18-11-2010)
		WO2010132625A3	24 February 2011 (24-02-2011)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
BORDEN LADNER GERVAIS LLP
World Exchange Plaza
100 Queen Street, Suite 1300
OTTAWA, Ontario
Canada, K1P 1J9

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	6 October 2014 (06-10-2014)
Applicant's or agent's file reference PAT78496W-90	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA2014/050609	25 June 2014 (25-06-2014)	25 June 2013 (25-06-2013)

International Patent Classification (IPC) or both national classification and IPC
IPC: ***H05B 37/02*** (2006.01)

Applicant
LUMASTREAM CANADA ULC

1. This opinion contains indications relating to the following items:

- ☑ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☑ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/CA	Date of completion of this opinion	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	03 October 2014 (03-10-2014)	Andrew O'Malley (819) 953-5481

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CA2014/050609

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

☑ the international application in the language in which it was filed.

☐ a translation of the international application into which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

a. (means)

☐ on paper

☐ in electronic form

b. (time)

☐ in the international application as filed.

☐ together with the international application in electronic form

☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-21	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-21	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-21	YES
	Claims	NONE	NO

2. Citations and explanations:

Reference is made to the following documents cited in the International Search Report:

D1: CA 2,273,324 A1, 30 April 1998 (30-04-1998)
D2: CA 2,742,843 A1, 27 May 2010 (27-05-2010)

These documents constitute the closest available prior art to the present application, directed to an apparatus and method for controlling power to a solid state lighting device, which employs power monitoring and limiting means placed between the input power circuit and output current source of the lighting device. The power monitoring and limiting means reduces the power to the light load for a predetermined amount of time if the load power exceeds a predetermined power level.

Article 33(2) PCT – Novelty

Since the subject matter defined by claims 1-21 is not disclosed by any single document from the available prior art, these claims meet the requirements of Article 33(2) PCT with respect to novelty.

Article 33(3) PCT – Inventive step

Regarding independent claim 1, D1 discloses an apparatus for controlling power to a lighting load (figure 1) comprising:
- a power circuit (8) for receiving power from an external source (4);
- a power limit/control (16) connected to the power circuit;
- a power limit controller (10);

wherein the power limit controller monitors the level of load power (via 14) and controls the level of power to the load.

Although D1 does not explicitly teach a specific current driver for the load, per claim 1, it is interpreted that the power circuit (8) performs a similar function of delivering power to the load (see page 4, line25 tot page 6, line 10).

However, where the apparatus of D1 is directed to limiting the power to the load in response to the load power exceeding a predetermined limit, the power reduction arrangement of D1 is used for power savings (see page 1, lines 6 to 17).

While D2 is directed to providing output current regulation to LED loads when the detected load power exceeds a predetermined threshold, D2 is directed to a specific multi-channel LED arrangement and circuit arrangement (see abstract and figures).

Accordingly, the subject matter defined by independent claim 1, and by association, dependent claims 2-11, appears to include an inventive step above the available prior art. This applies similarly to the method defined by claims 12-21.

Claims 1-21 thereby comply with Article 33(3) PCT.

Continued on Supplemental Sheet . . .

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**

Continuation of: Box V

Article 33(4) PCT – Industrial applicability

Since the subject matter defined by claims 1 to 21 is directed to well established lighting arts, these claims satisfy Article 33(4) PCT.

Office de la Propriété Intellectuelle du Canada
Un organisme d'Industrie Canada

Canadian Intellectual Property Office
An agency of Industry Canada

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(12) BREVET CANADIEN
CANADIAN PATENT

(13) C

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(87) Date publication PCT/PCT Publication Date: 1998/04/30
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(85) Entrée phase nationale/National Entry: 1999/05/20
(86) N° demande PCT/PCT Application No.: AU 1996/000670
(87) N° publication PCT/PCT Publication No.: 1998/018296

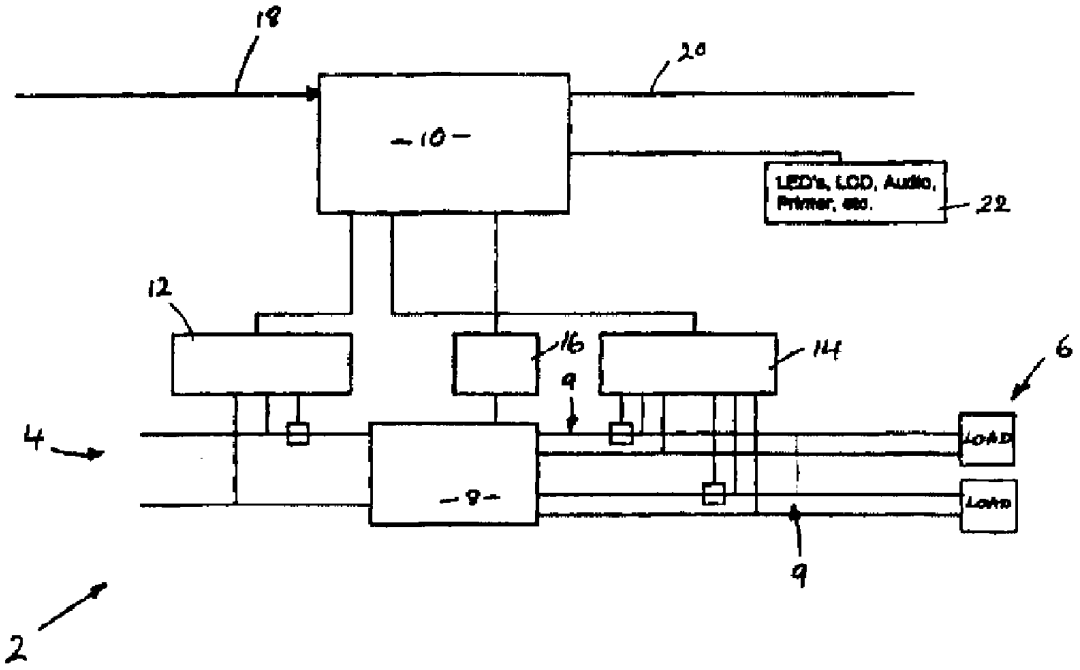
(51) Cl.Int.^{6}/Int.Cl.^{6} H05B 37/02, G05F 1/66, H05B 39/02

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(74) Agent: MOFFAT & CO.

(54) Titre : APPAREIL DE COMMANDE DE PUISSANCE POUR SYSTEMES D'ECLAIRAGE
(54) Title: A POWER CONTROL APPARATUS FOR LIGHTING SYSTEMS



(57) Abrégé/Abstract:
A power control apparatus, particularly for lighting systems such as fluorescent lights. A power variation circuit (16) is provided coupled between a main electrical input power source and at least one power output to a load (6) such as a lighting system. The power variation device is controllable to vary the power level supplied to the load according to control signals from a digital processing circuit (10). Monitoring circuitry (12, 14) is coupled to the digital processing circuit (10) to provide monitoring signals relating to electrical parameters of the input power source (4) and/or the at least one power output (9). The digital processing circuit (10) is responsive to a condition of the monitoring signals to control the power variation circuit (16) to supply the power output (9) at a first predetermined level for a predetermined time period and thereafter to reduce power output to a second predetermined level. The second predetermined level and the predetermined time period are set by the digital processing means according to control parameters stored in a first memory. The stored control parameters may include indications of predetermined times of day and/or days of week and corresponding values for the second predetermined level, wherein the digital processing circuit (10) is responsive to a timer at the predetermined times of day and/or days of week to change the second predetermined level to the corresponding value stored in the memory.

A POWER CONTROL APPARATUS FOR LIGHTING SYSTEMS

This invention relates to a power control apparatus which is particularly useful for lighting systems, such as those employing fluorescent lights.

Studies have shown that many buildings, for example, tend to be over illuminated by present lighting systems for the purposes required of them. Over illumination in this way results in a wastage of electrical power. Most often fluorescent lights are used in lighting systems for large buildings, for example, in view of their increased efficiency as compared to many other lights. Also, the relationship between light output and power required in a fluorescent light is non-linear, and it has been found that a significant decrease in power usage by fluorescent lights can be achieved without a correspondingly noticeable change in light output in many instances. However, if reduced power is continuously supplied to a fluorescent lighting system, the lights may experience starting difficulties, such as increased flickering time, which can reduce the life span of the lights. Furthermore, it may be desired to adjust the light level output of the lights, and in a large lighting system installation it may be desired to alter the light output or the power consumed thereby from a remote or centralised location.

In accordance with the present invention there is provided a power control apparatus for lighting systems comprising:

a power variation means coupled to receive an input power source of AC electricity and produce a controllable output power source of AC electricity for operating an electrical load comprising at least one light;

monitoring means for monitoring electrical parameters of the input power source and/or the output power source to produce monitoring signals;

a digital processing means coupled to receive said monitoring signals and coupled to said power variation means so as to control said power variation means to vary said output power source between a maximum output level and a minimum output level;

a timer coupled to said digital processing means; and

a first memory storing control parameters and coupled to said digital processing

means;

wherein said digital processing means is responsive to a condition of said monitoring signals to control said power variation means to produce said output power source at a first predetermined level for a predetermined time period and thereafter to reduce said output power source to a second predetermined level, and wherein said second predetermined level and said predetermined time period are set by said digital processing means according to the control parameters stored in said first memory.

Preferably said stored control parameters include indications of predetermined times of day and/or days of week and corresponding values for said second predetermined level, and wherein said digital processing means is responsive to said timer at said predetermined times of day and/or days of week to change said second predetermined level to the corresponding value stored in said memory.

In a preferred form of the invention, at least one light sensor is coupled to the digital processing means, and the digital processing means is also responsive to a light level detected by the at least one light sensor to increase or decrease the second predetermined level. In one form of the invention, the apparatus includes a plurality of light sensors coupled to said digital processing means, each producing a respective detected light level value, and wherein said digital processing means is operative to calculate a weighted average of the detected light level values on the basis of preselected respective weighting factors stored in said memory, said digital processing means being responsive to the weighted average to increase or decrease said second predetermined level.

Preferably, the apparatus further comprises an input port coupled to the digital processing means for receiving control commands, wherein said digital processing means is responsive to a first control command to change said stored control parameters including said second predetermined level.

Preferably, a second memory is also provided coupled to the digital processing means for

storing performance data, and wherein for each power variation in said output power source said digital processing means stores performance data in said second memory. The performance data may include data representing the output level of said output power source and the time the power variation occurred.

In one form of the invention a plurality of power variation means are provided coupled to a single digital processing means, with each power variation device being arranged to supply its output power source to a corresponding different electrical load. In this configuration, the digital processing means is preferably adapted to control each of the power variation means separately according to different corresponding second predetermined levels.

Various forms of power variation means may be utilised in the invention. For example, the power variation means may comprise a variable transformer, wherein said first predetermined level corresponds to a larger AC voltage than said first predetermined level. Alternatively, the power variation means may comprise, for example, a waveform modification device, such as a silicon controlled rectifier (SCR), wherein the difference between the first and second predetermined levels is effected by varying the firing time of the SCR with respect to the voltage zero crossing point of the AC electricity input power source.

In a preferred form of the invention, said power variation means comprises a variable transformer, and wherein said first predetermined level corresponds to a larger AC voltage than said second predetermined level. Preferably, said monitoring means monitors line voltage and/or line current of said input power source in order to determine the zero crossing times thereof, and wherein said digital processing means is adapted to control said power variation means to vary the output power source only at least substantially at a said zero crossing time.

As can be determined by those skilled in the art from the present specification, embodiments of the invention provide for a power control apparatus which can be utilised to reduce power consumption of an electrical load such as a fluorescent lighting system. When a condition such as the turning on of fluorescent lights is detected by the monitoring means, the preferred

power control apparatus responds by increasing the output power source to a first predetermined level (eg maximum available power) in order to facilitate starting of the lights. After a predetermined time period the output power source is then reduced to a second predetermined level in order to conserve electrical power. The second predetermined level and thus the amount of power saving, is adjustable by way of an input port for receiving power control commands. The second predetermined level may also be adjusted by the influence of other inputs, such as at selected times of the day, or in response to a light sensor which measures ambient light.

The invention is described in greater detail hereinafter by reference to several embodiments thereof illustrated by way of example in the accompanying drawings, wherein:

Figure 1 is a block diagram of a power control apparatus according to a first embodiment;

Figure 2 is a block diagram of a power control apparatus according to a second embodiment;

Figure 3 is a block diagram of a power control apparatus according to a third embodiment;

Figure 4 is a functional flow diagram illustrating an algorithm for controlling a microprocessor device in an embodiment of the invention;

Figure 5 is a block diagram illustrating a further embodiment of the invention;

Figure 6 illustrates an example of a power device for use in embodiments of the invention; and

Figure 7 is a timing diagram.

A power control apparatus 2 is illustrated in Figure 1 in block diagram form, coupled between a mains AC electrical input power source 4 and one or more electrical loads 6, such as a fluorescent or discharge lighting system, or the like. The power control apparatus 2 comprises generally a power variation means in the form of power device 8, and a digital processing means embodied in microprocessor circuit 10. The power device 8 is coupled to receive the

mains electrical input power source 4, and provides at least one output power source 9 providing power to the at least one load 6. Monitoring circuitry 12, 14 is provided for monitoring electrical parameters of the mains electrical input power source 4 and output power sources 9, respectively. As shown diagrammatically in Figure 1, each of the monitoring circuits 12, 14 receive signals which are indicative of voltage and current flow of the input and output power sources, respectively, and provide input to the digital processing circuit 10. Thus, as will be apparent to those skilled in the art, each of the monitoring circuits 12, 14 advantageously includes appropriate signal filtering and conditioning circuitry, and conversion circuitry for providing inputs to the digital processing circuit 10 in appropriate signal levels and formats, indicative of the voltages and currents monitored. Analog–to–digital conversion circuitry is also included in the monitoring circuits 12, 14 in order to provide the appropriate inputs to the digital processing circuit 10.

The power device 8 primarily provides a means for varying the power supplied to the electrical loads 6 through each of the output power sources 9. Several methods of varying the power supplied to the output power sources 9 are applicable, and the particular form of the power device 8 will depend upon the power variation method employed. For example, one way of reducing the power utilised by a load 6 is to supply the load at a reduced voltage. In that case, the power device 8 may comprise a voltage reduction transformer, and it is preferred that the transformer output voltage be capable of variation between at least 100% of input voltage down to a fraction of the input voltage such as 50%. This can be achieved through the use of, for example, an auto–transformer of conventional form, which has a plurality of voltage taps or is continuously variable. In order to vary the output voltage of the auto–transformer, the output tap is moved from one connection to another which, depending upon the physical characteristics of the transformer, can be achieved mechanically or through electrical switching. It will be readily apparent to those skilled in the art that the switching or mechanical movements, such as by way of stepper motor, required in order to vary the output voltage can be achieved by conventional means, and thus the details of implementation are not included here so as to avoid clouding the clarity of description of the invention.

Another way in which the power output of the power device can be varied from the input power source level is through the use of waveform modification such as may be achieved utilising a silicon controlled rectifier (SCR) or thyristor circuit. In that case, the level of output power from the power device can be varied by varying the firing time of the SCR or thyristor. By increasing the firing time with respect to the zero crossing point of the source power input voltage waveform, it is possible to vary the power delivered to the load 6 at the output of the power device 8. The manner in which the firing time of a waveform modification circuit of the type described will also be readily apparent to those skilled in the art, and thus is not described in detail.

The power device 8 is coupled to the digital processing circuit 10 by way of a power control circuit 16. The function of the power control circuit 16 is primarily to receive control signals from the digital processing circuit 10 and translate those signals into the form required for controlling the power variation of the power device 8. For example, where the power device 8 comprises a continuously variable auto-transformer whose output is controlled mechanically through the use of a stepper motor or the like, the power control circuit 16 is adapted to translate logic level control signals output from the digital processing circuit 10 into electrical signals for operating the stepper motor so as to vary output of the power device 8. On the other hand, for different embodiments of the power device 8, the power control circuitry 16 may not be required, or may be incorporated in the digital processing circuit circuit 10. For example, if the power device 8 comprises waveform modification circuitry such as SCRs which require only logic level signals which are timed accurately, then those firing signals may be provided directly from the digital processing circuit 10.

The digital processing circuit 10 may comprise any suitable digital processing circuitry, such as a microprocessor or microcontroller circuit or the like having provision for input and output of signals, and memory for storing control algorithms and data. For example, an 8251 microcontroller circuit, which will be recognised by those of skill in the art, can be effectively utilised in the digital processing circuit 10. As mentioned, the digital processing circuit 10 receives input signals from the monitoring circuits 12 and 14, and outputs control signals to

the power device 8 by way of the power control circuitry 16. The digital processing circuit 10 is also provided with a programming input port 18, an output data port 20, and optionally is coupled to one or more display devices 22.

The digital processing circuit 10 includes processing circuitry which functions under the control of instructions stored in a memory circuit, preferably a non–volatile form of memory, such as ROM, PROM, EPROM, flash RAM or battery backed RAM. The circuit 10 is also provided with memory such as RAM memory for storing control parameters (which may be received from the programming port 18) and storing data to be output by way of the output port 20 or display device 22. The primary function of the digital processing circuit 10 is to act in accordance with its programmed instructions and control parameters, and on the basis of inputs received from the monitoring circuits 12, 14 and programming input port 18, so as to control the power device 8, and in particular the output power directed to the loads 6 through output power sources 9. Figure 4 illustrates an example of a control algorithm for the microprocessor control circuit 10. The algorithm illustrated in the flow chart diagram of Figure 4 in practice would be embodied in instruction codes stored in memory and executed by the microprocessor or microcontroller, although in an alternative the digital processing circuitry 10 could comprise a programmable logic circuit (PLC) or the like, in which case the algorithm may be hard wired into the PLC. As mentioned, in addition to memory storage for the control instructions, the digital processing circuit 10 preferably also is provided with memory storage for control parameters which may be received, for example, by way of the programming port 18. The control parameter data stored in the digital processing circuit 10 would typically include:

data indicative of a reduced operating power level for the loads coupled to the control apparatus;

the number of steps between the reduced operating power level and the full operating power level where the power device 8 is variable in discrete steps;

the time delay, when new load is added, to remain at full output power level before decrementing to the reduced output power level;

a threshold value indicating the amount of new load that must be added for the output

power source to be switched to full output power; and

the time interval to remain at each step where the power level varies in discrete steps or, where the power level is continuously variable, the total time to reduce the power level from the full output level to the reduced output level.

Referring to Figure 6, there is illustrated a simplified diagram of an auto–transformer 40 which may be utilised in the power device 8 of embodiments of the present invention. The auto–transformer 40 is configured to receive mains input voltage V_{IN} at the primary terminals thereof, and has a plurality of taps labelled P_1 to P_6 for secondary terminals. The taps P_1 to P_6 are coupled to respective inputs of a multiplexing circuit 42 which has a single output 44 which provides an output voltage V_{OUT}. The multiplexing circuit 42 is constructed so as to couple one and only one of the inputs thereof to the output 44, in accordance with a command input 46, provided in practice from the digital processing circuit 10.

By way of example, the taps P_1 to P_6 may be arranged so as to enable variation of the output voltage $_{OUT}$ within the range of 100% V_{IN} to 50% V_{IN} in 10% increments. Accordingly, the output voltage and consequently the output power supplied to the load, can be varied by changing the transformer tap to which voltage output line 44 is coupled. As mentioned, this is achieved through the use of multiplexing circuit 42 on command from the digital processing circuit 10. The switching from one tap to another is carried out at the zero crossing point time of the input voltage waveform so as to avoid significant discontinuities in the output voltage waveform thereby avoiding the introduction of noise into the output of the power device. It is also preferred that the output power be reduced by only a single increment at a time, with a delay in between so as to effect a gradual decrease in output power. On the other hand, when it is necessary to increase the output power, such as to enable starting of additional fluorescent lights which have been added to the load, then the output power is preferred to be increased to its maximum as soon as possible rather than incrementally.

Figure 7 illustrates a graph of output voltage referenced to input voltage for a power control apparatus employing a power device of the type shown in Figure 6 during operation. When

first initiated (t_0) the microprocessor controller of the power control apparatus sets the output voltage of the power device to maximum voltage (maximum power level). The output voltage remains at maximum for a predetermined time period T_S, after which at time t_1 the voltage is reduced by one increment. This reduction by a single increment corresponds, for example, to the multiplexing circuit 42 switching the connection of output line 44 from tap P_1 to tap P_2. The output voltage remains at that voltage for an interval T_I before being decremented once more at time t_2. Again the voltage remains constant for the interval T, before being decremented again (at time t_3). By this time the output voltage has reached, in this example, 70% of the input voltage V_{IN}, corresponding to transformer tap P_4. In the present example, that output voltage corresponds to the desired output power level for the power control apparatus, and thus the output voltage remains at that level without being further decremented. When additional load is added, such as by switching on additional fluorescent lights, the output voltage is increased again to the maximum (illustrated at time t_4) and thereafter the output voltage returns to its quiescent level incrementally as before described, unless additional load is added in the meantime.

Referring to the above example, the parameter data which might typically be stored in memory by the digital processing circuit 10 would be the reduced (quiescent) output power level, or data corresponding thereto such as the identification of the transformer tap or the number of decrements from maximum voltage level or the actual output voltage as measured by the output monitoring circuitry, the time period to remain at maximum voltage (T_S), the decrement time interval T_I, and the threshold increase in load required before returning to maximum voltage.

For example, consider a power control apparatus in which the power device is constructed for an input voltage of 240 V a.c., and an output voltage of 240 V to 150 V variable in steps of 10 V (e.g. an auto-transformer having ten secondary taps). Control parameters for such an arrangement might be, for a typical application:

Reduced output $V_R = 200$ V

Maximum voltage time	T_S = 20 seconds
Decrement interval time	T_I = 3 seconds
Load increase threshold	I_T = 0.5 Amp output

Referring now to Figure 4, a flow chart 100 of a control algorithm for a microprocessor of the digital processing circuit 10 is shown, beginning with an initialisation step 102, where the microprocessor and its various inputs and outputs are initialised in order to ensure that the relevant signals are able to be received and dispatched. At this time, also, the microprocessor consults its associated memory to retrieve the control parameters of the type discussed above. Initially the output power to each of the loads 6 is set to maximum power (step 104), for example to facilitate starting of fluorescent lights. This is achieved by the digital processing circuit 10 controlling the power device 8, by way of the power control circuit 16 where applicable, in order to set the power device to provide maximum output power (e.g. full mains line voltage). In the example of Figure 6, this would correspond to a control signal on line 46 from the digital processing circuit controlling the multiplexing circuit 42 so as to couple output line 44 to the auto-transformer tap P_1. Once the power device is set to maximum power, a delay timer is started at step 106, in order to begin timing the maximum power interval (T_S, referring to Figure 7).

Parameters of the power device output are measured (step 108) by way of the monitoring circuitry 14 coupled to the output power source 9. Typically these parameters would include the output line voltage and output line current supplied to each load. If the line current supplied to a particular load increases, this may be indicative of an increased load, e.g. by extra lights being switched on. If the load remains constant, the procedure passes from step 110 to step 112 where it is determined whether or not the time delay T_S has expired. Whilst the time delay T_S remains unexpired, the procedure continues to monitor the output parameters for loading increase by repeating steps 108, 110 and 112. A loading increase is detected by comparing values of the measured output line current over time to sense an increase in current. When an increased current is detected, the amount of increase is compared to the load increase threshold control parameter in order to determine whether the

increased current constitutes an increase in load worthy of returning the output to full power level.

If an increase in load is detected at step 110, the procedure passes to step 126 at which time the input parameters monitored by the monitoring circuitry 12 are measured. The monitoring circuit 12 may monitor the mains input power source line voltage and current in a different way to the monitoring circuit 14 because it is phase information of the input electrical signals which are particularly important in this instance. As mentioned previously, it is preferred that any switching or variation between power levels by the power device take place at the zero crossing time of the input power source waveform so as to avoid noise and transitory phenomenon during switching. Thus, instantaneous values of the voltage and current waveforms may be supplied by the monitoring circuitry 12, as compared to peak or RMS values supplied by the circuitry 14. One way in which to detect the zero crossing point is by way of digital signal processing (DSP) circuitry included in the digital processing circuit 10. For example, digital samples of the instantaneous mains input power source voltage and current levels can be analysed by DSP for detection of the zero crossing points thereof. It will be readily recognised that the implementation of that feature is within the knowledge of those skilled in the art.

The input parameters are monitored at steps 126 and 128 until the phasing of the signals is appropriate (eg at the zero crossing point) before the procedure passes to step 104, whereupon the power of the power device 8 is set to maximum level, as described herein above.

When the maximum power time delay T_S is complete (step 112), the procedure sets about decrementally decreasing the power level to the required (reduced) power setting. This begins at steps 114 and 116 where the input parameters are monitored in similar fashion to steps 126 and 128, until the input phasing is correct. When the phasing reaches the zero crossing point, the power device 8 is controlled by the digital processing circuit 10 so as to decrement the output power level (step 118). Referring again to Figure 6, in the first instance this action may be reducing the output voltage from 1.0 V_{in} to 0.9 V_{in} by changing the multiplexor 42

connection from auto-transformer tap P_1 to P_2. The digital processing circuit 10 then determines whether the pre-selected reduced power level has been reached, by comparison with the stored control parameter data mentioned previously. In the example of Figure 7, this occurs after the power supplied to the load 6 has been decremented by the power device three times. If the desired reduced power level has not yet been reached, then the procedure returns to step 108, after initiating an interval timer which corresponds to the time interval T_I (Figure 7). Typically the interval timer might be of the order of several seconds, whereas the maximum power delay timer (T_S) may be of the order of 15 seconds or so.

In the example mentioned above concerning the control parameters, the reduced output power level was presented in terms of the actual output voltage V_R supplied to the load. In that case, the step 120 would be accomplished by comparing the control parameter V_R with the measured output voltage supplied by the monitoring circuit 14. Then, if V_R is greater than the actual output voltage the reduced output power level has been reached, and if not then the procedure continues to decrement the output level again.

Once the desired reduced power level has been reached, the microprocessor control algorithm enters a monitoring loop comprising steps 122 and 124, which monitor the output parameters from monitoring circuitry 14, and detect any load increase, similar to steps 108 and 110. If an increase in load current greater than the threshold is detected, the controller algorithm is passed to step 126 to monitor the phasing of the input signals before returning the output power to maximum level at step 104.

Figure 2 illustrates a power control apparatus according to an embodiement of the present invention which includes additional features to the embodiment shown in Figure 1. In particular, the input monitoring circuitry 12 includes an input from a light level measurement device 26, such as a photo-diode or the like. The light level measurement device would typically be positioned within a space illuminated by the fluorescent lights which constitute one of the loads 6, so as to provide a measurement of the light produced from the load supplied by the power control apparatus. This enables the digital processing circuit 10 to implement

a feedback loop, so that the power device can be controlled so as to output power according to a specified light level, rather than a particular power level as described hereinabove. The light level to be supplied may be set by way of a light level setting input 24, or may be specified by the control parameter data stored in memory. The control steps required in the procedure for the digital processing circuit 10 which are necessary to implement the light level feedback control will be apparent to those skilled in the art, and need not be described in detail here.

Figure 3 is a block diagram illustrating another embodiment of the power control apparatus, which is specifically adapted for use in controlling street lights or the like. Once again this embodiment includes a light level measurement device 26 so that the control apparatus can vary the power supplied by the power device 8 so as to supply the power needed to provide illumination to a preselected level. The light level measurement device is particularly advantageous where the lights comprising the load 6 illuminate an area which also receives natural light, such as a street light, so that power can be reduced to reduce illumination from the light load when additional illumination is supplied naturally (eg when the sun rises). In this embodiment, also, the mico processor 10 includes a control routine which enables it to determine if the light comprising the load 6 is faulty. This can be easily determined by reference to the monitoring signals provided by the output monitoring circuitry 14. The power control apparatus 2 in this instance also includes a telemetry circuit 28 which transmits an output from the digital processing circuit 10 in the event that the light load 6 is faulty. The telemetry circuit 28 transmits its output by way of radio signals or telephony signals, for example, to a central controller (not shown), which can then take action so as to replace the faulty light.

More than one light level measurement device 26 may in fact provide input to the digital processing circuit 10, in order to supply light level measurements from a plurality of locations illuminated by the lighting load 6. In this case, the digital processing circuit 10 may perform a weighted averaging of the light level measurements, for example depending upon the particular positioning of the measurement devices, in order to control the power device 8.

Thus, a plurality of light level measurement devices may provide input signals to the digital processing circuit 10, with the value of each signal being weighted by a respective predetermined weighting value. The weighted light level measurements are then averaged, and the averaged value compared with a preset value stored as a control parameter in memory. This allows the power control apparatus to take account of the actual effect of the load output, so that the averaged light level value and corresponding control parameter can be used to determine the appropriate reduced output power level, rather than a comparison between the output line voltage and the preset reduced output voltage level control parameter. Depending upon the illumination and power saving strategy employed, light level sensors which are placed so as to be affected by natural or external illumination may be treated with greater or lesser weight, as desired. Alternatively, the input signals provided by the plurality of light level sensors may be subjected to a threshold test instead of weighted averaging, wherein the highest or lowest light level sensor signal (averaged over time, perhaps, to allow for transitory variations) is compared with a threshold value to determine if the area concerned is over or under illuminated at any location.

Each power control apparatus 2 can be constructed to control a plurality of loads 6 through a plurality of output power sources 9. One way in which that may be achieved is to construct the power control apparatus with a plurality of power devices 8 coupled to the digital processing circuit 10 in parallel, and with each power device 8 coupled to a separate respective load 6. In order to control the power delivered to each load 6 individually, however, each of the respective power devices 8 should be controlled separately by the digital processing circuit 10, and for that purpose each power device would be provided with a separate control connection to the circuit 10. Furthermore, separate output monitoring circuitry 14 should be included for each power device 8, so that an increase in any individual load 6 can be detected, for example, and dealt with by controlling only the corresponding power device. The input monitoring circuitry 12 may be utilised in common for controlling each of the power devices. Similarly, it is possible to provide a plurality of output power sources from a single power device where the power device comprises a voltage transformer by constructing the transformer with a plurality of secondary outputs which can be tapped

individually by connection to respective multiplexing circuits, for example.

In order to control the output power source the control algorithm for the digital processing circuitry 10 must of course be adapted from that described in connection with Figure 4 to deal with multiple inputs and outputs. One way in which that may be achieved is to arrange the digital processing circuit 10 to multitask or swap between processing tasks utilising time-slices or the like, as is known to those skilled in the art. However, it will also be recognised that, in executing the algorithm illustrated in Figure 4, most of the time during normal operation the procedure will remain in the monitoring loop comprising steps 122 and 124. Therefore, one way in which the algorithm and digital processing circuit may be adapted for controlling multiple power devices is to provide a similar loop with an interrupt driven by a detected increase in loading on any one of the output power sources coupled to the digital control circuit. When the interrupt is activated the control algorithm of the digital processing circuit is directed to the sub-routine specific to the corresponding load and power device for control of an increase and decremental decrease in supplied power.

As mentioned herinabove, the power control apparatus 2 may also be constructed so as to alter the power level to be output from the power device according to the time of day or day of the week. The control parameter data may be arranged to also store information indicative of temporal changes in the desired output power level, for example by storing day and time data with corresponding reduced output power level values. The control algorithm of the digital processing circuit may also be modified to periodically examine the stored time/day data in order to determine when a stored time and day arises, and to thereupon replace the operative reduced output power level with that corresponding to the matching time and day. For example, in a commercial building it may be desirable to have one power level operative during trading hours, another during the time required by cleaners or the like, and yet another during other times. The manner in which provision for this function can be included in the control algorithm for the digital processing circuit will be readily apparent having regard to the preceding description.

The programming port 18 is arranged to receive instructions and/or data from an external source, such as a central control panel. One particular use of the programming port 18 is for alteration of the control parameter data stored in memory in the digital processing circuit 10. For example, if it is desired to increase the light level in a particular area in which illumination is controlled by the power control apparatus, then an instruction may be issued from a remote source, or indeed from a local input keyboard or the like, to alter the control parameter corresponding to the reduced power level. The programming port can be utilised by the power control apparatus to receive data modifying or replacing any of the control parameters described hereinabove, including those for altering the output power level at various times of the day. The digital processing circuit of each power control apparatus is may be individually coded such that only data received at the programming port 18 which is preceded by the correct code will be acted on by the microprocessor. This arrangement operates both as a security measure and as a means for allowing a plurality of power control apparatuses to be coupled to a single central controller communicating on a data bus. An arrangement such as this can be advantageous in a number of applications, such as in a large commercial building. For example, a large retail store having multiple floors might have a separate power control apparatus 2 for controlling the lights on each floor of the building. However, it may also be desirable to have the lights controllable or programmable from a central location such as the security office for the building. In this case a number of power control apparatuses might be connected to a single central control panel 50 in the manner shown in Figure 5.

The output port 20 mentioned previously also provides for external communication, and might be also connected to a central control panel by the same data bus as the programming port 18. The memory in the digital processing circuit 10 preferably allows storage room for storing data representative of the performance of the power control apparatus for the purposes of evaluation and analysis of power usage. In the simplest implementation, each time the digital processing circuit controls the power device to increase or decrease the power level, an entry is made in the memory storage indicating the time and the resulting power level. This data provides information sufficient to indicate the performance of the power control apparatus. As an additional measure, the output line current value (indicative of load) may be stored at

the time of each control change, which aids in determining both loading information, and power consumption information as compared to the same load operating on nominal mains line power without the power control apparatus. The mechanics of storing such information at each control change is well within the ability of the person skilled in the relevant art.

In order to retrieve the performance data stored in the digital processing circuit memory, the circuit 10 and control algorithm is preferably constructed to transmit the stored data on the output port in response to a download command received on the programming port 18 and coded for that particular power control apparatus. The performance data is then transmitted from the digital processing circuit, most likely to a remote site, for analysis and evaluation.

An advantage of utilising a transformer based power device over a waveform modification device, aside from the reduction of noise introduction which may be accomplished, is the benefit of being able to actually increase the output line voltage above that supplied by the input power source. This is particularly advantageous in the case where the mains power supply voltage varies. In that instance, the power control apparatus may compensate for the variation in the supply voltage, even to the point of controlling the output power source voltage to a level higher than the input voltage. For that purpose, where the power device employed is in the form of a transformer, the transformer is advantageously provided with one or more taps which provide a secondary voltage above the primary voltage. The control algorithm can then be further enhanced to monitor the peak line voltage of the input power source and provide a voltage boost when full power is required.

The foregoing detailed description of the invention has been presented by way of example only, and is not intended to be considered limiting to the invention which is defined in the claims appended hereto.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A power control apparatus for lighting systems comprising:

a power variation means coupled to receive an input power source of a.c. electricity and produce a controllable output power source of a.c. electricity for operating an electrical load comprising a plurality of lights;

monitoring means for monitoring electrical parameters of the input power source and the output power source to produce monitoring signals, the monitoring means detecting changes in line current suppled to said electrical load through said output power source;

a digital processing means coupled to receive said monitoring signals and coupled to said power variation means so as to control said power variation means to vary said output power source between a maximum output level and a minimum output level;

a timer coupled to said digital processing means; and

a first memory storing control parameters and coupled to said digital processing means, said control parameters including a line current increase threshold value;

wherein said digital processing means is responsive to a condition of said monitoring signals indicating a detected increase in said line current exceeding said threshold value to control said power variation means to produce said output power source at a first predetermined level for a predetermined time period and thereafter to reduce said output power source to a second predetermined level, and wherein said second predetermined level and said predetermined time period are set by said digital processing means according to the control parameters stored in said first memory.

2. A power control apparatus as claimed in claim 1, wherein said stored control parameters include indications of predetermined times of day and/or days of week and corresponding values for said second predetermined level, and wherein said digital processing means is responsive to said timer at said predetermined times of day and/or days of week to change said second predetermined level to the corresponding value stored in said memory.

3. A power control apparatus as claimed in claim 1 or 2, including at least one light sensor coupled to said digital processing means, wherein said digital processing means is

responsive to a light level detected by the at least one light sensor to increase or decrease said second predetermined level.

4. A power control apparatus as claimed in claim 3, including a plurality of light sensors coupled to said digital processing means, each producing a respective detected light level value, and wherein said digital processing means is operative to calculate a weighted average of the detected light level values on the basis of preselected respective weighting factors stored in said memory, said digital processing means being responsive to the weighted average to increase or decrease said second predetermined level.

5. A power control apparatus as claimed in any of claims 1 to 4, further comprising an input port coupled to the digital processing means for receiving control commands, wherein said digital processing means is responsive to a first control command to change said stored control parameters including said second predetermined level.

6. A power control apparatus as claimed in claim 5, further comprising a second memory coupled to the digital processing means for storing performance data, and wherein for each power variation in said input power source said digital processing means stores performance data in said second memory.

7. A power control apparatus as claimed in claim 6, wherein said performance data includes data representing the output level of said output power source and the time the power variation occurred.

8. A power control apparatus as claimed in claim 7, further comprising an output port coupled to said digital processing means, and wherein said digital processing means is responsive to a second said control command to transmit said performance data stored in said second memory to said output port.

9. A power control apparatus as claimed in any of claims 1 to 8, wherein said monitoring means monitors line voltage and/or line current of said input power source in order to determine the zero-crossing times thereof, and wherein said digital processing means is

adapted to control said power variation means to vary the output power source only at least substantially at a said zero-crossing time.

10. A power control apparatus as claimed in any of claims 1 to 9, wherein said power variation means comprises a variable transformer, and wherein said first predetermined level corresponds to a larger a.c. voltage than said second predetermined level.

11. A power control apparatus as claimed in claim 1, including a plurality of power variation means coupled to said digital processing means, each power variation means being arranged to supply its output power source to a corresponding different electrical load.

12. A power control apparatus as claimed in claim 11, wherein said digital processing means is adapted to control each of the power variation means according to different corresponding control parameters stored in said first memory.

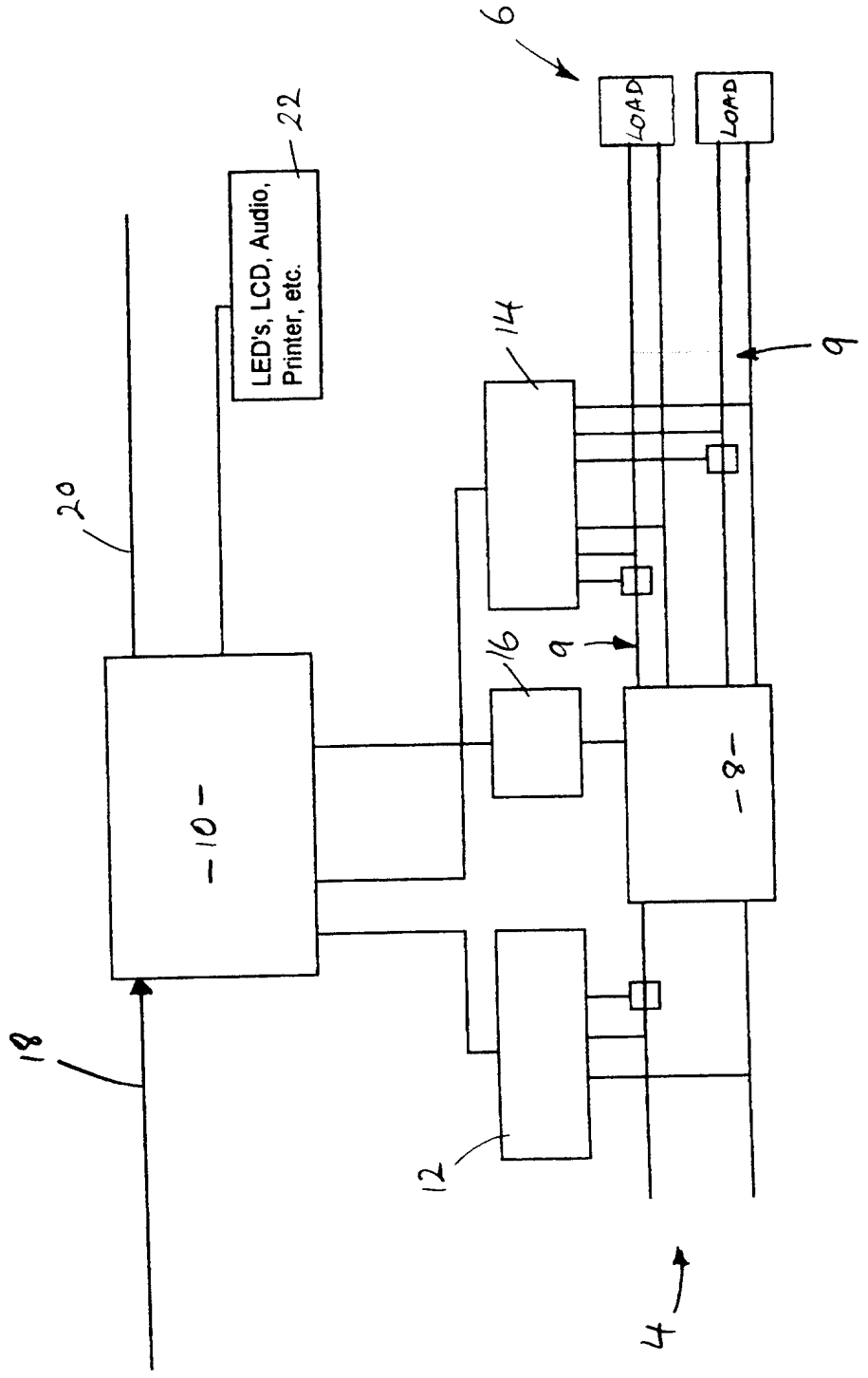

6
LOAD
LOAD
22
LED's, LCD, Audio,
Printer, etc.
14
9
20
16
9
-10-
-8-
18
12
4
2

FIG. 1

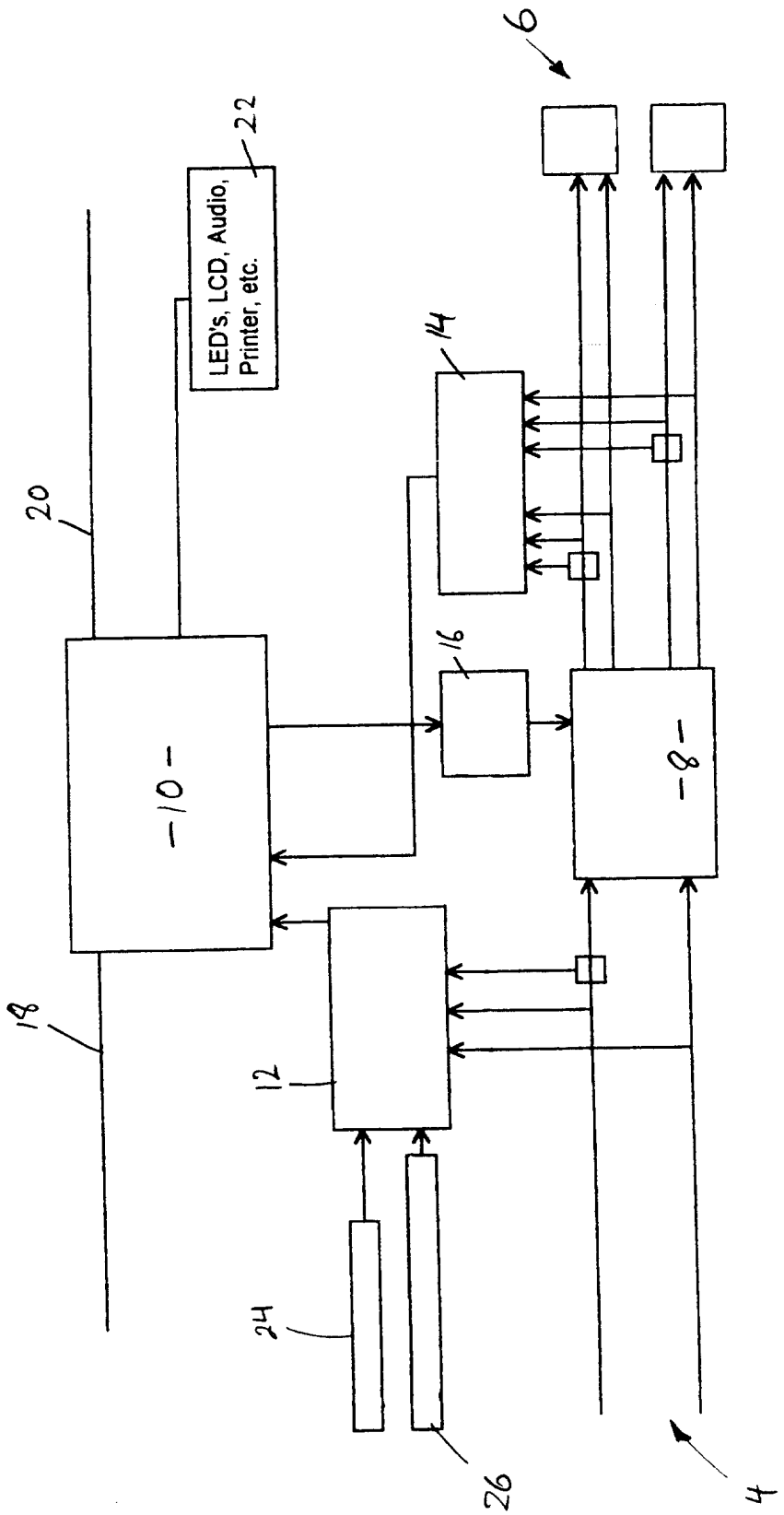


FIG. 2

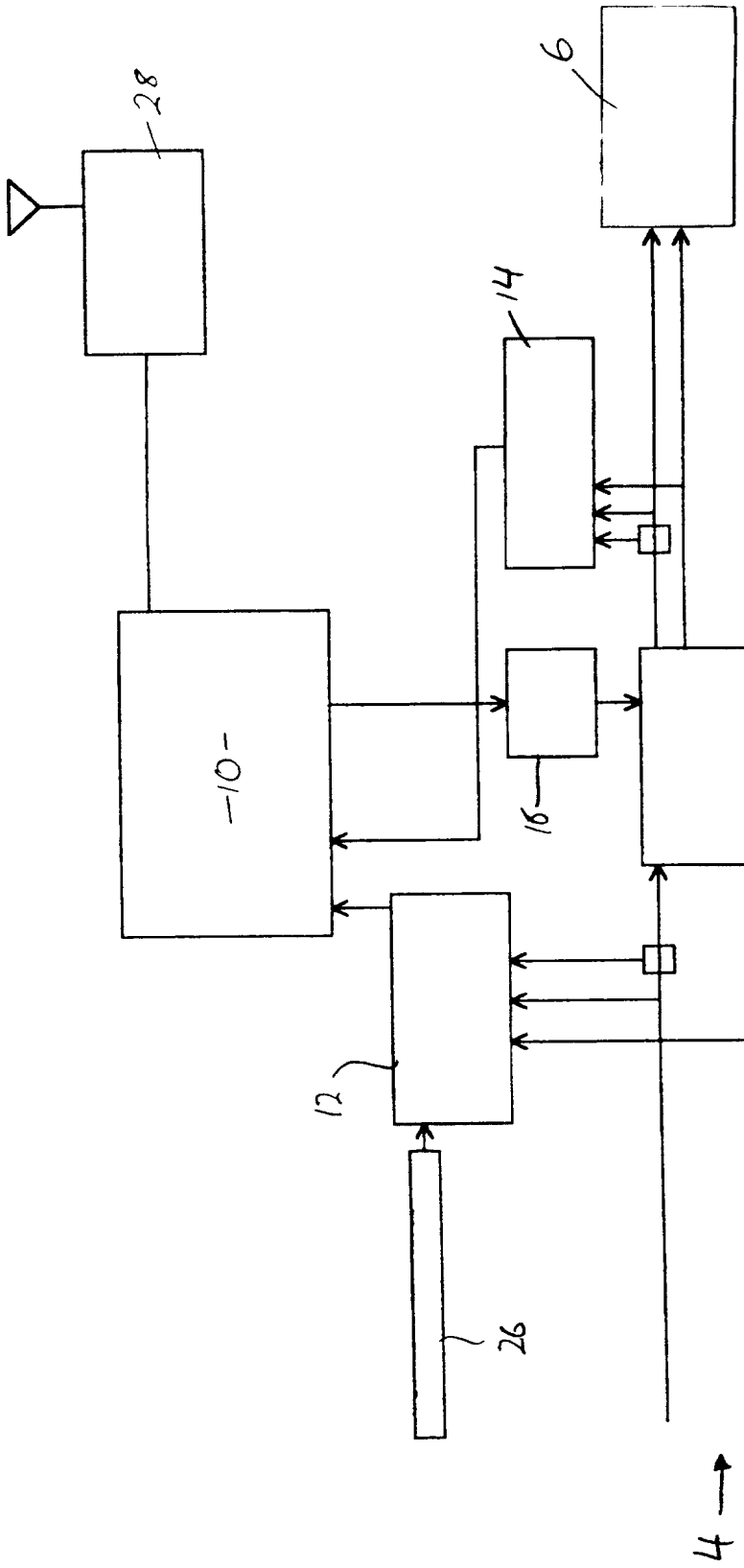


FIG. 3

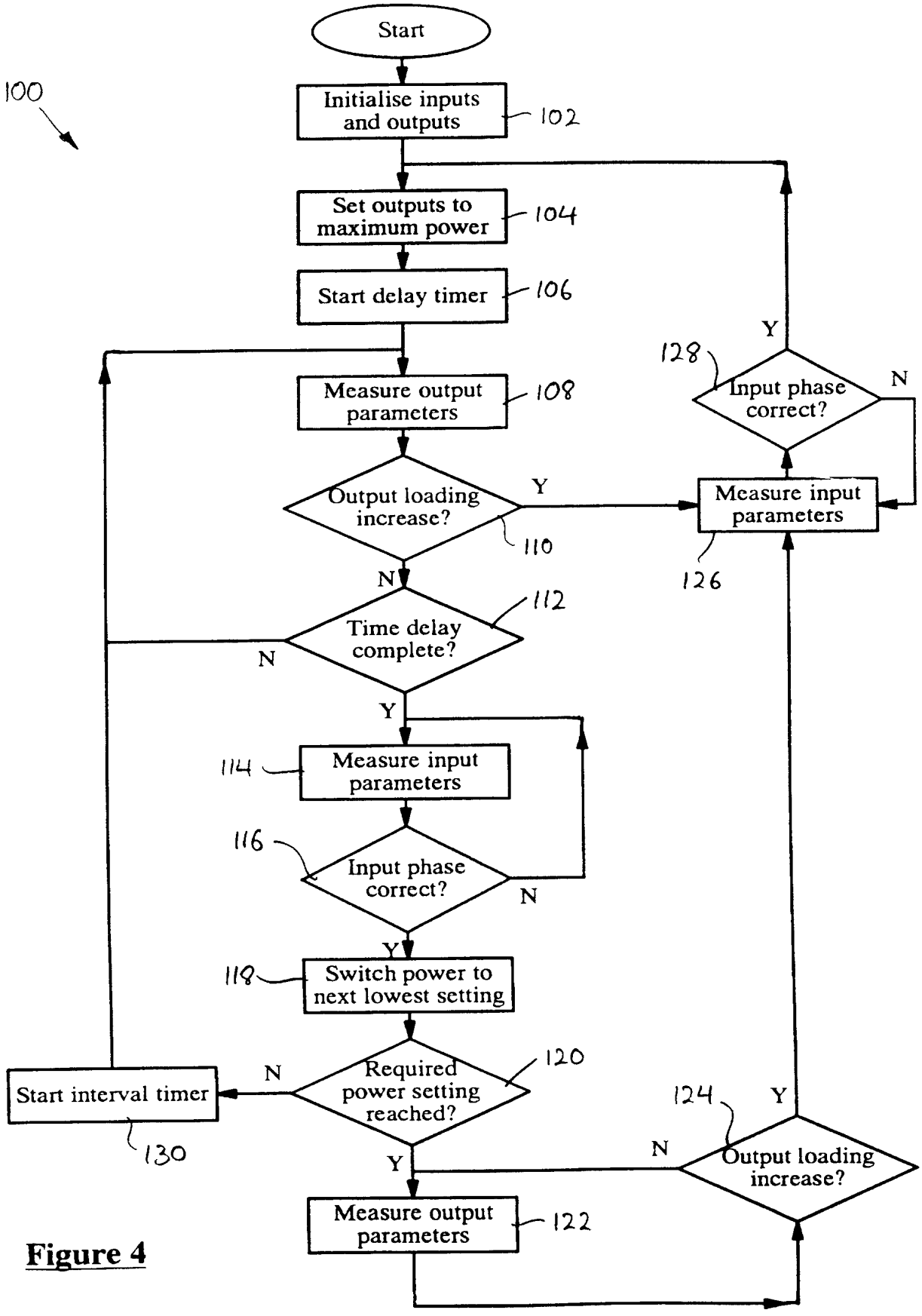

Start
100
Initialise inputs and outputs
102
Set outputs to maximum power
104
Start delay timer
106
Measure output parameters
108
Output loading increase?
110
Y
N
Time delay complete?
112
N
Y
Measure input parameters
114
Input phase correct?
116
N
Y
Switch power to next lowest setting
118
Required power setting reached?
120
N
Y
Start interval timer
130
Measure output parameters
122
Output loading increase?
124
N
Y
Measure input parameters
126
Input phase correct?
128
Y
N

Figure 4

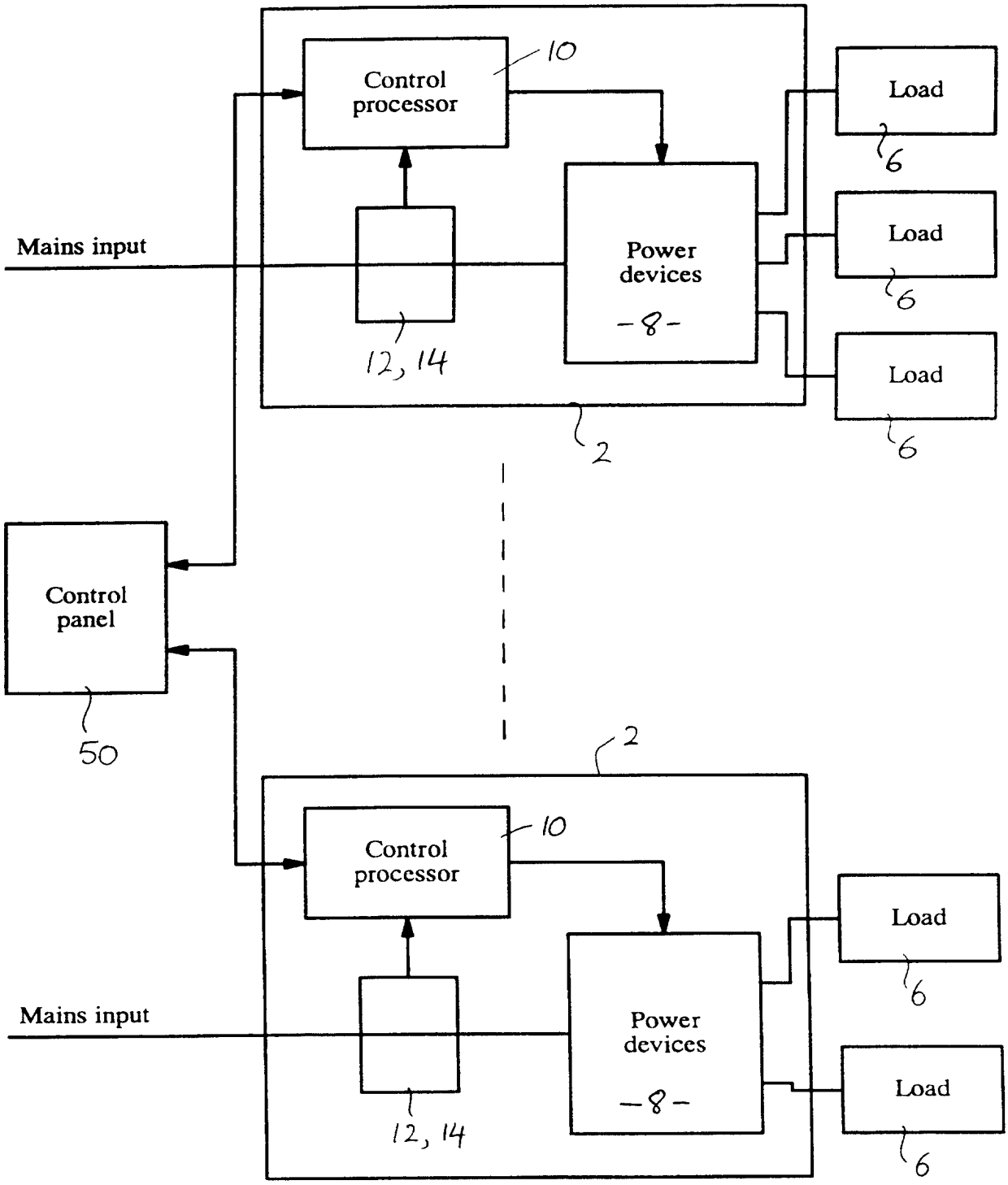

Control processor
10
Load
6
Load
6
Load
6
Power devices
-8-
Mains input
12, 14
2
Control panel
50
2
Control processor
10
Load
6
Load
6
Power devices
-8-
Mains input
12, 14

Figure 5

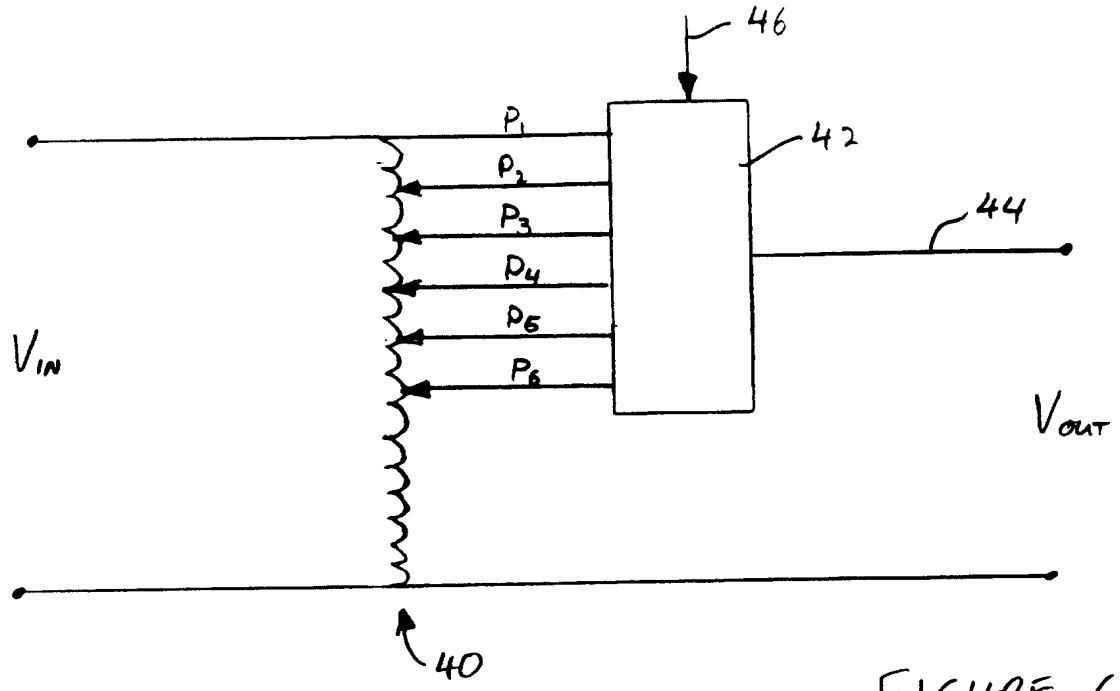


FIGURE 6.

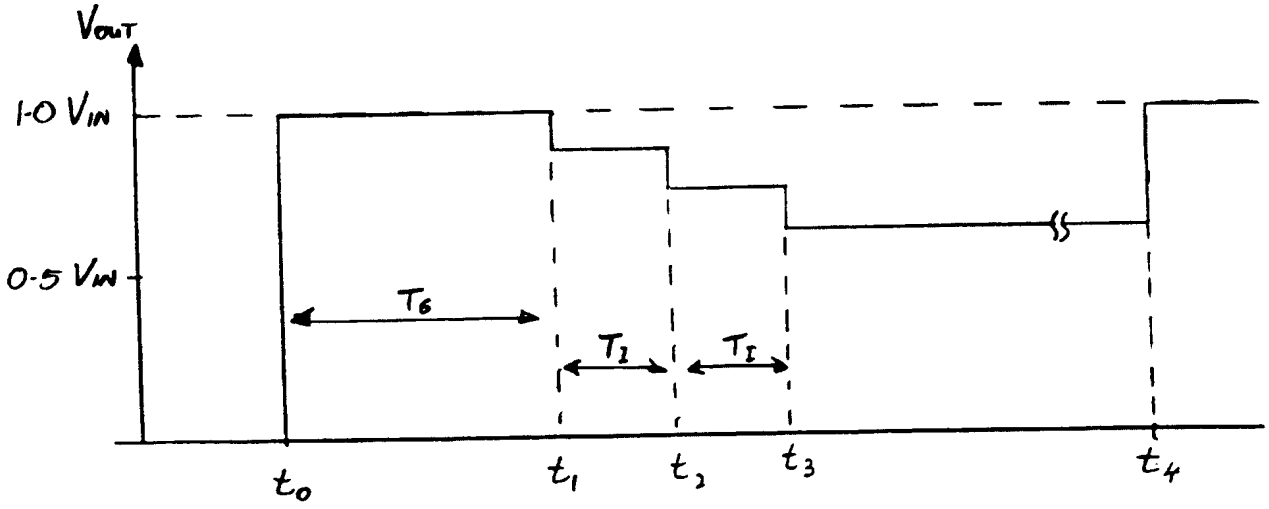


FIGURE 7.

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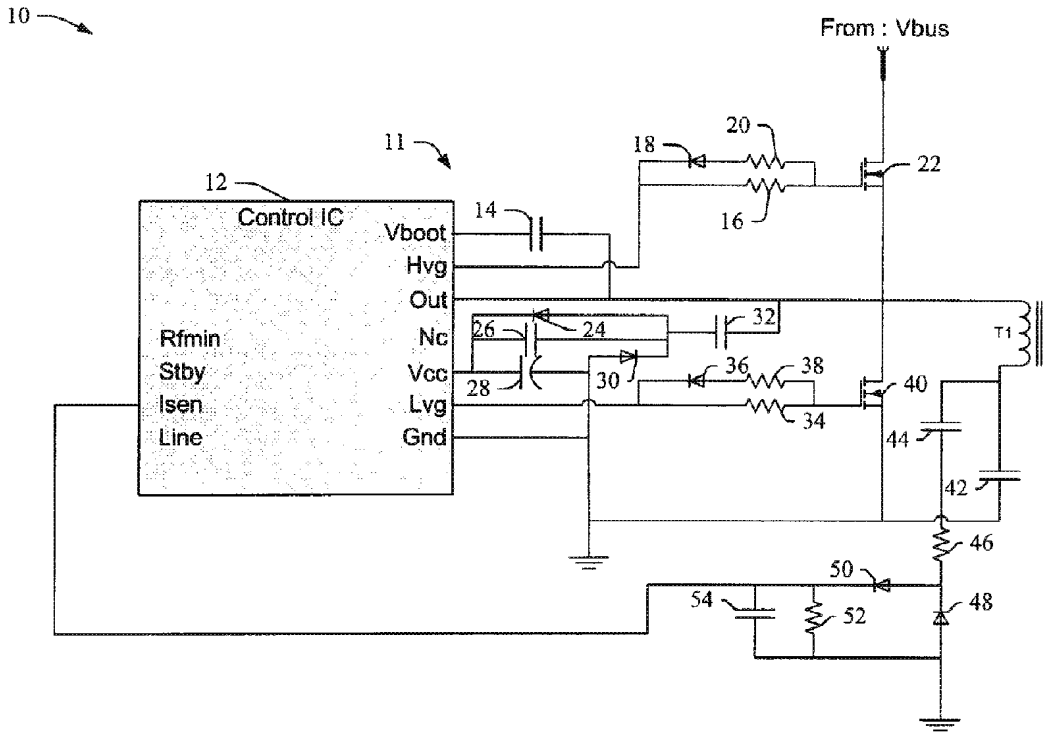
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(54) Titre : CIRCUIT D'ATTAQUE DE DEL A CIRCUIT ONDULEUR UNIQUE A SORTIES MULTICANAL ISOLEES
(54) Title: LED DRIVER WITH SINGLE INVERTER CIRCUIT WITH ISOLATED MULTI-CHANNEL OUTPUTS



(57) Abrégé/Abstract:
A single-converter circuit-based LED driver circuit (10) with isolated multi-channel outputs is disclosed. The circuit (10) includes an IC control circuit (11), a plurality of isolated output channels (70, 74) each having an output current sensing and conditioning circuit (74, 90), and an output current regulation circuit (128). The out-put current regulation circuit (128) includes a voltage-sensing transformer winding (T4) that senses an output voltage level across a secondary side of the circuit (10), and a peak output current sensing component (156) that senses output currents from the isolated out-put channels and determines which channel has a highest current output. Additionally, the circuit (10) facilitates providing output current regulation when detected output voltage is below a predetermined threshold, and providing output current regulation when the detected output voltage is above the predetermined threshold.

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) **Title**: LED DRIVER WITH SINGLE INVERTER CIRCUIT WITH ISOLATED MULTI-CHANNEL OUTPUTS

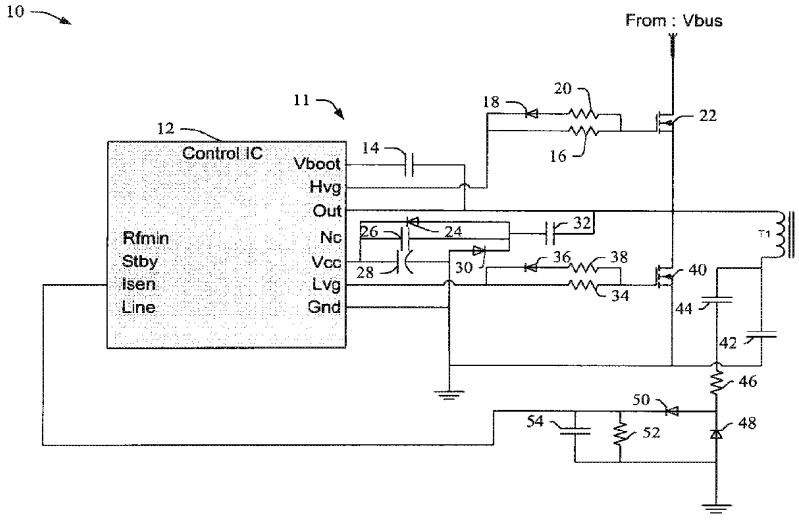


FIG. 1

(57) **Abstract**: A single-converter circuit-based LED driver circuit (10) with isolated multi-channel outputs is disclosed. The circuit (10) includes an IC control circuit (11), a plurality of isolated output channels (70, 74) each having an output current sensing and conditioning circuit (74, 90), and an output current regulation circuit (128). The output current regulation circuit (128) includes a voltage-sensing transformer winding (T4) that senses an output voltage level across a secondary side of the circuit (10), and a peak output current sensing component (156) that senses output currents from the isolated output channels and determines which channel has a highest current output. Additionally, the circuit (10) facilitates providing output current regulation when detected output voltage is below a predetermined threshold, and providing output current regulation when the detected output voltage is above the predetermined threshold.

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LED DRIVER WITH SINGLE INVERTER CIRCUIT WITH ISOLATED MULTI-CHANNEL OUTPUTS

BACKGROUND OF THE DISCLOSURE

[0001] Light emitting diode (LED) lighting systems have been gaining increasing popularity in replacing incandescent and discharge lamps due to their long life, energy efficiency, and flexibility in optical design. As a result, the application of LED systems has come to include not only low-power applications, but also high-power applications. LED systems are also gaining popularity in outdoor applications, in addition to indoor applications. Moreover, LED systems are being used in general applications, and not just in special lighting applications.

[0002] For some applications, a Class II isolation for output is required. A typical Class II high-power LED driver design uses a common front-end power factor correction section with either multiple isolated LED converters in parallel, or with multiple single stage isolated LED drivers connected to the same power sources. In such arrangements, component redundancy is undesirably high. Consequently, the cost and size of such arrangements are high and system efficiency is low.

[0003] Accordingly, there is an unmet need in the art for systems and methods that facilitate reducing component redundancy and increasing system efficiency in Class-II rated circuits, and for overcoming the deficiencies noted above.

SUMMARY OF THE DISCLOSURE

[0004] In accordance with one aspect, a circuit for controlling an LED lighting system comprises a single-converter control circuit with a primary winding T1, and a first isolated output channel circuit with at least one secondary winding T2, T3 tightly coupled to the primary winding T1 and to a first output current sensing and conditioning circuit. The circuit further comprises at least a second isolated output channel with at

least one secondary winding T6, T7 tightly coupled to the primary winding T1 and to a second output current sensing and conditioning circuit. The circuit further comprises an output current regulation circuit that determines peak current output through the first and second isolated output channels.

[0005] In accordance with another aspect, an LED driver output channel regulation circuit comprises a voltage-sensing winding T4 that senses voltage across a multi-channel secondary circuit, and at least first and second photodiodes that transmit current, the first and second photodiodes being coupled to respective isolated output channel circuits in the secondary circuit. The circuit further comprises a peak current regulation component that compares current transmitted by the photodiodes, determines which of the isolated output channel circuits has a higher peak output current, and regulates the output current thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIGURE 1 illustrates a primary side of the circuit, which includes an IC controller and a half-bridge-based resonant converter, in accordance with one or more aspects described herein.

[0007] FIGURE 2 illustrates a secondary side of the circuit, including multiple isolated output channels, in accordance with one or more aspects described herein.

[0008] FIGURE 3 illustrates a current regulation portion of the circuit, which regulates a channel having a highest sensed output current at any given time, in accordance with one or more aspects described herein.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0009] The following description relates to a single converter circuit-based LED driver with isolated multi-channel outputs. Advantages of the described circuit design include that all outputs meet Class II requirements, only one IC control and converter circuit is

used, component count is reduced, and efficiency is improved. That is, the single converter with multiple outputs facilitates providing a circuit at low cost, high efficiency and small size. A half-bridge-based resonant converter is employed as a platform for a high-power LED driver application. However, it will be appreciated that a current-fed, fly-back, or any other isolated circuit platform can be employed in conjunction with the various embodiment set forth herein.

[0010] FIGURES 1-3 illustrate a circuit 10 comprising a single converter circuit-based LED driver with isolated multi-channel outputs, in accordance with various aspects described herein. The following discussion relates to the specific configuration of the circuit 10, and features thereof. As shown in FIGURE 1, the circuit 10 comprises a control integrated circuit (IC) 12, which comprises a plurality of input/output (I/O) pins. In one example, the IC 12 is an L6599 IC. A capacitor 14 (e.g., a 0.1μF capacitor or the like) is coupled to a bootstrapped supply voltage (Vboot) pin on the control IC 12, as well as to a high-side driver reference (Out) pin and a primary transformer winding T1. According to an example, the winding T1 is a G30876 winding. A high-side driver output (Hvg) pin on the IC 12 is coupled to a resistor 16 and diode 18, which in turn is coupled to a resistor 20. Resistors 16 and 20 are coupled to a gate of a switch 22 (e.g., a MOSFET or the like), and the drain of the switch 22 is coupled to a voltage bus. In one example, the resistor 16 is a 20Ω resistor, the diode 18 is a 1N4148 diode, the resistor 20 is a 1kΩ resistor, and the switch 22 is an IRF740 MOSFET.

[0011] A source voltage (Vcc) pin on the IC 12 is coupled to each of a diode 24, a capacitor 26, and a capacitor 28. The capacitor 28 is coupled to a diode 30, which is coupled to a capacitor 32, as well as to the diode 24, the capacitor 26, and to ground. The capacitor 32 is further coupled the diode 24, the capacitor 26, the capacitor 14, the output pin on the IC 12, and the primary transformer winding T1. According to an example, the diodes 24 and 30 are 1N4148 diodes, the 26 is a 0.1μF capacitor, the capacitor 28 is a 10μF capacitor, and the capacitor 32 is a 150pF capacitor.

[0012] The low-side driver output (Lvg) pin on the IC 12 is coupled to a resistor 34 and diode 36, which in turn is coupled to a resistor 38. Resistors 34 and 38 are coupled to a gate of a switch 40 (e.g., a MOSFET or the like), and the drain of the switch 40 is

coupled to the source of the switch 22. The source of the switch 40 is coupled to the diode 30, the capacitor 28, a capacitor 42, and to ground. The capacitor 42 is further coupled to the primary transformer winding T1 and to a capacitor 44. In one example, the resistor 34 is a 20Ω resistor, the diode 36 is a 1N4148 diode, the resistor 38 is a 1kΩ resistor, the switch 40 is an IRF740 MOSFET, the capacitor 42 is a 15nF capacitor, and the capacitor 44 is a 100pF capacitor.

[0013] The capacitor 44 is coupled to a resistor 46, which is coupled to diodes 48 and 50. The diode 50 is coupled to a resistor 52 and a capacitor 54, both of which are coupled to ground and to the diode 48, which is also coupled to ground. The diode 50, the resistor 52, and the capacitor 54 are further coupled to a current sensing (Isens) pin on the IC 12. Other pins on the IC (e.g., Nc and Line, etc.) are left unconnected. A ground pin on the IC 12 is coupled to the capacitor 28, the diode 30, and to ground. In one example, the resistor 46 is a 50Ω resistor, diodes 48 and 50 are 1N4148 diodes, the resistor 52 is a 10kΩ resistor, and the capacitor 54 is a 33nF capacitor.

[0014] Turning now to FIGURE 2, with continued reference to Figure 1, the circuit 10 includes a first isolated output channel 70, a second isolated output channel 72, and an output current sensing and conditioning circuit 74.

[0015] The first output channel circuit 70 includes the winding T5, which is coupled to Earth ground1, as well as to a capacitor 76 and a diode 78. The capacitor 76 and diode 78 are coupled to a diode 80, which in turn is coupled to a capacitor 82. The capacitor 82 is coupled to the diode 78, the winding T5, and the Earth ground 1. The circuit further includes secondary transformer windings T2 and T3, both of which are coupled to Earth ground 1 (E-Gnd1), and inductively coupled to winding T1. In one example, the capacitors 76, 82 are 22nF capacitors, the diodes 78, 80 are 1N4148 diodes, and the windings T2, T3, T5 are G30876 windings.

[0016] Winding T5 is tightly coupled to the primary side windings (e.g., T1, T4), and has a voltage source Vcc3 (e.g., a power supply) that ensures a voltage even if the output of channel 1 is shorted.

[0017] The second output channel circuit 72 includes the transformer windings T6 and T7. A diode 84 is coupled to winding T6, as well as to a diode 86 that is coupled to winding T7. The diodes 84 and 86 are further coupled to a capacitor 88, which is coupled to the windings T6 and T7 and to Earth ground 2 (E-Gnd2). The diodes 84 and 86, and the capacitor 88, are coupled to an output current (Iout) sensing and conditioning component 90 and to an LED 92. The Iout sensing and conditioning circuit 90 (e.g., similar or identical to the output current sensing and conditioning circuit 74) is coupled to an LED 94. In one example, the diodes 84, 86 are MUR420 diodes, the capacitor 88 is a 100μF capacitor, and the LEDs are NCSW136 LEDs.

[0018] The circuit 10 further includes a resistor 96 and a resistor 98 that are coupled to an amplifier 100. The amplifier 100 is further coupled to a photodiode 102 and a resistor 104, which are also coupled to each other. The amplifier 100 is coupled to a capacitor 106, which is also coupled to the photodiode 102 and a resistor 108. The resistor 108 is coupled to the amplifier 100 and to a resistor 110, which is in turn coupled to a resistor 112 and an LED 114. The resistor 112 is additionally coupled to Earth ground 1 (E-Gnd1). According to an example, the resistor 96 is a 10kΩ resistor, the resistor 98 is a 1kΩ resistor, and the amplifier 100 is a LM325 amplifier. In another example, the photodiode 102 is am SFH6106 photodiode, the resistor 104 is a 50Ω resistor, the capacitor 106 is a 22nF capacitor, the resistor 108 is a 5.6kΩ resistor, and the resistor 110 is a 1kΩ resistor. In yet another example, the resistor 112 is a 0.25Ω resistor, and the LED 114 is an NCSW136 LED.

[0019] An LED 116 is coupled to a diode 118, a diode 120, and a capacitor 122. The diode 118 is coupled to secondary winding T2, and the diode 120 is coupled to the secondary winding T3. The diodes 118 and 120 are further coupled to the capacitor 122, which in turn is coupled to the secondary windings T2 and T3, and to Earth ground 1 (E-Gnd1). According to an example, the LED is an NCSW136 LED, the diodes 118, 120 are MUR420 diodes, and the capacitor 122 is a 100μF capacitor.

[0020] Now turning to FIGURE 3, with continued reference to Figures 1 and 2, the circuit 10 includes an output current regulator circuit 128 with a voltage-sensing winding T4 that is coupled to a diode 130, which in turn is coupled to a resistor 132.

Winding T4 is tightly coupled to the secondary windings (e.g., T2, T3, T5, T6, and T7) and senses a voltage across the secondary side of the circuit 10 (see Fig. 2). Output voltage increases when there is a light load or no-load condition, such as when one or more LEDs are not connected. If the output voltage reaches or exceeds a predetermined threshold voltage (e.g., approximately 55V or so in one example), then the circuit 10 switches from current regulation to voltage regulation. Output currents for all channels are sensed, and the channel with the highest output current is regulated. According to an example, the winding T4 is a G30876 winding, the diode 130 is a 1N4148 diode, and the resistor 132 is a 100Ω resistor.

[0021] The resistor 132 is coupled to a capacitor 134 and a resistor 136, which is further coupled to a capacitor 138. The resistors 132 and 136, and the capacitor 134 are coupled to a resistor 140 which in turn is coupled to a resistor 142 and to the winding T4. The capacitor 134 is coupled to the resistor 136 and to the winding T4, as well as to the resistor 142. In one example, the capacitors 134, 138 are 33nF capacitors, the resistors 136, 142 are 1kΩ resistors, and the resistor 140 is a 10kΩ resistor.

[0022] The resistor 142 is further coupled to a resistor 144, which in turn is coupled to a voltage source Vcc2. The resistors 142 and 144 are coupled to an error amplifier 146, which is also coupled to Vcc2. The capacitor 138 is coupled to a resistor 148, which is also coupled to a diode 150. The resistor 148 and diode 150 are coupled to the error amplifier 146, and the diode 150 is further coupled to a resistor 152 that is coupled to a Standby (Stby) pin on the IC 12. According to an example, the resistor 144 is a 10kΩ resistor, the amplifier 146 is an LM325 amplifier, the resistor 148 is a 6.2kΩ resistor, and the diode 150 is a 1N4148 diode. In another example the resistor 152 is a 5kΩ resistor.

[0023] A resistor 154 is coupled to a minimum oscillating frequency setting (RfMin) pin on the IC chip 12 and to a peak output current regulating component 156. The regulating component 156 is further coupled to phototransistors 158 and 160, which in turn are coupled to each other and to ground, and which receive current signal from the photodiode 102 and equivalent photodiodes in other isolated channels (e.g., such as a second photodiode in the output current sensing and conditioning circuit 90). According

to an example, the resistor 154 is a 4.7kΩ resistor, the current regulating component 156 is a G20678 component, and the phototransistors 158, 160 are SFH6106 phototransistors.

[0024] Still referring to Figures 1-3, in the main transformer, all isolated windings are tightly coupled to each other to ensure that even with unbalanced loads on each output, the voltages on each output are equal to each other with minimum error. In each channel, the output current is sensed and fed back to the primary side (e.g., Figs. 1 and 3) to control and regulate the output current. Although all the outputs' currents are sensed, it is the highest current in the outputs that is regulated. The voltage and current characteristic of the photodiodes and error amplifiers are used to determine the other channel's current. In one embodiment, each channel employs the same type and numbers of LEDs, which are connected in series with even thermal distribution.

[0025] As shown in the Figures, the two secondary outputs are tightly coupled together for matching voltage at the output of each channel. Each channel drives the same type and number of LEDs in a series/parallel configuration. On each channel, there are two windings, T2 and T3, on secondary outputs with the common tie to the E-Gnd1. The diodes 118 and 120 are connected to T2 and T3 respectively to charge 122 and maintain the energy on the cap 122 and current to the LEDs 114, 116.

[0026] The sensing resistor 112 senses the channel output current, and the amplifier 100 further conditions the sensed signal and drives cathode of an optocoupler (which communicate signal(s) to phototransistors 158, 160). The amplifier 100 has a non-inverting input that is connected to a scaled down reference and inverting input via resistor 110 connected to sensing resistor 112. The windings T2, T3, which are tightly coupled to the primary winding T1 and isolated from the main power converter, provide the power supply for the first channel 70. The second channel 72 is configured the same as the first channel 70, but isolated by the separated windings T6, T7. Additional channels can be added in the same fashion as the second channel 72. Therefore, all the channels are isolated from the main power converter to meet Class II requirements.

[0027] On each channel, the optocoupler feeds back the output current signal to the peak current regulator 156. The channel with the highest output current is regulated at any

given time. In the event that a light load or no load condition is present in an output channel, voltage on the winding T4, which is tightly coupled to secondary of the output transformer, is indicative of the voltage on the output channels. This voltage is processed by error amplifier 146 to take over the control loop to regulate the maximum output voltage.

[0028] Accordingly, the circuit 10 facilitates sensing output currents for a plurality of isolated output channels and regulating the current of the channel with the highest output current at a given time. In this manner, the circuit eliminates a need to use multiple Class II converters for LED applications. Thereby saving costs, reducing circuit size, and increasing efficiency.

[0029] It will be appreciated that the specific examples of component values and/or model numbers presented herein are illustrative in nature and are not to be interpreted in a limiting sense. Other component values and/or models may be employed to achieve the described circuit functionality, as will be appreciated by those of skill.

[0030] The invention has been described with reference to the preferred embodiments. Obviously, modifications and alterations will occur to others upon reading and understanding the preceding detailed description. It is intended that the invention be construed as including all such modifications and alterations.

WHAT IS CLAIMED IS:

1. A circuit for controlling an LED lighting system, comprising:

a single-converter control circuit with a primary winding T1;

a first isolated output channel circuit with at least one secondary winding T2, T3 coupled to the primary winding T1 and a first output current sensing and conditioning circuit;

at least a second isolated output channel with at least one secondary winding T6, T7 coupled to the primary winding T1 and a second output current sensing and conditioning circuit; and

an output current regulation circuit that determines peak output current through the first and second isolated output channels;

wherein the output current regulation circuit includes a voltage-sensing winding T4, tightly coupled to the secondary windings, that detects a peak output voltage across each isolated output channel.

2. The circuit according to claim 1, wherein the output current regulation circuit includes first and second phototransistors that detect current signal from first and second photodiodes in the first and second isolated output channel circuits, respectively, to determine the peak current output in the first and second isolated output channel circuits.

3. The circuit according to claim 2, wherein each isolated output channel circuit includes a sensing resistor.

4. The circuit according to claim 3, wherein the first photodiode receives current through the sensing resistor and amplifier and provides current that is sensed by the first phototransistor.

5. The circuit according to claim 4, wherein the second photodiode receives current through a sensing resistor in the second output current sensing and conditioning circuit and provides current that is sensed by the second phototransistor.

6. The circuit according to claim 5, further comprising a peak output current regulating component that compares the current sensed by the first and second

phototransistors, and determines which of the first and second isolated output channels has a higher peak output current.

7. The circuit according to claim 6, wherein the single-converter control circuit controls the power output of the isolated output channel having the highest output current to protect and regulate the isolated output channel having the highest output current.

8. The circuit according to claim 1, wherein the first isolated output channel comprises a secondary winding T5 that is tightly coupled to the voltage sensing winding T4, which supplies power to the output channel circuit.

9. The circuit according to claim 8, wherein the secondary winding T5 generates a dedicated voltage source.

10. The circuit according to claim 1, wherein the first and second isolated output channels are compliant with Class II output channel isolation requirements.

11. The circuit according to claim 1, wherein the single-converter control circuit comprises a control integrated circuit (IC).

12. The circuit according to claim 11, wherein the control IC has a low-side driver output pin coupled to a first half-bridge circuit.

13. The circuit according to claim 12, wherein the control IC has a high-side driver output pin coupled to a second half-bridge circuit.

14. An LED driver output channel regulation circuit, comprising:

a primary side and a secondary side;

the secondary side including a multi-channel secondary circuit, the multi-channel secondary circuit comprising secondary windings that form isolated output channel circuits for each channel in the multi-channel secondary circuit;

a voltage-sensing winding T4 on the primary side that is tightly coupled to the secondary windings on the secondary side of the multi-channel secondary circuit,

the voltage-sensing winding T4 being configured to sense voltage across the multi-channel secondary circuit;

at least first and second photodiodes that transmit current, the first and second photodiodes being coupled to respective isolated output channel circuits in the secondary circuit;

a peak current regulation component that compares current transmitted from the photodiodes, determines which of the respective isolated output channel circuits has a higher peak output current, and regulates the output current thereof.

15. The circuit according to claim 14, further comprising output current sensing and conditioning circuits, each including a photodiode, and coupled to respective isolated output channel circuits.

16. The circuit according to claim 15, wherein each output current sensing and conditioning circuit amplifies a current through a sensing resistor and provides the current as input to respective photodiodes.

17. The circuit according to claim 16, wherein the first photodiode forms an optocoupler with a first phototransistor coupled to the peak current regulation component, and the second photodiode forms an optocoupler with a second phototransistor coupled to the peak current regulation component.

18. The circuit according to claim 14, wherein the isolated output channel determined to have the higher peak output current is controlled using voltage regulation when the output voltage sensed at the voltage-sensing winding T4 exceeds a predetermined threshold, and using current regulation when the output voltage sensed at the voltage sensing winding T4 is less than or equal to the predetermined threshold.

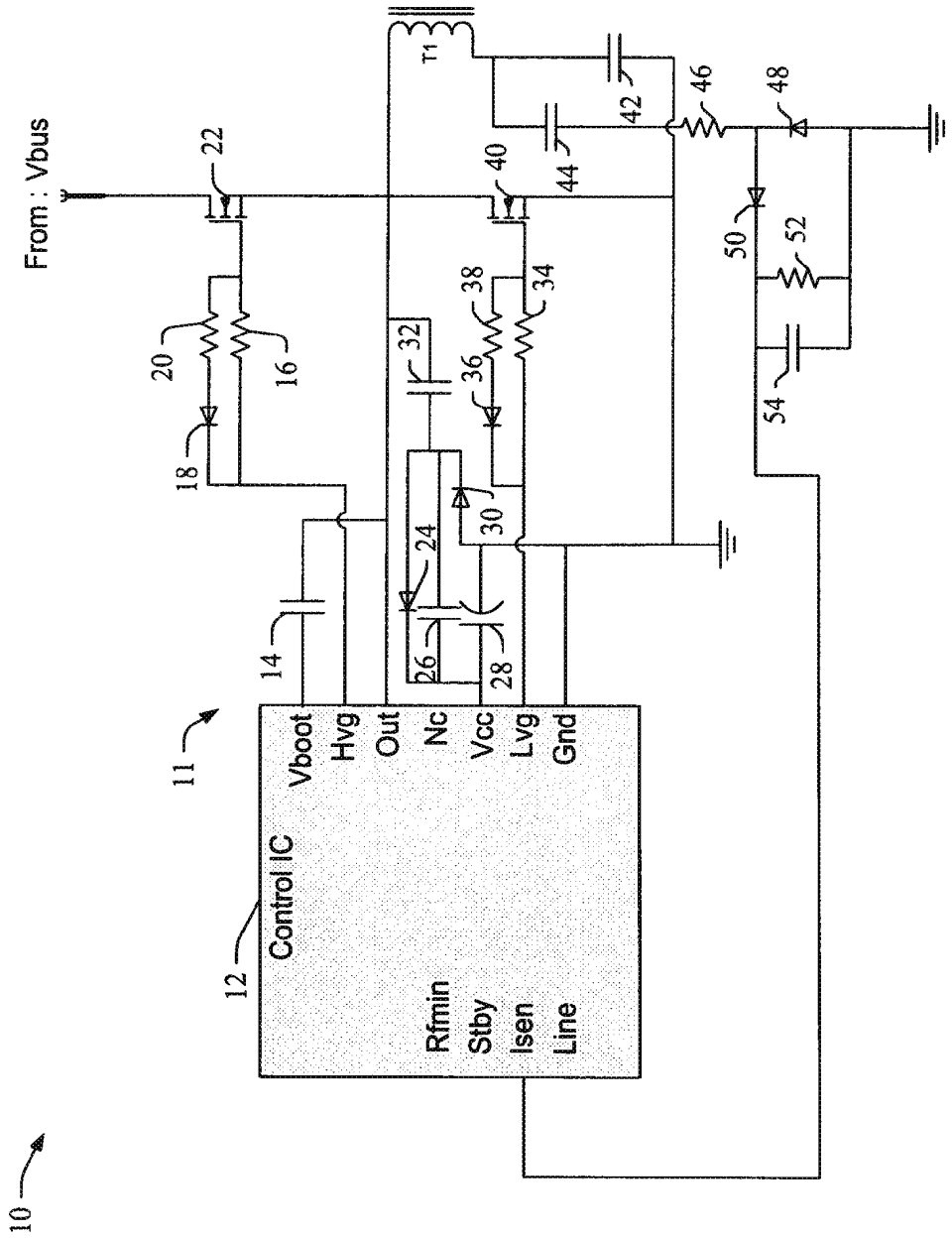

From : Vbus
T1
Vboot
Hvg
Out
Nc
Vcc
Lvg
Gnd
Control IC
Rfmin
Stby
Isen
Line
10
11
12
14
16
18
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48
50
52
54

FIG. 1

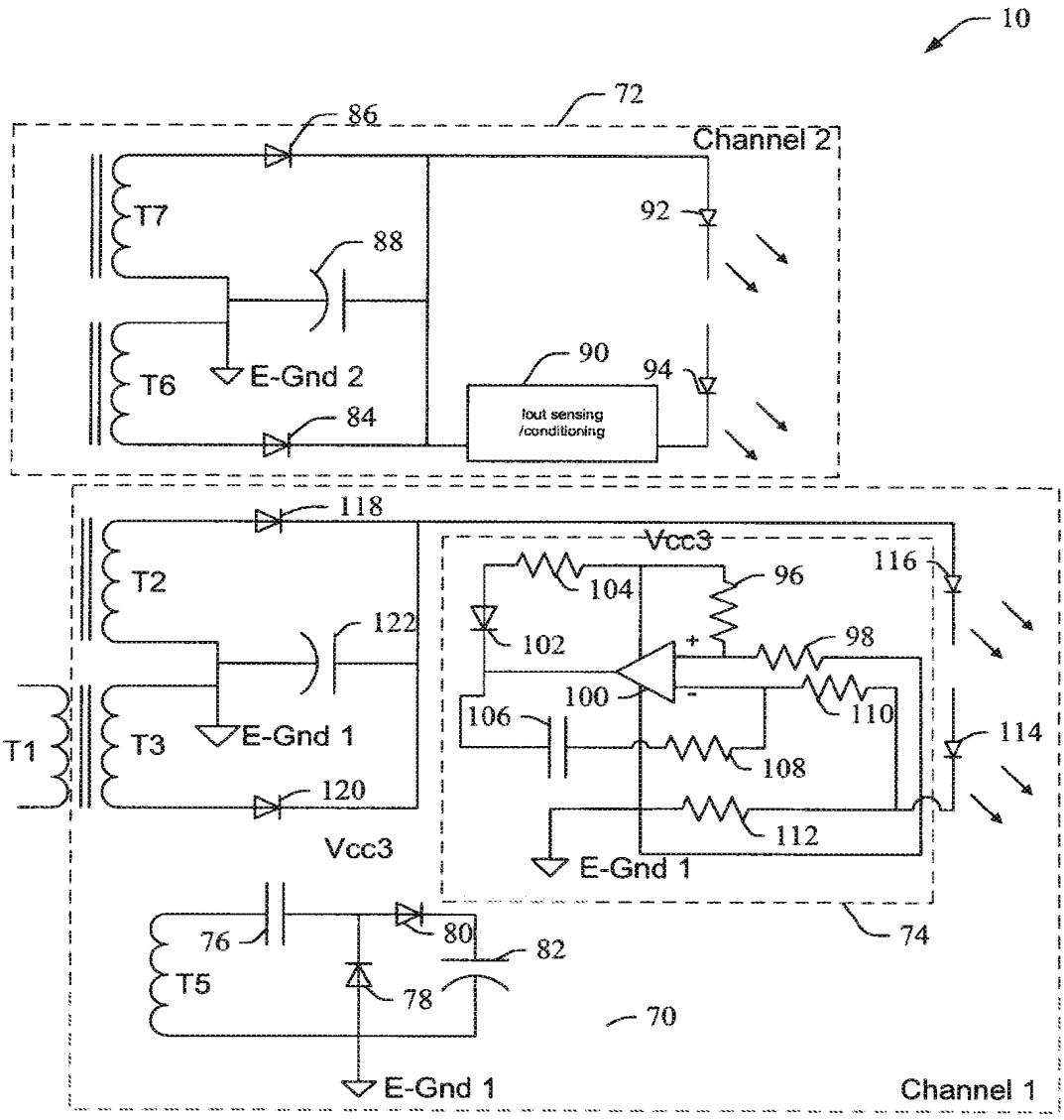

10
72
86
Channel 2
T7
92
88
T6
E-Gnd 2
90
94
Iout sensing
/conditioning
84
118
Vcc3
T2
104
96
116
102
122
98
+
100
-
106
110
T1
T3
E-Gnd 1
114
108
120
112
Vcc3
E-Gnd 1
74
76
80
82
T5
78
70
E-Gnd 1
Channel 1

FIG. 2

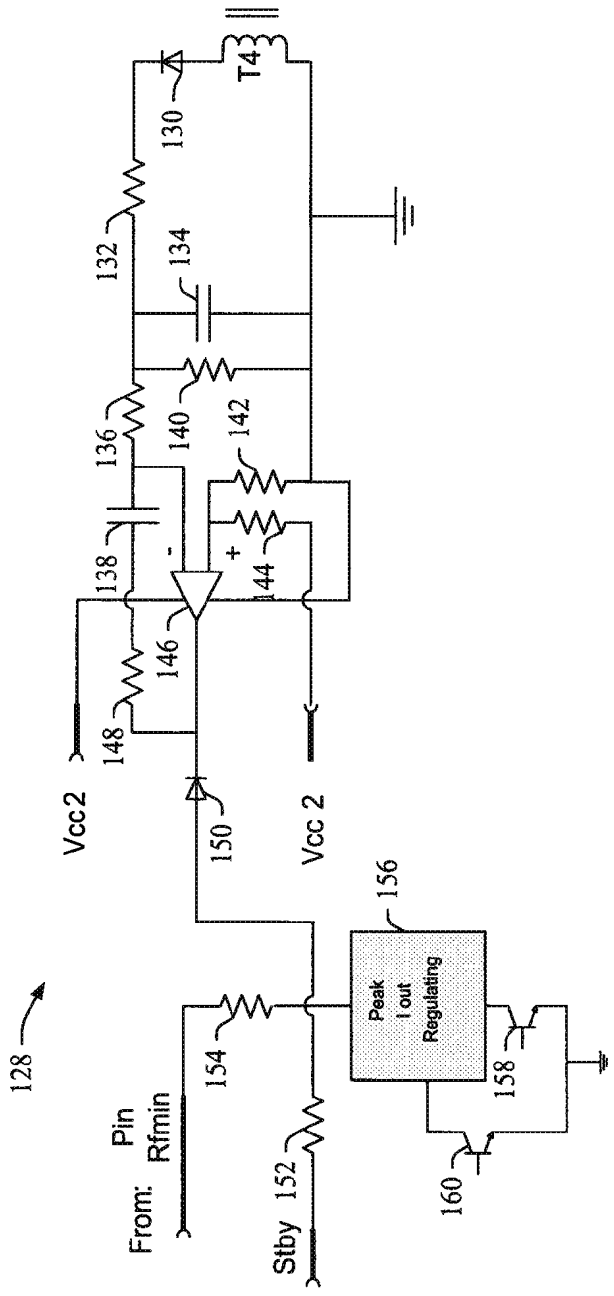
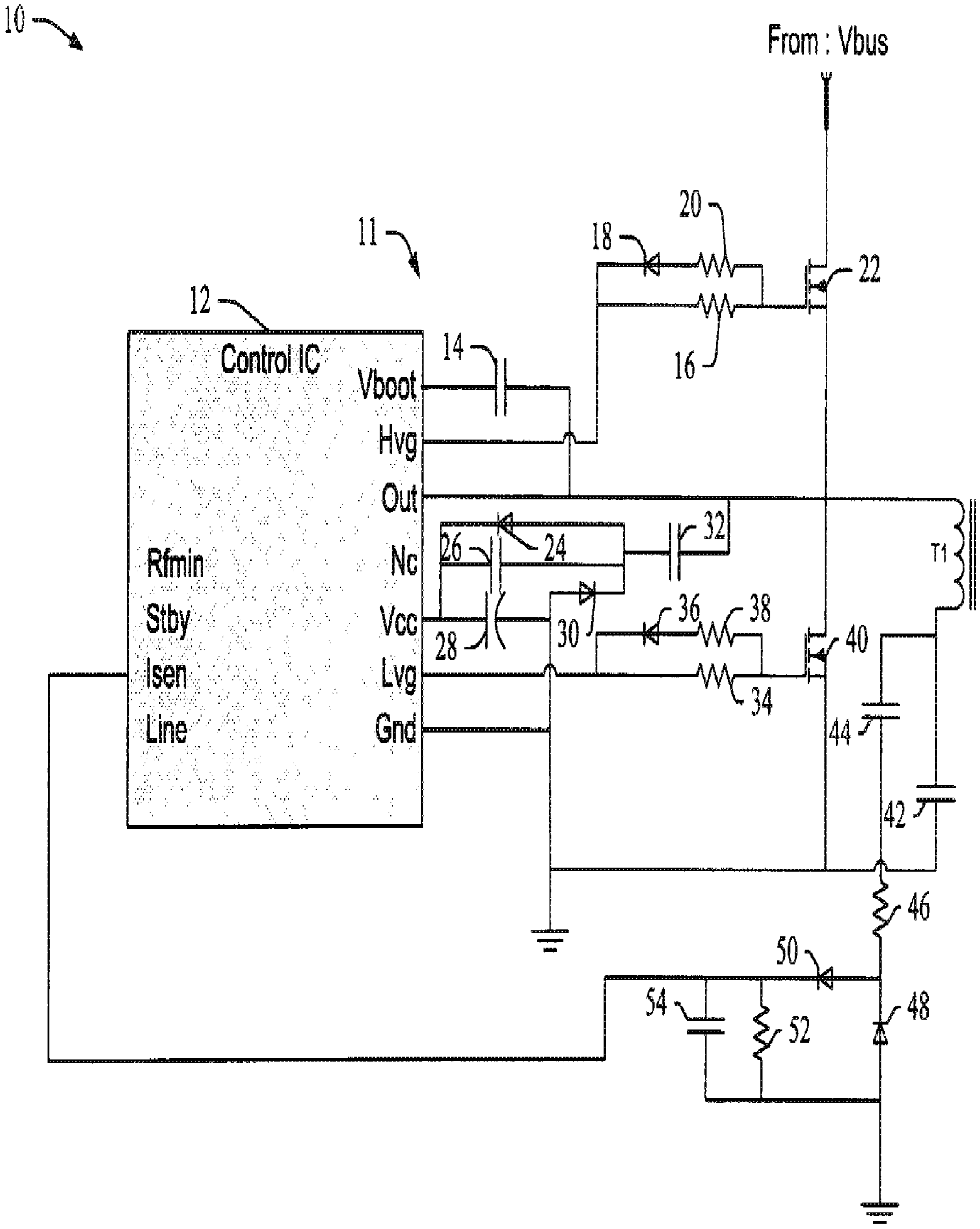

10
T4
130
132
134
136
140
142
138
144
146
148
150
Vcc2
Vcc 2
156
Peak
I out
Regulating
128
154
158
160
Pin
Rfmin
From:
Stby
152

FIG. 3


10
From : Vbus
11
12
Control IC
Vboot
Hvg
Out
Nc
Vcc
Lvg
Gnd
Rfmin
Stby
Isen
Line
14
16
18
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48
50
52
54
T1

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(54) Title: ELECTRONIC CIRCUIT FOR DC CONVERSION OF FLUORESCENT LIGHTING BALLAST

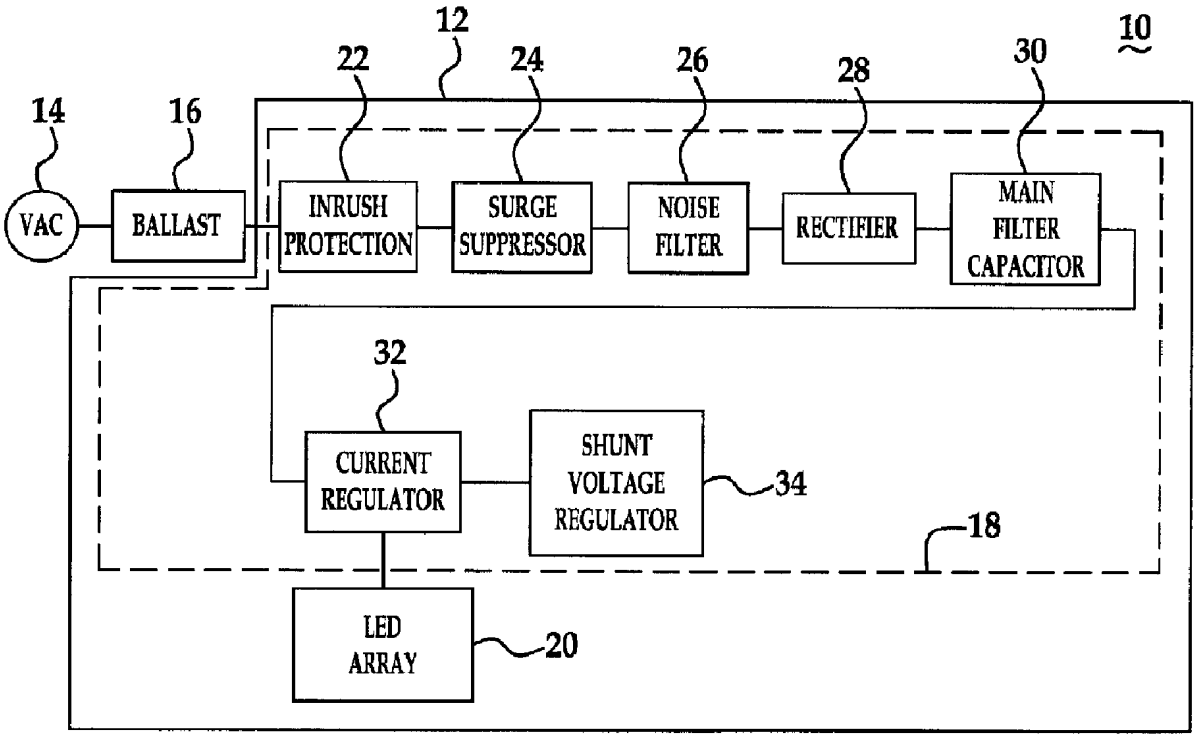


FIG. 1

(57) Abrégé/Abstract:
Embodiments of an illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast described. One illumination device includes protection circuitry configured to protect the illumination device

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(13) A1

(57) **Abrégé(suite)/Abstract(continued)**:
from the ballast current signal, a full-wave rectifier, a smoothing filter electrically coupled to the full wave rectifier, and a current regulator power circuit electrically coupled to the smoothing filter and the LEDS. The current regulator power circuit can include a first switching element configured to operate in response to a first (PWM) ON/OFF control signal; a current controller electrically coupled to a gate of the first switching element, the current controller configured to generate the first PWM control signal; and a current sense resistor electrically coupled to the first switching element and configured to sense the current through the LEDS, wherein the sensed current is fed back to the current controller.

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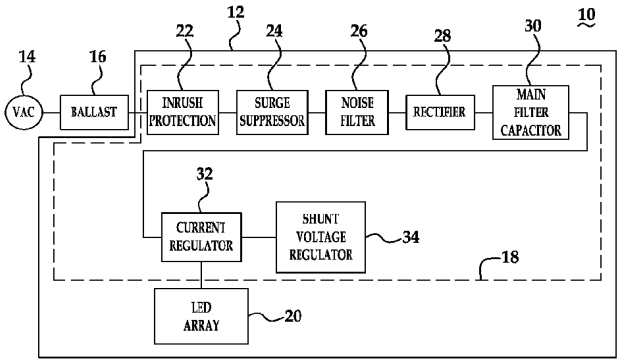


FIG. 1

(57) Abstract: Embodiments of an illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast described. One illumination device includes protection circuitry configured to protect the illumination device from the ballast current signal, a full-wave rectifier, a smoothing filter electrically coupled to the full wave rectifier, and a current regulator power circuit electrically coupled to the smoothing filter and the LEDS. The current regulator power circuit can include a first switching element configured to operate in response to a first (PWM) ON/OFF control signal; a current controller electrically coupled to a gate of the first switching element, the current controller configured to generate the first PWM control signal; and a current sense resistor electrically coupled to the first switching element and configured to sense the current through the LEDS, wherein the sensed current is fed back to the current controller.

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ELECTRONIC CIRCUIT FOR DC CONVERSION OF FLUORESCENT LIGHTING BALLAST

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Patent Application Ser. No. 12/778,632, filed May 12, 2010 and U.S. Provisional Patent Application Ser. No. 61/178,093, filed May 14, 2009, both of which are hereby incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] The present invention relates in general to LED fluorescent lamp replacements.

BACKGROUND

[0003] Fluorescent lamps are commonly installed with an additional device to regulate the voltage and current provided to the fluorescent lamp. This device, known as a ballast, can be designed to provide the proper starting voltage to establish an arc between two electrodes of the fluorescent lamp. Additionally, the ballast can designed to provide a controlled voltage to limit the amount of current to the fluorescent lamp during operation thereof. The starting and operating voltages provided by the ballast to power the fluorescent lamp can depend on, for example, the length and/or diameter of the fluorescent lamp. Accordingly, a fluorescent lamp may contain a ballast particularly designed to provide the proper starting and operating voltages.

[0004] Fluorescent lamps are gradually being replaced by light-emitting diodes (LEDs) in many applications. LEDs have many advantages over traditional fluorescent lamps in that they have, for example, longer operational life, reduced power consumption, greater durability and increased design flexibility.

[0005] Accordingly, LED replacement lamps have been developed that retrofit fluorescent lamp fixtures using existing ballasts. These LED replacements commonly contain electrical circuitry for power conversion that may not be, for example, universally compatible with any type of ballast found in existing fixtures.

SUMMARY

[0006] Embodiments of an illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast, the ballast configured to provide a current signal are disclosed herein. One such embodiment includes protection circuitry configured to protect the illumination device from the ballast current signal, a full-wave rectifier electrically coupled to the circuit protection means and configured to produce a rectified voltage output, a smoothing filter electrically coupled to the full wave rectifier and configured to produce a smoothed rectified voltage output and a current regulator power circuit electrically coupled to the smoothing filter and the LEDS. The current regulator power circuit includes a first switching element configured to operate in response to a first pulse width modulated (PWM) ON/OFF control signal, the first switching element delivering current to the LEDs in response to the ON control signal and the first switching element not delivering current to the LEDs in response to the OFF control signal. a current controller electrically coupled to a gate of the first switching element, the current controller configured to generate the first PWM control signal and a current sense resistor electrically coupled to the first switching element and configured to sense the current through the LEDS, wherein the sensed current is fed back to the current controller.

[0007] Embodiments of another illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast are disclosed herein. One such embodiment includes means for receiving a current signal from the conventional ballast and means for protecting the illumination device from the received current signal. The illumination device also includes means for rectifying the received current signal to produce a rectified voltage output and means for sensing the current through the LEDs. Further, the illumination device includes means for generating a pulse width modulated (PWM) control signal from a current control circuit based on the sensed current and means for supplying current to the LEDs in response to the PWM control signal so that the LED current reaches an average LED current.

[0008] Further, embodiments of a method of supplying power to an illumination device including LEDs and connected to an existing fluorescent lamp fixture including a conventional ballast are also disclosed herein. One such method includes receiving a current signal from the conventional ballast, protecting the illumination device from the received current signal, rectifying the received current signal to produce a rectified voltage output, sensing the current through the LEDs, generating a pulse width modulated (PWM) control

signal from a current control circuit based on the sensed current and supplying current to the LEDs in response to the PWM control signal so that the LED current reaches an average LED current.

[0009] Other embodiments of the invention are described in additional detail hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The various features, advantages and other uses of the present invention will become more apparent by referring to the following detailed description and drawing in which:

[0011] FIG. 1 is a block diagram of a light system containing a power converter in accordance with an embodiment of the invention.

[0012] FIG. 2 is a circuit schematic illustrating various components of the power converter of FIG. 1;

[0013] FIG. 3 is a circuit schematic of a current controller used in the power converter of FIG. 2;

[0014] FIG. 4 is a circuit schematic of a voltage controller used in the power converter of FIG. 2;

[0015] FIG. 5 is a circuit schematic of a voltage regulator used in the power converter of FIG. 2;

[0016] FIG. 6 is a circuit simulation waveform of an output forward voltage of an LED array along with a rectified DC voltage and a DC link voltage from the power converter of FIG. 2;

[0017] FIG. 7A is a circuit simulation waveform of switch turn-on di/dt changing as a function of a gate drive resistor value from the power converter of FIG. 2; and

[0018] FIG. 7B is a circuit simulation waveform of switch turn-on dv/dt changing as a function of a gate drive resistor value from the power converter of FIG. 2.

DETAILED DESCRIPTION

[0019] FIG. 1 is a block diagram of a light system 10 according to one embodiment of the invention. LED light system 10 can include a fixture (not shown) and an LED replacement lamp 12 powered by a signal source 14. The fixture can be, for example, an existing fluorescent lamp fixture that may have been previously used in a light system for a fluorescent lamp. According to the embodiments discussed herein, replacement lamp 12 can

be retrofitted to the existing fixture. The fixture can contain a ballast 16, which can be connected between signal source 14 and replacement lamp 12. Replacement lamp 12 can include a power converter 18 and an LED array 20. Although the embodiments will be discussed with reference to a replacement lamp that solely contains LEDs, other embodiments of light system 10 do not have to be exclusively limited to LEDs. For example, other embodiments of light system 10 may contain a replacement lamp that contains a combination a fluorescent lamp and LEDs.

[0020] Signal source 14 can be any suitable alternating current (AC) source or direct current (DC) source. For example, signal source 14 can be a 110/220 VAC single phase direct connect. As discussed previously, signal source 14 provides power to ballast 16. Ballast 16 can convert the power from signal source 14 to a power level designed to activate and operate a fluorescent lamp. Ballast 16 can be any type of ballast suitable for lighting fluorescent lamps by, for example, modifying the electrical voltage and frequency levels of signal source 14. Some non-limiting examples of ballast 16 are rapid start electronic ballasts, instant start electronic ballasts, magnetic ballasts or a hybrid containing components of both the electric and magnetic ballasts.

[0021] Power converter 18 can receive the power output from the ballast, by, for example, leads from the ballast that would have previously been connected to the lamp sockets for a fluorescent lamp. Power converter 18 can convert the power output by the ballast into power usable by and suitable for LED array 20. Power converter 18 can include an inrush protection circuit 22, a surge suppressor circuit 24, a noise filter circuit 26, a rectifier circuit 28, a main filter circuit 30, a current regulator circuit 32 and a shunt voltage regulator circuit 34. Current regulator circuit 30 can be connected to LEDs 20. As will be described in additional detail, power converter 18 is suitably designed to receive a wide range of currents and/or voltages from ballast 16.

[0022] LEDs 20 in replacement lamp 12 can include at least one LED, a plurality of series-connected or parallel- connected LEDs, or an LED array. At least one LED array can include a plurality of LED arrays. Any type of LED may be used in LEDs 20. For example, LEDs can be high-brightness semiconductor LEDs, an organic light emitting diodes (OLEDs), semiconductor dies that produce light in response to current, light emitting polymers, electro-luminescent strips (EL) or the like.

[0023] FIG. 2 is a circuit schematic of illustrating various details of power converter 18 of FIG. 1. Signal source 14 can provide, for example, an AC signal to inrush protection circuit 22. Inrush protection circuit 22 can be realized by inrush current limiters 42 and 44.

Capacitor 40 can be connected in parallel to output of the ballast 16 for filtering incoming voltage spikes. Inrush current limiter 40 can have one end connected to a common point between the output of ballast 16 and capacitor 40 for receiving the positive half cycle of the ballast output and the other end connected to surge suppressor circuit 24. Similarly, inrush current limiter 42 can have one end connected to a common point between the output of ballast 16 and capacitor 40 for receiving the negative half cycle of the ballast output and the other end connected to surge suppressor circuit 24.

[0024] When signal source 14 is initially connected, high inrush current can pass from the output of ballast 16 to components of power converter 18. High inrush currents may be moderated by placing inrush current limiters 42 and 44 in series with the current flow. In one embodiment, inrush current limiters 42 and 44 can be negative temperature coefficient (NTC) resistors. When signal source 14 is first connected, for example, NTC resistors can be cool and have a high resistance value thereby limiting inrush current. After a period of operation, NTC resistors can be warmed by current flowing therein, which in turn, can lower its resistance value. Alternate embodiments may use any other suitable inrush current limiter. One non-limiting example may be a fixed resistor or the like.

[0025] Selection of inrush current limiters 42 and 44 can be accomplished by, for example, calculating the maximum input energy the inrush current limiter will absorb when the device is turned on using equation (1):

$$E = \frac{1}{2} * C_{bus} * V_{max}^2; \text{ wherein} \quad (1)$$

E is the maximum energy rating;

C_{bus} is the amount of bus capacitance; and

V_{max} is the peak AC voltage or the maximum DC voltage.

[0026] Thus, for example, if C_{bus} is 100 μF and V_{max} is 1500v, then the maximum energy rating will be 112.5 J. Accordingly, inrush current limiters 42 and 44 can be selected to have an energy rating greater than 112.5 J. Further, the resistance of the inrush current limiter can be of a value such that components of rectifier circuit 28 are not stressed. An example of an inrush current limiter that fulfils these preferences is Ametherm Inrush Current Limiter Part No. MS22212103, which contains a maximum energy rating of 220 J and a resistance of 120 ohms at 25° C. Other suitable inrush current limiters and techniques for selecting inrush current limiters are also available.

[0027] Referring still to FIG. 2, surge suppressor circuit 24 can be realized by varistor 46. Varistor 46 is connected in parallel between inrush protection circuit 22 and noise filter circuit 42. Varistor 46 can be used to absorb high voltage transients or surges that may occur

from the output of ballast 16. Selection of varistor 46 can be accomplished by, for example, selecting a varistor that has a maximum allowable voltage no less than V_{max}, where V_{max} is the peak AC voltage or the maximum DC voltage from the output of ballast 16. In this manner, varistor 46 will not clamp as long as the voltage does not exceed V_{max}. An example of a surge suppressor that fulfils these preferences is Panasonic ZNR Transient/Surge Absorber Part No. ERZV10D182CS, which has a maximum allowable voltage of 1000 VAC_{rms} (1465 VDC). Other suitable surge suppressor devices and techniques for determining suitable surge suppressor devices are also available.

[0028] Incoming current passes through noise filter 26 to prevent noise interference from being received by power converter 18. Noise filter circuit 26 can be realized by X-class capacitor 56, Y-class capacitors 48 and 50 and discharge resistors 52, 54 and 56. Selection of the type and number of X-class capacitors can be accomplished by any suitable technique in order to, for example, pass EMC testing. One suitable technique is to select a specific capacitor, calculate the power dissipation of that capacitor and, if the calculated power dissipation for the selected capacitor is higher than the maximum allowed power dissipation for the specific capacitor, determining how many capacitors should be placed in parallel to achieve a power dissipation that is less than or equal to the maximum allowed power dissipation.

[0029] Accordingly, the RMS current of the X-class capacitor can be estimated, which as discussed in more detail below, to calculate the worst case power dissipation of X-class capacitor 56. RMS current of the X-class capacitor can be calculated using equations (2) and (3):

$$Z_c = \frac{1}{Cx \cdot 2 \cdot \pi \cdot Fb}; \text{ wherein} \qquad (2)$$

Z_c is the impedance of the X-class capacitor at the ballast switching frequency Fb;
Cx is the value of the X-class capacitor; and
Fb is the switching frequency of the ballast voltage.

$$Irms = \frac{\frac{4V\,max}{\pi \cdot \sqrt{2}}}{Z_c}; \text{ wherein} \qquad (3)$$

Irms is the RMS current for the X-class capacitor;
Vmax is the peak AC voltage or the maximum DC voltage; and
Z_c is the impedance of the X-class capacitor at the ballast switching frequency Fb.

[0030] In equation (3), Irms is found for the first harmonic of an input square wave. Alternatively, the RMS current for the X-class capacitor can be determined for a sinusoid, sawtooth or any other input waveform.

[0031] Once the type and value of X-class capacitor 56 is selected, X-class capacitor 56 can be evaluated based on its estimated power loss during operation of power converter 18 using equation (4) to determine the ESR of the X-class capacitor, equation (5) to determine the number of capacitors to place in parallel so that the power dissipation is less than the maximum allowable power dissipation and equation (6) to determine the estimated power loss of the X-class capacitor:

$$Resr = \frac{DF}{2 \cdot \pi \cdot f \cdot Cx}; \text{ wherein} \quad (4)$$

Resr is the theoretical equivalent series resistance of the X-class capacitor;

DF is the dissipation factor for the X-class capacitor;

f is the frequency at which the dissipation factor has been specified for the X-class capacitor; and

Cx is the value of the X-class capacitor.

$$n = \left| \begin{array}{l} n \leftarrow 1 \\ \quad \text{while} \left(\frac{Irms}{n} \right)^2 \cdot Resr > Pc \\ \quad n \leftarrow n + 1 \\ n \end{array} \right. \quad (5)$$

; wherein

n is the number of X-class capacitors in parallel;

Irms is the RMS current for the X-class capacitor;

Resr is the equivalent series resistance of the X-class capacitor; and

Pc is the maximum allowed power dissipation value for the X-class capacitor.

$$Pesr_{max} = \left(\frac{Irms}{n} \right)^2 \cdot Resr \text{ ; wherein} \quad (6)$$

$Pesr_{max}$ is the maximum power dissipation of an X-class capacitor;

Irms is the RMS current for an X-class capacitor;

Resr is the equivalent series resistance of an X-class capacitor; and

n is the number of X-class capacitors in parallel.

[0032] The ESR of the X-class capacitor determined by equation (4) may be different from the ESR at the operating frequency. Accordingly, the ESR at the operating frequency may be used to calculate the power dissipation of the X-class capacitor instead of the ESR of the X-class capacitor as determined by equation (4). An example of a suitable X-class capacitor 56 that can be used in noise filter 26 can have a value of 100 pF, a maximum allowed power dissipation of .25 W, and a DF of .001 at 1000 kHz. Other suitable capacitors and techniques for determining suitable capacitors for noise filter 26 are also available.

[0033] Rectifier 28 receives the filtered AC signal and outputs a rectified voltage using diodes 60, 62 64 and 66. Selection of diodes 60, 62 64 and 66 can be accomplished by, for example, selecting a type of diode that has a reverse voltage rating at least as high as Vmax so that the diode is able to withstand reverse voltages as high as the peak voltage or the maximum DC voltage . An example of a diode that fulfils these preferences is STMicroelectronics Part No. DTV1500SD, which has a maximum voltage rating of 1500V. Other suitable rectifier devices and techniques for determining suitable rectifier devices are also available.

[0034] The rectified voltage is smoothed by main filter 30, which is connected across rectifier 28. Main filter 30 can be realized electrolytic capacitor 68, 74, 80 and 86. Alternatively, main filter 30 can be realized by one or any other suitable number of capacitors. Electrolytic capacitors 68, 74, 80 and 86 act as a reservoir, supplying current to the output when the varying DC voltage from rectifier 28 is falling (i.e. resulting in a smoothed DC link voltage VDC). Selection of electrolytic capacitors can be accomplished by, for example, choosing a specific capacitor bus value (i.e. total electrolytic capacitance value) and verifying that this bus capacitance value permits the DC link voltage to be greater than the maximum LED forward voltage drop.

[0035] Referring to FIG. 6, a circuit simulation waveform 600 illustrates an example of how the selected bus capacitance value results in the DC link voltage (illustrated by a solid line 602) being greater than the maximum output forward voltage of LEDs 20 (illustrated by a dotted line 604) during both the charging and discharging of the selected bus capacitor. The point where DC link voltage and rectified output voltage (illustrated by a dashed line 606) intersect is greater than the maximum output forward voltage. If the selected bus capacitor did not begin recharging the DC link voltage, the DC link voltage would fall below the maximum output forward voltage. However, since the capacitor begins charging at the intersection point of the rising edge of the rectified output voltage, the DC link voltage does

not fall below the maximum output forward voltage of LEDs 20. Accordingly, selection of a bus capacitance value, such as 100μF, can fulfill these preferences and can also prevent the current regulator from entering discontinuous conduction mode. Other suitable bus capacitance values are also available. The maximum output forward voltage of LEDs 20, the rectified output voltage and DC link voltage can be represented using equations (7) and (8):

$$Vo_{max} = Vled_{max} \cdot Num_{leds}; \text{ wherein} \quad (7)$$

Vo_{max} is the maximum output forward voltage of the series connected LEDs;

$Vled_{max}$ is the maximum LED forward voltage drop; and

Num_{leds} is the number of series connected LEDs.

$$Vin(t, Vpk) = |Vpk \cdot \cos(\omega \cdot t)|; \text{ wherein} \quad (8)$$

Vin(t, Vpk) is the rectified output voltage;

Vpk is the peak voltage of the rectified output voltage;

ω is the fundamental frequency of the input waveform; and

t is the time.

[0036] The DC link voltage can be estimated and represented by using equations (9)-(12):

$$v_c(t) = \frac{1}{C_{bus}} \cdot \int_0^t - Idc\, dt \text{ ; wherein} \quad (9)$$

$v_c(t)$ is the DC link voltage;

C_{bus} is the bus capacitance;

Idc is the current drawn from the DC supply; and

t is the time. Finding the integral of equation (9) results in equation (10):

$$v_c(t) = \frac{-1}{C_{bus}} \cdot Idc \cdot t + C \quad (10)$$

[0037] Power converter 18 can keep constant power flowing out of the DC link voltage into LEDs 20 permitting Idc to increase as the DC link voltage decreases. Accordingly, equation (10) can also be represented as equation (11):

$$v_c(t) = \frac{1}{C_{bus}} \cdot \frac{-Po}{v_c(t)} \cdot t + C \quad (11)$$

Po is the output power of the LEDs. Solving for $v_c(t)$, results in equation (12):

$$v_c(t) = \frac{1}{2 \cdot C_{bus}} \cdot \left[C \cdot C_{bus} + \left(C^2 \cdot C_{bus}{}^2 - 4 \cdot C_{bus} \cdot Po \cdot t \right)^{\frac{1}{2}} \right] \quad (12)$$

To solve equation (12) for the constant of integration, we can approximate a worst case value for C when the initial condition (i.e. t =0) of the DC link voltage is valid from the peak of the rectified voltage Vpk, which results equation (13):

$$v_c(t) = \frac{1}{2 \cdot C_{bus}} \cdot \left[Vpk \cdot C_{bus} + \left(Vpk^2 \cdot C_{bus}^2 - 4 \cdot C_{bus} \cdot Po \cdot t \right)^{\frac{1}{2}} \right] \quad (13)$$

[0038] Once, the selected bus capacitance has been, realizable values can be selected for the capacitance. Selection of the type and number of capacitors in main filter 30 can be accomplished by any suitable technique in order to, for example, provide a DC link voltage that does not fall below the maximum output forward voltage of the LEDs 20. Preferably, capacitors should be able to sustain high voltages. By placing four capacitors 68, 74, 80 and 86 in series as shown in FIG. 2, main filter 30 can have a higher voltage rating.

[0039] However, if there is more than one capacitor in main filter capacitor 30, voltage may not be evenly distributed across each capacitor. Balancing resistors 70 and 72 can be placed in parallel with capacitor 68, balancing resistors 76 and 78 can be placed in parallel with capacitor 74, balancing resistors 82 and 84 can be placed in parallel with capacitor 80 and balancing resistors 88 and 90 can be placed in parallel with capacitor 86 so that each of the balancing resistors can assist in permitting capacitors 68 to assist capacitors 68, 74, 80 and 86 to share voltage evenly. Selection of the number and type of balancing resistors 70, 72, 76, 78, 82, 84, 88 and 90 can be accomplished by any suitable technique, such as by the resistors maximum voltage rating, and have any suitable value, such as 100kΩ.

[0040] Current regulator power section 32 applies the DC link voltage across LEDs 20. Current regulator circuit 32 can be realized by inductor 92, low-side switch 96, diode 98, capacitor 100, current controller circuit 102, a gate resistor 104, sense resistors 108, 110, 112, 114, 116, 118 and 120, feedback resistor 122 and feedback capacitor 124. One end of LEDs 20 are connected to inductor 92 while the other end of LEDs 20 are connected to low-side switch 96. Diode 98 is connected in parallel to LEDs 20 and inductor 92 and prevents reverse currents from flowing through current regulator 32. Capacitor 100 is Switch 96 is connected and connected in series Current regulator power section 32 applies the DC link voltage across to LEDs 20. Alternatively, although only one inductor is shown in the circuit, more than one inductor can be implemented in series with inductor 92.

[0041] More specifically, inductor 92, connected in series with LEDs 20, provides the charging and discharging current to LEDs 20 according to the state of switch 96. As will be discussed in more detail below, the state of switch 96 is controlled by current controller 102.

[0042] Current regulator power section 32 utilizes a buck converter topology and can operate in a continuous conduction mode to convert DC link voltage to a desired LED drive voltage while providing a desired average LED current I_L (also the average inductor current). During turn-on of switch 96, a function for current i_{Lon} can be represented using equations (14) - (16):

$$v_{Lon}(t) = Lf \cdot \frac{d}{dt} i_{Lon}(t) \text{; wherein} \quad (14)$$

t is the time;

$v_{Lon}(t)$ is the inductor voltage at time t;

Lf is the value of the inductor(s); and

$i_{Lon}(t)$ is the inductor current at time t. Taking the integral of both sides of equation (14) results in equation (15):

$$i_{Lon}(t) = \frac{1}{Lf} \cdot \int_0^t (Vin - Vo)dt \text{; wherein} \quad (15)$$

Vin is the DC link voltage; and

Vo is the output voltage for the LEDs. Vo can be calculated using equation (16):

$$Vo = Vled \cdot Num_{leds} \text{; wherein} \quad (16)$$

Vled is the LED forward voltage drop; and

Num_{leds} is the number of series connected LEDs.

[0043] Finding the integral of equation (15) results in equation (17):

$$i_{Lon}(t) = \frac{1}{Lf} \cdot (Vin - Vo) \cdot t + C \quad (17)$$

Evaluating the integration constant C at the beginning and end of the turn-on cycle of switch 96 results in two solutions as represented by equations (18) and (19):

$$i_{Lon}(0) = C = I_1 \text{; wherein} \quad (18)$$

I_1 is the minimum inductor current.

$$i_{Lon}(DTs) = C = Ipk - \frac{1}{Lf} \cdot (Vin - Vo) \cdot D \cdot Ts \text{; wherein} \quad (19)$$

D is the operational duty cycle;

Ts is the switching period of the DC-DC converter; and

Ipk is the maximum inductor current.

[0044] During turn-off of switch 96, a function for current i_{Loff} can be represented using equations (20) - (22):

$$v_{Loff}(t) = Lf \cdot \frac{d}{dt} i_{Loff}(t) \tag{20}$$

Taking the integral of both sides of equation (20) results in equation (21):

$$i_{Loff}(t) = \frac{1}{Lf} \cdot \int_0^t (-Vo)dt \tag{21}$$

Finding the integral of equation (21) results in equation (22):

$$i_{Loff}(t) = \frac{-Vo}{Lf} \cdot t + C \tag{22}$$

Evaluating the integration constant C at the beginning and end of the turn-off cycle of switch 96 results in two solutions as represented by equations (23) and (24):

$$i_{Loff}(0) = C = Ipk \tag{23}$$

$$i_{Loff}[(1-D)\cdot Ts] = C = I_1 - \left[\frac{-Vo}{Lf} \cdot (1-D)\cdot Ts\right] \tag{24}$$

[0045] An expression for the average inductor current I_L current can be represented by equation (25):

$$I_L = \frac{1}{Ts} \cdot \left[\int_0^{D\cdot Ts} i_{Lon}(t)dt + \int_0^{(1-D)\cdot Ts} i_{Loff}(t)dt\right] \tag{25}$$

Substituting equation (17) (using the integration constant from equation (18)) and equation (22) (using the integration constant from equation (24)) into equation (25) results in equation (26):

$$I_L = \frac{1}{Ts} \cdot \left[\int_0^{D\cdot Ts}\left[\frac{1}{Lf} \cdot (Vin - Vo)\cdot t + I_1\right]dt + \int_0^{(1-D)\cdot Ts}\left[\frac{-Vo}{Lf} \cdot t + I_1 - \left[\frac{-Vo}{Lf} \cdot (1-D)\cdot Ts\right]\right]dt\right]$$

(26)

Substituting Vo/Vin for the duty cycle D and solving for I_1 results in an equation (27):

$$I_1 = \frac{1}{2} \cdot \frac{2\cdot I_L \cdot Vin \cdot Lf - Vo\cdot Ts\cdot Vin + Vo^2 \cdot Ts}{Vin \cdot Lf} \tag{27}$$

Setting equation (27) equal to 0 and solving for Lf results in a value for inductor Lf that will provide inductor current operating at the boundary between discontinuous conduction mode and continuous conduction mode as represented by equation (28):

$$Lf = \frac{-1}{2} \cdot Vo \cdot Ts \cdot \frac{-Vin + Vo}{I_L \cdot Vin} \tag{28}$$

Selecting an inductor value Lf that is larger than the value calculated by equation (28) can permit current regulator 32 to provide inductor current for maintaining continuous conduction mode. In other embodiments, inductor value Lf may be selected so that current regulator 18 is in discontinuous conduction mode.

[0046] For instance, if the maximum DC link voltage Vin is 400 V, maximum output voltage for the LEDs Vo is 117 V, the desired average LED current I_L is .35 A, and the switching period of the converter T_S is .01 ms, will result in an inductor value Lf of 1200 uH. One or more inductors can be used to realize the Lf inductor value in current regulator power section 32. For example, two inductors connected in series each having a value of 750 uH can be sufficient to meet an inductor value Lf of 1200 uH. Other suitable inductor values Lf and techniques for determining suitable inductor values Lf are also available.

[0047] The average for the average current I_L from equation (25) can also be used to calculated the peak inductor current Ipk. Substituting equation (17) (using the integration constant from equation (19)) and equation (22) (using the integration constant from equation (23)) into equation (25) results in equation (29):

$$I_L = \frac{1}{Ts}\cdot\left[\int_0^{D\cdot Ts}\left[\frac{1}{Lf}\cdot(Vin - Vo)\cdot t + Ipk - \left[\frac{1}{Lf}\cdot(Vin - Vo)\cdot D\cdot Ts\right]\right]dt + \int_0^{(1-D)\,Ts}\left[\frac{-Vo}{Lf}\cdot t + Ipk\right]dt\right] \quad (29)$$

Substituting Vo/Vin for the duty cycle D and solving for Ipk results in an equation (30):

$$Ipk = \frac{1}{2}\cdot\frac{2\cdot I_L\cdot Vin\cdot Lf + Vo\cdot Ts\cdot Vin - Vo^2\cdot Ts}{Vin\cdot Lf} \quad (30)$$

[0048] When switch 96 is closed, current controller 102 monitors the current through LEDs 20 by measuring the voltage drop across sense resistors 108, 110, 112, 114, 116, 118 and 120. This current feedback IswFbk can be fed through a first order RC filter composed of feedback filter resistor 122 and feedback filter capacitor 124. A time constant τ can be calculated for the current feedback using equation (31):

$$\tau = \frac{1}{N\cdot F_c}; \text{ wherein} \quad (31)$$

N is a constant indicating the magnitude of τ as compared to the switching period of the DC-DC converter;

τ is the time constant for the current feedback; and

F_c is the switching frequency of the power converter.

In conjunction with equation (31), values for resistor 122 and capacitor 124 can be calculated using equation (32):

$$\tau = Rf \cdot Cf \quad (32)$$

[0049] After passing through feedback filter resistor 122 and feedback filter capacitor 124, current feedback is fed to current controller 102, which can provide a pulse width modulated (PWM) control signal through a gate resistor 104 to switch 96.

[0050] As illustrated in FIG. 3, current controller 102 can be realized by an IC 200 that can control the average LED current I_L by comparing the current feedback to an internal reference. In response to the current feedback, current controller 103 provides a PWM control signal through gate resistor 104 to the gate of switch 96. According to techniques such as that described in UCC3800 BiCMOS Current Mode Control ICs, which is incorporated herein in its entirety by reference, the oscillator frequency, voltage reference V5REF and compensation waveform can be configured to provide the appropriated output Vg1 for driving the gate of switch 96.

[0051] Generally, as shown in FIG. 3, the oscillator frequency can be configured to, for example, 100kHz by selecting appropriate values for a timing capacitor 202 and serially connected timing resistors 204 and 205. Timing resistors 204 and 205 can be connected between voltage reference V5REF and an RC input of IC 200. Alternatively, timing resistors may be implemented using a single resistor, multiple resistors in series, multiple resistors in parallel, or any other suitable series or parallel combination of resistors. Timing capacitor 202 can be connected between the RC input and a digital ground DGND.

[0052] For example, a sawtooth waveform can be generated by IC 200. The oscillator waveform can be generated by a ramp up waveform and a ramp down waveform represented by equations 33 and 34, respectively:

$$Vrmp_{up}(t) = Vlow_{th} + Vref \cdot \left(1 - e^{\frac{-t}{R_T \cdot C_T}}\right); \text{ wherein} \quad (33)$$

$Vrmp_{up}(t)$ is the ramp up interval;

t is the time;

$Vlow_{th}$ is the low oscillator threshold voltage;

Vref is the reference voltage V5REF;

R_T is the timing resistor; and

C_T is the timing capacitor.

$$Vdwn_{up}(t) = Vhi_{th} \cdot Vref \cdot e^{\frac{-t}{Rd \cdot C_T}}; \text{ wherein} \quad (34)$$

$Vrmp_{dwn}(t)$ is the ramp down interval;

Vhi_{th} is the high oscillator threshold voltage; and

Rd is the discharge current of the timing capacitor.

[0053] Substituting Vhi_{th} for $Vrmp_{up}(t)$ in equation (33) and solving equation (33) for time t results in the time to ramp up to the high oscillator threshold voltage as represented by equation (35):

$$t_{up}(R_t, C_T) = -\ln\left(\frac{-Vhi_{th} + Vlow_{th} + Vref}{Vref}\right) \cdot R_t \cdot C_T \text{ ; wherein} \qquad (35)$$

t_{up} is the time to ramp up to the high oscillator threshold voltage. Similarly, substituting $Vlow_{th}$ for $Vrmp_{dwn}(t)$ in equation (34) and solving equation (34) for time t results in the time to ramp down to the low oscillator threshold voltage as represented by equation (36):

$$t_{dwn}(C_T) = -\ln\left(\frac{Vlow_{th}}{Vhi_{th}}\right) \cdot Rd \cdot C_T \text{ ; wherein} \qquad (36)$$

t_{up} is the time to ramp up to the high oscillator threshold voltage.

[0054] Accordingly, from equations (33)-(36) the oscillator waveform can be represented by equation (37):

$$Vosc(t) = \begin{cases} Vrmp_{up}(t) \text{ if } t \le t_{up}(R_T, C_T) \\ Vrmp_{dwn}(t - t_{up}(R_T, C_T)) \text{ if } t \ge t_{up}(R_T, C_T) \end{cases} \text{ ; wherein} \qquad (37)$$

Vosc(t) is the oscillator waveform.

[0055] Current controller 102 can also include a slope compensation scheme for providing constant current regulation. Preferably, the slope of the oscillator waveform Vosc(t) should be constant so as to not affect the slope compensation technique. The slope compensation scheme can be realized by a transistor 206 and compensation resistor 208 to buffer the oscillator waveform generated from timing capacitor 202. Transistor 206 and compensation resistor 208 may cause the ramp up waveform $Vrmp_{up}(t)$ to have a different shape due to, for example, current gain of transistor 206. For example, still referring to FIG. 3, the altered ramp up waveform can be represented by equation (38):

$$Vrmp_{up2}(t) = -R_e \cdot \beta \cdot \frac{R_{T1} \cdot Vbe + Vbe \cdot R_{T2} - R_{T2} \cdot Vref - R_{T1} \cdot Vrmp_{up}(t)}{R_{T1} \cdot R_e \cdot \beta + R_{T1} \cdot R_{T2} + R_{T2} \cdot R_e \cdot \beta};$$

wherein (38)

$Vrmp_{up2}$ is the altered ramp up waveform as a function of time t;

R_e is the emitter resistance of transistor 206.

β is the current gain of transistor 206;

Vbe is the base-emitter voltage of transistor 206;

R_{T1} and R_{T2} are the timing resistors 204 and 205;

Vref is the reference voltage V5REF; and

$Vrmp_{up}(t)$ is the ramp up interval as a function of time t.

[0056] Preferably, the current feedback at the minimum DC link voltage $Vlink_{min}$ and maximum voltage $Vlink_{max}$ will be the same. Using, for example, superposition, feedback current can be represented by equation (39):

$$i_{I.fbk} = \frac{i_L(t) \cdot Rs \cdot Rcmp}{Rs + Rcf + Rcmp} + Vrmp_{up2}(t) \cdot \frac{Rs + Rcf}{Rs + Rcf + Rcmp}; \text{ wherein (39)}$$

$i_{I.fbk}$ is the feedback current;

$i_L(t)$ is inductor current as a function of time t;

Rs is the current sense resistor;

Rcmp is the compensation resistor;

Rf is the feedback filter resistor; and

$Vrmp_{up2}(t)$ is the altered ramp up interval waveform as a function of time t.

[0057] If the inductor value Lf calculated in equation (28) provides a peak value of current feedback that is over a preferred peak value of current feedback, such as .5 A, the value of the inductor Lf can be varied so that the peak value does not exceed this preferred value. Specifically, the peak values of the current at the minimum DC link voltage $Vlink_{min}$ and the maximum voltage $Vlink_{max}$, can be calculated using equation (30). Further, the peak ramp waveform values at the minimum DC link voltage $Vlink_{min}$ and the maximum voltage $Vlink_{max}$ can be calculated using equation (38). Accordingly, substituting these values into equation (39) can give equations for the peak feedback current at the minimum and maximum DC link voltage operating points as represented by equations (40) and (41).

$$i_{I.fbk\_pk} = \frac{i_{L\_pk1} \cdot Rs \cdot Rcmp}{Rs + Rcf + Rcmp} + Vrmp_{iLpk1} \cdot \frac{Rs + Rcf}{Rs + Rcf + Rcmp}; \text{ wherein (40)}$$

i_{Lfbk_pk} is the peak feedback current at the maximum voltage $Vlink_{max}$;

i_{L_pk1} is the peak value of the inductor current at the maximum voltage $Vlink_{max}$; and

$Vrmp_{iLpk1}$ is the peak ramp waveform value at the maximum voltage $Vlink_{max}$.

$$i_{Lfbk\_pk} = \frac{i_{L\_pk2} \cdot Rs \cdot Rcmp}{Rs + Rcf + Rcmp} + Vrmp_{iLpk2} \cdot \frac{Rs + Rcf}{Rs + Rcf + Rcmp}; \text{ wherein (41)}$$

$i_{I.fbk\_pk}$ is the peak feedback current at the minimum voltage $Vlink_{min}$;

i_{L_pk2} is the peak value of the inductor current at the minimum voltage $Vlink_{min}$; and

$Vrmp_{iLpk2}$ is the peak ramp waveform value at the minimum voltage $Vlink_{min}$.

[0058] Setting equations (40) and (41) equations equal to each other gives a peak

value of current feedback that is the same at the minimum and maximum DC link voltage operating points. From these equations, appropriate values for current sense resistor 108 (Rs) and compensation resistor 208 (Rcmp) can be determined. Power loss calculations can be performed, by assuming worst case RMS currents, for current sense resistor 108 and compensation resistor 208. However, power loss may be minimal in, for example, compensation resistor 208 so that a value, such as 7.5k, can be utilized without a power loss analysis. Other suitable compensation resistor values and techniques for selecting compensation resistor values are also available.

[0059] A realizable value and a number of resistors can be chosen for current sense resistor by determining the worst case power loss. One technique to determine the worst case power loss is to assume that the ramp waveform $Vrmp_{up2}(t)$ is not added to the feedback current. The scalar for the current can be represented by equation (42) and the limited peak current can be represented by equation (43)

$$K_{ifbk} = \frac{Rs \cdot Rcmp}{Rs + Rcf + Rcmp}; \text{ wherein} \quad (42)$$

K_{ifbk} is the scalar for the feedback current. The peak current that

$$I_{lim} = \frac{Voref_{max}}{K_{ifbk}}; \text{ wherein} \quad (43)$$

I_{lim} is the peak current limited by the maximum voltage reference in the IC current controller; and

$Voref_{max}$ is the maximum voltage reference in the in the IC current. Accordingly, the worst case power loss can be

$$P_{Rs} = \left(\sqrt{D_{max}} \cdot I_{lim}\right)^2 \cdot Rs; \text{ wherein} \quad (44)$$

P_{Rs} is the power rating for the current sense resistor Rs;

Dmax is the maximum duty cycle;

I_{lim} is the peak current. As such, a suitable number of resistors can be implemented in lieu of one current sense resistor 108 such that the power rating of current sense resistor 108 is not exceeded. For example, 7 resistors can be connected in parallel, each having a value of 2.7 Ω. Other suitable current resistor values and techniques for selecting current resistor values are also available.

[0060] UCC3800 BiCMOS Current Mode Control ICs, referenced above, also provides a technique to set up the internal current reference of IC 200. Still referring to FIG. 3, a potentiometer 210 is connected between voltage reference V5REF and DGND.

Connected in parallel to potentiometer 210 are resistors 212 and 214. Capacitor 216 is connected in parallel to resistor 214. Resistor 218 has one end connected to capacitor 216 and the other end connected to a point connecting the inverting input of the error amplifier (FB) as well as the output of the error amplifier (COMP), which is connected through capacitor 220 and resistor 222. Other suitable current resistor values and techniques for selecting current resistor values are also available.

[0061] Referring to FIG. 5, IC 200 can be powered by providing a voltage reference V12 to pin VCC by using power circuitry 400. Referring to FIG. 5, voltage reference V12 is generated through IC 401. IC 401 can be a positive voltage regulator such as Texas Instruments Part No. UA78M12. DC link voltage VDC is provided through a bias resistor 402 to create a voltage potential Vz. A zener diode 404 is connected to a point between bias resistor 402 and VIN and to one end of a resistor 406 to absorb excess voltage. The other end of resistor 406 is connected to PGND. Vz is filtered by an input filter capacitor 406 and is fed into the input of IC 401 (VIN).

[0062] VIN can also be fed from the drain-source voltage of switch 96 through a boost resistor 126. Accordingly, the drain source-voltage of switch 96 may provide the power to permit control circuits of power converter 18 to operate over a wide range. The output of IC 401 provides the voltage reference V12 filtered by an output filter capacitor 408. Other suitable techniques, components and configurations for powering IC 200 are also available.

[0063] Returning to FIG. 1, selection of switch 96 can be accomplished by, for example, estimating the maximum power loss of the switch using equation (45):

$$Ptot = Psw + Pcnd \text{ ; wherein} \quad (45)$$

Ptot is the total power loss of the switch;

Psw is the switching loss of the switch; and

Pcnd is the conduction loss of the switch. The maximum switching loss Psw of switch 96 can be calculated using equation (46):

$$Psw = Fs \cdot \left(\frac{1}{2} \cdot Vlink_{max} \cdot I_L \cdot t_r + \frac{1}{2} \cdot Vlink_{max} \cdot I_L \cdot t_f \right) \text{; wherein} \quad (46)$$

Fs is the switching frequency of the converter;

$Vlink_{max}$ is the maximum DC link voltage

I_L is the average inductor current;

t_r is the switching rise time; and

t_f is the switching fall time. Assuming that switch 96 is continuously on at the highest temperature, the maximum conduction loss Pcnd of switch 96 can be estimated using equation (47):

$$Pcnd = I_L^2 Rds_{on\_max} \text{ ; wherein} \quad (47)$$

Rds_{on_max} is the maximum resistance between the drain and the source when the switch is closed. The resistance Rds_{on_max} can also be scaled by a temperature scale factor to obtain a more accurate conduction loss Pcnd.

[0064] If switch 96 were to operate without a heatsink, the temperature rise of switch 96 due to power dissipation can be estimated using equation (48):

$$TempRise = Ptot \cdot \theta_{ja} \text{ ; wherein} \quad (48)$$

TempRise is the temperature rise of the switch; and

θ_{ja} is the junction to ambient thermal resistance of the switch. If switch 96 does not operate within its proper temperature limits, a heat sink may be used in conjunction with switch 96. If a heat sink is used, the thermal resistance of the heat sink can be estimated such that switch 96 can operate within its proper temperature limits. The thermal resistance of the heat sink can be estimated using equation (49):

$$\theta_{ca} = \frac{\Delta T}{Ptot} - \theta_{jc} \text{ ; wherein} \quad (49)$$

θ_{ca} is the case to ambient thermal resistance of the heat sink;

θ_{ja} is the junction to case thermal resistance of the switch; and

ΔT is the change between the maximum temperature of the switch and the ambient temperature.

[0065] Switch 96 may be any suitable controllable switching device such as a BJT, IGBT, standard FET, etc., that can be controlled through application of a control signal. An example of a suitable switch 96 is STMicroelectronics N-Channel Power MOSFET Part No. STFV4N150. Other suitable switching devices and techniques for determining suitable switching devices are also available.

[0066] The rise time rate of change of current di/dt and rise time rate of change of voltage dv/dt of switch 96 can change depending on the value of gate resistor 104. Equation (50) represents an estimation of turn-on di/dt:

$$didt_{on} = \frac{Id}{t_{rsw}} \text{ ; wherein} \quad (50)$$

$didt_{on}$ is the rise time rate of change of current of the switch;

Id is the load current during the switching time test circuit; and

t_{rsw} is the rise time scaled by the gate resistor value. The rise time scaled by the gate resistor value t_{rsw} can be calculated using equation (51):

$$t_{rsw} = \frac{R}{Rg_{avg}} \cdot t_r \text{; wherein} \quad (51)$$

R is the gate resistor value;

t_r is the rise time of the switch;

Rg_{avg} is the minimum average resistor value to achieve the rise and fall times of the switch. The minimum average resistor value Rg_{avg} can be calculated using equation (52):

$$Rg_{avg} = \frac{\frac{Vgs - Vgs_{th}}{\frac{Qgs}{t_r}} + \frac{Vgs - Vgs_{th}}{\frac{Qgs}{t_f}}}{2} \text{; wherein} \quad (52)$$

Vgs is the gate to source voltage of the switch;

Vgs_{th} is the gate to source threshold voltage of the switch;

Qgs is the gate to source charge of the switch;

t_r is the rise time of the switch; and

t_f is the fall time of the switch.

[0067] The rise time rate of change of voltage dv/dt of switch 96 can be estimated using equation (53):

$$dvdt_{on} = \frac{Vdd \cdot 80\%}{t_{rsw}} \text{; wherein} \quad (53)$$

$dvdt_{on}$ is the rise time rate of change of voltage of the switch;

Vdd is the DC link voltage during the switching time test circuit; and

t_{rsw} is the rise time scaled by the gate resistor value (as calculated by equation (51)).

[0068] FIGS. 7A and 7B illustrate di/dt and dv/dt, respectively, as a function of different values of gate resistor 104. Preferably, a value for gate resistor 104 is chosen so that both di/dt and dv/dt are relatively constant. Gate resistor 104 may be implemented using a single resistor, multiple resistors in series, multiple resistors in parallel, or any other suitable series or parallel combination of resistors. For example, gate resistor may be implemented using a combination of two 100 ohm resistors. Other suitable gate resistor values and techniques for selecting gate resistor values are also available.

[0069] A shunt voltage regulator circuit 34 is optionally coupled in parallel to the current regulator power section 31. Shunt voltage regulator 34 as shown clamps the DC link voltage VDC so it does not exceed, for example, a maximum DC link voltage $Vlink_{max}$. The voltage clamping can be accomplished by, for example, PWM of a power switch 130 to provide a controllable power loss in a shunt regulator load 132 (e.g. one or more resistors). In other words, shunt voltage regulator 34 draws increasing current from the ballast 16 through the rectifier 28 and main filter capacitor 30 and wastes that power in the shunt regulator load 132if the voltage exceeds a preset value. This prevents the output voltage from the ballast 16 from rising excessively by having an amount of power dissipation. Accordingly, the operating point (e.g. 120 V) of light 10 can be controlled based on the impedance of shunt regulator load 132.

[0070] As one non-limiting example, the normal operating point of replacement lamp 30 can be around 120V and 220mA. Of course, other replacement lamps can operate at different operating points. When replacement lamp 30 is operating from ballast 34, the power in lamp 30 increases as the current in lamp 30 decreases, and vice versa, because the operating point voltage of lamp 30 is below the maximum power point of the ballast.

[0071] A first end of shunt regulator load 132 is connected to the cathode of recirculation diode 98 the second end of shunt regulator load 132 is connected to a first end of power switch 130. The second end of power switch 130 is connected to PGND. Further, a recirculation diode 134 is connected in parallel to shunt regulator load 132. While shunt voltage regulator 34 functions in part to protect components from high voltages, it also causes power dissipation through a shunt regulator load 132. The resistance of shunt regulator load can be calculated by using equation (54):

$$Rload = \frac{Vlink_{max}^{2}}{Po_{max}}; \text{ wherein} \qquad (54)$$

$Vlink_{max}$ is the maximum DC link voltage; and

Po_{max} is the maximum output power of the LEDs. Shunt regulator load 132 may be implemented with one resistor, multiple resistors in series, multiple resistors in parallel, or any other suitable series or parallel combination of resistors.

[0072] A voltage controller 136 provides a PWM control signal through gate resistor 138 to the gate of switch 130. A suitable value for gate resistor 138 can be determined by using techniques similar to that described in connection with gate resistor 104 of current controller 102. Further, the type of switch 130 can be chosen using techniques similar to that

described in connection with switch 96 of current controller 102. Although gate resistor 138 is shown as one resistor, gate resistor may be implemented multiple resistors in series, multiple resistors in parallel, or any other suitable series or parallel combination of resistors.

[0073] The embodiments of the present invention are not limited to shunt voltage regulator circuit 34. For example, a linear regulator in the form of an integrated circuit can be used in lieu of or in addition to shunt voltage regulator circuit 34. Of course, other regulator circuits are also available.

[0074] Referring to FIG. 4, voltage controller 136 can be realized by an IC 300 that can control the voltage to shunt regulator load 32. The DC link voltage VDC is fed into a resistor divider network, which can include resistors 304 and 306. Each resistors 304 and 306 may be implemented by any suitable number of resistors and may be in any suitable series or parallel configuration. For example, six resistors can be serially and parallely connected in lieu of one resistor 304 so that the power rating of each of the resistors is not exceeded. A filtering capacitor is connected in parallel to resistor 306, each having one end connected to ground. At the opposing end of capacitor 308 is connected to the inverting input of the error amplifier (FB).the ends of capacitor. The opposing end of capacitor 308 is also connected to the output of the error amplifier (COMP), which is connected through a capacitor 310 in parallel with a resistor 312 connected in series with a capacitor 314.

[0075] The oscillator frequency can be configured to, for example, 100kHz by selecting appropriate values for a timing resistors 316. Timing resistor 316 can be connected between RT and GND. Timing capacitor 202 can be connected between the RC input and a digital ground DGND.

[0076] IC 200 can be receive power (VCC) similar to the techniques described above in connection with IC 200 of FIG. 3. The short-circuit protection pin (SCP) and dead-time control pin (DTC) can be grounded.

[0077] The output driver may not have enough drive capability to supply the proper gate drive through gate resistor 138 to the gate of switch 130. Accordingly, an optional driver IC 402 can be connected to the output of IC 300 (OUT) to supply a suitable gate voltage drive. One suitable driver is Texas Instruments Mosfet Driver Part No. TPS2829. Other suitable drivers are also available.

[0078] While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiments but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope

of the appended claims, which scope is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures as is permitted under the law.

What is claimed is:

1. An illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast, the ballast configured to provide a current signal, the illumination device comprising:

protection circuitry configured to protect the illumination device from the ballast current signal;

a full-wave rectifier electrically coupled to the circuit protection means and configured to produce a rectified voltage output;

a smoothing filter electrically coupled to the full wave rectifier and configured to produce a smoothed rectified voltage output; and

a current regulator power circuit electrically coupled to the smoothing filter and the LEDS, the current regulator power circuit including:

a first switching element configured to operate in response to a first pulse width modulated (PWM) ON/OFF control signal, the first switching element delivering current to the LEDs in response to the ON control signal and the first switching element not delivering current to the LEDs in response to the OFF control signal;

a current controller electrically coupled to a gate of the first switching element, the current controller configured to generate the first PWM control signal; and

a current sense resistor electrically coupled to the first switching element and configured to sense the current through the LEDS, wherein the sensed current is fed back to the current controller.

2. The illumination device of claim 1, further comprising:

a load resistor; and

a shunt voltage regulator circuit electrically coupled to the current regulator power circuit and the load resistor and configured to dissipate power through the load resistor when the rectified output voltage is greater than a maximum voltage.

3. The illumination device of claim 2, wherein the shunt voltage regulator circuit further comprises:

a second switching element configured to operate in response to a second pulse width modulated (PWM) ON/OFF control signal, the second switching element delivering voltage to the load resistor in response to the ON control signal and the second

switching element not delivering voltage to the load resistor in response to the OFF control signal; and

a voltage controller electrically coupled to a gate of the second switching element, the voltage controller configured to generate the second PWM control signal; and

4. The illumination device of any of claims 1 to 3, wherein the protection circuitry comprises at least one of:

an inrush protection circuit configured to limit inrush current from the ballast; and

a surge suppressor configured to suppress ballast voltage from the ballast.

5. The illumination device of any of claims 1 to 3, wherein the smoothing filter comprises:

at least one capacitor;

at least one discharge resistor electrically coupled in parallel to the at least one capacitor.

6. The illumination device of any of claims 1 to 3, wherein the current regulator power circuit further comprises:

at least one inductor in series with the LEDs.

7. The illumination device of claim 6, wherein the current regulator power circuit further comprises:

a recirculation diode electrically coupled in parallel with the at least one inductor and the LEDs.

8. A method of supplying power to an illumination device including LEDs and connected to an existing fluorescent lamp fixture including a conventional ballast, the method comprising:

receiving a current signal from the conventional ballast;

protecting the illumination device from the received current signal;

rectifying the received current signal to produce a rectified voltage output;

sensing current through the LEDs;

generating a pulse width modulated (PWM) control signal from a current control circuit based on the sensed current; and

supplying current to the LEDs in response to the PWM control signal so that the LED current reaches an average LED current.

9. The method of claim 1, wherein the average LED current is determined based on the rectified voltage output and an output voltage of the LEDs.

10. The method of claims 1 or 2, wherein the PWM control signal is supplied to a switching element.

11. The method of claims 1 or 2, further comprising:

regulating the voltage in the illumination device so that the rectified voltage output does not exceed a maximum rectified voltage.

12. The method of claims 1 or 2, wherein protecting the illumination device further comprises at least one of:

limiting the current received from the conventional ballast; and

suppressing ballast voltage from the conventional ballast.

13. The method of claims 1 or 2, further comprising:

filtering the rectified current signal.

14. An illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast, the illumination device comprising:

means for receiving a current signal from the conventional ballast;

means for protecting the illumination device from the received current signal;

means for rectifying the received current signal to produce a rectified voltage output;

means for sensing the current through the LEDs;

means for generating a pulse width modulated (PWM) control signal from a current control circuit based on the sensed current; and

means for supplying current to the LEDs in response to the PWM control signal so that the LED current reaches an average LED current.

15. The illumination device of claim 14, further comprising:

means for dissipating excess power through a load resistor when the rectified output voltage is greater than a maximum voltage.

16. The illumination device of claims 14 or 15, further comprising:

means for filtering the rectified current signal.

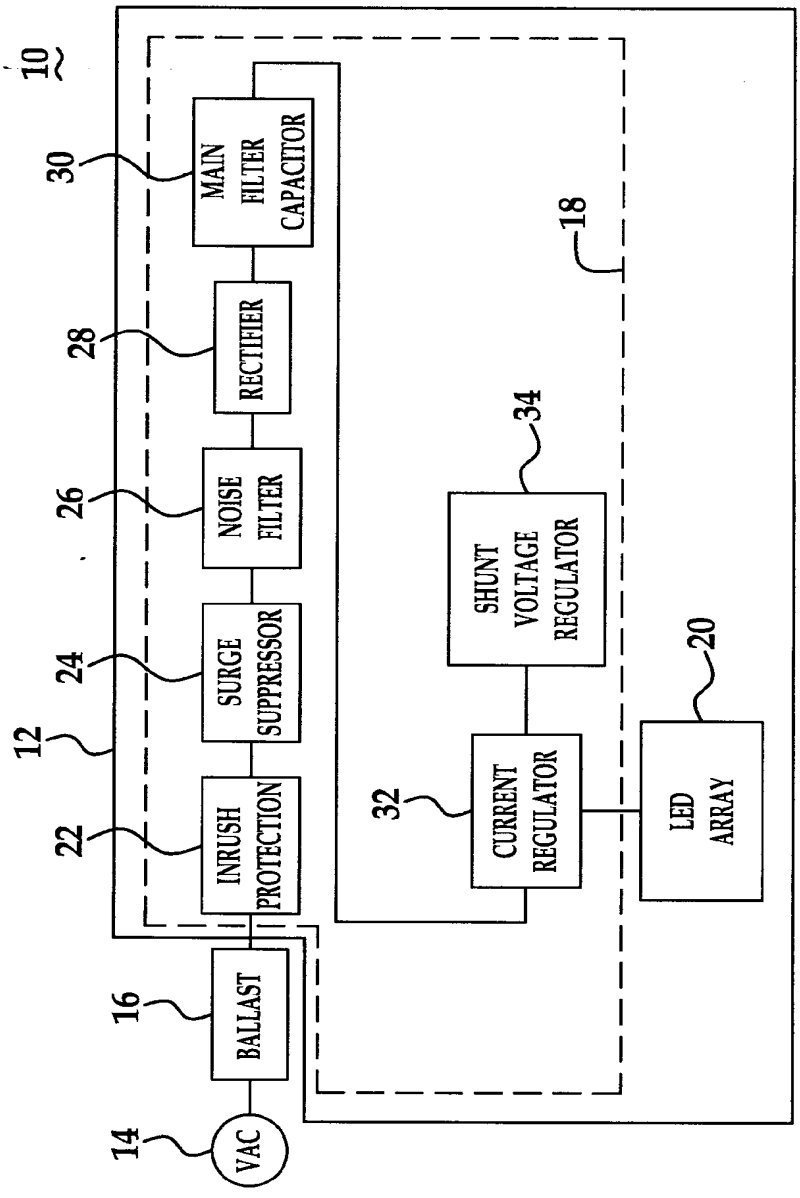

10
30
MAIN FILTER CAPACITOR
28
RECTIFIER
26
NOISE FILTER
24
SURGE SUPPRESSOR
12
22
INRUSH PROTECTION
16
BALLAST
14
VAC
18
34
SHUNT VOLTAGE REGULATOR
32
CURRENT REGULATOR
20
LED ARRAY

FIG. 1

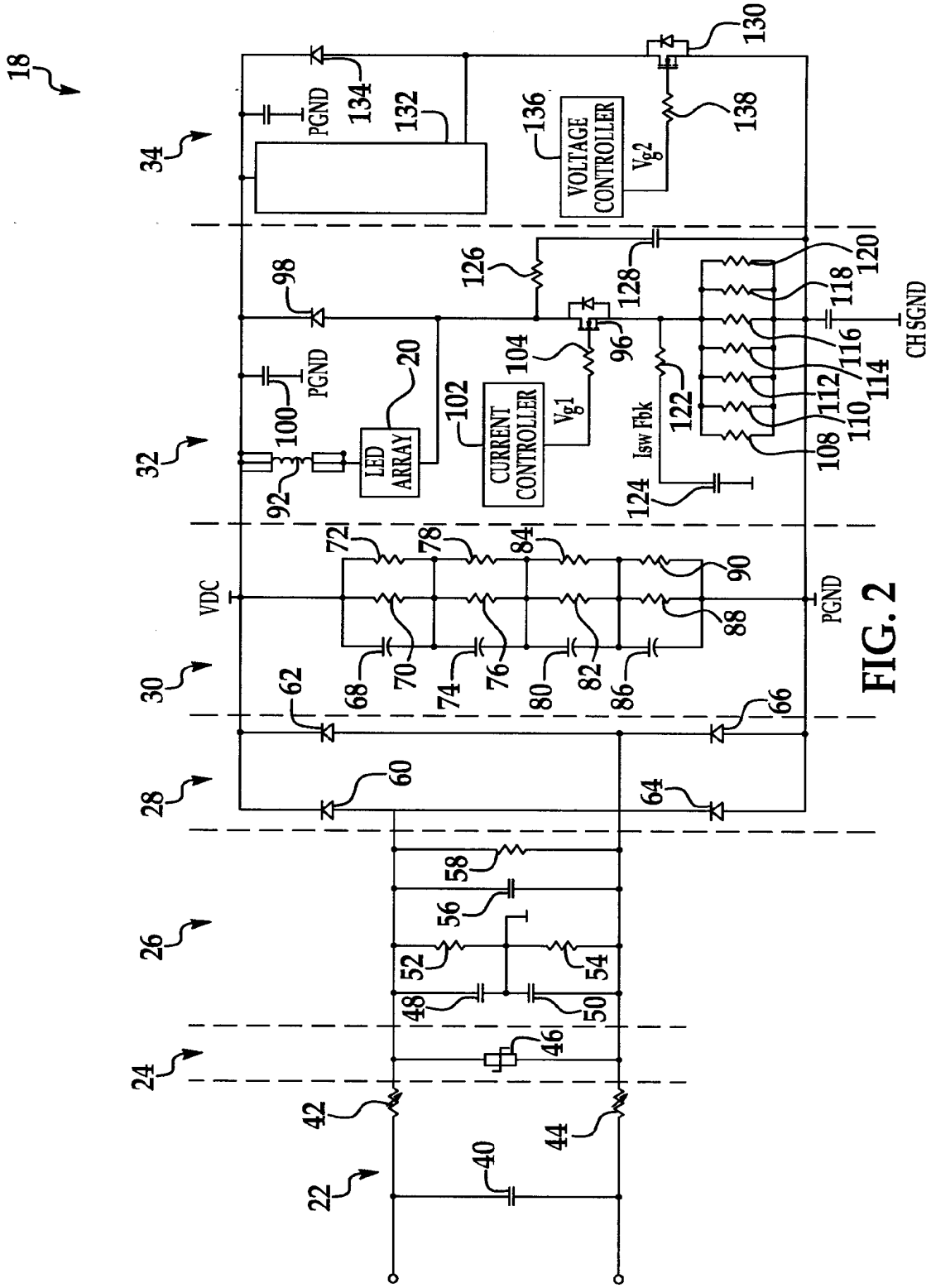

18
34
32
30
28
26
24
22
PGND
134
132
136
VOLTAGE CONTROLLER
V_g2
138
130
98
126
128
120
118
116
114
112
110
108
CH SGND
PGND
100
92
LED ARRAY
20
102
CURRENT CONTROLLER
104
V_g1
96
Isw Fbk
122
124
VDC
72
78
84
90
88
PGND
68
70
74
76
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66
60
64
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52
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46
42
44
40

FIG. 2

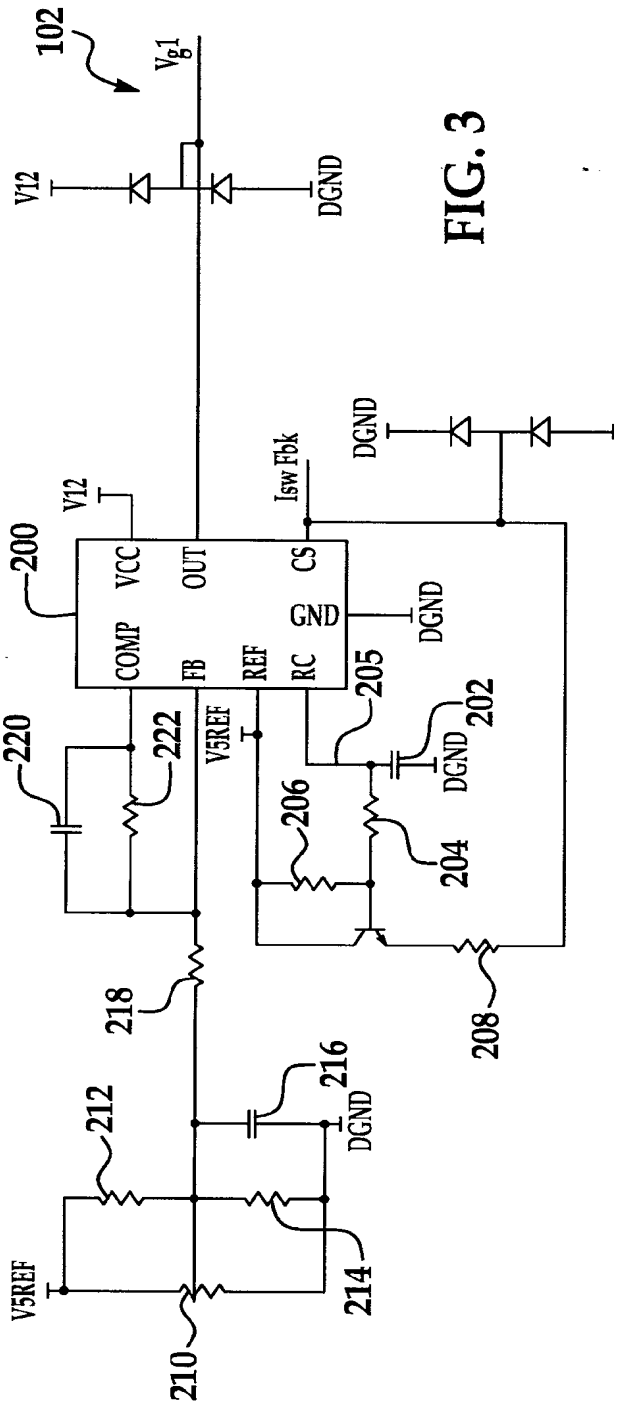

102
Vg1
V12
DGND
200
VCC
OUT
CS
GND
COMP
FB
REF
RC
Isw Fbk
205
202
206
204
208
220
222
V5REF
218
212
216
214
210

FIG. 3

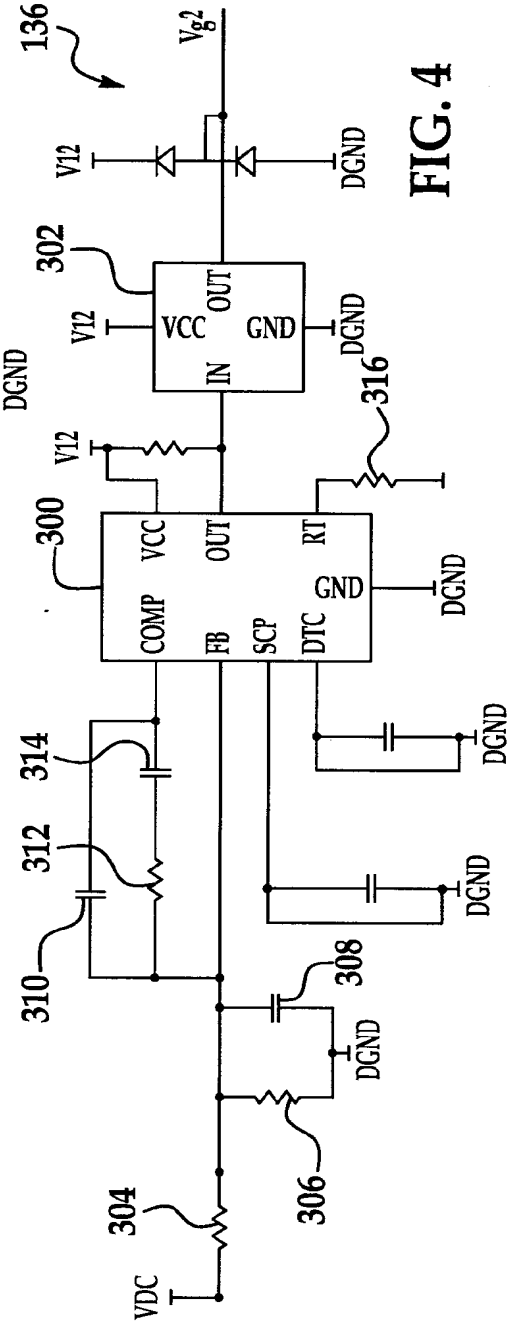

136
Vg2
V12
DGND
302
VCC
OUT
GND
IN
316
300
VCC
OUT
RT
GND
COMP
FB
SCP
DTC
314
312
310
308
306
304
VDC

FIG. 4

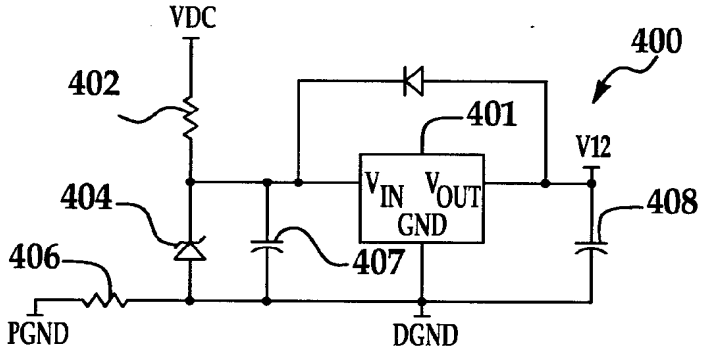

VDC
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402
401
V12
404
V_{IN} V_{OUT}
GND
408
406
407
PGND
DGND

FIG. 5

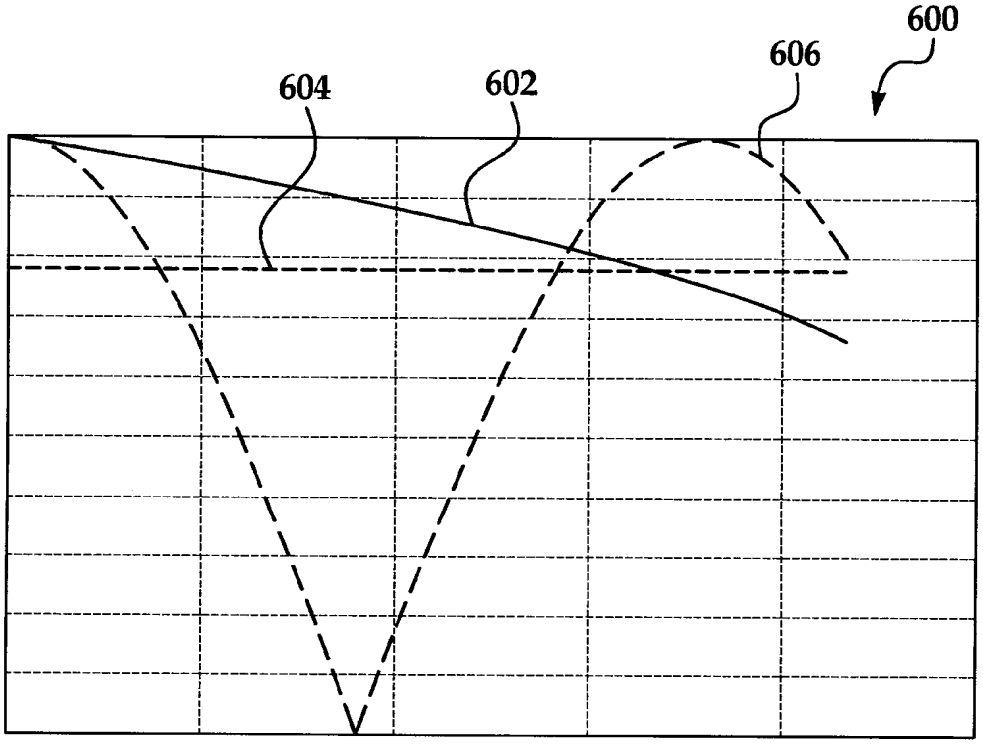

600
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FIG. 6

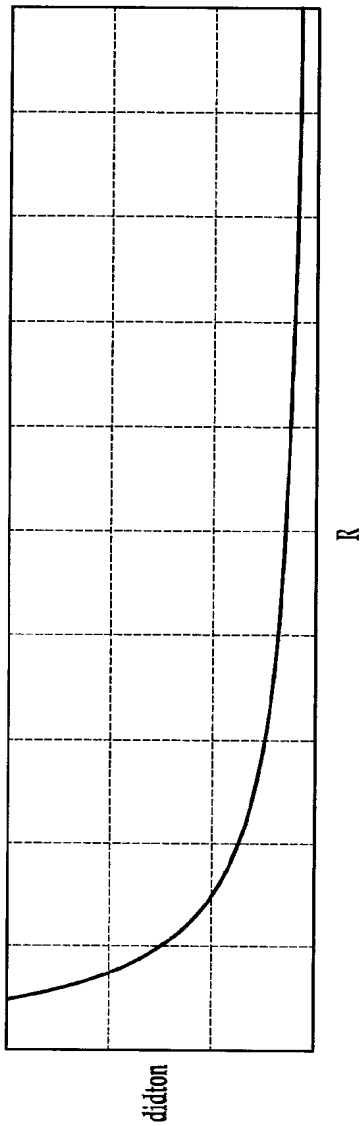


FIG. 7A

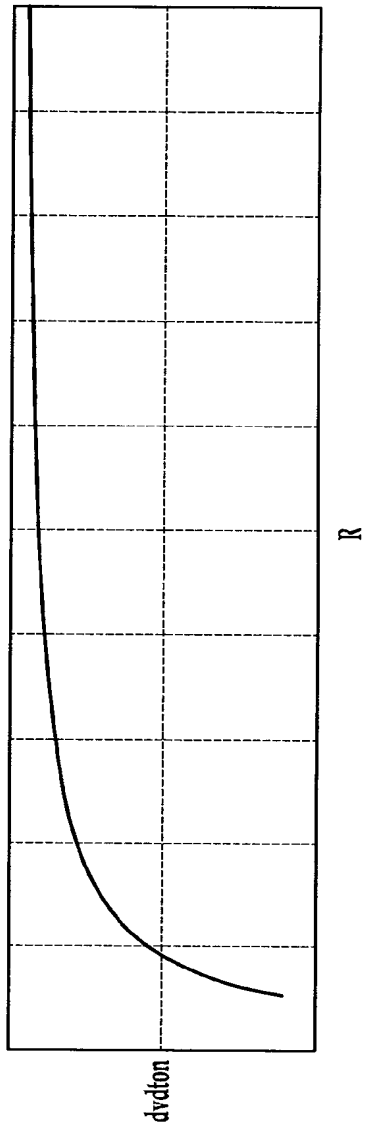


FIG. 7B

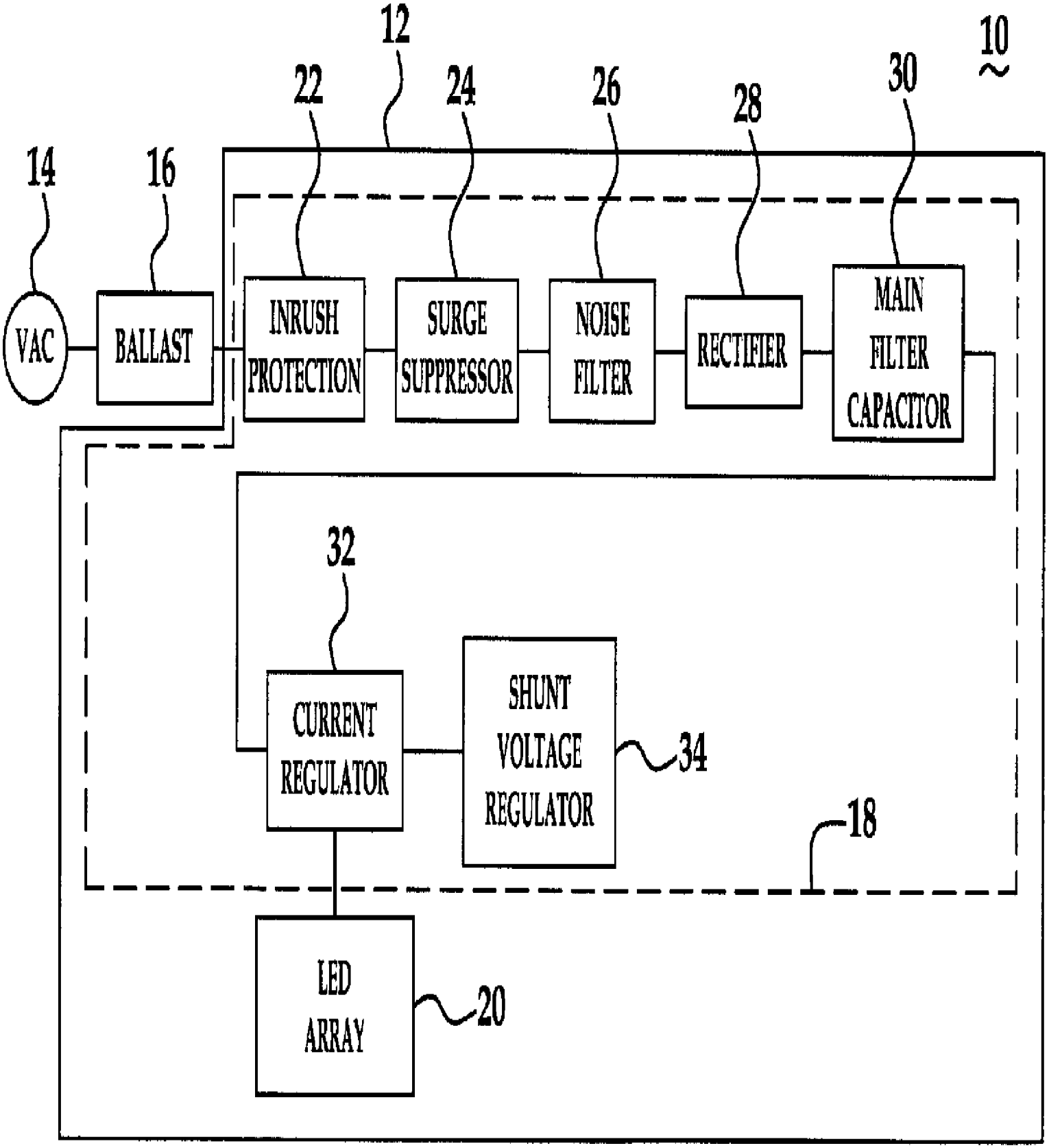

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VAC
BALLAST
INRUSH PROTECTION
SURGE SUPPRESSOR
NOISE FILTER
RECTIFIER
MAIN FILTER CAPACITOR
32
CURRENT REGULATOR
SHUNT VOLTAGE REGULATOR
34
18
LED ARRAY
20

FIG. 1

Electronic Acknowledgement Receipt

EFS ID:	25008237
Application Number:	14893375
International Application Number:	
Confirmation Number:	6653
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001051WOUS
Receipt Date:	24-FEB-2016
Filing Date:	23-NOV-2015
Time Stamp:	14:39:48
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	K8001051WOUS-IDS.pdf	1056194 49dc53c046bd88c9f2f139614f2aeb9bc0999334	no	4
Warnings:					
Information:					

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.

2	Other Reference-Patent/App/Search documents	K8001051WOUS-SR.pdf	280600 25a4b5cb0becc0627bbe66c6c52bfc33df897550	no	7
Warnings:					
Information:					
3	Foreign Reference	CA2273324.pdf	1182518 8976ef70fea2c8e64d4e8178f9b8f6f533c330dc	no	27
Warnings:					
Information:					
4	Foreign Reference	CA2742843C.pdf	745619 be88616680b5a687aad6c52b2c9e5f8ee1595861	no	18
Warnings:					
Information:					
5	Foreign Reference	CA2761294A1.pdf	1304428 d4080375d3f352c75d405f3b1b1ace05d99fc925	no	36
Warnings:					
Information:					
		Total Files Size (in bytes):	4569359		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/893,375

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	480
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	21 minus 20 =	* 1			OR	x 80 =	80
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1560

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/893,375	11/23/2015		1560	K8001051WOUS	21	2

CONFIRMATION NO. 6653

FILING RECEIPT

34236
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

OC000000080115934

Date Mailed: 01/28/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

David TIKKANEN, Waterloo, ON, CANADA;
Kyle HATHAWAY, Kitchener, ON, CANADA;

Applicant(s)

LUMASTREAM CANADA ULC, Calgary, AB, CANADA;

Power of Attorney: The patent practitioners associated with Customer Number 34236

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/CA2014/050609 06/25/2014
which claims benefit of 61/838,965 06/25/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/26/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/893,375**

Projected Publication Date: 05/05/2016

Non-Publication Request: No

Early Publication Request: No
Title

APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

Substitute for Form PTO-1360
(For use with Form PTO/SB/06)

Application Number	Filing Date
14893375	

Applicant(s) David TIKKANEN

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT	
	Indep	Depend	Indep	Depend	Indep	Depend
1	1					
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Total Indep	2		0		0	
Total Depend	19	↵	0	↵	0	↵
Total Claims	21		0		0	

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	Indep	Depend	Indep	Depend	Indep	Depend
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U.S. APPLICATION NUMBER NO.	FIRST NAMED INVENTOR	ATTY. DOCKET NO.
14/893,375	David TIKKANEN	K8001051WOUS

34236
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

INTERNATIONAL APPLICATION NO.	
PCT/CA2014/050609	
I.A. FILING DATE	PRIORITY DATE
06/25/2014	06/25/2013

CONFIRMATION NO. 6653
371 ACCEPTANCE LETTER

OC000000080115935

Date Mailed: 01/28/2016

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office, in its capacity as a Designated / Elected Office (37 CFR 1.495), has ACCEPTED the above identified international application for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above. A Filing Receipt will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE "FILING DATE or 371(c) DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1) and (c)(2) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN BELOW.** The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363)

11/23/2015
DATE OF RECEIPT OF 35 U.S.C.
371(c)(1) and (c)(2) REQUIREMENTS

The following items have been received:

- Copy of the International Application filed on 11/23/2015
- Copy of the International Search Report filed on 11/23/2015
- Inventor's Oath or Declaration filed on 11/23/2015
- U.S. Basic National Fees filed on 11/23/2015
- Priority Documents filed on 11/23/2015
- Power of Attorney filed on 12/16/2015
- Application Data Sheet (37 CFR 1.76) filed on 11/23/2015

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

MARILYN J YOUNGER

Telephone: (571) 272-8183

FORM PCT/DO/EO/903 (371 Acceptance Notice)

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
14/893,375	2015-11-23

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 34236

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Lumastream Canada ULC

☐ Inventor or Joint Inventor (title not required below)
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	David Tikkanen	Date (Optional)	Dec 7/2015
Name	DAVID TIKKANEN		
Title	Vice President		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	24383956
Application Number:	14893375
International Application Number:	
Confirmation Number:	6653
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001051WOUS
Receipt Date:	16-DEC-2015
Filing Date:	
Time Stamp:	16:29:46
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	K8001051WOUS-POA.pdf	186763 86356b982e9883877cb0cee9539d3ba4856 2410c	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	186763

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO-1390 (06-13)
Approved for use through 6/30/2013. OMB 0651-0021
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371

Attorney Docket No.	U.S. Application No. (if known, see 37 CFR 1.5)
K8001051WOUS	

International Application No.	International Filing Date	Priority Date Claimed
PCT/CA2014/050609	2014-06-25	2013-06-25

Title of Invention
APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

First Named Inventor
TIKKANEN, David

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). NOTE: The express request under 35 U.S.C. 371(f) will not be effective unless the requirements under 35 U.S.C. 371(c)(1), (2), and (4) for payment of the basic national fee, copy of the International Application and English translation thereof (if required), and the oath or declaration of the inventor(s) have been received.
2. ☐ A copy of the International Application (35 U.S.C. 371(c)(2)) is attached hereto (not required if the International Application was previously communicated by the International Bureau or was filed in the United States Receiving Office (RO/US)).
3. An English language translation of the International Application (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
4. An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4))
   a. ☑ is attached.
   b. ☐ was previously filed in the international phase under PCT Rule 4.17(iv).

Items 5 to 8 below concern amendments made in the international phase.

PCT Article 19 and 34 amendments

5. ☐ Amendments to the claims under PCT Article 19 are attached (not required if communicated by the International Bureau) (35 U.S.C. 371(c)(3)).
6. ☐ English translation of the PCT Article 19 amendment is attached (35 U.S.C. 371(c)(3)).
7. ☐ English translation of annexes (Article 19 and/or 34 amendments only) of the International Preliminary Examination Report is attached (35 U.S.C. 371(c)(5)).

Cancellation of amendments made in the international phase

8a. ☐ Do not enter the amendment made in the international phase under PCT Article 19.

8b. ☐ Do not enter the amendment made in the international phase under PCT Article 34.

NOTE: A proper amendment made in English under Article 19 or 34 will be entered in the U.S. national phase application absent a clear instruction from applicant not to enter the amendment(s).

The following items 9 to 17 concern a document(s) or information included.

9. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
10. ☐ A preliminary amendment.
11. ☑ An Application Data Sheet under 37 CFR 1.76.
12. ☐ A substitute specification. NOTE: A substitute specification cannot include claims. See 37 CFR 1.125(b).
13. ☐ A power of attorney and/or change of address letter.
14. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.3 and 37 CFR 1.821-1.825.
15. ☐ Assignment papers *(cover sheet and document(s))*. Name of Assignee: _____
16. ☐ 37 CFR 3.73(c) Statement *(when there is an Assignee)*.

This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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U.S. APPLN. No. (if known – see 37 CFR 1.5)	INTERNATIONAL APPLICATION No.	ATTORNEY DOCKET No.

17. ☐ Other items or information:

The following fees have been submitted.	CALCULATIONS	PTO USE ONLY
18. ☑ Basic national fee (37 CFR 1.492(a)) **$280**	$ 280	
19. ☑ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** All other situations **$720**	$ 720	
20. ☑ Search fee (37 CFR 1.492(b)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority ..... **$120** International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB ..... **$480** All other situations **$600**	$ 480	
TOTAL OF 18, 19, and 20 =	$ 1480	
☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)). Fee for each additional 50 sheets of paper or fraction thereof **$400**		

Total Sheets	Extra Sheets	Number of each addition 50 or fraction thereof (round **up** to a whole number)	RATE	
- 100 =	/ 50 =		x **$400**	$

Surcharge of **$140.00** for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	21 - 20 =	1	x **$80**	$ 80	
Independent claims	- 3 =		x **$420**	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$780**	$	
Processing fee of **$140.00** for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). +				$	
TOTAL OF ABOVE CALCULATIONS =				$ 1560	
☐ **Applicant asserts small entity status.** See 37 CFR 1.27. Fees above are reduced by ½.					
☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Fees above are reduced by ¾. Applicant must attach form PTO/SB/15A or B or equivalent.					
TOTAL NATIONAL FEE =				$ 1560	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property. +				$	
TOTAL FEES ENCLOSED =				$ 1560	
				Amount to be refunded:	$
				Amount to be charged:	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☑ Please charge my Deposit Account No. 501613 in the amount of $ 1865 to cover the above fees.

c. ☑ The Director is hereby authorized to charge additional fees which may be required, or credit any overpayment, to Deposit Account No. 501613 as follows:

i. ☑ any required fee.

ii. ☐ any required fee except for excess claims fees required under 37 CFR 1.492(d) and (e) and multiple dependent claim fee required under 37 CFR 1.492(f).

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. The PTO-2038 should only be mailed or faxed to the USPTO. However, when paying the basic national fee, the PTO-2038 may NOT be faxed to the USPTO.

ADVISORY: If filing by EFS-Web, do **NOT** attach the PTO-2038 form as a PDF along with your EFS-Web submission. Please be advised that this is **not** recommended and by doing so your **credit card information may be displayed via PAIR**. To protect your information, it is recommended to pay fees online by using the electronic payment method.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File)Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013, and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE 1: By providing this statement under 37 CFR 1.55 or 1.78, **this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA**.

NOTE 2: A U.S. national stage application may not claim priority to the international application of which it is the national phase. The filing date of a U.S. national stage application is the international filing date. See 35 U.S.C. 363.

Correspondence Address

☑ The address associated with Customer Number: 34236 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone			
Email					

Signature	/Jeffrey W. Wong/	Date	2015-11-23
Name (Print/Type)	Jeffrey W. Wong	Registration No. (Attorney/Agent)	46414

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ▩ United States application or PCT international application number PCT/CA2014/050609 filed on 2014-06-25.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Kyle HATHAWAY Date (Optional): Nov. 19/2015

Signature: [signature]

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number PCT/CA2014/050609 filed on 2014-06-25.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

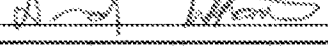
I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: David TIKKANEN Date (Optional): Nov. 19/2015

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Filer:	Jeffrey Wong/Christopher Kreider
Attorney Docket Number:	K8001051WOUS

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
National Stage Fee	1631	1	280	280
Natl Stage Search Fee - Report provided	1642	1	480	480
National Stage Exam - all other cases	1633	1	720	720
Pages:				
Claims:				
Claims in excess of 20	1615	1	80	80
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1560**

Electronic Acknowledgement Receipt

EFS ID:	24165926
Application Number:	14893375
International Application Number:	PCT/CA2014/050609
Confirmation Number:	6653
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001051WOUS
Receipt Date:	23-NOV-2015
Filing Date:	
Time Stamp:	16:25:57
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1560
RAM confirmation Number	3535
Deposit Account	501613
Authorized User	WONG, JEFFREY W.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. 1.492 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	K8001051WOUS-ADS.pdf	1819418 9ebde6774da7a5cfb41aef01272e776d2641f701	no	7
Warnings:					
Information:					
2	Transmittal of New Application	K8001051WOUS-Transmittal.pdf	1524792 0953ac3c976cf1c07b4c086e0757002025c3f612	no	3
Warnings:					
Information:					
3	Oath or Declaration filed	K8001051WOUS-Decs.pdf	730203 463711e7eb1766f0b27d76bc0cca1e1fa8729cd0	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	37002 4a971d3486328d73264bce3f383badc63094859a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	4111415		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	K8001051WOUS
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	David		TIKKANEN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Waterloo	Country of Residence [i]	CA

Mailing Address of Inventor:

Address 1	194 Silverwood Place		
Address 2			
City	Waterloo	State/Province	ON
Postal Code	N2T 2R9	Country [i]	CA

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kyle		HATHAWAY	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Kitchener	Country of Residence [i]	CA

Mailing Address of Inventor:

Address 1	5 Norbert Place		
Address 2			
City	Kitchener	State/Province	ON
Postal Code	N2K 1E5	Country [i]	CA

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	K8001051WOUS
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ **An Address is being provided for the correspondence Information of this application.**			
Customer Number	34236		
Email Address	waterloo.ip@gowlings.com	Add Email	Remove Email

Application Information:

Title of the Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES		
Attorney Docket Number	K8001051WOUS	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	9	**Suggested Figure for Publication (if any)**	1a

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	34236		

PTO/AIA/14 (07-14)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	K8001051WOUS
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	PCT/CA2014/050609	2014-06-25
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/CA2014/050609	Claims benefit of provisional	61838965	2013-06-25

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	K8001051WOUS
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	K8001051WOUS
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee ( ) Legal Representative under 35 U.S.C. 117 ( ) Joint Inventor

( ) Person to whom the inventor is obligated to assign. ( ) Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	LUMASTREAM CANADA ULC		
Mailing Address Information For Applicant:			
Address 1	400-3rd Avenue S.W.		
Address 2			
City	Calgary	**State/Province**	AB
Country [i]	CA	Postal Code	T2P 4H2
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. [ ]

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	K8001051WOUS
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Jeffrey W. Wong/			Date (YYYY-MM-DD)	2015-11-23
First Name	Jeffrey W.	Last Name	Wong	Registration Number	46414

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371

Attorney Docket No.	U.S. Application No. (if known, see 37 CFR 1.5)
K8001051WOUS	

International Application No.	International Filing Date	Priority Date Claimed
PCT/CA2014/050609	2014-06-25	2013-06-25

Title of Invention
APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

First Named Inventor
TIKKANEN, David

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). NOTE: The express request under 35 U.S.C. 371(f) will not be effective unless the requirements under 35 U.S.C. 371(c)(1), (2), and (4) for payment of the basic national fee, copy of the International Application and English translation thereof (if required), and the oath or declaration of the inventor(s) have been received.
2. ☐ A copy of the International Application (35 U.S.C. 371(c)(2)) is attached hereto (not required if the International Application was previously communicated by the International Bureau or was filed in the United States Receiving Office (RO/US)).
3. An English language translation of the International Application (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
4. An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4))
   a. ☑ is attached.
   b. ☐ was previously filed in the international phase under PCT Rule 4.17(iv).

Items 5 to 8 below concern amendments made in the international phase.

PCT Article 19 and 34 amendments

5. ☐ Amendments to the claims under PCT Article 19 are attached (not required if communicated by the International Bureau) (35 U.S.C. 371(c)(3)).
6. ☐ English translation of the PCT Article 19 amendment is attached (35 U.S.C. 371(c)(3)).
7. ☐ English translation of annexes (Article 19 and/or 34 amendments only) of the International Preliminary Examination Report is attached (35 U.S.C. 371(c)(5)).

Cancellation of amendments made in the international phase

8a. ☐ Do not enter the amendment made in the international phase under PCT Article 19.

8b. ☐ Do not enter the amendment made in the international phase under PCT Article 34.

NOTE: A proper amendment made in English under Article 19 or 34 will be entered in the U.S. national phase application absent a clear instruction from applicant not to enter the amendment(s).

The following items 9 to 17 concern a document(s) or information included.

9. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
10. ☐ A preliminary amendment.
11. ☑ An Application Data Sheet under 37 CFR 1.76.
12. ☐ A substitute specification. NOTE: A substitute specification cannot include claims. See 37 CFR 1.125(b).
13. ☐ A power of attorney and/or change of address letter.
14. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.3 and 37 CFR 1.821-1.825.
15. ☐ Assignment papers *(cover sheet and document(s))*. Name of Assignee: _____
16. ☐ 37 CFR 3.73(c) Statement *(when there is an Assignee)*.

This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO-1390 (06-13)
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U.S. APPLN. No. (if known – see 37 CFR 1.5)	INTERNATIONAL APPLICATION No.	ATTORNEY DOCKET No.

17. ☐ Other items or information:

The following fees have been submitted.	CALCULATIONS	PTO USE ONLY
18. ☑ Basic national fee (37 CFR 1.492(a)) **$280**	$ 280	
19. ☑ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** All other situations **$720**	$ 720	
20. ☑ Search fee (37 CFR 1.492(b)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority ..... **$120** International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB ..... **$480** All other situations **$600**	$ 480	
TOTAL OF 18, 19, and 20 =	$ 1480	
☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)). Fee for each additional 50 sheets of paper or fraction thereof **$400**		

Total Sheets	Extra Sheets	Number of each addition 50 or fraction thereof (round **up** to a whole number)	RATE	
- 100 =	/ 50 =		x **$400**	$

Surcharge of **$140.00** for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	21 - 20 =	1	x **$80**	$ 80	
Independent claims	- 3 =		x **$420**	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$780**	$	
Processing fee of **$140.00** for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). +				$	
TOTAL OF ABOVE CALCULATIONS =				$ 1560	
☐ **Applicant asserts small entity status.** See 37 CFR 1.27. Fees above are reduced by ½.					
☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Fees above are reduced by ¾. Applicant must attach form PTO/SB/15A or B or equivalent.					
TOTAL NATIONAL FEE =				$ 1560	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property. +				$	
TOTAL FEES ENCLOSED =				$ 1560	
				Amount to be refunded:	$
				Amount to be charged:	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☑ Please charge my Deposit Account No. 501613 in the amount of $ 1865 to cover the above fees.

c. ☑ The Director is hereby authorized to charge additional fees which may be required, or credit any overpayment, to Deposit Account No. 501613 as follows:

i. ☑ any required fee.

ii. ☐ any required fee except for excess claims fees required under 37 CFR 1.492(d) and (e) and multiple dependent claim fee required under 37 CFR 1.492(f).

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. The PTO-2038 should only be mailed or faxed to the USPTO. However, when paying the basic national fee, the PTO-2038 may NOT be faxed to the USPTO.

ADVISORY: If filing by EFS-Web, do **NOT** attach the PTO-2038 form as a PDF along with your EFS-Web submission. Please be advised that this is **not** recommended and by doing so your **credit card information may be displayed via PAIR**. To protect your information, it is recommended to pay fees online by using the electronic payment method.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File)Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013, and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE 1: By providing this statement under 37 CFR 1.55 or 1.78, **this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA**.

NOTE 2: A U.S. national stage application may not claim priority to the international application of which it is the national phase. The filing date of a U.S. national stage application is the international filing date. See 35 U.S.C. 363.

Correspondence Address

☑ The address associated with Customer Number: 34236 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone			
Email					

Signature	/Jeffrey W. Wong/	Date	2015-11-23
Name (Print/Type)	Jeffrey W. Wong	Registration No. (Attorney/Agent)	46414

Priority Document Access Service
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The International Bureau certifies that the document in this package is a copy of the patent application provided through the WIPO priority document access service. The document has been available to the Priority Document Access Service since the date of availability indicated, and has been available to the indicated Office as of the date specified following the relevant Office code:

Document details:	Country/Office:	**US**
	Filing date:	**25 Jun 2013 (25.06.2013)**
	Application number:	**61838965**

Date of availability of document:	**25 Sep 2013 (25.09.2013)**
Availability to Office:	**IB [27 Jun 2014 (27.06.2014)]**

Date of issue of this certificate: **11 Jul 2014 (11.07.2014)**

34, chemin des Colombettes
1211 Geneva 20, Switzerland
www.wipo.int

1111

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

July 11, 2014

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE UNDER 35 USC 111.

APPLICATION NUMBER: *61/838,965*
FILING DATE: *June 25, 2013*

THE COUNTRY CODE AND NUMBER OF YOUR PRIORITY APPLICATION, TO BE USED FOR FILING ABROAD UNDER THE PARIS CONVENTION, IS *US61/838,965*

Certified by

David J. Kappos

Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

Inventor(s)

Inventor 1 — Remove

Given Name	Middle Name	Family Name	City	State	Country i
David		TIKKANEN	Waterloo	ON	CA

Inventor 2 — Remove

Given Name	Middle Name	Family Name	City	State	Country i
Kyle		HATHAWAY	Kitchener	ON	CA

All Inventors Must Be Listed – Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
Attorney Docket Number (if applicable)	PAT 78496P-2

Correspondence Address

Direct all correspondence to (select one):

◉ The address corresponding to Customer Number	○ Firm or Individual Name
Customer Number	26123

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

◉ No.

○ Yes, the invention was made by an agency of the United States Government. The U.S. Government agency name is:

○ Yes, the invention was under a contract with an agency of the United States Government. The name of the U.S. Government agency and Government contract number are:

Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (11-08)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Entity Status
Applicant asserts small entity status under 37 CFR 1.27 or applicant certifies micro entity status under 37 CFR 1.29

- ◯ Applicant asserts small entity status under 37 CFR 1.27
- ◯ Applicant certifies micro entity status under 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
- ◉ No

Warning

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Signature

Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/			Date (YYYY-MM-DD)	2013-06-25
First Name	Jeffrey W.	Last Name	Wong	Registration Number (If appropriate)	46414

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **This form can only be used when in conjunction with EFS-Web. If this form is mailed to the USPTO, it may cause delays in handling the provisional application.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or paten. Accordingly, pursuant to the requirements of the Act, please be advised that : (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, t o a n other federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 78496P-2
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

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Prefix	Given Name	Middle Name	Family Name	Suffix
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	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

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Title of the Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES		
Attorney Docket Number	PAT 78496P-2	**Small Entity Status Claimed**	☐
Application Type	Provisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
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Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

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In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

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If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 78496P-2
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

Email Address	

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Signature:

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Signature	/Jeffrey W. Wong/			Date (YYYY-MM-DD)	2013-06-25
First Name	Jeffrey W.	Last Name	Wong	Registration Number	46414

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 78496P-2
	Application Number	
Title of Invention	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES	

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Apparatus and Method for Monitoring and Limiting Power to SSL Devices

Background of The Disclosure

Continuing development of SSL (solid-state lighting) devices such as light emitting diodes (LEDs) or LED arrays for low power and high power general illumination applications as well as OLEDs (organic LEDs) has introduced a need to limit power within predetermined limits to these devices to mitigate or reduce over temperature operation or abnormal operation of lighting apparatus. Such a power limit capability is desirable under internal or external fault conditions, transient load conditions, as well as ambient temperature conditions.

In terms of fault conditions, OLEDs may have failure mechanisms that include an increase in impedance. In this failure mode, the increased impedance results in increased power dissipation for a fixed LED drive current which may increase the risk of a fire hazard.

In terms of ambient temperature conditions, low power and high power LEDs vary in voltage drop with operating junction temperatures whereby as the junction temperature increases, the voltage drop across the LED is reduced. Conversely, if the junction temperature is reduced, the voltage drop across the LED is increased.

For instance, in a cold ambient operating temperature such as -40 °C, the LED voltage drop is highest during initial cold start conditions at power up. This results in a higher initial power requirement during turn on and operation until the voltage drop across the LED drops as its junction temperature increases. Cold start operating requirements and corresponding power requirements can exceed predetermined power limits such as UL1310 Class 2 power levels of 100 watts or any other predetermined value.

Approaches exist to limit power and current to a LED as a result of an external failure of the LED load, or an internal failure of a component within an LED power source. One common approach is to disable or turn off the LED power source if an over power or over current condition is detected. Another approach is to implement a “hiccup” mode whereby the output of the LED power source is continually cycled on and off in an over power or over current condition.

However, it is not always ideal to immediately disconnect power to a LED load under transient conditions whether by a potential fault or an AC mains transient or load transient or temporary overload condition. It is advantageous to monitor the power to a LED load and reduce the power level first before asserting a shutdown of the LED power source.

Therefore, there is provided a novel apparatus and method for monitoring and limiting power to SSL devices.

Detailed Description of the Disclosure

The present disclosure is directed at a system, apparatus, and method to monitor and limit power to solid state lighting (SSL) devices such as light emitting diodes (LEDs). While much of this disclosure refers to LEDs, other SSL devices may be used without loss of generality. In the current description, the reference to LED power source can also be referred to as a LED driver, or LED power supply.

Detailed Description of Preferred Embodiment

Turning to Figure 1, a block diagram of an embodiment for the LED power source is shown.

An LED power source 10 comprises a Power Factor Conversion **(PFC)** Boost 22 which receives AC power from the AC mains input 20 located externally from the LED power source 10. The PFC Boost 22 is connected to the DC/DC converter 24 which in turn is connected to the output voltage bus 28. A galvanic isolation barrier 26 provides an electrical safety barrier between the output low voltage bus 28 and high voltage levels on the AC mains input 20, the PFC boost 22 and the DC/DC converter 24.

In one embodiment, the PFC Boost 22, the DC/DC converter 24, the galvanic isolation barrier 26, and the voltage bus 28 can be seen as a power circuit 29. The power circuit 29 is connected to a power limit 31 which in turn is connected to an output current driver 35. It will be understood that there may be multiple power limit 31 circuits connected to the output voltage bus and there may be multiple output current drivers 35 connected to each individual power limit 31. The output of the one or more output current drivers 35 is connected to one or more external LED loads 42.

The LED power source 10 further includes a primary controller 50 which is connected to the PFC Boost 22 and the DC/DC Converter 24 power conversion stages and fault optocoupler 54.

With reference to power limit 31, the secondary controller 56 is connected to the fault optocoupler 54 via a control line 52, and also connected to the current source controller 68 via data line 60. The secondary controller 56 is also connected to power monitor 30 via a sense line 58 and port 66 for programming and calibrating various parameters.

With reference to output current driver 35, the current source controller 68 is further connected to the current source 36 and current sense 38 via control lines 62 and 64 respectively and also connected to port 65 for programming and calibrating various parameters. An optional voltage sense#2 40 is also connected in parallel with each individual LED load 42.

As will be understood, not all of the components or connections of the LED power source required for operation are shown as they will be understood by one skilled in the art. For example, the power circuit 29 can also include an EMI filter, inrush current limit or a bridge rectifier. With respect to connections, it will be understood that more than one sense line, control line or data line can be implemented between function blocks. For example, more than one sense line may be connected between power monitor 30 and secondary controller 56 to provide both voltage and current sense information to the secondary controller. Also, there may be multiple data line connections 60 between the secondary controller 56 and current source controller 68.

In operation, the power circuit 29 is a two stage power converter comprising a PFC Boost 22 and DC/DC converter 24 both of which are controlled by the primary controller 50 to provide an output bus voltage 28. The primary controller 50 transmits control signals to the PFC Boost 22 and DC/DC converter 24 power stages and receives voltage and/or current sense information from the PFC Boost and DC/DC converter. The output voltage bus 28 is typically a regulated voltage output with a feedback loop coupled to the primary controller via an optocoupler (not shown).

The power from the output voltage bus 28 is transferred to at least one output current source 36 via the power limit 31 comprised of a power monitor 30 and secondary controller 56. The power monitor 30 senses current delivered from the output voltage bus 28 and may also sense voltage 32 across the output voltage bus and transmits this current and/or voltage information to the secondary controller 56.

The power limit 31 and associated ancillary circuits provide an apparatus to limit power to the external LED load 42 in the event of a single component failure within the LED power source 10, such as within output current source 36, or current sense 38, or current source controller 68.

The power limit 31 may also limit power in the event of an external LED load fault or over load condition. A fault condition may include a high impedance fault at the LED or OLED load. An over load condition may be a transient condition such as a cold start or power up of an LED load in ambient temperatures less than 0 °C or an improper LED load connected to the LED power source 10.

The secondary controller 56 compares the current and/or voltage values to predetermined power limits (given by the formula, power=voltage x current) which have been programmed into the controller. In the event that the power level from the output bus 28 exceeds a predetermined value, the secondary controller 56 may assert one or more options to limit output power to the LED load.

For instance, the secondary controller 56 may assert various power limit options at different points in time. A power limit sequence may include a dimming command through data line 60 to the current source controller 68 to reduce the average output current either gradually or stepwise to the LED load 42 and a subsequent gradual or stepwise increase in average current after a period of time.

Alternatively, the secondary controller 56 may complete a sequence of tasks attempting to reduce the output power to the LED load 42 first then, if it is determined that the output power level is still beyond predetermined limits as sensed by the power monitor 30, it will then assert a shutdown of the power circuit 29.

With reference to output current driver 35, the current source 36 provides a constant current output to the LED load 42. The current sense#2 38 provides a feedback signal to current source controller 68 to regulate the output current to the LED load 42.

The current source controller 68 regulates the output current provided to the LED load and also provides a means of reducing the average current to the LED load via a gate pulse signal with a variable duty cycle through control line 62.

The optional voltage sense#2 40 permits the current source controller 68 to monitor the power transferred to the LED load as a redundant power limit capability. In this instance, power is monitored by the current sense#2 38 and voltage sense#2 40 directly across the LED load 42. The redundant power limit capability provides back up protection in the event of a failure of the power limit 31.

With reference to Figure 1, the LED power source 10 includes multiple power conversion stages to convert AC power to DC power for the LED load 42 and monitor and limit power to the load.

In a more specific embodiment of Figure 1, the power circuit 29 comprises a PFC boost stage which implements a boost power conversion topology with an input AC voltage mains range of 103 Vac to 300 Vac from the AC mains input 20. The PFC boost stage 22 outputs a loosely regulated 430 Vdc over the input AC range.

The DC/DC converter 24 is derived from the isolated switch mode buck converter topology and comprises a gavanically isolated 26 full bridge converter. The output bus 28 is a tightly regulated output, typically 46 Vdc, and controlled by a feedback loop (not shown) to the primary controller 50.

The power monitor 30 includes the current sense#1 34 and optional voltage sense#1 32 to provide at least one analog voltage signal to the secondary controller 56 through sense line 58. The current sense 34 typically includes a resistor connected in series with the output voltage bus 28 and current source 36. The voltage sense 32 typically includes a resistor divider network connected in parallel with the output voltage bus 28. Both current sense#1 34 and voltage sense#1 32 may include ancillary circuits to scale and filter the analog control signals before transmitting the signals to the appropriate analog to digital ports in the secondary controller 56.

The secondary controller 56 comprises an averaging digital filter which takes 1024 readings for current and/or voltage over a period of time such as but not limited to 500 milliseconds, then calculates an average value and compares this value to a predetermined power limit such as 97 watts. If the power level exceeds the predetermined limit, the secondary controller will assert one or more power limit options.

In one embodiment, the voltage sense#1 32 is not required if the output voltage bus 28 is a tightly regulated voltage output since the secondary controller 56 can complete the power calculation based on an assumed constant voltage level.

In terms of power limit options, one option may be to transmit a change in light intensity command through data line 60 to the current source controller 68. This control information or words of data, is preferably transmitted over a "sync" line, "clock" line and "data" lines. The start of each word is preferably delimited by the "sync" line and the start of each bit is delimited by the "clock" line. This control information is translated by the current source controller 68 to on-time and off time information and transmitted as a gate pulse through control line 62 to the output current source 36.

Another power limit option may include a shutdown command via control line 52 to the fault optocoupler 54 to immediately disable the power circuit 29.

Alternatively, the secondary controller 56 may complete a sequence of tasks attempting to reduce the output power to the LED load 42 first then, if it is determined that the output power level is still beyond predetermined limits as sensed by the power monitor 30, it will then assert a shutdown of the power circuit 29.

With reference to power limit 31, the secondary controller 56 includes a connection to a port 66. The port is comprised of five pins for in circuit serial programming of the controller 56 and at least one pin for calibration of the power limit 31. Calibration may be required to account for component tolerances in the various circuits such as in the power monitor 30 to establish accurate current and or voltage readings.

For example, assuming a required power limit of 97 watts, calibration may comprise changing the state of the controller to "calibration mode" such as via a jumper connected to port 66; applying the appropriate load representing the desired power limit (97 watts); and saving the applicable parameters by adjusting the constants stored in the EEPROM memory of the controller 56.

With reference to output current driver 35, as referenced in Figure 1, the current source 36 and current sense 38 may comprises a switch mode buck topology with a MOSFET switch implementing a hysteretic control method. The current source 36 provides a regulated output current to the LED load 42 implemented by means of a feedback loop 64 to the current source controller 68. The current source controller 68 may also output a dimming signal, as a result of an over power condition, implemented through a gate drive control line 62 to the output current source 36. The current source controller is typically a digital controlled device implemented by means of a microcontroller and firmware.

The dimming method may be implemented by various methods such as those disclosed in US Patent 8,299,987 or in US Patent Application 2013/0049634 which are herein incorporated by reference.

The output current driver 35 may also perform a redundant power limit function similar to the power limit 31 whereby it can be programmed and calibrated for a predetermined power limit. In this embodiment, the secondary controller 56 is placed into calibration mode via port 66 in order to stop communication with the current source controller 68 and permit current source controller 68 to accept calibration commands through port 65.

The current sense#2 38 and voltage sense#2 40 communicate a measured value to the current source controller 68 in order to calculate power (given by the formula, power =voltage x current). If an over power event occurs, the current source controller 68 may reduce the average current to the LED load 42 by a dimming pulse comprising a variable duty cycle through control line 62 to the current source 36 or the controller 68 may assert a shutdown signal through control line 63 to shut down the power circuit 29.

Alternatively, the current source controller 68, as part of a redundant power limit function, may also complete a sequence of attempting to reduce the output power to the LED load 42 first then, if it is determined that the output power level is still beyond predetermined limits as sensed by the voltage sense#2 40 and current sense#2 38, it will then assert a shutdown of the power circuit 29.

The port 65 connected to current source controller 68 is also used for programming the output current driver 35 to the desired output current (such as but not limited to 350mA, 700mA) for the LED load 42

Turning to Figures 2a to 2d, various examples of power monitoring and power limiting sequences as a function of time are presented.

Figure 2a is an example of a power limit sequence where an internal fault occurs within the LED power source or an external fault occurs with the LED load. In this example, normal power is applied to the load until a fault occurs resulting in monitored power exceeding the power threshold at t_1. The power limit 31 or redundant power limit within output current driver 35 will attempt to reduce the power while continuing to monitor the power for a period

of time t_1 to t_2. At the time period t_2, given that monitored power still exceeds the threshold, the LED power source 10 is disabled at t_3.

Figure 2b is an example of a cold start scenario where the LED load exceeds the power threshold at start up t_0. The power limit 31 or redundant power limit within output current driver 35, steps down the output power to a reduced power level such as 75% at t_1. Power is continuously monitored for a period of time (t_1 to t_2) at the reduced power level. Starting at t_2, power is gradually increased (t_2 to t_3) in small increments such as 2.5% with a time interval between increments of typically 10 seconds until normal power operation is restored.

Figure 2c is an example of another fault condition where an initial power threshold is exceeded at t_1. The power is stepped down to a reduced level and after a period of time, the power is gradually increased until a second power threshold limit is exceeded at t_4. The LED power source is then immediately disabled at t_5.

Figure 2d is an example of a transient condition on the AC mains input to the LED source 10 causing a transient voltage or current over shoot on the output bus 28 resulting in an exceeded power threshold at t_1. Power is stepped down at t_2 and after a period of time (t_2 to t_3) with power continuously monitored, power is gradually increased to a normal power level at t_4.

In a further embodiment, with reference to Figure 1, the power circuit 29 may include alternative DC/DC converter topologies. For instance, such power conversion topologies may include but are not limited to a half bridge resonant converter, a flyback, or forward converter topologies. The primary controller 29 may be two separate controllers to provide individual gate drive and feedback control signals to the PFC boost 22 and DC/DC converter 24.

In yet a further embodiment, the output voltage bus 28 may be an unregulated output voltage with no feedback loop to the DC/DC converter 24. In this instance, the DC/DC converter may be implemented by means of an isolated half bridge topology where both power switches alternately operate at close to a 50% duty cycle.

With reference to power limit 31, further embodiments may include an op amp or comparator as opposed to an analog to digital port. Other embodiments may also include alternate filtering methods such as but not limited to a moving average filter to filter the power monitor readings.

With reference to transmitting a change in light intensity command through data line 60, alternate embodiments may include a UART, an I^2C bus, SPI (Serial Peripheral Interface Bus) or a parallel communication apparatus.

In a further embodiment, the output current source 36 may further include other topologies such as boost, buck-boost, or SEPIC (single ended primary inductor converter). Alternate embodiments may also include an analog controller as opposed to a digital controller where no firmware is required for implementation. Other control methods to regulate output current to the LED load 42 may include pulse width modulation.

As an alternate embodiment, the output current source 35 may be a linear regulator with a constant current output as opposed to a switch mode topology.

With respect to the secondary controller 56 and the current source controller 68, the power limit function and regulation of output current may be implemented by means of a single controller.

Other change in light intensity or dimming methods may include a pulse width modulation method or a constant current reduction method (CCR) or a combination of various other methods. The CCR method is a continuous current flow through a LED that is reduced in order to reduce the brightness of the LED.

Figure 3 shows another embodiment where the power limit function is implemented within the output current driver 35 alone with no redundant power limit function implemented in the apparatus.

Figure 4 shows another embodiment where the voltage sense#2 40 is not implemented in the output current driver 35 and the output current driver 35 provides a regulated constant current output with no redundant power limit capability.

What is Claimed is:

1. A method of controlling power to a SSL device comprising:
limiting the power delivered to the SSL device.

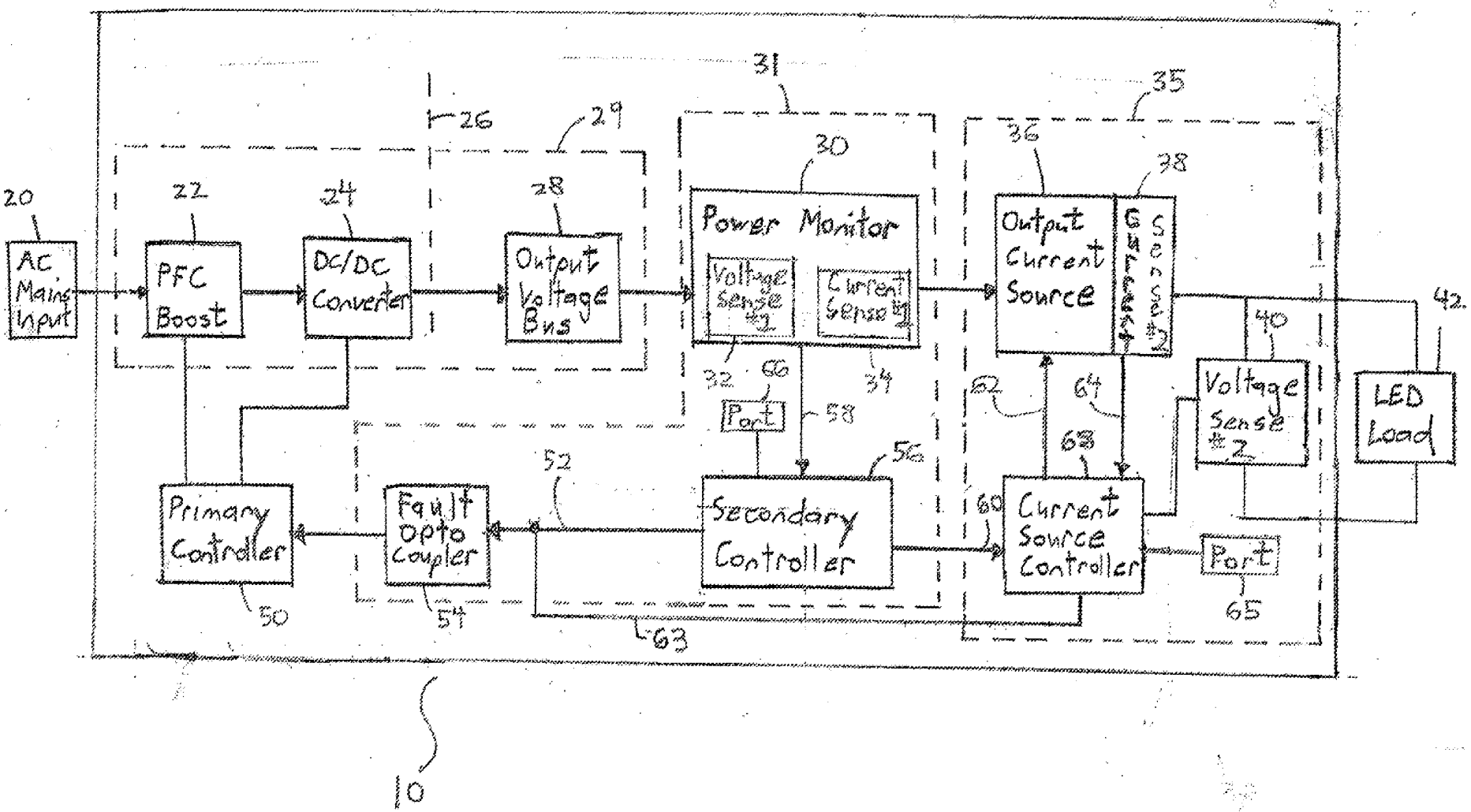

AC Mains Input
20
PFC Boost
22
DC/DC Converter
24
Output Voltage Bus
28
26
29
31
Power Monitor
30
Voltage Sense #1
Current Sense #1
32
34
Port
66
58
Output Current Source
36
Current Sense #2
38
35
40
Voltage Sense #2
42
LED Load
62
64
68
Primary Controller
50
Fault Opto Coupler
54
52
Secondary Controller
56
60
Current Source Controller
Port
65
63
10

Figure #1

Figure 2

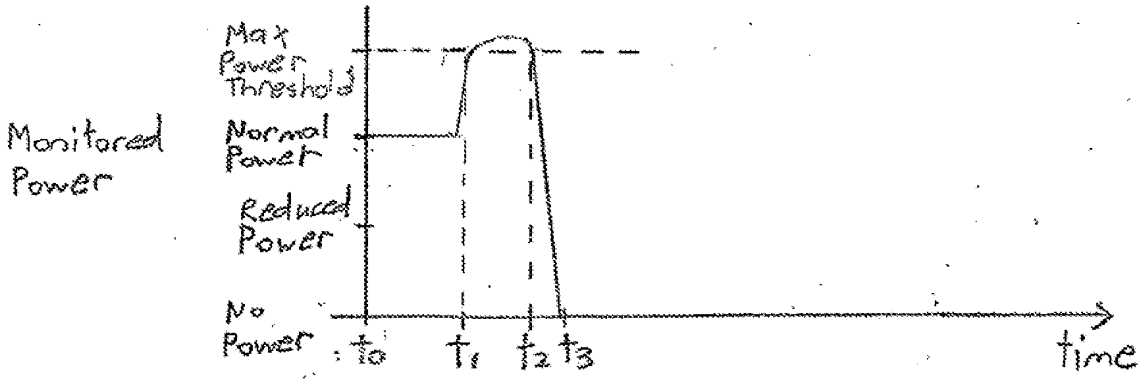


Fig 2a

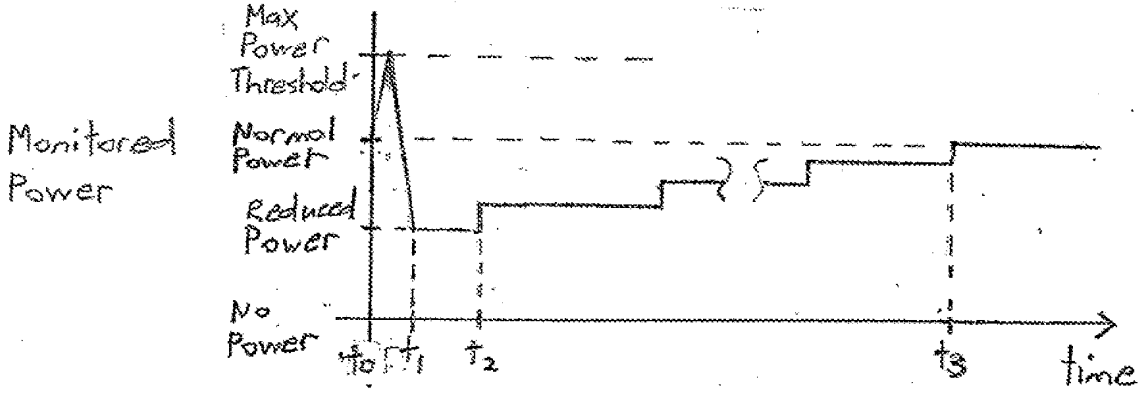


Fig 2b

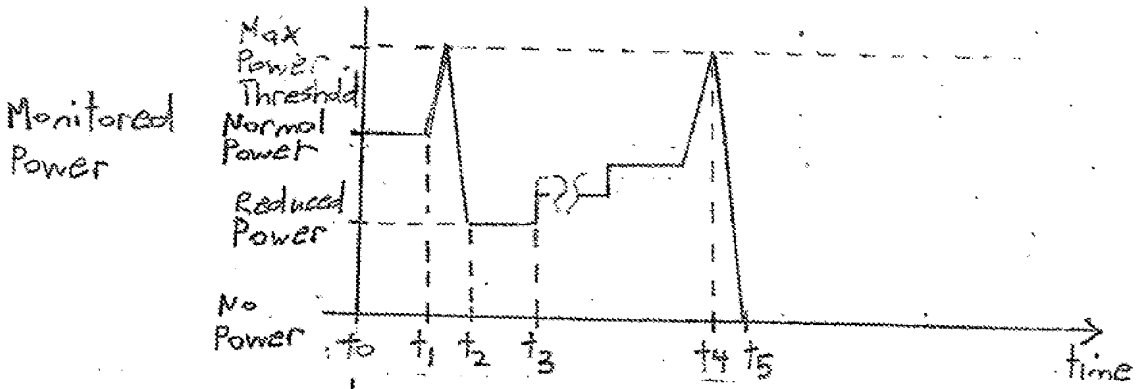


Fig 2c

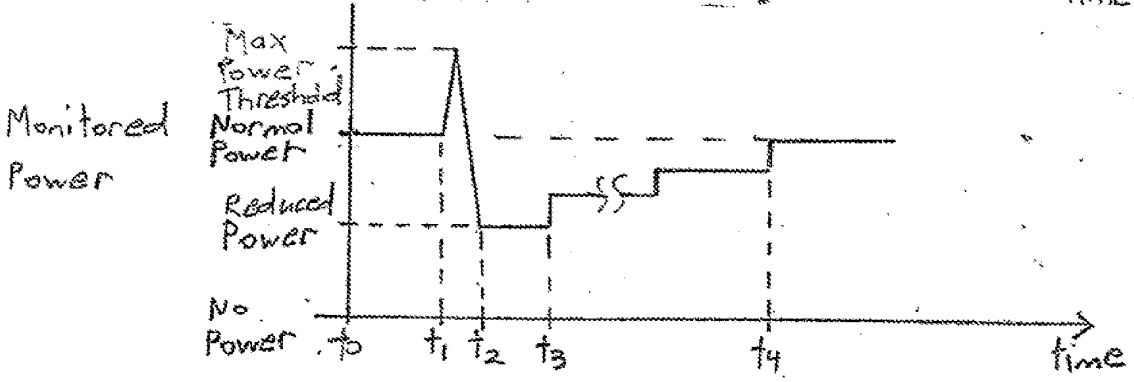


Fig 2d

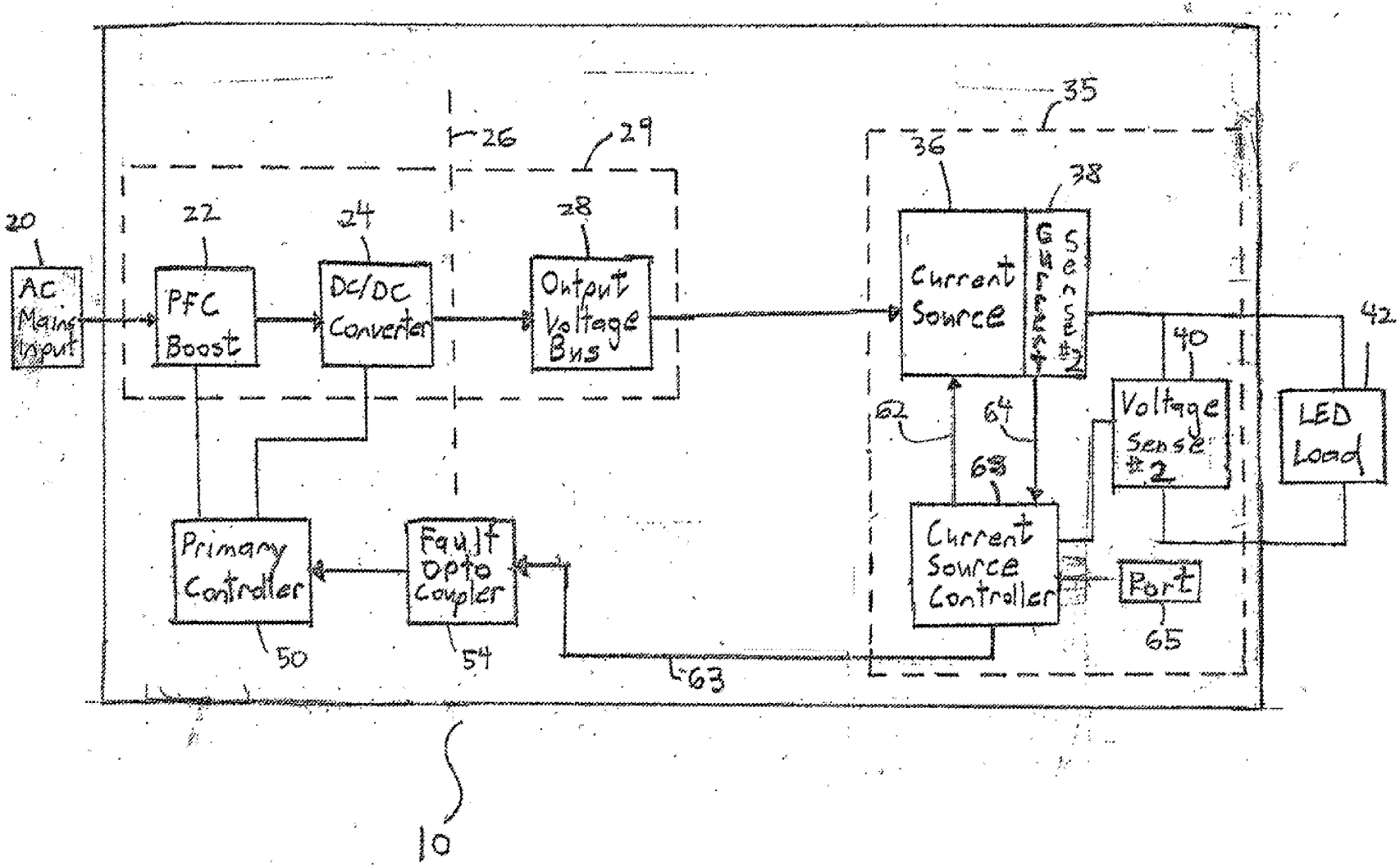

20
AC Mains Input
22
PFC Boost
24
DC/DC Converter
26
28
Output Voltage Bus
29
35
36
Current Source
38
Current Sense #2
40
Voltage Sense #2
42
LED Load
62
64
68
Current Source Controller
Port
65
Primary Controller
50
Fault Opto Coupler
54
63
10

Figure #3

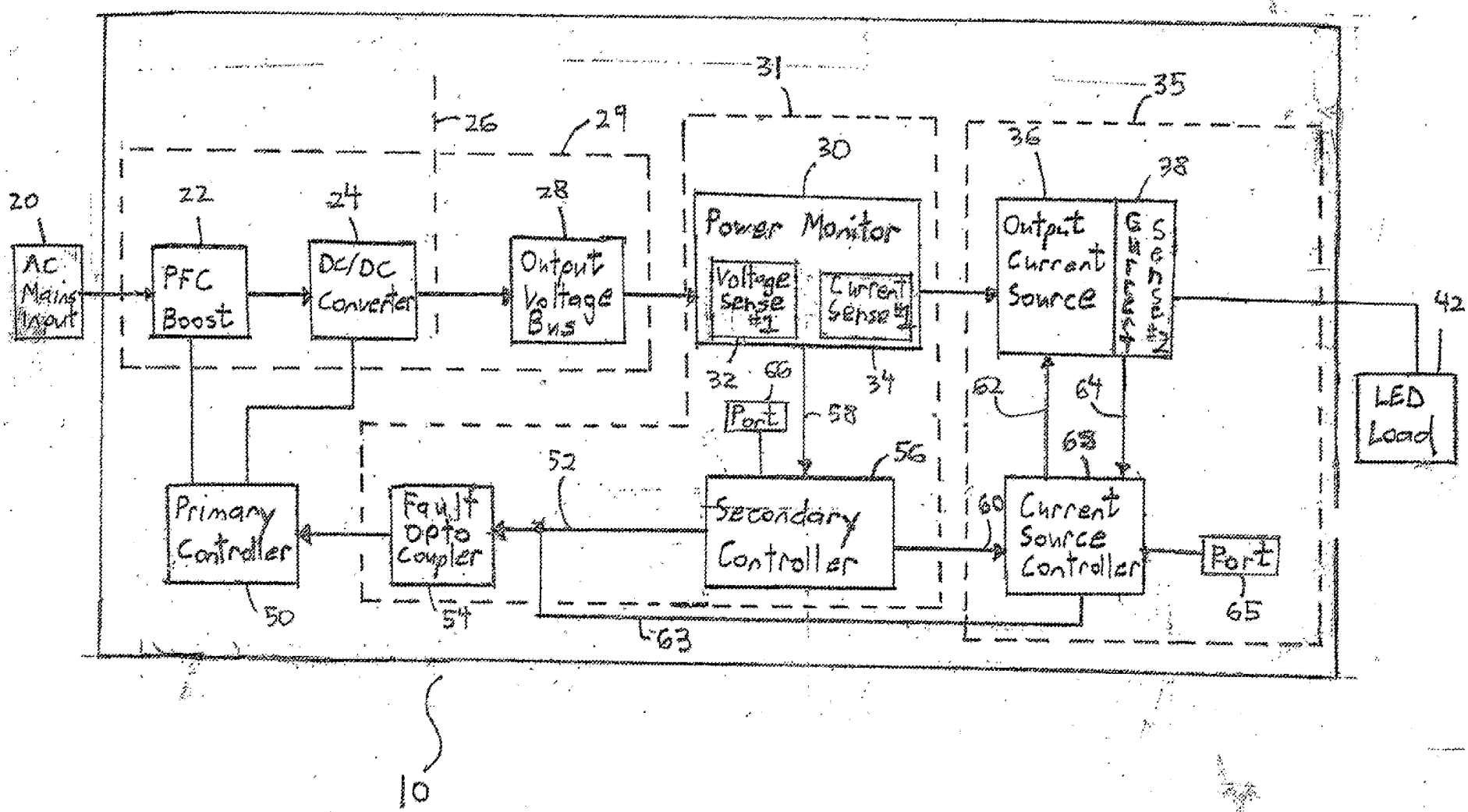

AC Mains Input
20
PFC Boost
22
DC/DC Converter
24
Output Voltage Bus
28
26
29
31
Power Monitor
30
Voltage Sense #1
Current Sense #1
32
34
Port
66
58
Output Current Source
36
Current Sense #2
38
35
42
LED Load
62
64
63
Primary Controller
50
Fault Opto Coupler
54
52
Secondary Controller
56
Current Source Controller
60
Port
65
63
10

Figure #4

Electronic Acknowledgement Receipt

EFS ID:	16144207
Application Number:	61838965
International Application Number:	
Confirmation Number:	1267
Title of Invention:	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	26123
Filer:	Jeffrey Wong/Tara Charbonneau
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	PAT 78496P-2
Receipt Date:	25-JUN-2013
Filing Date:	
Time Stamp:	12:42:16
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$260
RAM confirmation Number	13589
Deposit Account	501593
Authorized User	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Provisional Cover Sheet (SB16)	PAT78496P-2_Provisional_Coversheet.PDF	1477348 a41d2813242771204 68c89316e9e1b16676 1538e	no	3
Warnings:					
Information:					
2	Application Data Sheet	PAT78496P-2_ADS.PDF	1255627 7a7d1808a4a8d08ded828589ffeaf0af82a6 9815	no	7
Warnings:					
Information:					
3		PAT78496P-2_Specification.pdf	90882 810e9389c9318300851d578f2dd75b8c829 3fb36	yes	8

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	7
Claims	8	8

Warnings:					
Information:					
4	Drawings-only black and white line drawings	PAT78496P-2_Drawings.pdf	1017846 1d6d7f1a56d17aee94ed0b6342c7ebcf3e0 05795	no	4
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30041 2e2ef883469dffa27915dca97b72630b979d 825b	no	2
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		Total Files Size (in bytes):	3871744		

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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DOCUMENT MADE AVAILABLE UNDER THE PATENT COOPERATION TREATY (PCT)

International application number:		**PCT/CA2014/050609**
International filing date:		**25 June 2014 (25.06.2014)**
Document type:		**Certified copy of priority document**
Document details:	Country/Office:	**US**
	Number:	**61/838,965**
	Filing date:	**25 June 2013 (25.06.2013)**
Date of receipt at the International Bureau:		**27 June 2014 (27.06.2014)**

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a),(b) or (b-*bis*)

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1211 Geneva 20, Switzerland
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PCT REQUEST

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0	**For receiving Office use only**	
0-1	International Application No.	PCT/CA2014/050609
0-2	International Filing Date	25 June 2014 (25.06.2014)
0-3	Name of receiving Office and "PCT International Application"	RO/CA

0-4	**Form PCT/RO/101 PCT Request**	
0-4-1	Prepared Using	PCT-SAFE Version 3.51.063.239 MT/FOP 20140613/0.20.5.21
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	Canadian Intellectual Property Office (RO/CA)
0-7	**Applicant's or agent's file reference**	PAT78496W-90
I	**Title of Invention**	APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES
II	**Applicant**	
II-1	This person is	Applicant only
II-2	Applicant for	All designated States
II-4	Name	LUMASTREAM CANADA ULC
II-5	Address	400-3rd Avenue S.W. Calgary, Alberta T2P 4H2 Canada
II-6	State of nationality	CA
II-7	State of residence	CA
III-1	**Applicant and/or inventor**	
III-1-1	This person is	Inventor only
III-1-3	Inventor for	All designated States
III-1-4	Name (LAST, First)	TIKKANEN, DAVID
III-1-5	Address	194 Silverwood Place Waterloo, Ontario N2T 2R9 Canada
III-2	**Applicant and/or inventor**	
III-2-1	This person is	Inventor only
III-2-3	Inventor for	All designated States
III-2-4	Name (LAST, First)	HATHAWAY, KYLE
III-2-5	Address	5 Norbert Place Kitchener, Ontario N2K 1E5 Canada

PCT REQUEST

Print Out (Original in Electronic Form)

IV-1	**Agent or common representative; or address for correspondence**	
	The person identified below is hereby/ has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	Agent
IV-1-1	Name (LAST, First)	WONG, Jeffrey W.
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IV-1-4	Facsimile No.	(613) 787-3558
IV-1-5	e-mail	ipinfo@blg.com
IV-1-5(a)	E-mail authorization The receiving Office, the International Searching Authority, the International Bureau and the International Preliminary Examining Authority are authorized to use this e-mail address, if the Office or Authority so wishes, to send notifications issued in respect of this international application:	exclusively in electronic form (no paper notifications will be sent)
IV-2	**Additional agent(s)**	additional agent(s) with same address as first named agent
IV-2-1	Name(s)	ALLARD, Louis; ANISHCHENKO, Alexander; BEHMANN, Curtis B.; CHAKRAPANI, Mukundan; CHATTERJEE, Alaka; CHUMAK, Yuri; COLLARD, Christine J.; CONN, David L.; DE KLEINE, Geoffrey; DECZKY, Thomas; FRITZ, Joachim T.; HENDERSON, Neil; HOFF, Heather; HOWG, Jason L.; HUNG, Shin; JOHNSON, Richard; KEELER, Todd; KENEFORD, L. Brooke; KINSMAN, L. Anne; MARSMAN, Kathleen E.; MORRISON, Lesley; NAUMAN, David; PUNDSACK, Scott R.; RAOUL, Jennifer M.; SILVER, Gail C.; SOJONKY, Andrew D.; WEBB, Tim E.; ZIMMERMAN, Gordon
V	**DESIGNATIONS**	
V-1	**The filing of this request constitutes under Rule 4.9(a), the designation of all Contracting States bound by the PCT on the international filing date, for the grant of every kind of protection available and, where applicable, for the grant of both regional and national patents.**	

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VI-1	**Priority claim of earlier national application**		
VI-1-1	Filing date	25 June 2013 (25.06.2013)	
VI-1-2	Number	61/838,965	
VI-1-3	Country	US	
VI-2	**Priority document request** The International Bureau is requested to obtain from a digital library a certified copy of the earlier application(s) identified above as item(s), using, where applicable, the access code(s) indicated:	VI-1 Access code: 1267	
VI-3	**Incorporation by reference :** where an element of the international application referred to in Article 11(1)(iii)(d) or (e) or a part of the description, claims or drawings referred to in Rule 20.5(a) is not otherwise contained in this international application but is completely contained in an earlier application whose priority is claimed on the date on which one or more elements referred to in Article 11(1)(iii) were first received by the receiving Office, that element or part is, subject to confirmation under Rule 20.6, incorporated by reference in this international application for the purposes of Rule 20.6.		
VII-1	**International Searching Authority Chosen**	Canadian Intellectual Property Office (ISA/CA)	
VIII	**Declarations**	Number of declarations	
VIII-1	Declaration as to the identity of the inventor	–	
VIII-2	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	–	
VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	–	
VIII-4	Declaration of inventorship (only for the purposes of the designation of the United States of America)	–	
VIII-5	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty	–	
IX	**Check list**	Number of sheets	Electronic file(s) attached
IX-1	Request (including declaration sheets)	4	✓
IX-2	Description	18	✓
IX-3	Claims	4	✓
IX-4	Abstract	1	✓
IX-5	Drawings	9	✓
IX-7	TOTAL	36	

PCT REQUEST

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	Accompanying Items	Paper document(s) attached	Electronic file(s) attached
IX-8	Fee calculation sheet	–	✓
IX-19	Other	Documents in pre-conversion format Statement (Section 706): This is a complete and accurate copy of the international application prior to its conversion into the electronic document format in which it is filed.	✓
IX-20	**Figure of the drawings which should accompany the abstract**	1a	
IX-21	**Language of filing of the international application**	English	
X-1	**Signature of applicant, agent or common representative**	(PKCS7 Digital Signature)	
X-1-1	Name (LAST, First)	WONG, Jeffrey W.	
X-1-2	Name of signatory		
X-1-3	Capacity (if such capacity is not obvious from reading the request)		

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10-1	**Date of actual receipt of the purported international application**	25 June 2014 (25.06.2014)
10-2	**Drawings:**	
10-2-1	Received	
10-2-2	Not received	
10-3	**Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application**	
10-4	**Date of timely receipt of the required corrections under PCT Article 11(2)**	
10-5	**International Searching Authority**	ISA/CA
10-6	**Transmittal of search copy delayed until search fee is paid**	

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11-1	**Date of receipt of the record copy by the International Bureau**	

ADVANCE E-MAIL

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92*bis*.1 and Administrative Instructions, Section 422)

To:

WONG, Jeffrey W.
Gowling Lafleur Henderson LLP
50 Queen Street North, Suite 1020
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Kitchener, Ontario N2H 6M2
CANADA

Date of mailing *(day/month/year)*
21 October 2014 (21.10.2014)

Applicant's or agent's file reference
K8001051WO

IMPORTANT NOTIFICATION

International application No.
PCT/CA2014/050609

International filing date *(day/month/year)*
25 June 2014 (25.06.2014)

1. The following indications appeared on record concerning:

☐ the applicant ☐ the inventor ☒ the agent ☐ the common representative

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Borden Ladner Gervais LLP
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Ottawa, Ontario K1P 1J9
Canada

State of Nationality:
State of Residence:
Telephone No.: (613) 237-5160
Facsimile No.: (613) 787-3558
E-mail address: ipinfo@blg.com

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

☐ the person ☐ the name ☒ the address ☐ the nationality ☐ the residence

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Gowling Lafleur Henderson LLP
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P.O. Box 2248
Kitchener, Ontario N2H 6M2
Canada

State of Nationality:
State of Residence:
Telephone No.: 519-576-6910
Facsimile No.: 519-576-0141
E-mail address: waterloo.ip@gowlings.com
☒ Notifications by e-mail authorized

3. Further observations, if necessary:
Please note the change of agent's file reference.

4. A copy of this notification has been sent to:

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☐ the International Searching Authority
☐ the Authority(ies) specified for supplementary search
☐ the International Preliminary Examining Authority
☐ the designated Offices concerned
☐ the elected Offices concerned
☒ other: BORDEN LADNER GERVAIS LLP

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 89 95

Authorized officer
Vernhes Thierry
e-mail pt04.pct@wipo.int
Telephone No. +41 22 338 74 04

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WIPO | PCT

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25 June 2014 (25.06.2014)

(25) Filing Language: English

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(30) Priority Data:
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(71) Applicant: **LUMASTREAM CANADA ULC** [CA/CA]; 400-3rd Avenue S.W., Calgary, Alberta T2P 4H2 (CA).

(72) Inventors: **TIKKANEN, David**; 194 Silverwood Place, Waterloo, Ontario N2T 2R9 (CA). **HATHAWAY, Kyle**; 5 Norbert Place, Kitchener, Ontario N2K 1E5 (CA).

(74) Agents: **WONG, Jeffrey W.** et al.; Gowling Lafleur Henderson LLP, 50 Queen Street North, Suite 1020, P.O. Box 2248, Kitchener, Ontario N2H 6M2 (CA).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

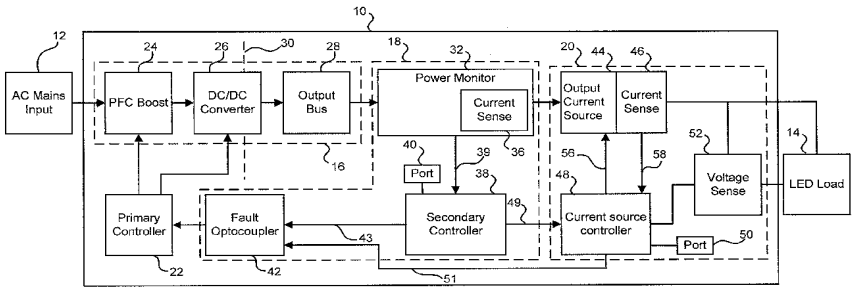


FIGURE 1a

(57) **Abstract**: The disclosure is directed at a system, method and apparatus for monitoring and limiting power supplied to a solid state lighting (SSL) device when an operational fault condition is sensed such as when the power level being supplied to the device is sensed to be meeting or higher than an expected or predetermined level. The system, method and apparatus provide a recovery aspect which means that the SSL device will not be automatically shut down (or power being supplied to the SSL device will not be immediately stopped) upon the discovery of the operational fault condition but will enter a recovery mode. The system may be used for white light general illumination applications as well as to color changing applications.

WO 2014/205575 A1

APPARATUS AND METHOD FOR MONITORING AND LIMITING POWER TO SSL DEVICES

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of priority of U.S. Provisional Patent Application No. 61/838,965 filed June 25, 2013, which is hereby incorporated by reference.

BACKGROUND OF THE DISCLOSURE

Continuing development of solid state lighting (SSL) devices such as light emitting diodes (LEDs) or LED arrays, as well as organic LEDs (OLEDs), for low power and high power general illumination applications has introduced a need to limit power within predetermined limits to these devices to mitigate or reduce over-temperature or abnormal operation of these SSL devices. Such a power limit capability is desirable under internal or external fault conditions, transient load conditions, as well as ambient temperature conditions.

In terms of fault conditions, OLEDs may have failure mechanisms that include an increase in impedance. In this failure mode, the increased impedance results in increased power dissipation for a fixed LED drive current which may, however, increase the risk of the SSL device being a fire hazard.

In terms of ambient temperature conditions, low and high power LEDs vary in voltage drop with operating junction temperatures whereby as the junction temperature increases, the voltage drop across the LED is reduced. Conversely, if the junction temperature is reduced, the voltage drop across the LED is increased.

For instance, in a cold ambient operating temperature such as -40°C, the LED voltage drop is highest during initial cold start conditions at power up. This results in a higher initial power requirement during turn on and operation until the voltage drop across the LED drops as its junction temperature increases. Cold start operating requirements and corresponding power requirements can exceed predetermined power limits such as defined by UL1310 Class 2 power levels of 100 watts or any other predetermined value.

Approaches exist to limit power and current to an LED load as a result of an external failure of the LED load or an internal failure of a component within an LED power source.

One common approach is to disable or turn off the LED power source if an over power or over current condition is detected. Another approach is to implement a "hiccup" mode whereby the output of the LED power source is continually cycled on and off in an over power or over current condition. However, it is not always ideal to immediately disconnect power to a LED load under transient conditions caused by a potential fault, an AC mains transient, a load transient or a temporary overload condition.

Therefore, there is provided a novel apparatus and method for monitoring and limiting power to SSL devices.

SUMMARY OF THE DISCLOSURE

The present disclosure is directed at a system, apparatus, and method for monitoring and limiting power to solid state lighting (SSL) devices such as light emitting diodes (LEDs). More specifically, the current disclosure is directed at a method and apparatus which, after the determination of a fault operation condition, assists in the recovery process for providing power to the SSL device without having to automatically shut down the system or apparatus of providing power. This is beneficial when the fault operation condition is a simple transient matter and not a permanent fault. If the issue is determined to be a permanent fault, then the system of the disclosure may be shut down.

In one embodiment, the disclosure provides an apparatus and method for configuring a power limit function to specific power levels while remaining within Class 2 power levels to address the variability in electrical circuits and variability in electrical characteristics of the LED loads.

In one aspect, there is provided an apparatus for controlling power to a solid state lighting (SSL) device load comprising a power circuit for receiving power from an external source; at least one power limit connected to the power circuit; at least one output current driver for supplying a load power to the SSL device load, the at least one output current driver connected to the at least one power limit; and a power limit controller; wherein the power circuit transmits the power to the at least one power limit which, in turn, transmits a current to the at least one output current driver; wherein the power limit controller directly or indirectly monitors a level of the load power and controls the at least one power limit to reduce the level

of the load power for a predetermined period of time when the load power exceeds a predetermined power limit.

In another aspect, there is provided a method of controlling power to a solid state lighting (SSL) device load comprising receiving an input power, delivering load power to the SSL device load, monitoring current level in load power, limiting load power to the SSL device for a predetermined period of time after a predetermined operational fault condition is met.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present disclosure will now be described, by way of example only, with reference to the attached Figures.

Figure 1a is a schematic diagram of a first embodiment of an apparatus for providing power to a solid state lighting (SSL) device;

Figure 1b is a schematic diagram of another embodiment of apparatus for providing power to a SSL device;

Figures 2a to 2d are graphs of power vs time for various SSL device operation scenarios;

Figure 3a is a schematic diagram of another embodiment of apparatus for providing power to a SSL device;

Figure 3b is a schematic diagram of yet a further embodiment of apparatus for providing power to a SSL device;

Figure 4a is a schematic diagram of a fifth embodiment of apparatus for providing power to a SSL device;

Figure 4b is a schematic diagram of a sixth embodiment of apparatus for providing power to a SSL device;

Figure 5 is a flowchart outlining a method of monitoring and limiting power to a SSL device.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

The disclosure is directed at a system, method and apparatus for monitoring and limiting power supplied to a solid state lighting (SSL) device when an operational fault condition is sensed such as when the power level being supplied to the device is sensed to be meeting or higher than an expected or predetermined level. The system, method and apparatus provide a recovery aspect which means that the SSL device will not be automatically shut down (or power being supplied to the SSL device will not be immediately stopped) upon the discovery of the operational fault condition but will enter a recovery mode. If the system of the disclosure is unable to respond to the recovery mode to overcome the operational fault condition, power being delivered or supplied to the SSL device may then be stopped causing the SSL device to be shut down. While much of this disclosure refers to light emitting diodes (LEDs), other SSL devices may be used without loss of generality. The disclosure is also directed at a system, method, and apparatus for configuring a power limit to address the variability in electrical circuits and variability in electrical characteristics of SSL devices.

The system of the disclosure may be used for white light general illumination applications as well as color changing applications.

It is advantageous to monitor the power being supplied to the LED load and reduce the power level first before asserting a shutdown of the system of the disclosure.

Turning to Figure 1a, a schematic diagram of an apparatus for providing power to a SSL device, such as a LED power source, is shown. The LED power source 10, which may also be referred to as a LED driver or LED power supply, receives power from an AC mains input 12 and then controls and delivers power to an external LED load 14 (which may be seen as the SSL device). The LED power source 10 includes a power circuit 16 which is connected to a power limit 18 which, in turn, is connected to an output current driver 20. For simplicity, only one power limit 18 and one output current driver 20 is shown, however, any number of power limits 18 and output current drivers 20 may be integrated within the LED power source 10. Further, although shown in one to one relation, there may be one power limit 18 associated with multiple output current drivers 20 and vice versa. In the current figure, a single output current driver 20 is connected to the LED load 14, however the output

of one of more output current drivers 20 may be connected to one or more external LED loads 14.

In the preferred embodiment, the LED power source 10 includes multiple power conversion stages to convert AC power (from the AC mains input 12) to DC power for the external LED load 14. The source 10 further includes apparatus for monitoring and limiting the power being supplied to the load 14 when an operational fault condition arises, such as, but not limited to, when the power level being supplied to the load is sensed to be above a normal or expected threshold. In one embodiment, the power may be sensed in the output current driver by means of the current sense, a voltage sense and current source controller as described below.

The LED power source 10 further includes a primary, or power circuit, controller 22 which is connected to the power circuit 16 and the power limit 18.

The power circuit 16 includes a power factor conversion (PFC) boost 24, a DC/DC converter 26 and an output bus 28. The PFC boost 22 receives power from the AC mains input 12 while the output bus 28 is connected to the power limit 18. The primary controller 22 is connected to the PFC boost 24 and the DC/DC converter 26 to provide signals, such as control signals, to these circuits. A galvanic isolation barrier 30, typically implemented as part of a full bridge converter within the DC/DC converter 26, provides an electrical safety barrier between the low voltage of the output bus 28 and the high voltage levels of the AC mains input 12, the PFC boost 24 and the primary side of the DC/DC converter 26.

In a more specific embodiment of Figure 1a, the PFC boost 24 implements a boost power conversion topology with the input from the AC mains input 12 which is typically in the range of about 100 Vac to about 300 Vac. In this specific embodiment, the PFC boost 24 outputs a loosely regulated 430 Vdc over the input AC range. The DC/DC converter 26 is derived from an isolated switch mode buck converter topology. In the preferred embodiment, the output bus 28 provides a tightly regulated output, such as, but not limited to, about 46 Vdc which is controlled by a feedback loop to the primary controller 22 (as will be described in more detail below).

The power limit 18 provides an apparatus to limit power to the external LED load 14 in the event of an operational fault condition such as, but not limited to, a single component

failure within the LED power source 10. The single component failure may occur within the output current source, the current sense or the current source controller. The power limit 18 may also limit power in the event of an external LED load fault or over load condition. The operational fault condition may further include a high impedance fault at the LED load. An over load condition may be a transient condition such as a cold start or power up of an LED load in ambient temperatures less than 0 degrees Celsius or an improper LED load connected to the LED power source.

The power limit 18 includes a power monitor 32 (having a current sense 36), a secondary, or power limit, controller 38 (with a port 40) and a fault optocoupler 42. In the preferred embodiment, the port 40 includes five pins for in circuit serial programming of the controller 38 and at least one pin for calibration of the power limit 18. The secondary controller 38 performs a power calculation based on an assumed tightly regulated voltage on output bus 28 and monitored current sense 36 readings. Calibration may be required to account for component tolerances in the various circuits of the LED power source 10 such as in the power monitor 32 or variations in the output bus 28 voltage to establish accurate power calculations.

Connection between the power monitor 32 and the secondary controller 38 is via a sense line 39 while the secondary controller 38 is connected to the fault optocoupler 42 via a control line 43. The fault optocoupler 42 is also connected to the primary controller 22.

The current sense 36 provides at least one analog signal to the secondary controller 38 through the sense line 39. The current sense 36 typically includes a resistor connected in series with the output bus 28 and the output current source 44 and may include ancillary circuits to scale and filter the analog control signals before transmitting the signals to the appropriate analog to digital ports in the secondary controller 38.

In operation, the secondary controller 38 includes an averaging digital filter which takes a set, such as 1024, of readings for current over a period of time and then calculates an average value and compares this value to a predetermined power limit. In one embodiment, the predetermined power limit may be set at about 97 watts. If the power level is at or exceeds the predetermined limit, the secondary controller 38 will assert one or more power limit options.

The output current driver 20 includes an output current source 44 which is associated with, or connected to, a current sense 46. Both the output current source 44 and the current sense 46 are connected with a current source controller 48 (having a port 50) that is connected to the secondary controller 38 via a data line 49 and to the fault optocoupler 42 via data line 51. As shown in Figure 1, the output current driver 20 further includes an optional voltage sense 52 that is connected to the current sense 46, the current source controller 48 and the LED load 14.

The current source 44 and current sense 46 may include a switch mode buck topology with a MOSFET switch implementing a hysteretic control method. The current source 44 provides a regulated output current to the LED load 14 implemented by a feedback loop 58 to the current source controller 48. The current source controller 48 may also output a dimming signal, as a result of an over power condition, implemented through a gate drive control line 56 to the output current source 44. The current source controller is typically a digitally controlled device implemented by means of a microcontroller and firmware.

In terms of power limit options, one option may be to transmit a change in light intensity command through data line 49 to the current source controller 48. This control information or words of data, is preferably transmitted over a "sync" line, "clock" line and "data" lines. The start of each word is preferably delimited by the "sync" line and the start of each bit is delimited by the "clock" line. This control information is translated by the current source controller 48 to on-time and off-time information and transmitted as a gate pulse through control line 56 to the output current source 44 in order to reduce the average output current either gradually or stepwise to the LED load 14 and a subsequent gradual or stepwise increase in average current after a period of time.

Another power limit option may include a shutdown command via control line 43 to the fault optocoupler 42 to immediately disable the power circuit 16.

Alternatively, the secondary controller 38 may complete a sequence of tasks attempting to initially reduce the power being supplied to the LED load 14 then, if it is determined that the power being supplied is still beyond a predetermined power limit (as sensed by the power monitor 32), it will then assert a shutdown of the power circuit 16.

Graphs illustrating these operational fault conditions and how they may be handled in one embodiment are schematically illustrated in Figures 2a to 2d.

With further reference to output current driver 20, the current source controller 48 is further connected to the current source 44 and current sense 46 via control lines 56 and 58 respectively and also connected to port 50 for programming and calibrating various parameters. As shown in Figure 1, the voltage sense 52 is connected in parallel with the LED load 14, however, in other embodiments, the voltage sense 52 may be omitted.

In the current Figures and description, not all of the components or connections of the LED power source required for operation are shown as they will be understood by one skilled in the art. For example, the power circuit 16 may also include an EMI filter, inrush current limit or a bridge rectifier. With respect to connections, it will be understood that more than one sense line, control line or data line can be implemented between components even though only one line current connects these components. For example, more than one sense line may be connected between power monitor 32 and secondary controller 38 to provide current sense information to the secondary controller 38. Also, there may be multiple data line connections between the secondary controller 38 and current source controller 48.

In one embodiment of operation, the power circuit 16 is a two stage power converter comprising a PFC Boost 24 and DC/DC converter 26 both of which are controlled by the primary controller 22 to provide power to the output bus 28. The primary controller 22 transmits control signals to the PFC Boost 24 and DC/DC converter 26 and receives current sense information from the secondary controller 38. The output bus 28 typically provides a regulated voltage output with a feedback loop coupled to the primary controller 22.

Furthermore, the power from the output bus 28 is transferred to the output current source 44 of the output current divider 20 via the power limit 18. The power monitor 30 senses current or power (via the current sense 36) delivered from the output bus 28 and transmits this current information to the secondary controller 38.

In further aspects of operation, the current source 44 provides a constant current output to the LED load 14 while the current sense 46 provides a feedback signal to current source controller 48 to regulate the current supplied to the LED load 14. The output voltage

across the LED load 14 is variable and dependent on the forward voltage drops of the LED load 14.

The current source controller 48 regulates the output current provided to the LED load 14 and also provides apparatus for reducing the average current to the LED load 14 via a gate pulse signal with a variable duty cycle through control line 56.

With reference to power limit 18, the secondary controller 38 may be programmed to an initial predetermined power limit via port 40, such as, for example 97 watts. If necessary, subsequent calibration of the power limit is completed to account for electrical circuit tolerances or alternative predetermined power limit values. Calibration may include changing the state of the controller to "calibration mode" such as via a jumper connected to port 40; applying the appropriate load representing the predetermined power limit; and saving the applicable parameters by adjusting the constants stored in the EEPROM memory of the controller 38.

In another embodiment, the voltage sense 52 allows the current source controller 49 to monitor the power transferred to the LED load as a redundant power limit capability. In this instance, power is monitored by the current sense 46 and voltage sense 52 directly across the LED load 14. The redundant power limit capability provides back up protection in the event of a failure of the power limit 18.

In an alternative embodiment, the output current driver 20 may also perform a redundant power limit function similar to the power limit 18 whereby it can be programmed and calibrated to the predetermined power limit. In this embodiment, the secondary controller 38 is placed into calibration mode via port 40 in order to stop communication with the current source controller 48 and permit current source controller 48 to accept calibration commands through port 50.

The current sense 46 and voltage sense 52 communicate a measured value to the current source controller 48 in order to calculate power (given by the formula, power =voltage x current). If an operational fault condition such as an over power event occurs, the current source controller 48 may reduce the average current (or power) to the LED load 14 by a dimming pulse including a variable duty cycle through control line 56 to the current source 44

or the controller 48 may assert a shutdown signal through control line 51 to shut down the power circuit 16 or power source 10.

Alternatively, the current source controller 48, as part of a redundant power limit function, may also complete a sequence of attempting to reduce the output power to the LED load 14 first then, if it is determined that the output power level is still beyond predetermined limits as sensed by the voltage sense 52 or current sense 46 or both, it will then assert a shutdown of the power circuit 16.

The port 50 connected to current source controller 48 is also used for programming the output current driver 20 to the desired output current (such as, but not limited to, 350mA or 700mA) for the LED load 14.

Turning to Figure 1b, another embodiment of apparatus for providing power to a SSL device is shown. The embodiment of Figure 1b is similar to the embodiment of Figure 1a with the inclusion of a voltage sense 34 located within the power monitor 32. The embodiment of Figure 1b operates in a similar manner to the embodiment of Figure 1a, with the addition of further information relating to the voltage level being provided to the secondary controller.

The power limit 18 includes a power monitor 32 (having the voltage sense 34 and a current sense 36), a secondary controller 38 (with a port 40) and a fault optocoupler 42. In the preferred embodiment, the port 40 includes five pins for in circuit serial programming of the controller 38 and at least one pin for calibration of the power limit 18. The secondary controller 38 performs a power calculation based on the voltage on output bus 28 and monitored current sense 36 and voltage sense 34 readings. Calibration may be required to account for component tolerances in the various circuits of the LED power source 10 such as in the power monitor 32 or variations in the output bus 28 voltage to establish accurate power calculations

The current sense 36 and voltage sense 34 provide at least one analog voltage signal to the secondary controller 38 through the sense line 39. The current sense 36 typically includes a resistor connected in series with the output bus 28 and the output current source 44. The voltage sense 34 may include a resistor divider network connected in parallel with the output bus 28. Both the current sense 36 and the voltage sense 34 may include ancillary circuits to

scale and filter the analog control signals before transmitting the signals to the appropriate analog to digital ports in the secondary controller 38.

The voltage sense 34 is required if the output bus 28 is a loosely regulated or an unregulated voltage output such that the secondary controller 38 can perform a power calculation based on a voltage and current reading.

When the power from the output bus 28 is transferred to the output current source 44 of the output current divider 20 via the power limit 18, the power monitor 30 senses current (via the current sense 36) delivered from the output bus 28 and may also sense voltage (via the voltage sense 34) across the output bus 28 and transmits this current and/or voltage information to the secondary controller 38.

Turning to Figures 2a to 2d, schematic graphs illustrating various examples of LED power source operation when an operational fault condition occurs is shown. In the following graphs, the Y-axis relates to the power level being supplied to or used by the LED power source while the X-axis is a reflection on elapsed time. In the current figures, the power level reflected on the Y-axis is the power transmitted from output bus 28 to the input of output current source 44 by the current sense 36 and the voltage sense 34 (where appropriate).

Figure 2a is an exemplary graph of a power limit sequence where an internal fault occurs within the LED power source or an external fault occurs with the LED load. In this example, normal power is applied to the load (starting at time t0) until the operational fault condition occurs which causes the power level being supplied by the power source to increase resulting in the power level being supplied meeting or exceeding the predetermined power limit (or maximum power threshold) at t1. Upon sensing the predetermined power limit being met or exceeded, the power limit or a redundant power limit within output current driver will attempt to reduce the power while continuing to monitor the power level for a period of time (such as between t1 and t2). If the power limit is unable to reduce the power level being supplied to an acceptable level (which is less than the predetermined power limit) between t1 and t2, the LED power source 10 is disabled at t3 via known methods.

Figure 2b is an exemplary graph of a cold start scenario where the power being supplied to the LED load reaches or exceeds the predetermined power limit after start up at time (t0). In response to this, the power limit or redundant power limit within output current

driver steps down the power level being supplied to the LED load to a reduced power level (such as 75% of the normal power operation) at t1. It is understood that this example of a reduced power level is simply for explanation purposes and that any reduced power level is acceptable as long as it is less than the predetermined power limit. The supplied power level is continuously monitored for a period of time (t1 to t2) to confirm that the power level being supplied remains at the reduced power level. Starting at t_2, the power level being supplied is gradually increased for a time period (t2 to t3) in small increments towards the normal power level. In one example, the power can be increased at increments of 2.5% with a time interval between increments of 10 seconds until the normal power level is reached or sensed, however, any intervals relating to time or power may be selected.

Figure 2c is an exemplary graph of how another operation fault condition is handled. In the current graph, the predetermined power limit is met or exceeded at t1. In response to the power level being supplied meeting or exceeding the predetermined power limit, the power level being supplied is stepped down to a reduced level (between t1 and t2) and maintained at this level for a period of time (between t2 and t3). After time t3, the supplied power level may be gradually increased until the power level being supplied is to the normal operational power level. If the power level being supplied meets or exceeds the predetermined power limit again (such as the operational fault condition resulting in a rapid increase in power), such as at time t4, the LED power source is then disabled at t5.

Figure 2d is an exemplary graph of an operational fault condition involving a transient condition on the AC mains input. In the current graph, the input to the LED source from the AC mains input causes a transient voltage or current over shoot on the output bus resulting in a power level being supplied exceeding a predetermined power limit at t1. In response, the supplied power is stepped down at t2 and maintained at this reduced level for a period of time (between t2and t3) and the supplied power is then gradually increased to a normal power level at t4 while continuously being monitored.

Turning to Figure 5, a flowchart outlining a method of monitoring and limiting power provided to an SSL device when the power level being supplied meets or exceeds a predetermined power limit or threshold is shown. In operation, power is received 100 by the LED power source 10 from the AC mains input 12. After the power circuit 16 (acting as a

two stage power converter) receives the power, the primary controller 22 transmits control signals to the PFC boost 24 and the DC/DC converter 26 to produce an output voltage 102 which is transmitted via the output bus 28 to the power limit 18. The primary controller 22 also receives current sense information from the PFC boost 24 and DC/DC converter 26. Voltage sense information may be supplied in embodiments where a voltage sense is included in the apparatus.

After receiving the output voltage from the output bus 28, the power monitor 32 senses the characteristics of the output bus 104 such as the current delivered by the output bus 28 (via the current sense 36) and the voltage across the output voltage bus (if the voltage sense 34 is present) and transmits this information (106) to the secondary controller 38. In other words, the power being supplied to the LED load is monitored or sensed.

The secondary controller 38 compares the received current values, and possibly the received voltage values or both to predetermined power limits 108 (whereby power = voltage x current) stored within the secondary controller 38 or within a database associated with the secondary controller. This comparison is preferably performed with only the received or sensed current values. The secondary controller then determines if the received values meet or exceed the predetermined value 110 and may assert one or more options to limit output power to the LED load 112 if the predetermined value is met or exceeded and then controls the limited output power to the output current driver 114. If the predetermined power limit is not met or exceeded, the power level being supplied is directed to the LED load without needing to be limited.

More specifically, with respect to the one or more options to limit power 112, in one embodiment, when it is sensed that the power level being supplied meets or exceeds the predetermined power limit, the power level being supplied is reduced and then monitored for a period of time such that if the power limit is unable to reduce the power level to an acceptable level within a predetermined period of time, the LED power source is disabled (such as described in Figure 2a). In another embodiment of operation to limit power supplied to the load, when it is determined that the power supplied has met or exceeded a predetermined power limit, the power level being supplied is reduced to a percentage of the normal operation power level being supplied and then gradually increased until the power

level being supplied reaches the normal operation power level. In yet a further embodiment, the power supplied is reduced to a percentage of the normal operation power level and then gradually increased until the supplied power level reaches the normal operation power level. However, if the normal operation power level is not reached whereby the power level being supplied again meets or exceeds the predetermined power limit, the LED power source is disabled.

As will be understood, the secondary controller 38 may limit the power from the output bus in other scenarios, such as, but not limited to transmitting a signal through a data line to the current source controller 48 to reduce the average output current either gradually or stepwise to the LED load 14 and a subsequent or stepwise increase in average current after a period of time. Alternatively, the secondary controller 38 may complete a sequence of tasks attempting to reduce the output power to the LED load first and them if it is determined that the power level being supplied still exceeds beyond a predetermined power limit, as sensed by the power monitor 32, assert a shutdown of the power circuit 16.

Turning to Figure 3a, another embodiment of apparatus for providing power to a SSL device, such as an LED power source 10 is shown. The LED power source 10 includes a power circuit 16, an output current driver 20, a primary controller and a fault optocoupler. In this embodiment, the power limit functionality is performed via a current sense 46 and controller 48 integrated within the output current driver 20. The power circuit 16 includes a power factor conversion (PFC) boost 24, a DC/DC converter 26 and an output bus 28. The PFC boost 22 receives the power from the AC mains input 12 while the output bus 28 is connected to the output current driver 20. The primary controller 22 is connected to the PFC boost 24 and the DC/DC converter 26 to provide signals to these components. A galvanic isolation barrier 30 is integrated within the DC/DC converter 26 to provide an electrical safety barrier between the low voltage of the output bus 28 and the high voltage levels of the AC mains input 12, the PFC boost 24 and the DC/DC converter 26.

The output current driver includes an output current source 44 which is associated with, or connected to, a current sense 46. Both the output current source 44 and the current sense 46 are connected to a current source controller 48 (having a port 50) that is also connected to the secondary controller 38 via a data line.

Turning to Figure 3b, another embodiment of apparatus for providing power to a SSL device, such as an LED power source 10 is shown. The LED power source 10 includes a power circuit 16, an output current driver 20, a primary controller and a fault optocoupler. In this embodiment, the power limit functionality is performed by a current sense 46, voltage sense 52, and controller 48 is integrated within the output current driver 20. The power circuit 16 includes a power factor conversion (PFC) boost 24, a DC/DC converter 26 and an output bus 28. The PFC boost 24 receives the power from the AC mains input 12 while the output bus 28 is connected to the output current driver 20. The primary controller 22 is connected to the PFC boost 24 and the DC/DC converter 26 to provide signals to these components. A galvanic isolation barrier 30 is located between the DC/DC converter 26 and the output bus 28 to provide an electrical safety barrier between the low voltage of the output bus 28 and the high voltage levels of the AC mains input 12, the PFC boost 24 and the DC/DC converter 26.

The output current driver includes an output current source 44 which is associated with, or connected to, a current sense 46. Both the output current source 44 and the current sense 46 are connected to a current source controller 48 (having a port 50) that is also connected to the secondary controller 38 via a data line. The output current driver 20 further includes a voltage sense 52 that is connected to the current sense 46, the current source controller 48 and the LED load 14.

Turning to Figure 4a, yet another embodiment of apparatus for providing power to a SSL device, such as an LED power source 10 is shown. The power source 10 includes a power circuit 16 which is connected to a power limit 18 which, in turn, is connected to an output current driver 20.

The power circuit 16 includes a power factor conversion (PFC) boost 24, a DC/DC converter 26 and an output bus 28. The PFC boost 22 receives the power from the AC mains input 12 while the output bus 28 is connected to the power limit 18. The primary controller 22 is connected to the PFC boost 24 and the DC/DC converter 26 to provide signals to these components. A galvanic isolation barrier 30 is located within the DC/DC converter 26 to provide an electrical safety barrier between the low voltage of the output bus 28 and the high voltage levels of the AC mains input 12, the PFC boost 24 and the DC/DC converter 26.

The power limit 18 includes a power monitor 32 (including a current sense 36), connected to a secondary controller 38 with a port 40 and a fault optocoupler 42. The secondary controller 38 is connected to a fault optocoupler 42 via a control line while the fault optocoupler 42 is also connected to the primary controller 22.

The output current driver includes an output current source 44 which is associated with, or connected to, a current sense 46. Both the output current source 44 and the current sense 46 are connected with a current source controller 48 (having a port 50) that is also connected to the secondary controller 38 via a data line.

Turning to Figure 4b, yet another embodiment of apparatus for providing power to a SSL device, such as an LED power source 10 is shown. The power source 10 includes a power circuit 16 which is connected to a power limit 18 which, in turn, is connected to an output current driver 20.

The power circuit 16 includes a power factor conversion (PFC) boost 24, a DC/DC converter 26 and an output bus 28. The PFC boost 22 receives the power from the AC mains input 12 while the output bus 28 is connected to the power limit 18. The primary controller 22 is connected to the PFC boost 24 and the DC/DC converter 26 to provide signals to these components. A galvanic isolation barrier 30 is located within the DC/DC converter 26 to provide an electrical safety barrier between the low voltage of the output bus 28 and the high voltage levels of the AC mains input 12, the PFC boost 24 and the DC/DC converter 26.

The power limit 18 includes a power monitor 32 (comprising a voltage sense 34 and a current sense 36), connected to a secondary controller 38 with a port 40 and a fault optocoupler 42. The secondary controller 38 is connected to a fault optocoupler 42 via a control line while the fault optocoupler 42 is also connected to the primary controller 22.

The output current driver includes an output current source 44 which is associated with, or connected to, a current sense 46. Both the output current source 44 and the current sense 46 are connected with a current source controller 48 (having a port 50) that is also connected to the secondary controller 38 via a data line. The output current driver may include a voltage sense (not shown) that is connected to the current sense 46, the current source controller 48 and the LED load 14.

In an alternative embodiment, the power circuit 16 may further include at least one of an electromagnetic interference (EMI) filter, an inrush current limit and/or a bridge rectifier.

In a further embodiment, the power circuit 16 may include alternative DC/DC converter topologies. Such power conversion topologies may include, but are not limited to, a half bridge resonant converter, a flyback, or forward converter topologies. The primary controller 22 may also be two separate controllers to provide individual gate drive and feedback control signals to the PFC boost 24 and DC/DC converter 26.

With reference to power limit 18, further embodiments may include an op amp or comparator as opposed to an analog to digital port. Other embodiments may also include alternate filtering methods such as, but not limited to, a moving average filter to filter the power monitor readings.

With reference to transmitting a change in light intensity command through data line 49, alternate embodiments may include a UART, an I^2C bus, SPI (Serial Peripheral Interface Bus) or a parallel communication apparatus. Other changes in light intensity or dimming methods may include a pulse width modulation method or a constant current reduction method (CCR) or a combination of various other methods. The CCR method is a continuous current flow through a LED that is reduced in order to reduce the brightness of the LED. In another embodiment, the dimming method may be implemented by various methods such as those disclosed in US Patent 8,299,987 or in US Patent Publication No. 2013/0049634 which are herein incorporated by reference.

In a further embodiment, the output current source 44 may further include other topologies such as boost, buck-boost, or SEPIC (single ended primary inductor converter). Alternate embodiments may also include an analog controller as opposed to a digital controller where no firmware is required for implementation. Other control methods to regulate output current to the LED load 14 may include pulse width modulation.

As an alternate embodiment, the output current source 20 may be a linear regulator with a constant current output as opposed to a switch mode topology. With respect to the secondary controller 38 and the current source controller 48, the power limit function and regulation of output current may be implemented by means of a single controller.

The above-described embodiments are intended to be examples only. Alterations, modifications and variations can be effected to the particular embodiments by those of skill in the art without departing from the scope, which is defined solely by the claims appended hereto.

What is claimed is:

1. Apparatus for controlling power to a solid state lighting (SSL) device load comprising:

a power circuit for receiving power from an external source;

at least one power limit connected to the power circuit;

at least one output current driver for supplying a load power to the SSL device load, the at least one output current driver connected to the at least one power limit; and

a power limit controller;

wherein the power circuit transmits the power to the at least one power limit which, in turn, transmits a current to the at least one output current driver;

wherein the power limit controller directly or indirectly monitors a level of the load power and controls the at least one power limit to reduce the level of the load power for a predetermined period of time when the load power exceeds a predetermined power limit.

2. The apparatus of Claim 1 wherein the at least one power limit is integrated within one of the at least one output current drivers.

3. The apparatus of Claim 1 wherein the at least one power limit comprises:

the power limit controller;

a power monitor; and

a fault optocoupler,

wherein if the load power exceeds the predetermined power limit, the power limit controller transmits a signal to the fault optocoupler to control the load power.

4. The apparatus of Claim 3 further comprising:

a power circuit controller;

wherein the fault optocoupler transmits a signal to the power circuit controller to control the power being supplied to the power limit.

5. The apparatus of Claim 1 wherein the at least one output current driver comprises:

an output current source;

a current sense; and

a current source controller.

6. The apparatus of Claim 5 wherein if the load power exceeds the predetermined power limit, the power limit controller transmits a signal to the current source controller to control the load power to the load.

7. The apparatus of Claim 1 wherein the power limit controller comprises a digital filter.

8. The apparatus of Claim 7 wherein the power limit controller comprises at least one port.

9. The apparatus of Claim 8 wherein the at least one port receives instructions to calibrate the at least one power limit to the predetermined power limit.

10. The apparatus of Claim 2 wherein the power monitor comprises a current sense.

11. The apparatus of Claim 6 wherein the at least one output current driver reduces the load power by a pulsing apparatus.

12. A method of controlling power to a solid state lighting (SSL) device load comprising:

receiving an input power;

delivering load power to the SSL device load;

monitoring current level in load power;

limiting load power to the SSL device for a predetermined period of time after a predetermined operational fault condition is met.

13. The method of Claim 12 wherein the predetermined operational fault condition is one of a single component failure, an external light emitting diode (LED) fault and an overload condition.

14. The method of Claim 12 wherein monitoring current level in load power comprises:

sensing current delivered by an output bus to a power limit or sensing current delivered to a load by an output current driver.

15. The method of Claim 12 further comprising:

gradually increasing load power to a normal operational power level.

16. The method of Claim 15 wherein the load power is gradually increased at predetermined time intervals.

17. The method of Claim 15 wherein the load power is gradually increased in predetermined power increments.

18. The method of Claim 12 wherein if a maximum power threshold is met, load power delivered to the load is disabled.

19. The apparatus of Claim 2 wherein the at least one power limit comprises:

the power limit controller;

a power monitor; and

a fault optocoupler,

wherein if the load power exceeds the predetermined power limit, the power limit controller transmits a signal to the fault optocoupler to control the load power.

20. The apparatus of Claim 6 wherein the at least one output current driver reduces load power by a constant current apparatus.

21. The apparatus of Claim 1 wherein the SSL device load is one of an organic light emitting diode (OLED) load, a light emitting diode (LED) load or a LED array load.

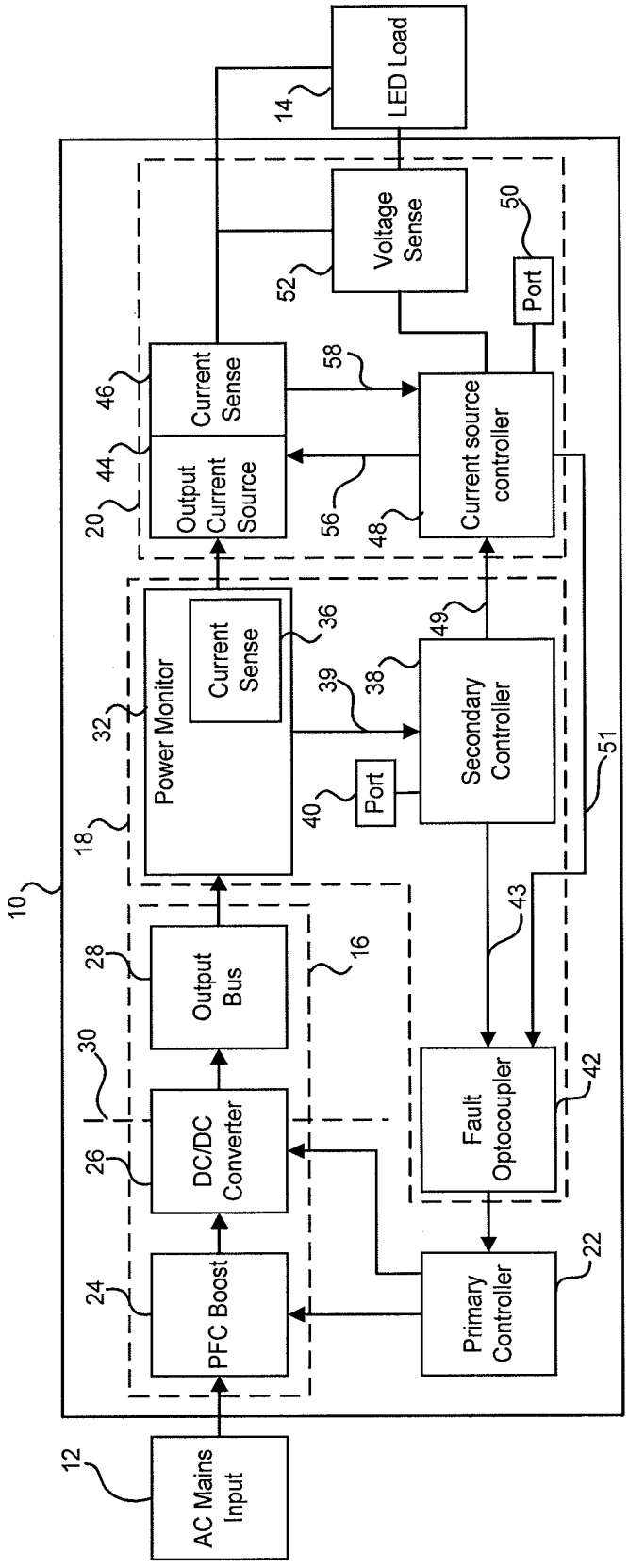

LED Load
14
Voltage Sense
52
Port
50
Current Sense
46
Output Current Source
44
20
58
56
48
Current source controller
Power Monitor
32
Current Sense
36
39
38
49
Secondary Controller
Port
40
18
51
10
Output Bus
28
16
30
DC/DC Converter
26
Fault Optocoupler
42
43
PFC Boost
24
Primary Controller
22
AC Mains Input
12

FIGURE 1a

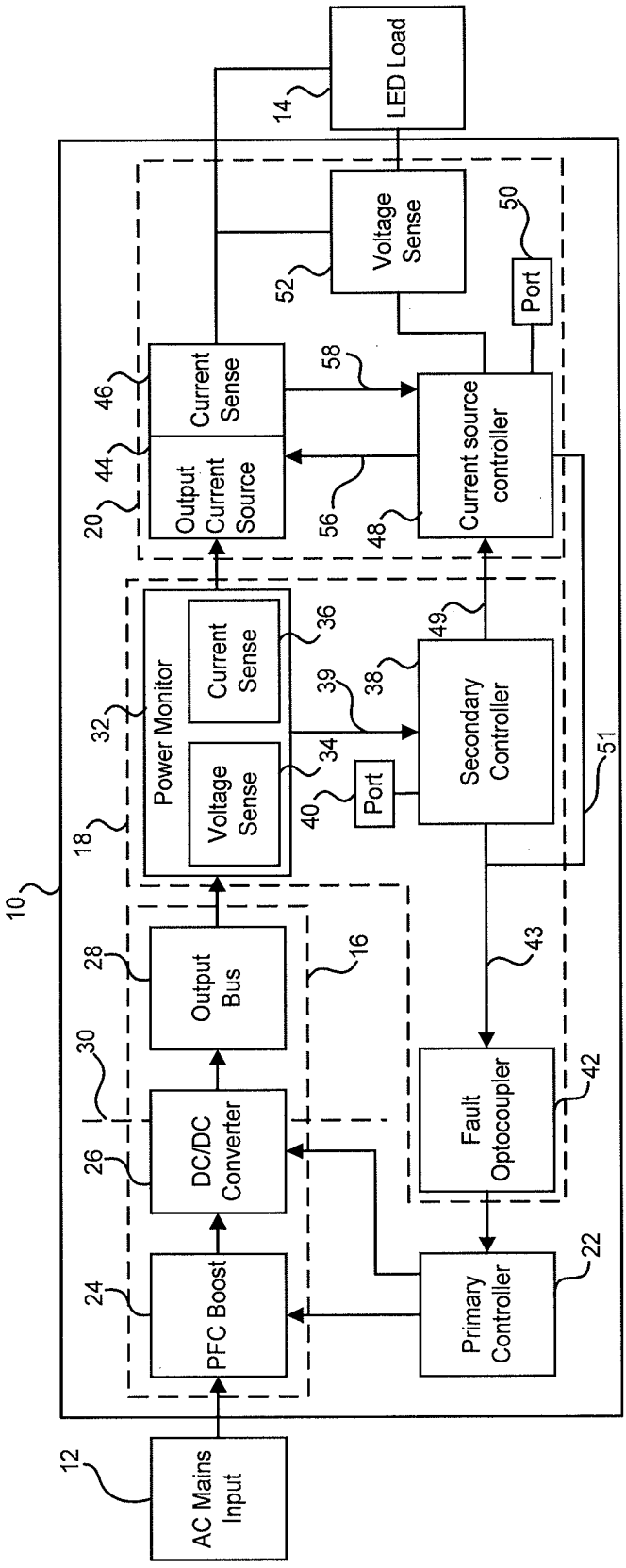

LED Load
14
Voltage Sense
52
50
Port
Current Sense
46
58
Output Current Source
44
20
56
48
Current source controller
Power Monitor
32
Current Sense
36
49
39
38
Voltage Sense
34
Port
40
Secondary Controller
18
51
10
Output Bus
28
16
43
30
DC/DC Converter
26
Fault Optocoupler
42
PFC Boost
24
Primary Controller
22
AC Mains Input
12

FIGURE 1b

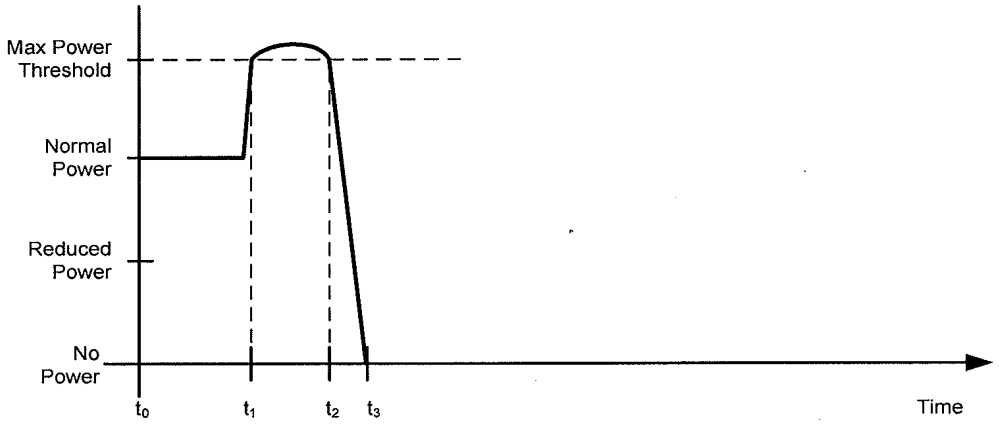


FIGURE 2a

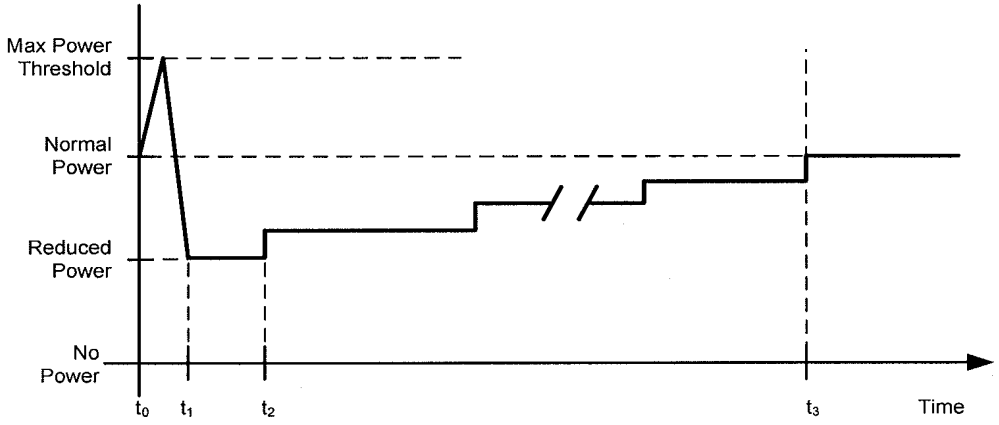


FIGURE 2b

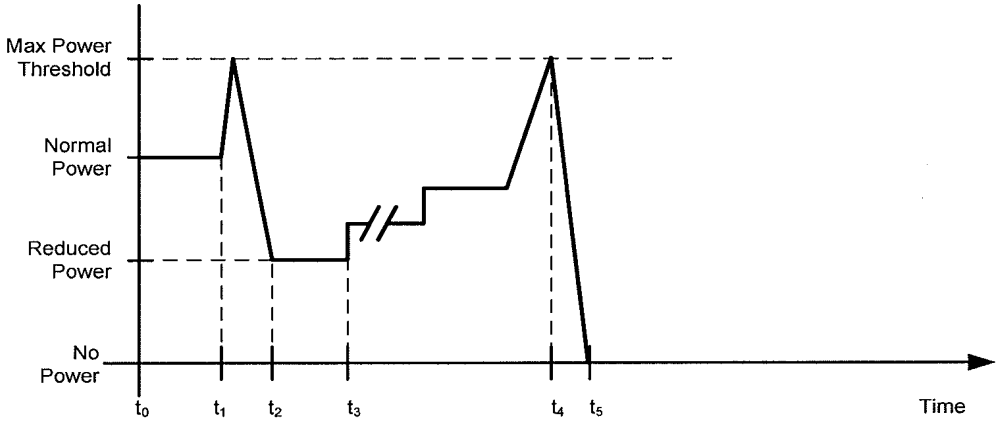


FIGURE 2c

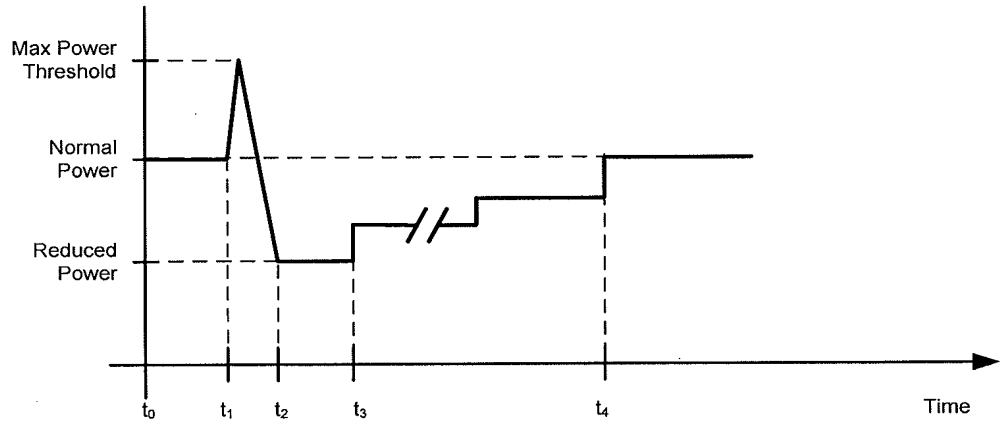

Max Power Threshold
Normal Power
Reduced Power
t_0
t_1
t_2
t_3
t_4
Time

FIGURE 2d

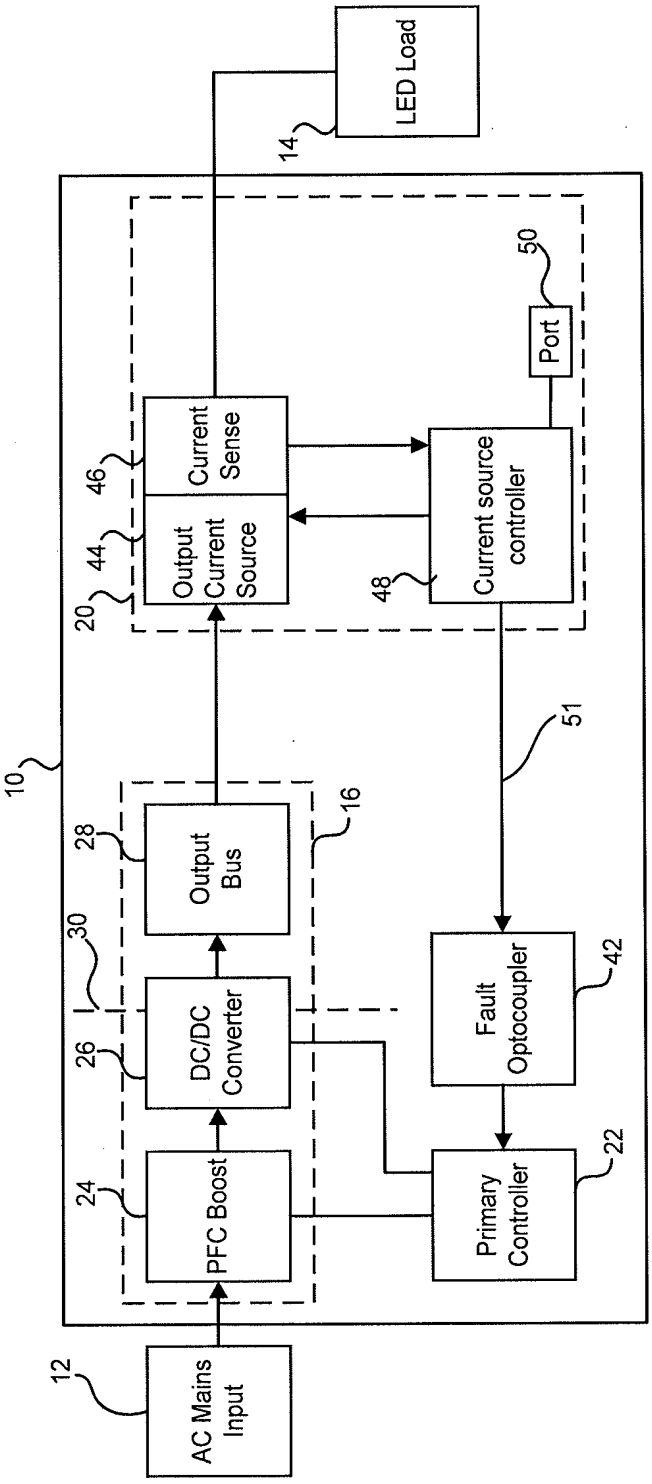

LED Load
14
10
20
Current Sense
46
Output Current Source
44
Current source controller
48
Port
50
51
Output Bus
28
16
30
DC/DC Converter
26
PFC Boost
24
Fault Optocoupler
42
Primary Controller
22
AC Mains Input
12

FIGURE 3a

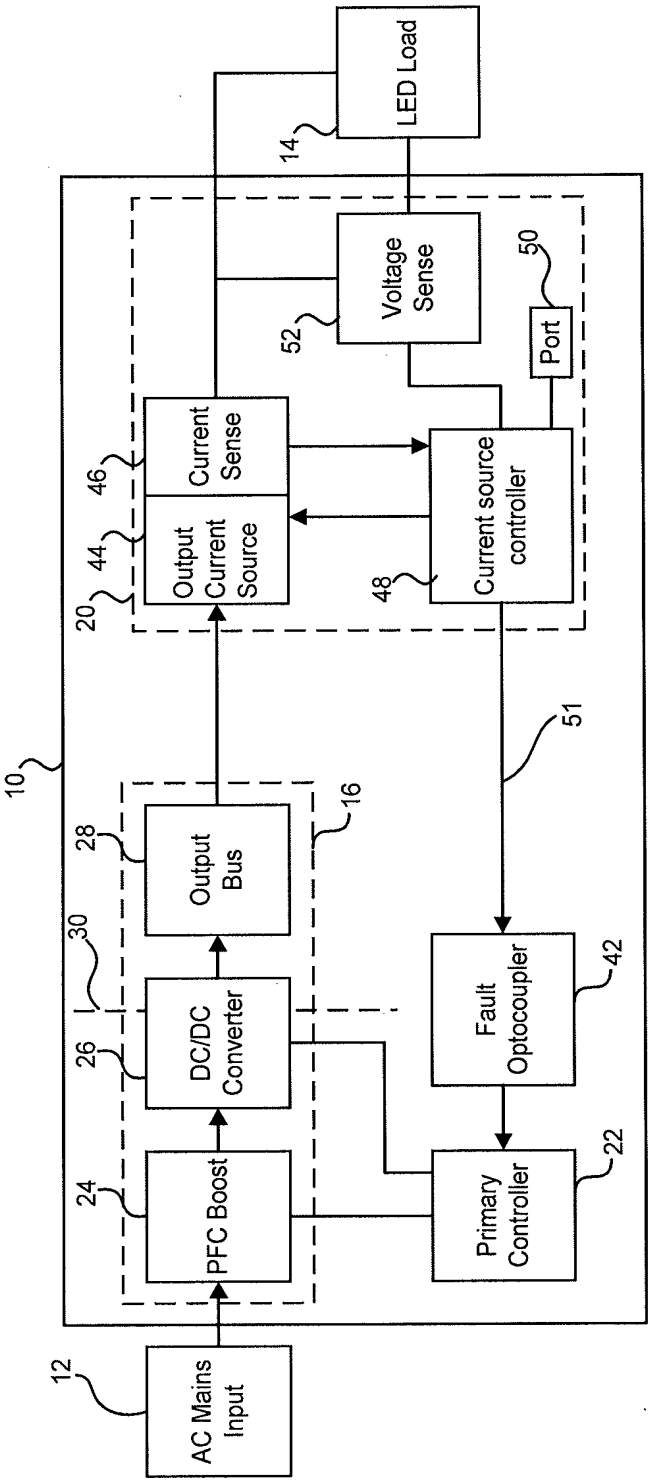

LED Load
14
Voltage Sense
52
Port
50
Current Sense
46
Output Current Source
44
20
Current source controller
48
51
10
Output Bus
28
16
30
DC/DC Converter
26
Fault Optocoupler
42
PFC Boost
24
Primary Controller
22
AC Mains Input
12

FIGURE 3b

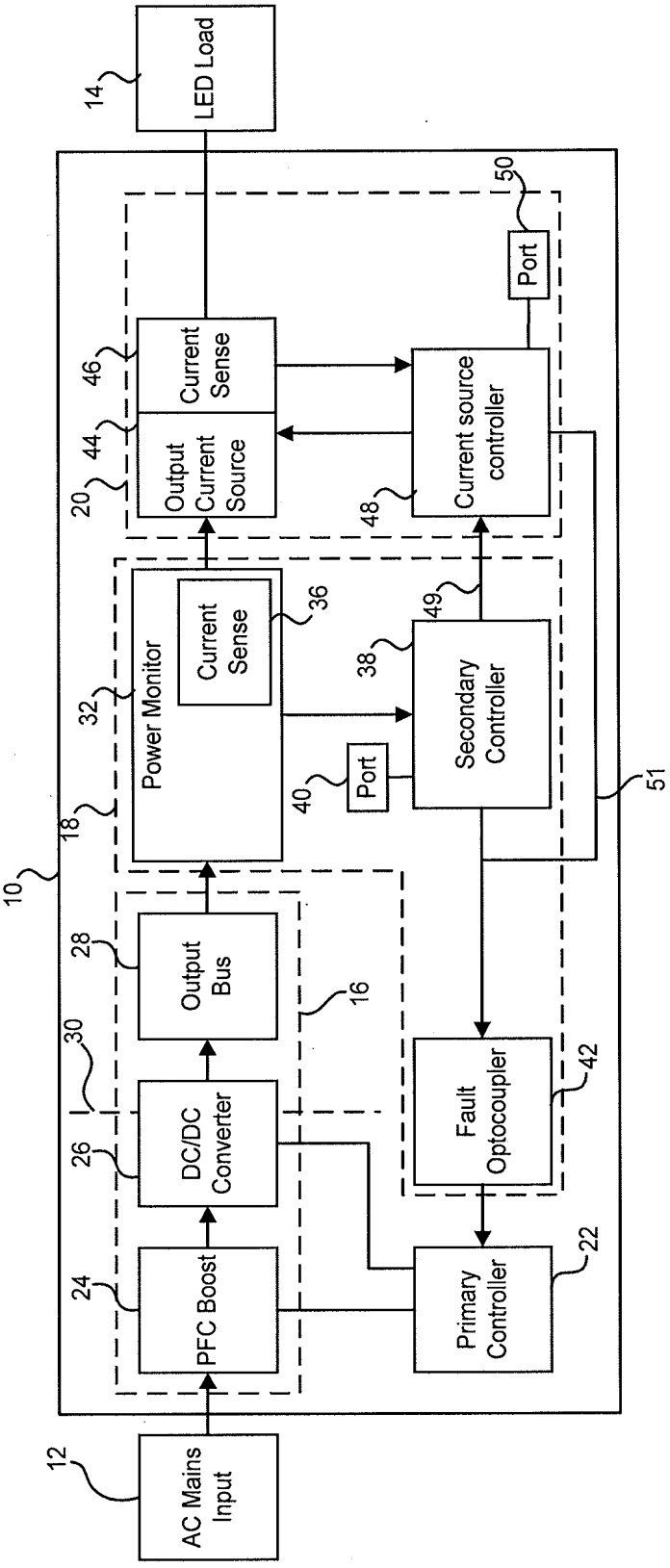

LED Load
14
50
Port
46
Current Sense
44
Output Current Source
20
48
Current source controller
49
36
Current Sense
32
Power Monitor
38
Secondary Controller
40
Port
18
51
10
28
Output Bus
16
30
26
DC/DC Converter
42
Fault Optocoupler
24
PFC Boost
22
Primary Controller
12
AC Mains Input

FIGURE 4a

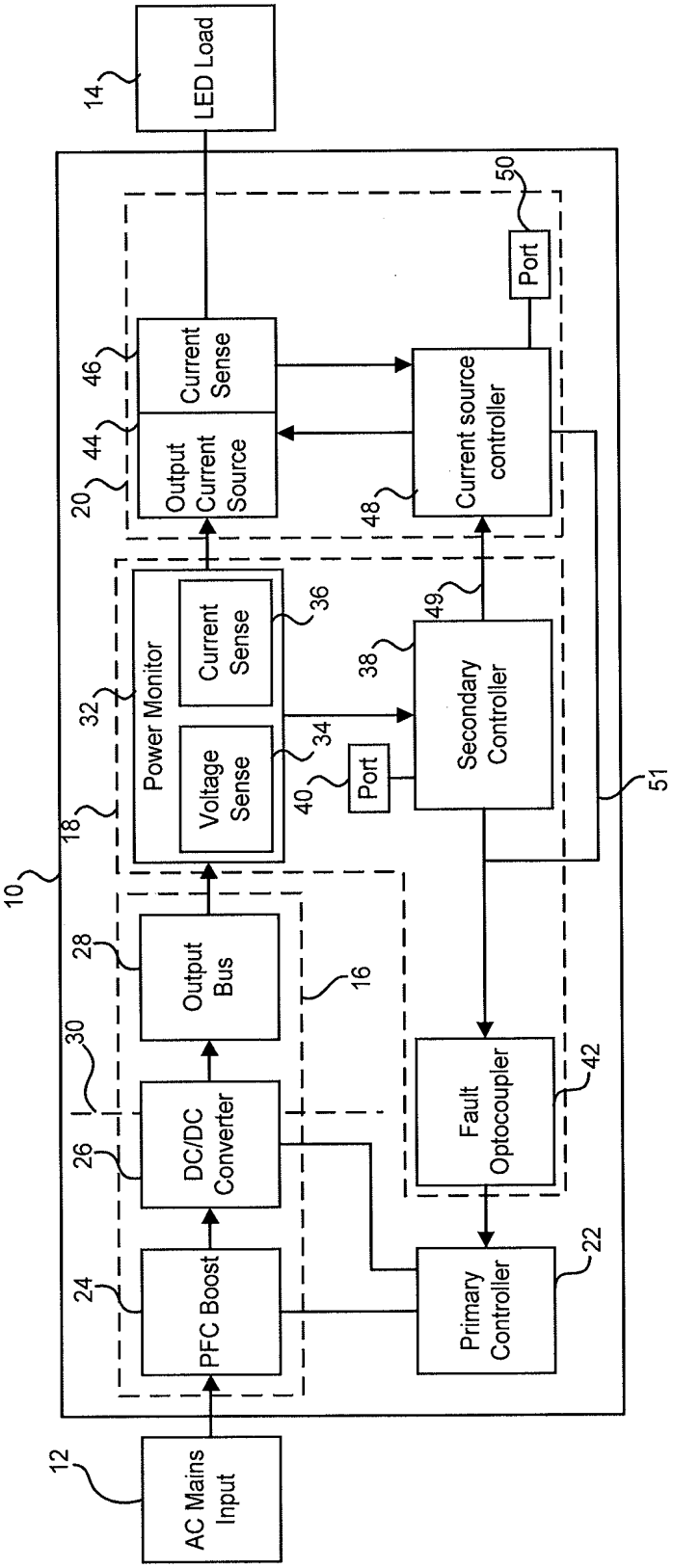

LED Load
14
50
Port
46
Current Sense
44
Output Current Source
20
48
Current source controller
49
38
Secondary Controller
32
Power Monitor
Current Sense
36
Voltage Sense
34
40
Port
18
51
10
28
Output Bus
16
30
26
DC/DC Converter
24
PFC Boost
42
Fault Optocoupler
22
Primary Controller
12
AC Mains Input

FIGURE 4b

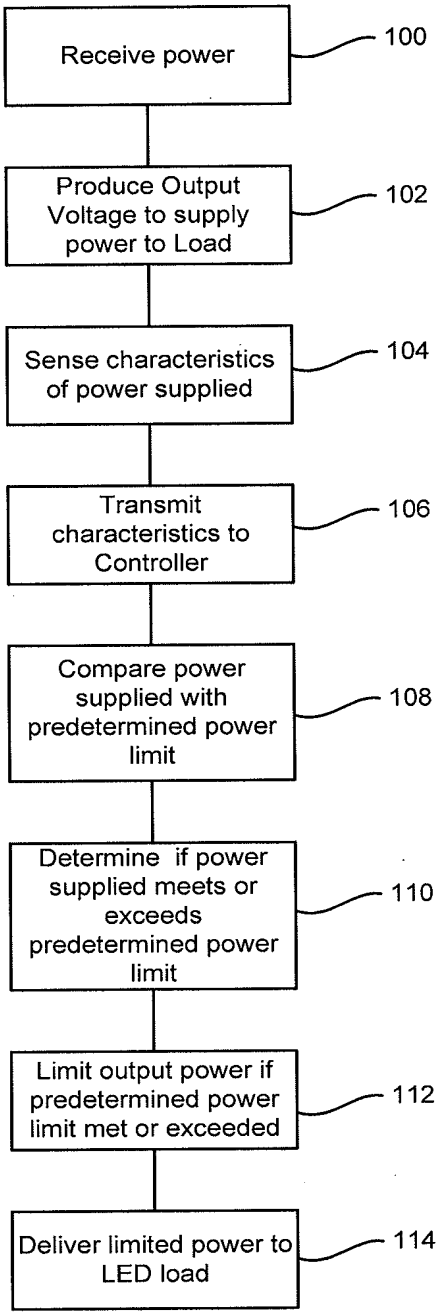

Receive power
100
Produce Output Voltage to supply power to Load
102
Sense characteristics of power supplied
104
Transmit characteristics to Controller
106
Compare power supplied with predetermined power limit
108
Determine if power supplied meets or exceeds predetermined power limit
110
Limit output power if predetermined power limit met or exceeded
112
Deliver limited power to LED load
114

FIGURE 5