

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED LIGHTING CONCEPTS LLC,
Petitioner

v.

MATE LLC.,
Patent Owner

Case No. IPR2023-01259

U.S. Patent No. 9,591,713

DECLARATION OF JOSEPH C. McALEXANDER IN SUPPORT OF
PETITIONER'S PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT
NO. 9,591,713 UNDER 35 U.S.C. §§311-319 AND 37 C.F.R. §42.100 ET SEQ.

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INTRODUCTION

1. My name is Joseph C. McAlexander III, President of McAlexander Sound, Inc., located at 101 W. Renner Rd., Suite 350, Richardson, TX 75082. I have been retained by Munsch Hardt Kopf and Harr, Counsel for Advanced Lighting Concepts LLC d/b/a Environmental Lights (“EL”) in connection with the above-captioned matter, to provide my analyses and conclusions in this *inter partes* review proceeding before the United States Patent and Trademark Office regarding U.S. Patent No. 9,591,713 (“the ‘713 Patent”).

2. I understand that mate., LLC is the Plaintiff and that EL is the Defendant in a patent infringement case filed in the United States District Court for the Southern District of California, Civil Action No. 3:22-cv-0195-CAB-DEB.

3. I submit this declaration based on my personal knowledge and experience, as well as the materials that I reviewed and considered in formulating my opinions.

QUALIFICATIONS AND EXPERIENCE

4. I am a technical expert in the subject matter areas relevant to the ‘713 Patent, including the design and testing of LED drivers and dimmers. I am qualified to reach the opinions and conclusions stated in this Declaration. I address my background and qualifications in Section I below and provide additional detail in my CV submitted with this report.

5. I am the Founder and President of M^cAlexander Sound, Inc., formerly IP Director of CCI and Vice President of EPI Technologies, Inc.

6. I am a Registered Professional Engineer (#79454) in the State of Texas and am also a senior lifetime member of the Institute of Electrical and Electronics Engineers, Inc. (IEEE) and, in particular, have joined the Computer, Electron Devices, and Solid-State Circuits societies of IEEE. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University and completed 1.5 years of graduate level studies in Neurophysiology at the University of Texas Graduate School of Biomedical Science. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 50 years and am a named inventor on 31 U.S. patents and a number of foreign patents, some of which are related to LED systems.

7. My skills and experience are in the areas of circuit design and analysis, device fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, software development, management, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level

shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;

- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and Fast Fourier Transform (FFT) for High Aspect Ratio Inspection (HARI) applications;
- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control; provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

8. Of particular relevance is my experience as an integrated circuit designer, manager, and consultant. I spent nine years designing integrated circuit products at Texas Instruments, Inc., and an additional five years there managing wafer fabrication operations and assembly (packaging), test, and reliability analysis facilities. As such, I participated directly in the strategic design and process decisions required to bring competitive products to market and managed cost and revenue (both projected and actual) associated with those marketed products. I also worked directly with clients regarding product manufacturer-to-customer

integration, implementing direct-ship-to-customer productivity enhancements and establishing and executing product reliability and performance assessment studies. Often, such analyses suggested that certain modifications be made to design, fabrication, or assembly structures or methods, or to product flow and distribution. It was my responsibility to implement selected improvements to achieve the designated goals without negatively impacting the revenue models and time-to-market projections while maintaining and improving product yield and reliability.

9. As a designer and design manager, for example, I developed new, leading edge technology designs from conception to production. As such, my designs were always created in parallel with innovations in design simulation, in wafer processing, and in packaging architecture. I had to develop simulation behavioral models, tested against actual prototype designs, to determine the most appropriate fit between design, process, and assembly to deliver the best product to the market. In each case, my product prototype and production designs worked the first time; and the memory products were widely accepted in the market by major OEM companies.

10. I also worked with consumers evaluating performance of my designs in system applications to better match those designs to the consumers' requirements. New outgoing test methods and algorithm test patterns were designed to improve overall performance and reliability and to provide feedback for design and process

improvements. I thus developed a comprehensive understanding of the key factors, such as design, process, assembly, cost, equipment, facility, personnel resources, and timing necessary to bring a product from conception to market. These factors have continued to be key contributors to the success of products throughout the history of integrated circuits, even to the present.

11. Additionally, I have evaluated and provided expert services related to memory technology, both as standalone components and as components integrated into memory modules and systems, and also process and design technologies of various devices including microprocessors, controllers, memory, and programmable logic. I have also provided expert services related to product procurement and contract purchase order fulfillment according to contract agreement deliverables. I am also knowledgeable of communication control, addressing, and data transfer protocol as it relates to system architecture.

12. Additionally, I have innovations in the areas of LED technology, as embodied in a number of my patents, including LED drivers.

13. Because of my background, education, training, and experience, I am qualified as an expert to opine on the technology and other, related technical factors. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae. Ex. 1003.

I. METHODOLOGY AND MATERIALS CONSIDERED

14. My opinions expressed herein are based on my review of the U.S. Patent Nos. 8,525,446 (“the ‘446 Patent”), 8,957,601 (“the ‘601 Patent”), 9,049,759 (“the ‘759 Patent”), 9,078,310 (“the ‘310 Patent”), 9,320,093 (“the ‘093 Patent”) and 9,591,713 (“the ‘713 Patent”) (collectively, the “Challenged Patents”), their respective prosecution histories (including several patents listed within those prosecution histories), extrinsic evidence relating to the technology of the Challenged Patents, and other evidence cited in this declaration.

15. I further understand that this application is a national stage filing under 35 U.S.C. 371 of International Patent Application PCT/CA2009/001295, filed on September 17, 2009, which claims the benefit of priority of U.S. Provisional Application No. 61/097,963, filed September 18, 2008, and that the Patents all but the ‘713 Patent share the same specification. My opinions are also based on my technical experience, knowledge, and expertise in the area of LED drivers and dimmers.

16. More specifically, for this work, I have been asked to review the ‘713 Patent including the specification and claims, and the ‘713 Patent’s prosecution history (file history). In developing my opinions related to the ‘713 Patent, I have considered the materials cited herein, including those items itemized in the Exhibit Table below.

<u>EXHIBIT</u>	<u>DESCRIPTION</u>
Ex. 1001	U.S. Patent No. 9,591,713
Ex. 1004	File Wrapper for U.S. Patent No. 9,591,713
Ex. 1005	U.S. Patent 9,173,273 to Zudrell-Koch
Ex. 1006	U.S. Patent Application No. US20140103804A1 to Zhdanau
Ex. 1007	U.S. Patent Application No. US20130063047A1 to Veskovic

17. This declaration contains my opinions with respect to the subject matter of this proceeding and with the understandings as set forth herein. I specifically reserve the right to formulate and offer additional or supplemental opinions based on any additional information, depositions, discovery, or evidence that may be provided or derived, future court rulings, or agreements between the parties, to the extent permitted by the Board.

II. OVERVIEW OF LEGAL STANDARDS

18. I do not have any formal legal training, and I am not an attorney. EL's counsel has informed me of certain legal principles that I applied in my analysis. Those legal principles are summarized below.

19. I understand that patent claims are presumed valid and cannot be invalidated unless there is a showing the preponderance of the evidence demonstrates that the claim is invalid.

20. The following section summarizes the law as I have been instructed to apply it in formulating and rendering my opinions found later in this declaration. I

understand that, in an *inter partes* review proceeding, patent claims may be deemed unpatentable if it is shown that they were anticipated or rendered obvious in view of the prior art. I understand that prior art in an *inter partes* review is limited to patents or printed publications that predate the priority date of the patent at issue.

A. Person of Ordinary Skill in the Art

21. I was asked to provide my opinion as a person of skill in the art as it relates to the '713 Patent during the period leading up to the earliest claimed priority date. I considered several factors, including the types of problems encountered in the art, the solutions to those problems, the pace of innovation in the field, the sophistication of the technology, and the education level of active workers in the field. I provide that level below in Section V.

B. Anticipation

22. I understand that, when determining whether a claim is anticipated, is based on underlying factual issues including the content of the prior art and the level of ordinary skill in the art. I further understand that, for a single reference to anticipate a claim, the four corners of that document describes every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation.

23. I understand that invalidity for anticipation requires that the identical invention must be shown in as complete detail as contained in the patent claim.

C. Obviousness

24. I understand that when determining whether a claim is “obvious,” the analysis is based on underlying factual issues including the content of the prior art and the level of ordinary skill in the art. I further understand that for a single reference or a combination of references to render the claimed invention obvious, a POSITA must have been able to arrive at the claims by modifying or combining the references.

25. I have further been informed and understand that a claim is unpatentable as obvious if the difference between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a POSITA at the time the invention was made.

26. I also have been informed and understand that the combination of familiar elements according to known methods is obvious when it does no more than yield predictable results. However, I further understand that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. I understand that to prove a claim would have been obvious, one must demonstrate that a POSITA would have been motivated to combine or modify the prior art to achieve the claimed invention, while having a reasonable expectation of success in doing so.

27. I further understand that a claim may be obvious if common sense directs one to combine multiple prior art references or add missing features to reproduce the alleged invention recited in the claims. I also understand that if a POSITA could implement a predictable variation, then the claim is likely unpatentable. For the same reason, if a technique has been used to improve one device and a POSITA would recognize that it would improve similar devices in the same way, then using the technique is obvious. I further understand that a claim can be obvious if it combines old elements with no change to their respective functions, or alters prior art by merely substituting one element for another known in the field to yield a predictable result.

D. Claim Construction

28. I have been advised that “in an *inter partes* review proceeding, a claim of a patent . . . shall be construed using the same claim construction standard that would be used to construe the claim in a civil action . . . , including construing the claim in accordance with the ordinary and customary meaning of such claim as is understood by” a person of ordinary skill in the art (“POSITA”). 37 C.F.R. § 42.100(b). Each claim term in the ‘446 Patent should be construed in accordance with its ordinary and customary meaning for the purposes of resolving the issues raised in the Petition.

29. I have followed these principles in my analysis throughout this declaration.

III. LEVEL OF ORDINARY SKILL IN THE ART

30. In determining the characteristics of a person of ordinary skill in the art at the time of the claimed invention, several things should be considered, including the factors discussed below, as well as (1) the levels of education and experience of the inventor and other persons actively working in the relevant field; (2) the types of problems encountered in the field; (3) prior art solutions to these problems; (4) the rapidity in which innovations are made; and (5) the sophistication of the relevant technology.

31. All of the opinions that I provide herein are provided through the lens of a person having ordinary skill at the relevant time (prior to 2006, which I understand is the priority date claimed by the '713 Patent). In my opinion, a person having ordinary skill in the art ("POSITA") at the time of the alleged invention would have had at least a bachelor's degree in electrical engineering, computer science, or a related field and significant experience with power regulation devices, like LED drivers and dimmers.

32. I am prepared to testify as an expert in this field and also as someone who had at least the knowledge of a POSITA, and someone who worked with other POSITAs at the time of the alleged invention.

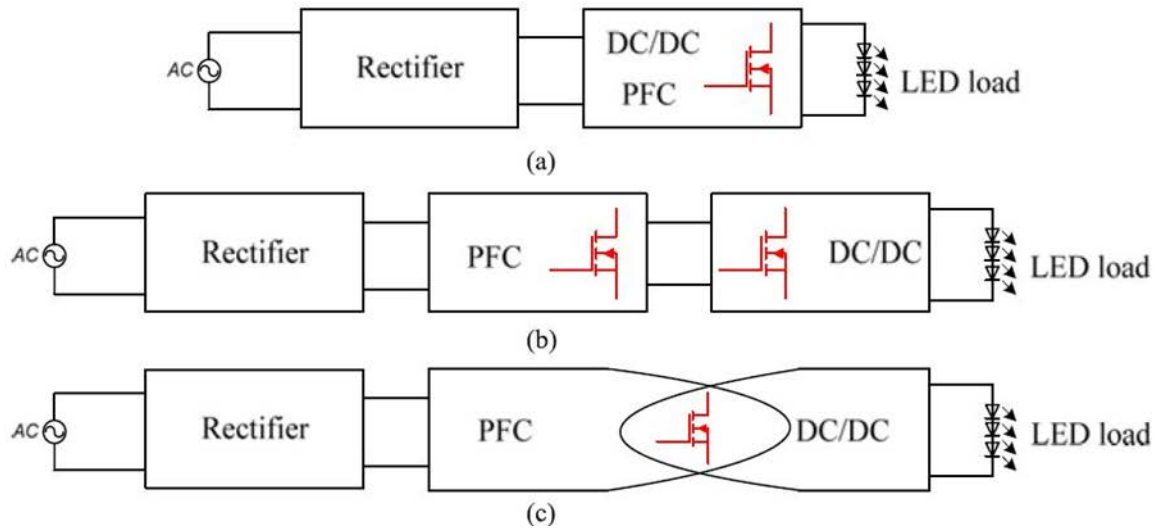
IV. TECHNICAL BACKGROUND AND THE ‘713 PATENT

A. Background of the Relevant Technology

33. The Challenged Patents relate to LED drivers. “LED drivers are devices that regulate and supply the power used to ‘drive’ runs of LED strip lights. Similar to traditional transformers, they convert mains voltage (240v AC) into a lower value (usually 12 or 24v).” *What Is an LED Driver & Which Driver Do I Need?*, ULTRA LEDs, <https://www.ultraleds.co.uk/what-is-led-driver-what-driver-do-i-need> (last visited July 29, 2023).

34. “Generally speaking, the driver circuit plays a significant role in dominating the energy efficiency, which means the system efficiency can be further improved via an appropriate driver circuit. Traditional LED systems are based on single-stage or two-stage LED drivers.” Yijie Wang, et al., *A Review of LED Drivers and Related Technologies*, 64 IEEE TRANSACTIONS ON INDUS. ELECTRONICS 5754, 5754 (July 2017).

35. A single-stage LED driver is a DC/DC converter with constant output current that can obtain power factor (PF) correction (PFC), while a two-stage system consists of a PFC circuit and a DC/DC converter as shown below. *Id.*



Id. at 5756 fig. 3.

36. “[D]ue to the unique characteristics of LEDs, a current loop is always included in the [DC/DC stage] . . . to acquire constant current control. Moreover, in practical applications when several strings of LEDs are adopted, a current balance stage may also be required. The advantage of the above two LED drivers is that they are easy to design with more accurate control. However, one of the drawbacks of single stage converters is the high value of the storage capacitor, which also increases the volume of the driver. As for the two-stage system, more devices are needed, which means the cost is quite high and reliability is relatively low.” *Id.* at 5754-55.

37. “In recent years, many integrated-stage topologies are designed for the sake of efficiency and cost.” *Id.* at 5755. “In order to obtain high PF and low total harmonic distortion (THD), a topology which performs PFC characteristics as PFC

stage is usually chosen, and a [DC/DC] stage is selected according to the power level of the system.” *Id.* Due to the integration technology, the PFC stage and DC/DC stage can be simplified into one stage by sharing active power switches and control circuit. Therefore, cost and size of the system is reduced while ensuring high efficiency, high reliability, and fast output dynamics. *Id.*

B. Overview of the ‘713 Patent

38. The ‘713 Patent describes a system, method, and apparatus for monitoring and limiting power supplied to a solid state lighting (SSL) device when an operational fault condition is sensed such as when the power level being supplied to the device is sensed to be meeting or higher than an expected or predetermined level. Ex. 1001, Abstract. The ‘713 Patent purports to address the need to “limit power within predetermined limits to [LED] devices to mitigate or reduce over-temperature or abnormal operation of these SSL devices.” Ex. 1001, 1:18-20.

39. The ‘713 Patent further notes that, in terms of fault conditions, “OLEDs may have failure mechanisms that include an increase in impedance. In this failure mode, the increased impedance results in increased power dissipation for a fixed LED drive current, which may, however, increase the risk of the SSL device being a fire hazard.” Ex. 1001, 1:24-29.

40. Approaches exist to limit power and current to an LED load as a result of an external failure of the LED load or an internal failure of a component within

an LED power source. One common approach is to disable or turn off the LED power source if an over power or over current condition is detected. Another approach is to implement a “hiccup” mode whereby the output of the LED power source is continually cycled on and off in an over power or over current condition. However, it is not always ideal to immediately disconnect power to a LED load under transient conditions caused by a potential fault, an AC mains transient, a load transient or a temporary overload condition. Ex. 1001, 1:46-59

C. The Alleged Invention

41. The claims of the ‘713 Patent are generally directed to a “system, method, and apparatus for monitoring and limiting power supplied to a solid state lighting (SSL) device when an operational fault condition is sensed such as when the power level being supplied to the device is sensed to be meeting or higher than an expected or predetermined level.” Ex. 1001, Abstract. The LED device of the ‘759 Patent further includes a power circuit; “at least one power limit connected to the power circuit; at least one output current driver for supplying a load power to the SSL device load, the at least one output current driver connected to the at least one power limit; and a power limit controller.” Ex. 1001, 12:23-28. “The power circuit transmits the power to the at least one power limit which, in turn, transmits a current to the at least one output current driver.” Ex. 1001, 12:29-31. Further, “the power limit controller directly or indirectly monitors a level of the load power and controls

the at least one power limit to reduce the level of the load power for a predetermined period of time when the load power exceeds a predetermined power limit.” Ex. 1001, 12:32-36. “If the load power exceeds the predetermined power limit, the power limit controller internally generates and transmits a signal to the current source controller to control the load power to the load where the signal is based on internal controls.” Ex. 1001, 12:37-41

D. Summary of Prosecution History

42. The application that issued as the ‘713 Patent (US14/893,375) was filed on June 25, 2014, and claims the benefit of priority of U.S. Provisional Patent Application No. 61/838,965 filed June 25, 2013.

43. In a first Office Action, several claims were rejected as being anticipated by or obvious in view of (1) Tikkanen et al. (US 2011/0204820, now U.S. Patent No. 8,525,713); and (2) Tikkanen et al. (US 2011/0204820, now U.S. Patent No. 8,525,713) in view of Xie et al. (U.S. Patent No. 9,024,541). Ex. 1004, at 27.

44. In response, the applicant amended claim 1 to add the additional limitations of wherein if the load power exceeds the predetermined power limit, the power limit controller internally generates and transmits a signal to the current source controller to control the load power to the load and wherein the signal is based on internal controls. Ex. 1004, at 36.

45. In a second Office Action, several claims were rejected as being anticipated by Burlak et al. (U.S. Patent No. 7,671,571). Ex. 1004, at 50. The Examiner noted that certain claims contained allowable subject matter. Ex. 1004, at 62. In response, the applicant cancelled the claim subject to the 102(a) rejection and requested allowance of the claims that contained allowable subject matter. Ex. 1004, at 75.

E. Overview of the Prior Art

46. The challenged claims are anticipated by or are obvious over the following prior art.

47. U.S. Patent No. 9,173,273 (“Zudrell-Koch”) was filed on January 23, 2013, and published on February 27, 2014. Zudrell-Koch issued on October 27, 2015. Zudrell-Koch is prior art to the ‘713 Patent under 35 U.S.C. § 102(a). Zudrell-Koch teaches a driver circuit for controlling the dimming of SSL devices.

48. The driver circuit comprises a transistor operable in two modes, either alternating between on/off states or continuously controlling a current through the transistor. A power converter network provides a switched-mode power converter in conjunction with the transistor when operated in the first mode generating a drive voltage for the SSL. The control unit controls the transistor to selectively operate in one of the two modes: to control the transistor to determine that the input voltage exceeds an input voltage threshold; and to control a drive current through the SSL

based on a measurement of a phase-cut angle thereby controlling an illumination level of the SSL device. Ex. 1005, Abstract.

49. U.S. Patent Application Publication No. US2014/0103804 (“Zhdanau”). Zhdanau was filed on March 15, 2013, and claims priority to provisional patent application no. 61/612,741, filed March 19, 2012. Zhdanau was published on April 17, 2014, and is prior art to the ‘713 Patent under 35 U.S.C. § 102(b). Zhdanau teaches an improved LED lighting system and method which limits current and employs a voltage significantly greater than line voltage in order to allow lighting circuits to be built with up to thousands of Watts fed from a single power/data source. The present system and method allows exceptionally long lengths of LED lighting of 200 meters or more for large scale LED lighting applications such as the architectural delineation of skyscrapers and bridges. Ex. 1006, Abstract.

50. U.S. Patent Application Publication No. US2013/0063047 (“Veskovic”). Veskovic was filed on March 9, 2012, and was published on March 14, 2013. Veskovic is prior art to the ‘713 Patent under 35 U.S.C. § 102(b). Veskovic teaches: [a]n LED driver for controlling the intensity of an LED light source includes a power converter circuit for generating a DC bus voltage, an LED drive circuit for receiving the bus voltage and controlling a load current through, and thus the intensity of, the LED light source and a controller operatively coupled to the power

converter circuit and the LED drive circuit. The LED drive circuit comprises a controllable-impedance circuit adapted to be coupled in series with the LED light source. The controller adjusts the magnitude of the bus voltage to a target bus voltage and generates a drive signal for controlling the controllable-impedance circuit. To adjust the intensity of the LED light source, the controller controls both the magnitude of the load current and the magnitude of the regulator voltage. The controller controls the magnitude of the regulator voltage by simultaneously maintaining the magnitude of the drive signal constant and adjusting the target bus voltage. Ex. 1007, Abstract

V. SUMMARY OF MY OPINIONS

51. Having reviewed the '713 Patent and the prior art discussed herein, I have formed the following opinions:

- U.S. Patent No. 9,173,273 to Zudrell-Koch ("Zudrell-Koch") discloses all limitations of claims 1-2, 5, 10 and 13 and these claims are anticipated by Shteynberg.
- The combination of Zudrell-Koch and U.S. Patent Application Publication No. US2014/0103804 to ("Zhdanau") discloses all limitations of claims 12 and 13 and these claims are rendered obvious by this combination.
- The combination of Zudrell-Koch and U.S. Patent Application Publication No. US2013/0063047 to ("Veskoic") discloses all limitations of claims 12 and 13 and these claims are rendered obvious by this combination.
- In support, I have attached a chart to this declaration establishing that the prior art teaches the limitations of each claim. Ex. A.

A. Opinions

1. Ground 1: Zudrell-Koch anticipates Claims 1-2, 5, 10, and 13

52. Independent claim 1 and dependent claims 2, 5, 10, and 13 of the ‘713 Patent are anticipated by Zudrell-Koch under 35 U.S.C. § 102. In reaching this conclusion, I provide the opinions as one of ordinary skill in the art below.

53. An LED driver changes the power supply to a specific voltage current to drive the LED voltage converter. In general, the input of the LED driver includes the high voltage power frequency AC (i.e., the city electricity), the low voltage DC, the high voltage DC, the low voltage and high frequency AC (such as the output of the electronic transformer). The output of LED driver power is mostly a constant current source that can change voltage with the change of LED forward voltage drop. The core components of the LED power supply include switch controller, inductor, switch component (MOSFET), feedback resistor, input filter device, output filter, and so on. According to the requirements of different occasions, there must be input over-voltage protection circuit, input under-voltage protection circuit, LED open circuit protection, over-current protection circuit and so on. *LED Driver Basics and Its Circuit Design*, APOGEEWEB (Apr. 9, 2018), at 2, https://www.power.com/sites/default/files/forum/files/LED%20Driver%20Circuits%20Design_0.pdf.

54. Solid-state lighting (SSL) is a type of lighting that uses semiconductor light-emitting diodes (LEDs), organic light-emitting diodes (OLEDs), or polymer

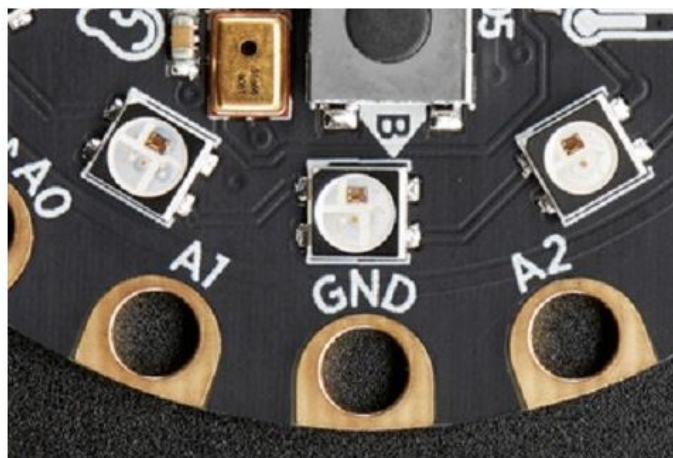
light-emitting diodes (PLEDs) as light sources instead of filaments, plasma (used in arc lamps such as fluorescent lamps), or gas. SSL uses solid-state electroluminescence as opposed to incandescent bulbs (which use heat radiation) and fluorescent tubes. Compared to incandescent lighting, SSL produces visible light that generates less heat and dissipates less energy. *Solid State Lighting*, ACAD. ACCELERATOR, <https://academic-accelerator.com/encyclopedia/solid-state-lighting> (last visited Aug. 2, 2023); see also Arpad Bergh et al., *The Promise and Challenge of Solid-State Lighting*, 54 PHYSICS TODAY 12, 42-47 (2001), available at <https://pubs.aip.org/physicstoday/article/54/12/42/411668/The-Promise-and-Challenge-of-Solid-State>.

55. A power circuit generally is any circuit used to carry electricity that operates a load. *Everything About Power Distribution Board Manufacturing*, DAS & Co. (Feb. 22, 2022), available at <https://www.dasnko.net/blog/post/1670466/electrical-power-distribution-panel-board-in-kolkata#:~:text=A%20power%20circuit%20is%20any,electricity%20that%20operates%20a%20load>.

56. Similarly, a power converter processes and controls the flow of electrical energy by supplying voltages and currents in a form that is optimally suited for user loads, in this case to provide variable brightness levels for solid-state lighting. R. Petrocelli, *One-Quadrant Switched-Mode Power Converters*, CAS-CERN ACCELERATOR SCH. (2015), available at <http://cds.cern.ch/record/2038620>;

Roger Bailey, *Proceedings of the CAS–CERN Accelerator School: RF for Accelerators*, CAS–CERN ACCELERATOR SCH. (2012), at 15, available at <https://cdsweb.cern.ch/record/1231364>.

57. IC power-supply pins denote voltage and current supply terminals in electric, electronics engineering, and in integrated circuit design. Digital input is where a pin will detect the presence of a voltage level that is either “high” or “low.” Whether a pin input level is high or low depends on where the microcontroller on the Adafruit Circuit Playground Express has set the voltage threshold for each. This is somewhere near the supply voltage for high (the voltage at the 3.3V pin) and near ground voltage for low (the voltage at GND pin, or 0V). Also, when a digital input is used for reading data, the input level is interpreted as a binary value of 1 for high and 0 for low. Multiple digital inputs are often combined in digital electronics to read larger values of binary numbers.



Digital Input, MAKECODE, <https://makecode.adafruit.com/learnsystem/pins-tutorial/digital-input> (last visited on August 2, 2023).

a. Claim 1

58. As discussed above, a POSITA would understand that the input voltage pin is the power limiter that receives power from the power circuit. A POSITA would also understand that the “appropriate drive current” is then transmitted to the output current driver. As such, Zudrell-Koch discloses that the power circuit transmits power to the at least one power limit which transmits current to the output current driver as required by claim 1 of the ‘713 Patent.

59. A POSITA would understand that current sensing means configured to determine a feedback signal which indicates the level of the current. Further, the control unit uses an input voltage pin to monitor the voltage level which controls the load power to the load. As such, Zudrell-Koch discloses wherein if the load power exceeds the predetermined power limit, the power limit controller internally generates and transmits a signal to the current source controller to control the load power to the load as required by claim 1 of the ‘713 Patent.

60. Feedback is a term that describes comparing the actual output of a system to the desired output and adjusting the actual output to produce the desired end result. In electronics, feedback is defined as the process of returning part of the signal output from a circuit or device back to the input of that circuit or device.

Feedback systems are widely used in amplifier circuits, oscillators, process control systems, and in many other areas. Janet Heath, *What is Feedback?*, ANALOG IC TIPS (Sept. 19, 2016), <https://www.analogictips.com/faq-what-is-feedback/#:~:text=In%20electronics%2C%20feedback%20is%20defined,and%20in%20many%20other%20areas> (last visited August 2, 2023).

b. Claim 5

61. In electrical engineering, current sensing is any one of several techniques used to measure electric current. The measurement of current ranges from picoamps to tens of thousands of amperes. The selection of a current sensing method depends on requirements such as magnitude, accuracy, bandwidth, robustness, cost, isolation or size. The current value may be directly displayed by an instrument, or converted to digital form for use by a monitoring or control system. Current sense resistors, or shunt resistors, are devices used to gauge the flow of current. They detect and convert current to a measured output voltage. Current sense resistors are generally low-value, high-power resistors. They are designed for low resistance to minimize power consumption and to eliminate the risk of short circuits which are likely to damage other components. Stephen Oxley, *Using Current Sense Resistors to Improve Efficiency*, TT ELECTRONICS, <https://blog.ttelectronics.com/current-sense-resistors#:~:text=Current%20sense%20resistors%2C%20or%20shunt,value%2C%20high%2Dpower%20resistors> (last visited August 2, 2023).

62. A POSITA would understand Zudrell-Koch's disclosure that the control unit is configured to control the level of current and it is equivalent to the current source controller found in claim 5 of the '713 Patent.

2. Ground 2: Zudrell-Koch in view of Zhdanau or Veskoic renders Claims 12 and 13 obvious

63. Claims 12 and 13 of the '713 Patent are rendered obvious under 35 U.S.C. § 103 by Zudrell-Koch in view of Zhdanau or Veskoic. Zudrell-Koch anticipates independent claim 1 for the reasons discussed above.

a. Claim 12

64. Constant current reduction (CCR) or analog dimming control the light output of the LEDs by adjusting the current flowing continuously to the LEDs. Dimmable LED Drivers, OPEN LIGHTING PRODUCT DISCOVERY, [https://www.shine.lighting/products/dimmable-led-drivers/#:~:text=Constant%20current%20reduction%20\(CCR\)%20or,current%20flowing%20through%20the%20LED](https://www.shine.lighting/products/dimmable-led-drivers/#:~:text=Constant%20current%20reduction%20(CCR)%20or,current%20flowing%20through%20the%20LED) (last visited August 2, 2023).

VI. MOTIVATION TO COMBINE ZUDRELL-KOCH AND ZHDANAU OR VESKOVIC

65. A POSITA would have been motivated to combine Zudrell-Koch and Zhdanau or Veskovic for several reasons.

66. First, Zudrell-Koch and Zhdanau or Veskovic are analogous art to the '713 Patent because they each reference is in the same field of endeavor—namely,

LED drivers. The ‘713 Patent defines its “Technical Field” as a “a novel apparatus and method for monitoring and limiting power to SSL devices.” Ex. 1001, 1:59-60. Like the ‘713 Patent, Zudrell-Koch, Zhdanau, and Veskovice are directed to powering and controlling SSL applications. Ex. 1005, 1:18; Ex. 1006, Abstract; Ex. 1001 Abstract. Specifically, Zudrell-Koch defines its “Technical Field” as “a method and system for controlling the degree of dimming of solid state lighting devices such as LED or OLED assemblies.” Ex. 1005, 1:6-8. Similarly, Zhdanau describes its Field as “[t]his present disclosure relates generally to a power distribution system and method for light emitting diode (LED) lighting. Ex. 1006, 1[0001]. Still further, Veskovice provides that its Field of the Invention is “[t]he present invention relates to a load control device for a light-emitting diode (LED) light source, and more particularly, to an LED driver for controlling the intensity of an LED light source.” Ex. 1007, 1[0003].

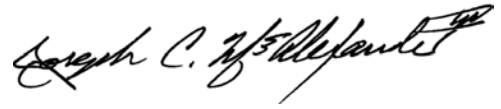
67. Moreover, Zudrell-Koch and Zhdanau or Veskovice are analogous to the ‘713 Patent because they are reasonably pertinent to the technical problem allegedly addressed by the claimed invention. For example, the ‘713 Patent describes that the existing approaches of limiting power and current to an LED load as a result of an external failure of the LED load or an internal failure of a component within an LED power source are insufficient. 1005, 1:45-47. Similarly, Veskovice discloses that its load control device is operable to adjust the maximum controllable-impedance

voltage threshold in response to the load current feedback signal, such that the power dissipated in the regulation transistor is limited to a predetermined constant maximum power. Ex. 1007, 1[0011], [Claim 18].

68. Finally, a POSITA would have had a reasonable expectation of success in making this modification. The LED Driver components described in Zudrell-Koch and Zhdanau or Veskovic were well-known at the time. Indeed, Veskovic notes that the prior dealing with LED driver is extensive. Ex. 1007, 1[0006]. As such, it would also have been straightforward for a POSITA to modify the LED driver of Zudrell-Koch and Zhdanau or Veskovic to include constant current reduction technique and LED loads and that such a system would work.

69. Therefore, a POSITA would be motivated to combine Zudrell-Koch and Zhdanau; or Zudrell-Koch and Veskovic.

I declare under penalty of perjury that the foregoing is true and accurate.

A handwritten signature in black ink, reading "Joseph C. McAlexander III". The signature is written in a cursive style with a large, stylized "J" and "M".

Joseph C. McAlexander III

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Claims	Prior Art References		
U.S. Patent No 9,591,713	U.S. Patent No 9,173,273 to Zudrell-Koch	U.S. Patent Application No US2014/0103804 to Zhdanau	U.S. Patent Application No US2013/0063047 to Veskovic
1[p] Apparatus for controlling power to a solid state lighting (SSL) device load comprising:	“A control unit for a driver circuit which is configured to drive a solid state lightening, referred to as SSL device, subject to an input voltage derived from a mains voltage using a phase-cut dimmer, wherein the driver circuit comprises a transistor operable in a first mode and in a second mode; and a power converter network[.]” Zudrell-Koch, 18:25-30. “A first step 500 depicts a provision of a control unit, a driver circuit comprising a single power Switch, and a SSL device, wherein the driver circuit is setting an illumination level of the SSL device in accordance to a setting of the phase-cut dimmer. The next		

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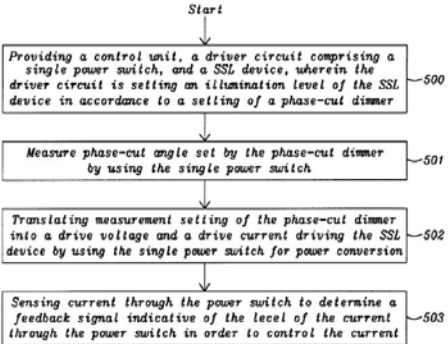
Claims	Prior Art References		
U.S. Patent No 9,591,713	U.S. Patent No 9,173,273 to Zudrell-Koch	U.S. Patent Application No US2014/0103804 to Zhdanau	U.S. Patent Application No US2013/0063047 to Veskovic
	step 501 shows measuring a phase-cut-angle set by the phase-cut dimmer by using the single power switch.” Zudrell-Koch, 17:50-56.  <pre> graph TD Start([Start]) --> 500[Providing a control unit, a driver circuit comprising a single power switch, and a SSL device, wherein the driver circuit is setting an illumination level of the SSL device in accordance to a setting of a phase-cut dimmer] 500 --> 501[Measure phase-cut angle set by the phase-cut dimmer by using the single power switch] 501 --> 502[Translating measurement setting of the phase-cut dimmer into a drive voltage and a drive current driving the SSL device by using the single power switch for power conversion] 502 --> 503[Sensing current through the power switch to determine a feedback signal indicative of the level of the current through the power switch in order to control the current] </pre> FIG. 5 Zudrell-Koch, fig. 5.		
1(a): a power circuit for receiving power from an external source	“In order to control of dimming of solid state lighting devices (SSL) a driver circuit drives the SSL subject to an input voltage using a phase-cut dimmer. The driver circuit comprises a		

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	transistor operable in two modes, either alternating between on/off states or continuously controlling a current through the transistor. A power converter network provides a switched-mode power converter in conjunction with the transistor when operated in the first mode generating a drive voltage for the SSL.” Zudrell-Koch, Abstract. “The driver circuit may comprise a current source and the control unit may be configured to control the current source to provide the appropriate drive current for the determined illumination level.” Zudrell-Koch, 5:26-28.		

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Claims	Prior Art References		
U.S. Patent No 9,591,713	U.S. Patent No 9,173,273 to Zudrell-Koch	U.S. Patent Application No US2014/0103804 to Zhdanau	U.S. Patent Application No US2013/0063047 to Veskovic
1(b): at least one power limit connected to the power circuit;	“The control unit may be configured to determine that the input Voltage exceeds a pre-determined input Voltage threshold (i.e. that the phase-cut dimmer goes into its on-state) by monitoring the input Voltage (or a Voltage derived from the input Voltage, or a Voltage derived from the mains Voltage). For this purpose, the control unit may comprise an input Voltage pin. The input Voltage pin may be linked to input Voltage measurement means of the driver circuit. The input Voltage measurement means may e.g. be a Voltage divider configured to provide a Voltage derived from the input Voltage to the input Voltage pin of the control unit. The input		

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Claims	Prior Art References		
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	Voltage measurement means may be coupled to a rectifier unit of the driver circuit, on one side, and to the input Voltage pin of the control unit on the other side. As such, the control unit may be configured to receive a Voltage derived from the input Voltage. Furthermore, the control unit may be configured to determine that the input voltage exceeds a pre-determined input voltage threshold by determining that the received voltage exceeds a respective pre-determined threshold.” Zudrell-Koch, 4:60-5:11.		
1(c): at least one output current driver for supplying a load power to the	“The driver circuit may comprise a current source and the control unit may be configured to control the		

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Claims	Prior Art References		
U.S. Patent No 9,591,713	U.S. Patent No 9,173,273 to Zudrell-Koch	U.S. Patent Application No US2014/0103804 to Zhdanau	U.S. Patent Application No US2013/0063047 to Veskovic
SSL device load, the at least one output current driver connected to the at least one power limit; and	current source to provide the appropriate drive current for the determined illumination level.” Zudrell-Koch, 5:26-28. “By controlling the current through the Switch, the control unit may provide overstress protection of the components of the driver circuit and/or of the control unit (by limiting the current through the Switch to a value below a maximum current).” Zudrell-Koch, 4:47-50. “The estimated angle 113 indicates a desired dim level and is passed to an LED control unit 103 which controls the LED power supply 101 via a control signal 114 to provide an output power 115 to the LED 104 (referred to as light source		

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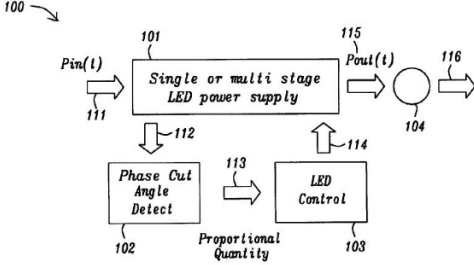
Claims	Prior Art References		
U.S. Patent No 9,591,713	U.S. Patent No 9,173,273 to Zudrell-Koch	U.S. Patent Application No US2014/0103804 to Zhdanau	U.S. Patent Application No US2013/0063047 to Veskovice
	6 in FIG. 1) which drives the LED 104 to provide light 116 at the desired dim level.” Zudrell-Koch, 9:58-63.  <i>FIG. 2a</i> Zudrell-Koch, fig. 2a.		
1(d): a power limit controller;	“The example power supply arrangement 100 comprises a phase-cut angle detection unit 102 which senses the input voltage 112 and which estimates the angle at which the original sinusoidal mains		

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Claims	Prior Art References		
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	voltage has been cut by the dimmer. The estimated angle 113 indicates a desired dim level and is passed to an LED control unit 103 which controls the LED power supply 101 via a control signal 114 to provide an output power 115 to the LED 104 (referred to as light source 6 in FIG. 1) which drives the LED 104 to provide light 116 at the desired dim level.” Zudrell-Koch, 9:53-63. “The control unit may be configured to determine that the input Voltage exceeds a pre-determined input Voltage threshold (i.e. that the phase-cut dimmer goes into its on-state) by monitoring the input Voltage (or a Voltage derived from the input Voltage, or a Voltage		

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Claims	Prior Art References		
U.S. Patent No 9,591,713	U.S. Patent No 9,173,273 to Zudrell-Koch	U.S. Patent Application No US2014/0103804 to Zhdanau	U.S. Patent Application No US2013/0063047 to Veskovic
	derived from the mains Voltage). For this purpose, the control unit may comprise an input Voltage pin. The input Voltage pin may be linked to input Voltage measurement means of the driver circuit. The input Voltage measurement means may e.g. be a Voltage divider configured to provide a Voltage derived from the input Voltage to the input Voltage pin of the control unit. The input Voltage measurement means may be coupled to a rectifier unit of the driver circuit, on one side, and to the input Voltage pin of the control unit on the other side. As such, the control unit may be configured to receive a Voltage derived from the input Voltage. Furthermore,		

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U.S. Patent No 9,591,713	U.S. Patent No 9,173,273 to Zudrell-Koch	U.S. Patent Application No US2014/0103804 to Zhdanau	U.S. Patent Application No US2013/0063047 to Veskovich
	the control unit may be configured to determine that the input voltage exceeds a pre-determined input voltage threshold by determining that the received voltage exceeds a respective pre-determined threshold.” Zudrell-Koch, 4:60-5:11.		
1(e) wherein the power circuit transmits the power to the at least one power limit which, in turn, transmits a current to the at least one output current driver;	“The driver circuit may comprise a current source and the control unit may be configured to control the current source to provide the appropriate drive current for the determined illumination level.. Zudrell-Koch 5:25-28. “The control unit may be configured to determine that the input Voltage exceeds are-determined input Voltage threshold (i.e. that the phase-cut		

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	dimmer goes into its on-state) by monitoring the input Voltage (or a Voltage derived from the input Voltage, or a Voltage derived from the mains Voltage). For this purpose, the control unit may comprise an input Voltage pin. The input Voltage pin may be linked to input Voltage measurement means of the driver circuit. The input Voltage measurement means may e.g. be a Voltage divider configured to provide a Voltage derived from the input Voltage to the input Voltage pin of the control unit. The input Voltage measurement means may be coupled to a rectifier unit of the driver circuit, on one side, and to the input Voltage pin of the control unit on the		

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	other side. As such, the control unit may be configured to receive a Voltage derived from the input Voltage. Furthermore, the control unit may be configured to determine that the input voltage exceeds a pre-determined input voltage threshold by determining that the received voltage exceeds a respective pre-determined threshold.” Zudrell-Koch, 4:60-5:11.		
1(f): wherein the power limit controller directly or indirectly monitors a level of the load power and controls the at least one power limit to reduce the level of	“The control unit may be configured to determine that the input voltage exceeds a pre-determined input voltage threshold (i.e. that the phase-cut dimmer goes into its on-state) by monitoring the input voltage (or a voltage derived from the input voltage, or a voltage		

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Claims	Prior Art References		
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the load power for a predetermined period of time when the load power exceeds a predetermined power limit;	derived from the mains voltage).” Zudrell-Koch, 4:60-64. “The input voltage measurement means may e.g. be a voltage divider configured to provide a voltage derived from the input voltage to the input voltage pin of the control unit. The input voltage measurement means may be coupled to a rectifier unit of the driver circuit, on one side, and to the input voltage pin of the control unit on the other side. As such, the control unit may be configured to receive a voltage derived from the input voltage.” Zudrell-Koch, 5:1-7. “The control unit may be configured to determine an indicator of a phase-cut angle		

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	set by the dimmer based on the time interval between the first and second time instants. In particular, the control unit may be configured to determine the illumination level corresponding to the phase-cut angle (or corresponding to the time interval).” Zudrell-Koch, 5:12-17).		
1(g): wherein if the load power exceeds the predetermined power limit, the power limit controller internally generates and transmits a signal to the current source controller to control	“The driver circuit may further comprise current sensing means configured to determine a feedback signal indicative of the level of the current through the switch.” Zudrell-Koch, 4:35-37. “The feedback signal may correspond to the voltage drop across the sensing resistor, wherein the voltage drop across the sensing resistor is typically		

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Claims	Prior Art References		
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the load power to the load;	proportional to the current through the switch. The control unit may comprise a pin for receiving the feedback signal. Furthermore, the control unit may be configured to control the level of the current through the switch, when in the second mode, based on the feedback signal.” Zudrell-Koch, 4:39-44. “The control unit may be configured to determine that the input voltage exceeds a pre-determined input voltage threshold (i.e. that the phase-cut dimmer goes into its on-state) by monitoring the input voltage (or a voltage derived from the input voltage, or a voltage derived from the mains voltage). For this purpose, the control unit may comprise an		

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	input voltage pin.” Zudrell-Koch, 4:60-66.		
1(h) wherein the signal is based on internal controls.	“[The feedback signal may correspond to the voltage drop across the sensing resistor, wherein the voltage drop across the sensing resistor is typically proportional to the current through the switch.” Zudrell-Koch, 4:39-43. “The control unit may comprise a pin for receiving the feedback signal. Furthermore, the control unit may be configured to control the level of the current through the switch, when in the second mode, based on the feedback signal. By controlling the current through the switch, the control unit may provide overstress protection of the components of the driver circuit		

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	and/or of the control unit (by limiting the current through the switch to a value below a maximum current). Furthermore, the control unit may ensure that the components of the driver circuit are discharged within a pre-determined discharging time interval (by ensuring that the current through the switch exceeds a minimum current). In particular, it may be ensured that the components of the driver circuit are discharged prior to the second time instant (when the phase-cut dimmer goes into its on-state). As a result, the re-increase of the input voltage (due to the dimmer going into its on-state) can be reliably detected by the		

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	control unit.” Zudrell-Koch, 4:35-59.		
Claim 2: The apparatus of claim 1 wherein the at least one power limit is integrated within one of the at least one output current drivers.	“The control unit may be configured to determine that the input Voltage exceeds a pre-determined input Voltage threshold (i.e. that the phase-cut dimmer goes into its on-state) by monitoring the input Voltage (or a Voltage derived from the input Voltage, or a Voltage derived from the mains Voltage). For this purpose, the control unit may comprise an input Voltage pin.” Zudrell-Koch, 4:60-66.		
Claim 5: The apparatus of claim 1 wherein the at least one output current driver comprises: an output current	“The driver circuit may further comprise current sensing means configured to determine a feedback signal indicative of the level of the current through the switch. By way of example,		

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Source; a current sense; and a current source controller.	the current sensing means may comprise a sensing resistor which is arranged in series with the switch. The feedback signal may correspond to the voltage drop across the sensing resistor, wherein the voltage drop across the sensing resistor is typically proportional to the current through the switch.” Zudrell-Koch, 4:35-39. “The driver circuit may comprise a current source and the control unit may be configured to control the current source to provide the appropriate drive current for the determined illumination level.” Zudrell-Koch, 5:25-28. “The control unit may comprise a pin for receiving the feedback signal. Furthermore, the control		

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	unit may be configured to control the level of the current through the switch, when in the second mode, based on the feedback signal.” Zudrell-Koch, 4:43-46.		
Claim 10: The apparatus of claim 1 wherein the at least one output current driver reduces the load power by a pulsing technique.	“FIG. 3c illustrates block diagrams of example control units 320, 380 for a driver circuit 300. The control unit 320 of FIG. 3c corresponds to the control unit 320 shown in FIG. 3b. Furthermore, the control unit 320 of FIG. 3c comprises a switch 372 configured to provide the pulse width modulated control signal to the switch 304, for operating the switch 304 in an on/off mode.” Zudrell-Koch, 16:1-7.		
Claim 12: The apparatus of claim 1		“The gauge or cross-section area of the conducting wires	“The controller 140 is operable to control the

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Claims	Prior Art References		
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wherein the at least one output current driver reduces load power by a constant current reduction technique.		used to connect LED luminaires 260A . . . 260N may be selected much less [sic] than for conventional AC LED lighting system 100 (FIG. 1) due to the limited current, and output voltage from PFC 230 being significantly higher than AC line voltage used in conventional AC LED lighting system 100.” Zhdanau, 2[0032].	LED drive circuit 130, so as to control the amount of power delivered to the LED light source 102 using the two different modes of operation (i.e., the current load control mode and the voltage load control mode). During the current load control mode, the LED drive circuit 130 regulates the peak magnitude IPK of the load current ILOAD through the LED light source 102 to control the average magnitude IAVE to a target load current ITRGT in response to the load current feedback signal VILOAD (i.e.,

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			using closed loop control). The target load current ITRGT may be stored in the memory 170 and may be programmed to be any specific magnitude depending upon the LED light source 102.” Veskovic, 4[0043].
Claim 13: The apparatus of claim 1 wherein the SSL device load is one of an organic light emitting diode (OLED) load, a light emitting diode (LED) load or a LED array load.	“A further object of the disclosure is to achieve a control unit for a driver circuit which is configured to drive a SSL device, e.g. an LED or an OLED.” Zudrell-Koch, 1:50-52.	“There is disclosed an improved LED lighting system and method which limits current and employs a voltage significantly greater than line voltage in order to allow lighting circuits to be built with up to thousands of Watts fed from a sing power/data source. The present system and method allows exceptionally long	“An LED driver for controlling the intensity of an LED light source includes a power converter circuit for generating a DC bus voltage, an LED drive circuit for receiving the bus voltage and controlling a load current through, and thus the intensity of, the LED

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		lengths of LED lighting of 200 meters or more for large scale LED lighting applications such as the architectural delineation of skyscrapers and bridges. Zhdanau, Abstract.	light source, and a controller operatively coupled to the power converter circuit and the LED drive circuit.” Veskovic, Abstract.