

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**REQUEST FOR WITHDRAWAL
AS ATTORNEY OR AGENT AND
CHANGE OF
CORRESPONDENCE ADDRESS**

Application Number	14/597,788, Patent No. 9,078,310
Filing Date	January 15, 2015
First Named Inventor	David Tikkanen
Art Unit	2844
Examiner Name	Jason Crawford
Practitioner Docket Number	6008.014

To: **Commissioner for Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

Please withdraw me as attorney or agent for the above-identified patent application, and

- ☐ all the practitioners of record;
- ☐ the practitioners (with registration numbers) of record listed on the attached paper(s); or
- ☒ the practitioners of record associated with Customer Number: 30589

NOTE: The immediately preceding box should only be marked when the practitioners were appointed using the listed Customer Number.

The reason(s) for this request are those described in 37 CFR:

- | | | |
|---|---------------------------------------|--|
| ☐ 11.116(a)(1) | ☐ 11.116(a)(2) | ☒ 11.116(a)(3) |
| ☒ 11.116(b)(1) | ☐ 11.116(b)(2) | ☐ 11.116(b)(3) |
| ☐ 11.116(b)(4) | ☐ 11.116(b)(5) | ☐ 11.116(b)(6) |
| ☐ 11.116(b)(7) Please explain below: | | |

Certifications

Check each box below that is factually correct. **WARNING: If a box is left unchecked, the request will likely not be approved.**

- ☒ I/We have given reasonable notice to the client, prior to the expiration of the response period, that the practitioner(s) intend to withdraw from employment.
- ☒ I/We have delivered to the client or a duly authorized representative of the client all papers and property (including funds) to which the client is entitled.
- ☒ I/We have notified the client of any responses that may be due and the time frame within which the client must respond.

Please provide an explanation, if necessary:

[Page 1 of 2]

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

if you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Complete the following section only when the correspondence address will change. *Changes of address will only be accepted to an applicant.*

Change the correspondence address and direct all future correspondence to:

A. ☐ The address of the applicant associated with Customer Number: _____

OR

B. ☒ Applicant

Address 219 W. Wilshire Blvd., Suite 104D

City **Oklahoma City**

State **OK**

Zip **73116**

Country **US**

Telephone **405-520-9220**

Email **Jenn@onyxtheater.com**

I am authorized to sign on behalf of myself and all withdrawing practitioners.

Signature **/Ann M. Robl/**

Name **Ann M. Robl**

Registration No. **71541**

Address **609 W. Sheridan**

City **Oklahoma City**

State **OK**

Zip **73102**

Country **US**

Date **April 28, 2021**

Telephone No. **405-607-8600**

NOTE: Withdrawal is effective when approved rather than when received.

[Page 2 of 2]

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	42581950
Application Number:	14597788
International Application Number:	
Confirmation Number:	9654
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	30589
Filer:	Ann M. Robl/Bradley Thompson
Filer Authorized By:	Ann M. Robl
Attorney Docket Number:	6008.014
Receipt Date:	28-APR-2021
Filing Date:	15-JAN-2015
Time Stamp:	16:43:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	6008014_SB21Transmittal_04282021.pdf	205306	no	2
			538df15362801d9f72412ab79dddefb9b24bb08b		

Warnings:

Information:					
2	Petition to withdraw attorney or agent (SB83)	6008014_AIA83Withdrawal_04282021.pdf	178000	no	3
			672d6c5026568478740cf07ec30f5bd115b38a43		
Warnings:					
Information:					
Total Files Size (in bytes):			383306		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	14/597,788, Patent No. 9,078,310
Filing Date	January 15, 2015
First Named Inventor	David Tikkanen
Art Unit	2884
Examiner Name	Jason Crawford
Attorney Docket Number	6008.014

ENCLOSURES (Check all that apply)

☐ Fee Transmittal Form	☐ Drawing(s)	☐ After Allowance Communication to TC
☐ Fee Attached	☐ Licensing-related Papers	☐ Appeal Communication to Board of Appeals and Interferences
☐ Amendment/Reply	☐ Petition	☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
☐ After Final	☐ Petition to Convert to a Provisional Application	☐ Proprietary Information
☐ Affidavits/declaration(s)	☒ Power of Attorney, Revocation Change of Correspondence Address	☐ Status Letter
☐ Extension of Time Request	☐ Terminal Disclaimer	☐ Other Enclosure(s) (please identify below):
☐ Express Abandonment Request	☐ Request for Refund	
☐ Information Disclosure Statement	☐ CD, Number of CD(s) _____	
	☐ Landscape Table on CD	
☐ Certified Copy of Priority Document(s)	Remarks	
☐ Reply to Missing Parts/Incomplete Application	Electronically Transmitted:	
☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	1) sb21 Transmittal (1 page); and, 2) aia83 Request for Withdrawal as Attorney or Agent and Change of Correspondence Address (2 pages)	

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Dunlap Coddington, P.C.		
Signature	/Ann M. Robl/		
Printed name	Ann M. Robl		
Date	April 28, 2021	Reg. No.	71,541

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	/Ann M. Robl/		
Typed or printed name	Ann M. Robl	Date	April 28, 2021

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/597,788	01/15/2015	David TIKKANEN	K8001064WOUSCON1

CONFIRMATION NO. 9654

POA ACCEPTANCE LETTER

30589
DUNLAP CODDING, P.C.
PO BOX 16370
OKLAHOMA CITY, OK 73113



Date Mailed: 01/11/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/04/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/mnnguyen/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/597,788	01/15/2015	David TIKKANEN	K8001064WOUSCON1

CONFIRMATION NO. 9654

POWER OF ATTORNEY NOTICE



OC000000122530228

34236
GOWLING WLG (CANADA) LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

Date Mailed: 01/11/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/04/2021.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/mnguyen/

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒

Practitioners associated with Customer Number:

30589

OR

☐

Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒

The address associated with Customer Number:

30589

OR

☐

Firm or individual name

Address

City

State

Zip

Country

Telephone

Email

Assignee name and address:

Mate, LLC
219 W. Wilshire Blvd, Suite 104D
Oklahoma City, Oklahoma 73116

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature

Jon Upton

Date 12/20/20

Name Jon Upton

Telephone 405-520-9220

Title Manager, Mate, LLC

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Lumastream Canada ULCApplication No./Patent No.: 9,078,310Filed/Issue Date: July 7, 2015Titled: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONSMate. LLC, a limited liability corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: David Tikkanen, Jason Neudorf, Steven Lyons, Kyle Hathaway To: Electronic Craftsmen CorporationThe document was recorded in the United States Patent and Trademark Office at
Reel 034728, Frame 0313, or for which a copy thereof is attached.2. From: Electronic Craftsmen Corporation To: E Craftsmen CorporationThe document was recorded in the United States Patent and Trademark Office at
Reel 034728, Frame 0383, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: E Craftsmen Corporation To: Lumastream Canada ULC

The document was recorded in the United States Patent and Trademark Office at
Reel 034728, Frame 0478, or for which a copy thereof is attached.

4. From: Lumastream Canada ULC To: Lumastream, Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 054134, Frame 0089, or for which a copy thereof is attached.

5. From: Lumastream, Inc. To: E Craftsmen Corporation

The document was recorded in the United States Patent and Trademark Office at
Reel 054134, Frame 0330, or for which a copy thereof is attached.

6. From: E Craftsmen Corporation To: Mate. LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 054709, Frame 0940, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Ann M. Robl/

Signature

Ann M. Robl

Printed or Typed Name

January 4, 2021

Date

71,541

Title or Registration Number

Electronic Acknowledgement Receipt

EFS ID:	41543038
Application Number:	14597788
International Application Number:	
Confirmation Number:	9654
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Ann M. Robl/Anne Burns
Filer Authorized By:	Ann M. Robl
Attorney Docket Number:	K8001064WOUSCON1
Receipt Date:	04-JAN-2021
Filing Date:	15-JAN-2015
Time Stamp:	13:51:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	6008014_sb21_Transmittal_01 042021.pdf	170377 a19814680535a7d9960ba4ee49f26f956f356a4	no	1

Warnings:

Information:					
2	Power of Attorney	6008014_AIA80_POA_01042021.pdf	109218	no	1
			54e52203de16e97b99820c10489fa6c6134a47b5		
Warnings:					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73	6008014_AIA96_Statement_01042021.pdf	81790	no	2
			3094ef2c39df495a152cd0054fd702ac8fad1227		
Warnings:					
Information:					
Total Files Size (in bytes):			361385		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	14/597,788
Filing Date	January 15, 2015
First Named Inventor	David Tikkanen
Art Unit	2844 (conf. 9654)
Examiner Name	Jason Crawford
Attorney Docket Number	6008.014

ENCLOSURES (Check all that apply)

☐ Fee Transmittal Form ☐ Fee Attached ☐ Amendment/Reply ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☐ Certified Copy of Priority Document(s) ☐ Reply to Missing Parts/ Incomplete Application ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert to a Provisional Application ☒ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	☐ After Allowance Communication to TC ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☒ Other Enclosure(s) (please identify below): See Remarks
Remarks Electronically Transmitted: January 4, 2021 1) sb21 Transmittal (1 page); 2) AIA80 Power of Attorney (1 page); and 3) AIA96 Statement Under 37 CFR 3.73(c) (2 pages).		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	DUNLAP CODDING, P.C.		
Signature	/Ann M. Robl/		
Printed name	Ann M. Robl		
Date	January 4, 2021	Reg. No.	71,541

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being electronically transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	/Ann M. Robl/		
Typed or printed name	Ann M. Robl	Date	January 4, 2021

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,788	07/07/2015	9078310	K8001064WOUSCON1	9654

34236 7590 06/17/2015
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

David TIKKANEN, Waterloo, CANADA;
LUMASTREAM CANADA ULC, Calgary, CANADA;
Jason NEUDORF, Kitchener, CANADA;
Steven LYONS, Kitchener, CANADA;
Kyle HATHAWAY, Kitchener, CANADA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

34236 7599 05/11/2015
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,788	01/15/2015	David TIKKANEN	K8001064WOUSCON1	9654

TITLE OF INVENTION: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/11/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JASON	2844	315-312000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Gowling Lafleur Henderson LLP
2. Jeffrey W. Wong
3. _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

LUMASTREAM CANADA ULC

Calgary, Canada

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 501613 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jeffrey W. Wong/

Date 2015-05-19

Typed or printed name Jeffrey W. Wong

Registration No. 46414

Electronic Patent Application Fee Transmittal

Application Number:	14597788			
Filing Date:	15-Jan-2015			
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS			
First Named Inventor/Applicant Name:	David TIKKANEN			
Filer:	Jeffrey Wong/Christopher Kreider			
Attorney Docket Number:	K8001064WOUSCON1			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	22383248
Application Number:	14597788
International Application Number:	
Confirmation Number:	9654
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001064WOUSCON1
Receipt Date:	19-MAY-2015
Filing Date:	15-JAN-2015
Time Stamp:	10:18:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$960
RAM confirmation Number	9514
Deposit Account	501613
Authorized User	WONG, JEFFREY W.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	K8001064WOUSCON1-Form.pdf	361762	no	1
			0bf80aa77665d45cd87e4dbca661385cb011fde5		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30766	no	2
			67596f4c15e2ef7ded027f84adf8cd6a9f8c5316		

Warnings:

Information:

Total Files Size (in bytes):			392528
------------------------------	--	--	--------

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

34236 7590 05/11/2015
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

EXAMINER

CRAWFORD, JASON

ART UNIT

PAPER NUMBER

2844

DATE MAILED: 05/11/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

14/597,788

01/15/2015

David TIKKANEN

K8001064WOUSCON1

9654

TITLE OF INVENTION: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/11/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

34236 7590 05/11/2015
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,788	01/15/2015	David TIKKANEN	K8001064WOUSCON1	9654

TITLE OF INVENTION: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/11/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JASON	2844	315-312000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____
 Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/597,788	01/15/2015	David TIKKANEN	K8001064WOUSCON1	9654

34236 7590 05/11/2015
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

EXAMINER

CRAWFORD, JASON

ART UNIT	PAPER NUMBER
----------	--------------

2844

DATE MAILED: 05/11/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/597,788	Applicant(s) TIKKANEN ET AL.	
	Examiner Jason M. Crawford	Art Unit 2844	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 1/15/2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>1/15/15</u> | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/Jason M. Crawford/
Primary Examiner, Art Unit 2844

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Allowable Subject Matter

Claims 1-20 are allowed. The following is an examiner's statement of reasons for allowance:

In regards to claim 1, the prior art does not disclose of a configurable light emitting diode (LED) driver for powering a set of light fixture loads comprising: a power circuit including: an inrush current limit, an apparatus for power factor correction and DC/DC conversion, and a regulated output voltage bus connected to the apparatus for power factor correction and DC/DC conversion; a primary controller for controlling the power circuit; a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for powering the connected light fixture load; and an apparatus for mapping the set of output current drivers to various dimming zones and for mapping output channels into groups, nor would it have been obvious to one of ordinary skill in the art to do so. Claims 2-20 are also allowed as being dependent on claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Crawford whose telephone number is (571)272-6004. The examiner can normally be reached on Mon-Fri 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alex Taningco can be reached on (571) 272-8048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M. Crawford/
Primary Examiner, Art Unit 2844

Notice of References Cited	Application/Control No. 14/597,788		Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.	
	Examiner Jason M. Crawford		Art Unit 2844	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,525,446	09-2013	Tikkanen et al.	315/312
*	B	US-2008/0018261	01-2008	Kastner, Mark Allen	315/192
*	C	US-2008/0025028	01-2008	Gloisten et al.	362/294
*	D	US-2002/0047642	04-2002	Miyagawa, Shozo	315/307
*	E	US-2010/0164403	07-2010	Liu, Da	315/297
*	F	US-2005/0218838	10-2005	Lys, Ihor A.	315/291
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification 	Application/Control No. 14597788	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.
	Examiner JASON M CRAWFORD	Art Unit 2844

CPC						
Symbol					Type	Version
H05B		33	/	08	F	2013-01-01
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
				
				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/JASON M CRAWFORD/ Primary Examiner.Art Unit 2844	03/24/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Issue Classification 	Application/Control No. 14597788	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.
	Examiner JASON M CRAWFORD	Art Unit 2844

☐ Claims renumbered in the same order as presented by applicant															
☐ CPA															
☐ T.D.															
☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	18	17												
2	2	19	18												
3	3	20	19												
4	4	5	20												
6	5														
7	6														
8	7														
9	8														
10	9														
11	10														
12	11														
13	12														
14	13														
15	14														
16	15														
17	16														

NONE	Total Claims Allowed: 20	
(Assistant Examiner)	(Date)	
/JASON M CRAWFORD/ Primary Examiner.Art Unit 2844	03/24/2015	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 8

<i>Index of Claims</i> 	Application/Control No. 14597788	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.
	Examiner JASON M CRAWFORD	Art Unit 2844

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	03/24/2015									
1	1	=									
2	2	=									
3	3	=									
4	4	=									
6	5	=									
7	6	=									
8	7	=									
9	8	=									
10	9	=									
11	10	=									
12	11	=									
13	12	=									
14	13	=									
15	14	=									
16	15	=									
17	16	=									
18	17	=									
19	18	=									
20	19	=									
5	20	=									

Receipt date: 01/15/2015

14597788 - GAU: 2844

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	TIKKANEN, David
Art Unit	
Examiner Name	
Attorney Docket Number	K8001064WOUSCON1

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8197079		2012-06-12	RUUD ET AL.	
	2	5420780		1995-05-30	BERNSTEIN ET AL.	
	3	8604712		2013-12-10	BLOOM ET AL.	
	4	8310171		2012-11-13	REISENAUER ET AL.	
	5	8258721		2012-09-04	MEYER	
	6	7405523		2008-07-29	WILHELM ET AL.	
	7	7310074		2007-12-18	CHEN	
	8	6720745		2004-04-13	LYS ET AL.	

Receipt date: 01/15/2015 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14597788 - GAU: 2844	
	Filing Date			
	First Named Inventor	TIKKANEN, David		
	Art Unit			
	Examiner Name			
	Attorney Docket Number	K8001064WOUSCON1		

	9	5008595		1991-04-16	KAZAR	
	10	8436555		2013-05-07	LO ET AL.	
	11	7804189		2010-09-28	KOEHLER ET AL.	
	12	7961113		2011-06-14	RABINER ET AL	
	13	8143792		2012-03-27	JOO ET AL.	

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS

Remove

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20050289279		2005-12-29	FAILS ET AL.	
	2	20050218838		2005-10-06	LYS	
	3	20080018261		2008-01-24	KASTNER	
	4	20090179594		2009-07-16	YANG	

Receipt date: 01/15/2015 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14597788 - GAU: 2844	
	Filing Date			
	First Named Inventor	TIKKANEN, David		
	Art Unit			
	Examiner Name			
	Attorney Docket Number	K8001064WOUSCON1		

5	20020047642		2002-04-25	MIYAGAWA	
6	20080025028		2008-01-31	GLOISTEN ET AL.	
7	20100164403		2010-07-01	LIU	
8	20060132063		2006-06-22	HUNG ET AL.	
9	20100231136		2010-09-16	REISENAUER ET AL.	
10	20100066267		2010-03-18	MEYER	
11	20110018464		2011-01-27	LO ET AL.	
12	20110309746		2011-12-22	ECKEL ET AL.	

If you wish to add additional U.S. Published Application citation information please click the Add button. [Add](#)

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1	2008052293	WO		2008-05-08	CLIPSAL AUSTRALIA PTY LTD.		☐

Receipt date: 01/15/2015 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14597788 - GAU: 2844	
	Filing Date			
	First Named Inventor	TIKKANEN, David		
	Art Unit			
	Examiner Name			
	Attorney Docket Number	K8001064WOUSCON1		

	2	2009039112	WO		2009-03-26	EXCLARA		☐
--	---	------------	----	--	------------	---------	--	--------------------------

If you wish to add additional Foreign Patent Document citation information please click the Add button **Add**

NON-PATENT LITERATURE DOCUMENTS

Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	ERICSSON AB, Power Supplies Goes Digital White Paper, October 2006	☐
	2	SKANDA; MICROCHIP TECHNOLOGY INC., Power Factor Correction in Power Conversion Applications using the dsPIC® DSC", AN1106, June 2007	☐
	3	TRAXON TECHNOLOGIES, LED Engine XB 3W-108 Technical Specifications and User Manual Version 1.1, 2007	☐
	4	PENWELL CORPORATION, Dialight Lumidrives Launches Colurdriver XP for High-Power LEDs, LEDs MAGAZINE, downloaded from http://www.ledsmagazine.com/press/15469 , 2007-09-25	☐
	5	Colourdriver XP data sheet, 2008-07-30	☐
	6	US-TECH ONLINE, Dialight: New High Power LED Driver, downloaded from http://www.us-tech.com , October 2007	☐
	7	IST LTD., iDrive™ 1000 The Intelligent 210W LED Driver User Manual, v. 1.7, 2008-06-20	☐
	8	ROAL ELECTRONICS, S.P.A, Programmable RGB LED Driver 200 Watts Model RHPS180 Product Details, Rev. 2, 2007-10	☐

Receipt date: 01/15/2015 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14597788 - GAU: 2844	
	Filing Date			
	First Named Inventor	TIKKANEN, David		
	Art Unit			
	Examiner Name			
	Attorney Docket Number	K8001064WOUSCON1		

9	INTERNATIONAL SEARCHING AUTHORITY (CA), International Search Report and Written Opinion for International Patent Application No. PCT/CA2009/001295, 2010-01-13	☐
10	SEARCH & EXAMINATION REPORT (UK), Further Search Report and Examination Report for GB1102782.8, 2012-09-06	☐
11	UNITED STATES PATENT AND TRADEMARK OFFICE, Office Action for 13/059336, 2013-01-23	☐
12	UNITED STATES PATENT AND TRADEMARK OFFICE, Office Action for US Patent App. No. 13/466,529, 2013-12-13	☐
13	UNITED STATES PATENT AND TRADEMARK OFFICE, Office Action for US Patent App. No. 13/466,509, 2014-02-21	☐
14	UNITED STATES PATENT AND TRADEMARK OFFICE, Office Action for US Patent App. No. 13/466,509, 2014-06-27	☐
15	UNITED STATES PATENT AND TRADEMARK OFFICE, Notice of Allowance for US Patent App. No. 13/466,509, 2014-10-06	☐
16	POWER VECTOR, A DIVISION OF ELECTRONIC CRAFTSMEN, Product Information Sheet for IRIS LED Driver/ Dimmer, 2007-10-22	☐
17	TRYKA L.E.D. LTD, Product Information Sheet for IDS-12 Intelligent Drive System, http://www.tryka.co.uk/IDS-12.htm , downloaded 2007-07-18	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Jason Crawford/ (03/23/2015)	Date Considered	
--------------------	-------------------------------	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Receipt date: 01/15/2015 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14597788 - GAU: 2844
	Filing Date		
	First Named Inventor	TIKKANEN, David	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	K8001064WOUSCON1	

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Receipt date: 01/15/2015 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14597788 - GAU: 2844
	Filing Date		
	First Named Inventor	TIKKANEN, David	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	K8001064WOUSCON1	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2015-01-15
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 9654

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/597,788	01/15/2015	315	2844	K8001064WOUSCON1		
RULE						
APPLICANTS LUMASTREAM CANADA ULC, Calgary, CANADA, Assignee (with 37 CFR 1.172 Interest);						
INVENTORS David TIKKANEN, Waterloo, CANADA; Jason NEUDORF, Kitchener, CANADA; Steven LYONS, Kitchener, CANADA; Kyle HATHAWAY, Kitchener, CANADA;						
** CONTINUING DATA ***** This application is a CON of 13/941,871 07/15/2013 which is a CON of 13/059,336 03/22/2011 PAT 8525446 which is a 371 of PCT/CA2009/001295 09/17/2009 which claims benefit of 61/097,963 09/18/2008 (*)Data provided by applicant is not consistent with PTO records.						
** FOREIGN APPLICATIONS *****						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 01/20/2015						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /JASON CRAWFORD/ Acknowledged Examiner's Signature		☐ Met after Allowance JC Initials	STATE OR COUNTRY CANADA	SHEETS DRAWINGS 12	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 1
ADDRESS GOWLING LAFLEUR HENDERSON LLP 50 QUEEN STREET NORTH, STE. 1020 P.O. BOX 2248 KITCHENER, ON N2H6M2 CANADA						
TITLE CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 14597788	Applicant(s)/Patent Under Reexamination TIKKANEN ET AL.
	Examiner JASON M CRAWFORD	Art Unit 2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B 33/0815, 41/28, 33/0803, 33/0806	3/24/2015	JC

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
315	247,291,294,297,302,307,312	3/24/2015	JC

SEARCH NOTES		
Search Notes	Date	Examiner
See attached search	3/24/2015	JC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
All	see text search	3/24/2015	JC

	/JASON M CRAWFORD/ Primary Examiner.Art Unit 2844
--	--

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S230	14	S228 not S229	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 08:12
S229	2	((primary and secondary) adj2 control\$4) and S228	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 08:11
S228	16	S225 and (LED (light adj emit\$4 adj diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 08:11
S227	0	(S204 S205 S206 S207) and S225	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 08:11
S226	0	315/247,291,294,297,302,307,312.ccls. and S225	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 08:11
S225	44	S224 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 08:11
S224	92	(PFC (power adj factor)) and inrush and map\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 08:11
S223	12	S218 not S219	US-PGPUB;	OR	ON	2015/03/24

JC

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			07:42
S222	5	S220 not S221	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:42
S221	1	S220 and inrush	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:41
S220	6	S218 and (PFC (power adj factor\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:41
S219	6	S218 and (PFC inrush (power adj factor\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:41
S218	18	S215 not (S217 S216)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:41
S217	12	("20050024877" "7141941" "20050105311" "4492899" "20060001381" "7276861" "5661645" "7489086" "3176204" "6507159" "6274987" "7129652").PN.	US-PGPUB; USPAT	OR	ON	2015/03/24 07:41
S216	7	("20050218838" "20050289279" "20020047642" "20080018261" "20080018261" "8197079" "20090179594" "5420780").PN.	US-PGPUB; USPAT	OR	ON	2015/03/24 07:41
S215	25	("20020047642" "20050218838" "20050289279" "20060132063" "20080018261" "20080025028" "20090179594" "20100066267" "20100164403" "20100231136" "20110018464" "20110309746" "5008595" "5420780" "6720745" "7310074" "7405523" "7804189" "7961113" "8143792" "8197079" "8258721" "8310171" "8436555" "8604712").PN.	US-PGPUB; USPAT	OR	ON	2015/03/24 07:41

S214	5	S213 and (ICSP (in adj circuit adj serial adj program\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:39
S213	413	("315"/\$.ccls. "361"/\$.ccls.) and S212	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:39
S212	964	(u adj shap\$3) with (heatsink\$3 (heat adj sink\$3)) and fins	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:39
S211	0	S210 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:37
S210	10	S209 and (LED (light adj emit\$4 adj diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:37
S209	12	((primary and secondary) adj2 control\$4) and S208	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:37
S208	8608	(S204 S205 S206 S207) and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:37
S207	1168	h05b33/0806.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:37
S206	6678	h05b33/0803.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2015/03/24 07:37

			DERWENT; IBM_TDB			
S205	2795	h05b41/28.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:37
S204	11156	h05b33/0815.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:37
S203	1	S202 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:36
S202	6	S201 and (PFC (power adj factor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:36
S201	20	((primary and secondary) adj2 control\$4) and S200	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:36
S200	9206	315/247,291,294,297,302,307,312.ccls. and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:36
S199	13	S198 and (LED (light adj emit\$4 adj diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:36
S198	30	S197 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:36
S197	232	("315"/\$.ccls. "361"/\$.ccls.) and S196	US-PGPUB; USPAT; USOCR;	OR	ON	2015/03/24 07:36

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S196	1702	S195 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:36
S195	3474	(PFC (power adj factor)) and (heatsink\$3 (heat adj sink\$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/24 07:36
S194	18	S191 not (S193 S192)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/23 12:56
S193	12	("20050024877" "7141941" "20050105311" "4492899" "20060001381" "7276861" "5661645" "7489086" "3176204" "6507159" "6274987" "7129652").PN.	US-PGPUB; USPAT	OR	ON	2015/03/23 12:56
S192	7	("20050218838" "20050289279" "20020047642" "20080018261" "20080018261" "8197079" "20090179594" "5420780").PN.	US-PGPUB; USPAT	OR	ON	2015/03/23 12:56
S191	25	("20020047642" "20050218838" "20050289279" "20060132063" "20080018261" "20080025028" "20090179594" "20100066267" "20100164403" "20100231136" "20110018464" "20110309746" "5008595" "5420780" "6720745" "7310074" "7405523" "7804189" "7961113" "8143792" "8197079" "8258721" "8310171" "8436555" "8604712").PN.	US-PGPUB; USPAT	OR	ON	2015/03/23 12:55
S190	0	S189 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 13:33
S189	10	S188 and (LED (light adj emit\$4 adj diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 13:33
S188	12	((primary and secondary) adj2 control\$4) and S187	US-PGPUB; USPAT;	OR	ON	2015/03/09 13:32

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S187	8586	(S183 S184 S185 S186) and @ad< "20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 13:28
S186	1159	h05b33/0806.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 13:21
S185	6611	h05b33/0803.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 13:21
S184	2787	h05b41/28.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 13:20
S183	10952	h05b33/0815.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 13:20
S179	6	S178 and (DC adj DC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S178	13	S177 and (LED (light adj emit\$4 adj diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S177	30	S176 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40

S176	232	("315"/\$.ccls. "361"/\$.ccls.) and S175	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S175	1701	S174 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S174	3458	(PFC (power adj factor)) and (heatsink\$3 (heat adj sink\$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S173	10	S171 not S172	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S172	2	S171 and (thermistor and coil)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S171	12	S170 and (heatsink\$3 (heat adj sink\$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S170	30	(PFC (power adj factor)) and S169	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S169	176	S168 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S168	273	((inrush (in adj rush)) adj2 limit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2015/03/09 12:40

			DERWENT; IBM_TDB			
S167	12	S166 and (heatsink\$3 (heat adj sink\$3) fins)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S166	30	(PFC (power adj factor)) and S165	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S165	176	S164 and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S164	273	((inrush (in adj rush)) adj2 limit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S163	1	S162 and (inrush (in adj rush))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S162	6	S161 and (PFC (power adj factor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S161	20	((primary and secondary) adj2 control\$4) and S160	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40
S160	9203	315/247,291,294,297,302,307,312.ccls. and @ad<"20080918"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/09 12:40

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S236	2	S235 and (light\$3 illuminat\$3)	US-PGPUB; USPAT; UPAD	OR	ON	2015/03/24 07:54
S235	4	S234 and @ad<"20080918"	US-PGPUB; USPAT; UPAD	OR	ON	2015/03/24 07:54
S234	11	(ICSP (in adj circuit adj serial adj program\$4)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/03/24 07:54
S233	13	(PFC (power adj factor)).clm. and S232	US-PGPUB; USPAT; UPAD	OR	ON	2015/03/24 07:54
S232	19	(PFC (power adj factor)) and S231	US-PGPUB; USPAT; UPAD	OR	ON	2015/03/24 07:54
S231	62	((led (light\$3 adj emit\$4 adj diode)) and (inrush (in adj rush))).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/03/24 07:54
S181	19	(PFC (power adj factor)) and S180	US-PGPUB; USPAT; UPAD	OR	ON	2015/03/09 12:41
S180	60	((led (light\$3 adj emit\$4 adj diode)) and (inrush (in adj rush))).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/03/09 12:41

3/ 24/ 2015 1:23:13 PM
H:\ EAST\ Workspaces\ 14597788.wsp



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/597,788	01/15/2015	David TIKKANEN	K8001064WOUSCON1

CONFIRMATION NO. 9654

PUBLICATION NOTICE



OC000000074912814

34236
GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

Title:CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

Publication No.US-2015-0115839-A1

Publication Date:04/30/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In The Matter of United States Patent Application:

Applicant : **Lumastream Canada ULC**
Application No. : **14/597,788**
Filed : **January 15, 2015**
Title : **CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS**
TC/A.U. : **2844**
Docket No. : **K8001064WOUSCON1**
Conf Number : **9654**
Date : **February 9, 2015**

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Preliminary Amendment

Dear Commissioner of Patents:

Kindly amend this application as follows:

Amendments to the Abstract begin on page **2** of this paper, and include a replacement sheet submitted herewith.

Remarks begin on page **3** of this paper.

Amendments to the Abstract:

Please replace the Abstract currently on file with the following amended abstract. A replacement clean copy of the amended Abstract is submitted herewith.

~~The disclosure is directed at a~~ A configurable light emitting diode (LED) driver/dimmer for ~~controlling~~ powering a set of light fixture loads ~~comprising~~including a power circuit;and a primary digital controller for controlling the power circuit;. The driver further includes a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load;and a secondary digital controller for controlling the set of output current drivers. The driver also includes an apparatus for mapping the set of output current drivers to various dimming zones and for mapping output channels into groups.; ~~wherein the secondary controller transmits LED control information to control outputs of the set of output current drivers; and wherein the secondary digital controller provides digital feedback control information to the primary digital controller.~~

REMARKS

The Abstract has been amended to more accurately reflect the disclosure. No new matter has been added as a result of this amendment.

Respectfully submitted,

By: /Jeffrey W. Wong/
Jeffrey W. Wong
Agent for Applicant
Reg. No. 46414

Gowling Lafleur Henderson LLP
Suite 1020
50 Queen Street North
P.O. Box 2248
Kitchener, Ontario N2H 6M2
Canada

T 519-575-7543
F 519-579-0141

EDC_LAW\1265195\1

ABSTRACT

A configurable light emitting diode (LED) driver for powering a set of light fixture loads including a power circuit and a primary controller for controlling the power circuit. The driver further includes a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load and a secondary controller for controlling the set of output current drivers. The driver also includes an apparatus for mapping the set of output current drivers to various dimming zones and for mapping output channels into groups.

Electronic Acknowledgement Receipt

EFS ID:	21441295
Application Number:	14597788
International Application Number:	
Confirmation Number:	9654
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001064WOUSCON1
Receipt Date:	09-FEB-2015
Filing Date:	15-JAN-2015
Time Stamp:	16:21:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		k8001064-pa.pdf	78942 f18603ef2bd51ea6bea1836ab85f06cbfd4a8af8	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Preliminary Amendment	1	1
	Abstract	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3

Warnings:

Information:

2	Abstract	k8001064-abstract.pdf	54209	no	1
			36103f86571c7a7b44387d15f9e059aae75a baa4		

Warnings:

Information:

Total Files Size (in bytes):			133151
------------------------------	--	--	--------

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/597,788	Filing Date 01/15/2015	☐ To be Mailed
---	---	----------------------------------	---------------------------------------

 ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	02/09/2015	CLAIMS REMAINING AFTER AMENDMENT					
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	
AMENDMENT	(Column 1)	(Column 2)	(Column 3)	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
		CLAIMS REMAINING AFTER AMENDMENT					
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE							

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

 LIE
/STELLA LITTLE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/597,788	01/15/2015	2844	1600	K8001064WOUSCON1	20	1

CONFIRMATION NO. 9654

34236

GOWLING LAFLEUR HENDERSON LLP
50 QUEEN STREET NORTH, STE. 1020
P.O. BOX 2248
KITCHENER, ON N2H6M2
CANADA

FILING RECEIPT



OC000000072932711

Date Mailed: 01/22/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

David TIKKANEN, Waterloo, CANADA;
Jason NEUDORF, Kitchener, CANADA;
Steven LYONS, Kitchener, CANADA;
Kyle HATHAWAY, Kitchener, CANADA;

Applicant(s)

LUMASTREAM CANADA ULC, Calgary, CANADA

Power of Attorney: The patent practitioners associated with Customer Number 34236

Domestic Priority data as claimed by applicant

This application is a CON of 13/941,871 07/15/2013
which is a CON of 13/059,336 03/22/2011 PAT 8525446 *
which is a 371 of PCT/CA2009/001295 09/17/2009
which claims benefit of 61/097,963 09/18/2008

(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 01/20/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/597,788**

Projected Publication Date: 04/30/2015

Non-Publication Request: No

Early Publication Request: No

Title

CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

Preliminary Class

315

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
14/597,788

APPLICATION AS FILED - PART I

(Column 1)		(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
			TOTAL			TOTAL	1600

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:



Practitioners associated with Customer Number:

34236

OR



Practitioner(s) named below (If more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:



The address associated with Customer Number:

34236

OR

☐	Firm or Individual Name			
	Address			
	City	State	Zip	
	Country			
	Telephone	Email		

Assignee Name and Address: Lumastream Canada ULC
400-3rd Avenue S.W. , Calgary, AB, T2P 4H2, Canada

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	Aug 21/2014
Name	David TIKKANEN	Telephone	519-744-5677
Title	Vice President, Lumastream Canada ULC		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)****Title of
Invention****CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING
APPLICATIONS**

As the below named inventor, I hereby declare that:

This declaration
is directed to:

The attached application, or



United States application or PCT international application number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001
by fine or imprisonment of not more than five (5) years, or both.**WARNING:**

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: _____

Date (Optional): _____

Signature: _____

Kyle Grahame HATHAWAY

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS, SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of
Invention

CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

As the below named inventor, I hereby declare that:

This declaration
is directed to:



The attached application, or



United States application or PCT international application number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: _____

Date (Optional): _____

Signature: Steven LYONS

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)****Title of
Invention****CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING
APPLICATIONS**

As the below named inventor, I hereby declare that:

This declaration
is directed to:

The attached application, or

United States application or PCT International application number _____
filed on _____

The above-identified application was made or authorized to be made by me;

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001
by fine or imprisonment of not more than five (5) years, or both.**WARNING:**

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor:

Signature:


Jason NEUDORF

Date (Optional): 2013 July 9

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1460, Alexandria, VA 22313-1460.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of
Invention

CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

As the below named inventor, I hereby declare that:

This declaration
is directed to:



The attached application, or



United States application or PCT international application number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor:



Date (Optional): _____

Signature:

David TIKKANEN

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

WORLDWIDE

ASSIGNMENT

We:

- | | |
|--|--|
| 1) TIKKANEN, David
194 Silverwood Place
Waterloo, Ontario N2T 2R9
Canada | 2) NEUDORF, Jason
306-30 Bridge Street West
Kitchener, Ontario N2K 1K4
Canada |
| 3) LYONS, Steven
7800 Rd, 45 Glen Allan
Wallenstein, Ontario N0B 2S0
Canada | 4) SCOTT, Todd, William
581 Drummerhill Crescent
Waterloo, Ontario N2T 1G3
Canada |
| 5) HATHAWAY, Kyle
5 Norbert Place
Kitchener, Ontario N2K 1E5
Canada | 6) JANSEN, David, Waineworth
333A Mayview Crescent
Waterloo, Ontario N2V 1P9
Canada |

for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, confirm that effective at least as early as September 18, 2008, we did sell and assign to:

ELECTRONIC CRAFTSMEN CORPORATION
73 Schaefer Street
Waterloo, Ontario N2L 4C4
Canada

all our right, title and interest in the United States of America, Canada, and all countries foreign thereto, in and to the invention, disclosed in, relating to, and entitled:

A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS

as fully described in our United States patent application filed September 18, 2008, serial no. 61/097,963, and to any application for patent claiming priority therefrom, and to all our corresponding right, title and interest in and to any patent issued therefrom, and to any patent issued from a continuation, continuation-in-part, re-issue, divisional or re-examination application derived, or claiming priority, from the above application.

We authorize the firm of Borden Ladner Gervais LLP to insert any further identification necessary to make this assignment suitable for recordation in the Patent Offices of any country as may be required.

SIGNED at

Kitchener, Ontario
City or Town

Canada
Country

this

06
Day

day of

Oct
Month

2008

David Tikkanen
David Tikkanen

STATEMENT BY WITNESS

I, SCOTT COLQUHOUN

(name of witness)

whose full post office address is

120 MANSON STREET, KITCHENER, ONTARIO, N2H 0A1

was personally present and did see **David Tikkanen** execute the within assignment and such assignor is personally known to me to be the person described in such document.

[Signature]
Signature of Witness

SIGNED at

Kitchener, Ontario
City or Town

Canada
Country

this

6
Day

day of

Oct
Month

2008

Jason Neudorf
Jason Neudorf

STATEMENT BY WITNESS

I, SCOTT COLQUHOUN

(name of witness)

whose full post office address is

120 MANSON STREET, KITCHENER, ONTARIO, N2H 0A1

was personally present and did see **Jason Neudorf** execute the within assignment and such assignor is personally known to me to be the person described in such document.

[Signature]
Signature of Witness

SIGNED at KITCHENER ONTARIO CANADA
City or Town Country
this 6 day of OCTOBER, 2008
Day Month
Steven Lyons
Steven Lyons

STATEMENT BY WITNESS	
I, <u>SCOTT COLQUHOUN</u> (name of witness)	whose full post office address is
<u>120 MANSION STREET, KITCHENER, ONTARIO, N2H 0A1</u>	
was personally present and did see Steven Lyons execute the within assignment and such assignor is personally known to me to be the person described in such document.	
<u>[Signature]</u> Signature of Witness	

SIGNED at KITCHENER, ONTARIO CANADA
City or Town Country
this 6th day of OCTOBER, 2008
Day Month
Todd William Scott
Todd William Scott

STATEMENT BY WITNESS	
I, <u>SCOTT COLQUHOUN</u> (name of witness)	whose full post office address is
<u>120 MANSION STREET, KITCHENER, ONTARIO, N2H 0A1</u>	
was personally present and did see Todd William Scott execute the within assignment and such assignor is personally known to me to be the person described in such document.	
<u>[Signature]</u> Signature of Witness	

SIGNED at Kitchener Canada
City or Town Country
this 06 day of Oct, 2008
Day Month
Kyle Hathaway
Signature of Assignor

STATEMENT BY WITNESS	
I, <u>SCOTT COLQUHOUN</u> (name of witness)	whose full post office address is
<u>120 MANSION STREET, KITCHENER, ONTARIO, N2H 0A1</u>	
was personally present and did see Kyle Hathaway execute the within assignment and such assignor is personally known to me to be the person described in such document.	
<u>[Signature]</u> Signature of Witness	

SIGNED at Kitchener Canada
City or Town Country
this 6th day of October, 2008
Day Month
David Waineworth Jansen
Signature of Assignor

STATEMENT BY WITNESS	
I, <u>SCOTT COLQUHOUN</u> (name of witness)	whose full post office address is
<u>120 MANSION STREET, KITCHENER, ONTARIO, N2H 0A1</u>	
was personally present and did see David Waineworth Jansen execute the within assignment and such assignor is personally known to me to be the person described in such document.	
<u>[Signature]</u> Signature of Witness	

ASSIGNMENT OF INTELLECTUAL PROPERTY RIGHTS

In consideration of One Dollar and other good and valuable consideration, the receipt and adequacy of which is hereby acknowledged,

Electronic Craftsmen Corporation
(a corporation under the laws of the Province of Ontario, Canada)
73 Schaefer Street
Waterloo, Ontario N2L 4C4
CANADA

does hereby sell and assign to:

E Craftsmen Corporation
(a corporation under the laws of the Province of Ontario, Canada)
73 Schaefer Street
Waterloo, Ontario N2L 4C4
CANADA

all its right, title and interest in and to the patents, design patents, industrial designs, trademarks, and applications for same listed in Schedule A hereto, specifically including any rights granted based on any of the applications and any divisional, continuation, reissue or other related applications derived from any of the patents, design patents, industrial designs, trademarks, and applications for same; and with respect to the trademarks, specifically including all associated goodwill.

SIGNED at MISSISSAUGA PEEL Canada
City or Town Country
this 30TH day of JUNE, 2009.

Electronic Craftsmen Corporation


Authorized Signing Officer

Name: L.M. SAYERS

Title: SECRETARY

STATEMENT BY WITNESS

I, PETER A. PENN, whose full post office address is 906 MARAMIS CRT
(name of witness)

MISSISSAUGA, ONTARIO, CANADA L5H 4G8
was personally present and did see CHRIS SAYERS

(Signing Officer)

execute the within assignment and who is personally known to me to be the person
signing such document.



Signature of Witness

SCHEDULE A

INDUSTRIAL DESIGNS AND DESIGN PATENTS

Country	Serial No.	Filing Date	Title	BLG Ref No.
Canada	127922	23-09-2008	LIGHT EMITTING DIODE DIMMER CONTROL	ID 21790-1
Canada	129957	11-03-2009	CONFIGURABLE LED DRIVER/DIMMER	ID 21796-1
U.S.	29/334,022	19-03-2009	CONFIGURABLE LED DRIVER/DIMMER	ID 21790-2

PATENTS

Country	Serial No.	Filing Date	Title	BLG Ref No.
Canada	2,564,659	19-10-2006	MODULATION METHOD AND APPARATUS FOR DIMMING AND/OR COLOUR MIXING UTILIZING LEDS	PAT 60829-1
U.S.	11/550,937	19-10-2006	MODULATION METHOD AND APPARATUS FOR DIMMING AND/OR COLOUR MIXING UTILIZING LEDS	PAT 60829-2
U.S.	61/097,963	18-09-2008	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	PAT 67545P-2

TRADE-MARKS

Country	Serial No.	Filing Date	Reg. No.	Reg. Date	Title/Mark	BLG Ref No.
Canada	1,367,373	12-10-2007			POWER VECTOR ENGINEERED LED POWER & DESIGN	TM 66688-1
U.S.	77/346,154	06-12-2007			POWER VECTOR ENGINEERED LED POWER & DESIGN	TM 66688-2
Canada	855,165	04-09-1997	512,251	26-05-1999	POWER VECTOR	TM 66689-1
Canada	859,673	24-10-1997	512,295	26-05-1999	POWER VECTOR & DESIGN	TM 66690-1
U.S.	77/346,161	06-12-2007			POWER VECTOR & DESIGN	TM 66690-2
U.S.	77/346,166	06-12-2007	3,624,883	19-05-2009	ENGINEERED LED POWER	TM 67081-2

ASSIGNMENT OF PATENTS

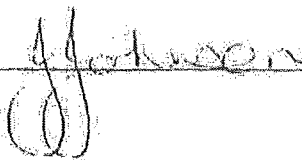
IN CONSIDERATION of One (\$1.00) Dollar and for other good and valuable consideration, the receipt and adequacy of which is hereby acknowledged, E CRAFTSMEN CORPORATION (the "Assignor"), whose registered head office address is 73 Schaefer Street, Waterloo, Ontario N2L 4C4, does hereby sell, assign and transfer to LUMASTREAM CANADA ULC (the "Assignee"), whose registered office is 400-3rd Avenue S.W., Calgary Alberta, T2P 4H2, all of its right, title and interest in and to the patents and applications for same listed on Schedule "A" annexed hereto, specifically including any rights granted based on any of the applications and any divisional, continuation, reissue or other related applications derived from any of the patents and applications.

THE ASSIGNOR further hereby covenants that it will, at any time, upon the request of the Assignee, execute and deliver to the Assignee new or confirmatory instruments and perform (at the Assignee's reasonable expense) any other acts which the Assignee may reasonably request in order to fully assign and transfer to and vest in the Assignee, all of the Assignor's right, title and interest in and to the patents including those listed in Schedule "A" annexed hereto.

DATED this 15th day of April, 2011.

E. CRAFTSMEN CORPORATION

Witness



Name: Tom Richards

Title: President

I have authority to bind the Corporation

SCHEDULE A

INDUSTRIAL DESIGNS AND DESIGN PATENTS

Country	Serial No.	Filing Date	Title	BLG Ref No.
Canada	127922	23-09-2008	LIGHT EMITTING DIODE DIMMER CONTROL	ID 21790-1
Canada	129957	11-03-2009	CONFIGURABLE LED DRIVER/DIMMER	ID 21796-1
U.S.	29/334,022	19-03-2009	CONFIGURABLE LED DRIVER/DIMMER	ID 21790-2

PATENTS

Country	Serial No.	Filing Date	Title	BLG Ref No.
Canada	2,564,659	19-10-2006	MODULATION METHOD AND APPARATUS FOR DIMMING AND/OR COLOUR MIXING UTILIZING LEDS	PAT 60829-1
U.S.	11/550,937	19-10-2006	MODULATION METHOD AND APPARATUS FOR DIMMING AND/OR COLOUR MIXING UTILIZING LEDS	PAT 60829-2
U.S.	61/097,963	18-09-2008	A CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	PAT 67545P-2

TRADE-MARKS

Country	Serial No.	Filing Date	Reg. No.	Reg. Date	Title/Mark	BLG Ref No.
Canada	1,367,373	12-10-2007			POWER VECTOR ENGINEERED LED POWER & DESIGN	TM 66688-1
U.S.	77/346,154	06-12-2007			POWER VECTOR ENGINEERED LED POWER & DESIGN	TM 66688-2
Canada	855,165	04-09-1997	512,251	26-05-1999	POWER VECTOR	TM 66689-1
Canada	859,673	24-10-1997	512,295	26-05-1999	POWER VECTOR & DESIGN	TM 66690-1
U.S.	77/346,161	06-12-2007			POWER VECTOR & DESIGN	TM 66690-2
U.S.	77/346,166	06-12-2007	3,624,883	19-05-2009	ENGINEERED LED POWER	TM 67081-2

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		
	First Named Inventor	TIKKANEN, David	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	K8001064WOUSCON1	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8197079		2012-06-12	RUUD ET AL.	
	2	5420780		1995-05-30	BERNSTEIN ET AL.	
	3	8604712		2013-12-10	BLOOM ET AL.	
	4	8310171		2012-11-13	REISENAUER ET AL.	
	5	8258721		2012-09-04	MEYER	
	6	7405523		2008-07-29	WILHELM ET AL.	
	7	7310074		2007-12-18	CHEN	
	8	6720745		2004-04-13	LYS ET AL.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		
Filing Date		
First Named Inventor	TIKKANEN, David	
Art Unit		
Examiner Name		
Attorney Docket Number	K8001064WOUSCON1	

	9	5008595		1991-04-16	KAZAR	
	10	8436555		2013-05-07	LO ET AL.	
	11	7804189		2010-09-28	KOEHLER ET AL.	
	12	7961113		2011-06-14	RABINER ET AL	
	13	8143792		2012-03-27	JOO ET AL.	

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS

Remove

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050289279		2005-12-29	FAILS ET AL.	
	2	20050218838		2005-10-06	LYS	
	3	20080018261		2008-01-24	KASTNER	
	4	20090179594		2009-07-16	YANG	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		
Filing Date		
First Named Inventor	TIKKANEN, David	
Art Unit		
Examiner Name		
Attorney Docket Number	K8001064WOUSCON1	

5	20020047642		2002-04-25	MIYAGAWA	
6	20080025028		2008-01-31	GLOISTEN ET AL.	
7	20100164403		2010-07-01	LIU	
8	20060132063		2006-06-22	HUNG ET AL.	
9	20100231136		2010-09-16	REISENAUER ET AL.	
10	20100066267		2010-03-18	MEYER	
11	20110018464		2011-01-27	LO ET AL.	
12	20110309746		2011-12-22	ECKEL ET AL.	

If you wish to add additional U.S. Published Application citation information please click the Add button. **Add**

FOREIGN PATENT DOCUMENTS

Remove

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1	2008052293	WO		2008-05-08	CLIPSAL AUSTRALIA PTY LTD.		☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		
Filing Date		
First Named Inventor	TIKKANEN, David	
Art Unit		
Examiner Name		
Attorney Docket Number	K8001064WOUSCON1	

	2	2009039112	WO		2009-03-26	EXCLARA		☐
--	---	------------	----	--	------------	---------	--	--------------------------

If you wish to add additional Foreign Patent Document citation information please click the Add button **Add**

NON-PATENT LITERATURE DOCUMENTS

Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	ERICSSON AB, Power Supplies Goes Digital White Paper, October 2006	☐
	2	SKANDA; MICROCHIP TECHNOLOGY INC., Power Factor Correction in Power Conversion Applications using the dsPIC® DSC", AN1106, June 2007	☐
	3	TRAXON TECHNOLOGIES, LED Engine XB 3W-108 Technical Specifications and User Manual Version 1.1, 2007	☐
	4	PENWELL CORPORATION, Dialight Lumidrives Launches Colurdriver XP for High-Power LEDs, LEDs MAGAZINE, downloaded from http://www.ledsmagazine.com/press/15469 , 2007-09-25	☐
	5	Colourdriver XP data sheet, 2008-07-30	☐
	6	US-TECH ONLINE, Dialight: New High Power LED Driver, downloaded from http://www.us-tech.com , October 2007	☐
	7	IST LTD., iDrive™ 1000 The Intelligent 210W LED Driver User Manual, v. 1.7, 2008-06-20	☐
	8	ROAL ELECTRONICS, S.P.A, Programmable RGB LED Driver 200 Watts Model RHPS180 Product Details, Rev. 2, 2007-10	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		
Filing Date		
First Named Inventor	TIKKANEN, David	
Art Unit		
Examiner Name		
Attorney Docket Number	K8001064WOUSCON1	

9	INTERNATIONAL SEARCHING AUTHORITY (CA), International Search Report and Written Opinion for International Patent Application No. PCT/CA2009/001295, 2010-01-13	☐
10	SEARCH & EXAMINATION REPORT (UK), Further Search Report and Examination Report for GB1102782.8, 2012-09-06	☐
11	UNITED STATES PATENT AND TRADEMARK OFFICE, Office Action for 13/059336, 2013-01-23	☐
12	UNITED STATES PATENT AND TRADEMARK OFFICE, Office Action for US Patent App. No. 13/466,529, 2013-12-13	☐
13	UNITED STATES PATENT AND TRADEMARK OFFICE, Office Action for US Patent App. No. 13/466,509, 2014-02-21	☐
14	UNITED STATES PATENT AND TRADEMARK OFFICE, Office Action for US Patent App. No. 13/466,509, 2014-06-27	☐
15	UNITED STATES PATENT AND TRADEMARK OFFICE, Notice of Allowance for US Patent App. No. 13/466,509, 2014-10-06	☐
16	POWER VECTOR, A DIVISION OF ELECTRONIC CRAFTSMEN, Product Information Sheet for IRIS LED Driver/ Dimmer, 2007-10-22	☐
17	TRYKA L.E.D. LTD, Product Information Sheet for IDS-12 Intelligent Drive System, http://www.tryka.co.uk/IDS-12.htm , downloaded 2007-07-18	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	TIKKANEN, David
Art Unit	
Examiner Name	
Attorney Docket Number	K8001064WOUSCON1

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	TIKKANEN, David
Art Unit	
Examiner Name	
Attorney Docket Number	K8001064WOUSCON1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey W. Wong/	Date (YYYY-MM-DD)	2015-01-15
Name/Print	Jeffrey W. Wong	Registration Number	46414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
8 May 2008 (08.05.2008)

PCT

(10) International Publication Number
WO 2008/052293 A1

(51) International Patent Classification:
H05B 37/02 (2006.01) G09G 3/14 (2006.01)

(74) Agent: MADDERNS PATENT & TRADE MARK
ATTORNEYS, Level 1, 64 Hindmarsh Square, Adelaide,
S.A. 5000 (AU).

(21) International Application Number:
PCT/AU2007/001697

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH,
CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG,
ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL,
IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK,
LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW,
MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL,
PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY,
TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA,
ZM, ZW.

(22) International Filing Date:
5 November 2007 (05.11.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Date:
2006/06139 3 November 2006 (03.11.2006) AU

(71) Applicant (for all designated States except US): CLIP-
SAL AUSTRALIA PTY LTD [AU/AU]; 12 Park Terrace,
Bowden, S.A. 5007 (AU).

(72) Inventors; and

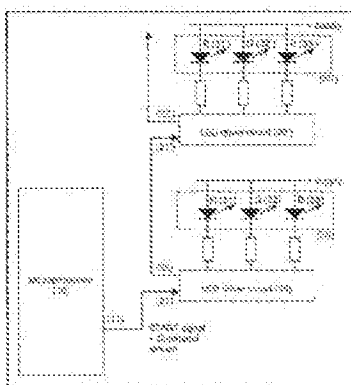
(75) Inventors/Applicants (for US only): QUICK, Ashleigh,
Glen [AU/AU]; 12 Park Terrace, Bowden, S.A. 5007 (AU);
NEWMAN, Andrew [AU/AU]; 12 Park Terrace, Bowden,
S.A. 5007 (AU).

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL,
PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

(54) Title: LIGHT EMITTING DIODE DRIVER AND METHOD



(57) Abstract: Disclosed is a method and apparatus for controlling a plurality of Light Emitting Diodes (LEDs). A communications protocol is also provided, which comprises a START code, a first Command packet and at least one subsequent Command packet. An LED driver receives a signal according to the protocol, and separates the first Command packet from the signal and controls an LED associated with the LED driver in accordance with instructions in the first Command packet. The LED driver then outputs the remaining signal for use by one or more subsequent LED drivers.

LIGHT EMITTING DIODE DRIVER AND METHOD

TECHNICAL FIELD

This invention relates to Light Emitting Diodes and to apparatus and methods for their control.

PRIORITY

The present application claims priority from Australian Provisional Patent Application No. 2006906139 entitled "Light Emitting Diode Driver and Method".

The entire content of this provisional application is hereby incorporated by reference.

BACKGROUND

A common requirement for electronic equipment is to have a visual indication on a control device. Such a control device could be a button, lever, knob, or similar, and the visual indication is often used to show the state of whatever is controlled – for example an electrical load being turned on or off, or a door open or closed.

In modern electronic equipment, the visual indication is readily provided by a light emitting diode (LED) which has the advantages of being small, cheap, and a long operating life. Multiple colours may be achieved by making use of several LEDs of different colour – these can even be mounted in the same physical package.

By separate dimming of each component colour, a dual-colour combination LED can be used to mix the two component colours to create additional colours, as perceived by a human observer. More recently, three colour combination LEDs have become available, and some of these include elemental components that emit in the colours Red, Green and Blue. By selective dimming of these components, any colour, including white, can be obtained.

In order to produce any resultant colour, an RGB combination LED needs each of the colour components to have a separate dimmable drive. Whilst LED dimming is

straightforward using the well-established method of pulse-width modulation, such a typical combination LED will usually have at least 4 terminals: a common point and a drive input for each of the three colour elements.

Using a single three colour RGB combination LED with a common point and 3 drive inputs is relatively easy to drive to obtain any desired human-perceived colour. For example, a small micro-processor can use 3 separate pulse-width modulated outputs to drive such an indicator. An exemplary arrangement of this application is shown in prior art figure 1. In figure 1, there is shown microprocessor 10 driving two LEDs 30 and 30'. Each LED has respective colour components of red (31), green (32) and blue (33). Respective resistors 34, 35 and 36 are also provided to limit the current applied to the LED components.

In operation, microprocessor 10 generates and transmits control signals to each LED 30 and corresponding colour component 31, 32 and 33 to control the operation of each LED in accordance with a sequence of instructions programmed into microprocessor 10 as will be understood by the person skilled in the art.

As can be seen from Figure 1, driving 2 LEDs requires 6 drive signals 11, 12, 13, 14, 15 and 16, one for each LED component, or three for each LED in the case of a three-colour LED.

It will be appreciated however, that when many such combination LEDs need to be driven (irrespective of the number and nature of the coloured elements) - potentially all showing separate information (for example colour and brightness) the number of drive signals rapidly increases. For example to drive 10 such RGB combination LEDs would require 30 drive signals. As the number of multi-colour combination LEDs in a product increases, the complexity of wiring these to a controller device increases, as does the complexity of the controlling device. For example, a large number of wiring paths might be needed on a printed circuit board, and a large number of pulse width modulated outputs might be needed on a microprocessor.

LED controller devices are currently available that make use of serial data buses – the most notable being the Philips inter-integrated circuit (I2C) bus. Such LED controllers allow a 2-wire control output from a microprocessor to be connected to a LED driver IC, which in turn is connected to one or more combination LEDs. By sending appropriate commands to the I2C driver IC, a suitable colour and brightness can be obtained from the combination LED(s). If the combination LED contains red, green and blue elements, then by appropriate selection of brightness of the elements, any colour can be obtained.

Whilst being an improvement on directly connecting LEDs to a microprocessor, systems using these approaches have a number of deficiencies. These deficiencies include the high cost of the LED driver ICs, the limited addressing range of these bus systems, and the additional need to route power and / or ground separately to the LEDs and the driver IC's - increasing circuit board layout complexity and potentially cost, through the need for multi-layer PCBs. Whilst this limited addressing can be overcome by the use of I2C bridges, this adds extra devices and cost to such an arrangement.

It is therefore an object of the present invention to provide an alternative to existing LED control systems.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention, there is provided a communications protocol for use in controlling a plurality of Light Emitting Diodes (LEDs) associated with respective LED drivers, the communications protocol comprising a first Command packet containing at least one instruction for controlling a first of the plurality of LEDs, and at least one subsequent Command packet containing instructions for controlling at least one subsequent LED, connected in series with the first LED.

In one form, the protocol further comprises a START code prior to the first Command packet.

In one form, the respective START codes are provided prior to each subsequent Command packets.

In one form, at least one of the first and subsequent Command packets contains instructions for controlling a plurality of elements within a respective LED.

According to a second aspect of the present invention, there is provided a Light Emitting Diode (LED) driver comprising:

- an input for receiving a signal according to the communications protocol as claimed in any one of claims 1 to 4;

- means for controlling an associated LED in accordance with the at least one instruction in the first Command packet; and

- an output for outputting the at least one subsequent Command packet.

In one form, the LED further comprises means for separating the first Command packet from the signal.

According to a third aspect of the present invention, there is provided a Light Emitting Diode (LED) comprising an LED driver according to the second form of the present invention.

According to a fourth aspect of the present invention, there is provided a device for controlling a plurality of LEDs, the device comprising:

- means for generating and outputting a signal comprising a START code, a first Command packet and at least one subsequent Command packet;

- first means for receiving the signal and controlling an LED associated with the first means in accordance with instructions in the first Command packet;

first means for separating the first Command packet from the signal to provide a remaining signal; and

means for outputting the remaining signal.

In one form, the means for generating is a microprocessor.

In one form, the first means for receiving and controlling, the first means for separating and the means for outputting comprise an LED driver.

In one form, the LED driver is a microprocessor.

In one form, there is at least one subsequent driver associated with at least one subsequent LED.

According to a fifth aspect of the present invention, there is provided an electronic device comprising:

a plurality of Light Emitting Diodes (LEDs);

a plurality of LED drivers as claimed in claim 5 for controlling a respective one of the plurality of Light Emitting Diodes; and

a microprocessor for generating and outputting a signal according to the communications protocol as claimed in any one of claims 1 to 4 to a first of the plurality of LED drivers.

According to a sixth aspect of the present invention, there is provided a method for controlling a plurality of LEDs, the method comprising:

generating and outputting a signal comprising a START code, a first Command packet and at least one subsequent Command packet;

receiving the signal and controlling an LED in accordance with instructions in the first Command packet;

separating the first Command packet from the signal to provide a remaining signal; and

outputting the remaining signal.

According to a seventh aspect of the present invention, there is provided a machine readable medium containing machine executable instructions to perform the method of the sixth aspect of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 - shows a prior art arrangement with 2 RGB combination LEDs connected to a microcontroller;

Figure 2 - shows a first exemplary implementation of an aspect of the present invention in which several LED driver circuits are connected to a single microprocessor output;

Figure 3 - shows an exemplary timing diagram and command sequence that could be applied to the arrangement of Figure 2;

Figure 4 - shows an alternative exemplary timing diagram and command sequence that could be applied to the arrangement of Figure 2;

Figure 5 - shows a second exemplary implementation according to an aspect of the present invention, in which two LED driver circuits are connected to 2 microprocessor outputs;

Figure 6 - shows an exemplary timing diagram and command sequence that could be applied to the arrangement of Figure 5;

Figure 7 - shows a block diagram of an LED driver as shown in Figure 2;

Figure 8 - shows a reference circuit diagram of the LED driver of Figure 2;

Figure 9 - shows a block diagram of an LED driver as shown in Figure 5.

Figure 10 - shows a circuit diagram of an exemplary embodiment of the master section of the arrangement shown in Figure 2; and

Figure 11 - shows a circuit diagram of an exemplary embodiment of the driver section of the arrangement shown in Figure 2.

DETAILED DESCRIPTION

Figure 2 shows an electronic device 1 showing an exemplary arrangement of components according to a first aspect of the present invention. In Figure 2 there is

shown a microprocessor 10 with a single output signal 11 connected to LED driver circuit constructed according to another aspect of the present invention. Details of the operation of LED driver circuit 20 will be discussed in more detail further below. LED driver 20 drives LED 30.

Figure 2 also shows a second LED 30', driven by a second LED driver 20'.

Microprocessor 10 can be any microprocessor, from any manufacturer, that is capable of transmitting a data stream out of a single output – a technique commonly referred to as “bit bashing”. Such microprocessors are readily available from many manufacturers, in an almost infinite variant of capability variations. Suitable microprocessors are available from manufacturers including Atmel, Texas Instruments, Zilog, Freescale, ST, and many others.

According to an aspect of the present invention, microprocessor 10 generates a control signal and transmits this along output 11 to an input 21 of the LED driver 20.

As will be described in more detail further below, the signal generated by microprocessor 10 consists of a series of Command packets, each intended for one of the LEDs needed to be controlled by microcontroller 10. Driver 20 accepts the signal, and strips off (or separates) the first Command packet in the signal or data stream, and outputs the remainder of the signal or data stream via output 22. The remainder of the signal is then input into the input 21' of the next LED driver 20', which then strips off the next Command packet and outputs the remainder of the signal via output 22'. The signal continues to travel from one LED driver to the next, until all Command packets have been stripped off or separated.

The Command packet for each LED contains information to allow each LED driver 20 to drive each of the red (31), green (32) and blue (33) light components of respective LEDs.

In one form, the communication protocol includes a START code indication, followed by one or more subsequent Command packets. The first Command packet is applied to the first LED driver circuit that the signals reach after the controlling device, and is removed from the stream. Everything after the first Command packet is then passed out of the first LED driver circuit to the second LED driver circuit and so on, as described above. Each LED driver circuit knows to expect a new Command packet when it sees the START code. To ensure that the START code is passed along, each LED driver circuit can either re-generate the START code, as shown in Figure 3, or can simply pass it out when it is received, as shown in Figure 4.

In one form, the LED driver circuit 20 has the function of accepting in its Command packet a setting of the brightness of each of the colour elements of its attached combination LED.

By placing the LED driver circuits in a sequential cascade arrangement, there is no need to address information to each circuit – instead, addressing will be achieved by the order of the electrical interconnection. Thus, for example, the first Command packet will be accepted by the first LED driver circuit (and subsequent Command packets are simply passed out to the next one in the line). Similarly the second LED driver circuit, not seeing the Command packet that was removed by the first LED driver circuit, will accept the second Command packet transmitted, and pass on any that follow. This process is repeated until the last LED driver circuit is reached.

Figures 3 and 4 show an exemplary structure of such a signal, containing multiple Command packets. Figure 3 shows the case where the START code is regenerated, while Figure 4 shows the case where the START code is copied instead of being regenerated. The first row (A) of Figures 3 and 4 show the signal as generated by the microprocessor 10. This signal is input to the input 21 of the first LED driver device 20 (for example as seen in Figure 2). In one form, the signal may include a START code 110 at the beginning of the signal. In one form, the START code 110 comprises a pattern that is distinguishable from the Command packet information. When a LED

driver circuit recognises the sequence comprising the START code, it knows that the Command packet that follows is for its use, and subsequent commands are to be relayed out to a subsequent device.

One suitable method of generating the START code is to encode the Command portions using "bit-stuffing", and use a coding violation as the START code – a technique which is well established in the prior art. Another possible method is to transmit the Command portion as a stream of asynchronous serial data bits, and to transmit a "Break" symbol as the START code. Whilst these are two suitable methods, there are many others that provide the same behaviour.

Following the START code 110, when present, is the first Command 120. This Command contains control information for the first LED driver 20 to control the various elements of the LED 30 to which it is connected (see Figure 2). Upon receiving the signal, LED driver 20 strips off, or otherwise "switches off" the first Command so as to be not present, or ignored by subsequent LED drivers, and retransmits or otherwise forwards the signal from its output 22 to the next LED driver 20' in the series.

The signal may contain as many Commands as there are LED drivers, or may contain more or less, depending upon the required function of the LEDs to be controlled. For example, if there are more Commands than LEDs, the extra Commands could be simply ignored. If there are fewer Commands than LEDs, either the extra LEDs may not be provided instructions, or the extra LEDs may perform the same function as the last LED which had a specific Command, or could be otherwise connected to previous LEDs to perform the same function as those.

In line B of Figures 3 and 4, the signal can be seen to have had the first Command 120 removed, with subsequent Commands 130 and 140 remaining. This is the structure of the signal on the output 22 of LED driver 20 and the input 21' of LED driver 20' in Figure 2. In row C, the signal can be seen to have had first and second Commands removed, to have remaining the last Command for the last LED required to be

controlled. In the case of Figure 2, this signal structure will appear on the output 22' of LED driver 20', for input into the next LED driver (not shown).

The structure of each Command will be tailored for the required operation of each individual LED 30. In one example, the structure of the Command can be a set of binary coded brightness levels for each individual LED. For RGB LEDs, the Command might comprise typically between 4 and 8 bits to encode the brightness levels of the Red, Green, and Blue component LEDs. Any precise ordering or encoding of these brightness levels is unimportant, provided it is applied consistently between the microprocessor 10 and all LED driver circuits.

In this manner, a single microprocessor could drive a single combination LED, or any other number, without additional hardware interconnections being required to the microprocessor. In another form, this arrangement could be used to drive two or more LEDs having only one colour component, or having any number of colour components. In some forms, the LEDs driven could have varying numbers of colour or other control components, for example, the microprocessor might set a flash pattern on a LED, or combination LED, by setting a flash rate, or setting periods of time for a LED or LED components are to be switched on and off.

For example, a system may have 10 LEDs, 5 of which may be single colour components, 2 may be 2-colour components and 3 may be 3-colour components. Of course the number of controllable components within an LED need not be restricted to 3, but could be any number as may be required for the particular application.

One example of a structure of a Start bit used as the Start code, is 1440us wide, with a low for 960us and a high pulse for 480us. A data bit definition for the Command packets could be "Bit 0" having 60 us width with a 20us low and a 40us high pulse. The "Bit 1" definition could have a 60us width with 40us low and 20us high pulse. Such coding is known as Manchester coding and is well known to the person skilled in the art. Of course, any other form of suitable coding may also be used.

In generating a signal according to this aspect of the invention, the microprocessor does so in accordance with a software program. An example of a suitable program for controlling five LEDs, 2 of a single colour component and 3 of 3 colour components is shown in the following pseudo-code:

Assumptions:

A single Command comprises brightness for Red, Green and Blue, in that order

A single colour LED has its brightness set by the Red component of a Command only

A suitable coding system has been chosen for the Commands and the START code

The two single colour LEDs are wired closest to the microprocessor, followed by the 3, 3 colour LEDs

Pseudo-code:

Send the START code

Send the Command for the first single colour LED comprising the set (First brightness, anything, anything)

Send the Command for the second single colour LED comprising the set (Second brightness, anything, anything)

Send the Command for the third LED comprising the set (Third Red, third Green, Third Blue)

Send the Command for the fourth LED comprising the set (Fourth Red, Fourth Green, Fourth Blue)

Send the Command for the fifth LED comprising the set (Fifth Red, Fifth Green, Fifth Blue)

In an alternative form of the present invention, the signal generated by the microprocessor 10 need not have a START code embedded therein. In this case, two microprocessor outputs may be used, the first such output being used to signal the start of a new command stream, and the second such output being used to encode

the stream of Commands being sent to each of the driver circuits in turn. Such an encoding of the Commands could comprise digital data, typically as a stream of binary digits (bits).

Figure 5 shows an arrangement according to this aspect of the invention, in which like elements are numbered accordingly. In this arrangement, microprocessor 10 has two outputs, 11 and 12. Output 11 functions as previously described with reference to Figure 2, but output 12 now provides the START information to inform each LED driver 20, 20' ... when a new Command stream is being transmitted, in place of the START code being present in the signal.

In this arrangement, LED drivers 20, 20' ... will have a third input 23, for receiving the START code from microprocessor 10.

Figure 6 shows an exemplary structure of the control signals generated by microprocessor 10 in the arrangement as shown in Figure 5. In row A of Figure 6, a START code is provided on output 12 of microprocessor 10 and input to each of the LED drivers 20 via respective inputs 23. Row B shows the structure of the signal generated by microprocessor 10 and output on output 11, to be received by each LED driver 20 in turn. It will be noted that no START code is present in this structure as it is being provided by output 12. Rows B, C and D of Figure 6 correspond to rows A, B and C of Figures 3 and 4 and function in the same way.

Figure 7 shows an exemplary system block diagram of an LED driver circuit for an LED driver as shown in Figure 2 that has a single input for receiving a START code and Command packets. In this arrangement, the START code and Command packets enter driver 20 at data input 21. The START code is detected at block 24 and the Command packet is received at block 26, decoded and passed to pulse width modulation (PWM) channels block 27 for application to the components of the LED (not shown) via an optional current limiting block 29. Oscillator/clock generator 28 provides the timing for block PWM block 27.

From block 26, the remaining Command packets are passed through to data output 22. If the START code is to be regenerated and passed through to subsequent drivers, this is done at block 35 and provided to output 22 with the remaining Command codes from block 26.

Figure 8 shows a reference circuit diagram of the arrangement of Figure 7. This reference circuit uses a small, low-cost microprocessor as the main element of the LED driver circuit, with all major functions implemented in software. Suitable microprocessors are available from Texas Instruments, Freescale, and other manufacturers. Naturally, such an arrangement can be replaced by any other functionally equivalent circuit, whether using software or not.

Figure 9 shows an exemplary system block diagram of an LED driver circuit for an LED driver as shown in Figure 5 that has a single input for receiving a START code and Command packets. This is an alternative arrangement for driver 20 to that of Figure 7. In this arrangement, the Command packets enter driver 20 at data input 21. The START code that is generated separately at a second output of microprocessor 10 (as described previously with reference to Figure 5) enters driver 20 at second input 23. The Command packets and START code are received at block 26. The Command packets are decoded and passed to pulse width modulation (PWM) channels block 27 for application to the components of the LED (not shown) via an optional current limiting block 29. Oscillator/clock generator 28 provides the timing for block PWM block 27.

The START code and remaining Command packets are then sent to subsequent drivers via output 22.

The arrangement of Figure 9 can equally be implemented as a single microprocessor having programmed thereon instructions to carry out the functions of the arrangement of Figure 9. This would be as shown in Figure 8.

Figure 10 shows an alternative embodiment of the LED controller master section, showing microprocessor 10, which in this example is a PIC16F73. The particular layout and function of the surrounding circuitry will be apparent to the person skilled in the art and will not be described in detail herein.

Figure 11 shows an implementation of an LED driver 20 and associated LED 30 with individually-drivable colour components 31 (Red), 32 (Green) and 33 (Blue). In this example, the microprocessor used for the driver 20 is an EM78P153S available from ELAN Microelectronics Corporation in Taiwan. Again, the layout and function of the surrounding circuitry will be apparent to the person skilled in the art and will not be described in detail herein.

In use, a circuit will be built up using a plurality of drivers 20 as shown in Figure 11, cascaded in daisy-chain style. Each LED 30, 30', 30'' e.t.c. would be associated with its own driver 20, 20', 20'' e.t.c.

In another aspect of the invention, there is provided a method of controlling a plurality of LEDs. The first aspect of the method provides for the generation of a signal or data stream according to the protocol described above. In particular, the method includes generating the signal or data stream by generating a Start code, generating a first Command packet, generating at least one subsequent Command packet and then outputting the signal. A further aspect of the method includes receiving the data stream or signal, separating the first Command packet from the data stream or signal to provide a remaining data stream or signal, controlling a first LED in accordance with instructions in the first command packet and outputting the remaining data stream or signal. The remaining data stream or signal is then processed in the same way with respect to the at least one subsequent Command packet.

In another aspect, the present invention provides computer executable instructions which cause a computer to perform the various steps of the methods described herein. In particular, the computer executable instructions cause the computer (such

as microprocessor 10) to execute the steps of generating a first Command packet containing at least one instruction for controlling a first of the plurality of LEDs, and generating at least one subsequent Command packet containing instructions for controlling at least one subsequent LED, connected in series with the first LED. In another form, the computer executable instructions cause the computer to also generate a START code and insert this in a data stream in front of the Command and subsequent Command packets. In another form, the computer executable instructions cause the computer to generate separate START codes prior to each of the Command and subsequent Command packets.

In another aspect, the computer executable instructions also cause a computer to perform the steps performed by the driver 20. As described with reference to Figure 8, the computer could also be a microprocessor. In this aspect, the computer executable instructions cause the computer to execute the steps of receiving a data stream including a first Command packet and at least one subsequent Command packet, separating the first Command packet from the data stream, controlling an LED associated with the computer in accordance with instructions in the first Command packet, and outputting the at least one subsequent Command packet for use by another driver.

In one form, the computer executable instructions may also cause the computer to detect a START code in the data stream, and either pass that START code through and output it with the at least one subsequent Command packet or generate a new START code and output that with the at least one Command packet.

In another aspect of the invention, there is also provided a machine readable medium containing the machine executable instructions described above. Such a machine readable medium includes the memory on the microprocessor 10, or other, separate memory medium, including a CD, a DVD, a Flash drive or other portable memory medium.

In one embodiment, the LED driver circuit could be implemented as an integrated circuit, using a suitable semiconductor technology such as but not limited to silicon. A variation of this embodiment would be to attach and integrate the circuit with an LED device. In one example, this could be an LED with 3 primary colour LED elements. In such an embodiment the current limit resistors may be integrated, or replaced by a transistor based current limiting arrangement, both techniques being well established.

In such an embodiment, which made use of a single control signal from a microprocessor, the completed packaged integrated driver circuit and LEDs would have four electrical connections comprising a power input, a power return (or ground), a data in signal, and a data out signal. An embodiment making use of two outputs from microprocessor would include a fifth electrical connection used to indicate the start of a new stream of Commands.

In one form the microprocessor 10 would transmit the Command stream at a rate of at least 100,000 bits/second. Such a rate would allow the colour and brightness of 10 RGB LEDs to be completely updated in less than 3 milliseconds. Naturally, operation at even faster speeds would be straightforward and yield commensurately lower update times. Naturally, where rapid update or only a small number of LEDs is to be controlled, a lower rate would also be suitable.

This arrangement has the advantages that it allows any number of combination LEDs to be driven without need for special expansion devices when an addressing range is exceeded; it allows a small number of drive signals from the controlling device; and it offers the benefit of integrating such a LED driver circuit into the same component package as the combination LED. Integration of the driver circuit into the LED package minimises the overall cost, and dramatically reduces the number of electrical interconnections between the driver IC and the colour elements of the combination LED.

The various aspects of the present invention may be used in any number of electronic devices that have LEDs as part of their circuitry. This includes entertainment devices such as televisions, digital set-top boxes, sound systems, DVD players, CD players, remote control units. It also includes computers and computer peripherals, and displays for vehicles and other devices. The various aspects of the present invention can also be applied to electronic devices that have not yet been invented at the time of filing the present application.

It will be understood that the above has been described with reference to particular embodiments and that many variations and modifications may be made within the scopes of the different aspects of the present invention.

Throughout the specification and the claims that follow, unless the context requires otherwise, the words "comprise" and "include" and variations such as "comprising" and "including" will be understood to imply the inclusion of a stated integer or group of integers, but not the exclusion of any other integer or group of integers.

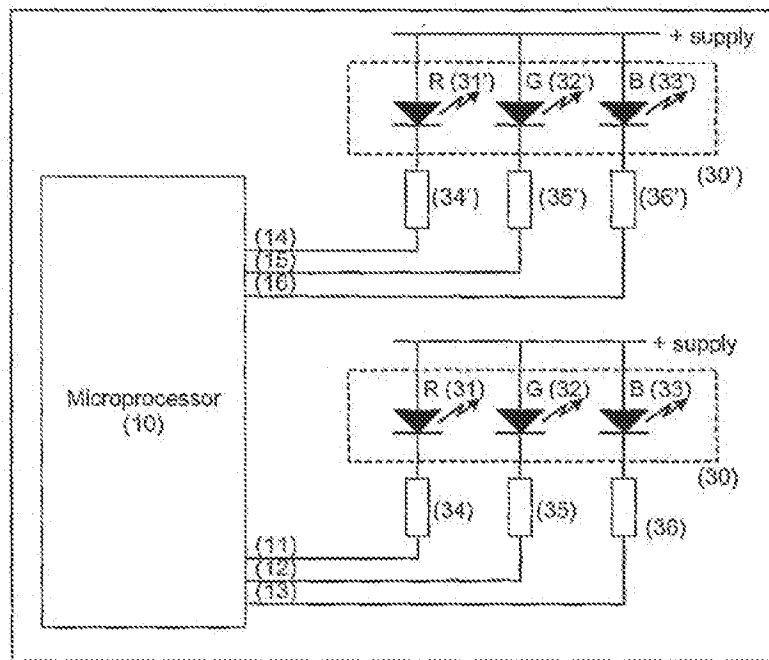
The reference to any prior art in this specification is not, and should not be taken as, an acknowledgement of any form of suggestion that such prior art forms part of the common general knowledge.

THE CLAIMS:

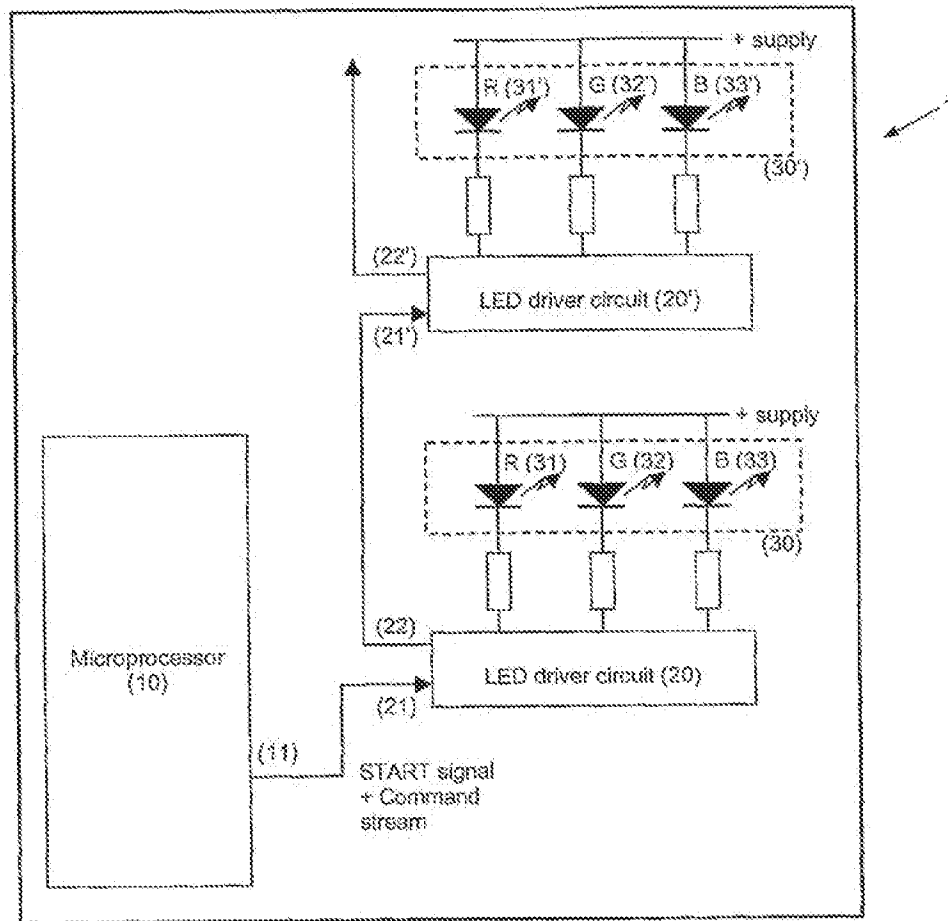
1. A communications protocol for use in controlling a plurality of Light Emitting Diodes (LEDs) associated with respective LED drivers, the communications protocol comprising a first Command packet containing at least one instruction for controlling a first of the plurality of LEDs, and at least one subsequent Command packet containing instructions for controlling at least one subsequent LED, connected in series with the first LED.
2. A communications protocol as claimed in claim 1 further comprising a START code prior to the first Command packet.
3. A communications protocol as claimed in claim 2 wherein respective START codes are provided prior to each subsequent Command packet.
4. A communications protocol as claimed in claim 1 wherein at least one of the first and subsequent Command packets contains instructions for controlling a plurality of elements within a respective LED.
5. A Light Emitting Diode (LED) driver comprising:
 - an input for receiving a signal according to the communications protocol as claimed in any one of claims 1 to 4;
 - means for controlling an associated LED in accordance with the at least one instruction in the first Command packet; and
 - an output for outputting the at least one subsequent Command packet.
6. A Light Emitting Diode (LED) driver as claimed in claim 5 further comprising means for separating the first Command packet from the signal.
7. A Light Emitting Diode (LED) comprising an LED driver as claimed in claim 5.

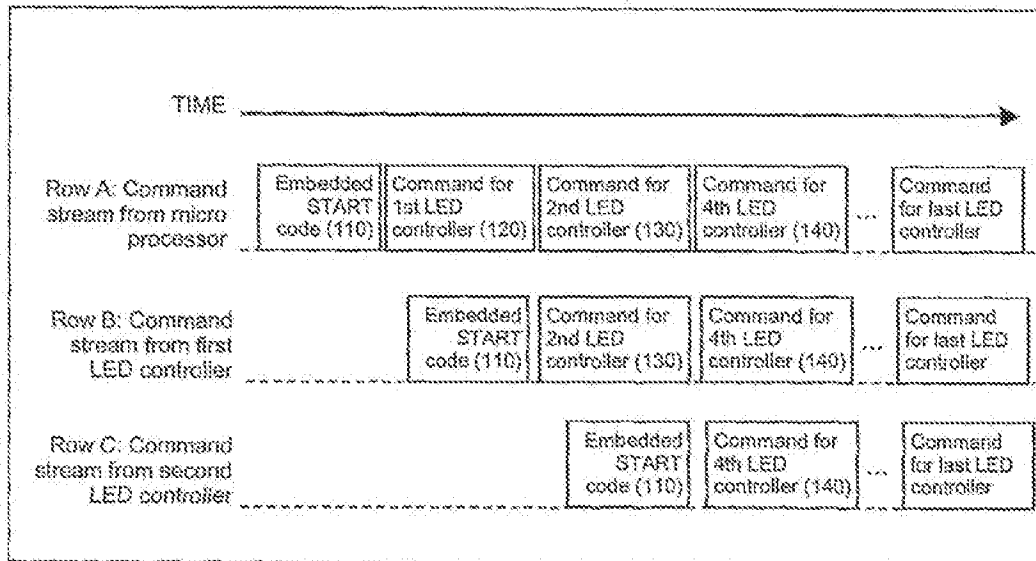
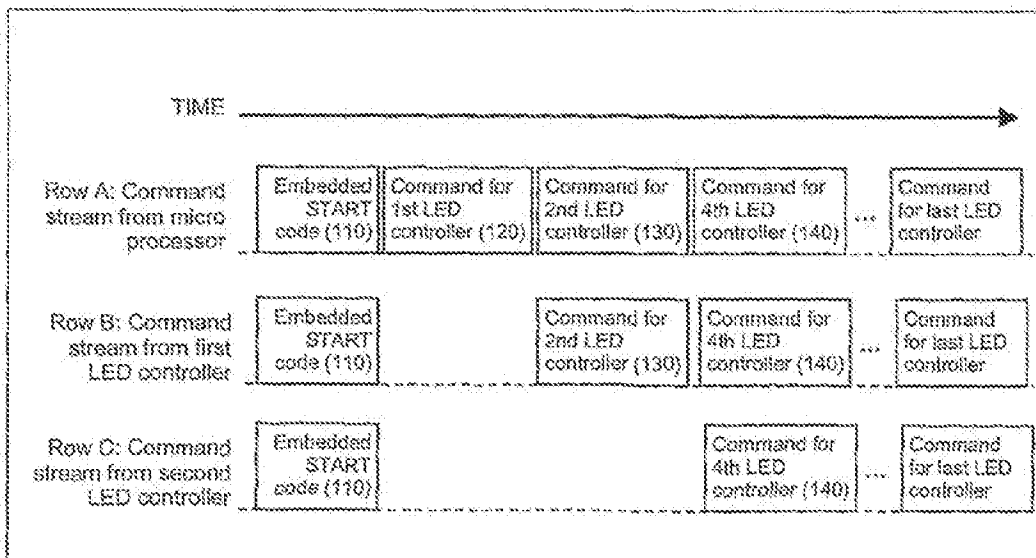
8. A device for controlling a plurality of LEDs, the device comprising:
 - means for generating and outputting a signal comprising a START code, a first Command packet and at least one subsequent Command packet;
 - first means for receiving the signal and controlling an LED associated with the first means in accordance with instructions in the first Command packet;
 - first means for separating the first Command packet from the signal to provide a remaining signal; and
 - means for outputting the remaining signal.
9. A device as claimed in claim 8 wherein the means for generating is a microprocessor.
10. A device as claimed in claim 9 wherein the first means for receiving and controlling, the first means for separating and the means for outputting comprise an LED driver.
11. A device as claimed in claim 10 wherein the LED driver is a microprocessor.
12. A device as claimed in claims 10 to 11 further comprising at least one subsequent driver associated with at least one subsequent LED.
13. An electronic device comprising:
 - a plurality of Light Emitting Diodes (LEDs);
 - a plurality of LED drivers as claimed in claim 5 for controlling a respective one of the plurality of Light Emitting Diodes; and
 - a microprocessor for generating and outputting a signal according to the communications protocol as claimed in any one of claims 1 to 4 to a first of the plurality of LED drivers.

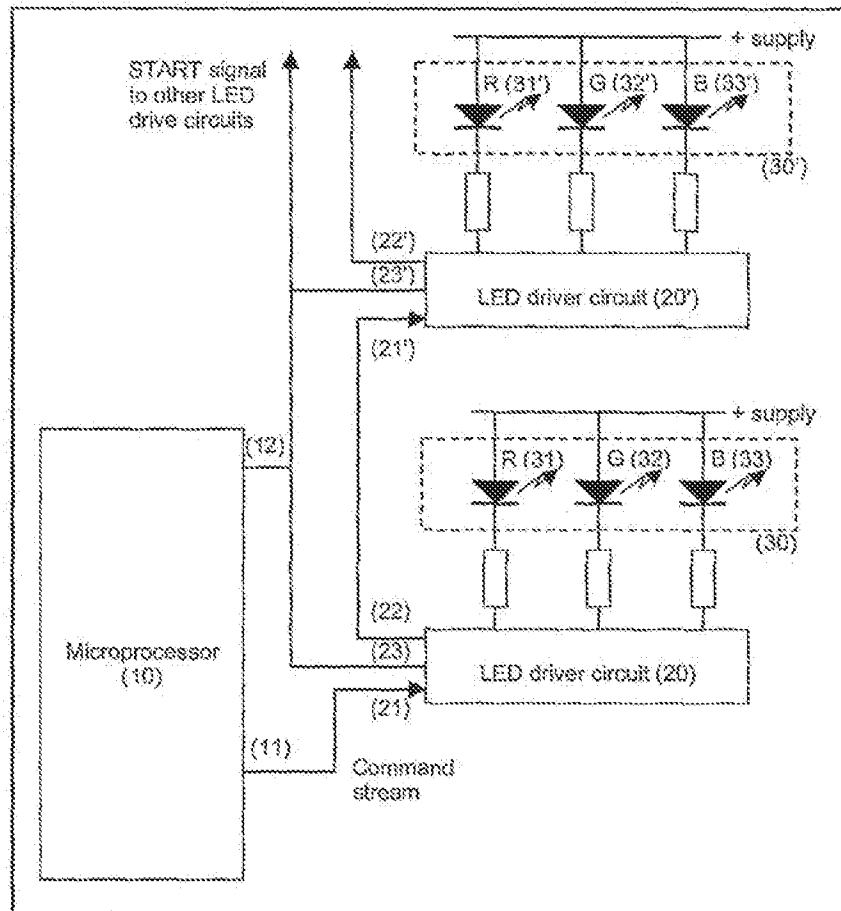
14. A method for controlling a plurality of LEDs, the method comprising:
- generating and outputting a signal comprising a START code, a first Command packet and at least one subsequent Command packet;
 - receiving the signal and controlling an LED in accordance with instructions in the first Command packet;
 - separating the first Command packet from the signal to provide a remaining signal; and
 - outputting the remaining signal.
15. A machine readable medium containing machine executable instructions to perform the method of claim 14.

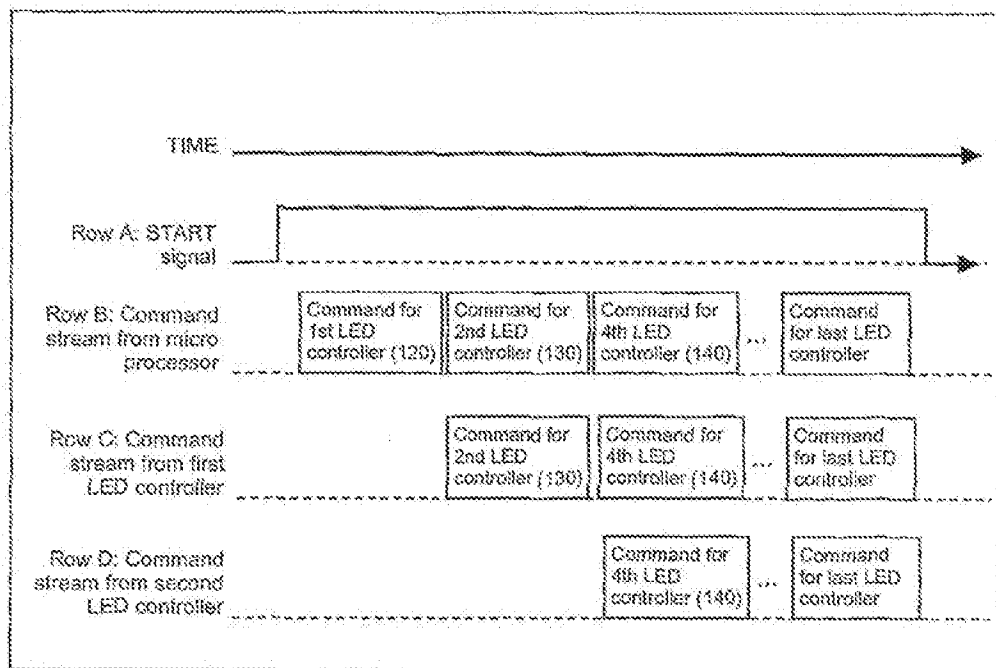
**Figure 1**

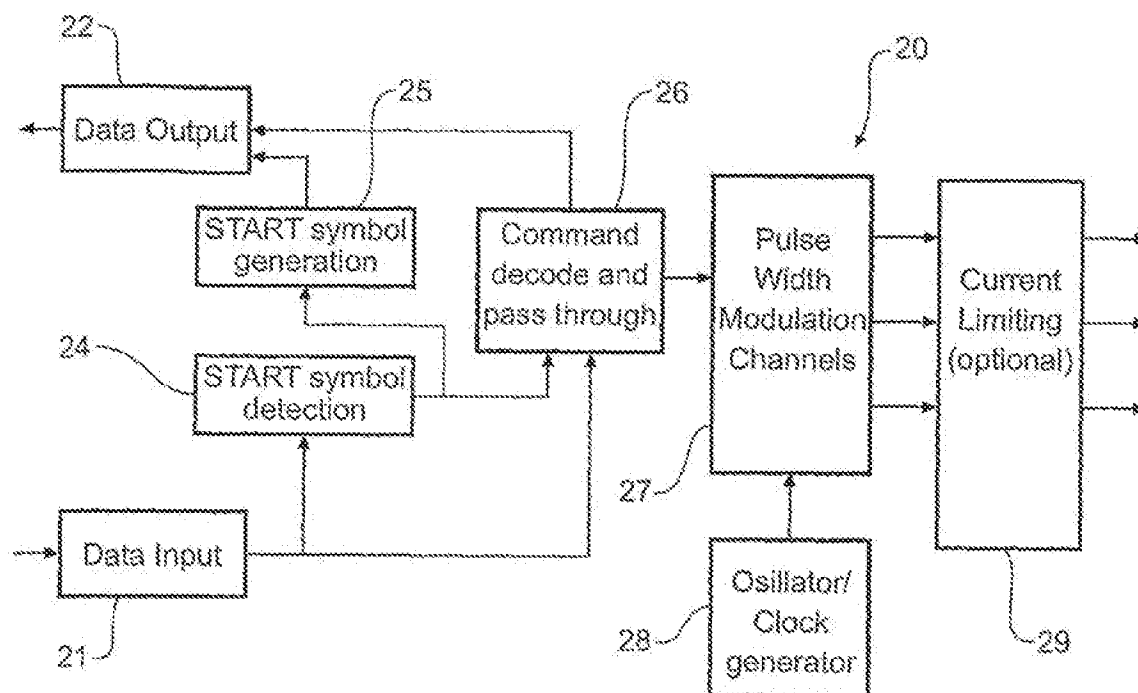
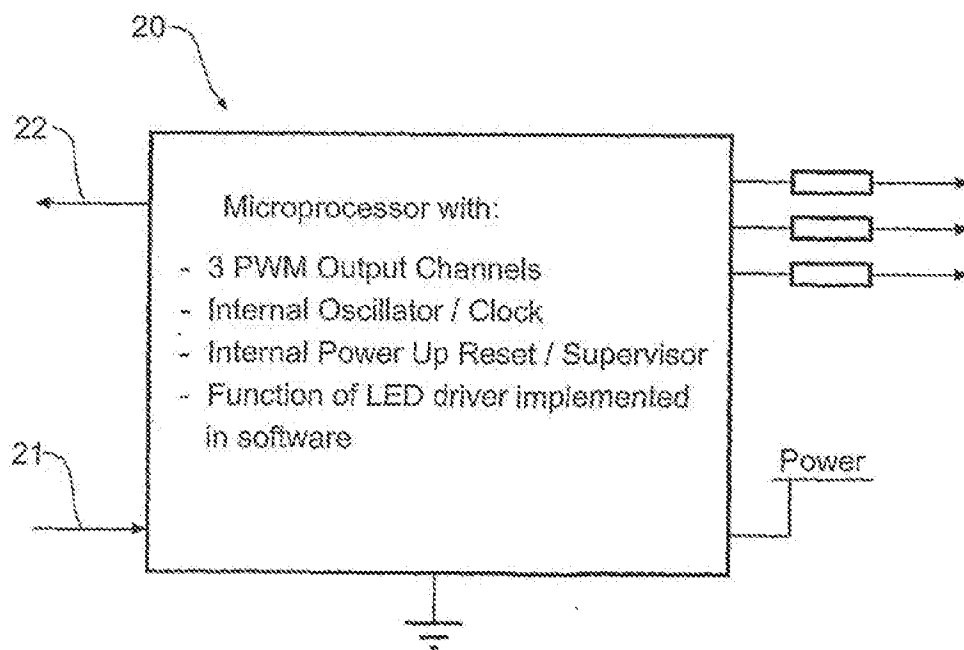
Prior Art

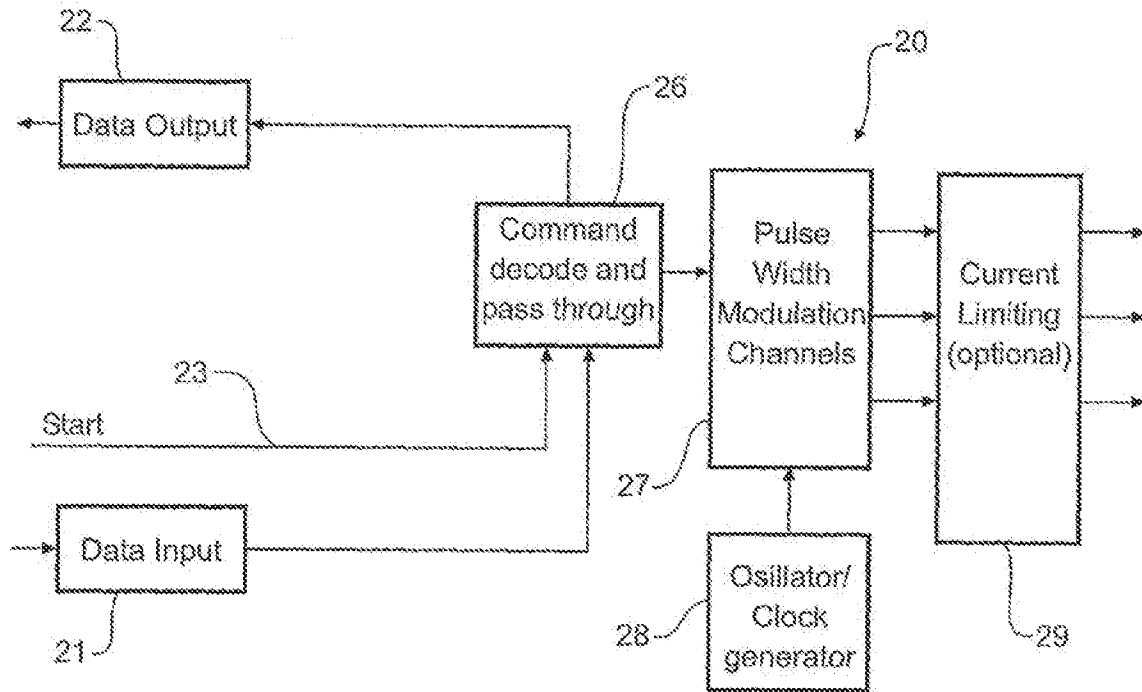
**Figure 2**

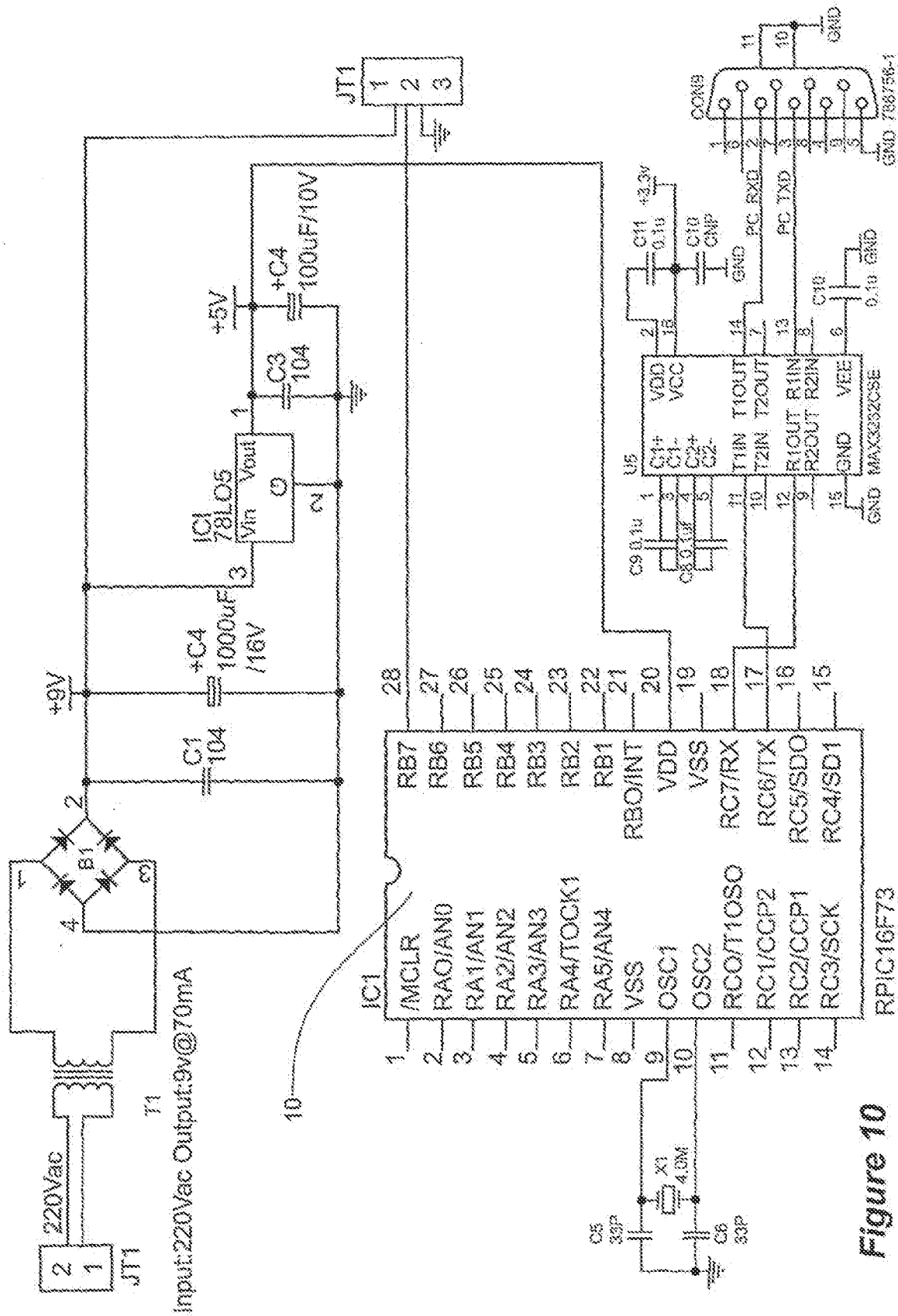
**Figure 3****Figure 4**

**Figure 5**

**Figure 6**

**Figure 7****Figure 8**

**Figure 9**



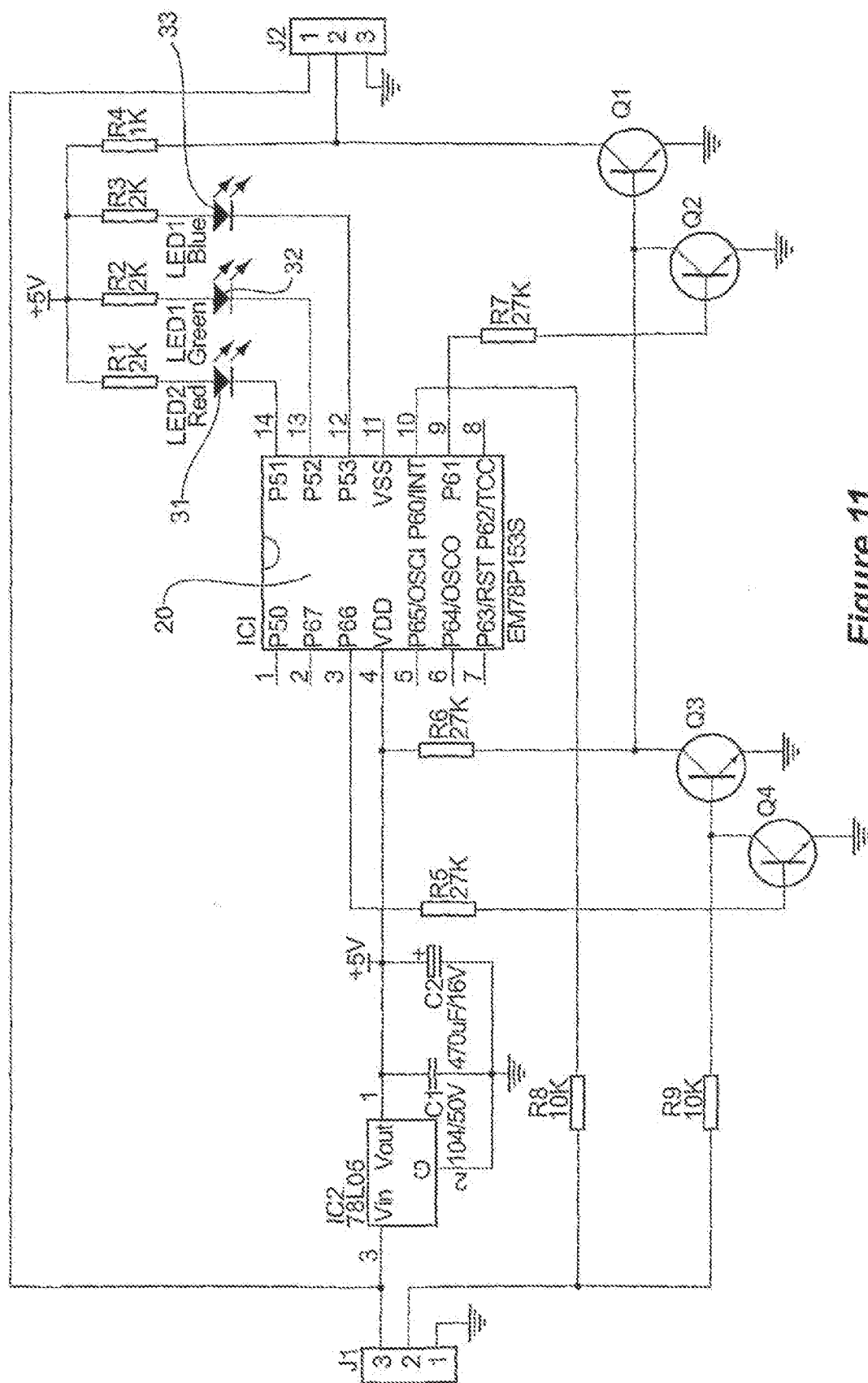


Figure 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/AU2007/001697

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H05B 37/02 (2006.01)

G09G 3/14 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPAT: led control, driver, packets and similar terms

USPTO: controlling led, packets

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0257007 A1 (LYS et al.) 23 December 2004 Page 1 Para [0005]-Page 8 Para [0111]	1-15
A	US 2003/0057887 A1 (DOWLING et al.) 27 March 2003 Abstract	1-15



Further documents are listed in the continuation of Box C



See patent family annex

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"G" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

07 January 2008

Date of mailing of the international search report

10 JAN 2008

Name and mailing address of the ISA/AU

AUSTRALIAN PATENT OFFICE
PG BOX 200, WODEN ACT 2506, AUSTRALIA
E-mail address: pct@ipaustralia.gov.au
Facsimile No. +61 2 6283 7999

Authorized officer

JUZER KHANBHAI

AUSTRALIAN PATENT OFFICE
(ISO 9001 Quality Certified Service)
Telephone No: (02) 6283 2176

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/AU2007/001697

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member			
US	2004257007	AU	17825/01	AU	19241/99
		AU	41484/02	AU	53129/99
		AU	63473/00	AU	70018/01
		AU	77185/01	AU	77308/00
		AU	88659/01	AU	91111/01
		AU	2002360721	AU	2003210890
		AU	2003265764	AU	2003268540
		AU	2004200183	AU	2004300444
		AU	2007216901	CA	2302227
		CA	2336184	CA	2466717
		CA	2559718	CA	2579196
		CA	2591205	CN	1809867
		EP	1040398	EP	1090459
		EP	1195740	EP	1224843
		EP	1234140	EP	1287724
		EP	1337784	EP	1340412
		EP	1388276	EP	1393599
		EP	1422975	EP	1428415
		EP	1474633	EP	1501763
		EP	1535495	EP	1610593
		EP	1624728	EP	1687692
		EP	1729615	EP	1731004
		EP	1800034	EP	1831866
		HK	1025416	JP	2004006253
		KR	2006013198	US	6016038
		US	6166496	US	6211626
		US	6340868	US	6459919
		US	6548967	US	6577080
		US	6624597	US	6717376
		US	6774584	US	6777891
		US	6788011	US	6801003
		US	6869204	US	6888322
				AU	39470/02
				AU	59134/01
				AU	73694/01
				AU	85398/01
				AU	92060/98
				AU	2003237827
				AU	2003279157
				AU	2005222987
				CA	2314163
				CA	2552683
				CA	2591133
				EP	1016062
				EP	1172748
				EP	1224845
				EP	1295515
				EP	1356610
				EP	1395975
				EP	1459600
				EP	1502483
				EP	1620843
				EP	1704752
				EP	1754121
				EP	1849152
				KR	2006010875
				US	6150774
				US	6292901
				US	6528954
				US	6608453
				US	6720745
				US	6781329
				US	6806659
				US	6897624

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/AU2007/001697

US	6936978	US	6965205	US	6967448
US	6975079	US	7014336	US	7031920
US	7038398	US	7038399	US	7042172
US	7064498	US	7113541	US	7132785
US	7132804	US	7135824	US	7139617
US	7161311	US	7161313	US	7180252
US	7186003	US	7187141	US	7202613
US	7204622	US	7221104	US	7228190
US	7231060	US	7233115	US	7233831
US	7242152	US	7248239	US	7253566
US	7255457	US	7256554	US	7274160
US	7300192	US	7303300	US	7308296
US	2001028227	US	2002038157	US	2002044066
US	2002047569	US	2002047628	US	2002047646
US	2002048169	US	2002057061	US	2002070688
US	2002074559	US	2002078221	US	2002101197
US	2002101200	US	2002113355	US	2002130627
US	2002152045	US	2002153851	US	2002158583
US	2002163316	US	2002171365	US	2002171377
US	2002171378	US	2002176259	US	2002195975
US	2003011538	US	2003028260	US	2003057884
US	2003057886	US	2003057887	US	2003057890
US	2003076281	US	2003100837	US	2003133292
US	2003137258	US	2003206411	US	2003214259
US	2003222587	US	2004052076	US	2004090191
US	2004090787	US	2004105261	US	2004113568
US	2004130909	US	2004155609	US	2004160199
US	2004178751	US	2004212320	US	2004212321
US	2004212993	US	2004240890	US	2005030744
US	2005035728	US	2005036300	US	2005040774
US	2005041161	US	2005041424	US	2005044617
US	2005047132	US	2005047134	US	2005062440
US	2005063194	US	2005099824	US	2005116667
US	2005151489	US	2005174473	US	2005213352
US	2005213353	US	2005218838	US	2005218870
US	2005219872	US	2005231133	US	2005236998
US	2005248299	US	2005253533	US	2005275626

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/AU2007/001697

US	2005276053	US	2005285547	US	2006002110
US	2006012987	US	2006016960	US	2006022214
US	2006050509	US	2006076908	US	2006098077
US	2006104058	US	2006109649	US	2006152172
US	2006158881	US	2006208667	US	2006221606
US	2006262516	US	2006285325	US	2007047227
US	2007086754	US	2007086912	US	2007115658
US	2007115665	US	2007153514	US	2007188427
US	2007189026	US	2007195526	US	2007206375
US	2007236156	US	2007237284	US	2007258240
WO	0001067	WO	0105195	WO	0124584
WO	0136864	WO	0182657	WO	0199475
WO	0210847	WO	0211497	WO	0212127
WO	0218913	WO	0225842	WO	0240921
WO	0245467	WO	9910867	WO	9931560
WO	02061330	WO	02091805	WO	02098182
WO	02098183	WO	02099780	WO	02101702
WO	03024269	WO	03026358	WO	03055273
WO	03067934	WO	03096761	WO	2004021747
WO	2004023850	WO	2004032572	WO	2004080291
WO	2004094896	WO	2005012997	WO	2005052751
WO	2005060309	WO	2005084339	WO	2005089293
WO	2005089309	WO	2006023149	WO	2006031753
WO	2006069002	WO	2006069117	WO	2006071628

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
26 March 2009 (26.03.2009)

PCT

(10) International Publication Number
WO 2009/039112 A1(51) International Patent Classification:
G05F 1/00 (2006.01)(21) International Application Number:
PCT/US2008/076552(22) International Filing Date:
16 September 2008 (16.09.2008)

(25) Filing Language: English

(26) Publication Language: English

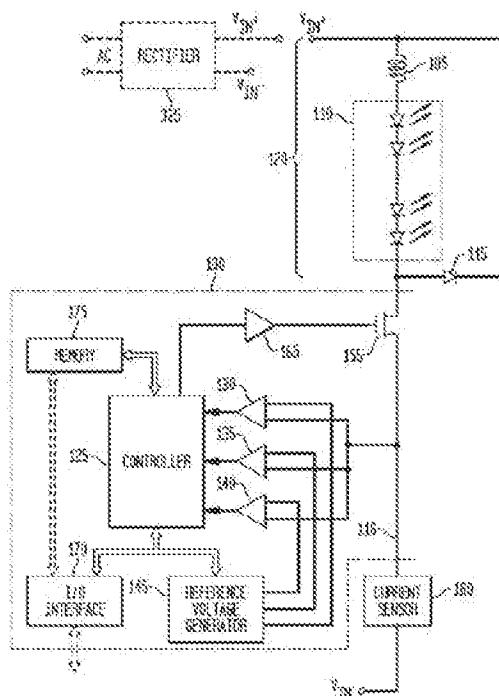
(30) Priority Data:
11/859,680 21 September 2007 (21.09.2007) US(71) Applicant (for all designated States except US):
EXCLARA, INC. [US/US]; Suite 120, 3920 Freedom Circle, Santa Clara, CA 95054 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): ZHOU, Dongsheng
[US/US]; 1355 Kintyre Way, San Jose, CA 95129 (US);
SHTEYNBERG, Anatoly [US/US]; 1191 Quail CreekCircle, San Jose, CA 95120 (US); RODRIGUEZ, Harry
[US/US]; 10525 Foothill Ave., Gilroy, CA 95020 (US);
EASON, Mark [US/US]; 1670 Monte Vista Drive, Bol-
livier, CA 95023 (US); NGUYEN, Lamh [US/US]; 2338
Dundee Drive, Santa Clara, CA 95051 (US).(74) Agent: GAMBURD, Nancy, R.; Gamburd Law Group
LLC, 600 West Jackson Blvd., Suite 625, Chicago, IL
60661 (US).(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AP, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BI, BR, BW, BY, BZ, CA,
CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE,
EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID,
IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LR,
LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW,
MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT,
RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ,
TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM,
ZW.(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,

[Continued on next page])

(54) Title: DIGITAL DRIVER APPARATUS, METHOD AND SYSTEM FOR SOLID STATE LIGHTING

FIG. 1
120

(57) Abstract: An apparatus, method and system are provided for controlling the solid state lighting, such as LEDs. An exemplary apparatus comprises a switch for switching electrical current through the LEDs, a current sensor, a first comparator adapted to determine a switch current first predetermined threshold, a second comparator determining the switch current reached an average level, controller adapted to turn the switch into on/off states, determine a first on time period as a duration between either second predetermined threshold detection or the turning the switch into the on state, and the detection of the predetermined average current level, determine a second on time period as a duration between predetermined average current level and first predetermined threshold detection, determine an on time switch period as proportional to first and second on time periods. Additionally, utilize a difference between first and second on time periods to generate an error signal.



GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LI, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

- 1 -

DIGITAL DRIVER APPARATUS, METHOD AND SYSTEM FOR SOLID STATE LIGHTING

5 FIELD OF THE INVENTION

The present invention in general is related to supplying and controlling power to solid state lighting devices, and more particularly, to digitally controlling the current of solid state lighting devices such as light emitting diodes utilized in lighting and other applications.

10 BACKGROUND OF THE INVENTION

Arrays of light emitting diodes ("LEDs") are utilized for a wide variety of applications, including for general lighting and multicolored lighting. Because emitted light intensity is proportional to the average current through an LED (or through a plurality of LEDs connected in series), adjusting the average current through the LED(s) is one typical method of regulating the intensity or the color of the illumination source. Solid state lighting, such as LEDs, are typically coupled to a converter as a power source.

A step-down (Buck) converter can be controlled either in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). Typically DCM is suitable only for low power processing, while CCM mode is utilized for higher power conversion, such as for high brightness LEDs.

In the prior art, a technique referred to as "current programming mode" ("CPM") is utilized in an attempt to simplify compensator designs for the Buck converter; *see, e.g.*, U.S. Patent Nos. 6,034,517; 4,975,820; 4,672,518; 4,674,020; and 25 4,717,994. Prior art circuits for this CPM mode typically regulate the inductor current in CCM mode around a set point within the Buck converter. This set point is further manipulated by an outer compensating loop. For a Buck converter implemented with CPM mode, the outer compensating loop can be a single pole network.

A CPM implementation, however, cannot simply utilize a controller for 30 a Buck converter, but must also be accompanied with a circuit implementing DCM. One challenge facing this CCM implementation is that the control system needs to transition between DCM and CCM modes in both directions. Many prior art control

- 2 -

systems will oscillate around these two modes, which causes LED current to fluctuate, and which may be visually apparent as flicker, for example. When the outer compensator bandwidth may be low, another problem with this CCM technique is that the LED current may also fluctuate, particularly when the input voltage to the Buck converter contains a high ripple percentage.

Most prior art LED control systems also utilize a "high side sensing" technique, in which the output current of a Buck converter is sensed by a sensing resistor in series with the inductor (see, e.g., U.S. Patent Nos. 6,853,174; 6,166,528; and 5,600,234). With high side sensing, output current can be regulated accurately, and high side sensing can also be utilized with CPM techniques. In order to overcome the various stability problems and other disadvantages mentioned above, the prior art has utilized various controllers to implement hysteretic (or so called "bang-bang") control to regulate this inductor current.

The high side sensing technique works well when the controller integrated circuit ("IC") can tolerate the Buck converter input voltage range. This is typically not the case for an LED driver, however, which involves input voltages which are much higher than what a controller IC is capable of tolerating or specified to tolerate and, accordingly, such a high side sensing technique cannot be utilized with typical controller ICs.

Various techniques for "low side sensing" are also found in the prior art, in which the sense resistor is in between the main converter switching element (MOSFET) and ground, see, e.g., U.S. Patent Nos. 6,580,258 and 5,912,552. The low side sensing technique is usually associated with a control method called "constant off time" (U.S. Patent Nos. 6,580,258 and 5,912,552). Detailed analysis of this constant off time method shows that while it may be suitable for controlling Buck converter output voltage, it exhibits a very large error if it is used for controlling output current, due to converter component and environmental variations (e.g., manufacturing variations, component aging or life span, and environmental conditions such as temperature).

A need remains, therefore, for a control method, apparatus and system, using low side sensing and suitable for IC implementation, that can regulate output current accurately while eliminating those drawbacks caused by existing techniques.

- 3 -

Such an apparatus, method and system should provide a simpler controller compared to CPM techniques, and further provide excellent accuracy and not exhibiting the problems associated with prior art techniques such as CPM technique. Such an apparatus, system and method should also control the intensity (brightness) of light emissions for solid state devices such as LEDs, while simultaneously providing for substantial stability of perceived color emission and control over wavelength shifting, over both a range of intensities and a range of LED junction temperatures. Such an apparatus, system and method should be capable of being implemented with few components, and without requiring extensive feedback systems.

SUMMARY OF THE INVENTION

The exemplary embodiments of the present invention provide numerous advantages for providing power to solid state lighting, such as light emitting diodes. The exemplary embodiments allow for energizing one or more LEDs, using digital control and low side sensing, enabling low voltage IC implementations. The exemplary apparatus and system embodiments may be implemented with either fixed or variable frequency switching, and may be implemented with either AC or DC power sources. As a digital implementation, the exemplary embodiments may also be implemented at a reduced cost. The exemplary embodiments also provide for precise current control, within any selected tolerance levels. In addition, the exemplary embodiments also eliminate the required RC filtering of the prior art.

Further advantages of the exemplary embodiments further provide for controlling the intensity of light emissions for solid state devices such as LEDs, while simultaneously providing for substantial stability of perceived color emission, over both a range of intensities and also over a range of LED junction temperatures. The exemplary embodiments provide digital control, without requiring external compensation. The exemplary embodiments do not utilize significant resistive impedances in the current path to the LEDs, resulting in appreciably lower power losses and increased efficiency. The exemplary current regulator embodiments also utilize comparatively fewer components, providing reduced cost and size, while simultaneously increasing efficiency and enabling longer battery life when used in portable devices, for example.

- 4 -

An exemplary embodiment provides a method of controlling solid state lighting, with the solid state lighting coupled to a switch providing an electrical current path, and the solid state lighting having an electrical current. The exemplary method comprises: turning the switch into an on state; detecting when the electrical current has
5 reached a predetermined average current level; detecting when the electrical current has reached a first predetermined current threshold; determining a first on time period as a duration between detection of a second predetermined current level or turning the switch into the on state and the detection of the predetermined average current level; determining a second on time period as a duration between the detection of the
10 predetermined average current level and the detection of the first predetermined current threshold; and determining an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period. When the on time period has elapsed, the exemplary also provides for turning the switch into an off state. The exemplary method may also provide for detecting when the electrical current has
15 reached the second predetermined current threshold.

The exemplary embodiments may operate in a fixed or variable frequency switching mode. For the fixed frequency switching, subsequent to turning the switch into the off state, when a fixed time period has elapsed from having turned the switch into the on state, the exemplary method again turns the switch into an on
20 state and repeats the detection and determination steps. For this exemplary embodiment, the method also provides for generating an error signal as a difference between the second on time period and the first on time period, and adjusting the on time period proportionally to the error signal.

For variable frequency switching, when a current off time period has elapsed, the exemplary method provides for determining the current off time period of the switch as a function of the first on time period and the second on time period, and more particularly, determining the current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period. In an exemplary embodiment, the current off time period of the switch may be determined
30 as:

- 5 -

$T_{OFF}(K+1) \approx \frac{2 \cdot T_{ON2}(K) \cdot T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$, in which $T_{OFF}(K+1)$ is the current off time

period, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period. In another exemplary embodiment, the current off time period of the switch may be determined as:

$$5 \quad T_{OFF}(K+1) \approx \frac{(T_{ON1}(K)_A + T_{ON2}(K)) \cdot T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}, \text{ in which } T_{OFF}(K+1) \text{ is the current off}$$

time period, $T_{ON1}(K)_A$ is a previous first on time period determined using the detection of the second predetermined current level, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period.

In another exemplary embodiment, the current off time period of the switch may be
 10 determined as a function of a current first on time period, a previous second on time period, and a previous off time period, or as a function of a current first on time period, a previous first on time period, a previous second on time period, and a previous off time period.

In another exemplary embodiment, the method includes adjusting the
 15 current off time period to provide that the first on time period is substantially equal to the second on time period. In addition, the exemplary method also provides for decreasing the current off time period proportionally to a driving gate rising edge time period, or decreasing the on time period proportionally to a driving gate falling edge time period and a comparator falling edge time period. In another variation, the
 20 exemplary method may include adjusting the second on time period proportionally to a driving gate falling edge time period, or decreasing the second on time period proportionally to a driving gate falling edge time period and a comparator falling edge time period.

The exemplary method also provides for determining a blanking time
 25 interval following turning the switch into the on state. During the blanking time interval, the exemplary method provides for ignoring the detection of the second predetermined current threshold, the detection of the predetermined average current level, or the detection of the first predetermined current threshold. The blanking time interval may be determined as proportional to a gate rising edge time period and a

- 6 -

transient current time period, or as proportional to a gate rising edge time period and detection of the predetermined average current level, for example.

In another exemplary embodiment, the exemplary method includes adjusting a brightness level of the solid state lighting by using at least two different and
5 opposing electrical biasing techniques. In addition, the method of adjusting a brightness level of the solid state lighting may include using a hysteresis of at least two electrical current amplitude levels and at least two electrical current duty cycle ratios.

In an exemplary embodiment, the solid state lighting comprises at least one light emitting diode which has a comparatively high voltage node and a
10 comparatively low voltage node, and wherein the detection of the second predetermined current threshold, the detection of the predetermined average current level, and the detection of the first predetermined current threshold occur at the comparatively low voltage node.

In another exemplary embodiment, the solid state lighting comprises a
15 plurality of arrays of a plurality of series-connected light emitting diodes, and each array of the plurality of arrays further coupled to a corresponding switch providing an electrical current path. The exemplary method may also include separately determining a corresponding first on time period, a corresponding second on time period, and a corresponding on time period as substantially proportional to the sum of the
20 corresponding first on time period and the corresponding second on time period for each array of the plurality of arrays; when the corresponding on time period has elapsed, separately turning the corresponding switch into an off state; and separately determining a corresponding off time period for each array of the plurality of arrays. In addition, the exemplary method may also include interleaving the corresponding on
25 time periods of the corresponding switches of the plurality of arrays, such as by successively switching electrical current to each array of the plurality of arrays for the corresponding on time period.

Another exemplary embodiment provides an apparatus for controlling
solid state lighting, with the apparatus comprising: a switch couplable to the solid state
30 lighting; a first comparator adapted to determine when a switch electrical current has reached a first predetermined current threshold; a second comparator adapted to determine when the switch electrical current has reached a predetermined average

- 7 -

current level; and a controller coupled to the first comparator and to the second comparator. In an exemplary embodiment, the controller is adapted to turn the switch into an on state and an off state, to determine a first on time period as a duration between either a detection of a second predetermined current threshold or the turning
5 the switch into the on state, and the detection of the predetermined average current level; to determine a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; and to determine an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period. The
10 controller is further adapted to perform the methodology discussed above.

In an exemplary embodiment, the apparatus also includes a gate driver circuit coupled between the controller and the switch, and wherein the controller is adapted to turn the switch on and to turn the switch off by generating a corresponding signal to the gate driver circuit. The exemplary apparatus may also include a third
15 comparator adapted to determine when the electrical current has reached the second predetermined current threshold; a reference voltage generator adapted to provide reference voltages respectively corresponding to the first and second predetermined current thresholds and to the predetermined average current level; an input-output interface coupled to the controller and adapted to receive an input control signal; and a
20 current sensor coupled to the first and second comparators and to the switch. An exemplary current sensor is embodied as a resistive circuit element.

When the solid state lighting comprises a plurality of arrays of a plurality of series-connected light emitting diodes, with each array of the plurality of arrays is further coupled to a corresponding switch, the controller is further adapted to
25 turn each corresponding switch into an on state and an off state; to separately determine a corresponding first on time period, a corresponding second on time period, and a corresponding on time period as substantially proportional to the sum of the corresponding first on time period and the corresponding second on time period for each array of the plurality of arrays; when the corresponding on time period has
30 elapsed, to separately turn the corresponding switch into an off state; to separately determine a corresponding off time period for each array of the plurality of arrays; and to interleave the corresponding on time periods of the corresponding switches of the

- 8 -

plurality of arrays, such as by successively turn into an on state each corresponding switch for each array of the plurality of arrays for the corresponding on time period.

The exemplary embodiments also provide a solid state lighting system, the system couplable to a power source, with the system comprising: a plurality of
5 arrays of series-connected light emitting diodes; a plurality of switches, a corresponding switch of the plurality of switches coupled to each the array of the plurality of arrays of light emitting diodes; at least one corresponding first comparator adapted to determine when a corresponding switch electrical current has reached a corresponding first predetermined current threshold; at least one corresponding second
10 comparator adapted to determine when the corresponding switch electrical current has reached a corresponding predetermined average current level; and at least one controller coupled to the corresponding first comparator and to the corresponding second comparator, the controller adapted to turn the corresponding switch into an on state and an off state, to determine a corresponding first on time period as a duration
15 between either a detection of a corresponding second predetermined current threshold or the turning the corresponding switch into the on state, and the detection of the corresponding predetermined average current level; to determine a corresponding second on time period as a duration between the detection of the corresponding predetermined average current level and the detection of the corresponding first
20 predetermined current threshold; and to determine a corresponding on time period of the corresponding switch as substantially proportional to a sum of the corresponding first on time period and the corresponding second on time period. The exemplary controller is also adapted to separately perform the methodology of the invention for each array, including the interleaving and the other features discussed above and below.

25 In addition, in the exemplary system, the exemplary apparatus may be coupled to a DC-DC power converter receiving a DC input voltage or coupled to AC-DC power converter receiving a rectified AC input voltage. When the power source provides a rectified AC input voltage, an electrical current through a corresponding switch is substantially zero when the rectified AC input voltage is below a selected or
30 predetermined threshold. In addition, when the power source provides a rectified AC input voltage, the at least one controller is in an off state when the rectified AC input voltage is below a selected or predetermined threshold.

- 9 -

Another exemplary embodiment includes an apparatus for controlling solid state lighting, with the apparatus comprising: a switch couplable to the solid state lighting; a current sensor coupled to the switch; a first comparator adapted to determine when a switch electrical current has reached a first predetermined current threshold; a
5 second comparator adapted to determine when the switch electrical current has reached a predetermined average current level; a third comparator adapted to determine when the switch electrical current has reached a second predetermined current threshold; a reference voltage generator coupled to the first, second and third comparators and adapted to provide reference voltages respectively corresponding to the first
10 predetermined current threshold, the second predetermined current threshold; and to the predetermined average current level; an input-output interface adapted to receive an input control signal; and a controller coupled to the first, second and third comparators and to the input-output interface, the controller adapted to turn the switch into an on state and an off state, to determine a first on time period as a duration between either
15 the detection of a second predetermined current threshold or the turning the switch into the on state, and the detection of the predetermined average current level; to determine a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; to determine an on time period of the switch as substantially proportional to a sum of the
20 first on time period and the second on time period; to turn the switch into an off state when the on time period has elapsed; and to determine a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period.

Numerous other advantages and features of the present invention will
25 become readily apparent from the following detailed description of the invention and the embodiments thereof, from the claims and from the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention will be
30 more readily appreciated upon reference to the following disclosure when considered in conjunction with the accompanying drawings, wherein like reference numerals are used to identify identical components in the various views, and wherein reference numerals

- 10 -

with alphabetic characters are utilized to identify additional types, instantiations or variations of a selected component embodiment in the various views, in which:

Figure (or "FIG.") 1 is a block and circuit diagram of an exemplary first system embodiment and first apparatus embodiment in accordance with the teachings
5 of the present invention.

Figure (or "FIG.") 2, divided into FIGs. 2A and 2B, are graphical diagrams illustrating a first exemplary current waveform through the solid state lighting and through a switch, respectively, in accordance with the teachings of the present invention.

10 Figure (or "FIG.") 3 is a graphical diagram illustrating an exemplary current waveform of a solid state lighting current overshoot, in accordance with the teachings of the present invention.

Figure (or "FIG.") 4 is a graphical diagram illustrating an exemplary current waveform of a solid state lighting current undershoot, in accordance with the
15 teachings of the present invention.

Figure (or "FIG.") 5 is a graphical diagram of an inrush current and a blanking time interval in accordance with the teachings of the present invention.

Figure (or "FIG.") 6 is a graphical diagram illustrating combined pulse width modulation ("PWM") and amplitude modulation for brightness adjustment in
20 accordance with the teachings of the invention.

Figure (or "FIG.") 7 is a graphical diagram illustrating hysteresis between two amplitude levels and duty cycle ratios for brightness adjustment in accordance with the teachings of the invention.

Figure (or "FIG.") 8 is a block and circuit diagram of an exemplary
25 second system embodiment and second apparatus embodiment in accordance with the teachings of the present invention.

Figure (or "FIG.") 9 is a graphical diagrams illustrating a second exemplary current waveform through the solid state lighting and a rectified AC current in accordance with the teachings of the present invention.

30 Figure (or "FIG.") 10 is a block and circuit diagram of an exemplary third system embodiment in accordance with the teachings of the present invention.

- 11 -

Figure (or "FIG.") 11 is a timing diagram illustrating exemplary multiphase switching of the exemplary third system embodiment in accordance with the teachings of the present invention.

Figure (or "FIG.") 12 is a flow diagram of an exemplary method
5 embodiment in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

While the present invention is susceptible of embodiment in many different forms, there are shown in the drawings and will be described herein in detail
10 specific exemplary embodiments thereof, with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention and is not intended to limit the invention to the specific embodiments illustrated. In this respect, before explaining at least one embodiment consistent with the present invention in detail, it is to be understood that the invention is not limited in its
15 application to the details of construction and to the arrangements of components set forth above and below, illustrated in the drawings, or as described in the examples. Methods and apparatuses consistent with the present invention are capable of other embodiments and of being practiced and carried out in various ways. Also, it is to be understood that the phraseology and terminology employed herein, as well as the
20 abstract included below, are for the purposes of description and should not be regarded as limiting.

As mentioned above, exemplary embodiments of the present invention provide numerous advantages for providing power to solid state lighting, such as light emitting diodes. The exemplary embodiments allow for energizing one or more LEDs,
25 using digital control and low side sensing, enabling low voltage IC implementations. The exemplary apparatus and system embodiments may be implemented with either fixed or variable frequency switching, and may be implemented with either AC or DC power sources. As a digital implementation, the exemplary embodiments may also be implemented at a reduced cost. The exemplary embodiments also provide for precise
30 current control, within any selected tolerance levels. In addition, the exemplary embodiments also eliminate the required RC filtering of the prior art. Further advantages are discussed below.

- 12 -

Figure 1 is a block and circuit diagram of an exemplary first system 150 embodiment and first apparatus 100 embodiment in accordance with the teachings of the present invention, for a single channel of LEDs 110. As illustrated in Figure 1, the system 150 comprises an apparatus 100, a converter 120 with an array of LEDs 110 (as an exemplary type of solid state lighting), and a current sensor 160 (illustrated in Figure 8 as implemented using a resistor 160_A). The illustrated configuration for the converter 120 is a Buck converter, although many other configurations and types of converters may be utilized equivalently, requiring only the capability for "low side" (node 116) current sensing, *i.e.*, current sensor 160 is on the comparatively low side (*e.g.*, at node 116) of the power converter 120, as described in greater detail below. The converter 120 comprises an inductor 105 and a diode 115, with the inductor 105 having a series connection with the LEDs 110. The switch 155 may be considered part of the apparatus 100 or part of the converter 120. As known in the art, other components may also be included within the converter 120, and are also within the scope of the present invention.

The apparatus 100, also referred to as a "digital LED driver", comprises a controller 125, a plurality of comparators 130, 135, 140, and a reference voltage generator 145. The comparators 130, 135, 140 and reference voltage generator 145 may be implemented as known or becomes known in the electronic arts. Optionally, the apparatus 100 may also include an input-output ("I/O") interface 170, to receive (and/or transmit) various signals, such as on, off, brightness (dimming) information, or other control information (such as from a building control system), and may communicate using any protocol, as described below. The apparatus 100 also may include a memory 175, such as to store settings, values, and other parameters which may be used by the controller 125, and which also may have a connection to the I/O interface 170, for input or modification of such parameters. Various implementations of the controller 125 (and other controller 225 embodiments), the I/O interface 170, and the memory 175 are described in greater detail below. A switch 155, typically implemented as a field effect transistor ("FET") or any other type of transistor or switching device, may be considered to be part of either the apparatus 100, the converter 120, or the system 150, and is controlled by the controller 125, typically through an optional gate driver (buffer) 165. The current sensor 160 also may be

- 13 -

considered to be part of either the apparatus 100 or the system 150. Those of skill in the art will recognize that the current sensor 160 may be implemented in innumerable ways, in addition to the illustrated resistor (Figure 8), and any and all of which are considered equivalent and within the scope of the invention. Not separately illustrated in Figure 1 are the typical power (V_{DD} and/or V_{IN}), ground, and clock (oscillator) inputs and connections for the apparatus 100. In addition, either terminal illustrated as V_{IN}^+ or V_{IN}^- may also be a ground (GND) connection (e.g., V_{IN}^+ and GND, or GND and V_{IN}^-). Also as illustrated, V_{IN}^+ and V_{IN}^- may be a DC voltage or a rectified AC (AC line voltage), using an optional rectifier 325. Exemplary current waveforms for an AC implementation are illustrated and discussed below with reference to Figure 9.

As mentioned above, the apparatus 100 implements "low-side" sensing, such that voltages are detected on the "low" side of LEDs 110, compared to prior art "high-side" sensing of inductor 105 (or LED 110) current. Accordingly, the apparatus 100 is not required to tolerate high voltages which would be necessary with high-side sensing. The apparatus 100 operates by detecting various LED 110 current levels when the switch 155 is on and conducting, and by the controller 125 calculating and predicting optimal switch 155 "on time" durations (" T_{ON} ") (divided into first and second portions) and switch 155 "off time" durations (" T_{OFF} "). By controlling the on and off durations of the switch 155, the controller 125 thereby regulates the current through the LEDs 110, with current increasing during the on time, and decreasing during the off time (and flowing through diode 115, rather than the switch 155), as illustrated in Figure 2A. In addition, for these first system and apparatus embodiments, because the combined duration (arithmetic sum) of the on (T_{ON}) and off (T_{OFF}) times for the LEDs 110 is not constant, but is variable, the system 150 has a variable switching frequency (a constant switching frequency is discussed below with reference to Figure 8). The LED 110 current levels are detected as corresponding voltage levels across the current sensor 160 during the on time, and compared by the plurality of comparators 130, 135, 140, to corresponding reference voltages generated by reference voltage generator 145. When the switch 155 is off and not conducting, however, it should be noted that no current flow through or otherwise will be available to the current sensor 160 (switch 155 current falls to zero during T_{OFF} , as illustrated in Figure 2B), and as a consequence, the comparators 130, 135, 140, will not have corresponding

- 14 -

voltage input and will therefore have a low (binary zero) output. Described another way, during the off time of the switch 155, the comparators 130, 135, 140 are not providing any (valid) information concerning the LED 110 current levels.

In accordance with the present invention, the controller 125 will
5 determine various "on" times of the switch 155 to provide a selected or predetermined average current level through the LEDs 110, which current is further less than a selected or predetermined first, high threshold level and greater than a selected or predetermined second, low threshold level, thereby regulating average current through the LEDs 110 with a predetermined current ripple level. A first comparator 130 is
10 utilized to detect the first, high threshold ("HT") level, typically as a voltage across the current sensor 160, by comparing the voltage level across the current sensor 160 with a first reference voltage level provided by the reference voltage generator 145. A second comparator 135 is utilized to detect the second, low threshold ("LT") level, by comparing the voltage level across the current sensor 160 with a second reference
15 voltage level provided by the reference voltage generator 145, and a third comparator 140 is utilized to detect the third, average level, by comparing the voltage level across the current sensor 160 with a third (e.g., average ("AV")) reference voltage level provided by the reference voltage generator 145. Based upon those detected levels, the controller 125 will determine the accurate (and optimal) on time durations for the
20 switch 155. Using those switch 155 on time durations, and a current "off" time duration (which at initial start up may be a default value), the controller 125 will calculate a next off time duration. Quite rapidly and within very few on and off cycles of the switch 155, the controller 125 will cause the on and off durations of the switch 155 to converge to accurate (and optimal) values, and further, to provide any
25 corrections within very few clock cycles, such as due to potentially fluctuating input voltage levels (V_{IN}^{+} and/or V_{IN}^{-}).

Figure 2, divided into FIGS. 2A and 2B, are graphical diagrams illustrating a first exemplary current waveform through the solid state lighting (LEDs 110) (and being equal to the current through the inductor 105) and through the switch
30 155, respectively, in accordance with the teachings of the present invention. As illustrated in Figure 2A, during initial start up, the switch 155 is on ($T_{ON1}(1)$, interval 214), and the current through the LEDs 110 will increase (180). During this time

- 15 -

period, as the current increases and the voltage across the current sensor 160 increases, the voltage level across the current sensor 160 will be compared by the comparators 130, 135, 140. As the various threshold levels are reached, the comparators 130, 135, 140 will provide corresponding signals to the controller 125, and the controller 125, in turn, is adapted to determine the corresponding time intervals (durations) for the current to increase, for example, either from when the switch 155 has been turned on to the third, average current level (signal from the third comparator 140) ($T_{ON1}(K)$), or from the second, low threshold (signal from second comparator 135) to the third, average current level (also a signal from the third comparator 140) ($T_{ON1}(K)_A$), and then from the third, average current level to the first, high threshold level (T_{ON2}) (signal from the first comparator 130). Upon reaching the first, high threshold, the first comparator 130 will provide a corresponding signal to the controller 125, which will then turn off the switch 155, typically via the gate driver 165, and the current through the LEDs 110 will begin to decrease (181). During initial start up ($T_{ON1}(1)$), the $T_{ON1}(1)$ interval is not utilized (e.g., insufficiently accurate, due to the start up time), and a default off time is implemented ($T_{OFF}(1)$), such that following the default interval, the switch 155 will be turned on again (187).

In accordance with the exemplary embodiments, the on time of the switch 155 is divided into two intervals, $T_{ON1}(K)$ and $T_{ON2}(K)$, indexed for each switching cycle "K" of the switch 155, with consecutive cycles referred to as "K" and "K+1", with $T_{ON1}(K)$ being the time interval commencing with turning on the switch 155 and ending with the LED 110 current reaching the third, average current level (I_{AV}), and with $T_{ON2}(K)$ being the time interval commencing with the current having reached the third, average current level (I_{AV}) and ending with the LED 110 current reaching the first, high threshold current level (I_{HT}). In addition, to accommodate various input (V_{IN}) and output (V_O) voltage levels, another T_{ON1} time interval is utilized, illustrated in Figure 2A as $T_{ON1}(K)_A$ (177) and $T_{ON1}(K+1)_A$ (198), which is the time interval commencing with the LED 110 current reaching the second, low threshold current level (I_{LT}) and ending with the LED 110 current reaching the third, average current level (I_{AV}). The $T_{ON1}(K)_A$ and $T_{ON1}(K+1)_A$ time periods are utilized for the non-linear rising of the inductor 105 current, illustrated as curves 183, 186 in Figure 2A. The alternative first on time, $T_{ON1}(K)_A$, from the second, low threshold (I_{LT}) to the

- 16 -

third, average current level (I_{AV}), also may be utilized generally when valid second, low threshold (I_{LT}) information is obtainable (depending upon whether the low threshold has already been reached when the blanking time interval has elapsed, as discussed below). Also in accordance with the exemplary embodiments, as the apparatus 100 has
5 a few cycles of operation, the time at which the switch 155 is turned on will be at about the second, low threshold current level (I_{LT}).

When the switch 155 is turned on again (187), depending on the input (V_{IN}) and output (V_O) voltage levels, the increase in current through LEDs 110 may be comparatively linear (182, 185), typically for the input voltage V_{IN} being significantly
10 greater than the output voltage V_O , or may be nonlinear (183, 186), typically for the input voltage V_{IN} being comparatively close in value to the output voltage V_O . The exemplary embodiments of the present invention provide current control for and regardless of either the linear or the nonlinear situation. As the current increases, based upon the input from the comparators 130, 135, 140, the controller 125 will determine
15 the time intervals (durations) $T_{ON1}(K)$ and $T_{ON2}(K)$. When the first, high threshold has been reached, the controller 125 will again turn off the switch 155 (189, 199), and will calculate the next off duration for the switch 155 (to be utilized currently), such that the LED current level is generally kept above the second, low threshold (188), and does not have undershoot (or has insignificant undershoot) (as may have occurred previously
20 (187) during initial start up, as illustrated).

The controller 125, generally, will determine a current off time of the switch 155 as a function of the on time and the previous off time. More specifically, the controller 125 will determine a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period.
25 Even more specifically, the controller 125 will determine a current off time period of the switch as a function of a current first on time period, a previous second on time period, and a previous off time period. In another alternative, and also more specifically, the controller 125 will determine a current off time period of the switch as a function of a current first on time period, a previous first on time period, a previous
30 second on time period, and a previous off time period. In addition, current and previous should be understood in their relative sense, which are also pair-wise equivalent to the relative terms next and current (respectively, as a pair), so that any

- 17 -

reference or claim to current and previous should be understood to mean and include next and current, respectively.

During any given cycle, at the point of turning off the switch 155 (189, 199), the current values (or parameters) for $T_{ON1}(K+1)$, $T_{ON2}(K+1)$ and the previous values (or parameters) for $T_{ON1}(K)$, $T_{ON2}(K)$, and $T_{OFF}(K)$ are known. In accordance with the exemplary embodiments, the next off time ($T_{OFF}(K+1)$) which will be utilized in the current cycle ($K+1$) will be calculated or otherwise determined by the controller 125 using the previous off time ($T_{OFF}(K)$), and the various on times, such as the previous second on time $T_{ON2}(K)$ and the current first on time $T_{ON1}(K+1)$, or the previous second on time $T_{ON2}(K)$, the current first on time $T_{ON1}(K+1)$ and the previous first on time $T_{ON1}(K)$. More specifically, in accordance with the invention, the switch 155 off time ($T_{OFF}(K)$) is adjusted such that the first and second on times are generally about or substantially equal to each other, $T_{ON1}(K) \approx T_{ON2}(K)$, which then provides the desired current regulation, maintaining the average current level (I_{AV}), while generally maintaining the current below the first, high threshold (I_{HT}) and above the second, low threshold (I_{LT}), depending upon the allowed or tolerated current ripple level.

When V_{IN} is significantly higher than V_O , the inductor 105 current rise slope generally is substantially linear (182, 185). We may assume that the converter 120 input and output voltages V_{IN} and V_O do not vary between consecutive cycles. For a Buck converter, the current rising slope is defined by (Equation 1):

$$\text{current_rising_slope} = \frac{V_{IN} - V_O}{L},$$

such that the current rising slope does not vary appreciably between consecutive cycles.

Since comparators 130, 135, 140 are comparing against fixed thresholds I_{HT} , I_{LT} and I_{AV} , T_{ON2} should remain the same across the consecutive cycles, i.e., (Equation 2):

$$T_{ON2}(K+1) = T_{ON2}(K),$$

such that any calculation using a current second on time $T_{ON2}(K+1)$ is equivalent to and includes using a previous second on time period $T_{ON2}(K)$, and vice versa. By the time $T_{ON1}(K+1)$ elapses, the controller 125 knows $T_{OFF}(K)$, $T_{ON2}(K)$ and $T_{ON1}(K+1)$. Since $T_{OFF}(K)$, $T_{ON1}(K+1)$, and $T_{ON2}(K+1)$ (which equals $T_{ON2}(K)$ from Equation 2) share the same peak (I_{HT}) and valley (I_{LT}) currents, then (Equation 3)

- 18 -

$$\begin{aligned}\Delta I &= \frac{V_o}{L} T_{OFF}(K) = \frac{V_o - V_o}{L} \{T_{ON1}(K+1) + T_{ON2}(K+1)\} \\ &\approx \frac{V_o - V_o}{L} \{T_{ON1}(K+1) + T_{ON2}(K)\}\end{aligned}$$

Because an average current of I_{AV} and equal halves (time intervals) for of peak (I_{PT}) and valley (I_{LT}) currents are desired, then (Equation 4):

$$T_{ON1}(K+1) = T_{ON2}(K).$$

- 5 The desired $T_{OFF}(K+1)$ can be formulated as (Equation 5):

$$\Delta I_{desired} = \frac{V_o}{L} T_{OFF}(K+1) = \frac{V_o - V_o}{L} \{2 \cdot T_{ON2}(K)\}.$$

Dividing Equation 5 by Equation 3 (i.e., Equation 5 over Equation 3) to remove a dependence over V_{IN} , V_O and L , yields (Equation 6):

$$\frac{T_{OFF}(K+1)}{T_{OFF}(K)} = \frac{2 \cdot T_{ON2}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}.$$

- 10 Thus, for an exemplary embodiment, the next $T_{OFF}(K+1)$ should be generated by the controller 125 as (Equation 7):

$$T_{OFF}(K+1) = \frac{2 \cdot T_{ON2}(K) \cdot T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}.$$

- Implementation of Equation 7 requires one multiply, one shift, one addition and one divide operation per converter 120 switching cycle. The performance of the apparatus 100, therefore, is about two switching cycles to converge to its target values or parameters for I_{AV} , I_{PT} , and I_{LT} . In addition, the requirement of one multiply and divide per converter 120 switching cycle can be relaxed if the converter 120 switching frequency is much higher than normal ripple found in V_{IN} and V_O . As mentioned above, however, when the current first on time $T_{ON1}(K+1)_A$ or previous first on time $T_{ON1}(K)_A$ are available (i.e., may be measured after the blanking interval described below), these measurements may be utilized instead of the current first on time $T_{ON1}(K+1)$ or previous first on time $T_{ON1}(K)$.

- When V_{IN} is not much higher than V_O , the rising slope of the inductor 105 current is no longer linear (183, 186 in Figure 2A). Typically, the initial slope during the $T_{ON1}(K)$ interval is steeper than the $T_{ON2}(K)$ interval. Because in this case Equation 7 may yield a much lower valley (I_{LT}) current than the desired average current I_{AV} , Equation 7 can be modified as (Equation 8):

- 19 -

$$T_{OFF}(K+1) = \frac{(T_{ON1}(K)_A + T_{ON2}(K)) * T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}$$

As mentioned above, $T_{ON1}(K)_A$ is the time interval from I_{LT} to I_{AV} , and may be determined along curves 183, 186 or the curves 182, 185. As discussed in greater detail below, however, because the controller 125 of various exemplary embodiments does not utilize any output of comparators 130, 135, 140 during a "blanking" interval following turning on the switch 155, it is possible that the output of the second comparator 135 (I_{LT}) may be already high when the blanking interval has elapsed and, in which case, Equation 7 is utilized to calculate $T_{OFF}(K+1)$ as well, rather than Equation 8.

Referring again to Figure 1, the thresholds (peak (I_{HT}), valley (I_{LT}) and average (I_{AV}) currents used by comparators 130, 135, 140 are set (predetermined) within the apparatus 100, such as by inputting values using the I/O interface 170, and storing those values as parameters or values in memory 175. For example, for an allowable or selectable 20% ripple in LED 110 current regulation, peak (I_{HT}), average (I_{AV}) and valley (I_{LT}) currents can be set to be apart by 10% intervals. Typical values for peak (I_{HT}), average (I_{AV}) and valley (I_{LT}) currents are represented by corresponding voltages across the current sensor 160, e.g., at around 0.3 Volts (and can be lower when using an IC). The current sensor 160 is selected based upon the desired application; for example, when implemented as a resistor, a value is selected to pass a desired average current.

For even more fine-grained current regulation, the exemplary embodiments of the invention also account for rise and fall delays of the various switching elements, such as the rising and falling time delays of the switch 155, the gate driver 165, and the comparators 130, 135, 140, with any propagation delays included within any such rising and falling time delays. Figure 3 is a graphical diagram illustrating an exemplary current waveform of a solid state lighting current overshoot, in accordance with the teachings of the present invention, illustrating in greater detail section 215 from Figure 2. Figure 4 is a graphical diagram illustrating an exemplary current waveform of a solid state lighting current undershoot, in accordance with the teachings of the present invention, illustrating in greater detail section 210 from Figure 2.

- 20 -

Referring to Figure 3, when the LED 110 current reaches the first, high threshold (I_{HT}) at time t_1 , there is a rise time associated with the first (peak) comparator 130 (interval 201), such that the controller 125 does not receive the corresponding information until time t_2 . At time t_2 , the controller 125 will turn off the gate driver 165 to turn off the switch 155, resulting in a fall time associated with the gate driver 165 and the switch 155 (interval 202), such that the switch 155 has stopped conducting at time t_3 . As the current through the LEDs 110 (and switch 155) decreases, there is another fall time associated with the first (peak) comparator 130 (interval 203), such that the controller 125 does not receive the corresponding information until time t_4 .
Because of these rising and falling time delays, unless the delays are accounted for, there can be an overshoot of the LED 110 current, with the LED 110 current being higher than the selected first, high threshold. Accordingly, the controller 125 receives the corresponding comparator (130) rising and falling edge information at t_2 and t_4 .

Similarly, referring to Figure 4, when the LED 110 current decreases to the second, low threshold (I_{LT}) during an off time period, no current is flowing through the switch 155 (Figure 2B), so no information is available to the controller 125. At time t_5 , the end of the off time period, the controller 125 will turn on the gate driver 165 to turn on the switch 155, resulting in a rise time associated with the gate driver 165 and the switch 155 (interval 205), such that the switch 155 will start conducting at time t_7 . As the current through the LEDs 110 (and switch 155) increases to the low threshold (I_{LT}), there is a rise time associated with the second (valley) comparator 135 (interval 206), such that the controller 125 does not receive the corresponding information until time t_6 . Because of these rising and falling time delays, unless the delays are accounted for, there can be an undershoot of the LED 110 current, with the LED 110 current being lower than the selected second, low threshold. Accordingly, the controller 125 receives the corresponding comparator (135) rising edge information at t_6 .

The exemplary embodiments of the invention may be implemented to account the various delays associated with the rising and falling times of the first (peak) comparator 130, the gate driver 165 and the switch 155, and the second (valley) comparator 135. By making the rising and falling delay times equal (symmetrical) for each comparator 130, 135, then the time interval during which the controller 125

- 21 -

receives the corresponding comparator (130, 135) rising and falling edge information (e.g., at t_2 and t_4) is equal to the actual overshoot time interval (of t_1 to t_3).

Accordingly, the overshoot time may be measured from the first comparator 130 rising edge (t_1) (also coincident with the falling edge of the off command/signal to the gate driver 165) to the first (peak) comparator 130 falling edge (t_3), resulting in (Equation 9):

$$T_{\text{overshoot}} \approx T_{p_gate_drv_fall} + T_{pk_comp_fall}$$

Accordingly, for finer-grained control, the overshoot time is subtracted from T_{ON2} by the controller 125, such that the actual LED 110 current would barely reach the first, high threshold I_{HT} .

Because the second comparator 135 is not receiving comparable information during T_{OFF} , a different approach may be utilized, as an option, for determining an undershoot time interval or duration. Accordingly, by also making the first comparator 130 and second comparator 135 to be similar, such that each effectively having the same rising and falling time intervals as the other (symmetrical), then the undershoot time may be considered to be substantially equal or otherwise comparable to the overshoot time. Assuming such symmetry between comparators 130, 135, results in (Equation 10):

$$T_{\text{undershoot}} \approx T_{\text{overshoot}}$$

such that the interval from t_3 to t_4 in turn also would be equal to the undershoot time interval (of t_1 to t_3). In this instance, the undershoot time is subtracted from T_{OFF} by the controller 125, such that the actual LED 110 current would barely decrease to the second, low threshold I_{LT} . In both overshoot and undershoot circumstances, the measurements of these intervals may be completed during the initial system 150 start up, and treated as constants during subsequent switching cycles or, alternatively, the overshoot and undershoot time intervals may be calibrated whenever the corresponding first (peak) comparator 130 has valid information. In addition, because the undershoot and overshoot time periods may be symmetrical, when the gate driver 165 and switch 155 have symmetrical rise and fall times, and when the various comparators have symmetrical rise and fall times, then the measurement of one (overshoot) also may be used for the other (undershoot).

- 22 -

In another variation, when the second comparator 135 does not provide valid information during an on time interval (e.g., the second comparator 135 has already indicated that the low threshold of current has been reached when the blanking time has elapsed), then the relevant undershoot time may be considered to be only the rise time of the gate driver 165 and switch 155 which, given the symmetrical rise and fall times, would be equal to the fall time of the gate driver 165 and switch 155. This may be determined as described below, or as another alternative, the overshoot time (which also includes first comparator 130 rise or fall time) may be utilized as a sufficiently accurate estimation.

In addition, in exemplary embodiments, depending upon selected tolerance levels, the undershoot compensation may be omitted, as lower current levels are not harmful to the LEDs 110, and if the undershoot is not large, may not be visually apparent. Alternatively, the first, high threshold I_{HT} and the second, low threshold I_{LT} may also be adjusted in advance, to provide tighter regulation, such as spacing them apart by 5% of 7.5% intervals, rather than 10% intervals, for example.

Both of the overshoot and undershoot controls, however, generally should be implemented such that both the first (peak) comparator 130 and the second (valley) comparator 135 periodically trip, to avoid the LED 110 current from deviating down or up without notice. Accordingly, in accordance with the exemplary embodiments, the controller 125 will periodically allow the LED 110 current to rise and fall sufficiently to trip the first (peak) comparator 130 and the second (valley) comparator 135, respectively.

Conversely, if the specification for LED 110 current ripple allow current overshoot (e.g., allowing the LED 110 current envelope to follow V_{IN} ripple), then the overshoot and undershoot may be made symmetrical as well, such as by increasing the off time T_{OFF} by the undershoot (or symmetrical overshoot) interval. By doing so, the LED 110 average current would remain constant.

Figure 5 is a graphical diagram of an inrush current through the switch 155 when it is turned on and a "blanking" time interval in accordance with the teachings of the present invention. In the prior art, such an inrush (transient) current would be filtered using an additional capacitor and resistor (RC filter) in parallel with the current sensor 160; in the exemplary embodiments, the use of such an RC filter is

- 23 -

not required, and a blanking time interval is utilized instead, as mentioned above and as described below. Initially the controller 125 issues a command to the gate driver 165 (and thereby switch 155) to turn on, at time t_{10} . After the gate driver 165 and switch 155 rise time (interval 211) (combined as "Tp_gate_drive_rise" time), the switch 155 current exhibits a transient spike, referred to as an "inrush", starting at time t_{11} , typically caused by its terminal capacitance and the reverse recovery of diode 115, which lasts for interval 212 (through time t_{13}). This inrush current through the switch 155 may be higher than the average current (I_{AV}) and potentially even higher than the first, high threshold (I_{TH}), causing their respective comparators 140, 130 to trip (and provide corresponding logic high signals to the controller 125). In accordance with the exemplary embodiments, the controller 125 disregards this information by establishing or setting a "blanking" time interval (216) ("Tblank"), during which the outputs of the comparators 130, 135, and 140 are ignored. The blanking time interval commences when the controller 125 generates the command to turn on the gate driver 165 (and switch 155) (t_{10}), and extends until the transient inrush current has settled (t_{13}), resulting in (Equation 10): $T_{blank} > T_{P_gate_drive_rise} + T_{inrush}$.

The transient, inrush time interval (212) is generally a function of switch 155 terminal capacitance, diode 115 reverse recovery charge, and the sense resistance value (when current sensor 160 is implemented as a resistor). If the inrush current is higher than the average current (I_{AV}), it is possible for the controller 125 to determine the inrush time and adjust the blanking time appropriately.

Ideally, Equation 4 provides that T_{ON1} should be equal to T_{ON2} . The controller 125, however, as mentioned above, should turn on the gate driver 165 and switch 155 earlier by an amount equal to their combined rise time (Tp_gate_drive_rise time). In a system where the gate driver 165 is designed such that its rise time is close to the overshoot time (e.g., the gate driver 165 and switch 155 have symmetrical rising and falling times and comparator delay time is not significant), then the overshoot time can be utilized to decrease T_{OFF} .

Yet another method of determining the rise time of the gate driver 165 and switch 155 (Tp_gate_drive_rise) is through the third, average current (I_{AV}) comparator 140. Although the moment when the switch 155 inrush current trips the third, average current (I_{AV}) comparator 140 should not be used as an indicator of the actual inductor

- 24 -

105 average current, it can be used to indicate the time when the switch 155 actually starts to conduct. Accordingly, the rise time of the gate driver 165 and switch 155 and the rise time of the third, average current (I_{AV}) comparator 140 ("Tav_comp_rise") ($Tp_gate_drive_rise + Tav_comp_rise$) can be measured from the time the controller
5 125 issues the turn on command until the third, average current (I_{AV}) comparator 140 trips. Then the third, average current (I_{AV}) comparator 140 rise time (Tav_comp_rise) is subtracted from the measurement in order to obtain the rise time of the gate driver 165 and switch 155 ($Tp_gate_drive_rise$). In an exemplary embodiment, the third, average current (I_{AV}) comparator 140 rise time (Tav_comp_rise) is a known design
10 parameter or is significantly smaller than the rise and fall times of the gate driver 165 and switch 155 ($Tp_gate_drive_rise$ and $Tp_gate_drive_fall$).

The rise times of the various comparators 130, 135 and 140 may also affect the measurements of T_{ON1} and T_{ON2} . As mentioned above, T_{ON1} is the interval from the time the current reaches the low threshold current level (I_{LT}), as determined by
15 the second (I_{LT}) comparator 135 (or from the time when the switch 155 actually conducts) to the time the current reaches the average current level (I_{AV}), as determined by the third, average current (I_{AV}) comparator 140. T_{ON2} is the time interval from the average current level to the first, high (peak) current level, namely, as determined by the third, average current (I_{AV}) comparator 140 and the first (I_{HT}) comparator 130,
20 respectively. In the exemplary embodiments, therefore, the first (I_{HT}) comparator 130 and the third, average current (I_{AV}) comparator 140 are designed or implemented to have the same or substantially similar delay times (i.e., $T_{av_comp_rise} = T_{ht_comp_rise}$). With the rise times of the first (I_{HT}) comparator 130 and the third, average current (I_{AV}) comparator 140 being substantially the same, then T_{ON2} can be measured by the interval
25 from when the controller 125 receives the rising edge of the third, average current (I_{AV}) comparator 140 to when the controller 125 receives the rising edge of the first (I_{HT}) comparator 130. It should be noted, as mentioned above, that this measurement does not apply during the blanking time interval, or when the controller 125 does not receive a valid rising edge of the first (I_{HT}) comparator 130 (e.g., due to overshoot
30 compensation, in which case T_{ON2} may be adjusted occasionally in order for the first (I_{HT}) comparator 130 to trip and provide information at these various intervals).

- 25 -

As indicated above, T_{ON1} may be measured from the interval beginning with the controller 125 receiving the rising edge of the second (I_{LT}) comparator 135 (when available (*i.e.* when the rising edge did not occur during the blanking interval)) until the controller 125 receives the rising edge of the third, average current (I_{AV}) comparator 140, or beginning with the controller 125 generating the turn on command for the gate driver 165 and switch 155) until the controller 125 receives the rising edge of the third, average current (I_{AV}) comparator 140 (T_{ON1} measured). For the former case, given the symmetry of the comparators, no additional compensation is needed for determining T_{ON1} measured. In the latter case however, when the rising edge of the second (I_{LT}) comparator 135 does not provide valid information (during the blanking interval, or due to undershoot compensation), then for this measurement, the rise time of the gate driver 165 and switch 155 should then be subtracted, to provide the actual value of T_{ON1} ($T_{ON1} \approx T_{ON1 \text{ measured}} - T_{AV_comp_rise}$). T_{ON1} may also be measured using the transient current spike (inrush current), if the inrush current is sufficiently high to trip the third, average current (I_{AV}) comparator 140, indicating a start of the conduction by the switch 155. T_{ON1} is then the interval between the controller 125 receiving the first rising edge of the third, average current (I_{AV}) comparator 140 due to the inrush current and receiving the second rising edge of the third, average current (I_{AV}) comparator 140 (after the transient has settled). Knowing both T_{ON1} and T_{ON2} , the controller 125 may then determine T_{OFF} .

In the event that during initial start up, the third, average current (I_{AV}) comparator 140 stays high after the transient current spike (inrush current) has settled, indicating that the current is already too high, there is no need to measure T_{ON1} and T_{ON2} . Rather, T_{OFF} is extended, to allow current to decrease, with valid measurements for T_{ON1} and T_{ON2} obtainable in the next cycle.

Figure 6 is a graphical diagram illustrating combined pulse width modulation ("PWM") and amplitude modulation for brightness adjustment in accordance with the teachings of the invention. The exemplary embodiments implement brightness control (dimming) using a combination of at least two different electrical biasing techniques across the LEDs 110, such as PWM and amplitude modulation (or constant current regulation ("CCR")). A first electrical biasing technique, by itself, will tend to produce a first wavelength shift (higher or lower) in

- 26 -

response to a change in intensity, such as in response to a change in duty cycle for PWM, while a second electrical biasing technique, by itself, will tend to produce a second, opposite or opposing wavelength shift (lower or higher, respectively) in response to the change in intensity, such as in response to a change in amplitude for analog regulation or CCR. In accordance with the exemplary embodiments, any resulting wavelength shift is minimized or maintained within a selected tolerance level by utilizing at least two different and opposing electrical biasing techniques (such that the opposing wavelength shifts effectively "cancel" each other). Additional discussion of that methodology is in one or more related patent applications. To decrease brightness, for PWM, the duty cycle is decreased (*e.g.*, from D1 to D2), and for amplitude modulation (CCR), the amplitude of the LED current is decreased (*e.g.*, from ILED1 to ILED2), as illustrated in Figure 6. In accordance with the exemplary embodiments, the controller 125 implements dimming by using both PWM and amplitude modulation, either alternating them in successive modulation intervals or combining them during the same modulation interval, with the latter illustrated in Figure 6. This inventive combination of at least two different electrical biasing techniques having opposing effects on wavelength emission allows for both regulating the intensity of the emitted light while controlling the wavelength emission shift, from either or both the LED response to intensity variation (dimming technique) and due to p-n junction temperatures changes, and also to produce dynamic lighting and color effects.

Figure 7 is a graphical diagram illustrating hysteresis between two amplitude levels (ILED1, ILED2) and duty cycle ratios (D1L, D2L, D1H, D2H) for brightness adjustment in accordance with the teachings of the invention. In order to prevent jitter, a hysteresis is implemented as illustrated in Figure 7. The operating points (ILED1, D1L) have the same brightness (color) to (ILED2, D2L), and the same brightness applies to (ILED1, D1H) and (ILED2, D2H). When D1 comes from high brightness down to D1L, ILED1 is changed to ILED2 and D2L is used instead. When D2 comes up from low brightness to D2H, ILED2 is switched to ILED1 and D1H is used.

Figure 8 is a block and circuit diagram of an exemplary second system 250 embodiment and second apparatus 200 embodiment, for fixed frequency switching

- 27 -

operation, in accordance with the teachings of the present invention. The second system 250 and second apparatus 200 differ from the first system 150 and first apparatus 100 insofar as: (1) the combined duration (arithmetic sum) of the on (T_{ON}) and off (T_{OFF}) times for the LEDs 110 is constant, not variable, such that the second system 250 has a fixed or constant switching frequency (rather than the variable switching frequency previously discussed); and (2) the controller 225 is adapted to provide current control when the commencement or initiation of the on time of the switch 155 is at a fixed, regular frequency. In addition, as an illustrated alternative, the controller 225 is coupled directly to the switch 155, rather than via a gate driver (165). It should be understood, however, that the second system 250 and second apparatus 200 may also include such a gate driver circuit 165, such as a buffer.

For the second system 250 and second apparatus 200, the controller 225 includes an error generator 260, a compensator 255, and a control block 251 for determining the respective on (T_{ON}) and off (T_{OFF}) durations for the switch 155. In this embodiment, the controller 225 also provides that T_{ON1} is substantially equal to T_{ON2} , with the error generator 260 generating an error signal substantially equal or proportional to the difference between T_{ON1} and T_{ON2} (error = $T_{ON2} - T_{ON1}$, error $\approx T_{ON2} - T_{ON1}$, or error $\approx c \cdot (T_{ON2} - T_{ON1})$, where "c" is a constant of proportionality). The error signal is provided to the compensator 255, which then adjusts the on time (T_{ON}) of the switch 155, which is then correspondingly switched on and off by the control block 251. It should be noted, because the switch 155 is switched on at a fixed frequency, adjusting the on time (T_{ON}) of the switch 155 automatically changes the off time (T_{OFF}) of the switch 155 (e.g., increasing the on time T_{ON} decreases the off time T_{OFF} , and vice versa).

Figure 9 is a graphical diagrams illustrating a second exemplary current waveform through the solid state lighting and a rectified AC current in accordance with the teachings of the present invention. Such a rectified AC current 301 (or voltage) may be provided by a rectifier 325 to provide a voltage input V_{IN} (illustrated as V_{IN}^+ and V_{IN}^-) having a DC average value, from an AC line voltage (AC mains), for example, and may be utilized with either the first or second system 150, 250 and first or second apparatus 100, 200, and also may be utilized with the third system 350 discussed below. When the rectified AC current 301 is below a selected (or

- 28 -

predetermined) threshold, illustrated as intervals 303, there is generally no switch 155 current, and the apparatus 100, 200 will typically be off during these AC zero crossing intervals. As illustrated, the switch 155 is turned on, above the selected (or predetermined) threshold, the LED 110 current 302 will initially track the rectified AC current 301, increasing to the second, low threshold (I_{LT}), reaching the average current level (I_{AV}) and then the first, high threshold (I_{HT}), followed by turning the switch 155 off for its calculated duration, and followed by successive on and off cycles, as described above, using the measurements and calculations described above for T_{ON1} , T_{ON2} , and T_{OFF} , or using the error signal (e.g., $error \approx T_{ON2} - T_{ON1}$) described above, for either variable or fixed frequency embodiments. Such an apparatus and system can be built directly into an Edison socket, and further, can provide power factor correction ("PFC"). In order to achieve PFC operation, the controller 125 or compensator 255 is comparatively slow with respect to a V_{IN} ripple frequency of 120Hz (or 100Hz). For example and without limitation, for each half of the AC cycle, the T_{ON} determined and outputted by the compensator 255 can be regarded as a constant, and is adjusted during successive half-cycles.

It should be noted that the first system 150, first apparatus 100, the second system 250 and second apparatus 200, and their versions including an AC rectifier 325, may be scaled or extended to multiple channels of LEDs 110. In one such implementation, the first or second apparatus 100, 200 is instantiated in its entirety for each separate channel of LEDs 110.

In another such implementation, discussed below with reference to Figure 10, the comparators 130, 135, 140 are instantiated separately for each separate or independent channel of LEDs 110, such that the LED 110 current through each channel is separately monitored. In this scaled embodiment, the controller 125, 225 then has multiple outputs, one to each to each gate driver 165 (which in turn is coupled to a corresponding switch 155 for each separate or independent channel of LEDs 110). The controller 125, 225 separately computes the various on (T_{ON1} and T_{ON2}) durations for the switch 155, and for apparatus 100, the controller 125 also computes the off (T_{OFF}) duration, for each separate (or independent) channel of LEDs 110, and separately controls each gate driver 165 to each switch 155 for each separate channel of

- 29 -

LEDs 110 to provide the current regulation through each such channel of LEDs 110 as discussed above and as discussed below.

Figure 10 is a block and circuit diagram of an exemplary third system 350 embodiment, for multichannel operation, in accordance with the teachings of the present invention. As mentioned above, the various first and second apparatus 100, 200 may be extended to control current through a plurality of separate arrays 310 (also referred to equivalently as channels or strings) of LEDs 110, illustrated as array 310₁ having LEDs 110₁, array 310₂ having LEDs 110₂, through array 310_n having LEDs 110_n. Each such array or channel 310 includes at least one LED 110 or a plurality of LEDs 110 connected in series. In contrast with the prior art, the plurality of LEDs 110 of each array are not required to be identical or from the same manufacturing bin; instead, because of the separate control and regulation provided by the exemplary embodiments, there may be significant variation among the LEDs 110, for a considerable cost savings.

With the separate current control for each LED array 310, the regulated current can be matched to each separate LED array 310. Accordingly, various LED arrays 310 are not subject to excessive current levels, that would be caused in the prior art systems from some LED arrays having a higher impedance and drawing less current than expected. As a consequence, the exemplary third system 350 enables increased durability, improved system lifetime, decreased heat generated (also enabling a corresponding decrease in the size of heat sinks for the LEDs 110), a decrease in the number of LEDs 110 required for the same optical output, and overall increased system efficiency and efficacy.

As illustrated for the third system 350, each array 310 has a corresponding switch 155, illustrated as switch 155₁, switch 155₂, through switch 155_n, which are controlled by respective gate driver circuits (buffers) 165 (illustrated collectively, for ease of discussion), under the control of at least one controller 125, 225. The comparators 130, 135, 140 are instantiated separately for each separate or independent array or channel 310 of LEDs 110, such that the LED 110 current through each array (channel) 310 (via corresponding current sensors 160₁, 160₂, through 160_n) is separately monitored and separately controlled, as described above for the first and second systems 100, 200. At least one reference voltage generator 145 provides the

- 30 -

corresponding reference voltages (corresponding to the first (high) threshold, average, and second (low) threshold) for each current through each separate array 310. It should be noted that the various average, first and second threshold currents may be either the same or different across the various arrays 310, such that any selected array 310 may
5 have its own set average and threshold current levels, separate from the average and threshold currents of the other arrays 310.

In this scaled, third system 350 embodiment, the controller 125, 225 then has multiple outputs, one to each to each gate driver 165, to turn on or off a corresponding switch 155 for each separate array 310 of LEDs 110. The controller
10 125, 225 separately determines the various on (T_{ON1} and T_{ON2}) durations for each corresponding switch 155₁, switch 155₂, through switch 155_n, and for variable frequency operation, the controller 125 also computes the off (T_{OFF}) duration, for each separate (or independent) array 310 of LEDs 110. The controller 125, 225 separately controls each gate driver 165 to each switch 155₁, switch 155₂, through switch 155_n, for
15 each separate array 310 of LEDs 110, to provide separate current regulation through each separate channel of LEDs 110 in accordance with the exemplary embodiments of the invention.

Accordingly, for each separate array 310 of LEDs 110, for variable frequency switching, the controller 125 will determine T_{ON1} and T_{ON2} , and a
20 corresponding T_{OFF} , as previously described above for the first system 150 and first apparatus 100, to provide regulated current control, for each array 310, and for fixed frequency switching, the controller 225 will determine T_{ON1} and T_{ON2} , as previously described above for the second system 250 and second apparatus 200, to provide regulated current control, for each array 310.

While the exemplary third system 350 provides separate control to each
25 LED array 310, such control may be independent, controlling each LED array 310 completely independently of all the other LED arrays 310, or such control may include any type of coordinated, joint or dependent regulation, for any selected lighting or color effect, as may be necessary or desirable for any selected application. In addition, such
30 independent or dependent regulation may be implemented for any type of LEDs 110, such as separate or independent control of red, blue, and green LEDs 110, or coordinated control of such red, blue, and green LEDs 110, such as to produce various

- 31 -

lighting effects having a selected hue, for example. Also for example, lighting effects such as output intensity, color output, color temperature, etc. may be regulated independently or in a coordinated manner for each LED array 310. Importantly, the exemplary third system 350 is capable of providing completely separate and
5 independent current regulation of each LED array 310, with any such independence selectively implemented or not, for example, by the end user of the exemplary third system 350. Also importantly, the exemplary third system 350 is capable of providing any type of coordinated current regulation of each LED array 310, with any such coordination selectively implemented or not, for example, by the end user of the
10 exemplary third system 350.

As an example of one form of coordinated control, in the exemplary third system 350, interleaving of switch 155 on (T_{ON}) durations may be implemented, providing a multiphase control, such that only selected arrays 310 are switched on and are conducting current during a given time interval. Figure 11 is a timing diagram
15 illustrating exemplary multiphase switching of the exemplary third system embodiment, for "n" arrays 310 of LEDs 110, in accordance with the teachings of the present invention. As illustrated, each T_{ON} "pulse" 370 represents the on duration (T_{ON}) of a switch 155 of an array 310; while illustrated as a square wave, it may have any waveform, and merely represents a signal from the controller 125, 225 to turn on
20 (and keep on for the selected on time duration) the corresponding switch 155 (via a corresponding gate driver 165). Also as illustrated, the timing of each such T_{ON} pulse 370 differs across the "n" arrays, with T_{ON} pulses 370₁, 370_{n-3}, and 370_{n-2} occurring during time interval t_A for LED arrays 310₁, 310_{n-3}, and 310_{n-2}, respectively; T_{ON} pulses 370₁, 370₂, 370_{n-2} and 370_{n-1} occurring during time interval t_B for LED arrays 310₁,
25 310₂, 310_{n-2} and 310_{n-1}, respectively; T_{ON} pulses 370₂, 370₃, 370_{n-1} and 370_n occurring during time interval t_C for LED arrays 310₂, 310₃, 310_{n-1} and 310_n, respectively; and so on. The various on durations may be selected to be separate (e.g., T_{ON} pulses 370₁ and 370₄) or to overlap (e.g., T_{ON} pulses 370₁ and 370₂), as may be necessary or desirable.

Because of this interleaving, multiphase control, not all LED arrays 310
30 are receiving current at the same time. This enables a much smoother AC input current, which minimizes any requirement on input electromagnetic interference (EMI)

- 32 -

filter size, further enabling a reduction in the input filter capacitor size, and reduced component costs. It is also expected to work well with a thyristor-type dimming.

It should be noted that the controllers 125, 225 may be implemented the same, and configured or otherwise programmed for operation as part of any of the systems 150, 250, and 350.

Figure 12 is a flow diagram of an exemplary method embodiment, in accordance with the teachings of the present invention, for controlling the energizing of solid state lighting, such as LEDs 110, and provides a useful summary. As discussed above, the solid state lighting is coupled to a switch (155) providing an electrical current path (e.g., through current sensor 160), and with the solid state lighting having an electrical current. The method begins, start step 400, with turning the switch 155 into an on state, step 405. The method then detects when the electrical current has reached a predetermined average current level, step 410, and detects when the electrical current has reached a first predetermined (e.g., high) current threshold, step 415. When available (*i.e.*, not during the blanking interval), and prior to detecting the average current level, step 410 may also include detecting when the electrical current has reached a second predetermined (e.g., low) current threshold. The method then determines a first on time period (T_{ON1}) as a duration between the detection of the second predetermined (e.g., low) current threshold (or turning the switch into the on state) and the detection of the predetermined average current level, step 420, and determines a second on time period (T_{ON2}) as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold, step 425. An on time period (T_{ON}) of the switch is then determined as substantially equal or proportional to the sum of the first on time period and the second on time period ($T_{ON} \approx T_{ON1} + T_{ON2}$), step 430. When the on time period has elapsed, the switch is turned off, step 435. For a first embodiment, the exemplary method also determines a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period (Equations 7 and 8), step 440. When the method continues, step 445, then following expiration of the off time period, step 450, the method returns to step 405 to turn the switch on, and the method iterates. When the method does not continue in step 445, the method may end, return step 455.

- 33 -

Not separately illustrated, the method may also include: adjusting the current off time period to provide that the first on time period is substantially equal to the second on time period ($T_{ON1} \approx T_{ON2}$); or decreasing the current off time period proportionally to a driving gate rising edge time period. In addition, the determination
5 of the current off time period of the switch may be a further function, more specifically, of previous first and second on times and one or more current first on times.

The exemplary method may also provide for determining a blanking time interval following turning the switch into the on state, and ignoring the detection of the second predetermined current threshold, the detection of the predetermined
10 average current level or the detection of the first predetermined current threshold during the blanking time interval. The blanking time interval may be determined as proportional to a gate rising edge time period and a transient current time period, or as proportional to a gate rising edge time period and detection of the predetermined average current level.

The exemplary method may also provide for adjusting a brightness level of the solid state lighting by using at least two electrical biasing techniques, and for
15 example, adjusting a brightness level of the solid state lighting by using a hysteresis of at least two electrical current amplitude levels and at least two electrical current duty cycle ratios.

The method may also provide for current overshoot protection, by
20 adjusting the second on time period proportionally to a driving gate falling edge time period, and more particularly, such as by decreasing the second on time period proportionally to a driving gate falling edge time period and a comparator falling edge time period.

The method may also provide for current undershoot protection by
25 adjusting the first on time period proportionally to a driving gate rising edge time period, such as by increasing the first on time period proportionally to a driving gate rising edge time period. Such undershoot protection may be provided equivalently by decreasing the current off time period proportionally to a driving gate rising edge time
30 period, such as by decreasing the current off time period proportionally to a driving gate rising edge time period.

- 34 -

In another exemplary embodiment, the method may include generating an error signal as a difference between the second on time period and the first on time period, and then adjusting the on time period proportionally to the error signal.

Referring to Figures 1, 8 and 10, as mentioned above, the I/O interface
5 170 is utilized for input/output communication, providing appropriate connection to a relevant channel, network or bus; for example, and the interface 170 may provide additional functionality, such as impedance matching, drivers and other functions for a wireline interface, may provide demodulation and analog to digital conversion for a wireless interface, and may provide a physical interface for the memory 175 and
10 controller 125, 225 with other devices. In general, the interface 170 is used to receive and transmit data, depending upon the selected embodiment, such as to receive intensity level selection data, temperature data, and to provide or transmit control signals for current regulation (for controlling an LED driver), and other pertinent information. For example and without limitation, the interface 170 may implement
15 communication protocols such as DMX 512, DALI, I²C, SPI, etc.

Also as mentioned above, a controller 125, 225 (or, equivalently, a "processor") may be any type of controller or processor, and may be embodied as one or more controllers 125, 225, adapted to perform the functionality discussed herein. As the term controller or processor is used herein, a controller 125, 225 may include use of
20 a single integrated circuit ("IC"), or may include use of a plurality of integrated circuits or other components connected, arranged or grouped together, such as controllers, microprocessors, digital signal processors ("DSPs"), parallel processors, multiple core processors, custom ICs, application specific integrated circuits ("ASICs"), field programmable gate arrays ("FPGAs"), adaptive computing ICs, associated memory
25 (such as RAM, DRAM and ROM), and other ICs and components. As a consequence, as used herein, the term controller (or processor) should be understood to equivalently mean and include a single IC, or arrangement of custom ICs, ASICs, processors, microprocessors, controllers, FPGAs, adaptive computing ICs, or some other grouping of integrated circuits which perform the functions discussed below, with associated
30 memory, such as microprocessor memory or additional RAM, DRAM, SDRAM, SRAM, MRAM, ROM, FLASH, EPROM or E²PROM. A controller (or processor) (such as controller 125, 225), with its associated memory, may be adapted or

- 35 -

configured (via programming, FPGA interconnection, or hard-wiring) to perform the methodology of the invention, as discussed above and below. For example, the methodology may be programmed and stored, in a controller 125, 225 with its associated memory (and/or memory 175) and other equivalent components, as a set of
5 program instructions or other code (or equivalent configuration or other program) for subsequent execution when the processor is operative (*i.e.*, powered on and functioning). Equivalently, when the controller 125, 225 may implemented in whole or part as FPGAs, custom ICs and/or ASICs, the FPGAs, custom ICs or ASICs also may be designed, configured and/or hard-wired to implement the methodology of the
10 invention. For example, the controller 125, 225 may be implemented as an arrangement of controllers, microprocessors, DSPs and/or ASICs, collectively referred to as a "controller", which are respectively programmed, designed, adapted or configured to implement the methodology of the invention, in conjunction with a memory 175.

15 The memory 175, which may include a data repository (or database), may be embodied in any number of forms, including within any computer or other machine-readable data storage medium, memory device or other storage or communication device for storage or communication of information, currently known or which becomes available in the future, including, but not limited to, a memory
20 integrated circuit ("IC"), or memory portion of an integrated circuit (such as the resident memory within a controller 125, 225 or processor IC), whether volatile or non-volatile, whether removable or non-removable, including without limitation RAM, FLASH, DRAM, SDRAM, SRAM, MRAM, FeRAM, ROM, EPROM or E²PROM, or any other form of memory device, such as a magnetic hard drive, an optical drive, a
25 magnetic disk or tape drive, a hard disk drive, other machine-readable storage or memory media such as a floppy disk, a CDROM, a CD-RW, digital versatile disk (DVD) or other optical memory, or any other type of memory, storage medium, or data storage apparatus or circuit, which is known or which becomes known, depending upon the selected embodiment. In addition, such computer readable media includes any form
30 of communication media which embodies computer readable instructions, data structures, program modules or other data in a data signal or modulated signal, such as an electromagnetic or optical carrier wave or other transport mechanism, including any

- 36 -

information delivery media, which may encode data or other information in a signal, wired or wirelessly, including electromagnetic, optical, acoustic, RF or infrared signals, and so on. The memory 175 may be adapted to store various look up tables, parameters, coefficients, other information and data, programs or instructions (of the software of the present invention), and other types of tables such as database tables.

As indicated above, the controller 125, 225 is programmed, using software and data structures of the invention, for example, to perform the methodology of the present invention. As a consequence, the system and method of the present invention may be embodied as software which provides such programming or other instructions, such as a set of instructions and/or metadata embodied within a computer readable medium, discussed above. In addition, metadata may also be utilized to define the various data structures of a look up table or a database. Such software may be in the form of source or object code, by way of example and without limitation. Source code further may be compiled into some form of instructions or object code (including assembly language instructions or configuration information). The software, source code or metadata of the present invention may be embodied as any type of code, such as C, C++, SystemC, LISA, XML, Java, Brew, SQL and its variations (e.g., SQL 99 or proprietary versions of SQL), DB2, Oracle, or any other type of programming language which performs the functionality discussed herein, including various hardware definition or hardware modeling languages (e.g., Verilog, VHDL, RTL) and resulting database files (e.g., GDSII). As a consequence, a "construct", "program construct", "software construct" or "software", as used equivalently herein, means and refers to any programming language, of any kind, with any syntax or signatures, which provides or can be interpreted to provide the associated functionality or methodology specified (when instantiated or loaded into a processor or computer and executed, including the controller 125, 225, for example).

The software, metadata, or other source code of the present invention and any resulting bit file (object code, database, or look up table) may be embodied within any tangible storage medium, such as any of the computer or other machine-readable data storage media, as computer-readable instructions, data structures, program modules or other data, such as discussed above with respect to the memory 175, e.g., a floppy disk, a CDROM, a CD-RW, a DVD, a magnetic hard drive, an

- 37 -

optical drive, or any other type of data storage apparatus or medium, as mentioned above.

Numerous advantages of the present invention for providing power to solid state lighting, such as light emitting diodes, are readily apparent. The exemplary
5 embodiments allow for energizing one or more LEDs, using digital control and low side sensing, enabling low voltage IC implementations. The exemplary apparatus and system embodiments may be implemented with either fixed or variable frequency switching, and may be implemented with either AC or DC power sources. As a digital implementation, the exemplary embodiments may also be implemented at a reduced
10 cost. The exemplary embodiments also provide for precise current control, within any selected tolerance levels. In addition, the exemplary embodiments also eliminate the required RC filtering of the prior art.

For changes in brightness levels, a combination of forward biasing techniques are implemented, which allow for both regulating the intensity of the
15 emitted light while controlling the wavelength emission shift, from either or both the LED response to intensity variation (dimming technique) and due to p-n junction temperatures changes. In addition, the exemplary embodiments of the invention also provide for varying intensity while simultaneously reducing the EMI produced by prior art lighting systems, especially because current steps in the pulse modulation are
20 dramatically reduced or eliminated completely. The exemplary LED controllers are also backwards-compatible with legacy LED control systems, frees the legacy host computer for other tasks, and allows such host computers to be utilized for other types of system regulation. The exemplary current regulator embodiments provide digital control, without requiring external compensation. The exemplary current regulator
25 embodiments also utilize comparatively fewer components, providing reduced cost and size, while simultaneously providing increased efficiency and enabling longer battery life when used in portable devices.

Although the invention has been described with respect to specific embodiments thereof, these embodiments are merely illustrative and not restrictive of
30 the invention. In the description herein, numerous specific details are provided, such as examples of electronic components, electronic and structural connections, materials, and structural variations, to provide a thorough understanding of embodiments of the

- 38 -

present invention. One skilled in the relevant art will recognize, however, that an embodiment of the invention can be practiced without one or more of the specific details, or with other apparatus, systems, assemblies, components, materials, parts, etc. In other instances, well-known structures, materials, or operations are not specifically shown or described in detail to avoid obscuring aspects of embodiments of the present invention. In addition, the various Figures are not drawn to scale and should not be regarded as limiting.

Reference throughout this specification to "one embodiment", "an embodiment", or a specific "embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention and not necessarily in all embodiments, and further, are not necessarily referring to the same embodiment. Furthermore, the particular features, structures, or characteristics of any specific embodiment of the present invention may be combined in any suitable manner and in any suitable combination with one or more other embodiments, including the use of selected features without corresponding use of other features. In addition, many modifications may be made to adapt a particular application, situation or material to the essential scope and spirit of the present invention. It is to be understood that other variations and modifications of the embodiments of the present invention described and illustrated herein are possible in light of the teachings herein and are to be considered part of the spirit and scope of the present invention.

It will also be appreciated that one or more of the elements depicted in the Figures can also be implemented in a more separate or integrated manner, or even removed or rendered inoperable in certain cases, as may be useful in accordance with a particular application. Integrally formed combinations of components are also within the scope of the invention, particularly for embodiments in which a separation or combination of discrete components is unclear or indiscernible. In addition, use of the term "coupled" herein, including in its various forms such as "coupling" or "couplable", means and includes any direct or indirect electrical, structural or magnetic coupling, connection or attachment, or adaptation or capability for such a direct or indirect electrical, structural or magnetic coupling, connection or attachment, including

- 39 -

integrally formed components and components which are coupled via or through another component.

As used herein for purposes of the present invention, the term "LED" and its plural form "LEDs" should be understood to include any electroluminescent diode or other type of carrier injection- or junction-based system which is capable of generating radiation in response to an electrical signal, including without limitation, various semiconductor- or carbon-based structures which emit light in response to a current or voltage, light emitting polymers, organic LEDs, and so on, including within the visible spectrum, or other spectra such as ultraviolet or infrared, of any bandwidth, or of any color or color temperature.

Furthermore, any signal arrows in the drawings/Figures should be considered only exemplary, and not limiting, unless otherwise specifically noted. Combinations of components of steps will also be considered within the scope of the present invention, particularly where the ability to separate or combine is unclear or foreseeable. The disjunctive term "or", as used herein and throughout the claims that follow, is generally intended to mean "and/or", having both conjunctive and disjunctive meanings (and is not confined to an "exclusive or" meaning), unless otherwise indicated. As used in the description herein and throughout the claims that follow, "a", "an", and "the" include plural references unless the context clearly dictates otherwise. Also as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

The foregoing description of illustrated embodiments of the present invention, including what is described in the summary or in the abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed herein. From the foregoing, it will be observed that numerous variations, modifications and substitutions are intended and may be effected without departing from the spirit and scope of the novel concept of the invention. It is to be understood that no limitation with respect to the specific methods and apparatus illustrated herein is intended or should be inferred. It is, of course, intended to cover by the appended claims all such modifications as fall within the scope of the claims.

- 40 -

It is claimed:

1. A method of controlling solid state lighting, the solid state lighting coupled to a switch providing an electrical current path, and the solid state lighting having an electrical current, the method comprising:
 - turning the switch into an on state;
 - detecting when the electrical current has reached a predetermined average current level;
 - detecting when the electrical current has reached a first predetermined current threshold;
 - determining a first on time period as a duration between detection of a second predetermined current level or turning the switch into the on state and the detection of the predetermined average current level;
 - determining a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; and
 - determining an on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period.
2. The method of claim 1, further comprising:
 - when the on time period has elapsed, turning the switch into an off state.
3. The method of claim 2, further comprising:
 - subsequent to turning the switch into the off state, when a fixed time period has elapsed from having turned the switch into the on state, again turning the switch into the on state and repeating the detection and determination steps.
4. The method of claim 3, further comprising:
 - generating an error signal as a difference between the second on time period and the first on time period.

- 41 -

5. The method of claim 5, further comprising:
adjusting the on time period proportionally to the error signal.
6. The method of claim 2, further comprising:
when a current off time period has elapsed, turning the switch into the
on state and repeating the detection and determination steps.
7. The method of claim 6, further comprising:
determining the current off time period of the switch as a function of the
first on time period and the second on time period.
8. The method of claim 6, further comprising:
determining the current off time period of the switch as a function of the
first on time period, the second on time period, and a previous off time period.
9. The method of claim 6, further comprising:
determining the current off time period of the switch as:

$$T_{OFF}(K+1) \approx \frac{2 * T_{ON2}(K) * T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)},$$
 in which $T_{OFF}(K+1)$ is the current off time
 period, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time
 period, and $T_{ON1}(K+1)$ is a current first on time period.
10. The method of claim 6, further comprising:
determining the current off time period of the switch as:

$$T_{OFF}(K+1) \approx \frac{(T_{ON1}(K)_A + T_{ON2}(K)) * T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)},$$
 in which $T_{OFF}(K+1)$ is the current off
 time period, $T_{ON1}(K)_A$ is a previous first on time period determined using the detection
 of the second predetermined current level, $T_{ON2}(K)$ is a previous second on time period,
 $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period.

- 42 -

11. The method of claim 6, further comprising:
determining the current off time period of the switch as a function of a
current first on time period, a previous second on time period, and a previous off time
period.
- 5 12. The method of claim 6, further comprising:
determining the current off time period of the switch as a function of a
current first on time period, a previous first on time period, a previous second on time
period, and a previous off time period.
- 10 13. The method of claim 6, further comprising:
adjusting the current off time period to provide that the first on time
period is substantially equal to the second on time period.
- 15 14. The method of claim 6, further comprising:
decreasing the current off time period proportionally to a driving gate
rising edge time period.
- 20 15. The method of claim 1, further comprising:
decreasing the on time period proportionally to a driving gate falling
edge time period and a comparator falling edge time period.
16. The method of claim 1, further comprising:
determining a blanking time interval following turning the switch into
25 the on state.
17. The method of claim 16, further comprising:
ignoring the detection of the second predetermined current threshold, the
detection of the predetermined average current level, or the detection of the first
30 predetermined current threshold during the blanking time interval.

- 43 -

18. The method of claim 16, further comprising:
determining the blanking time interval as proportional to a gate rising
edge time period and a transient current time period.
- 5 19. The method of claim 16, further comprising:
determining the blanking time interval as proportional to a gate rising
edge time period and detection of the predetermined average current level.
20. The method of claim 1, further comprising:
10 adjusting a brightness level of the solid state lighting by using at least
two different and opposing electrical biasing techniques.
21. The method of claim 1, further comprising:
adjusting a brightness level of the solid state lighting by using a
15 hysteresis of at least two electrical current amplitude levels and at least two electrical
current duty cycle ratios.
22. The method of claim 1, further comprising:
adjusting the second on time period proportionally to a driving gate
20 falling edge time period.
23. The method of claim 1, further comprising:
decreasing the second on time period proportionally to a driving gate
falling edge time period and a comparator falling edge time period.
- 25 24. The method of claim 1, further comprising:
detecting when the electrical current has reached the second
predetermined current threshold.
- 30 25. The method of claim 1, wherein the solid state lighting comprises at
least one light emitting diode.

- 44 -

26. The method of claim 25, wherein the at least one light emitting diode is coupled to a power converter, and wherein the electrical current detections occur at a comparatively low side of the power converter.

5 27. The method of claim 1, wherein the solid state lighting comprises a plurality of arrays of a plurality of series-connected light emitting diodes, and each array of the plurality of arrays further coupled to a corresponding switch providing an electrical current path.

10 28. The method of claim 27, further comprising:
separately determining a corresponding first on time period, a corresponding second on time period, and a corresponding on time period as substantially proportional to the sum of the corresponding first on time period and the corresponding second on time period for each array of the plurality of arrays.

15 29. The method of claim 28, further comprising:
when the corresponding on time period has elapsed, separately turning the corresponding switch into the off state.

20 30. The method of claim 29, further comprising:
separately determining a corresponding off time period for each array of the plurality of arrays.

31. The method of claim 29, further comprising:
25 interleaving the corresponding on time periods of the corresponding switches of the plurality of arrays.

32. The method of claim 27, further comprising:
successively switching electrical current to each array of the plurality of
30 arrays for the corresponding on time period.

- 45 -

33. An apparatus for controlling solid state lighting, the apparatus comprising:

a switch couplable to the solid state lighting;

a first comparator adapted to determine when a switch electrical current
5 has reached a first predetermined current threshold;

a second comparator adapted to determine when the switch electrical current has reached a predetermined average current level; and

a controller coupled to the first comparator and to the second comparator; the controller adapted to turn the switch into an on state and an off state, to
10 determine a first on time period as a duration between either a detection of a second predetermined current threshold or the turning the switch into the on state, and the detection of the predetermined average current level; to determine a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; and to determine an
15 on time period of the switch as substantially proportional to a sum of the first on time period and the second on time period.

34. The apparatus of claim 33, wherein the controller is further adapted, when the on time period has elapsed, to turn the switch into an off state.

35. The apparatus of claim 34, wherein the controller is further adapted, subsequent to turning the switch into the off state and when a fixed time period has elapsed from having turned the switch into the on state, to turn the switch into the on state.

36. The apparatus of claim 35, wherein the controller is further adapted to generate an error signal as a difference between the second on time period and the first on time period.

37. The apparatus of claim 36, wherein the controller is further adapted to adjust the on time period proportionally to the error signal.

- 46 -

38. The apparatus of claim 34, wherein the controller is further adapted to determine a current off time period of the switch as a function of the first on time period and the second on time period.

5 39. The apparatus of claim 34, wherein the controller is further adapted to determine a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period.

40. The apparatus of claim 34, wherein the controller is further adapted to
10 determine a current off time period of the switch as:

$$T_{OFF}(K+1) \approx \frac{2 * T_{ON2}(K) * T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)},$$

period, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period.

15 41. The apparatus of claim 34, wherein the controller is further adapted to determine a current off time period of the switch as a function of a current first on time period, a previous second on time period, and a previous off time period.

42. The apparatus of claim 34, wherein the controller is further adapted to
20 determine a current off time period of the switch as a function of a current first on time period, a previous first on time period, a previous second on time period, and a previous off time period.

43. The apparatus of claim 34, wherein the controller is further adapted to
25 adjust a current off time period to provide that the first on time period is substantially equal to the second on time period.

44. The apparatus of claim 33, further comprising:
a gate driver circuit coupled between the controller and the switch, and
30 wherein the controller is adapted to turn the switch on and to turn the switch off by generating a corresponding signal to the gate driver circuit.

- 47 -

45. The apparatus of claim 44, wherein the controller is further adapted to decrease a current off time period proportionally to a rising edge time period of the gate driver circuit.

5

46. The apparatus of claim 44, wherein the controller is further adapted to decrease the on time period proportionally to a falling edge time period of the gate driver circuit and a falling edge time period of the first comparator.

10

47. The apparatus of claim 44, wherein the controller is further adapted to adjust the second on time period proportionally to a falling edge time period of the gate driver circuit.

15

48. The apparatus of claim 44, wherein the controller is further adapted to decrease the second on time period proportionally to a falling edge time period of the gate driver circuit and a falling edge time period of the first comparator.

20

49. The apparatus of claim 44, wherein the controller is further adapted to determine a blanking time interval following turning the switch into the on state.

50. The apparatus of claim 49, further comprising:
a third comparator adapted to determine when the electrical current has reached the second predetermined current threshold.

25

51. The apparatus of claim 50, further comprising:
a current sensor coupled to the first, second and third comparators and to the switch.

30

52. The apparatus of claim 51, wherein the current sensor is embodied as a resistive circuit element.

- 48 -

53. The apparatus of claim 50, wherein the controller is further adapted to determine a current off time period of the switch as:

$$T_{OFF}(K+1) \approx \frac{(T_{ON1}(K)_A + T_{ON2}(K)) \cdot T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)},$$

time period, $T_{ON1}(K)_A$ is a previous first on time period determined using the detection
 5 of the second predetermined current level, $T_{ON2}(K)$ is a previous second on time period, $T_{OFF}(K)$ is a previous off time period, and $T_{ON1}(K+1)$ is a current first on time period.

54. The apparatus of claim 50, wherein the controller is further adapted to ignore the detection of the second predetermined current threshold, the detection of the
 10 predetermined average current level, or the detection of the first predetermined current threshold during the blanking time interval.

55. The apparatus of claim 50, wherein the controller is further adapted to determine the blanking time interval as proportional to a rising edge time period of the
 15 gate driver circuit and a transient current time period.

56. The apparatus of claim 50, wherein the controller is further adapted to determine the blanking time interval as proportional to a rising edge time period of the
 gate driver circuit and detection of the predetermined average current level.

57. The apparatus of claim 33, wherein the controller is further adapted to adjust a brightness level of the solid state lighting by generating control signals to a
 driver circuit for using at least two different and opposing electrical biasing techniques.

58. The apparatus of claim 33, wherein the controller is further adapted to adjust a brightness level of the solid state lighting by generating control signals to a
 driver circuit to use a hysteresis of at least two electrical current amplitude levels and at
 least two electrical current duty cycle ratios.

59. The apparatus of claim 33, wherein the solid state lighting comprises at least one light emitting diode.

- 49 -

60. The apparatus of claim 59, wherein the at least one light emitting diode is coupled to a power converter, and wherein the first and second comparators are coupled to a current sensor at a comparatively low side of the power converter.

5

61. The apparatus of claim 33, wherein the solid state lighting comprises a plurality of arrays of a plurality of series-connected light emitting diodes, each array of the plurality of arrays is further coupled to a corresponding switch, and wherein the controller is further adapted to turn each corresponding switch into an on state and an
10 off state.

62. The apparatus of claim 61, wherein the controller is further adapted to separately determine a corresponding first on time period, a corresponding second on time period, and a corresponding on time period as substantially proportional to the
15 sum of the corresponding first on time period and the corresponding second on time period for each array of the plurality of arrays.

63. The apparatus of claim 62, wherein the controller is further adapted, when the corresponding on time period has elapsed, to separately turn the
20 corresponding switch into an off state.

64. The apparatus of claim 62, wherein the controller is further adapted to separately determine a corresponding off time period for each array of the plurality of
25 arrays.

65. The apparatus of claim 62, wherein the controller is further adapted to interleave the corresponding on time periods of the corresponding switches of the plurality of arrays.

30 66. The apparatus of claim 62, wherein the controller is further adapted to successively turn into an on state each corresponding switch for each array of the plurality of arrays for the corresponding on time period.

- 50 -

67. The apparatus of claim 33, further comprising:
a reference voltage generator coupled to the first and second
comparators and adapted to provide reference voltages respectively corresponding to
5 the first predetermined current threshold and to the predetermined average current
level.
68. The apparatus of claim 33, further comprising:
an input-output interface coupled to the controller and adapted to receive
10 an input control signal.
69. The apparatus of claim 33, wherein the apparatus is coupled to a DC-DC
power converter receiving a DC input voltage or coupled to AC-DC power converter
receiving a rectified AC input voltage.

15

- 51 -

70. A solid state lighting system, the system couplable to a power source, the system comprising:

a plurality of arrays of series-connected light emitting diodes;

a plurality of switches, a corresponding switch of the plurality of

5 switches coupled to each the array of the plurality of arrays of light emitting diodes;

at least one corresponding first comparator adapted to determine when a corresponding switch electrical current has reached a corresponding first predetermined current threshold;

10 at least one corresponding second comparator adapted to determine when the corresponding switch electrical current has reached a corresponding predetermined average current level; and

at least one controller coupled to the corresponding first comparator and to the corresponding second comparator, the controller adapted to turn the corresponding switch into an on state and an off state, to determine a corresponding
15 first on time period as a duration between either a detection of a corresponding second predetermined current threshold or the turning the corresponding switch into the on state, and the detection of the corresponding predetermined average current level; to determine a corresponding second on time period as a duration between the detection of the corresponding predetermined average current level and the detection of the
20 corresponding first predetermined current threshold; and to determine a corresponding on time period of the corresponding switch as substantially proportional to a sum of the corresponding first on time period and the corresponding second on time period.

71. The system of claim 70, wherein the at least one controller is further
25 adapted, when the corresponding on time period has elapsed, to turn the corresponding switch into an off state.

72. The system of claim 70, wherein the at least one controller is further adapted, subsequent to turning the corresponding switch into the off state and when a
30 fixed time period has elapsed from having turned the corresponding switch into the on state, to turn the corresponding switch into the on state.

- 52 -

73. The system of claim 72, wherein the at least one controller is further adapted to generate a corresponding error signal as a difference between the corresponding second on time period and the corresponding first on time period.

5 74. The system of claim 73, wherein the at least one controller is further adapted to adjust the corresponding on time period proportionally to the corresponding error signal.

75. The system of claim 70, wherein the at least one controller is further
10 adapted to determine a corresponding current off time period of the corresponding switch as a function of the corresponding first on time period and the corresponding second on time period.

76. The system of claim 70, wherein the at least one controller is further
15 adapted to determine a corresponding current off time period of the corresponding switch as a function of the corresponding first on time period, the corresponding second on time period, and a corresponding previous off time period.

77. The system of claim 70, wherein the at least one controller is further
20 adapted to determine a corresponding current off time period of the corresponding switch as:

$$T_{off}(K+1) \approx \frac{2 \cdot T_{ON2}(K) \cdot T_{off}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}, \text{ in which } T_{off}(K+1) \text{ is the corresponding current}$$

off time period, $T_{ON2}(K)$ is a corresponding previous second on time period, $T_{off}(K)$ is a corresponding previous off time period, and $T_{ON1}(K+1)$ is a corresponding current
25 first on time period.

78. The system of claim 70, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as a function of a corresponding current first on time period, a corresponding
30 previous second on time period, and a corresponding previous off time period.

- 53 -

79. The system of claim 70, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as a function of a corresponding current first on time period, a corresponding previous first on time period, a corresponding previous second on time period, and a
5 corresponding previous off time period.

80. The system of claim 70, wherein the at least one controller is further adapted to adjust a corresponding current off time period to provide that the corresponding first on time period is substantially equal to the corresponding second on
10 time period.

81. The system of claim 70, further comprising:
at least one corresponding gate driver circuit coupled between the at least one controller and the corresponding switch, and wherein the at least one
15 controller is adapted to turn the corresponding switch on and to turn the corresponding switch off by generating a corresponding signal to the corresponding gate driver circuit.

82. The system of claim 81, wherein the at least one controller is further adapted to decrease a corresponding current off time period proportionally to a rising
20 edge time period of the at least one corresponding gate driver circuit.

83. The system of claim 81, wherein the at least one controller is further adapted to decrease the corresponding on time period proportionally to a falling edge time period of the at least one corresponding gate driver circuit and a falling edge time
25 period of the at least one first comparator.

84. The system of claim 81, wherein the at least one controller is further adapted to adjust the corresponding second on time period proportionally to a falling edge time period of the at least one corresponding gate driver circuit.
30

- 54 -

85. The system of claim 81, wherein the at least one controller is further adapted to decrease the corresponding second on time period proportionally to a falling edge time period of the at least one corresponding gate driver circuit and a falling edge time period of the at least one first comparator.

5

86. The system of claim 81, wherein the at least one controller is further adapted to determine a corresponding blanking time interval following turning the corresponding switch into the on state.

10

87. The system of claim 86, further comprising:
at least one corresponding third comparator adapted to determine when the corresponding electrical current has reached the corresponding second predetermined current threshold.

15

88. The system of claim 87, wherein the at least one controller is further adapted to determine a corresponding current off time period of the corresponding switch as:

$$T_{OFF}(K+1) \approx \frac{(T_{ON1}(K)_A + T_{ON2}(K)) \cdot T_{OFF}(K)}{T_{ON1}(K+1) + T_{ON2}(K)}, \text{ in which } T_{OFF}(K+1) \text{ is the}$$

20

corresponding current off time period, $T_{ON1}(K)_A$ is a corresponding previous first on time period determined using the detection of the second predetermined current level, $T_{ON2}(K)$ is a corresponding previous second on time period, $T_{OFF}(K)$ is a corresponding previous off time period, and $T_{ON1}(K+1)$ is a corresponding current first on time period.

25

89. The system of claim 87, wherein the at least one controller is further adapted to ignore the detection of the corresponding second predetermined current threshold, the detection of the corresponding predetermined average current level, or the detection of the corresponding first predetermined current threshold during the corresponding blanking time interval.

- 55 -

90. The system of claim 87, wherein the at least one controller is further adapted to determine the corresponding blanking time interval as proportional to a rising edge time period of the at least one corresponding gate driver circuit and a corresponding transient current time period.

5

91. The system of claim 87, wherein the at least one controller is further adapted to determine the corresponding blanking time interval as proportional to a rising edge time period of the at least one corresponding gate driver circuit and detection of the corresponding predetermined average current level.

10

92. The system of claim 70, wherein the at least one controller is further adapted to adjust a brightness level of at least one array of the plurality of arrays of light emitting diodes by generating control signals to a driver circuit for the at least one array for using at least two different and opposing electrical biasing techniques.

15

93. The system of claim 70, wherein the at least one controller is further adapted to adjust a brightness level of at least one array of the plurality of arrays of light emitting diodes by generating control signals to a driver circuit for the at least one array to use a hysteresis of at least two electrical current amplitude levels and at least two electrical current duty cycle ratios.

20

94. The system of claim 70, wherein each corresponding array of the plurality of arrays of light emitting diodes has a comparatively high voltage node and a comparatively low voltage node, and wherein the at least one first and second comparators are coupled via the corresponding switch to the comparatively low voltage node.

25

95. The system of claim 70, wherein the at least one controller is further adapted to interleave the corresponding on time periods of the corresponding switches of the plurality of arrays.

30

- 56 -

96. The system of claim 70, wherein the at least one controller is further adapted to successively turn into an on state each corresponding switch for each array of the plurality of arrays for the corresponding on time period.

5 97. The system of claim 70, further comprising:
at least one reference voltage generator coupled to the at least one corresponding first and second comparators and adapted to provide corresponding reference voltages respectively for the corresponding first predetermined current threshold and the corresponding predetermined average current level.

10

98. The system of claim 70, further comprising:
an input-output interface coupled to the at least one controller and adapted to receive an input control signal.

15 99. The system of claim 70, further comprising:
at least one rectifier couplable to the power source.

100. The system of claim 70, wherein the power source provides a DC input voltage or a rectified AC input voltage.

20

101. The system of claim 70, wherein when the power source provides a rectified AC input voltage, an electrical current through a corresponding switch is substantially zero when the rectified AC input voltage is below a selected or predetermined threshold.

25

102. The system of claim 70, wherein when the power source provides a rectified AC input voltage, the at least one controller is in an off state when the rectified AC input voltage is below a selected or predetermined threshold.

- 57 -

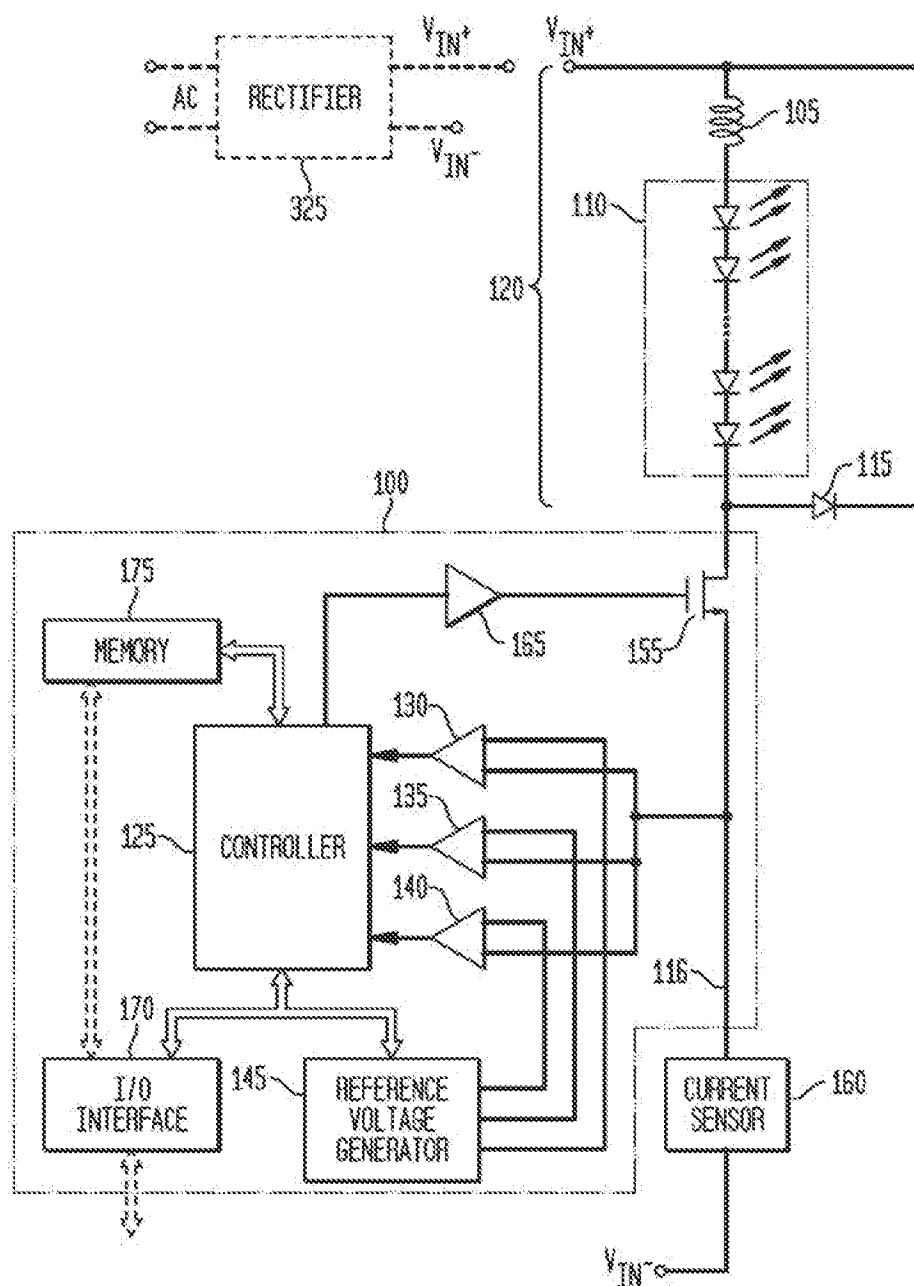
103. An apparatus for controlling solid state lighting, the apparatus comprising:

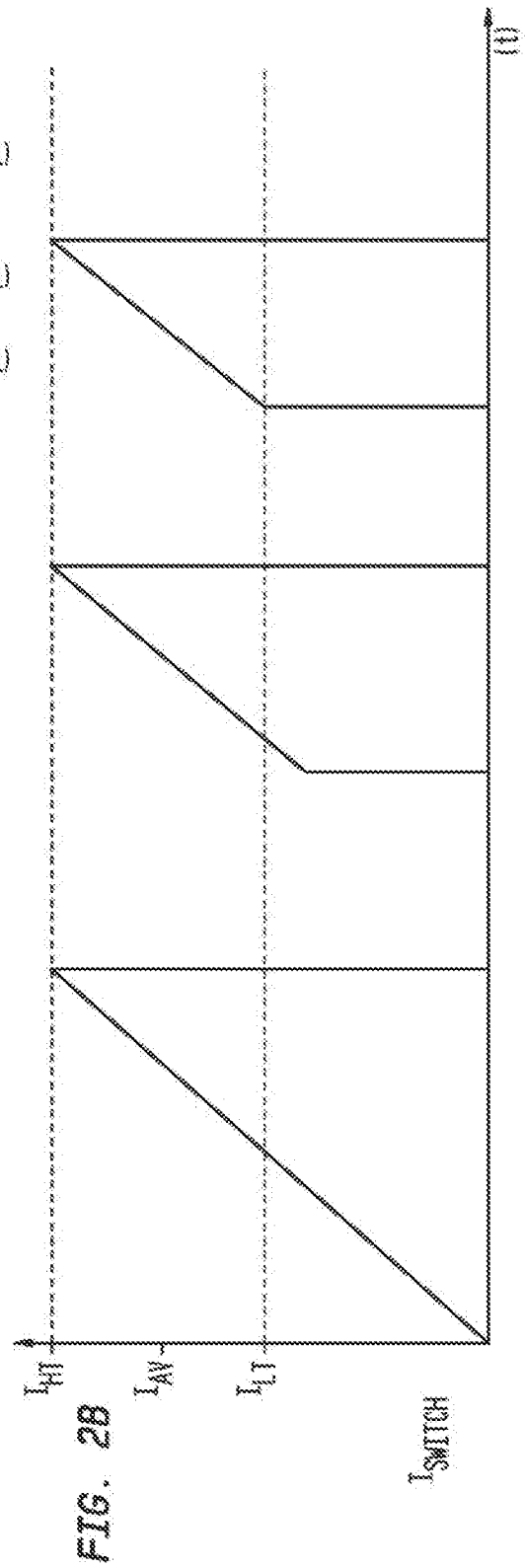
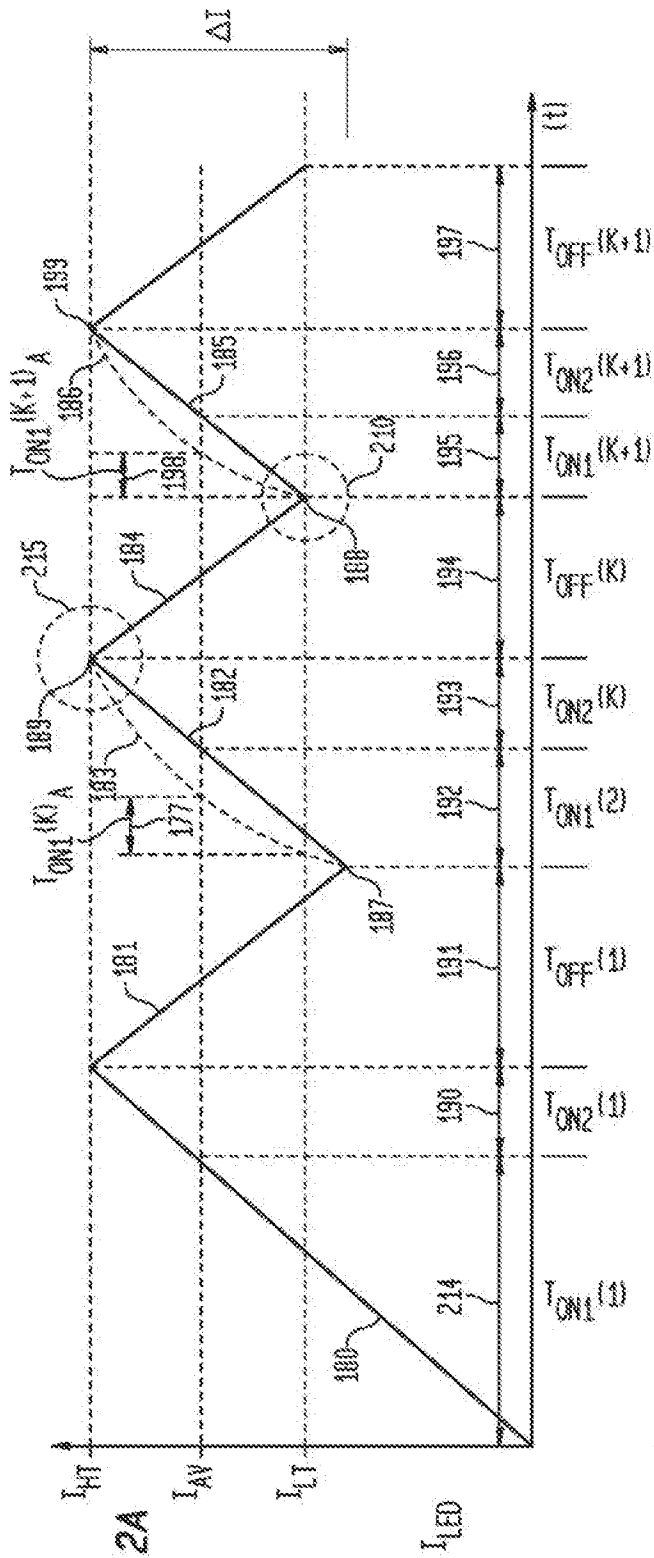
- a switch couplable to the solid state lighting;
- a current sensor coupled to the switch;
- 5 a first comparator adapted to determine when a switch electrical current has reached a first predetermined current threshold;
- a second comparator adapted to determine when the switch electrical current has reached a predetermined average current level;
- a third comparator adapted to determine when the switch electrical
- 10 current has reached a second predetermined current threshold;
- a reference voltage generator coupled to the first, second and third comparators and adapted to provide reference voltages respectively corresponding to the first predetermined current threshold, the second predetermined current threshold; and to the predetermined average current level;
- 15 an input-output interface adapted to receive an input control signal; and
- a controller coupled to the first, second and third comparators and to the input-output interface, the controller adapted to turn the switch into an on state and an off state, to determine a first on time period as a duration between either the detection
- 20 of a second predetermined current threshold or the turning the switch into the on state, and the detection of the predetermined average current level; to determine a second on time period as a duration between the detection of the predetermined average current level and the detection of the first predetermined current threshold; to determine an on time period of the switch as substantially proportional to a sum of the first on time
- 25 time period and the second on time period; to turn the switch into an off state when the on time period has elapsed; and to determine a current off time period of the switch as a function of the first on time period, the second on time period, and a previous off time period.

1/10

FIG. 1

150





3/10

FIG. 3

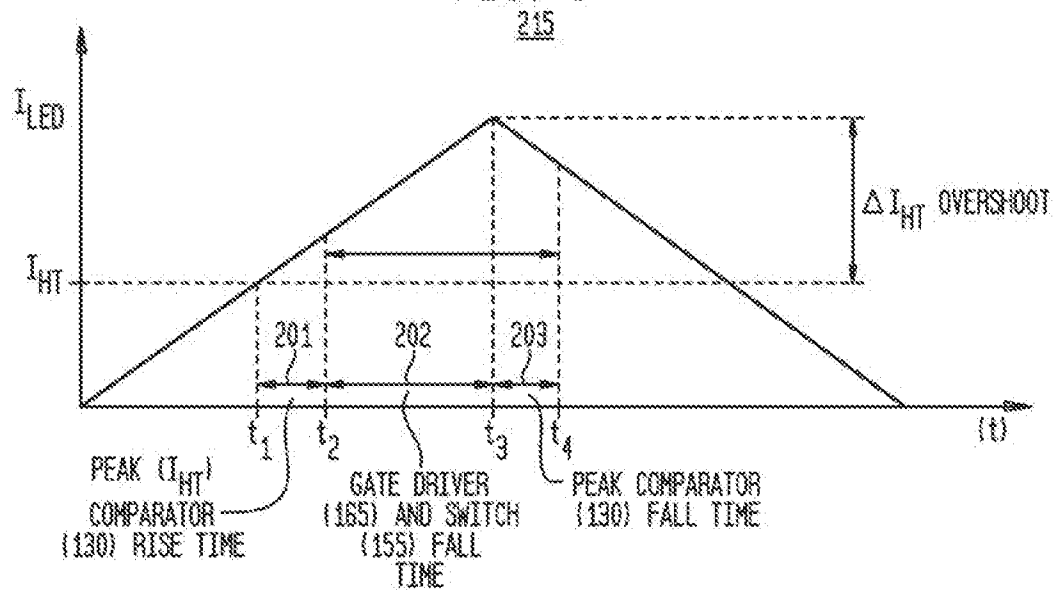
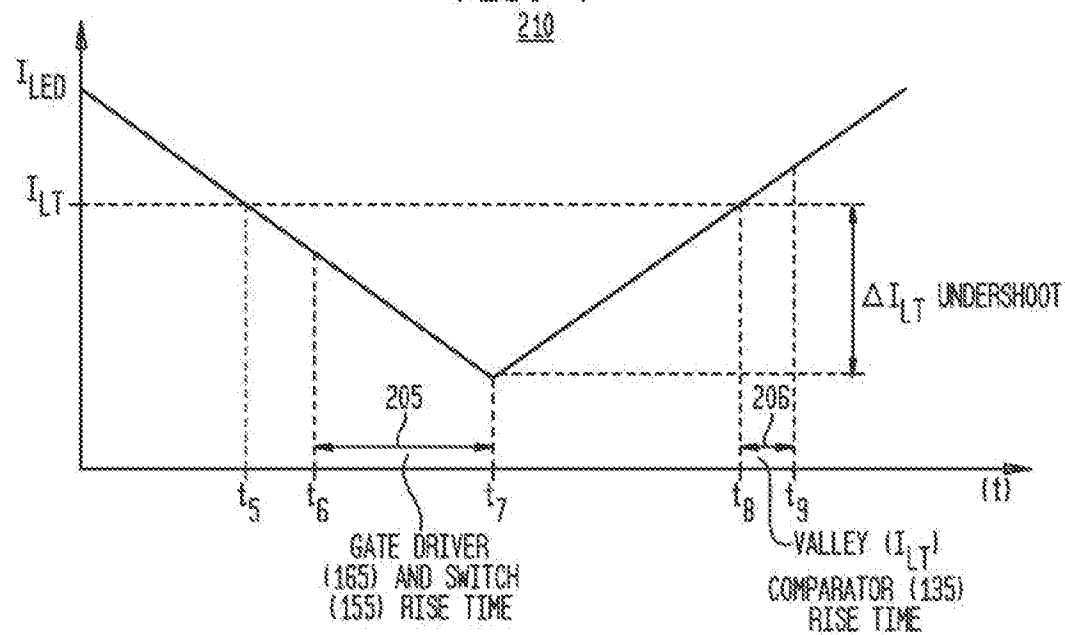
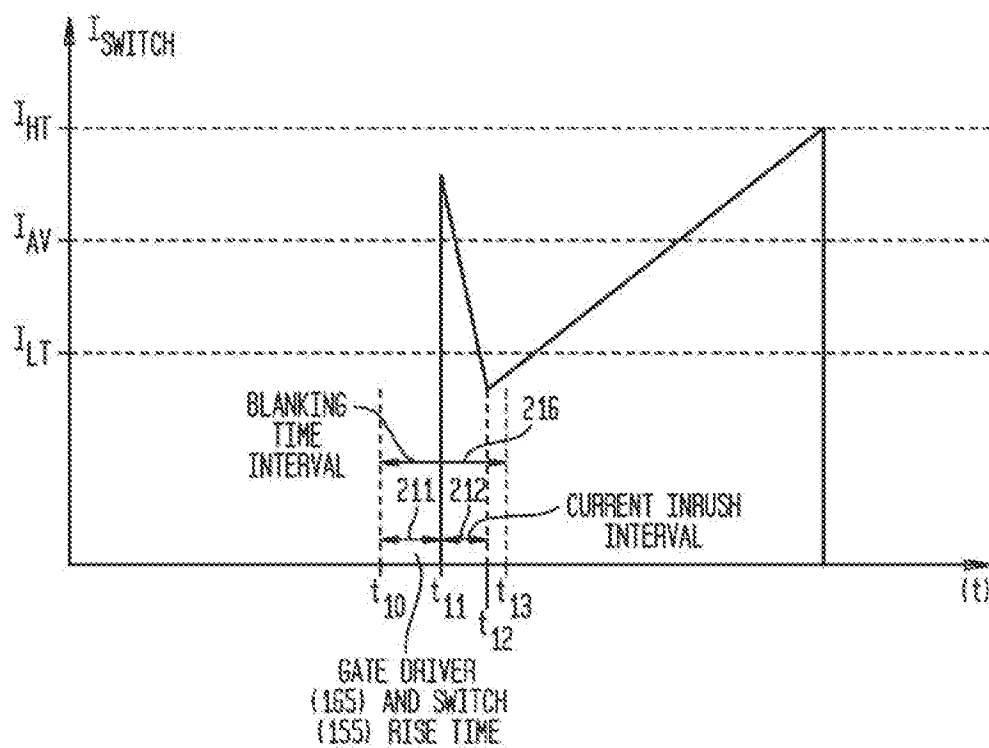


FIG. 4



4/10

FIG. 5



5/10

FIG. 6

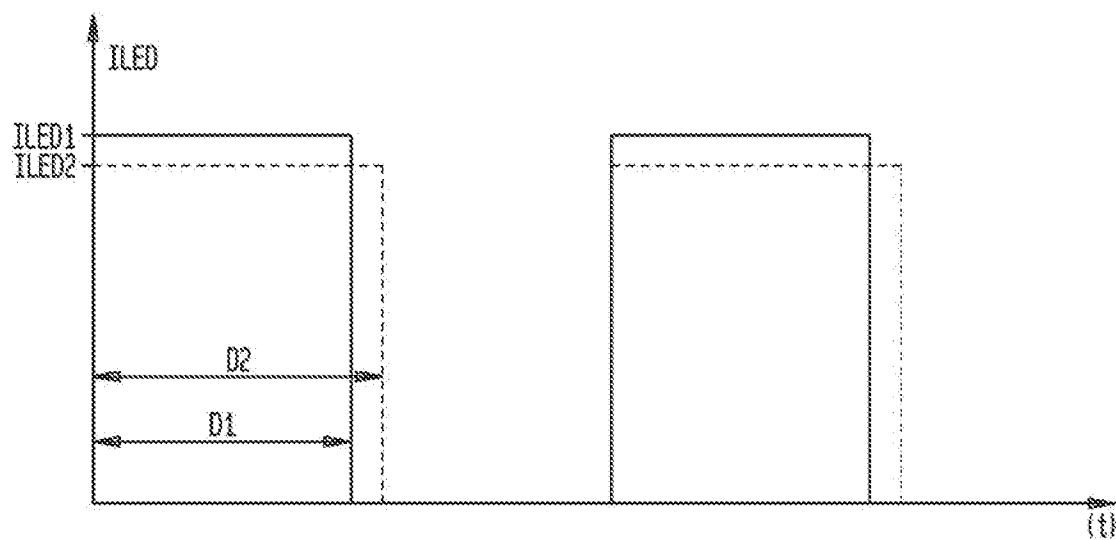
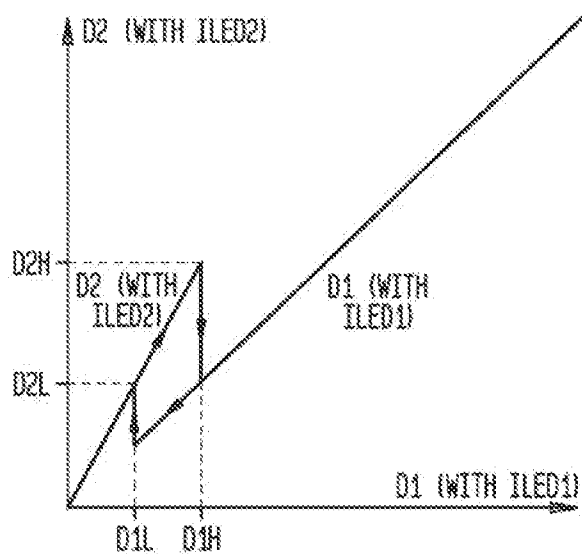


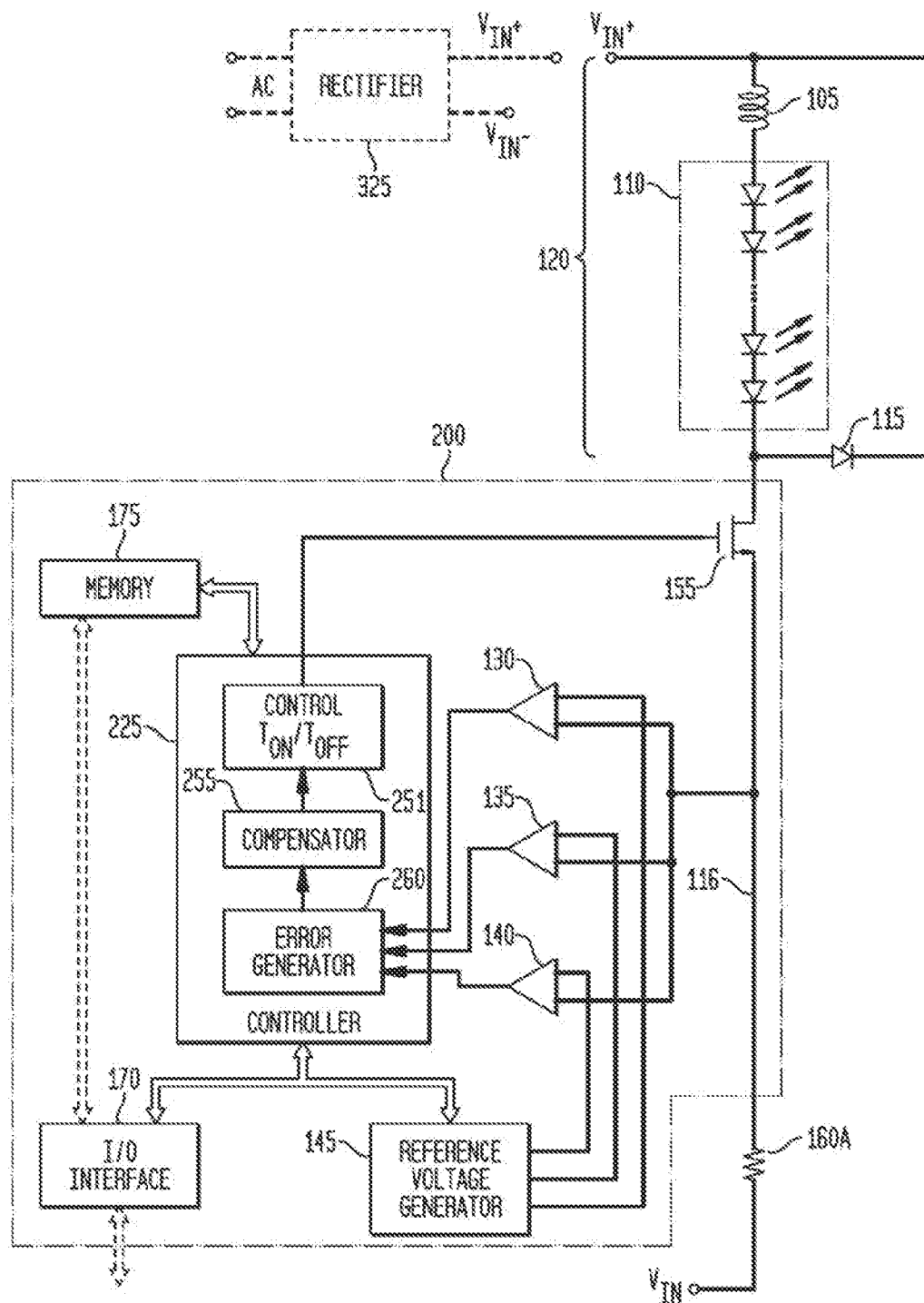
FIG. 7



2000

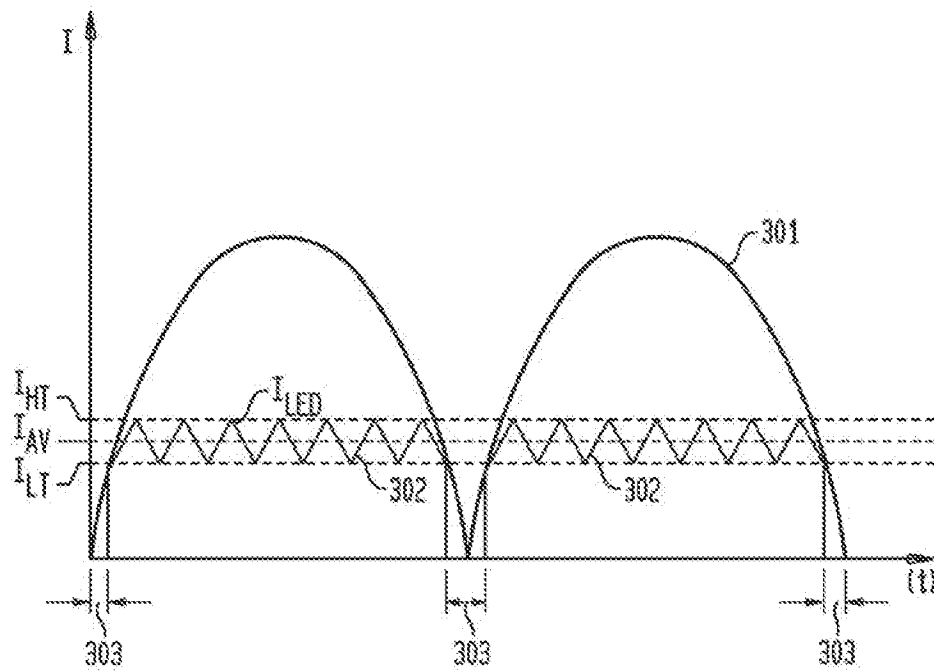
FIG. 8

250



7/10

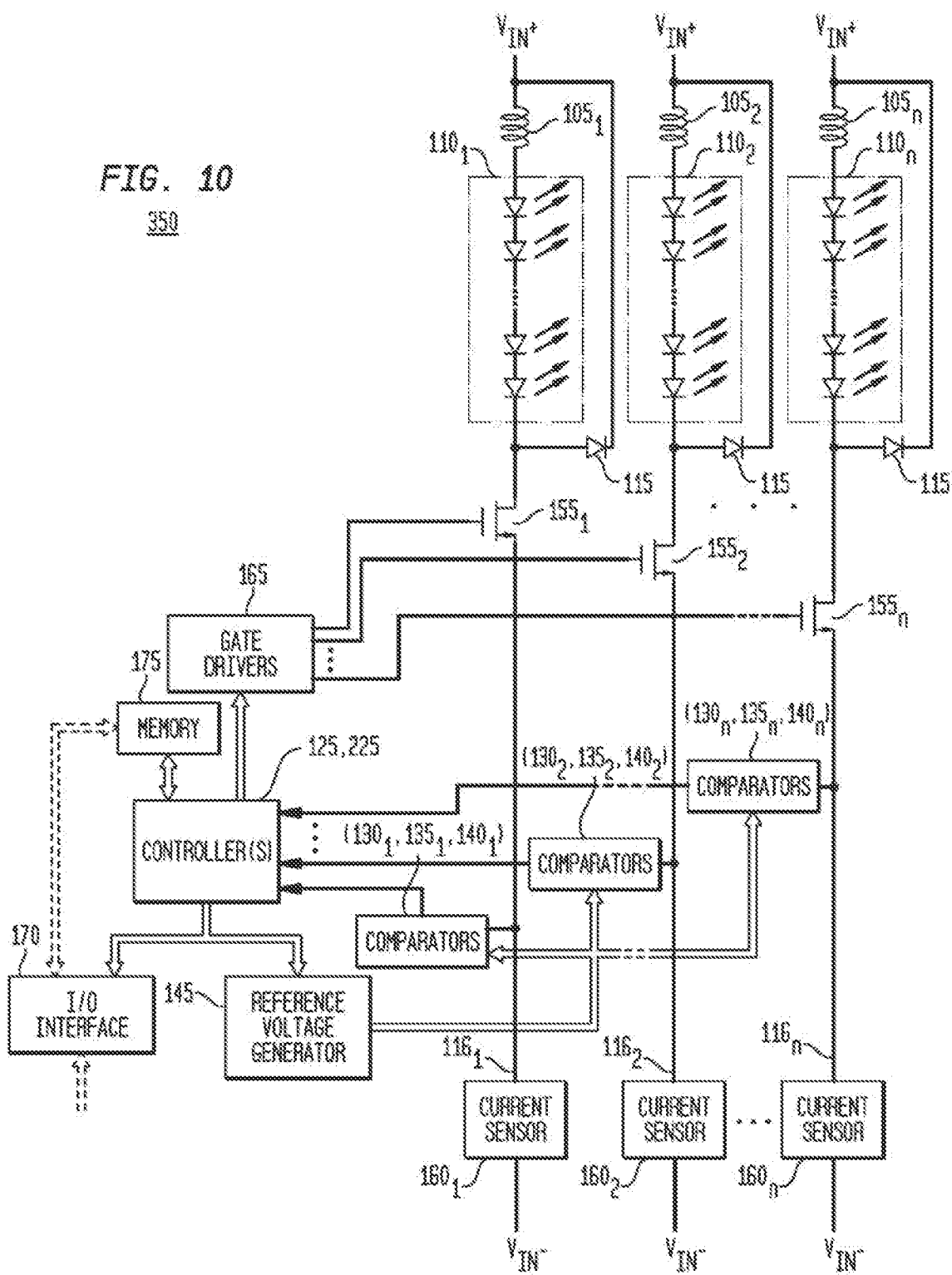
FIG. 9



8/10

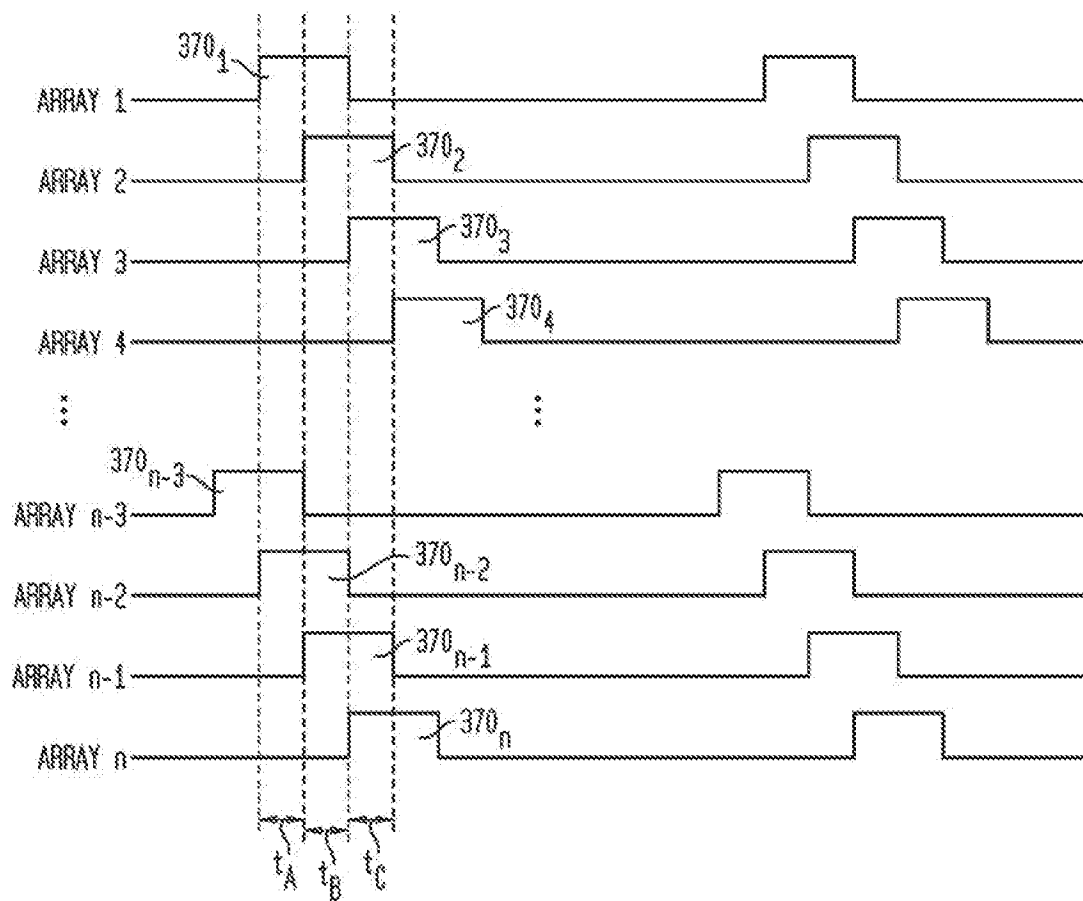
FIG. 10

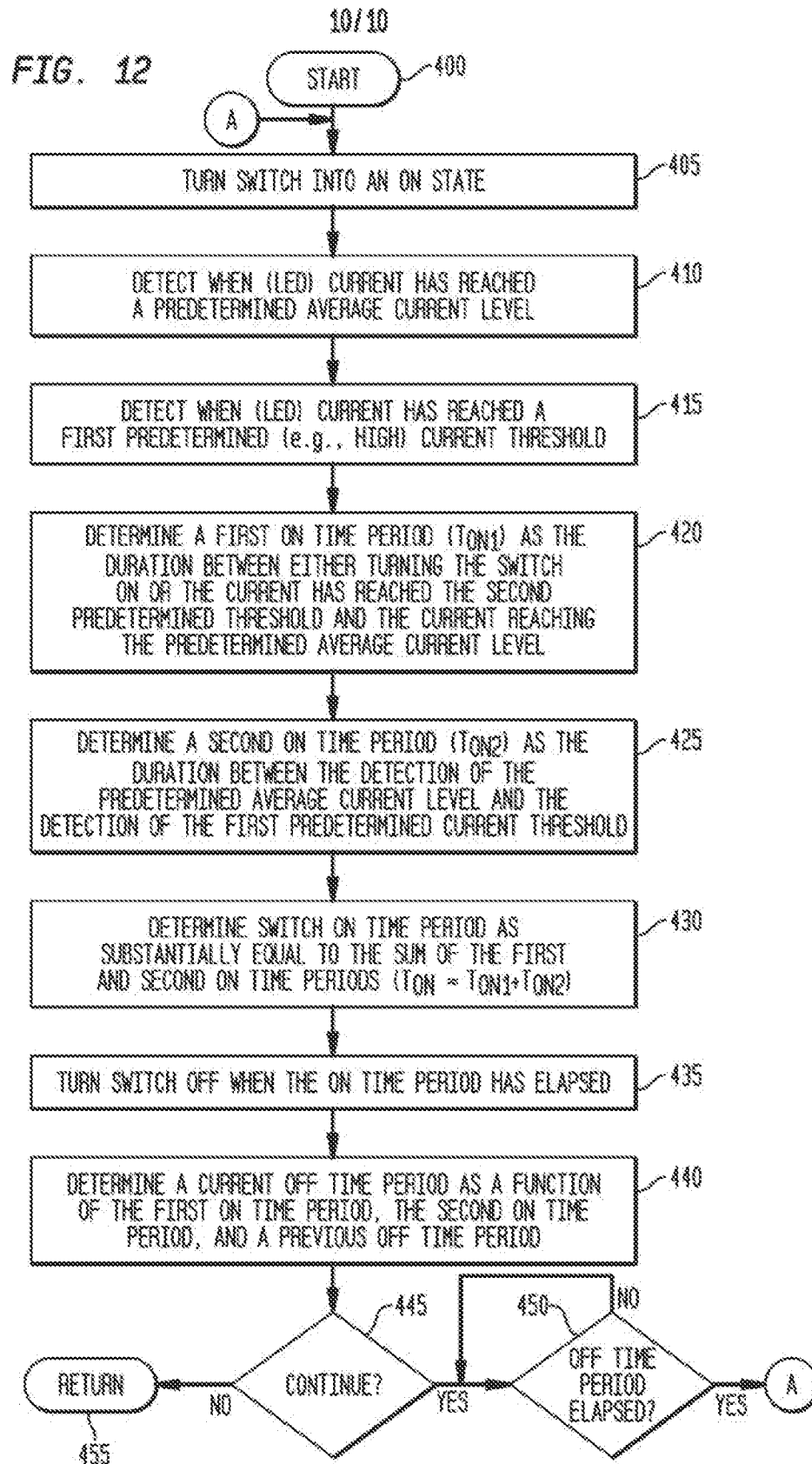
350



9/10

FIG. 11





INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 08/76552

A. CLASSIFICATION OF SUBJECT MATTER

IPC(B) - G05F 1/30 (2008.04)

USPC - 315/291

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC: 315/291

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 368/189, 315/291, 149, 150, 156, 159

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO WEST (PGPB, USPT, EPAB, JPAB); Google Scholar;

Search Terms Used: predetermined, current level, light control, controlling, LED, array, detect, current, period, time, phase, duration, interval, on time, circuit.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/0024213 A1 (Shleyenberg et al.) 1 February 2007 Especially (para (0007)-(0009), (0012), (0013), (0017)-(0019), (0047)-(0049), (0052), (0053), (0057)-(0059), (0065), (0066), (0072), (0075), para (0081) - Fig. 14, Fig. 2)	1-103
A	US 2007/0194210 A1 (Lee et al.) 23 August 2007	1-103
A	US 7381722 B1 (Huynh et al.) 25 July 2005	1-103
A	US 6731079 B2 (Anderson et al.) 4 May 2004 (04.05.2004)	1-103

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"Z" document member of the same patent family

Date of the actual completion of the international search

8 November 2008 (08.11.2008)

Date of mailing of the international search report

19 NOV 2008

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1480, Alexandria, Virginia 22313-1480
Facsimile No. 571-273-3201

Authorized officer:

Lee W. Young

PCT Helpdesk: 271-272-1320
PCT OSP: 571-272-7774

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		
First Named Inventor/Applicant Name:		David TIKKANEN		
Filer:		Jeffrey Wong/Christopher Kreider		
Attorney Docket Number:		K8001064WOUSCON1		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt

EFS ID:	21221979
Application Number:	14597788
International Application Number:	
Confirmation Number:	9654
Title of Invention:	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS
First Named Inventor/Applicant Name:	David TIKKANEN
Customer Number:	34236
Filer:	Jeffrey Wong/Christopher Kreider
Filer Authorized By:	Jeffrey Wong
Attorney Docket Number:	K8001064WOUSCON1
Receipt Date:	15-JAN-2015
Filing Date:	
Time Stamp:	16:05:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	2506
Deposit Account	501613
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ads.PDF	1562075	no	8
			a5461c112a1993944dd496faf1b4cefab2daa94c		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	drawings.PDF	733110	no	12
			9b6d1f1b7c4fc9cbbbedb134710bb863dac a78fe		
Warnings:					
Information:					
3		spec.pdf	98048	yes	19
			3f75f8648f2747792533a167914282f9e4d80127		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	15	
	Claims		16	18	
	Abstract		19	19	
Warnings:					
Information:					
4		20150115154447765.pdf	2104015	yes	16
			4538f80a6c6ff99507ded4d335482a9f36a46389		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Assignee showing of ownership per 37 CFR 3.73.		1	2	
	Power of Attorney		3	3	
	Oath or Declaration filed		4	7	

	Assignee showing of ownership per 37 CFR 3.73.	8	16		
Warnings:					
Information:					
5	Information Disclosure Statement (IDS) Form (SB08)	ids.PDF	614209 3780077bf5769670cb9392531808feed2228b4e	no	8
Warnings:					
Information:					
6		refs-1.PDF	7483141 1c1ae6e9dea1f8853c6373d6b295c120ddf73103	yes	40
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Non Patent Literature		1	3	
	Non Patent Literature		4	7	
	Other Reference-Patent/App/Search documents		8	16	
	Other Reference-Patent/App/Search documents		17	24	
	Other Reference-Patent/App/Search documents		25	32	
	Other Reference-Patent/App/Search documents		33	40	
Warnings:					
Information:					
7		refs-2.PDF	16635568 6e80a6f7b9493f7fe419b8836472f90960d6a53d	yes	104
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Foreign Reference		1	34	
	Foreign Reference		35	104	
Warnings:					
Information:					
8		refs-3.PDF	9174861 442b0ab552f28581f84e4ff9747d6b9531434bb2e	yes	59

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Non Patent Literature		1	16	
	Non Patent Literature		17	42	
	Non Patent Literature		43	59	
Warnings:					
Information:					
9		refs-4.PDF	12921855	yes	47
			ecac36ad357fa620b1ff70c6b04444cc987b3165		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Non Patent Literature		1	2	
	Non Patent Literature		3	3	
	Non Patent Literature		4	15	
	Non Patent Literature		16	19	
	Other Reference-Patent/App/Search documents		20	22	
	Other Reference-Patent/App/Search documents		23	45	
	Non Patent Literature		46	47	
Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	35254	no	2
			fb60262c06ff832149b41ecc7db62eba6b54a0fc		
Warnings:					
Information:					
Total Files Size (in bytes):			51362136		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	K8001064WOUSCON1
		Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	David		TIKKANEN		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Waterloo	Country of Residence i	CA		

Mailing Address of Inventor:

Address 1	194 Silverwood Place				
Address 2					
City	Waterloo	State/Province	ON		
Postal Code	N2T 2R9	Country i	CA		

Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Jason		NEUDORF		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Kitchener	Country of Residence i	CA		

Mailing Address of Inventor:

Address 1	306-30 Bridge Street West				
Address 2					
City	Kitchener	State/Province	ON		
Postal Code	N2K 1K4	Country i	CA		

Inventor 3					Remove
Legal Name					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	K8001064WOUSCON1
		Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Steven		LYONS	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Kitchener	Country of Residence i	CA	

Mailing Address of Inventor:

Address 1	1011 Queen's Boulevard			
Address 2				
City	Kitchener	State/Province	ON	
Postal Code	N2M 1B8	Country i	CA	
Inventor 4				Remove

Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Kyle		HATHAWAY	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Kitchener	Country of Residence i	CA	

Mailing Address of Inventor:

Address 1	5 Norbert Place			
Address 2				
City	Kitchener	State/Province	ON	
Postal Code	N2K 1E5	Country i	CA	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐ An Address is being provided for the correspondence Information of this application.	
Customer Number	34236
Email Address	waterloo.ip@gowlings.com Add Email Remove Email

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	K8001064WOUSCON1
		Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		

Application Information:

Title of the Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		
Attorney Docket Number	K8001064WOUSCON1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	12	Suggested Figure for Publication (if any)	3

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	34236		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	K8001064WOUSCON1
		Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
	Continuation of	13941871	2013-07-15		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13941871	Continuation of	13059336	2011-02-16	8525446	2013-09-03
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
13059336	a 371 of international	PCT/CA2009/001295	2009-09-17		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
PCT/CA2009/001295	Claims benefit of provisional	61097963	2008-09-18		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	K8001064WOUSCON1
	Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. ☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
--

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.
--

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	K8001064WOUSCON1
	Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS	

Applicant 1				Remove	
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.					
Clear					
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117		☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.			☐ Person who shows sufficient proprietary interest		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:					
Name of the Deceased or Legally Incapacitated Inventor :					
If the Applicant is an Organization check here. ☒					
Organization Name		LUMASTREAM CANADA ULC			
Mailing Address Information:					
Address 1		400-3rd Avenue S.W.			
Address 2					
City		Calgary	State/Province		AB
Country ⁱ	CA	Postal Code		T2P 4H2	
Phone Number			Fax Number		
Email Address					
Additional Applicant Data may be generated within this form by selecting the Add button. Add					

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.	
Assignee 1	
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.	
Remove	
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	K8001064WOUSCON1
		Application Number	
Title of Invention	CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONS		

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		State/Province	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Jeffrey W. Wong/		Date (YYYY-MM-DD)	2015-01-15
First Name	Jeffrey W.	Last Name	Wong	Registration Number
				46414

Additional Signature may be generated within this form by selecting the Add button.

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

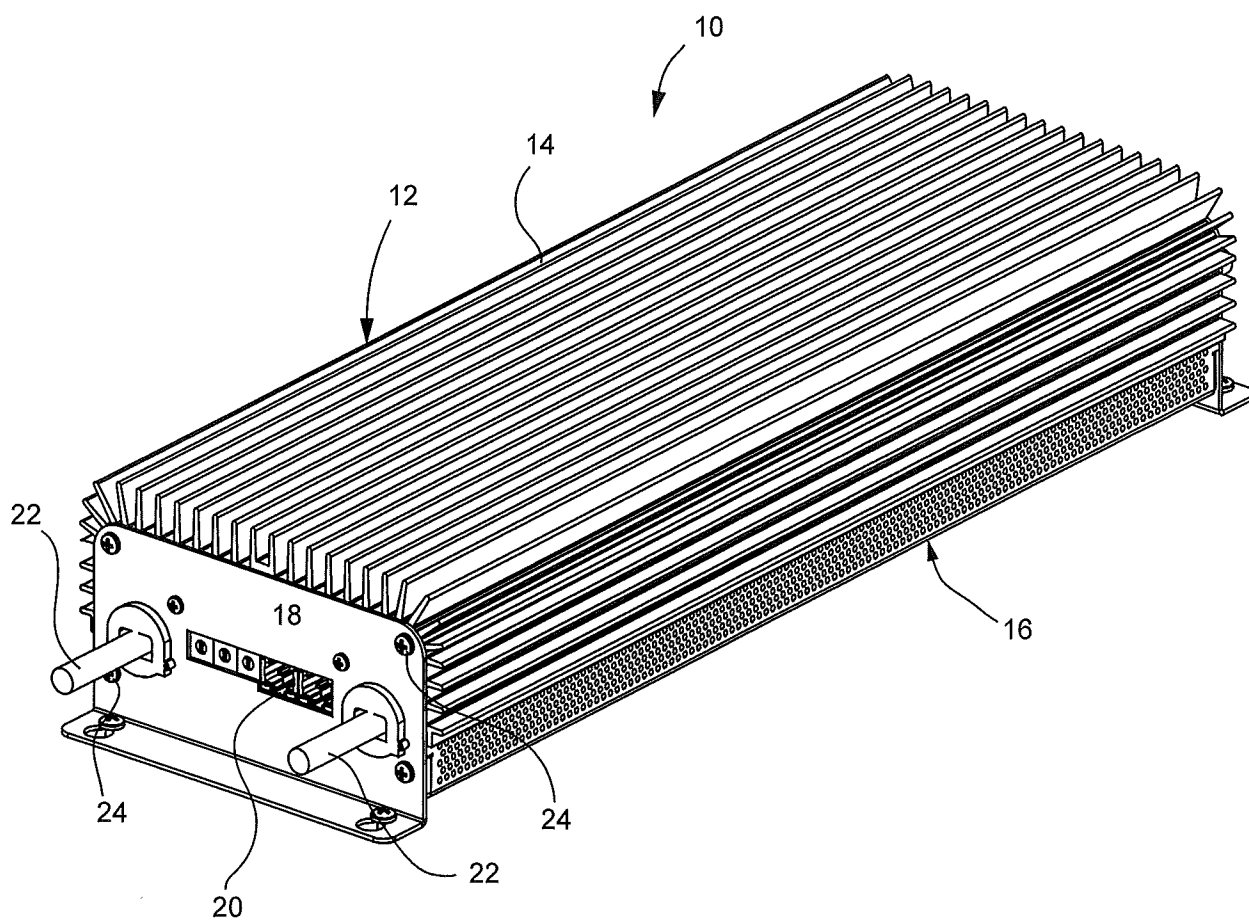


FIGURE 1

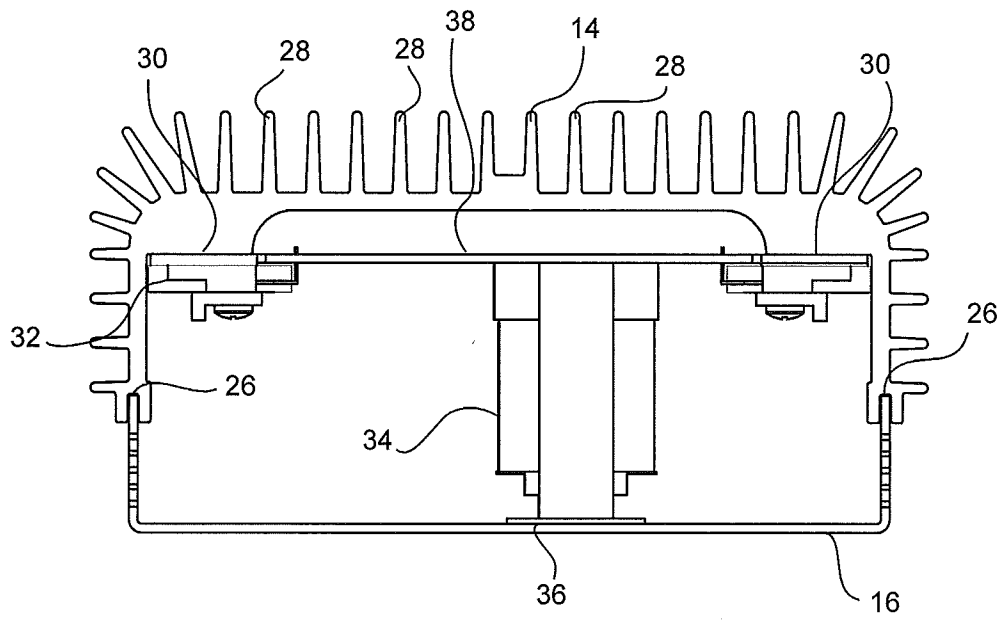


FIGURE 2a

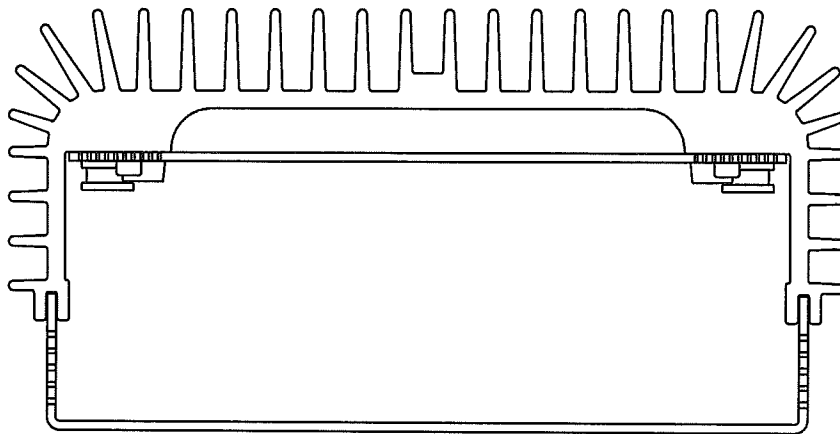


FIGURE 2b

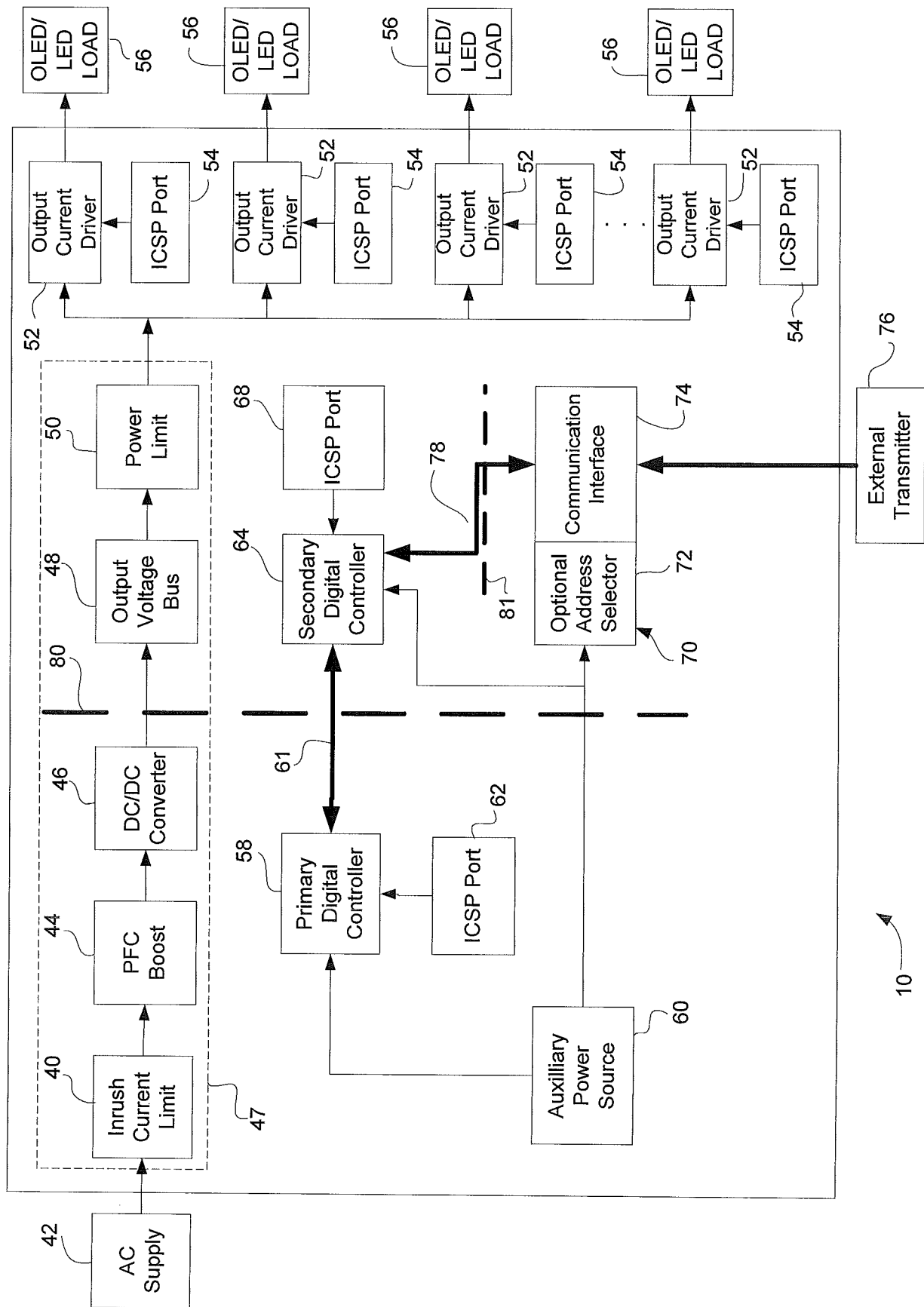


FIGURE 3

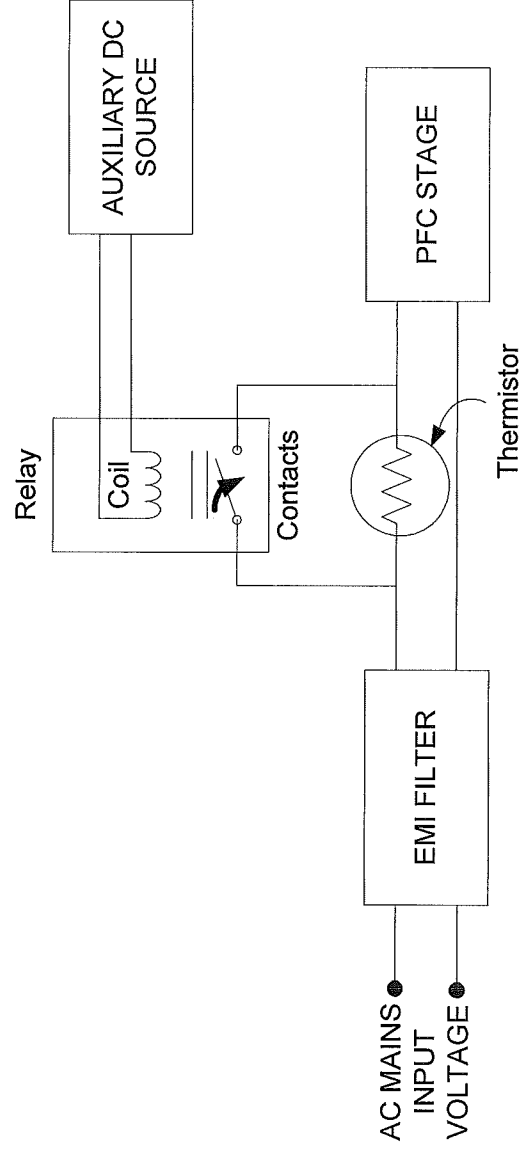


FIGURE 4 (PRIOR ART)

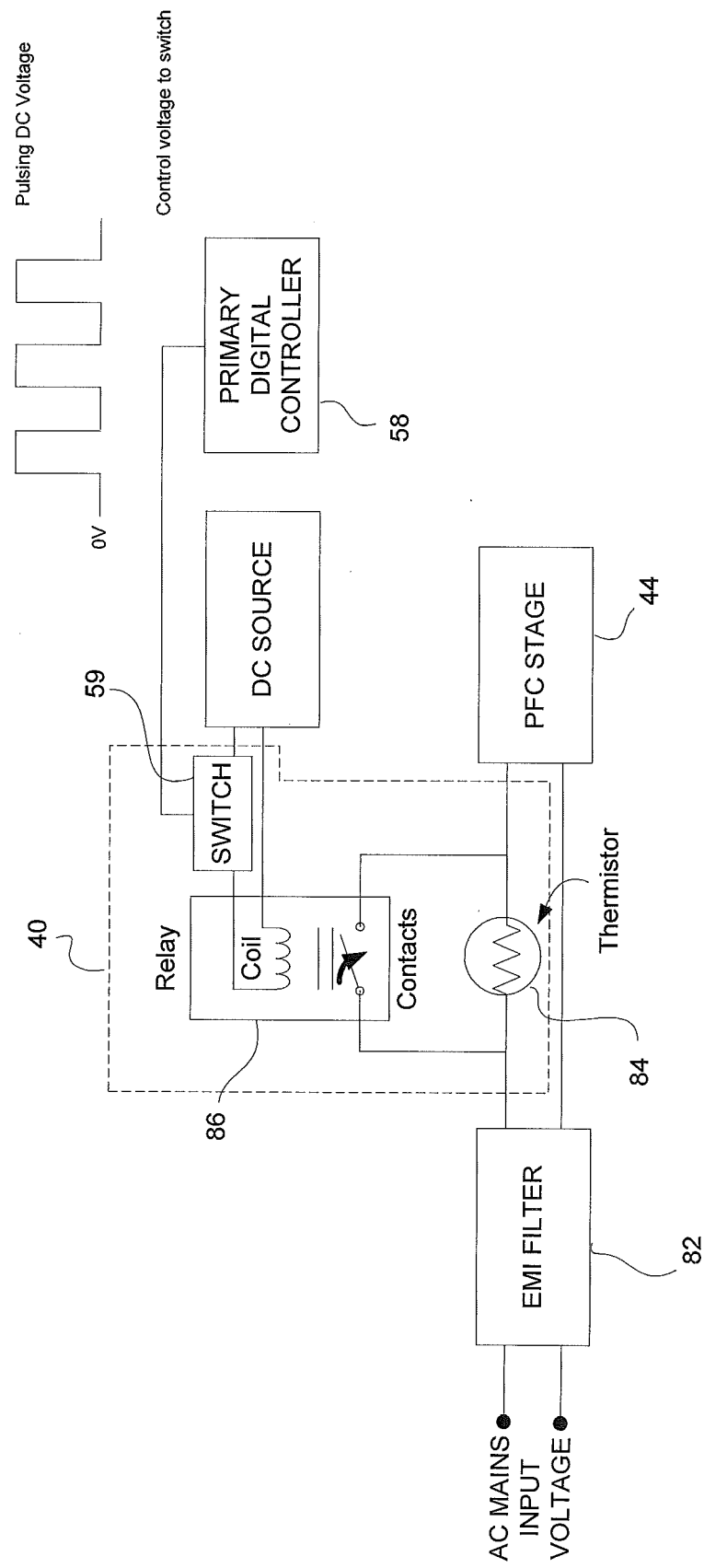


FIGURE 5

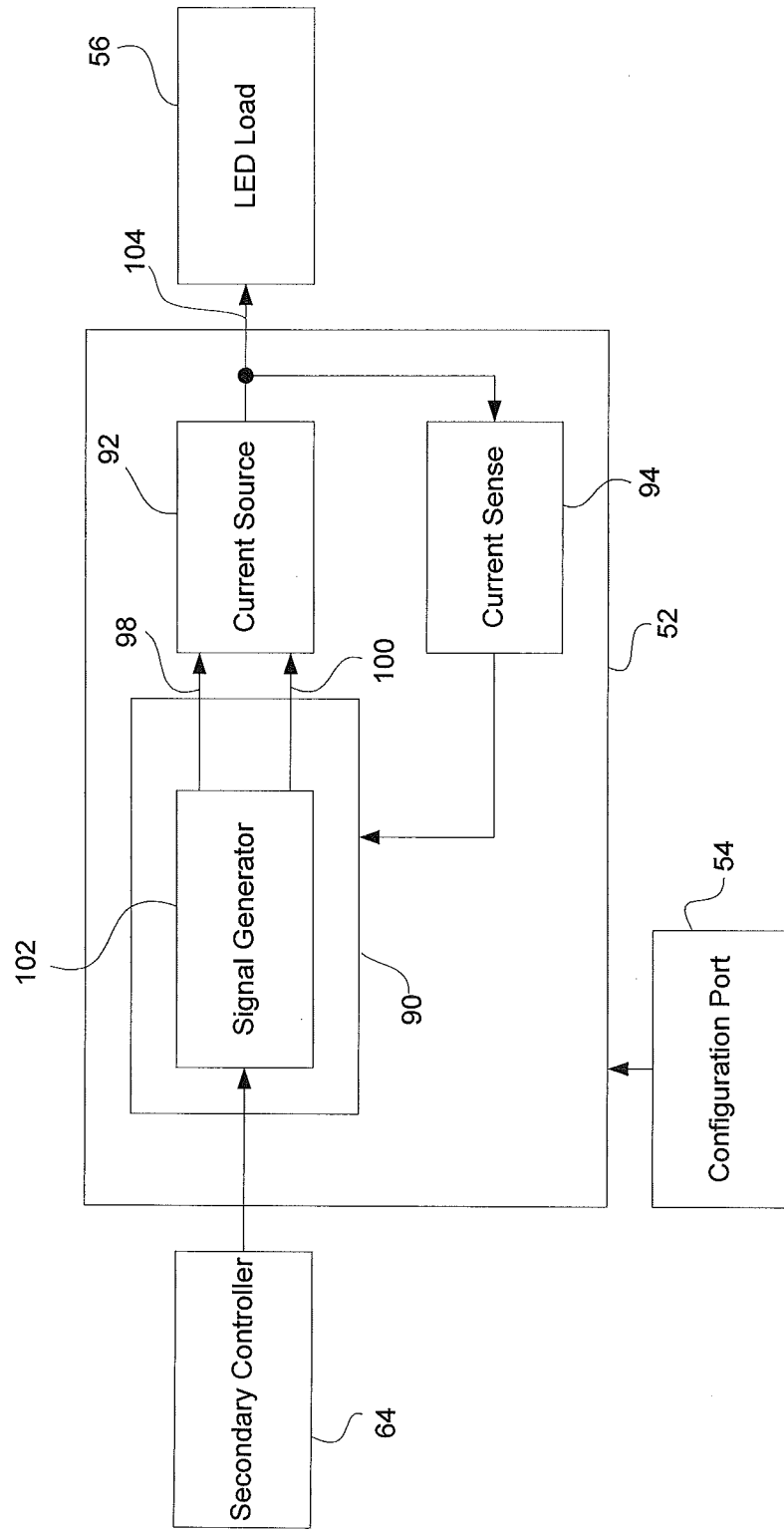


FIGURE 6

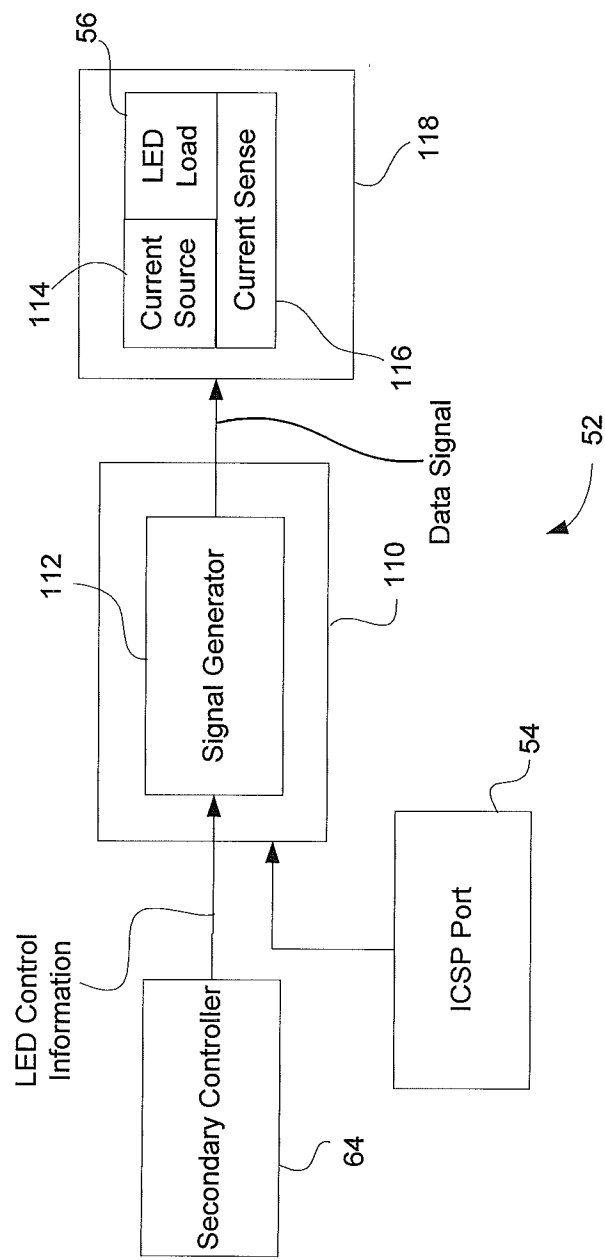


FIGURE 7

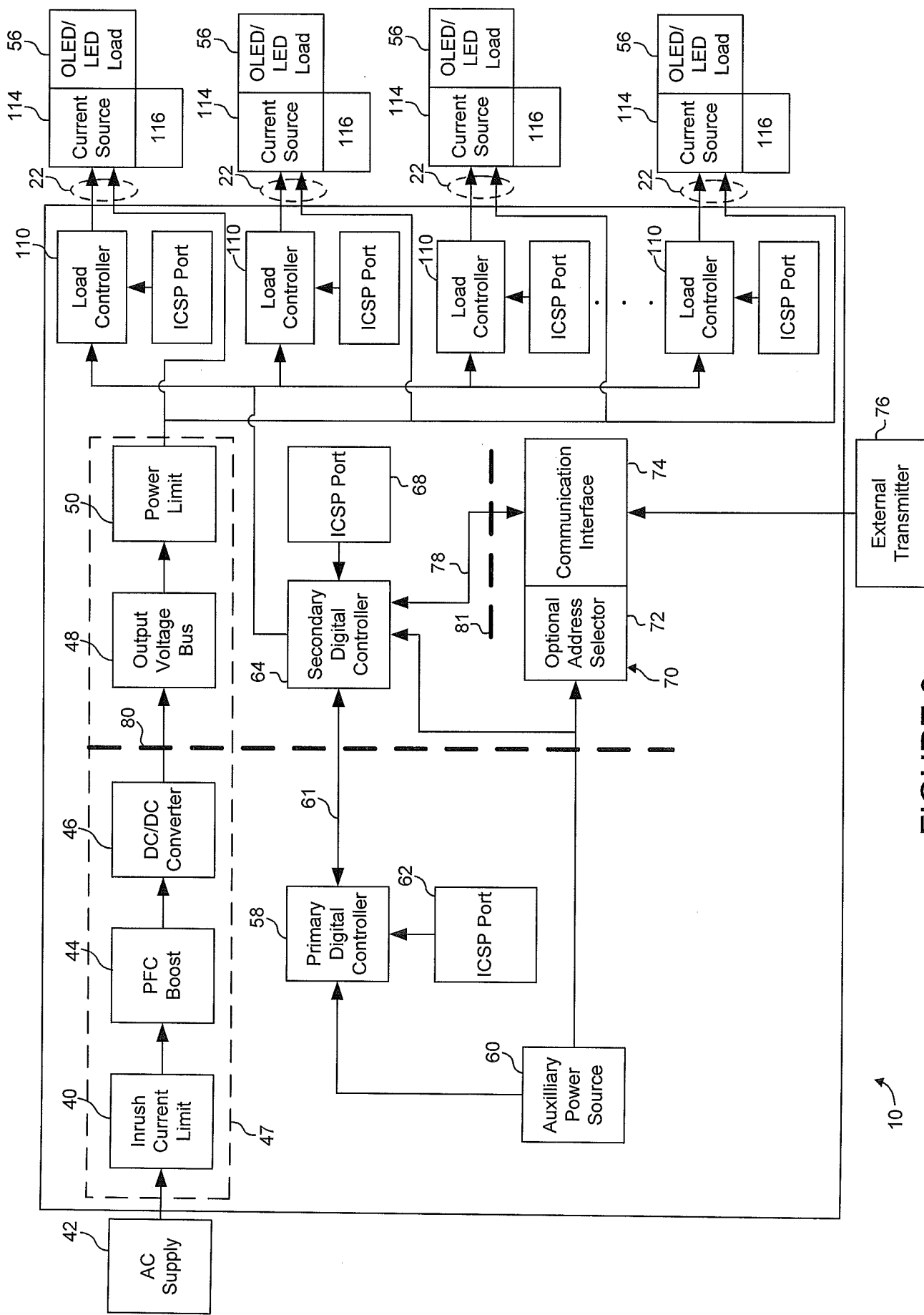


FIGURE 8

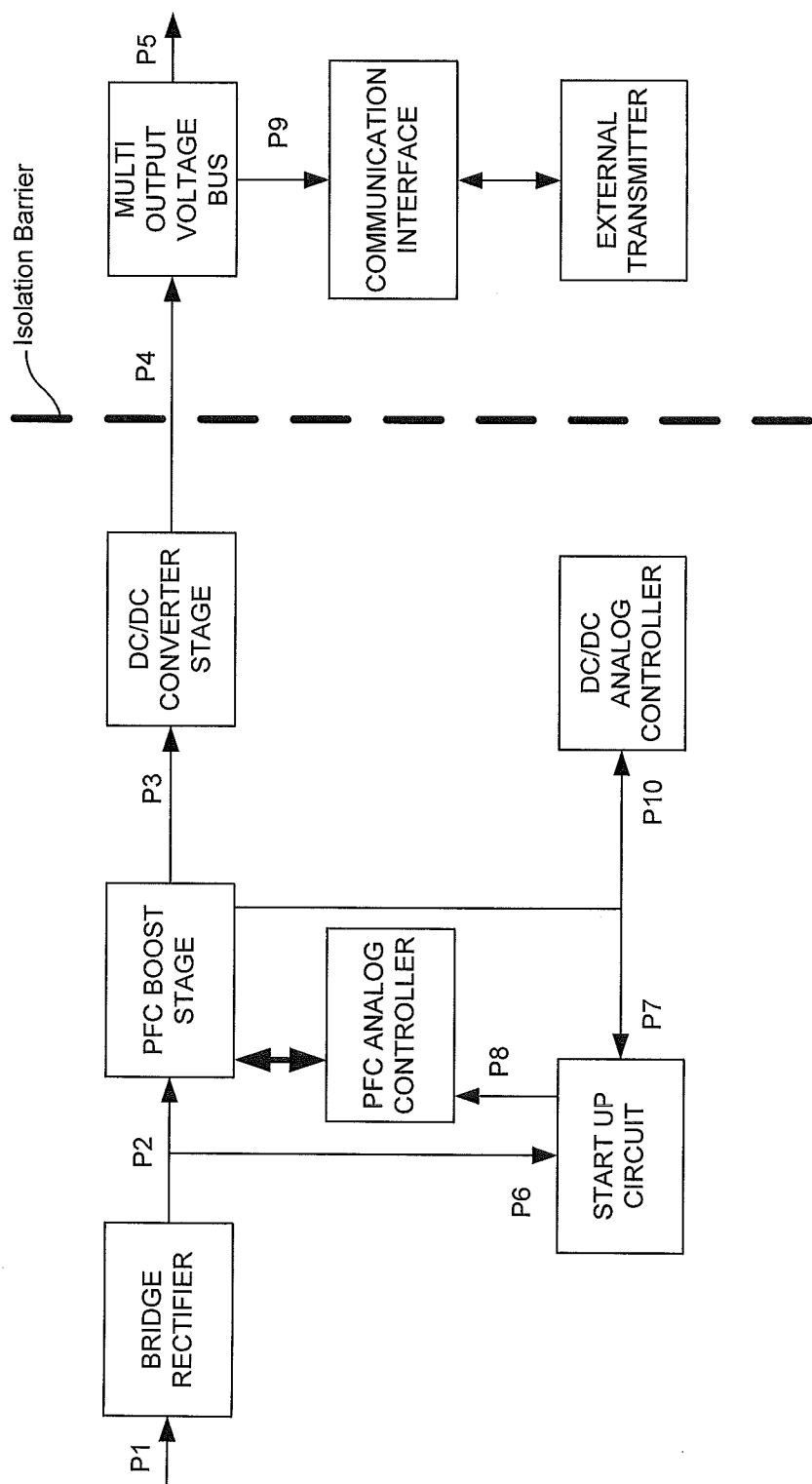


FIGURE 9 (PRIOR ART)

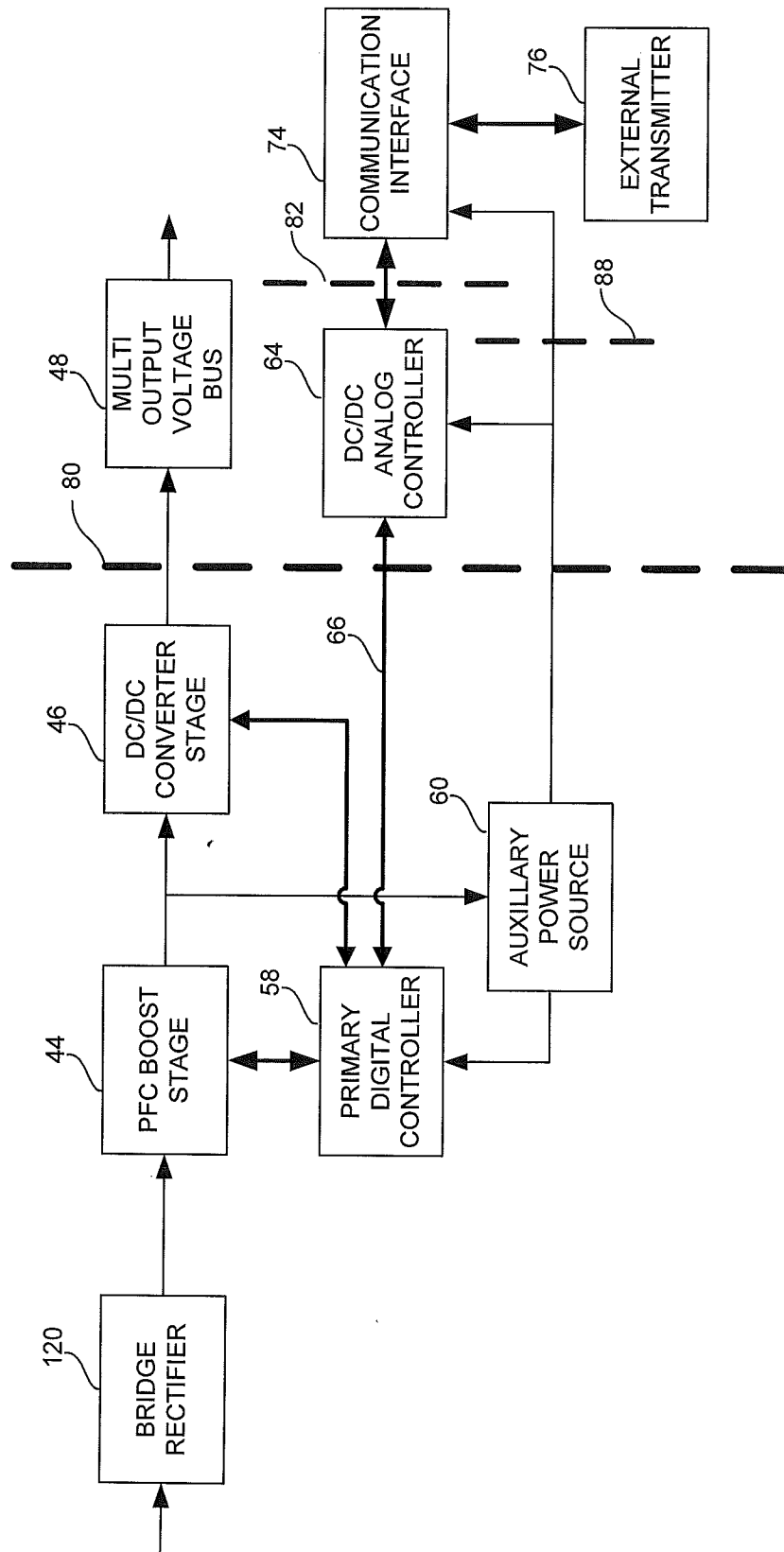


FIGURE 10

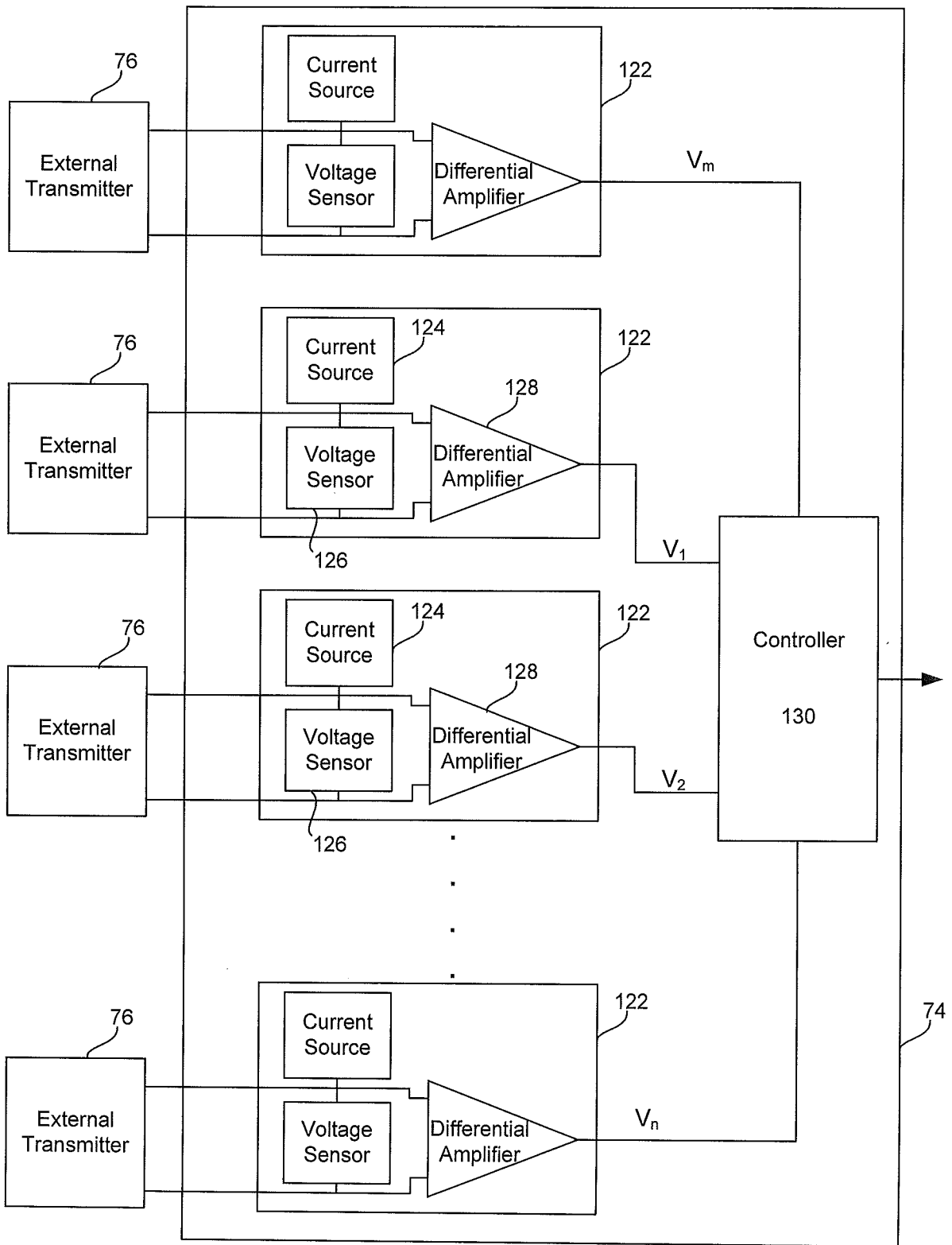


FIGURE 11

CONFIGURABLE LED DRIVER/DIMMER FOR **SOLID STATE LIGHTING APPLICATIONS**

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of US Patent Application No. 13/941,871, filed July 15, 2013, which is itself a continuation of US Patent Application No. 13/059,336, now Patent No. 8,525,446, filed February 16, 2011, which is a national stage filing under 35 U.S.C. 371 of International Patent Application PCT/CA2009/001295, filed on September 17, 2009, which claims the benefit of priority of U.S. Provisional Application No. 61/097,963, filed September 18, 2008, all of which are incorporated herein by reference.

BACKGROUND OF THE DISCLOSURE

[0002] With the rapid increase in light emitting diode (LED) efficacies for high powered LEDs, the latest technologies have exceeded incandescent and halogen sources and are now starting to compete with fluorescent, mercury vapour, metal halide and sodium lighting. In addition to better energy usage, LEDs also have considerable advantages over traditional light sources such as long life, better durability and improved color generating abilities. The advancement of LED technology by various manufacturers has produced high power LEDs with various recommended drive currents such as 350 mA, 500mA, 700mA, 1000mA, and 1400mA or higher.

[0003] In recent years, controllable power sources for Solid State Lighting (SSL) applications have entered the market with integrated features. In addition, digital controllers within power sources have enabled the development of configurable options to provide a wider flexibility of solutions for Solid State Lighting applications. The ability to dim the light output of LEDs is also important to reduce energy consumption.

[0004] However, lighting companies are faced with considerable challenges in adopting SSL technology due to their unfamiliarity and lack of expertise in the driving and dimming requirements for LEDs.

[0005] Therefore, there is provided a novel LED Driver/dimmer for solid state lighting applications.

SUMMARY OF THE DISCLOSURE

[0006] With the wide variety of communication interface options and LED drive currents available for numerous architectural and entertainment Solid State Lighting applications, the configurable LED Driver/dimmer of the current disclosure includes at least one of the following advantages: configurable output current options that maximize the available power in the “front end” PFC and isolated power conversion converter stage; multiple drive current options for the multiple LED drive current options for various LEDs; elimination of a cooling fan which can present issues with audible noise and flexibility in where the power source is located, relatively low standby power consumption during “black out” lighting conditions, where “black out” refers to no load operation on the output of the dimmer/driver; multiple communication interface options; the ability to map output current sources/channels to different DMX512A addresses and the ability to configure multiple groups of output current sources/channels such that each group is controlled by one 0 - 10 Vdc analog signal.

[0007] Some embodiments of the present disclosure are directed to a highly efficient enclosed, configurable power source, controllable by various external communication interfaces and a method for driving and dimming LEDs or OLEDs in lighting fixtures such as used for architectural or entertainment lighting applications. Such applications can include, but are not limited to, theater, convention centers, cruise ships, architectural building features, amusement parks, museums, and hospitality lighting in restaurants and bars.

[0008] In one aspect of the present disclosure, there is provided a configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads comprising: a power circuit; a primary digital controller for controlling the power circuit; a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load; a secondary digital controller for controlling the set of output current drivers; wherein the secondary controller transmits LED control information to control outputs of the set of output current drivers; and wherein the secondary digital controller provides digital feedback control information to the primary digital controller.

[0009] In another aspect of the present disclosure, there is provided a configurable power source that provides a plurality of output channels, such as 6, 8, 9, or 12, to color change or dim OLED or LED loads. In color changing applications, the number of available channels is a multiple of three or four to accommodate either red/green/blue LED loads or

red/green/blue/amber or white LED loads. The number of output channels and available output power is increased or maximized based on the LED current requirements. The output channels are programmable by means of in circuit serial programming (ICSP) ports and calibrated by a secondary digital controller to the required output current and other parameters such as dimming frequency range.

[0010] In another embodiment, the dimming of multiple monochromatic color or white LED loads (output channels) utilizing a single 0 - 10 Vdc analog control signal, or the control of groups of LED loads (output channels) with an associated 0 - 10 Vdc analog control signal for each group is contemplated.

[0011] In another aspect of the present disclosure, the output channels are digitally controlled current sources configurable for various peak currents to power and control a variety of LEDs. The LED average current is encoded within the three variables of on-time, off-time, and period whereby no three variables are held constant. Depending on the output drive currents of the LED loads, the number of available output channels is maximized based on the maximum output power available from the power factor and isolated DC/DC converter stages.

[0012] In another aspect of the present disclosure, the configurable power source is housed in a rectangular enclosure with a monolithic aluminum extrusion and a U shaped aluminum chassis and metal end plates. Various electrical components are thermally coupled to the heatsink to increase or maximize heat transfer to the outside surface of the enclosure.

[0013] In another aspect of the present disclosure, the power source includes a digital controller to decrease power consumption of a relay coil as part of an inrush current limit circuit to reduce power consumption and improve efficiency.

[0014] In another aspect of the present disclosure, the power source utilizes an independent efficient auxiliary power source and one or more digital controllers to provide power to the communication interface. A digital controller disables various electrical circuits during black out lighting conditions to reduce no load power consumption and improve efficiency.

BRIEF DESCRIPTION OF DRAWINGS

[0015] Embodiments of the present disclosure will now be described, by way of example only, with reference to the attached Figures, wherein:

[0016] Figure 1 is a perspective view of a configurable LED Driver/dimmer;

[0017] Figures 2a and 2b are cross-sectional views of the configurable LED Driver/dimmer;

[0018] Figure 2c is a schematic view of an internal layout of the LED Driver/dimmer;

[0019] Figure 3 is a schematic block diagram of the configurable LED Driver/dimmer;

[0020] Figure 4 is a schematic diagram of a prior art inrush current limit circuit;

[0021] Figure 5 is a schematic diagram of an embodiment of a novel inrush current limit circuit for use with the configurable LED Driver/dimmer;

[0022] Figure 6 is a schematic diagram of an embodiment of an output current driver;

[0023] Figure 7 is a schematic diagram of another embodiment of the output current driver;

[0024] Figure 8 is a schematic block diagram of another embodiment of the configurable LED Driver/dimmer;

[0025] Figure 9 is a schematic diagram of a prior art multistage power source;

[0026] Figure 10 is a schematic diagram of an embodiment of a novel multistage power source; and

[0027] Figure 11 is a schematic diagram of a communication interface for use with the configurable LED Driver/dimmer.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

[0028] In general, the present disclosure is directed at a method and apparatus for providing a configurable LED Driver/dimmer. In the current description, the Driver/dimmer will be referred to as a dimmer, however, it will be understood that the configurable apparatus can function as either a driver, a dimmer or both. In the preferred embodiment, the dimmer is used for Solid State Lighting (SSL) applications.

[0029] Turning to Figure 1, a perspective view of an LED dimmer is shown. The LED dimmer 10 includes a body portion 12, or housing, which includes a monolithic aluminum heatsink 14 and a U-shaped chassis 16. Cross-sectional views of the dimmer 10 are provided in Figures 2a and 2b.

[0030] The dimmer 10 further includes a front plate 18 which includes a plurality of ports 20 along with a set of conductor cables 22. The front plate 18 is fastened to the body portion 12

via a set of fasteners 24, such as screws. In this embodiment, as conductor cables are used to provide output power to LED/OLED loads, the space requirement for the front plate 18 is reduced with respect to other known connection means such as terminal blocks.

[0031] Turning to Figures 2a and 2b, a pair of cross-sectional views of the LED dimmer are provided. Figure 2c is a schematic view of one embodiment of an internal layout of the dimmer 10. The cross-sectional views for Figures 2a and 2b are taken along lines A-A and B-B of Figure 2c respectively.

[0032] As shown, the heatsink 14 includes a receptacle portion 26 for receiving the ends of the chassis 16. In order to increase, or optimize, the heat dissipation capability of the configurable dimmer 10 at full output power, the extruded aluminum heatsink 14 includes fins 28 to increase the surface area for heat dissipation. The heatsink 14 also has a mounting platform 30 for receiving power components, or semiconductors 32, such as a bridge rectifier, MOSFETs, and/or diodes to efficiently transfer heat to the outside surface of the heatsink 14. These components will be discussed in more detail below with respect to Figure 3. A power factor inductor and main isolation transformer pair 34 are thermally coupled to the chassis 16 by a thermally conductive, electrically isolated material 36 to further improve heat dissipation of these components. A circuit board 38 is also mounted to the heatsink 14.

[0033] Turning to Figure 3, a block diagram of another embodiment of the LED dimmer is shown. The LED dimmer 10 includes an inrush current limit 40, or inrush current limit circuit, which receives power from an AC power source or supply 42, located external to the dimmer 10. The inrush circuit 40 is connected to a Power Factor Correction (PFC) Boost 44 which, in turn, is connected to a DC/DC Converter 46, or power conversion stage. The converter 46 is connected to an Output Voltage bus 48 which is connected to a power limiter 50. The inrush circuit 40, the PFC boost 44, the DC/DC converter 46, the Output Voltage bus 48 and the power limit 50 can be seen as a power circuit 47. Although only one power limit 50 is shown, it will be understood that there could be multiple power limits. The power limiter 50 is connected to a set of output current drivers 52, whereby each of the output current drivers 52 has an associated in-circuit serial programming (ICSP) port 54. The output of the output current drivers 52 is connected to individual Organic Light-Emitting Diodes (OLED)/Light-Emitting Diodes (LED) loads 56, further referred to as LED loads.

[0034] Along with the above-identified components and circuitry, the dimmer 10 further includes a primary digital controller 58 which is connected to an auxiliary power source 60 and an ICSP Port 62. The primary digital controller 58 is further connected, via an isolated communication bus 61 to a secondary digital controller 64, which receives power from the auxiliary power source 60. An ICSP port 68 is also connected to the secondary digital controller 64.

[0035] The auxiliary power source 60 is also used to power an interface component 70 which includes an optional address selector 72 and a communication interface 74. The communication interface 74 receives inputs from an external transmitter 76 and communicates via an isolated serial communication bus 78 with the secondary digital controller 64. A set of isolation barriers 80 and 81 are located within the dimmer 10, each barrier separating various components of the dimmer 10 from each other.

[0036] As will be understood, not all of the components or connections of the LED dimmer 10 required for operation are shown as they will be understood by one skilled in the art. For instance, the dimmer 10 can also include an EMI filter and a bridge rectifier. With respect to connections, it will be understood that the primary digital controller 58 can also be connected to the PFC boost 44, the inrush current limit 40 and the DC/DC converter 46 while the secondary digital controller 64 can be connected to the output voltage bus 48, the power limit 50 and the output current drivers 52.

[0037] In operation, the PFC Boost 44 and DC/DC Converter 46 are controlled by the primary side digital controller 58 while the secondary digital controller 64 monitors the output voltage bus 48 and provides digital feedback control information via isolated communication bus 61 to regulate the output voltage bus 48. Secondary digital controller 64 also translates dimming and/or color mixing information from the external transmitter 76 into LED control information for the output current drivers 52. The primary 58 and secondary 64 digital controllers and output current drivers 52 have an associated programming port for further configuring the LED dimmer 10.

[0038] Turning to Figure 4, a prior art inrush current limit is shown. In order to limit inrush current limit during initial start up of the power source, one approach is to utilize a negative temperature coefficient thermistor (NTC) in parallel with a relay contact. During initial turn on of the power source, the NTC thermistor limits the inrush current. When the PFC boost stage bulk capacitor is charged, and before the PFC stage is enabled by the primary controller, the

primary controller closes the relay contact to bypass the NTC thermistor. This is accomplished by applying a DC voltage via a switch across the coil in the relay.

[0039] A limitation of this approach is the power consumption of the relay coil when a continuous DC voltage is applied. This power consumption becomes significant in terms of Energy Star requirements during no load or standby operation such as when a “black out” or minimum light intensity state is received by the communication interface.

[0040] Turning to Figure 5, an embodiment of an improved inrush current limit 40 is shown. An EMI filter 82 is connected between the power supply and the current limit 40 and is connected directly to the PFC boost 44 and via the current limit 40. The current limit 40 includes a thermistor 84, a relay or relay contact 86 and a switch 59. The relay contact 86 is connected in parallel with the thermistor 84. A typical relay coil requires greater energy to close the contacts than is required with the currently described limiter 40 to maintain the contacts in a closed position since less holding force is required. After the relay contacts have been closed by applying a voltage of 12 Vdc, modulation of the relay coil voltage can be initiated by the primary controller 58 to effectively reduce the average voltage across the coil to approximately 5 volts versus a DC voltage of 12V, reducing power consumption. It should be noted that the pulse duty cycle and frequency can also be changed to improve or optimize performance.

[0041] In one embodiment, the primary controller 58 pulses the DC voltage across the relay coil via the switch 59 to reduce power consumption.

[0042] In one embodiment, for the PFC boost 44, as shown in Figure 3, the PFC Boost 44 utilizes a boost topology with an input AC voltage mains range of 103 Vac to 300 Vac from the AC supply 42. Energy stored in an inductor within the PFC boost 44 is transferred and stored in the bulk capacitor on a cycle by cycle switching basis at a loosely regulated 430V DC over the input range. The energy is controlled in a manner that forces AC input current to be sinusoidal and in phase with the AC line voltage. By drawing current in phase with the input mains voltage 42, the amount of harmonic currents of the fundamental AC mains frequency being introduced into the power line is reduced.

[0043] For the DC/DC convertor 46 and the output voltage bus 48, the preferred embodiment for the DC/DC converter 46 is derived from the isolated buck converter topology and comprises a galvanically isolated full bridge converter employing a primary side phase modulation technique with a secondary side current doubler rectifier circuit.

[0044] The full bridge converter parasitic circuit elements in conjunction with primary magnetization current and reflected inductor ripple current cause resonant edge switching transitions on the MOSFET switch thus forcing zero voltage across the MOSFET switching device before turn on. The result is higher efficiency due to the elimination of Coss (drain to source MOSFET Capacitance) switching losses, reduction of gate charge across the Miller capacitance and minimized power loss during switching transitions when voltage and current are changing simultaneously.

[0045] Since the output of the DC/DC converter is a tightly regulated DC bus 48, the set of power limit circuits 50 are coupled to either one or more current drivers 52 to limit the power output of each of the output current drivers. 52 The power limit circuits 50 each include a current sensor that is monitored by the secondary controller 64. In the event of a single component failure within the output current driver module, the power limit circuits 50 limit the energy to the loads in accordance with the UL standard 1310 Class 2. Supplementary protection to the power limit circuits can also include one or more fuses.

[0046] For the primary digital controller 44, the controller 44 provides digital feedback control for the PFC Boost 44 and DC/DC Converter 46. The digital feedback method for the PFC Boost 44 utilizes average current mode control with duty cycle feed forward for the inner current loop and voltage mode control for the outer control loop. The DC/DC Converter 46 utilizes voltage mode control for the digital control loop.

[0047] The primary digital controller 44 also controls the inrush current limit circuit 40, provides primary current limit protection, and over voltage protection for the output of the PFC Boost 44. The primary digital controller 44 also disables the PFC Boost 44 and the DC/DC Converter 46 during black out or no load conditions to reduce power dissipation.

[0048] With respect to the output current drivers 52, configuring the required number of outputs and required output current is accomplished by populating the appropriate sections of a single printed circuit board with the appropriate electrical components and programming the output current driver via the in-circuit serial programming (ICSP) ports 54.

[0049] Turning to Figure 6, which is an embodiment of an output current driver, the output current driver 52 comprises a load controller 90, a current source 92, and current sense 94. Although only one current driver 52 is shown, it will be understood that multiple are present as reflected in Figure 3.

[0050] The output current driver utilizes the dimming/color mixing techniques for LEDs described in detail in US Patent Publication No. 2007/0103086, which is hereby incorporated by reference, wherein the LED average current is encoded within the three variables of on time, off time, and period where by no three variables are held constant.

[0051] The secondary controller 64 receives dimming or color mixing information in the form of a serial data stream from the external transmitter 76 via the communication interface 74 and then translates the data stream into LED control information. The LED control information is transmitted to the load controller 90 in the form of instructions to generate a digital signal 98 and an analog signal 100.

[0052] The load controller 90 further comprises a signal generator 102 which transmits the digital signal 98 and the analog signal 100 to the current source 92. The digital control signal 98 and the analog signal 100 are preferably generated via a digital control algorithm and a 1 Bit algorithm, respectively.

[0053] The current source 92 preferably includes ancillary circuitry for operation and comprises a buck topology power stage with hysteretic control. The current sense 94 provides a digital feedback loop for each current source 92. In the preferred embodiment, the current source 92 is a buck circuit topology however other embodiments can include topologies such as boost, buck-boost, or single ended primary inductor converter (SEPIC).

[0054] Output 104 of the current driver 52 provides a current pulse via current source 92 to the LED Load 56 whereby on times, off times, and period are not held constant.

[0055] Each output current driver 52, has an associated in-circuit serial programming (ICSP) port 54. The ICSP port 54 provides access to the load controller 90 such that firmware updates are possible to permit the configuration of the output current drivers 52. The ICSP port(s) 54 for the output current driver(s) 52 can be located on the printed circuit board assembly of the apparatus or they can be located on the outside of the enclosure.

[0056] The configuration options include, but are not limited to, such parameters as the adjustment of the frequency range of the dimming current pulse for the range of light intensity output or the set point adjustment of the peak on time output current.

[0057] For example, it might be necessary to increase the frequency range of the dimming current pulse in video recording applications where the dimming current pulse frequency can be programmed for a 2000Hz to 2500Hz range. This would negate a visible beat frequency effect that would other wise be noticeable on recorded video. There can be other applications

where the adjustment of the dimming current frequency range is required to reduce EMI effects.

[0058] The default peak output current set point is programmed via the ICSP port 54 which provides flexibility in the number of possible LEDs types that can be driven and is typically dependent on the recommended operating current specified by the manufacturer such as 350mA, 700mA, etc. The set point current is preferably programmed to within 4% of the manufacturer's specification. The peak output current set point can then be precisely calibrated to within typically 1% via the secondary controller 64 during factory calibration.

[0059] An alternate embodiment of an output current driver 52 is shown in Figure 7. In this embodiment, the output current driver 52 comprises a load controller 110 including a signal generator 112. A current source 114 and a current sense 116 are located within an apparatus 118, such as a light fixture. The light fixture 118 also includes the LED load 56. After receiving the LED control information from the secondary controller 64, the signal generator 112 provides a data signal to the light fixture 118 to operate the LED load 56 via the current source 114 and the current sense 116. This is also schematically shown in Figure 8.

[0060] Figure 8 is a schematic diagram of an alternate embodiment of a configurable LED dimmer 10. As shown, individual current sources 114 and current senses 116 are mounted in the light fixture containing the LED load 56, and power and data signals are provided to each output current source 114 by the multi conductor cable 22. In this embodiment, the current sources 114 are configured to regulate to a predetermined peak current. The load controller 110 transmits the data signal containing the output current information encoded within the three variables of on time, off time, and period whereby no three variables are held constant.

[0061] Turning to Figure 9, a known application of internal auxiliary power requirements in a multistage power source is shown and illustrates how auxiliary power is provided to the various blocks of a multistage power source. P1, P2...P10 represents the various power and voltage transfer requirements for each functional block. For simplicity, the various voltage regulator and filter circuits required for each of the power outputs have been omitted.

[0062] In operation, the bridge rectifier converts the AC mains voltage P1 to a rectified voltage P2. A portion of power P6 from the output of the bridge rectifier P2 is supplied to the start up circuit. The start up circuit is comprised of a power transistor or MOSFET and is

intended to provide power P8 to the PFC analog controller for only a short duration of a few seconds. Power P8 to the PFC analog controller will allow the PFC Boost stage to begin switching, providing power P10 to the DC/DC controller, and power P3 to the DC/DC converter power stage. Since the start up circuit dissipates an excessive amount of power, it is turned off by the voltage component of P7 supplied by the PFC boost stage. The P7 power is permitted to 'flow through' the start up circuit to continue to supply power P8 to the PFC analog controller.

[0063] The output of the DC/DC Analog Converter provides power P4 to the multi output voltage bus, power P9 to the Communication Interface, and the Output Current Drivers by means of P5.

[0064] In this implementation, the PFC and DC/DC Controllers are typically analog controllers. It should be noted that in this implementation, in order for the communication interface to continually receive dimming information from an external transmitter, the DC/DC Converter stage must remain turned on. Similarly, in order for the DC/DC converter stage to provide power P4, the PFC Boost stage must remain on.

[0065] In a 'black out' state, the communication interface may receive a "0" intensity value out of 255 intensity levels for all of its output current drivers via the external transmitter such as a DMX512A or RDM controller interface, or it may receive an analog voltage of between 0 to 1V via a controller compliant to ESTA E1.3-2001 or IEC60929 as one of many communication interface options. In this 'black out' state, the DC/DC Converter and PFC Boost Stage continue to dissipate an excessive amount of power.

[0066] Figure 10 is directed at an embodiment of an improved internal auxiliary power distribution in a multistage power source for providing auxiliary power to the various blocks of a multistage power source. For simplicity, the various voltage regulator and filter circuits required for each of the power outputs have been omitted. The transfer of power from AC mains to the Output Current Drivers (52) is unchanged. This embodiment shows an improved implementation of an independent auxiliary power source providing power to the primary digital controller 58, the secondary digital controller 64, and the communication interface 74. The auxiliary power source 60 comprises an efficient isolated flyback topology with a wide input voltage range and pulse skipping capability to minimize its power dissipation at light loads or no load conditions. In other words power can be provided to the primary digital

controller 58, the secondary digital controller 64, and the communication interface 74 via an auxiliary flyback converter.

[0067] A 'black out' state received from the external transmitter 76 to the communication interface 74 is communicated to the secondary digital controller 64 and then the primary digital controller 58 via the isolated communication bus 66. The primary digital controller 58 then disables the PFC Boost Stage 44 and DC/DC Converter Stage 46 reducing overall power dissipation of the configurable power source.

[0068] It should be noted that even when the PFC Boost 44 is disabled, power can continue to be supplied to the auxiliary power source 60 since rectified voltage from a bridge rectifier 120 can continue to peak charge the PFC boost 44 through an internal capacitor via the boost diode.

[0069] The auxiliary power source 60 continues to provide power to the primary digital controller 58, secondary digital controller 64, and communication interface 74 in order to be able to 'listen' for or sense a change in light intensity state that may be communicated by the external transmitter 76.

[0070] Alternate embodiments can include additional ancillary circuits that can be powered by the independent auxiliary power source that can be disabled by a controller to reduce over all power dissipation in black out or no load conditions.

[0071] With respect to the communication interface 74, the communication interface 74 comprises a removable and interchangeable module with each module adapted for different control options such as DMX512A, RDM, 0 - 10 Vdc and Zigbee. Operation of the communication interface with such control options will be understood by one skilled in the art.

[0072] The communication interface module receives lighting control information via the external transmitter 76 and converts the various protocols into a serial data stream. It then transmits this data by means of a Universal Asynchronous Receiver Transmitter (UART) to the secondary digital controller 64 via the isolated serial communication bus 78. The isolated serial communication bus 78 is comprised of a isolation barrier 82 to "float" the communication interface and prevent ground loops.

[0073] Turning to Figure 11, an embodiment of the communication interface is shown. In this embodiment, an analog interface module adapted for 0 - 10 Vdc IEC60929 or ESTA E1.3-2001 dimming methods as the communication interface 74 is shown. The analog interface module can be adapted to receive one or more analog control voltages from one or

more associated external transmitters 76. The external transmitter 76 is preferably an electronic resistor or potentiometer that sinks current from the current source located on the analog interface module and outputs a variable 0 - 10 Vdc control voltage proportional to the required light intensity.

[0074] Individual external transmitters 76 supply signals to various controls 122 within the communication interface 74. Each control 122 is representative of an area or group of LED loads 56. Within each control 122 is a current source 124, a voltage sensor 126 and a differential amplifier 128. The differential amplifier 128 senses a voltage across the voltage sensor 126 and converts this into a correlated voltage ($V_m, V_1, V_2 \dots V_n$) supplied to a controller 130. The controller 130 converts this analog voltage into a serial data stream for transmission to the secondary digital controller 64 via the isolated serial communication bus 78.

[0075] The communication interface 74 can be configured to have one 0 – 10 Vdc control voltage simultaneously control via the secondary digital controller 64, all output current drivers 52 and LED loads 56. This application is beneficial in monochromatic color or white lighting applications since only one control signal and associated wiring is required to control multiple light loads.

[0076] Furthermore, the communication interface 74 can be adapted to have one or more 0 - 10 Vdc signal voltages control an associated group of one or more output current drivers in zonal dimming applications. An optional master 0 - 10 Vdc signal voltage could be able to simultaneously control all of the individual groups of output current drivers.

[0077] In applications not requiring the complexity of DMX512A, these analog control options are beneficial in red/green/blue or red/green/blue/amber color changing or monochromatic color or white light applications whereby the addressability and corresponding control of individual LED light loads is not required.

[0078] With respect to the secondary digital controller 64, the controller 64 monitors and transmits digital output voltage bus information (feedback loop) via the two way isolated serial communication bus 78, decodes the serial data from the communication interface 74, and transmits control information to the output current drivers 52. As a protection feature, the secondary controller 64 also monitors output currents from the power limit stages 50 supplied to the output current drivers 52

[0079] The secondary digital controller 64 includes the ICSP port 68 to program and calibrate the output voltage bus 48 to the required voltage. In DMX512A applications, the ICSP port 68 also allows for the mapping of each of the output channels to a wide variety of addresses. Similarly, in 0 - 10 Vdc analog control applications, the secondary digital controller ICSP port allows for the mapping of output channels into groups for each associated 0 - 10Vdc control signal.

[0080] This mapping capability is particularly useful in addressable-networked lighting systems using a DMX512A control protocol where different lighting zones are required to respond to different illumination information. For example, in a 12 channel output configuration, the first 6 channels could be mapped to the DMX base address of the power source (i.e. DMX01) and the last 6 channels could be mapped to DMX address +1 (i.e. DMX02).

[0081] This mapping capability is also useful in zone dimming applications using 0 - 10 Vdc analog controls as the communication interface. For example, a 12 channel output LED dimmer configuration can have 7 output channels grouped for a first associated 0 - 10 Vdc signal, the next 3 channels can be grouped to a second associated 0 - 10 Vdc control signal, and the last 2 channels can be grouped to a third associated control signal.

[0082] Embodiments of the disclosure can be represented as a software product stored in a machine-readable medium (also referred to as a computer-readable medium, a processor-readable medium, or a computer usable medium having a computer-readable program code embodied therein). The machine-readable medium can be any suitable tangible medium, including magnetic, optical, or electrical storage medium including a diskette, compact disk read only memory (CD-ROM), memory device (volatile or non-volatile), or similar storage mechanism. The machine-readable medium can contain various sets of instructions, code sequences, configuration information, or other data, which, when executed, cause a processor to perform steps in a method according to an embodiment of the disclosure. Those of ordinary skill in the art will appreciate that other instructions and operations necessary to implement the described disclosure can also be stored on the machine-readable medium. Software running from the machine-readable medium can interface with circuitry to perform the described tasks.

[0083] The above-described embodiments of the disclosure are intended to be examples only. Alterations, modifications and variations can be effected to the particular embodiments

by those of skill in the art without departing from the scope of the disclosure, which is defined solely by the claims appended hereto.

What is claimed is:

1. A configurable light emitting diode (LED) driver for powering a set of light fixture loads comprising:
 - a power circuit including:
 - an inrush current limit,
 - an apparatus for power factor correction and DC/DC conversion, and
 - a regulated output voltage bus connected to the apparatus for power factor correction and DC/DC conversion;
 - a primary controller for controlling the power circuit;
 - a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for powering the connected light fixture load; and
 - an apparatus for mapping the set of output current drivers to various dimming zones and for mapping output channels into groups.
2. The LED driver of claim 1 wherein the apparatus for mapping comprises:
 - a secondary controller; and
 - a port for mapping the output channels into groups.
3. The LED driver of claim 2 wherein the output channels are mapped for DMX512A control.
4. The LED driver of claim 2 wherein the output channels are mapped for 0-10 Vdc analog control.
5. The LED driver of claim 1 further comprising a communication interface for receiving data from an external transmitter.
6. The LED driver of claim 5 wherein the communication interface is DMX512A, 0-10 Vdc analog control, Zigbee wireless or remote device management (RDM) compatible.

7. The LED driver of claim 2 further comprising a communication interface for receiving data from an external transmitter.
8. The LED driver of claim 7 wherein the communication interface includes a universal asynchronous receiver/transmitter (UART) to transmit data to the secondary controller.
9. The LED driver of claim 7 further comprising an auxiliary flyback converter to provide power to the primary controller, the secondary controller, and the communication interface.
10. The LED driver of claim 9 wherein the primary and secondary controllers are digital controllers.
11. The LED driver of claim 1 wherein the light fixture load is one of an Organic LED (OLED) load or an LED load.
12. The LED driver of claim 11 wherein the primary and secondary controllers are digital controllers.
13. The LED driver of claim 1 further comprising a housing with a heatsink portion for housing the components of the LED driver.
14. The LED driver of claim 13 wherein the heatsink comprises fins.
15. The LED driver of claim 1 wherein the apparatus for power factor correction and DC/DC conversion comprises:
 - a DC/DC converter; and
 - a power factor correction (PFC) boost connected to the inrush current limit and the DC/DC converter.
16. The LED driver of claim 15 further comprising at least one power limit connected to the regulated output voltage bus.

17. The LED driver of claim 1 further comprising a set of isolation barriers to separate components of the driver from each other.
18. The LED driver of Claim 1 wherein each of the set of output current drivers comprises:
 - a load controller;
 - a current source; and
 - a current sense.
19. The LED driver of Claim 18 wherein the load controller comprises a signal generator.
20. The LED driver of Claim 2 wherein the port is an in-circuit serial programming (ICSP) port.

ABSTRACT

The disclosure is directed at a configurable light emitting diode (LED) driver/dimmer for controlling a set of light fixture loads comprising: a power circuit; a primary digital controller for controlling the power circuit; a set of output current drivers, each of the set of output current drivers connected to one of the set of light fixture loads for controlling the associated light fixture load; a secondary digital controller for controlling the set of output current drivers; wherein the secondary controller transmits LED control information to control outputs of the set of output current drivers; and wherein the secondary digital controller provides digital feedback control information to the primary digital controller.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: LUMASTREAM CANADA ULC

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: CONFIGURABLE LED DRIVER/DIMMER FOR SOLID STATE LIGHTING APPLICATIONSLUMASTREAM CANADA ULC, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: TIKKANEN, David; NEUDORF, Jason; LYONS, Steven; HATHAWAY, Kyle To: ELECTRONIC CRAFTSMEN CORPORATION

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: ELECTRONIC CRAFTSMEN CORPORATION To: E CRAFTSMEN CORPORATION

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)3. From: E CRAFTSMEN CORPORATION To: LUMASTREAM CANADA ULCThe document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.☐ Additional documents in the chain of title are listed on a supplemental sheet(s).☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jeffrey W. Wong/

Signature

Jeffrey W. Wong

Printed or Typed Name

2015-01-15

Date

Agent, Reg. No. 46414

Title or Registration Number