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Agenda Item: **HSDPA**
Source: **Motorola**
Title: **A New Hybrid-ARQ Scheme Using Incremental Redundancy**
Document for: **Discussion and Decision**

1.0 Introduction

It was agreed at RAN1#21 that the HS-DSCH coding and modulation scheme should permit the use of incremental redundancy (IR), but also that terminal memory requirements should be derived based on Chase (soft) combining at the maximum data rate defined by the associated UE capability parameters. In order to support incremental redundancy as a form of ARQ combining, a single, unified puncturing scheme is necessary, which not only allows flexibility in choosing coding rates for the initial and subsequent transmissions, but also minimizes UE complexity and implementation engineering effort.

Conventional means of defining a puncturing pattern, such as the rate matching algorithm of Release ’99 [2] or alternatively a classical code puncturing matrix are unable to provide the necessary smooth and flexible transition between coding rates and hence obtain the benefits that IR has to offer when permitted by the UE. Current proposals such as [8] reflect this in their inability to offer full IR transmission except under highly constrained conditions.

In this contribution a simple IR scheme based on block interleaving and symbol priority mapping is proposed. The proposed scheme has the following attributes:

- flexible and fine-grained support of predefined redundancy versions at each transmission with progressive reduction in effective coding rates,
- support for Full and Partial forms of both Chase combining and IR
- re-use of a significant number of symbol interleaving and permuting structures from the Release 99 specification, with associated reduction in UE engineering effort, and
- support for systematic bit priority mapping onto the most reliable QAM constellation component bits.

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Simulation results are presented for the proposed scheme and compared with other schemes, such as IR based on puncturing matrices, symbol re-mapping, etc., in a companion paper [7].

2.0 Hybrid ARQ with Full IR (Proposed Scheme)

The proposed scheme closely follows the modulation and coding reference model agreed at RAN1#21, as shown in Figure 1.

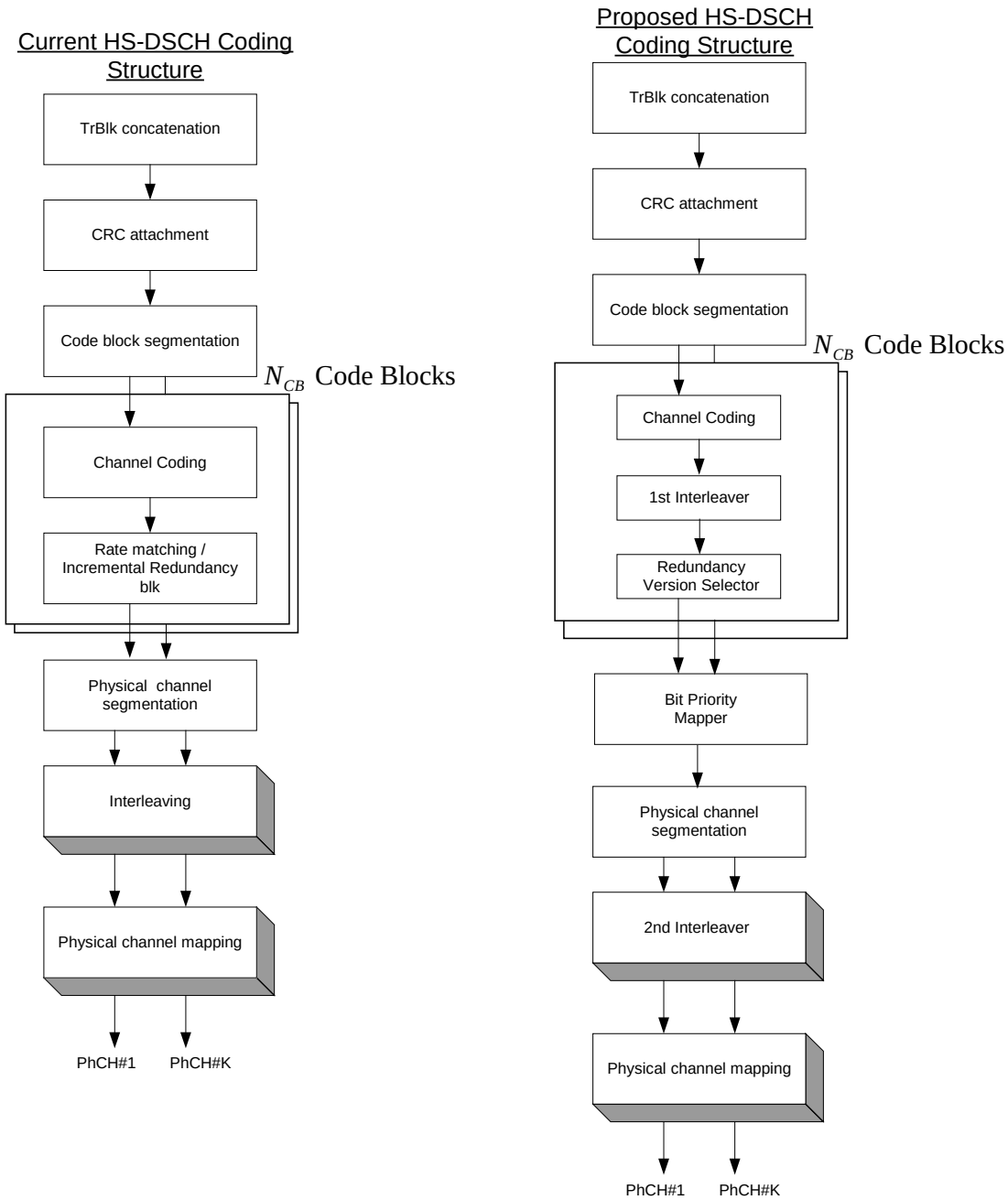

Figure 1 - Reference channel coding model for HSDPA.

The transport block concatenation, CRC attachment, and code block segmentation functions are identical to those defined for Release '99. Channel coding also proceeds according to the Release '99 rate-1/3 turbo-encoder function specification. The rate matching and incremental redundancy functionality is implemented in two units, however – specifically the 1st Interleaver and Redundancy Version Selector, and these are described next.

2.1 1st Interleaver

In the proposed puncturing scheme, the un-punctured codeword bits are separated into a "Systematic" and a "Parity" stream denoted by $x_{S,k}, x_{P,k}\ k \in \{1, \cdots, N_{\text{info}}\}$ respectively where $x_{S,k} \in \{0,1\}$ and $x_{P,k} \in \{\{0,0\},\{0,1\},\{1,0\},\{1,1\}\}$, $x_{P,k} = \{p_{1,k}, p_{2,k}\}$ as shown in Figure 2. Each stream is read into an $N_{row} \times N_{col}$ block matrix interleaver while the tail bits are buffered separately and are later appended onto the unpunctured instantaneous codeword[1]. The number of rows in each interleaver, N_{row} is always fixed at 30 while the number of columns, N_{col} is variable (dependent on the number of information bits N_{info}) and is determined in exactly the same manner as the turbo code internal interleaver defined for Release '99 in step 2 of section 4.2.3.2.3.1 of 25.212 [2].

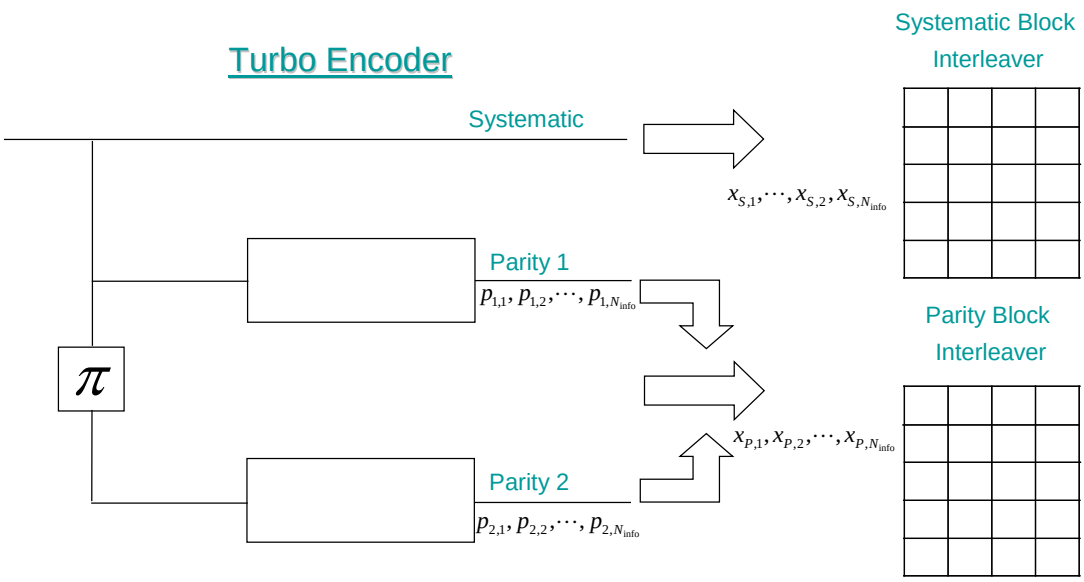

Figure 2 - Entering codeword into puncturing matrices

Data is read in a column-wise fashion from right-to-left into each interleaver as shown in Figure 3, with dummy bits padded if $N_{\text{info}} < N_{col} \times N_{row}$, where $y_{i,k} = x_{i,k}$ for

[1] Where the "instantaneous codeword" is the codeword transmitted in a specific TTI

$k = 1, 2, \cdots, N_{\text{info}}$ and $y_{S,k} \in \{0,1\}$, $y_{P,k} \in \{\{0,0\},\{0,1\},\{1,0\},\{1,1\}\}$ for $k = \{N_{\text{info}} + 1, \cdots, N_{row} \times N_{col}\}$. These dummy bits are later pruned away when reading the codeword data row-wise from top-to-bottom out from the matrix similar to section 4.2.3.2.3.3 of Release '99 25.212 [2].

To facilitate flexibility in supporting variable coding rates, both columns and rows are permuted prior to reading out of the block matrix contents. As an example of the benefit of row and column reordering, consider the case where $N_{row} = 30$ and $N_{col} = 100$. If the first two rows were to be read out, then without reordering the codeword bits would correspond to the 29th, 30th, 59th, 60th, 89th, 90th, ... stages in the encoder trellis. However, by swapping row 29 with row 15, then the transmitted codeword bits become those at the 15th, 30th, 45th, 60th, 75th, 90th, … stages in the encoder trellis, a more homogenous and therefore desirable distribution. In permuting the columns, we ensure no sub-block section of the trellis is neglected when only a portion of a row is read out to form the transmitted codeword. The same row permutation is proposed for both the systematic and parity interleavers and is that defined by Table 7 in section 4.2.11 in 25.212 [2]. On the other hand, different column permutations, given in the appendix, are proposed for each interleaver and are derived directly from the intra-row permutations of the Release '99 Turbo code internal interleaver defined in section 4.2.3.2.3.2 in 25.212 [2].

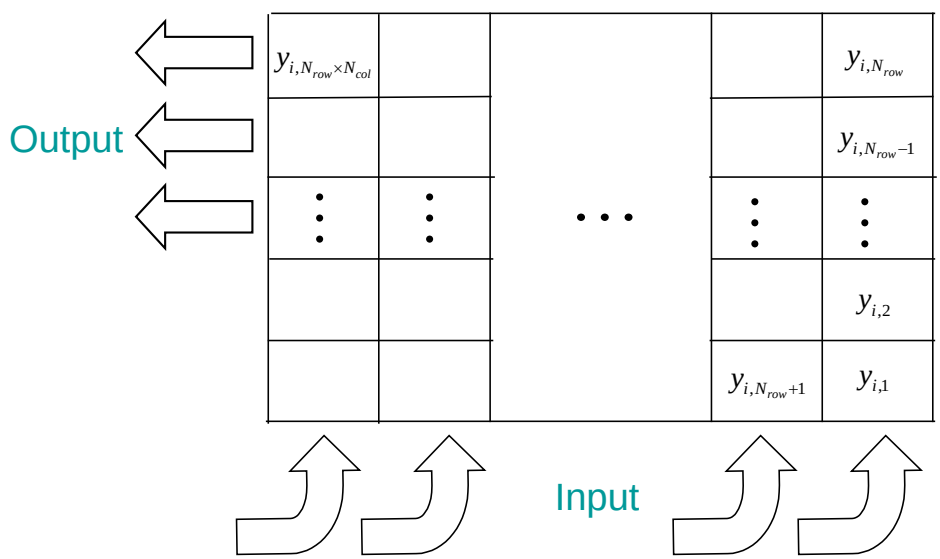

Figure 3 - Column-wise insertion, row-wise extraction

After row and column permutation, the desired number of codeword bits can then be read out in row-wise fashion. Using the notation of Figure 2, if the desired number of parity bits is an odd number and if $x_{P,k} = \{p_{1,k}, p_{2,k}\}$ is the last symbol read from the Parity interleaver, then the parity bit $p_{1,k}$ is used as a codeword bit while the parity bit $p_{2,k}$ is discarded.

In the case of the Parity interleaver the maximum number of rows that can be transmitted $N_{\mathrm{P,max_row}}$ may be less than N_{row} for the Parity interleaver due to UE memory restrictions, while for the Systematic interleaver $N_{\mathrm{S,max_row}}$ is always equal to N_{row}. Following the approach of [6], let N_{SML} denote the total number of Soft Metric Locations (SML's) provisioned at the UE, N_{tail} denote the number of tail bits per code block and N_{ARQ_proc} denote the number of ARQ processes currently defined in the UE, then $N_{\mathrm{P,max_row}}$ is given by;

$$N_{\mathrm{P,max_row}} = \min\left(\left\lfloor \frac{N_{SML}}{2\times N_{CB}\times N_{col}\times N_{ARQ_proc}} - \frac{N_{row}}{2\times N_{CB}} - \frac{N_{tail}}{2\times N_{col}\times N_{CB}} \right\rfloor, N_{row}\right) \quad (1.1)$$

Note that all the independent variables in equation (1.1) are derivable at the UE following delivery of the signaled HARQ information on the HS-DSCCH. When more coded bits are required than can be obtained by reading to the end of the $N_{\mathrm{i,max_row}}$ th row, $i \in \{S, P\}$, reading may continue by wrapping around to the beginning of the first row of the same or a different interleaver. One consequence of which is to allow coding rates less than 1/3. Once the desired number of codeword bits is read from both block interleavers, the buffered tail bits are then appended completing the desired instantaneous codeword.

2.2 Redundancy Version Selector

As the number of codeword bits read out from the Systematic and Parity block interleaver may differ, the proposed framework allows for both chase and IR coding schemes. In order to support different redundancy versions, any row may be assigned as a starting point at which to commence reading. The preferred approach is to pre-define a static set of eight redundancy versions. Each redundancy version j contains a starting row α_j in either the "Systematic" or "Parity" interleaver (i.e. $\alpha_j \in \{i, k\}$, $j \in \{0, \cdots, 7\}$, $i \in \{S, P\}$, and $k \in \{1, \cdots, N_{i,\max_\mathrm{row}}\}$). Coded bits are read from the selected starting row until either the desired number of bits has been read or the end of the $N_{i,\max_\mathrm{row}}$ th row is reached. In the case the end of the $N_{i,\max_\mathrm{row}}$ th row is reached, reading then continues from the first row of the other interleaver as shown in Figure 4. Starting rows are computed such that they are equally spaced throughout the lowest rate codeword supported by the UE. The procedure for their computation is as follows;

- $N_{vr} = N_{S,\max_\mathrm{row}} + 2\times N_{P,\max_\mathrm{row}}$
- $VR_j = \left\lfloor \frac{j\times N_{vr}}{8} \right\rfloor - j,\ j \in \{0,....,7\}$

- $$\alpha_j = \begin{cases} \{S, VR_j\} & \text{if } VR_j < N_{S,\max_row} \\ \left\{P, \left\lfloor \dfrac{VR_j - N_{S,\max_row}}{2} \right\rfloor\right\} & \text{otherwise} \end{cases}$$

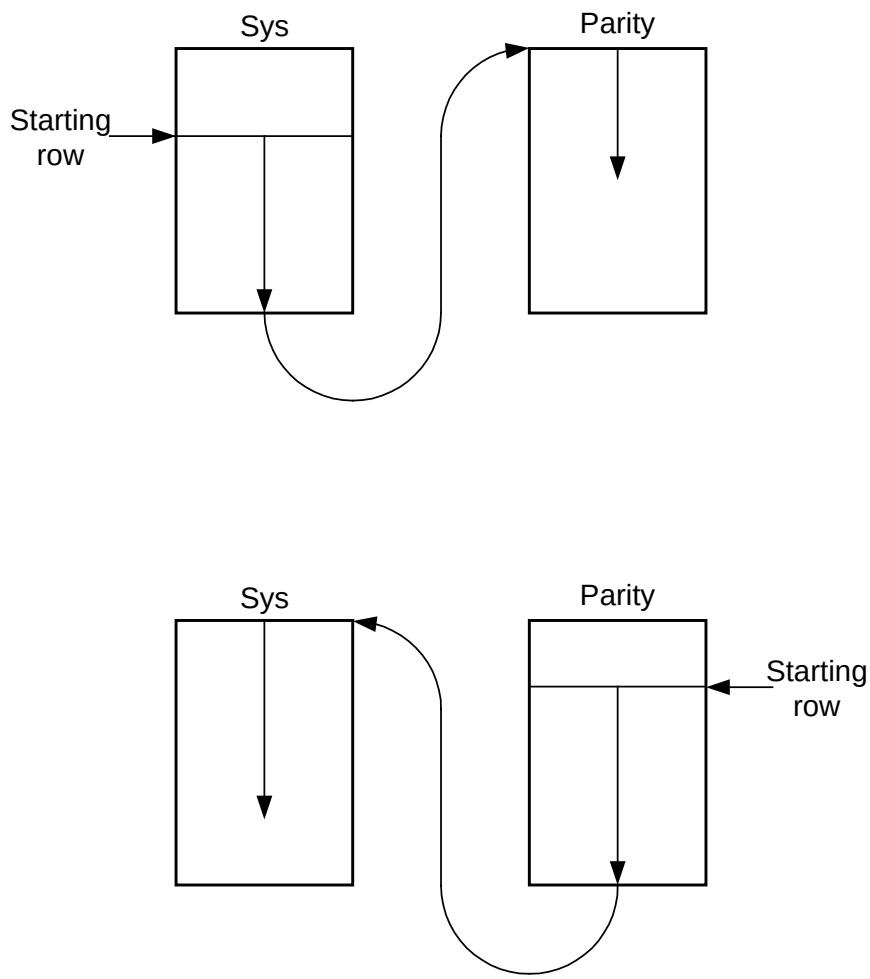

Figure 4 - Redundancy version wrap around

One aspect of these redundancy versions in this proposal is that their numbering does not suggest a particular order of transmission. For example, if the lowest supported coding rate by the UE for a particular transmission is 1/3 then the redundancy versions shown in Figure 5 apply. If on the first transmission RV_0 is signaled with enough codeword bits to result in a rate 3/5 code (all systematic bits and first 10 rows of parity interleaver transmitted), the scheduler is permitted choose RV_5 for the second transmission. Similarly, if in the first transmission a rate ¼ code with RV_0 is selected (both interleavers transmitted with Systematic interleaver repeated), RV_3 might be selected for the second transmission.

Using this simple approach the selected redundancy version sequence adjusts naturally to support Chase, partial and full IR schemes.

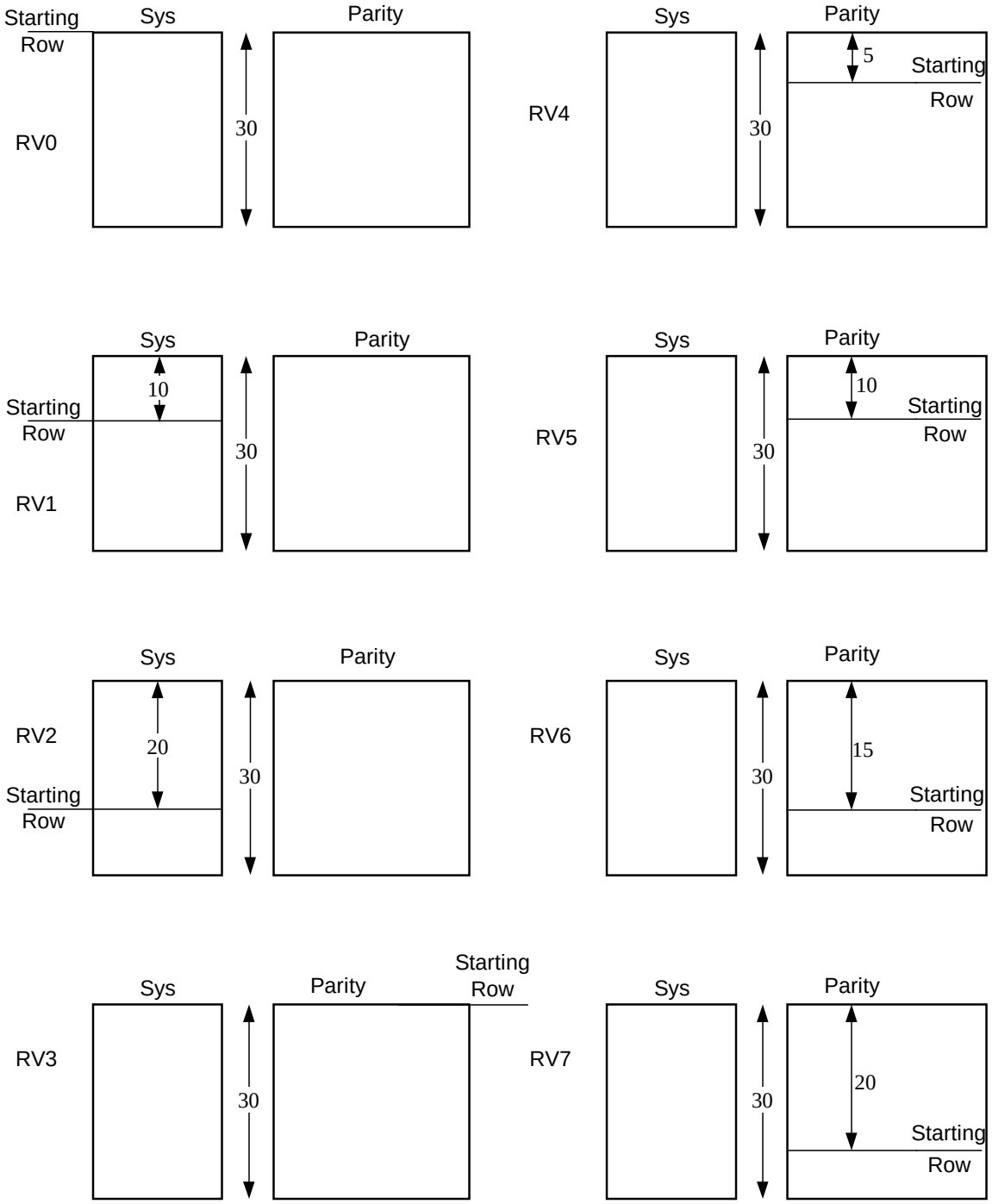

Figure 5 Redundancy versions for rate 1/3

2.3 Bit Priority Mapper

The next element in the proposed encoding chain is the Bit Priority Mapper (BPM). The performance of the IR scheme can be further improved by taking advantage of priority bit mapping. Priority bit mapping is based on utilizing the differing bit reliability offered by higher order constellations (16-QAM or higher) [4][5]. It is well known that systematic portions of a turbo codeword are of greater importance to decoder performance than the parity portions. It naturally follows that system performance can be further improved by placing systematic bits in positions of high reliability if a high order constellation is used. The symbol mapping is dependent on the type of modulation and the number of systematic and parity bits used in transmission. As an example, if redundancy version 0 is used with an effective code rate of ¾ and 16-QAM modulation, each QAM symbol comprises of 3 systematic bits and 1 parity bit while if the same version is used with a code rate of ½ and 16 QAM modulation, each QAM symbol then comprises of 2 systematic and 2 parity bits.

Figure 6 show an example of the proposed priority bit mapping for the case of 16-QAM modulation where a grouping of four bits is used to define one symbol. Here, the four bits are denoted i_1, q_1, i_2, q_2 with bits i_1 and q_1 offering greater reliability than bits i_2 and q_2 due to the nature of the constellation [5]. In Figure 6 codeword bits are taken from the Systematic and Parity puncturing block interleavers and read into the BPM array. The number of rows N_{row_BPM} of the BPM array is equal to $\log_2(M)$ where M is the constellation order or $N_{row_BPM} = 4 = \log_2(16)$ in the case of 16-QAM. The number of columns is $N_{col_BPM} = 480 \times K$ where K is the number of physical channels as shown in Figure 1 and 480 is the number of modulated symbols on each channel.

Consecutive systematic codeword bits are read code block wise and then from left-to-right row-wise into the BPM array as shown in Figure 6. Once all systematic codeword bits have been read in, parity codeword bits are read in again in code block wise fashion and then from left-to-right row-wise. The output of the BPM is a sequence of QAM symbols or bit vectors (a vector of 4 bits in the case of 16-QAM and a vector 2 bits in the case of QPSK) given by the columns of the BPM array, read in sequence from left-to-right. It is well known that alternately reversing codeword bit reliability during re-transmissions results in further performance improvements [5]. The same principle can also be applied to the BPM by reversing the sequence of high and low priority bits, incurring the extra bit required to signal this reversal to the UE.

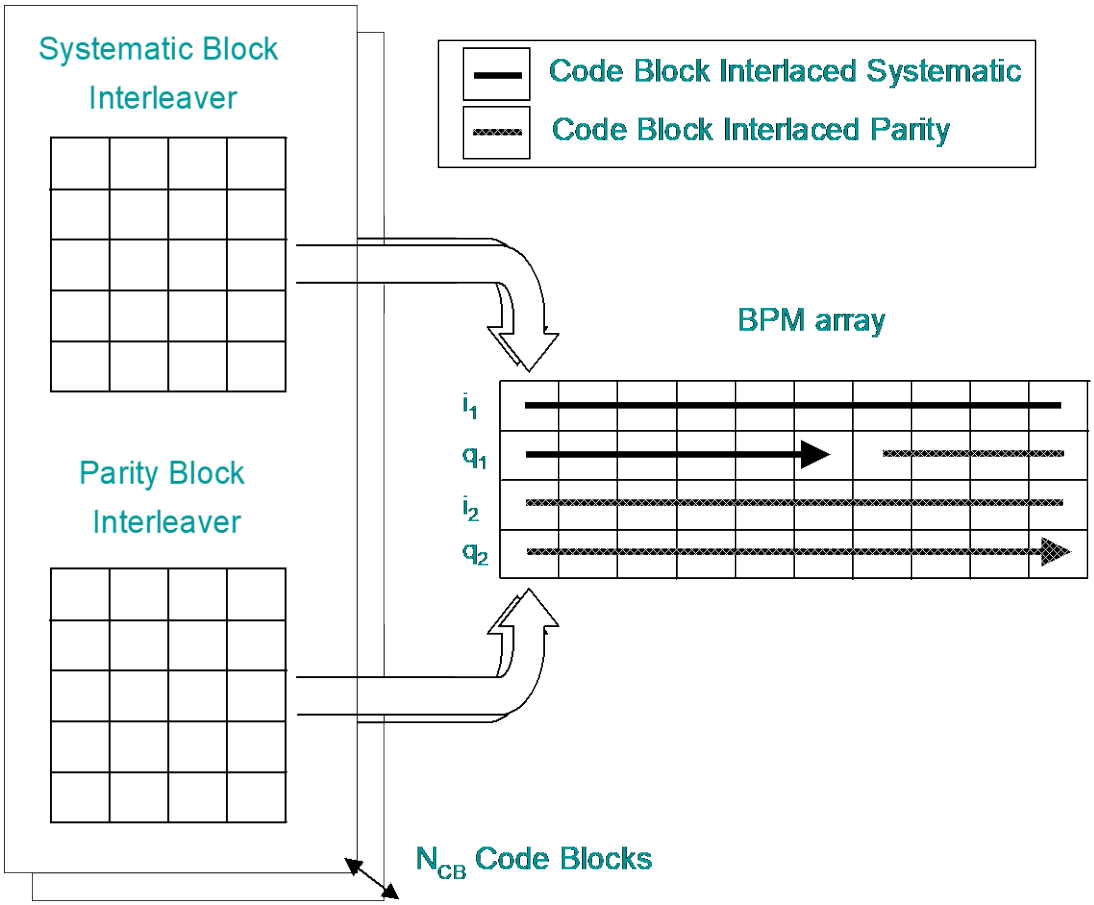

Figure 6 – Bit priority mapping for 16-QAM

2.4 Physical Channel Segmentation

Next, the physical channel segmentation algorithm given in section 4.2.10 of 25.212 [2] is used with a slight modification. Instead of applying the algorithm on bits, it is applied on the QAM symbols/bit vectors output from the Symbol Mapper described in the previous section.

2.5 2nd Interleaver

Following channel segmentation, the 2nd interleaving described in section 4.2.11 in 25.212 [2] is applied, again with a slight modification. Instead of applying the interleaver on the bits comprising each physical channel, it is applied on the QAM symbols values or symbol indices of each of the physical channel which are output from the physical channel segmentation module. Given the prior use of the Interleaving Unit above, the term '2nd Interleaver' is retained.

2.6 Physical Channel Mapping

Finally, the physical channel mapping described in section 4.2.12 of 25.212 [2] is applied, again with substitution of QAM data symbols for bits.

2.7 Bit Requirements to support the scheme

Table 1 shows the bit requirement to support HARQ operation for the proposed IR scheme. It may be noted that a total of 8 bits is required to support the scheme. However, the number of bits can be easily reduced to 7 if the number of redundancy versions is reduced by a factor of 2.

Table 1. Bit Requirements to support HARQ

Parameter	**HS-SHCCH**		
	Min	**Prop**	**Max**
FHARQ channel#	3	3	3
FHARQ IR bits	3	4	4
FHARQ new packet	0	1	2
Total	6	8	9

3.0 Conclusions

A generalized high performance and flexible IR scheme has been proposed. It is recommended that this scheme be adopted for 3GPP HSDPA.

4.0 References

[1] "Liaison statement on progress with HSDPA", R1-01-0945

[2] 3GPP TS 25.212-v3.5.0, "Multiplexing and channel coding (Release 99)"

[3] 3GPP TR 25.858 v 0.0.4

[4] Samsung, "Simulation Results of Chase Combining with Symbol Mapping based on Bit Priority", R1-01-0739

[5] Panasonic, "Enhanced HARQ method with Signal constellation rearrangement", TSG-RAN1-(01)0237, Las Vegas, Feb. 2001

[6] Motorola, "UE Capabilities for HS-DSCH", R1-01-1016

[7] Motorola, "Performance Comparison of various IR schemes," R1-01-1015

[8] Siemens, “Further Results on the Adaptation of Rate Matching for HSDPA”, TSG-RAN1-(01)0953, Turin, Italy, Aug. 2001

[9] Motorola, “A new HARQ scheme using IR-Rev0,” R1-01-1014

5.0 Appendix

Column permutation:

1. Select a primitive root v from table 2 in section 4.2.3.2.3.1 in [2], which is indicated on the right side of the prime number p.
2. Construct the base sequence $\langle s(j)\rangle_{j\in\{0,1,\cdots,p-2\}}$ for column permutation as;

$$s(j)=\left(v\times s(j-1)\right)\bmod\ p,\ j=1,2,\cdots,(p-2),\ \text{and}\ s(0)=1$$

3. Assign $q_S=1$ to be prime integer associated with the Systematic interleaver and determine q_P ,the prime integer associated with the Parity interleaver to be a least prime integer such that $g.c.d\left(q_P,p-1\right)=1,\ q_P>6$, where g.c.d. is greatest common divisor.

4. Perform the column permutation for the ith interleaver, $i\in\{S,P\}$ as

   If $(C=p)$ then

   $$U_i(j)=s\left(\left(j\times q_i\right)\bmod\left(p-1\right)\right),\ j=1,2,\cdots,(p-2),\ \text{and}\ U_i(p-1)=0,\ i\in\{S,P\},$$

   where $U_i(j)$ is the original bit position of the j-th permuted bit of the i-th interleaver.

   end if

   If $(C=p+1)$ then

   $$U_i(j)=s\left(\left(j\times q_i\right)\bmod\left(p-1\right)\right),\ j=1,2,\cdots,(p-2),U_i(p-1)=0\ \text{and}\ U_i(p)=p,$$

   $i\in\{S,P\}$,

where $U_i(j)$ is the original bit position of the j-th permuted bit of the i-th interleaver

end if

If $(C = p-1)$ then

$$U_i(j) = s\left(\left(j \times q_i\right) \bmod \left(p-1\right)\right) - 1,\ j = 1, 2, \cdots, \left(p-2\right),\ i \in \left\{S, P\right\},$$

where $U_i(j)$ is the original bit position of the j-th permuted bit of the i-th interleaver.

end if