

Development of a CDMA System with Rake Receiver for the Third Generation Wireless Communication Systems

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ABSTRACT

The main constituent of the third generation (3G) digital cellular mobile communication systems is a CDMA transceiver. The transmitter includes complex scrambling code generation, channelization code generation, and the spreading operation with both. The receiver involves Rake reception, code synchronization, descrambling code and channelization code-generation and the despreading operations. The Rake receiver is used to mitigate the fading introduced by the wireless channel by maximally combining the delayed replicas of the signal. Its output may be used for further baseband processing for detection.

With the present state-of-art VLSI technology, an ASIC solution is essential for a miniaturized full specification 3G air interface development. Therefore, in this paper, we present the development of an ASIC solution, which has been fabricated using the 0.25 μ CMOS technology, for a Rake receiver based 3G CDMA system.

Key words: 3G, CDMA, multipath fading, spreading, scrambling, Rake receiver, fading cancellation, maximal ratio combining.

1. INTRODUCTION

As the number of wireless handheld devices designed to access the Internet increases, there is a serious need for a faster and better wireless communications technology. The third generation wireless technology will provide superior wireless voice quality and data services, supporting video and multimedia content sent without wires to laptops, handhelds, smart phones, and potentially many other electronic devices. The 3G wireless access and mobility will be merged with the Internet to create essential new business opportunities and new services. Therefore it has the potential to be the nucleus of new services for the end users.

The 3G systems use CDMA as the access method [1], [2] in view of the several advantages of spread-spectrum communications such as ability to yield a good performance in the context of fading [3], ability for narrowband interference

rejection and support for different data rates as well as multiple users. These systems have a complex physical layer, which is essential in view of the requirements such as support for different transmission speeds, backward compatibility and other involved complicated mathematical operations. The Rake receiver is an important and essential block of a CDMA receiver used for reducing or canceling the effect of fading by the channel.

The computational complexity of a Rake receiver for 3G systems is huge and with the present state-of-art VLSI technology, it is very difficult to provide full speed processing in the form of a software solution on a digital signal processor and an ASIC solution is essential. The existing chip development efforts towards CDMA wireless solutions include systems developed by companies like Qualcomm, Phillips and LSI Logic. While some of these are ASIC's the others use a DSP core and a general-purpose system core. These solutions offer only low and mid-tier CDMA solutions. For instance the MSM6050 chipset of Qualcomm is designed for CDMA2000 1X and it is a mid-tier 3G solution (153 kbps), which works with a Zero IF direct conversion architecture [4]. Development of a full speed baseband processor is very useful and essential for a miniaturized 3G air interface development.

In this work, we developed a VLSI chip for a RAKE receiver based CDMA system, keeping in mind the UMTS standard. The receiver, apart from performing the de-spreading and descrambling operations, includes a Rake receiver to mitigate the fading introduced by the wireless channel. The hardware of the system is first designed, as per the specifications. Then it is coded in Verilog. The design is then synthesized and the layout is generated using the state-of-art Synopsys and Cadence design tools. The final design is fabricated in a 0.25 μ CMOS fabrication facility.

Organization of the paper

Section 1 contains an introduction to the subject of the paper. The details of the Rake receiver based baseband processor have been presented in section 2. Section 3 presents the hardware implementation of the Rake receiver. This is

followed by the design attributes and performance details in section 4. Finally, the paper has been concluded in section 5.

2. RAKE RECEIVER BASED BASEBAND PROCESSOR

As specified in the UMTS standards [5], the UTRA channels use the 10 ms radio frame structure. Each such frame is further split into 15 slots, each of length $T_{\text{slot}} = 2560$ chips, where the chip-rate is 3.84 Mcps. Fig. 1 shows the frame structure of a typical downlink channel.

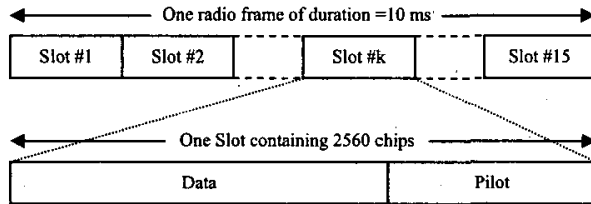


Fig. 1 Typical downlink frame format

To assist channel estimation and Rake reception, the transmission also includes some known pilot symbols [5], [6], along with data symbols, per slot. The pilot may be transmitted either on a parallel channel or on the same channel with data as shown in Fig.1. The Rake receiver uses delayed replicas of the received pilot, where each of the delayed replicas is multiplied with the scrambling as well as the channelization codes. Then the signal is correlated with the pilot signature whose output yields the estimate of the channel over the pilot burst. An algorithm such as the weighted mean squares averaging [7] algorithm can be used to get a better estimate by averaging such estimates over the past few slots. The delayed replicas of the received signal are fed to different fingers where they are multiplied by the conjugates of the channel estimates of the corresponding fingers and are summed. This yields the maximally combined signal, which can be used for further baseband processing for detection.

The time difference between the arrivals of the major multipaths, in urban and suburban areas, has been found to be around $1 \mu\text{s}$ [8], which is equivalent to 4 chip durations. Hence it is sufficient to look for the multipaths in a window of 4 chip durations. The minimum delay between two fingers of a Rake can not be less than one chip duration, as in that case both the spreading and scrambling codes lose orthogonality and it is not possible to resolve the two multipaths arriving within one chip duration. Considering these facts it makes sense to have a Rake receiver with four fingers with each finger processing the replica of the signal, delayed by one chip duration with respect to the adjacent fingers. In this case we can expect to extract all the resolvable multipaths arriving in a time window of 4 chip durations, i.e. $1.04 \mu\text{s}$. Let us note that this is a suboptimal solution, as ideally each finger should correspond to a peak in the multipath profile; however it is reasonable because it takes care of practically all the major multipaths.

As discussed above, we have gone for a four finger Rake diversity receiver, with each finger processing the replica of the received signal delayed by one chip duration with respect to the adjacent fingers. Fig. 2 shows the block schematic of the receiver.

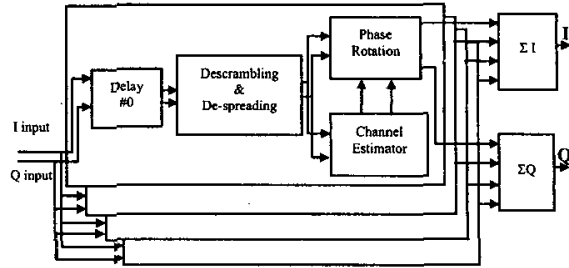


Fig. 2 Block schematic of the Rake receiver

Digitized input samples are received in I and Q branches in complex low-pass number format. The four fingers of the Rake receiver introduce delays of respectively 0, 1, 2 and 3 chip durations in the input samples. The code generators consist of Gold code generators for complex valued descrambling code generation, and OVFS code generators for de-spreading code generators [9]. The data in each finger is integrated after multiplication with both codes to get data symbols. The symbol rate is given by

$$\text{Symbol Rate} = \frac{3.84 \text{ Mbps}}{\text{Spreading Factor}} \quad (1)$$

where the spreading factor may be 4, 8, 16, ..., or 512 [9].

In each finger, the channel estimator uses the pilot symbols to estimate the channel characteristics. Either dedicated pilots, which are time multiplexed with user data slot, or common pilots, which are transmitted separately on PCPICH are used for this purpose [5]. To estimate the channel characteristics, apart from the received pilot values of the current slot, the pilots of previous slots may also be used. In a slowly varying channel it is useful to use the channel estimates of a few previous slots with some forgetting factor. Let, for any slot k , the channel estimate calculated from its pilots is ch_k and the interpolated channel estimate for the slot is est_k . We perform the operation,

$$est_k = (1 - 2^{-W}) ch_k + 2^{-W} est_{k-1} \quad (2)$$

where W is an externally controlled forgetting-factor which is signaled by higher layers.

The de-spread data in each finger is multiplied by the complex conjugate of the channel estimate corresponding to that finger. This has two effects. Firstly, the phase introduced to the signal is neutralized so that the outputs of all the fingers can be summed together. Secondly, stronger a multipath more is its weight in the final output, as a stronger multipath will cause higher amplitude of the channel estimate in the corresponding

finger. In fact this essentially takes care of maximal ratio combining [10]. Finally the outputs of all the four fingers are summed together to give I and Q outputs. These outputs may be used either as received symbols or for further processing, such as multi-user detection or soft Viterbi decoding [11].

3. IMPLEMENTATION OF THE RAKE RECEIVER

The hardware implementation of the Rake receiver design is presented in this section. As all the four fingers of the Rake are identical, the description of only one of them suffices. The structure of a finger can be summarized as a sequence of a delay element, multiplication by descrambling and de-spreading codes, integration over a symbol duration, and finally, multiplication by the complex conjugate of the channel estimate. The delays are introduced using flip-flops operating on the chip clock.

Descrambling and de-spreading code multiplication

Fig. 3 shows the operations of the multiplication of input data with descrambling and de-spreading codes.

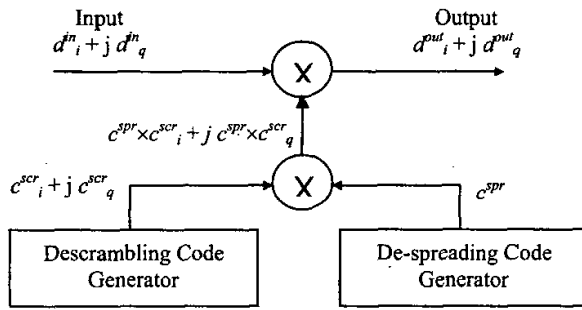


Fig. 3 Multiplication with descrambling & de-spreading codes

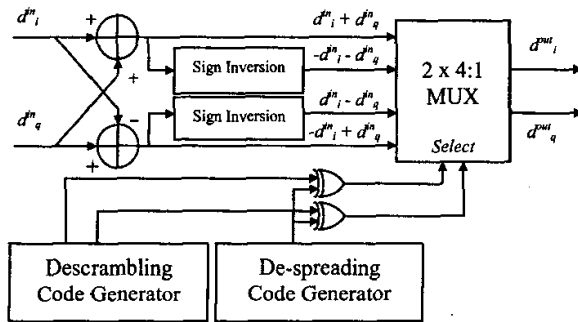


Fig. 4 Hardware for multiplication with descrambling and de-spreading codes

Descrambling codes are complex valued codes of the format $\pm 1 \pm j$, represented by two bits where bit '0' implies +1 and bit '1' implies -1. The de-spreading codes are real valued codes, having

values ± 1 . For better area and speed optimization, firstly these codes are multiplied together and the result, in turn, is multiplied to the input data. The first multiplication consists of two one-bit by one-bit multiplications, each of which can be performed by one XOR gate. For the second multiplication, we note that the output is of the form $(\pm d^in_i \pm d^in_q) + j(\pm d^in_i \pm d^in_q)$, where $d^in_i + j d^in_q$ is the input sample Fig. 4 shows the hardware requirement for this scheme.

Integration over symbol period

The de-spread chips have to be integrated over the symbol period, which depends on the spreading factor. We have designed an accumulator architecture, which is optimized for the purpose. Let the input, in 2's complement format, be N-bit wide. Then the width of the accumulator has to be N+9, as the maximum spreading factor is 512. Firstly, we change the format of the input chips to an unsigned format by adding 2^{N-1} to each of them. This removes the need for sign extension. The change of the format can be done just by inverting the MSB's of the input chips. Similarly the output is converted back to 2's complement format just by inverting the MSB of the truncated result. Another optimization is achieved by replacing the N+9 bit adder by an N-bit adder and a 9-bit counter. This improves both the area and speed of the design as 9 full-adders are replaced by 9 half-adders. Fig. 5 shows the structure of such an accumulator.

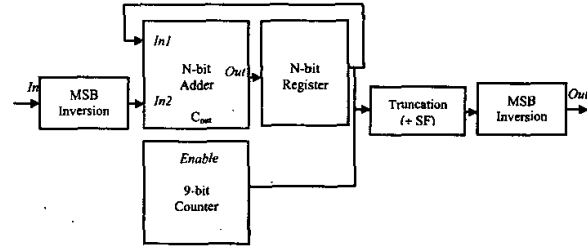


Fig.5 Integrator over symbol period

Channel estimation

The pilot chips, for each finger of the Rake, have to be multiplied with the descrambling codes, de-spreading codes and the complex conjugate of the transmitted pilot symbols before being integrated over the pilot burst to get the channel characteristics for the multipaths corresponding to that Rake finger. Both descrambling codes and pilot symbols are complex numbers of the format $\pm 1 \pm j$. Hence, each of them has amplitude of $\sqrt{2}$ and phase of $\pm 3\pi/4$ or $\pm \pi/4$. The de-spreading codes can have values ± 1 . Hence the product of all three of them will be a complex number having amplitude of 2 and phase of 0, π or $\pm \pi/2$. Multiplication with 2, or with any constant for that matter, is redundant for the end result. Hence, we only need to multiply ± 1 or $\pm j$ to the input chips, depending on the descrambling code, de-spreading code and pilot signature. This

multiplication, as can be easily seen, can be performed with just two sign-inverters and four 4:1 multiplexers. The result of the multiplication is accumulated over the pilot burst using an accumulator similar to the one shown in Fig. 5. The previous channel estimate is combined, with a variable weight, with the estimate obtained from the pilot of the current slot to get a better estimate of the channel. Fig. 6 shows the operations needed for this functionality.

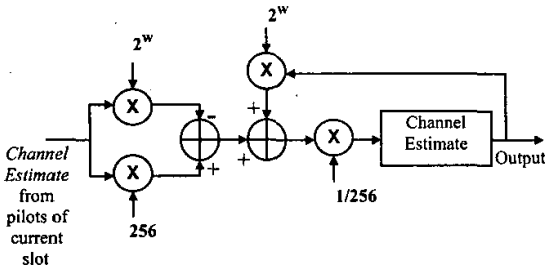


Fig. 6 Weighted averaging of channel estimate of multiple slots

Note that all the multiplications in the diagram can be done by shifting the inputs. This technique is especially useful in a slow varying channel.

Phase rotation

The phases of the de-spread symbols of each of the fingers have to be neutralized, using the channel estimate of that finger, before the outputs of the fingers can be summed together. The whole operation for a four finger Rake requires four complex multiplications per symbol, each of which, in turn, requires four real multiplications. The input throughput at this stage is slow, being at de-spread symbol rate. This fact lets one share a single fast multiplier-accumulator for the phase rotation and summations of the de-spread symbols of all the fingers.

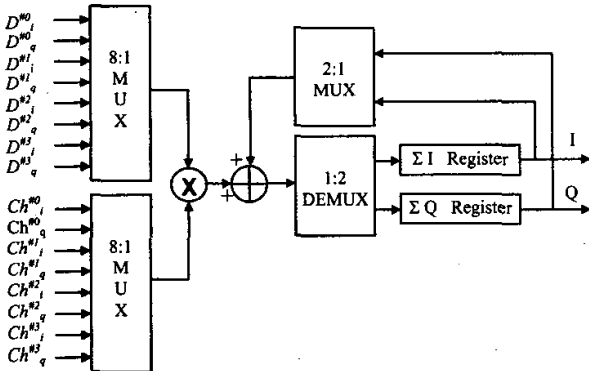


Figure 7: Shared hardware for phase neutralization and multipath summation

Word size

The word size at the different points in the design is a very crucial issue, which has effects on area, power, hardware complexity, speed and accuracy of the design. Following is a description of the word sizes used in the different parts of the design. The widths of I and Q part of the data at each point of the design are equal. The input samples are assumed to be 8-bit wide. The output after multiplication with descrambling and de-spreading codes is 9-bit wide. The output after the integration of the chips over the symbol period is truncated to 11-bits. At this stage the truncation has to be performed on both MSB and LSB depending on the spreading factor. The channel estimate has been kept 10-bit wide. The final truncation is done after combining the outputs of different fingers to get 8-bit wide soft outputs.

4. TEST RESULTS

A Rake receiver based CDMA processor, with the architecture discussed above, is designed using the Synopsys and Cadence design tools and fabricated in 0.25 μ CMOS technology. Fig. 8 shows the layout view of the design whereas Table 1 lists some of the design attributes and statistical details of the design.

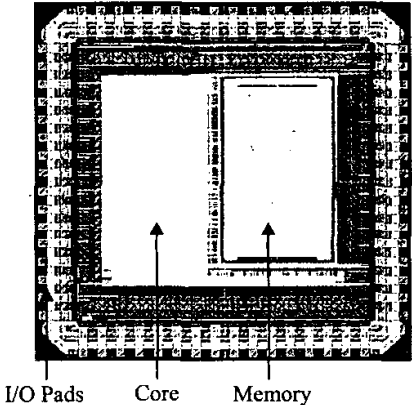


Fig. 8: Layout of the design

Chip rate	3.84 MHz
Slot duration	2560 chips
Frame duration	10 ms, 15 slots
Spreading factor	4, 8, 16, ..., 512
Spreading codes	OVSF codes
Average latency	670 μ s
Power	18 mW
Die size	4.3 mm x 4.3 mm
In-out pin count	64

Table 1: Design attributes and statistics

The bit error rate (BER) has been calculated, for both fading and non-fading environments. In the simulation setup, the

spreading factor was taken to be 16. Every slot contained 16 pilot symbols, multiplexed with 144 data symbols. The QPSK signal was transmitted, on zero IF, over the multipath Rayleigh fading channel, with a delay profile containing 3 discrete multipaths. Each of the multipaths underwent independent Rayleigh fading. Clarke's model [3] was used to simulate the fading channel. The Doppler frequency shift was assumed to be 100 Hz. A reasonable assumption, that the channel characteristics remain constant over the slot duration, was made. Apart from fading, white Gaussian noise was added to the signal. Extensive simulation of the layout was done in Verilog and C. Fig. 9 shows the plots of the BER versus input SNR for both the fading as well as non fading environments.

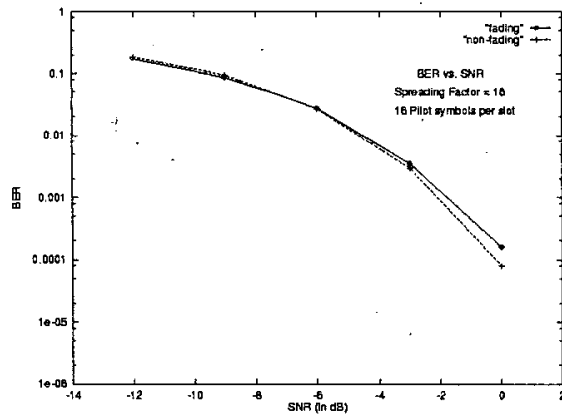


Fig. 9: Bit error probability performance of the receiver

From the results, it is observed that the performance in the fading channel is very close to that of a non-fading channel, especially at low SNR's. In fact, at very low SNR's, the BER is found to be slightly smaller than that of the non-fading channel which may possibly be due to the coherence in the signals from the different paths. This shows that the Rake architecture effectively mitigates the effect of fading. It can be verified that the performance of our design is reasonably close to theoretical results obtained using floating point arithmetic. Hence the word sizes used in the design ensure fair enough accuracy, keeping the area, speed, and power consumption within the reasonable limits at the same time.

5. CONCLUSIONS

In this work, the hardware development of a Rake receiver based CDMA baseband processor in the form of an ASIC for 3G wireless communication systems is made and it is presented here. This system includes the CDMA part of a transceiver. The hardware is optimized to the extent possible from the chip area and power consumption considerations while satisfying the requirements of a 3G wireless system. The proposed architecture of the receiver is shown, citing design attributes and Verilog and C simulation results, to be a feasible solution for UMTS in terms of area, power and performance.

The speed of the ASIC is sufficient for full 3 G wireless specifications. A four finger RAKE receiver is sufficient for a 3G application under channel fading up to 4 significant paths. The performance is almost equal to that of an AWGN channel without fading. The word sizes considered here are good enough for practical implementation. Using a 0.25 μ m technology, it is possible to confine the power consumption to within 18 mW. This design provides a path towards developing a full baseband chip for the 3G wireless communication systems.

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