

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS INC.

Petitioner,

v.

PANTECH WIRELESS, LLC,

Patent Owner.

Case IPR2023-01272

U.S. Patent No. 9,065,486

**DECLARATION OF DR. BERTRAND HOCHWALD
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,065,486**

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I. INTRODUCTION

1. I have been retained by LG Electronics Inc. (whom I will refer to as “LGE”) to provide my opinions on certain issues related to U.S. Patent No. 9,065,486 (the “’486 patent,” which I understand has been designated as Exhibit 1001) in connection with the above-captioned *inter partes* review (IPR) proceeding. In particular, I have been asked to provide my insights, analysis, and opinions regarding the validity of claims 1-6 of the ’486 patent (“Challenged Claims”), and whether the Challenged Claims are anticipated or rendered obvious by the prior art references identified below and as to whether persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence could have located these references. A listing of the Challenged Claims, including the element numbers assigned to each element in those claims, is attached to this declaration as **Appendix C**.

2. I understand the ’486 patent is titled “Detection, avoidance and/or correction of problematic puncturing patterns in parity bit streams used when implementing turbo codes,” identifies as its named inventors Philip J. Pietraski and Gregory S. Sternberg, and is currently owned by Pantech Wireless, LLC. I have considered the ’486 patent.

3. I understand that the file history of the '486 patent has been designated as Exhibit 1002. I have considered this file history, and I will refer to it as the "'486 File History" or by its exhibit number.

4. I understand that the '486 patent was filed as U.S. Patent Application 14/300,734 on 6/10/2014.

5. I have considered the prior art cited in my declaration, including:

1. U.S. Patent No. 7,260,770 to Stewart ("**Stewart**"), titled "Block puncturing for turbo code based incremental redundancy," filed 10/22/2001 and issued 8/21/2007. I understand that a copy of this patent has been designated as Exhibit 1005.
2. R1-01-1014, *A New Hybrid-ARQ Scheme Using Incremental Redundancy*, 3GPP TSG-RAN HSDPA Ad-Hoc Meeting (November 5-7, 2001) ("**Motorola**"). I understand that a copy of this reference has been designated as Exhibit 1006.
3. R1-01-1047, *Overview of Proposed Schemes for Incremental Redundancy*, 3GPP TSG-RAN HSDPA Ad-Hoc Meeting (November 5-7, 2001) ("**3GPP-Summary**"). I understand that a copy of this reference has been designated as Exhibit 1007.
4. TS 25.212 v5.1.0, *Universal Mobile Telecommunications System (UMTS); Multiplexing and channel coding (FDD) (3GPP TS 25.212 version 5.1.0 Release 5)*, 3GPP Technical Specification (2002-06) ("**TS25.212**"). I understand that a copy of this reference has been designated as Exhibit 1008.

6. I am being compensated by LGE at my standard hourly consulting rate of \$675 for my time on this matter. My compensation is not dependent on the outcome of this proceeding.

7. In forming my opinions, I relied on the documents cited in this declaration and the documents identified in the attached **Appendix B**. These documents comprise patents, file histories, printed publications, and other related documents. As discussed below, each document is a type that experts in my field would have reasonably relied upon when forming their opinions. Further, experts in my field would have had access to each document either through the applicable patent offices and/or well-known libraries, conferences, or publications in the field. My opinions are also based upon my personal and professional experience.

8. In parallel with this declaration, I have prepared declarations for IPR2023-01273 and IPR2023-01267. I also understand that declarations are being prepared by other experts in IPR2023-01269, IPR2023-01270, IPR2023-01271, and IPR2023-01268. Due to overlap in subject matter and prior art references and similarities in corresponding analyses, I understand that some parts of my declaration may bear superficial similarities to documents filed in these other IPRs, but all analysis and opinions presented herein are my own.

II. QUALIFICATIONS

9. My qualifications for forming the opinions in this report are summarized here and also noted in my Curriculum Vitae (“CV”), which is submitted as **Appendix A**.

10. In 1995, I received a Ph.D. in Electrical Engineering from Yale University. My Ph.D. work involved the analysis and processing of electromagnetic and audio signals for the estimation of the location of electromagnetic and audio sources. In 1993, I received a M.A. in Statistics from Yale University. My primary area of study was Signal Processing and Communications. I received a M.S. in Electrical Engineering from Duke University in 1986, and a B.S. in Engineering from Swarthmore College in 1984.

11. I have twenty-eight years of combined industry and academic experience in the research and design of hardware, software, and systems for various technologies, including electronic devices, sensors, signal and image processing, networking and wireless communications. I have worked in various industry jobs, including at the Department of Defense, Bell Labs, and a start-up in California before joining the University of Notre Dame in 2011. As I explain below, much of my work has been in the general areas of audio/video signal processing and communications.

12. My most recent appointment, starting in 2011, is with the University of Notre Dame, where I am currently a Freimann Chaired Professor of Electrical Engineering. I have taught both graduate and undergraduate classes in signal processing, information theory, communications, and in systems theory. I have also taught courses in electronics, analog and digital signal sensing, processing, computation, and electronic forms of wireline and wireless networking and communications. My primary areas of research include the design and analysis of wireless systems, sensors, and signal processing. I advise graduate students who are attaining Ph.D. degrees through research and coursework. My research work now includes processing of high data rate signals (similar to those used to transmit and receive coded signals) in communication systems.

13. An example of my current work at the University includes a project that I lead called RadioHound distributed spectrum sensor system for remote monitoring using radio signals (<https://wireless.nd.edu/research/radiohound-distributed-spectrum-sensing/>), which is a multi-year effort involving several students, faculty, and technicians. The RadioHound system captures data from hundreds of sensors and displays it in a real-time setting for human interpretation and assessment. This project, which is funded by government and industrial sponsors, involves the design of hardware sensors, and software communications transceivers. The project has

become an educational and research tool used by laboratories inside and outside the University of Notre Dame.

14. Prior to Notre Dame, I worked from 2005-2010 at Beceem Communications, a 4G WiMax and LTE cellular communication chipset start-up company in Santa Clara, California, where I was Chief Scientist and Vice President of Systems Engineering. I was an integral part of the chipset development team. Beceem was bought by Broadcom Corporation in 2010 and no longer exists as a separate company. Several aspects of channel coding and wireless communications for our products were developed within this team.

15. From 1996-2005, I worked at Lucent Bell Laboratories in New Jersey, where I was a Distinguished Member of the Technical Staff doing research into various communication and networking systems. For example, my work in Bell Labs included wireless communications and multi-antenna signal processing and coding.

16. Before Bell Laboratories, I was a Visiting Assistant Professor at the University of Illinois in Urbana-Champaign during the 1995-1996 school year, where I worked on a broad range of research topics related to signal processing and wireless communications.

17. Prior to completing my Ph.D., during 1986-1989 I worked at the Department of Defense as a system engineer for signal processing and wireless communication systems. In this role I designed wireless communication equipment for audio and video signal monitoring and processing. Much of this work is classified for security reasons.

18. As a result of my research, I have obtained 50 patents, and I have published more than one-hundred articles in scholarly journals, many of them within the journals of the Institute of Electrical and Electronic Engineers (IEEE), one of the premier societies for electrical engineers. I have been an invited and plenary speaker at several international conferences throughout the world and have received awards and recognition for my research and publications. An example relevant publication includes B. Hassibi and B. Hochwald, "High-rate codes that are linear in space and time," *IEEE Transactions on Information Theory*, vol. 48, pp. 1804-1824, July 2002.

19. Since 2012, I have engaged in consulting work as an expert in various litigation matters including acoustic echo cancelling, multi-antenna technologies, cellular and wireless local-area-net standards and technologies, and touch-screen technologies. I have served as an expert on behalf of both plaintiffs and defendants in patent cases. I have served as a technology expert in various aspects of the

litigation process, including trade secret disputes, trial testimony, *Markman* hearings, and IPRs.

20. Some of my patents deal with coding for multi-antenna communications. An example is US Patent No. 6,363,121, which designs multidimensional constellations with a unitary structure for transmission across multiple antennas.

III. LEGAL UNDERSTANDING

A. My Understanding of Claim Construction

21. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art of the patent at the time of the invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art in the relevant time period (*i.e.*, at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification, and the prosecution history (*i.e.*, the intrinsic record).

22. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and

prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office, and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or clearly and unambiguously disavowing claim coverage.

23. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider "extrinsic" evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of ordinary skill in the art at the time of the claimed invention. For example, this can be useful for a technical term whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

1. Means Plus Function Terms

24. I have been informed and understand that certain claim terms can be means-plus-function terms. I understand that a “means-plus-function” term is one that is expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support of that function in the claim. I understand that a term is presumed not to be a means-plus-function term if it is not drafted using the term means. I also understand that a term that connotes sufficient structure to a person of ordinary skill in the art would not be a means-plus-function term.

25. I understand that for means-plus-function terms, the term is construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof. My understanding of the doctrine of equivalents and equivalent structure is set forth below in Section III.D (My Understanding of the Doctrine of Equivalents).

26. If a term is determined to be a means-plus-function claim, I understand that the disclosed structure in the specification is deemed to be corresponding structure if the specification or prosecution history clearly links or associates that structure to the claimed function and the disclosure must be sufficient to achieve the claimed function.

B. My Understanding of Anticipation

27. I understand that a patent claim is invalid as “anticipated” if all of the limitations of the claim are present, either expressly or inherently, in a single pervious device, or described, either expressly or inherently, in a single prior art publication or patent. I understand that, in the relevant time period, 35 U.S.C. § 102 stated that a person shall be entitled to a patent unless:

- The invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or
- The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or
- He has abandoned the invention, or
- The invention was first patented or caused to be patented, or was the subject of an inventor’s certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor’s certificate filed more than twelve months before the filing of the application in the United States, or
- The invention was described in—(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language; or
- He did not himself invent the subject matter sought to be patented, or

- (1) during the course of an interference conducted under section 135 or section 291, another inventor involved therein establishes, to the extent permitted in section 104, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

28. I also understand that a prior art reference can disclose a claimed feature because the feature is expressly described or because the feature is inherent in the disclosure. I understand that something is inherent in a prior art reference if the missing descriptive matter must necessarily be present, not merely probably or possibly present, and it would be so recognized by a person of ordinary skill in the art as of the priority date of the patent.

29. Claim limitations that are not expressly found in a prior art reference are inherent if the prior art necessarily functions in accordance with, or includes, the claim limitations. I understand that it is acceptable to examine evidence outside of the prior art reference (i.e., extrinsic evidence) in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it.

C. My Understanding of Obviousness

30. I understand that a claim may be invalid if the subject matter described by the claim as a whole would have been obvious to a hypothetical person of ordinary skill in the art in view of a prior art reference or in view of a combination of references at the time the claimed invention was made. Therefore, I understand that obviousness is determined from the perspective of a hypothetical person of ordinary skill in the art and that the asserted claims of the patent should be read from the point of view of such a person at the time the claimed invention was made. I further understand that a hypothetical person of ordinary skill in the art is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit.

31. I have been informed that there are two criteria for determining whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a

reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering their problem.

32. I have also been advised that an analysis of whether a claimed invention would have been obvious should be considered in light of the scope and content of the prior art, the differences (if any) between the prior art and the claimed invention, and the level of ordinary skill in the pertinent art involved. I understand as well that a prior art reference should be viewed as a whole.

33. I have also been advised that in considering whether a claimed invention could be obvious over a combination of prior art references, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the marketplace, and/or the background knowledge possessed by a person of ordinary skill in the art. I understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;

- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a person of ordinary skill can implement a predictable variation, the variation is likely obvious;
- If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond their skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls whether the claim is obvious;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;
- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
- "Common sense" teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle;
- A person of ordinary skill in the art is also a person of ordinary creativity, and is not an automaton;
- A patent claim can be proved obvious by showing that the claimed combination of elements was "obvious to try," particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a person of ordinary skill in the

art would have had good reason to pursue the known options within his or her technical grasp; and

- One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

34. I further understand that, in making a determination as to whether the claimed invention would have been obvious to a person of ordinary skill, the Board may consider certain objective factors if they are present, such as: commercial success of products practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. These factors are generally referred to as “secondary considerations” or “objective indicia” of nonobviousness. I understand, however, that for such objective evidence to be relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence and that this nexus must be based on a novel element of the claim rather than something in the prior art. I also understand that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (such as motivation to combine with predictable results) that is sufficiently strong.

D. My Understanding of the Doctrine of Equivalents

35. I have been informed that there is a “doctrine of equivalents” in patent law that supports a finding of invalidity if a prior art element is equivalent to a claimed element, even if the prior art element is not identical to the claimed element.

Equivalence may be established if the prior art element performs the identical function specified in the claim in substantially the same way and produces substantially the same result.

36. I also understand that insubstantial differences between a prior art element and a claimed element—as understood in light of its specification—will not preclude a finding of invalidity. For example, a difference in a number of parts in a prior art element and the corresponding element disclosed in the patent specification may be an insubstantial difference. Similarly, if a prior art element lacks several components of an overall structure corresponding to a claimed function, that difference may be insubstantial. And, potential advantages of a structure that do not relate to a claimed function should not be considered in an equivalents determination.

37. I understand that the structures, materials, and acts to be considered equivalent or non-equivalent may be described in a patent's specification. A specification may therefore establish a narrow or broad range of equivalents, although an applicant also need not exhaustively describe the full range of equivalents.

E. My Understanding of Written Description and Enablement

38. I understand that the written description and enablement requirements are set forth in Pre-AIA 35 U.S.C. §112. This section provides:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

39. I have been informed that to have an adequate written description, the patent must convey with reasonable clarity to a person skilled in the art that, as of the filing date sought, the named inventor was in possession of the invention.

40. I have also been advised that, to demonstrate possession of the invention, the specification must permit a person with ordinary skill in the art to visualize or recognize the identity of the subject matter purportedly described. Although the specification need not describe the claimed subject matter verbatim to demonstrate possession of the invention, generalized language will not suffice if it does not convey the detailed identity of an invention.

41. I have also been advised that, to have an adequate written description, each limitation of the claimed invention must be disclosed expressly or inherently in the specification. It is not sufficient that the missing claim limitation may be obvious from the specification.

42. To be an enabling disclosure, the specification must adequately disclose to a person skilled in the art how to make or carry out the claimed invention without undue experimentation.

43. The omission of minor details from a patent specification's written description does not cause the specification to fail to meet the enablement requirement. However, when there is no disclosure of any specific starting material or of any of the conditions under which a process can be carried out, undue experimentation is required and there is a failure to meet the enablement requirement that cannot be rectified by asserting that all the disclosure related to the process is within the skill of the art.

F. My Understanding of the Priority Date of a Patent for Prior Art Purposes

44. I understand that for a prior art patent or patent application to be entitled to the priority date of a provisional application to which that patent or patent application claims priority, the specification of the provisional must contain a written description of the invention and the manner and process of making and using it, in such full, clear, concise, and exact terms, to enable a person of ordinary skill in the art to practice the invention claimed in the non-provisional application. To satisfy this requirement, I understand that the disclosure of the provisional application must

provide enabling written description support for both the claims of the patent and the subject matter of the patent relied upon for prior art purposes.

45. My understanding is that, similarly, a patent can claim priority to an earlier filing date of a foreign patent application if the patent expressly claims the benefit of the earlier filing date, and if disclosure of the foreign patent application provides support for the claims of the patent. I also understand, however, that a patent reference cannot claim the benefit of a filing date of a foreign priority document to establish the patent as prior art.

IV. BACKGROUND OF THE TECHNOLOGY

46. The '486 patent is generally directed to a technique for selecting between systematic bits or parity bits of cellular data for transmission in cellphone systems. '486, 4:60-5:13, 6:4-12, 6:26-51, 10:20-28, 18:15-55, 20:50-59. Systematic bits include bits of data transmitted to a receiving device from a sending device. The systematic bits undergo a turbo coding process that generates parity bits that include error correction information that is used by a receiver (such as a cellphone) to correct errors in messages received from a transmitting device (such as a base station). '486, Fig. 2, 1:59-2:6; 6:13-19. The Challenged Claims require interleaving systematic bits and parity bits; buffering the bits, and selecting between

systematic and parity bits in order to achieve a desired code rate for transmitting information.

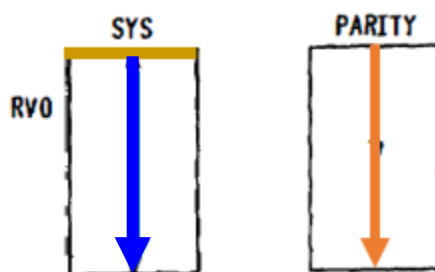
47. As I discuss further below in Section V.B (Prosecution History of the '486 Patent), the United States Patent and Trademark Office ("USPTO") did not reject the claims of the '486 over prior art references, other than a double patenting rejection over parent patent U.S. 8,074,143. Thus, the USPTO had not identified a particular allegedly novel aspect of the Challenged Claims that had been overcome in the art. Each of the Challenged Claims generally recites interleaving, buffering, and selecting between systematic bits and parity bits. The "Summary of the Invention" of the '486 patent describes a "two stage" rate matching process used to implement an "incremental redundancy (IR)" process that selects different numbers of systematic bits and parity bits for transmission based on whether systematic bits were successfully recovered from a prior transmission. '486, 4:60-5:8.

48. Incremental redundancy is one type of a hybrid automatic repeat request ("HARQ") process. Ex. 1009. In a HARQ process, a transmitter resends portions of systematic bits and parity bits to a receiver to ensure delivery of information to the receiver by providing the receiver with sufficient information to correct errors in the transmissions. '486, 4:60-5:8. The different numbers of systematic vs. parity bits in each transmission facilitate different "code rates" in a

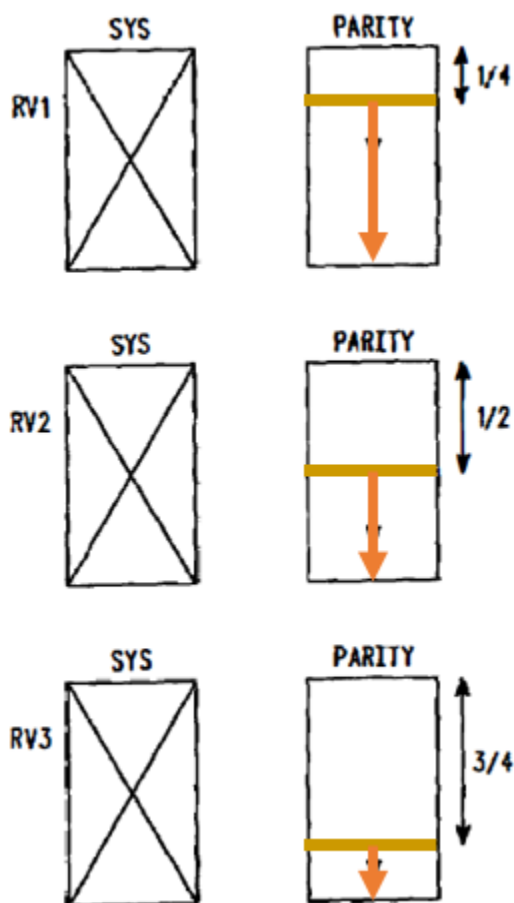
HARQ process. As discussed further below, a code rate is a ratio of an intended number of information bits (also called systematic bits) to the total number of bits (including redundancy bits or parity bits) that are transmitted. Lower code rates (e.g., more redundancy bits and fewer information bits) are used for poor channel conditions with more errors. Higher code rates (e.g., fewer redundancy bits and more information bits) are used for better channel conditions with fewer errors. '486, Figs. 1-2, 1:35-2:36, 3:10-32, 8:28-58, 13:17-36.

49. Based on the above discussions of the '486 patent, including the “Summary of the Invention,” the '486 patent appears to assert that the novel aspect of the claims is the selecting between systematic bits and parity bits to achieve different code rates to support the incremental redundancy process. '486, 4:60-5:8. However, this selecting process was known in the art. For example, the European Patent Office had rejected claims similar to the Challenged Claims over **TS25.212** and indicated that “large parts” of the '486 patent including Fig. 10 and other passages that describe the selecting process had been copied without indicating that **TS25.212** was the source of such information. Ex. 1010, pp.14-16; TS25.212, Fig. 17, §4.5.4(58-60); '486, Fig. 10, 16:10-26, 16:52-17:10, 18:10-19:13. In addition, **Stewart** discloses selecting between a “Systematic” bit stream and “Parity 1” and “Parity 2” bit streams based on a redundancy version parameter at the transmitting

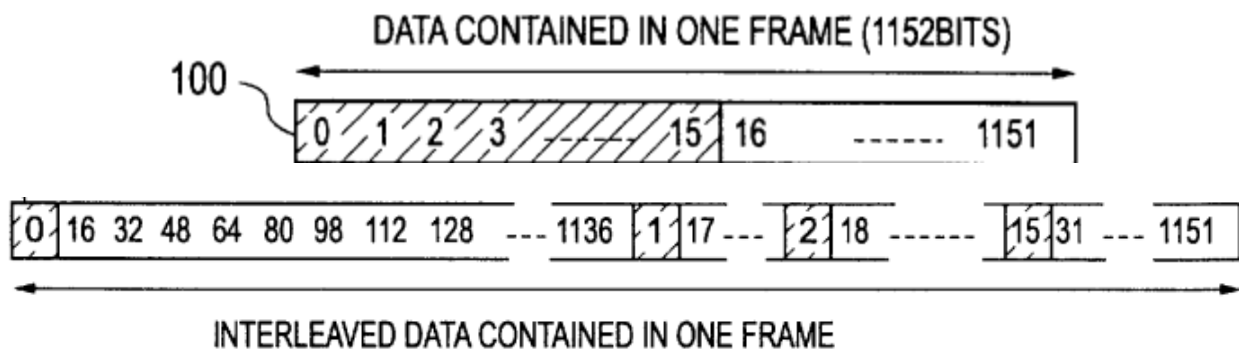
device. Stewart, Figs. 3-4, 6, 3:1-12, 3:64-4:45, 5:57-7:24, 9:65-10:1. As an example, Stewart discloses one subset of redundancy versions (*e.g.*, “RV0”) that selects **systematic bits** over **parity bits**, and also discloses other subsets (*e.g.*, “RV1,” “RV2,” RV3”) that select **parity bits** over **systematic bits**. In Fig. 6 of Stewart below, **starting points** for reading bits from a respective block matrix of a systematic bit interleaver or parity bit interleaver are annotated with a **gold line**. These **starting points** vary depending on the redundancy version. The direction of reading **systematic bits** is indicated by a **blue arrow**, and the direction of reading **parity bits** is indicated by an **orange arrow**. For example, Stewart discloses “RV0” that selects **systematic bits** over **parity bits** by selecting **systematic bits** before **parity bits** for transmission (*e.g.*, from the **starting point** in a systematic interleaver), or by selecting more **systematic bits** than **parity bits** for transmission. Stewart, Fig. 6, 6:57-61. This selection of **systematic bits** over **parity bits** is used to send information in good channel conditions—for example, conditions with few errors in the transmitted information.



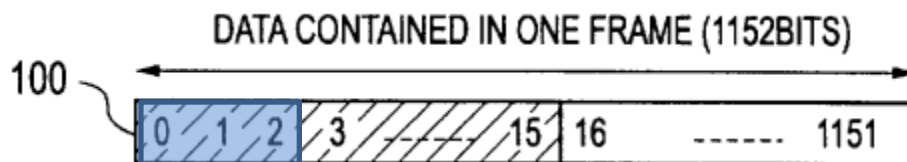
50. **Stewart** also teaches the example redundancy versions “RV1” to “RV3” that select **parity bits** over **systematic bits** by selecting **parity bits** starting from different **starting points** in a parity interleaver. ’486, Fig. 6, 5:33-36, 6:5-52, 6:62-7:4. Although the figures show that in redundancy versions “RV1” to “RV3” parity bits are selected over systematic bits (and systematic bits are crossed out on the left), these redundancy versions also select more **parity bits** than **systematic bits** for transmission, in which case none or some systematic bits are selected. *Id.*



51. The Challenged Claims also require “interleaving” and “buffering.” I will explain an example of how interleaving reduces burst errors in the context of excerpts of Fig. 1, which show non-interleaved “data contained in one frame” and “interleaved data contained in one frame”, both of which are excerpted below. The interleaved data frame is generated by taking every 16th bit from the non-interleaved frame. Shibutani (Ex. 1012), Fig. 1.

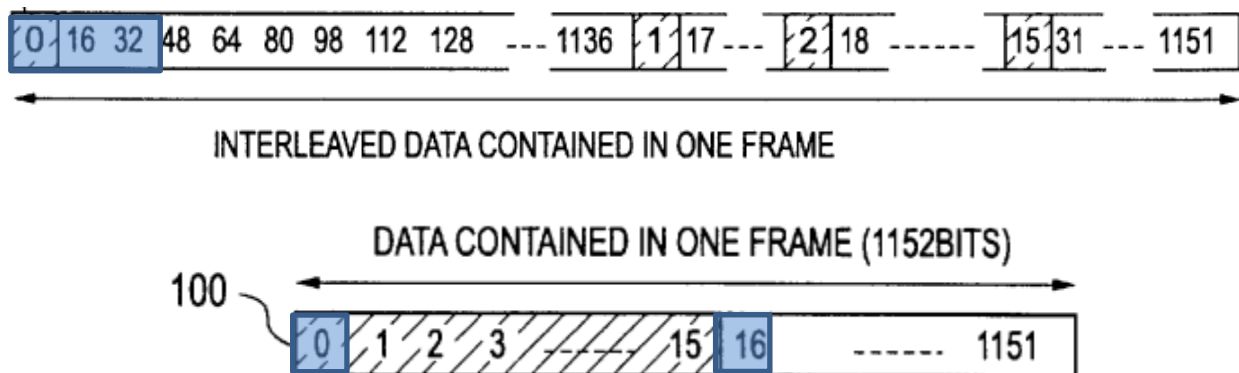


52. If a burst error, for example caused by noise over a contiguous time segment, occurs in a non-interleaved data frame, it would eliminate a contiguous range of bits that would be difficult to recover, as shown below by the solid box that indicates loss of bits 0-2.



53. On the other hand, applying the above noise to an interleaved data frame would affect a contiguous portion of the interleaved data frame (the first three

positions), but non-contiguous portions of the non-interleaved frame (corresponding to bits 0, 16, 32). Because the errors are spread out in the non-interleaved frame, they are more easily corrected through error correction codes because the errors are distributed throughout an information bit sequence. Shibutani, 1:9-32.



54. Other features of the claims are also taught by references discussed in this declaration. For example, **Motorola** also teaches selecting between systematic bits and parity bits for transmission based on a set of redundancy versions. As another example, **3GPP-Summary** additionally teaches buffering systematic bits and parity bits in a “ring buffer,” and selecting the systematic bits or parity bits from the ring buffer for transmission based on a redundancy version parameter. **3GPP-Summary**, §2.4. **TS25.212** additionally teaches a virtual IR buffer that buffers systematic bits and parity bits, and prioritizing either systematic bits or parity bits for transmission based on a redundancy version.

V. THE '486 PATENT

A. '486 Patent Overview

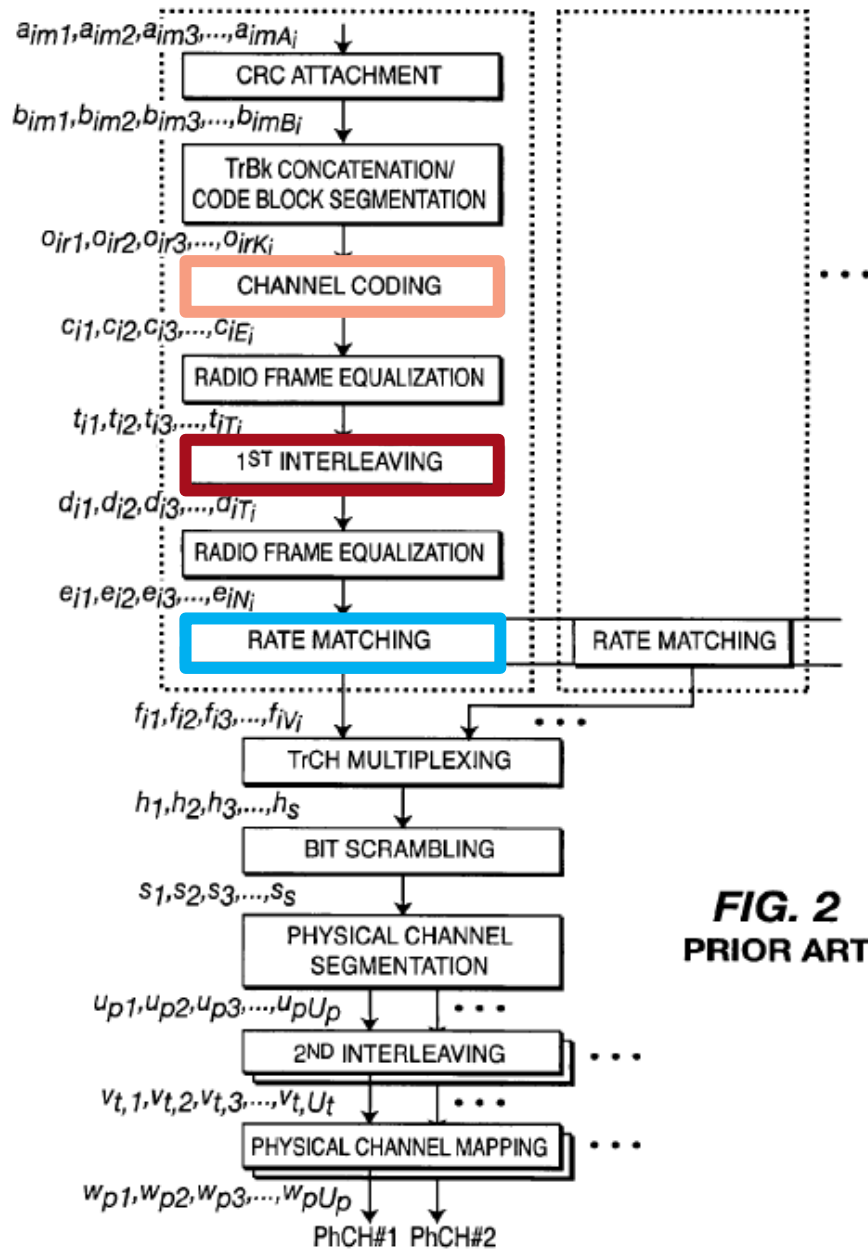
55. As discussed in the Section IV (Background of the Technology), the purported invention of the '486 patent is directed to a method (and apparatuses such as a user device or base station that perform the method) for selecting between types of bits (systematic bits and parity bits) that are to be transmitted in a wireless communication system such as a cellphone system. '486, 1:40-46, 4:60-5:13, 6:4-51, 10:20-28, 18:15-55, 20:50-59. In order to achieve reliable information transfer between transmitting and receiving devices in a cellphone system, a type or scheme called turbo coding is employed where transmissions contain systematic bits that carry the data, and a set of parity bits, generated from the systematic bits, that are used for error detection and correction of the systematic bits at a receiver. '486, 2:59-67, 14:54-64.

56. The '486 describes selecting systematic bits over parity bits for transmission, or selecting parity bits over systematic bits for transmission based on a redundancy version parameter. '486, 6:31-47, 10:20-28, 18:15-55, 20:50-59.

57. The Challenged Claims also generally recite interleaving the systematic bits and both sets of parity bits, and buffering the bits. '486, Figs. 2, 10, 1:59-2:49, 6:26-47, 11:7-25, 20:32-41. Interleaving and buffering are conventional processing

steps carried out in a wireless communication system as I describe herein. Interleaving allows for rearranging the order of the bits, e.g., prior to transmission; and de-interleaving allows for undoing the rearrangement of the bits, e.g., at a receiver. '486, Fig. 2, 1:59-2:6, 3:18-32, 11:7-25, 20:38-21:2; Ex. 1012 ("Shibutani"), 1:9-16, 44-48, Figs. 1-50; Ex. 1013 ("Huang"), 1:7-9, 26-48. The bits are interleaved to, e.g., mitigate against a type of error called burst error, which occurs when noise or interference from the system affects the integrity of a signal, and to mitigate against conditions where "bursts" of errors are concentrated in various portions of the pre-interleaved bit sequence. Another beneficial effect of interleaving is to break up periodic patterns in the coded bits. By rearranging the order of bits prior to transmission in an interleaving process, error and puncturing effects are less likely to affect continuous portions of the bits; instead, these effects are spread more randomly across the entire pre-interleaved bit sequence, which improves the ability to correct errors. '486, 3:18-32, 6:64-7:3, 10:20-28, 11:7-25, 11:26-42, 12:10-19, 21:53-22:30; Shibutani (Ex. 1012), 1:9-16, 44-48, Figs. 1-50; Huang (Ex. 1013), 1:7-9, 26-48; Section VIII.B.1(a) (Interleavers). Buffering refers to the process of temporarily storing information, as I discuss further below in Sections VIII.B.1(b) (Buffers), IX.A.1(a) (Buffering by Stewart).

58. Below are two figures that illustrate the Challenged Claims: Fig. 2 (color coded, below), which the '486 refers to as prior art and was copied from 3GPP TS 25.222 v3.8.0 ("TS25.222", Ex. 1011, Fig. 1), and Fig. 10, which was copied from Fig. 17 of TS25.212 (Ex. 1008). '486, 1:59-2:6. Fig. 2 depicts prior art processing of data in a wireless communication system, including: **channel coding**, **interleaving**, and **rate matching**. '486, Fig. 2. From the **channel coding** process, a systematic bit stream and a set of parity bit streams (*i.e.*, a first parity bit stream and a second parity bit stream) generated from the systematic bit stream are outputted. '486, 1:59-3:5, 14:61-64, Fig. 2. These outputted bit streams are then subject to a conventional **interleaving** process before they are passed to a conventional **rate matching** unit. '486, 1:59-2:6, 20:39-21:2. At least by referring to Fig. 2 as prior art, the named inventors of the '486 patent concede that the concepts of channel coding, interleaving and rate-matching, and the order thereof in Fig. 2, were well-known in the art prior to the invention of the '486 patent and I agree.



59. Fig. 10 (color coded, below) is a schematic block diagram that the '486 copied from the prior art, **TS25.212**, as I discuss in further detail below. *Compare* Fig. 10 of '486 *with* Fig. 17 of **TS25.212**. Note that **TS25.212** was published earlier (June 2002) than the first provisional patent application in the chain of patents

descending from the '486 was filed (December 16, 2002), regardless of whether this provisional actually includes the figure in question. Fig. 10 depicts the purportedly novel rate-matching process of the '486:

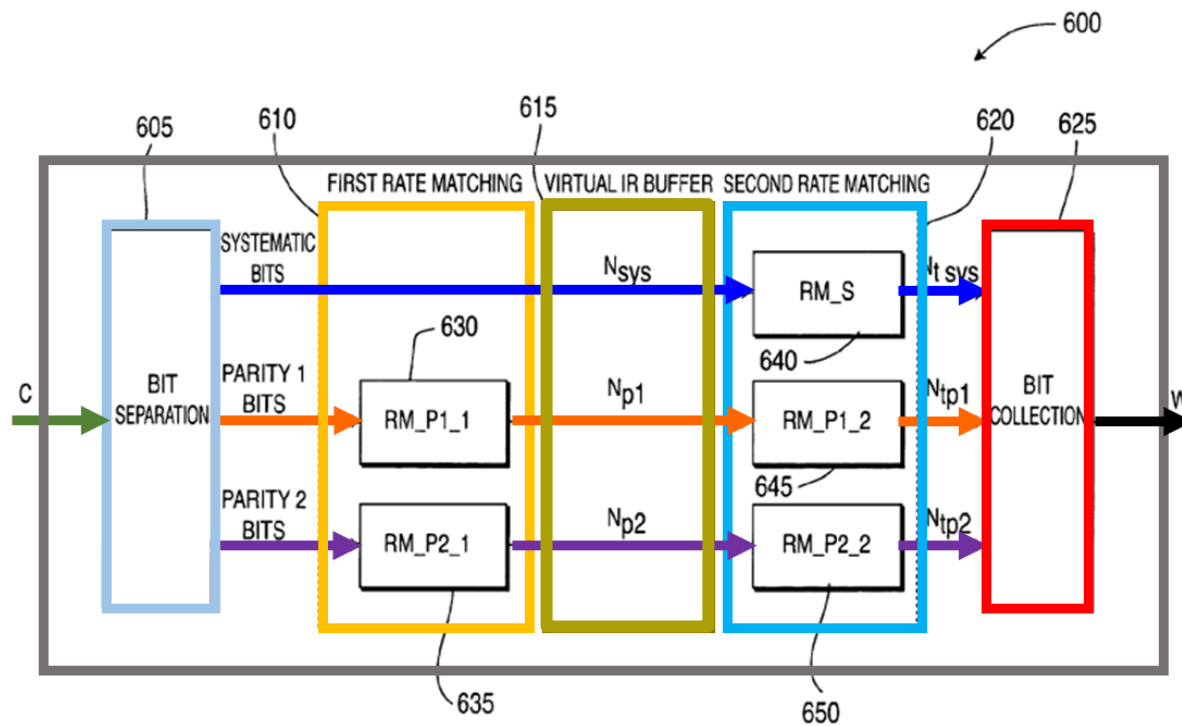


FIG. 10

60. Specifically, Fig. 10 depicts circuitry that implements the '486 patent's purportedly novel rate-matching process. '486, 6:31-45, Fig.10. The circuitry includes a: **bit separation circuit**, **first rate-matching stage**, **virtual incremental redundancy (IR) buffer**, **second rate matching stage**, and **bit collection circuit**. '486, Fig. 10. The **bit separation circuit** receives an input **signal** which it then separates into multiple bit streams: a **systematic bit stream**, **first parity bit stream**

(“P1”), and **second parity bit stream (“P2”)**. ’486, 6:31-34, 6:40-45, 11:7-11, Fig.

10. The **first rate-matching stage** punctures the parity bit streams if the total number of bits is greater than the size of the **virtual incremental redundancy (IR) buffer**, which entails selectively deleting enough bits so that the remaining bits are able to fit in the IR buffer. ’486, 5:5-7, 6:26-51, 8:16-20, 12:30-36, 16:19-23, Fig.10. Puncturing is a well-known process in the prior art. For example, European Patent Publication E.P. 0865172 to Honkasalo, which I understand was published on 9/4/2002, (“Honkasalo”, Ex. 1014) describes a puncturing process that is used to “delete some of the symbols from the data stream.” Honkasalo, [0039]. As another example, U.S. 6,356,601 to Chen, which I understand has an effective filing date of 9/1/1999, (“Chen”, Ex. 1015) describes a puncturing process that “removes, some of the symbols in accordance with a particular puncturing pattern.” Chen, 4:50-56.

61. The bit streams are then read into (e.g., buffered in) the **virtual incremental redundancy (IR) buffer**. ’486, Fig. 10, 4:60-5:8, 6:23-51, 8:16-27, 12:1-9, 12:30-36. The **second rate matching stage** selects systematic bits over both sets of parity bits for transmission or selects parity bits over systematic bits for transmission depending on redundancy versions parameters. ’486, 6:26-40, 16:24-26, 18:15-20:20, Tables 1-2, Fig.10. For example, the ’486 teaches two redundancy version parameters, ‘s’ and ‘r,’ and when ‘s’ is set to 1, the systematic bits are

prioritized; whereas, when ‘s’ is set to 0, the parity bits are prioritized. ’486, 18:15-17, Fig.10. The **second rate matching stage** outputs the selected bits which are fed into the **bit collection circuit** where they are combined into an output (“N_{data}”) for transmission. ’486, 6:40-47, 16:38-39, Fig.10.

62. The above discussion shows that the Challenged Claims of the ’486 patent are based on disclosures copied from the prior art, and implemented in a conventional manner. Even to the extent that it is argued that the Challenged Claims of the ’486 patent were an improvement upon the prior art, as I explain further below, **Stewart** alone, or in view of **Motorola**, **3GPP-Summary**, and/or **TS25.212** discloses or renders obvious the same aspects to a person of ordinary skill in the art. For example, **Stewart** also improved upon a similar downlink disclosure from an earlier version 3.5.0 of 3GPP TS 25.212. Stewart, 3:47-63, Fig. 2. Ex. 1036.

B. Prosecution History of the ’486 Patent

63. In formulating my opinions, I considered the contents of the prosecution history of the ’486 patent, a copy of which has been designated as Exhibit 1002 (“’486 FH”). The prosecution history shows that the Challenged Claims of the ’486 were allowed without any merit-based rejections of the Challenged Claims over prior art, other than a double patenting rejection over a parent patent U.S. 8,074,143 (“’143 patent”, Ex. 1046), without other rejections over

other prior art references. The USPTO rejected the originally-filed claims of the application that led to the '486 patent under what I have been informed to be a judicially-created doctrine of obviousness-type double patenting in an Office Action dated 10/3/2014. Ex. 1002, 86-91. In the same office action, the USPTO cited but did not analyze two references (U.S. 2009/0041110, Ex. 1020 and U.S. 8,726,121, Ex. 1021). The applicant overcame this rejection by filing a terminal disclaimer over the parent '143 patent. Ex. 1002, 103-110, at 107-119. A Notice of Allowance was issued by the USPTO on 2/17/2015. Ex. 1002, 118-119. The '486 issued thereafter, on 6/23/2015. Ex. 1002, 139. During prosecution, the USPTO did not otherwise reject the Challenged Claims over any prior art reference other than the parent patent.

64. I understand that the '486 patent is a continuation of a chain of four patent applications, and each of these applications led to a patent: U.S. Patent App. No. 13/744,984 now U.S. Patent No. 8,788,920; U.S. Patent App. No. 13/309,962, now U.S. Patent No. 8,359,520; U.S. Patent App. No. 11/974,381, now U.S. Patent No. 8,074,143; U.S. Patent App. No. 10/725,779, now U.S. Patent No. 7,293,217. In my review of the earlier applications in the priority chain, I have not seen substantive discussion of prior art relevant to the Challenged Claims. Ex. 1016; Ex. 1017; Ex. 1018; Ex. 1019.

VI. THE '486 PATENT PRIORITY DATE

65. I understand the '486 patent was filed on 6/10/2014, and claims priority to three provisional applications: U.S. Prov. App. No. 60/470,921 filed 5/15/2003, U.S. Prov. App. No. 60/444,068 filed on 1/30/2003, U.S. Prov. App. No. 60/434,232 filed on 12/16/2002. Exhibits 1002, 1016-1019. I have not formulated any opinion about the correct priority date for the '486 patent. For purposes of this declaration, I was asked to assume, with respect to each of the prior art Grounds discussed in this declaration, that the '486 patent is entitled to the alleged priority date of 12/16/2002. As further discussed below, regardless of whether the '486 is entitled to a 12/16/2002 priority date based on its earliest provisional application, each of **Stewart, Motorola, 3GPP-Summary**, and **TS25.212** is prior art to the Challenged Claims in any event. I have been instructed to consider the patent and the prior art from the perspective of a person of ordinary skill in the art as of 12/16/2002. However, a later or earlier priority date would not impact my opinions as long as these references are still prior art.

VII. LEVEL OF ORDINARY SKILL

66. In rendering the opinions set forth in this declaration, I was asked to consider the Challenged Claims of the '486 and the prior art cited in this declaration through the eyes of a person of ordinary skill in the art at the time of the alleged

invention. I understand determining the ordinary level of skill in a field of art includes looking at multiple factors including: (1) the level of education and practical experience; (2) the types of problems encountered in the field; (3) the teachings of the prior art; and (4) the sophistication of the technology at the time of the alleged invention. I understand that a person of ordinary skill in the art is not a real individual, rather a hypothetical individual having a certain set of qualities that embody the aforementioned factors listed. I understand that a person of ordinary skill in the art would also have knowledge from the teachings of the prior art, including the prior art cited in this declaration.

67. In my opinion, on or before the '486 patent's alleged priority date of 12/16/2002, a person of ordinary skill in the art relating to the technology of the '486 patent would have had a bachelor's degree in electrical and computer engineering, computer science, or the equivalent thereof, and at least two years of experience with networking and wireless communications systems. Additional graduate education could substitute for practical experience, or significant practice experience in the field could substitute for formal education. '486, 1:26-4:49.

68. I am qualified to opine concerning what a person of ordinary skill in the art would have known and understood at that time of the alleged invention. Indeed, by 12/16/2002, my level of skill in the art was at least that of a person of ordinary

skill, as I have defined above. My analysis and conclusions herein are from the perspective of a person of ordinary skill in the art as of 12/16/2002.

VIII. CLAIM CONSTRUCTION

69. In rendering the opinions set forth in this declaration, I was instructed that the Challenged Claims of the '486 patent are to be given their ordinary and customary meaning as understood by a person of ordinary skill in the art at the time of the alleged invention. I understand this meaning may shift in light of the '486 patent's specification and prosecution history pertaining to it and its patent family. I have followed these principles in the analysis I lay out in this declaration.

70. I understand that there is a pending district court litigation between Petitioner and Pantech involving the '486 patent, and the parties have not proposed any constructions for the '486 patent as reflected in Exhibit 1047. Thus, those constructions do not impact the opinions set forth in this declaration.

A. Preambles

71. I understand the preamble of a claim may or may not be limiting. For the purposes of this declaration, I have not been asked to formulate any opinion as to whether the preamble of any claim is limiting or not, nor have I formed any such opinion. However, as I will discuss further below, regardless of whether the

preambles are limiting, the prior art discloses the preambles. *See* Section IX (Grounds of Unpatentability).

B. Means-Plus-Function

72. For the purposes of this declaration, I was asked to analyze limitations [1.e] and [5.a]-[5.e] and whether these limitations would be met by the prior art Grounds discussed herein, to the extent these limitations are means plus function limitations having the structure and function set forth below. I have not developed these constructions. Regardless, as I discuss below, the prior art discloses and/or renders obvious the Challenged Claims, even if limitations [1.e] and [5.a]-[5.e] were construed to be means plus function limitations.

<i>Limitation</i>	<i>Structure</i>	<i>Function</i>
[5.a] circuitry configured to interleave systematic bits;	“interleaver” (1:66-2:3, 11:12-25, Fig. 2)	interleaving systematic bits
[5.b] circuitry is further configured to interleave a first parity bit stream;		interleaving first parity bit stream
[5.c] circuitry is further configured to interleave a second parity bit stream;		interleaving second parity bit stream
[5.d] circuitry is further configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and	buffer (6:26-52, Fig. 10)	buffering the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream

<i>Limitation</i>	<i>Structure</i>	<i>Function</i>
[1.e]/[5.e] [a rate matching unit/circuitry is further] configured to select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.	second rate matching stage (6:26-52, Fig. 10) / “microprocessor circuitry” (6:26-58) with algorithm for selecting systematic bits and parity bits for transmission based on a redundancy version by prioritising systematic bits or non systematic bits (18:10-55) (“The parameters of the second rate matching stage depend on the value of the RV parameters s and r. The parameter s can take the value 0 or 1 to distinguish between transmissions that prioritize systematic bits (s=1) and non systematic bits (s=0).”)	selecting bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits

1. The Terms Connote Sufficient Structure to a Person of Ordinary Skill in the Art

73. In the first instance, a person of ordinary skill in the art would have understood that the disputed limitations identified in the table above connote structure.

(a) Interleavers

74. An “interleaver” is a well-known device in the art of wireless communications that is used to interleave a sequence of bits prior to transmission by

permuting the order of bits in order to reduce burst errors and break patterns in the coded information. For example, U.S. 6,631,491 to Shibutani, which I understand has an effective prior art date of at least 8/20/1999, (“Shibutani”, Ex. 1012) Shibutani describes various examples of interleavers that improve error correction ability for “burst error.” Shibutani (Ex. 1012), 1:9-16, 44-48, Figs. 1-50. Shibutani explains that it is “well-known to a person skilled in the art” that the “interleaving method is to randomize the bit sequence of an input bit series and the bit sequence of an output bit series,” and provides an example of a device for performing interleaving in Fig. 50. *Id.*, 27:47-28:5.

75. As another example that interleavers were well-known, U.S. 5,537,420 to Huang, which I understand has an effective filing date of at least 5/4/1994, (“Huang”, Ex. 1013) describes additional types of interleavers that “reduc[e] the effects of burst errors in a digital communication system.” Huang (Ex. 1013), 1:7-9. Huang, like Shibutani, describes “burst errors” in the context of “consecutive errors” and describes using interleavers to mitigate such errors by “spread[ing]” them apart in the non-interleaved signal. Huang (Ex. 1013), 1:26-37. Huang also describes an “interleaver” as including devices that allow “rearrang[ing] (or permut[ing]) the ordering of a sequence of symbols in a deterministic manner.” Huang (Ex. 1013), 1:39-48.

76. For limitations [5.a]-[5.c] that recite “circuitry” configured to “interleave” bits, a person of ordinary skill in the art would have understood such “circuitry” terms to confer structure and implement or are implemented by at least by the “interleavers” disclosed by the ’486 and that were well-known in the art. For example, the ’486 states that “its actual implementation” is “executed by a common circuit or circuits, such as microprocessor circuitry,” indicating that one or multiple known/common circuits implement the claimed circuitry. ’486, 6:52-58. The ’486 describes a “1st interleaving” in prior art Fig. 2. It was well-known to implement “interleavers” in circuitry, as explained by Shibutani (27:47-64, “The above mentioned configuration can be realized by an integrated circuit such as an LSI and the like.”) and Huang (5:58-6:40, “FIG. 2 illustrates, in block diagram form, an interleaver or deinterleaver structure in accordance with the present invention that requires less memory than prior art devices. ... A control circuit 26 is responsive to a clock signal input via terminal 24 to actuate the RAM to either write a symbol into a currently addressed cell or to read a symbol from the currently addressed cell.”; 8:51-60, “the present invention provides a convolutional interleaving/deinterleaving structure that uses a unique address generator circuit formed from a plurality of accumulators with supporting logic.”).

(b) Buffers

77. A “buffer” is a well-known device in the art of wireless communications that is used to carry out buffering, which is a well-known process for temporarily storing information for transmission. For example, the IEEE Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, which I understand to have been published in 2000 (Ex. 1025), describes a buffer as a “device in which data are stored temporarily, in the course of transmission from one point to another; used to compensate for a difference in the flow of data, or time of occurrence of events, when transmitting data from one device to another.” As another example, the Microsoft Computer Dictionary, Fifth Edition, which I understand to have been published in 2002 (Ex. 1026), describes a buffer as “A region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations or devices.” The prevalent use of buffers in the prior art also demonstrates that buffers connote a well-known structure. For example, **3GPP-Summary** describes the use of buffers such as a “ring buffer” and “transmitter buffer.” 3GPP-Summary, §2.4.

78. For limitation [5.d] that recites “circuitry” configured to “buffer” bits, a person of ordinary skill in the art would have understood such “circuitry” term to confer structure and implement or are implemented by at least by the “buffers”

disclosed by the '486, and well-known in the art. As noted above, the '486 states that “its actual implementation” is “executed by a common circuit or circuits, such as microprocessor circuitry,” indicating that one or multiple circuits implement the claimed circuitry. '486, 6:52-58. The '486 describes a “virtual IR buffer 615” as part of “circuitry 600” in Fig. 10, that it copied from the prior art **TS25.212**. '486, 6:26-51, Fig. 10; Ex. 1010, at pp.14-16; TS25.212, Fig. 17, pp.59-60. It was well-known to implement “buffers” in circuitry, as explained by U.S. 2005/0094667 to Dahlman, which I understand has an effective filing date of at least 7/24/2000 (“Dahlman-667”, Ex. 1027). Dahlman-667 describes that its “individual function blocks” including buffers (e.g., Fig. 9) are “implemented using individual hardware circuits, using software functioning in conjunction with a suitably programmed digital microprocessor or general purpose computer, using an Application Specific Integrated Circuit (ASIC), and/or using one or more Digital Signal Processors (DSPs).” Dahlman-667 (Ex. 1027), Fig. 9, [0030].

(c) Rate Matching

79. For limitation [1.e], a “rate matching unit” is well-known in the art of wireless communications as a device that is used to select bits for transmission to achieve a certain code rate. For example, U.S. 7,372,837 to Kinjo, which I understand to have an effective filing date of at least 10/11/2002 (“Kinjo,” Ex. 1028),

describes a rate matching stage that selects bits for transmission based on a “redundancy version RV.” Kinjo (Ex. 1028), 2:31-43, 14:41-15:3. **TS25.212**, which is one of the references relied upon in the Grounds, describes a “rate matching stage” that “prioritise[s] systematic bits” or “non systematic bits” depending on “RV [redundancy version] parameters.” TS25.212, p.59. U.S. 7,000,173 to Buckley, which I understand to have an effective filing date of at least 2/11/2002 (“Buckley,” Ex. 1029), describes a rate matching stage that applies a rate-matching algorithm differently to select bits based on a “redundancy version (RV).” Buckley (Ex. 1029), 4:17-34.

80. For limitation [5.e] that recites “circuitry” configured to “select bits for transmission,” a person of ordinary skill in the art would have understood such “circuitry” term to confer structure and implement or are implemented by at least by the “rate matching stage” disclosed by the ’486, and well-known in the art. As noted above, the ’486 states that “its actual implementation” is “executed by a common circuit or circuits, such as microprocessor circuitry,” indicating that one or multiple circuits implement the claimed circuitry. ’486, 6:52-58. The ’486 describes a “second rate matching stage” as part of “circuitry 600” in Fig. 10 that prioritises systematic bits or non systematic bits depending on a redundancy version. ’486, 6:26-51, 18:15-22, Fig. 10. As noted above, the ’486 copied disclosures from the

prior art **TS25.212**. '486, 6:26-51, Fig. 10; Ex. 1010, at pp.14-16; TS25.212, Fig. 17, pp.59-60. It was well-known to implement “rate matching stages” in circuitry, as explained by Kinjo, which describes a “second rate matching circuitry” that is controlled by “RV [redundancy version]” parameters. Kinjo (Ex. 1028), 2:12-43, 2:62-3:7.

(d) Circuitry

81. Each of limitations [5.a]-[5.e] requires “circuitry configured to” implement the components of limitations [1.a]-[1.e]. Not only would a person of ordinary skill in the art have understood that such terms confer structure and implement or are implemented by the respective components (interleavers, buffers, rate matching units) as discussed above in Sections VIII.B.1(a) (Interleavers), VIII.B.1(b) (Buffers), VIII.B.1(c) (Rate Matching), but the person of ordinary skill in the art would also have understood that “circuitry” itself connotes structure.

82. For example, U.S. 7,020,455 to Krishnarajah, which I understand to have an effective filing date of at least 9/30/2002, (“Krishnarajah,” Ex. 1030), describes that a “user equipment [] includes data processing circuitry” and “transceiving circuitry.” Krishnarajah (Ex. 1030), Fig. 7A, 7:5-22.

83. It was further well-known in the art that circuitry implemented multiple components and operations. For example, U.S. 6,760,365 to Demir, which I

understand has an effective filing date of at least 10/9/2002, (“Demir”, Ex. 1031) describes that a “UE has a synchronization circuit,” “detection circuit” and “decision circuit.” Demir (Ex. 1031), 2:50-59 (“The present invention discloses a circuit for a User Equipment (UE) that performs the acquisition”), 3:4-24 (“The UE has a synchronization circuit for processing the received communication signal samples.”); “A detection circuit is operatively associated with the correlator ...”), 4:11-44.

84. As another example, E.P. 1209856A1 to Miya, which I understand has a publication date of at least 5/29/2002, (“Miya”, Ex. 1032) describes multiple circuits including a “synchronization circuit,” “demodulation circuit,” and radio circuit. Miya (Ex. 1032), Fig. 7, [0039]-[0051].

2. Even if the Claims were construed as means plus function limitations, the prior art Grounds disclose the claimed structure

85. If limitations [1.e] and [5.a]-[5.e] were construed as means plus function terms, it is my opinion that the art expressly discloses the respective claimed structure as shown in the tables below. Each of the references below, **Stewart**, **3GPP-Summary**, and **TS25.212** discloses to a person of ordinary skill in the art a UE or mobile station processor that carries out the respective algorithms cited in the table below, and does so at least in the same manner as the '486 patent. The '486 patent states that a “wireless transmit/receive unit (WTRU)” (e.g., as required by

Challenged Claim 5) “includes but is not limited to a UE, mobile station, fixed or mobile subscriber unit, pager, or any other type of device capable of operating in a wireless environment.” ’486, 4:60-5:12.

86. The teachings of **Stewart**, **3GPP-Summary** and **TS25.212** are equally applicable to both downlink and uplink connections. However, to the extent it is argued that their teachings are directed to downlink operations, a person of ordinary skill in the art also would have understood and alternatively found it obvious modify the teachings of those references to be used in an uplink connection to support incremental redundancy, and would have had a reasonable expectation of success when doing so. As an example, Kinjo teaches that a rate matching process that supports incremental redundancy in a downlink “may also be used during an uplink transmission” where “there is no real demand to increase the throughput during an uplink transmission” and that such a process was “equally applicable to an uplink transmission.” Kinjo, 6:55-64.

87. A person of ordinary skill in the art would have understood, or at least found it obvious that a UE, mobile station, or other device operating in a wireless environment includes a processor. For example, U.S. 6,754,253 to Guey, which I understand to have an effective filing date of 11/29/2000 (“Guey,” Ex. 1033), teaches that a “[m]obile terminal 100 comprises a microcontroller unit (MCU) 101,

an RF transceiver 110, a digital signal processor (DSP) 150,” and that a “microcontroller unit 101 typically comprises a microprocessor.” Guey (Ex. 1033), 3:41-45. U.S. 6,760,600 to Nickum, which I understand to have an effective filing date of 1/27/1999 (“Nickum,” Ex. 1034). Nickum, teaches that a “two digital signal processors (DSPs), a main DSP and a secondary or sub DSP, may be used in the communication apparatus to handle input and output functions of the communication apparatus” and that “Two digital signal processors (DSPs) 42 and 44, with associated circuitry, may be connected or built in to the cellular telephone 14 to assist in the control of the communication and power connection interfaces.” Nickum (Ex. 1034), 2:63-67, 4:57-5:5. U.S. 6,515,980 to Bottomley, which I understand to have an effective filing date of 9/22/1999 (“Bottomley,” Ex. 1035). Bottomley, teaches that a “wireless terminal” “includes a controller 370, such as a microprocessor, microcontroller or similar data processing device, that executes program instructions stored in a memory 360, such as a dynamic random access memory (DRAM), electrically erasable programmable read only memory (EEPROM) or other storage device.” Bottomley (Ex. 1035), 7:51-67, Fig. 3.

88. As shown in the table below, **Stewart** discloses the same structure as the '486 patent for each of the claim limitations.

Limitation	'486 Structure	Stewart
[5.a] circuitry configured to interleave systematic bits;	“interleaver” (1:66-2:3, 11:12-25, Fig. 2)	“systematic block interleaver” (Figs. 4-5); Stewart’s interleaver reads in bits and rearranges the bits (e.g., by permuting) in a different order for output (4:14-5:5) (“having data read in a column-wise fashion into each interleaver,” “To facilitate flexibility in supporting variable coding rates in the present invention, both columns and rows are permuted prior to reading out the block matrix contents,” and “codeword data row-wise from top-to-bottom from the block matrix”) The interleavers of the '486 and Stewart read bits into the interleaver and rearrange them in a different order before output.
[5.b] circuitry is further configured to interleave a first parity bit stream;		“parity block interleaver” (Fig. 4-5); Stewart’s interleaver reads in bits and rearranges the bits (e.g., by permuting and arranging by row) in a different order for output (4:14-5:5) (“having data read in a column-wise fashion into each interleaver,” “To facilitate flexibility in supporting variable coding rates in the present invention, both columns and rows are permuted prior to
[5.c] circuitry is further configured to interleave a second parity bit stream;		“parity block interleaver” (Fig. 4-5); Stewart’s interleaver reads in bits and rearranges the bits (e.g., by permuting and arranging by row) in a different order for output (4:14-5:5) (“having data read in a column-wise fashion into each interleaver,” “To facilitate flexibility in supporting variable coding rates in the present invention, both columns and rows are permuted prior to

Limitation	'486 Structure	Stewart
		reading out the block matrix contents,” and “codeword data row-wise from top-to-bottom from the block matrix”) The interleavers of the '486 and Stewart read bits into the interleaver, and rearrange them in a different order before output.
[5.d] a circuitry is further configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and	buffer (6:26-52, 16:17-26, Fig. 10)	“block matrix” (4:14-5:5, Fig. 4, Fig. 5); The buffer of the '486 and block matrix of Stewart load bits into a device for storage.
[1.e]/[5.e] [a rate matching unit/circuitry is further] configured to select bits for transmission based	second rate matching stage (6:26-52, Fig. 10) / “microprocessor circuitry” (6:26-58) with algorithm for selecting systematic bits and	“redundancy version selector” Fig. 3 (2:25-26, 3:64-4:13, 5:57-13:13, Fig. 3); ¹ UE processor performing selecting of systematic bits over

¹ As discussed above in Section VIII.B.2 (Even if the Claims were construed as means plus function limitations, the prior art Grounds disclose the claimed structure), a person of ordinary skill in the art would have understood, or at least found it obvious that a UE, mobile station, or other device operating in a wireless environment, such as those in **Stewart**, includes a processor.

Limitation	'486 Structure	Stewart
on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.	parity bits for transmission based on a redundancy version by prioritising systematic bits or non systematic bits (18:10-55) (“The parameters of the second rate matching stage depend on the value of the RV parameters s and r. The parameter s can take the value 0 or 1 to distinguish between transmissions that prioritize systematic bits ($s=1$) and non systematic bits ($s=0$).”)	parity bits and vice versa based on a redundancy version by an algorithm that selects bits for transmission based on a redundancy version by selecting a starting row in a systematic block interleaver or parity block interleaver based on a redundancy version, to transmits systematic bits before parity bits or vice versa; or more systematic bits than parity bits, or vice versa (2:25-26, 3:64-4:13, 5:57-13:13, Fig. 3) (“In order to support different redundancy versions, any row of any block puncturing interleaver may be assigned as a starting point at which to commence the readout of codeword bits. By defining multiple starting points for one redundancy version, the order and/or the ratio in which codeword bits are be read out from the systematic and parity interleavers can provide further degrees of freedom in describing any potential redundancy version.”) The selecting algorithms of the '486 and Stewart both select bits for transmission based on a redundancy version.

89. As shown in the table below, **3GPP-Summary** discloses the same structure as the '486 patent for the buffer limitation limitations [1.d]/[5.d]. As discussed in the Grounds below, 3GPP-Summary is relied upon to show the buffer limitations [1.d]/[5.d].

90. As shown in the table below, **3GPP-Summary** discloses the same structure as the '486 patent for each of the claim limitations.

Limitation	'486 Structure	3GPP-Summary
[1.d]/[5.d] [a buffer/circuitry is further] configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and	buffer (6:26-52, Fig. 10)	“buffering memory,” “buffer,” “ring buffer,” “transmitter buffer” that stores “interleaved systematic bits” and “interleaved parity bits” (§§1, 2.4) The buffers of the '486 and 3GPP-Summary store bits.

91. As shown in the table below, **TS25.212** discloses the same structure as the '486 patent for each of the claim limitations. With respect to **TS25.212**, each of the cited disclosures have been copied from **TS25.212** into the '486 as noted above, and thus would provide the same structure as disclosed by the sections copied into **TS25.212**. Ex. 1010, at pp.14-16; TS25.212, Fig. 17, pp.59-60.

Limitation	'486 Structure	TS25.212
[5.d] circuitry is further configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and	“Virtual IR buffer” (6:26-52, 16:17-26, Fig. 10) ²	“Virtual IR buffer” (§4.5.4, Fig. 17);
[1.e]/[5.e] [a rate matching unit/circuitry is further] configured to select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version	second rate matching stage (16:17-26, 6:26-52, 18:10-19:13, Fig. 10) ³ / “microprocessor circuitry” (6:26-58) with algorithm for selecting systematic bits and parity bits for transmission based on a redundancy version by prioritising systematic bits or non systematic bits (18:10-55) (“The parameters of the second rate matching stage depend on the value of the RV parameters s and	“second rate matching stage” (§4.5.4, Fig. 17); UE processor performing selecting of systematic bits over parity bits and vice versa based on a redundancy version by an algorithm that selects bits for transmission based on a redundancy version by prioritising systematic bits or non systematic bits (§4.5.4.3) (“The parameters of the second rate matching stage depend on the value of the RV parameters s and r. The parameter s can take the value 0 or 1 to distinguish

² The '486 (16:17-26, Fig. 10) copied this disclosure from **TS25.212** (§§4.5.4, 4.5.4.2, Fig. 17).

³ The '486 (16:17-26, 18:10-19:13, Fig. 10) copied this disclosure from **TS25.212** (§§4.5.4, 4.5.4.3, Fig. 17).

Limitation	'486 Structure	TS25.212
of the set selects first and second parity bits over systematic bits.	r. The parameter s can take the value 0 or 1 to distinguish between transmissions that prioritize systematic bits (s=1) and non systematic bits (s=0).")	between transmissions that prioritize systematic bits (s=1) and non systematic bits (s=0).") The selecting algorithms of the '486 and TS25.212 both select bits for transmission based on a redundancy version.

3. Even if the Claims were construed as means plus function limitations, the prior art Grounds disclose equivalents of the claimed structure

92. If limitations [1.e] and [5.a]-[5.e] were construed as means plus function terms, it is my opinion that the art discloses the claimed structure's equivalents by performing substantially the same functions, in substantially the same way, to achieve the same result as set forth in the tables below.

Limitation ⁴	Stewart's Disclosures	DOE Analysis
[5.a] circuitry configured to <i>interleave systematic bits</i> ;	"systematic block interleaver" (Figs. 4-5, 4:46-5:5);	Stewart's "systematic block interleaver" (Fig. 4) performs the same function of "interleav[ing] systematic bits" in substantially the same way (e.g., by reading data and reorganizing the bits) as the '486 to achieve the same result of interleaved systematic bits.

⁴ Functions are emphasized in ***bold and italics***.

Limitation ⁴	Stewart's Disclosures	DOE Analysis
[5.b] circuitry is further configured to <i>interleave a first parity bit stream</i>; [5.c] circuitry is further configured to <i>interleave a second parity bit stream</i>;	“parity block interleaver” (Fig. 4-5, 4:14-5:5) (“Preferably, the parity bits are combined into one Nrow×Ncol puncturing matrix, but separate Nrow×Ncol parity block interleavers can be used for each parity stream.”)	Stewart's “parity block interleaver[s]” (Fig. 4, 4:46-5:5) performs the same function of “interleav[ing]” “a first parity bit stream” and a “second parity bit stream” in substantially the same way (e.g., by reading data and reorganizing the bits) as the '486 to achieve the same result of an interleaved first parity bitstream and second parity bitstream.
[5.d] circuitry is further configured to <i>buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream</i>; and	“block matrix” (4:14-5:5, Fig. 4, Fig. 5);	Stewart's “block matrix” performs the same function of “buffer[ing] interleaved” systematic and parity bits in substantially the same way (e.g., by storing interleaved bits) as the '486 to achieve the same result of stored bits.
[1.e]/[5.e] [a rate matching unit/circuitry is further] configured to <i>select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one</i>	“redundancy version selector” Fig. 3 (2:25-26, 3:64-4:13, 5:57-13:13, Fig. 3); UE processor performing selecting of systematic bits over parity bits and vice versa based on a redundancy version by an algorithm that selects bits for transmission based on a redundancy version by selecting a starting row in a systematic block interleaver or parity	Stewart's “redundancy version selector” and UE processor perform the same function of “select[ing] bits for transmission” based on a plurality of “redundancy versions” in substantially the same way (e.g., by transmitting systematic bits before parity bits, or parity bits before systematic bits based on a redundancy version, or more systematic bits than parity bits or more parity bits than systematic bits based on a redundancy version) as the '486 to achieve the

Limitation ⁴	Stewart's Disclosures	DOE Analysis
<i>redundancy version of the set selects first and second parity bits over systematic bits.</i>	block interleaver based on a redundancy version, to transmits systematic bits before parity bits or vice versa; or more systematic bits than parity bits, or vice versa (2:25-26; 3:64-4:13, , 5:57-9:13; Fig. 3) (“In order to support different redundancy versions, any row of any block puncturing interleaver may be assigned as a starting point at which to commence the readout of codeword bits. By defining multiple starting points for one redundancy version, the order and/or the ratio in which codeword bits are be read out from the systematic and parity interleavers can provide further degrees of freedom in describing any potential redundancy version.”)	same result of selected bits for transmission.

Limitation	3GPP-Summary's Disclosures	DOE Analysis
[5.d] [a buffer/circuitry is further] configured	“buffering memory,” “buffer” “transmitter buffer” that stores	3GPP's “buffer” performs the same function of “buffer[ing] interleaved” systematic and parity

to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream;	“interleaved systematic bits” and “interleaved parity bits” (§§1, 2.4)	bits in substantially the same way (e.g., by storing bits) as the ’486 to achieve the same result of stored bits.
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Limitation	TS25.212’s Disclosures	DOE Analysis
[5.d] circuitry is further configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and	“Virtual IR buffer” (6:26-52, 16:17-26, 16:66-17:2, Fig. 10)	TS25.212’s “Virtual IR buffer” performs the same function of “buffer[ing] interleaved” systematic and parity bits in substantially the same way (e.g., by storing bits) as the ’486 to achieve the same result of stored bits.
[1.e]/[5.e] [a rate matching unit/circuitry is further] configured to select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version	“second rate matching stage” (§4.5.4, Fig. 17); UE processor performing selecting of systematic bits over parity bits and vice versa based on a redundancy version by an algorithm that selects bits for transmission based on a redundancy version by prioritising systematic bits or non-systematic bits (§4.5.4.3) (“The parameters of the second rate matching stage	TS25.212’s “second rate matching stage” performs the same function “select[ing] bits for transmission” based on a plurality of redundancy versions ...” in substantially the same way (e.g., prioritising systematic bits or non-systematic bits for transmission based on a redundancy version) as the ’486 to achieve the same result of selected bits for transmission.

Limitation	TS25.212's Disclosures	DOE Analysis
of the set selects first and second parity bits over systematic bits.	depend on the value of the RV parameters s and r. The parameter s can take the value 0 or 1 to distinguish between transmissions that prioritize systematic bits (s=1) and non systematic bits (s=0).”)	

IX. GROUNDS OF UNPATENTABILITY

93. In this section, I explain why the teachings from the following references alone or in combination disclose and/or render obvious each of the Challenged Claims. I have been instructed to assume that each of these references qualifies as prior art. I understand that Petitioner has retained Dr. Friedhelm Rodermund, an expert on 3GPP proceedings, to provide testimony regarding public accessibility of **Motorola, 3GPP-Summary** and **TS25.212**. The table below incorporates his analysis. *See* Declaration of Friedhelm Rodermund in Support of Petition for *Inter Partes* Review of U.S. Patent No. 9,065,486 (“Rodermund”, Ex. 1004). I have reviewed Dr. Rodermund’s declaration and agree with his analysis which is incorporated into the table below with respect to **Motorola, 3GPP-Summary** and **TS25.212**. Rodermund, ¶¶1-181.

Name	Publication/ Title	Exhibit	Filed	Published/ Issued
Stewart	U.S. Patent 7,260,770	1005	10/22/2001	8/21/2007
Motorola ⁵	R1-01-1014/ R1-01-1081	1006	N/A	By 1/2002 ⁶
3GPP- Summary	R1-01-1047	1007	N/A	By 1/2002

⁵ In my analysis, I have considered two versions of Motorola, R1-01-1014 and R1-01-1081, which are substantively the same. The substantively same disclosures are reflected by a comparison of R1-01-1014 (Ex. 1006) and R1-01-1081 (Ex. 1087). *See* Ex. 1088 (redline comparison between R1-01-1014 and R1-01-1081). Because the citations to both documents are identical, my citations throughout this declaration refer to both R1-01-1014 and R1-01-1081.

⁶ I understand from Dr. Rodermund's analysis that R1-01-1081, a substantively similar version of R1-01-1041, was presented and discussed at 3GPP RAN WG1 HSDPA Ad-Hoc meeting by no later than November 7, 2001. My analysis herein applies to both R1-01-1041 and R1-01-1081. Ex. 1087; Ex. 1088; Rodermund, ¶¶100-102.

Name	Publication/ Title	Exhibit	Filed	Published/ Issued
TS25.212	TS 25.212 v5.1.0	1008	N/A	By 12/15/2002 ⁷

94. As I explain below, the Challenged Claims are invalid based upon the following prior art grounds:

95. **Ground 1:** Challenged Claims 1-6 are anticipated or rendered obvious by **Stewart**.

96. **Ground 2:** Challenged Claims 1-6 are rendered obvious by **Stewart** in view of **3GPP-Summary**.

97. **Ground 3:** Challenged Claims 1-6 are rendered obvious by **Stewart** in view of **TS25.212**.

98. **Ground 4:** Challenged Claims 1-6 are rendered obvious by **Stewart** in view of **Motorola**.

⁷ I understand from Dr. Rodermund's analysis that in addition to publication of **TS25.212** by the 3rd Generation Partnership Project (3GPP), the ETSI organization also published a substantively identical version TS 125.212 v5.1.0 (Ex. 1094). My analysis with respect to TS25.212 applies equally to ETSI's TS 125.212. Ex. 1094; Rodermund, ¶¶122-125.

99. **Ground 5:** Challenged Claims 1-6 are rendered obvious by **Stewart** in view of **3GPP-Summary** and **Motorola**.

100. **Ground 6:** Challenged Claims 1-6 are rendered obvious by **Stewart** in view of **TS25.212** and **Motorola**.

101. It is my opinion that Challenged Claims of the '486 patent are unpatentable as explained below. I note that in this discussion, I may focus on the particular language in the specific claims, but it should be understood that my analysis applies to the corresponding elements of all Challenged Claims containing identical or substantially identical language.

A. Ground 1: Stewart (Claims 1-6)

102. Here, I explain why the teachings from **Stewart** anticipate and render obvious each of the Challenged Claims.

1. Overview of Stewart

103. **Stewart**, titled “Block puncturing for turbo case based incremental redundancy,” and like the '486 patent, is directed to a process that entails selecting between systematic bits and parity bits for transmission based on a redundancy version” selected from a plurality of redundancy versions that includes a subset that selects systematic bits over parity bits and another subset that selects parity bits over systematic bits. **Stewart**, Abstract, 1:44-64, 3:25-36, 4:14-19, 5:57-7:24. The

channel coding process disclosed in **Stewart** is depicted in Fig. 1 (color coded, below) and Fig. 4 (color coded, below). As was well-known in the prior art and illustrated in Fig. 1, **Stewart's** system entails a channel coding process that outputs **systematic bits** (e.g., " b_k ") and a set of parity bit streams (e.g., " p_{1k} " and " p_{2k} "), which are generated from the **systematic bits**. Stewart, 1:32-43, Fig. 1. Although there are channel coding processes that generate more than 2 parity streams, **Stewart** describes an example of two parity bit streams that includes **first parity bits** (" p_{1k} ") and **second parity bits** (" p_{2k} "). Stewart, 9:54-60, Fig. 1.

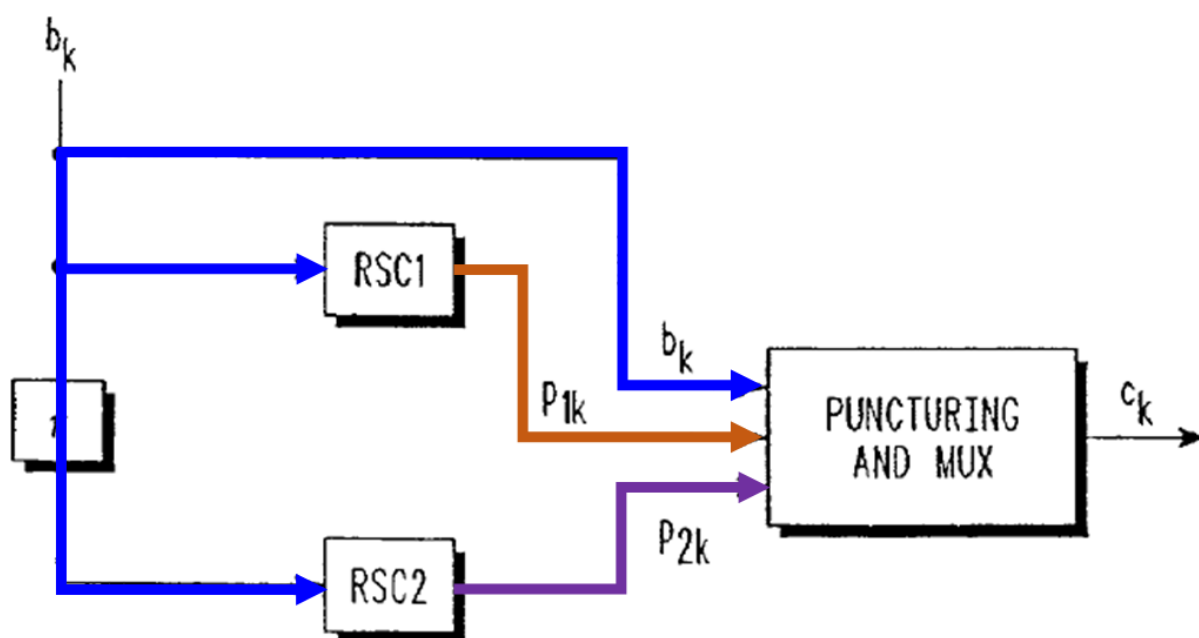


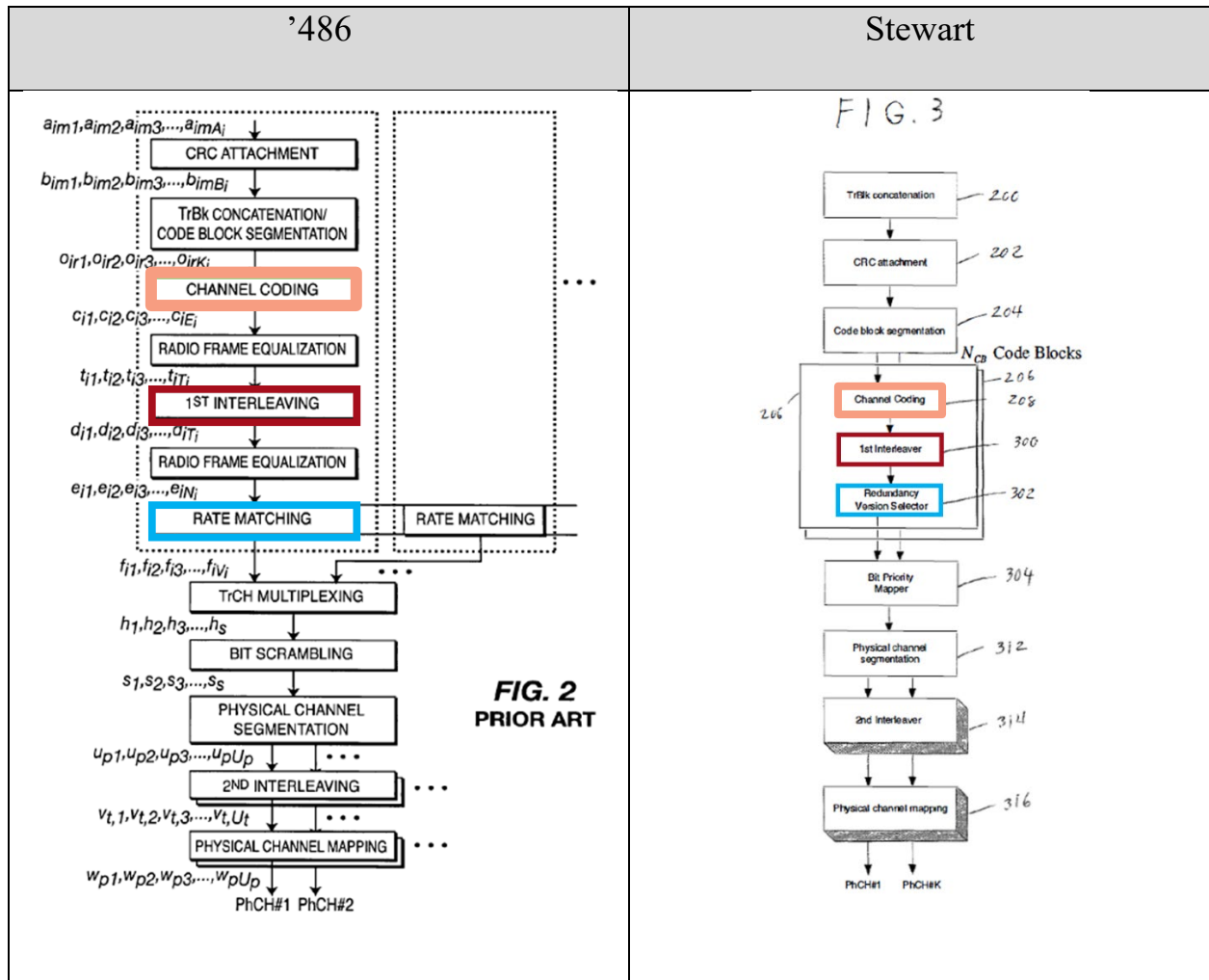
FIG. 1
- PRIOR ART -

104. As **Stewart** explains, and as was well known in the prior art, the purpose of the parity bits is to implement error detection and correction in an incremental redundancy process in which different numbers of systematic bits and parity bits are transmitted to achieve a desired target code rate. Stewart, 1:32-64, 2:60-64, 3:25-30, 5:6-8, 5:33-40, 7:55-62. The selected bits, which depend on a redundancy version parameter, are read out from memory starting from a starting point in the memory. Stewart, Fig. 3, Abstract, 1:32-64, 2:45-67, 3:64-4:13, 4:56-5:5, 5:62-65, 6:41-49, 6:56-7:24. The total number of bits that are selected for transmission depends on this starting point.

105. Both **Stewart** and the '486 patent are based on versions of the 3GPP TS 25.212. Stewart, 3:47-63, Fig. 2; Ex. 1036, Fig. 1; '486, Fig. 2; TS25.212, Fig. 1. **Stewart** acknowledges that an earlier version of TS 25.212 v3.5.0 (Ex. 1036) provided a basis for its disclosures, such as Fig. 2. Fig. 2 of the '486 patent is substantively similar to **TS25.212's** (v3.5.0) Fig. 1, as I noted above and explain below in Section IX.C (Ground 3: Stewart in View of TS25.212 (Claims 1-6)).

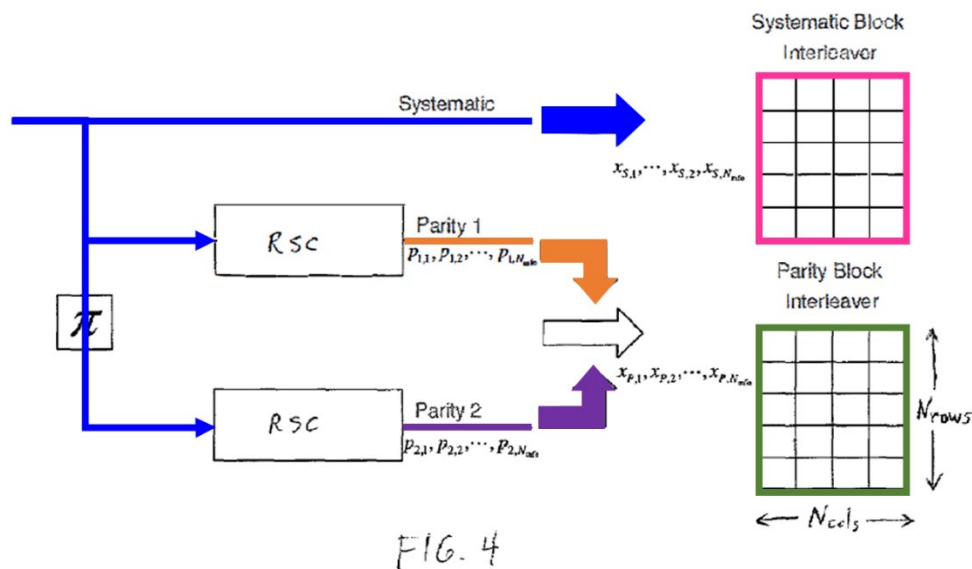
106. Below, I provide a side-by-side comparison of **Stewart's** Fig. 3 and the '486 patent's Fig. 2 to show the similarities between **Stewart** and the '486. Firstly, **Stewart** discloses a process and structure that support the selection between systematic bits and parity bits for transmission that are substantially the same as the

process and structure disclosed in the '486. Secondly, **Stewart** and the '486 disclose interleaving, in an **interleaver**, **systematic bits**, **first parity bits** and **second parity bits** outputted from a **channel coding** process. Stewart, Abstract, 3:7-12, 3:64-4:55, Figs. 3-4. Thirdly, **Stewart** and the '486 disclose buffering the interleaved bits, which is implemented in **Stewart** in the block matrix of the **interleaver**. Stewart, Abstract, 3:64-4:55, Figs. 3-5. Finally, **Stewart** and the '486 disclose selecting between the interleaved buffered systematic bits and parity bits portions of systematic, first parity, and second parity bits based on a redundancy version, which is implemented in **Stewart** by a **redundancy version selector** and in the '486 patent by a **rate-matching process** (*see* Section V.A ('486 Patent Overview)). Stewart, Abstract, 3:7-12, 3:64-4:55, 5:57-6:56, Figs. 3-6.



107. **Stewart** discloses, as depicted in Fig. 4 (color coded, below), that an input signal is separated into **systematic bits**, a **“Parity 1” bit stream**, and a **“Parity 2” bit stream**. Stewart, 4:14-29, Fig. 4. The bit streams are then read into block interleavers made up of N_{row} number of rows and N_{col} number of columns; a block interleaver performs interleaving on a bit stream that entails re-arranging the bits. Stewart, 4:34-36. Specifically, the **systematic bits** are read into a **“Systematic Block Interleaver”** and each parity bit stream is read into a separate **“Parity Block**

Interleaver.” (Note that while Fig. 4 illustrates one parity block interleaver, **Stewart** expressly teaches a case where “separate ... parity block interleavers are used for each parity stream.” Stewart, 4:19-23.) As **Stewart** teaches, interleaving includes at least: (1) inputting a bit stream into the block interleaver (*see, e.g.,* Fig. 5 “Input” arrows)); then (2) rearranging the bit stream (*e.g.,* by permutation or) to reorder the bits for output. Stewart, 4:56-5:5. When the bits have been reordered for output, the bits have been interleaved. The interleaved bits from each stream are buffered in the block matrix corresponding to a respective block interleaver until they are read out from the interleaver for transmission (*see, e.g.,* Fig. 5 “Output” arrows). Stewart, 4:14-5:8, 5:47-56, Figs. 4, 5, 11.



108. After the interleaving and buffering is completed, the systematic bits and parity bits are selected to be read out from the interleavers for transmission based

on a set of redundancy version parameters that are set at the transmitting device. Stewart, Figs. 5, 11, 5:6-8, 9:39-56. **Stewart** teaches that each of the eight redundancy version settings, each specifying a row in the **systematic block interleaver** or **parity block interleaver** that serves as the **starting point** for reading out the bits for transmission. Stewart, 5:62-65, 6:52-7:25.

109. As depicted in **Stewart's** Fig. 6 (color coded, below), **Stewart** teaches a set of redundancy versions which have a **starting point** inside a **systematic block interleaver** (e.g., "RV0"). **Stewart** also teaches a set of redundancy versions that have a **starting point** inside a **[first/second] parity block interleaver** (e.g., "RV1," "RV2," and "RV3"). Stewart, 6:62-7:24, Fig. 6. Similarly as I mentioned above regarding Fig. 4, Fig. 6, too, depicts one parity block interleaver per redundancy version, but **Stewart** expressly teaches using "separate $N_{row} \times N_{col}$ parity block interleavers" for "each parity stream." Stewart, 4:19-23. **Stewart** teaches to start reading at a **starting point** in an interleaver; if the desired number of bits has not been read after the last row in the first parity interleaver has been read out, reading continues at the first row of the same or another interleaver. Stewart, 5:6-15, 5:33-40. 5:50-52, 5:57-6:52.

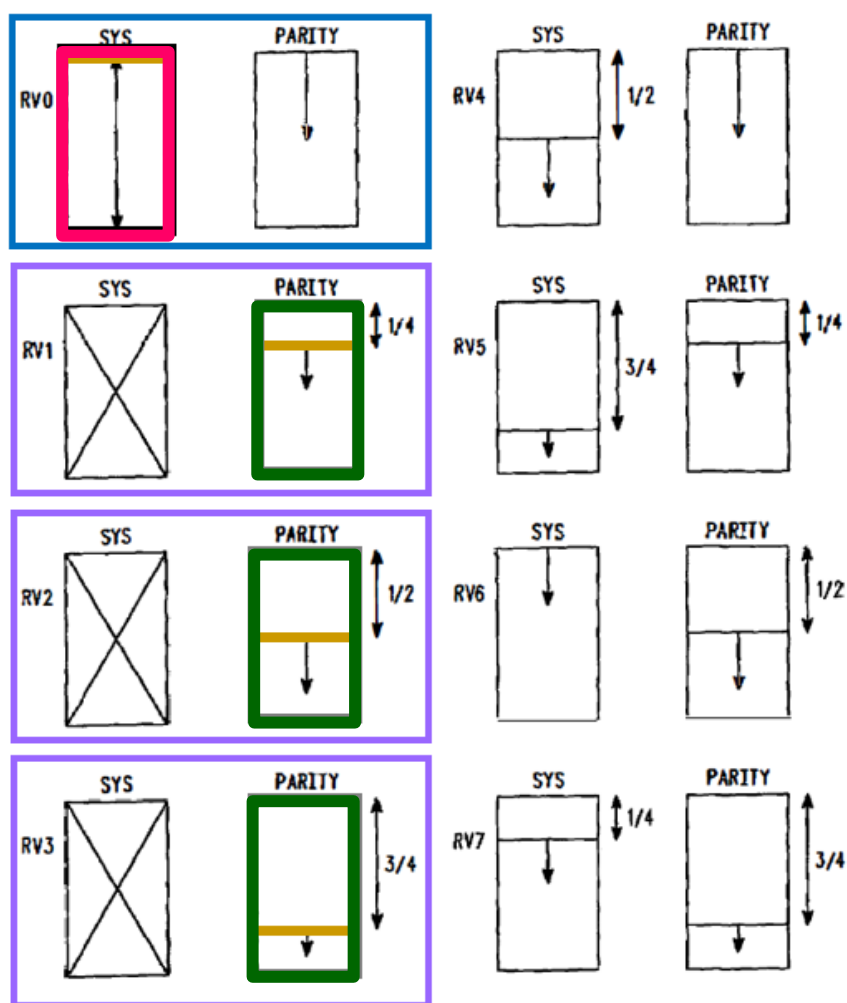
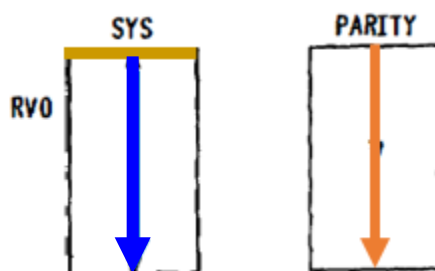


FIG. 6

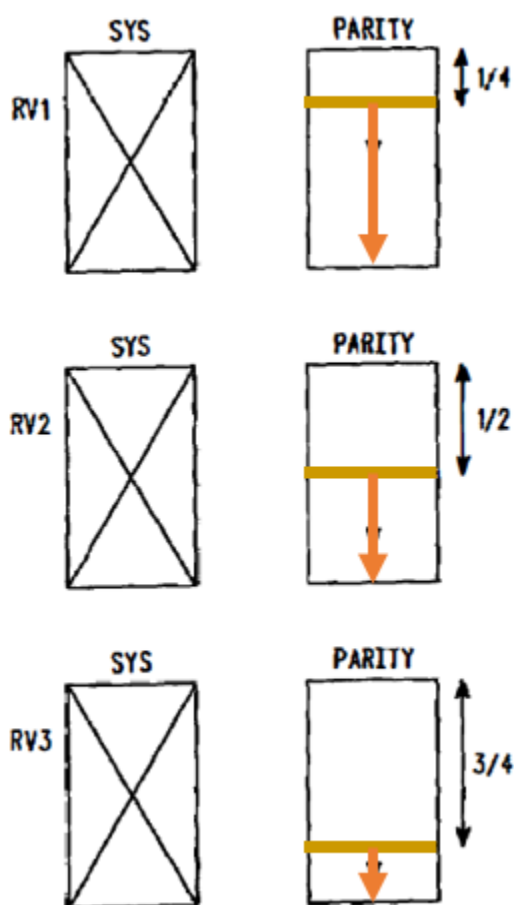
110. **Stewart** teaches a subset of redundancy versions in which systematic bits are transmitted before parity bits. As shown in the figure below (depicting RV0), all **systematic bits** are read before the **parity bits** are. '486, 6:57-61.



111. **Stewart** teaches a set of redundancy versions that result in a larger number of systematic bits selected for transmission than the number of parity bits selected for transmission, *e.g.*, RV0 which is “signaled with enough codeword bits to result in a rate of 3/5.” Stewart 7:27-33. In the context of **Stewart**, code rate refers to the total number of information bits (also referred to as systematic bits) divided by the total number of bits in a transmission. Ex. 1037 (“The effective code rate is defined as $n_i/(n_j+n_p)$, where n_i is the number of information bits and n_p is the number of unique parity bits[.]”), Section IV (Background of the Technology); *see also* Ex. 1009, pp.3-4 (“ratio $R = k/n$ is called the code rate, and can be interpreted as the number of information bits entering the encoder per transmitted symbol.”). For instance, a 3/5 code rate refers to the case in which 3 out of every 5 of the total bits transmitted are systematic bits, and the remaining 2 out of every 5 of the total bits transmitted are parity bits. Accordingly, to achieve a 3/5 code rate, a larger number of systematic bits than parity bits (in aggregate) are selected for transmission. **Stewart** therefore discloses a subset of **redundancy versions that**

select systematic bits over first and second parity bits (e.g., “RV0”). Stewart 7:27-33.

112. **Stewart** also teaches a subset of redundancy versions for which parity bits are selected for transmission before systematic bits. Stewart, 6:62-7:4. *E.g.*, as shown in the figure below (depicting “RV1,” “RV2,” and “RV3”) **Stewart** discloses reading **parity bits**, starting at the **starting point** in an interleaver, towards the last row in the interleaver. Stewart, 5:62-65.



As discussed below in Section IX.A.2(f) (Element [3.e]), with two parity block interleavers, if reading commences in a starting row of a first parity interleaver but the desired number of bits has not been read after the last row in the first parity interleaver has been read out, reading continues at the first row of the same or another interleaver, such as a second parity interleaver followed by the systematic interleaver; if the desired number of bits has not been read after the last row of the second parity interleaver has been read, then reading continues at the first row of another interleaver, such as a systematic interleaver followed by the first parity interleaver. Stewart, 5:33-40. The total number of bits that are to be read out for transmission is based on the payload size and a target code rate. For example, when reading is completed through the last row in the interleaver containing the **starting point** but the desired number of bits to be read out has not yet been reached, **Stewart** teaches to continue reading from (*e.g.*, “wrapping around to”) the first row of the same or another block interleaver. Stewart, 5:33-40. *E.g.*, reading continues in the systematic interleaver after reading completes in the parity interleaver(s). **Stewart** also teaches a redundancy version that results in a larger number of parity bits selected for transmission than systematic bits. For example, **Stewart** teaches a 1/4 code rate is desired with redundancy version four (“RV4”). Stewart, 7:33-34. For example, if when transmitting data, it takes four bits to transmit one bit of

information (for example, if 1 systematic bit and 3 parity bits are transmitted for every bit of information that is successfully transmitted), this results in a 1/4 code rate. Accordingly, one way to achieve a 1/4 code rate, more parity bits than systematic bits (in aggregate) are selected for transmission. Accordingly, where the **starting point** is located in a parity block interleaver (*e.g.*, “RV1,” “RV2,” “RV3”), **Stewart** discloses **redundancy versions that select first and second parity bits over systematic bits** (*e.g.*, “RV1,” “RV2,” “RV3”). Stewart, Fig. 6.

(a) Buffering by Stewart

113. In view of **Stewart’s** disclosures, a person of ordinary skill in the art would have: (1) understood that **Stewart's** interleavers are buffers, (2) been motivated to use **Stewart’s** interleavers as buffers, and (3) been motivated to modify **Stewart** to use an additional buffer to improve efficiency of its transmission process.

(i) Stewart Discloses Buffering

114. **Stewart** discloses buffering of interleaved bits through the operation of its interleavers. Buffering is a well-known process in the telecommunications space, to which **Stewart** and the ’486 are directed, and more generally in computer processing. Buffering is implemented in a buffer and both terms (*e.g.*, “buffering” and “buffer”) are well-known concepts. As one example and as discussed in Section VIII.B.1(b) (Buffers), according to the IEEE 1000 The Authoritative Dictionary of

IEEE Standard Terms, “buffer,” in the context of “supervisory control, data acquisition, and automatic control” is a “device in which data are stored temporarily, in the course of transmission from one point to another used to compensate for a difference in the flow of data, or time of occurrence of events, when transmitting data from one device to another.” Ex. 1025. In the same dictionary, in the context of “computers,” a “buffer” is defined as a “device or storage area used to store data temporarily to compensate for differences in rates of data flow, time of occurrence of events, or amounts of data that can be handled by the devices or processes involved in the transfer or use of the data.” *id.* As another example, the Microsoft Dictionary defines “buffer” as a “region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations or devices,” and “buffering” as “us[ing] a region of memory to hold data that is waiting to be transferred, especially to or from input/output (I/O) devices such as disk drives and serial ports.” Ex. 1026.

115. These two dictionaries show that buffering generally relates to the well-known process of using a region of memory to temporarily store information that is to be transmitted, consistent with the plain meaning of “buffering” and “buffer” in the ’486 patent, and as shown by **Stewart**. For example, the ’486 patent discloses a “virtual incremental redundancy (IR) buffer 615” that stores bits that are output from

a first rate matching process, prior to processing by a second rate matching process and subsequent output. '486, 6:26-51, Fig. 10. A person of ordinary skill in the art would have understood that **Stewart** discloses buffering interleaved **systematic bits** and bits of **“Parity 1” stream** and **“Parity 2” stream** in a block matrix of respective block interleavers because the interleavers temporarily store bits in the respective block matrices before they are read out of the interleavers for transmission. Stewart, 4:14-34, 4:46-48. That **Stewart** discloses to a person of ordinary skill in the art that **Stewart’s** interleavers are buffers is further supported by references that show interleavers include buffers and memories. U.S. 6,744,744, filed 4/7/2000, (“Tong”, Ex. 1038), teaches that an “interleaver...includes a working memory” such as “a FIFO (first-in, first-out) memory.” Ex. 1038, 6:17-23, 7:6-14. Similarly, U.S. 7,170,849 (“Arivoli”, Ex. 1039), filed 3/8/2002, teaches a that “typical interleaver implementation uses a memory as a buffer.” Ex. 1039, 1:53-60.

(ii) A Person of Ordinary Skill in the Art Would Have Used Stewart’s Interleavers as Buffers

116. It would have been obvious to a person of ordinary skill in the art to use the block matrixes of **Stewart’s** systematic and parity interleavers to buffer the systematic and parity interleaved bits to advantageously hold the bits until they need to be read out for transmission. As discussed above (Section IX.A.1 (Overview of Stewart)) **Stewart** is directed to an incremental redundancy system, which is a type

of HARQ process that entails retransmitting systematic and/or parity bits from a transmitting device whenever its original transmission is not successfully received by a receiving device (*see* Stewart, 1:52-2:1, 2:45-51, 3:25-30, 4:10-13). Because **Stewart** is directed to a type of HARQ process—it would have been obvious to use **Stewart’s** interleavers as buffers to support a HARQ process. *Id.* For example, **Stewart’s** interleavers would store bits associated with a transmission, and the interleavers would be accessed to carry out retransmissions as part of the HARQ process. Using buffers to support HARQ processes was known. For example, U.S. 2004/0037224A1 (“Choi”, Ex. 1040) teaches using a “HARQ retransmission buffer” to support retransmission in a HARQ process. Ex. 1040, [0034]-[0037], [0045] (“HARQ retransmission buffer”). As another example, U.S. 7,286,540 (“Kim,” Ex. 1041) teaches using “HARQ channel retransmission buffers” to support retransmission in a HARQ process. Ex. 1041, 4:1-7, 4:32-58, 11:48-57, 15:30-34. As a further example, Dahlman-667 (Ex. 1027) teaches using a retransmission buffer to support ARQ (a retransmission scheme like HARQ though simpler). Ex. 1027, [0034]. In view of the foregoing, a person of ordinary skill in the art also would have had a reasonable expectation of success in using **Stewart’s** interleavers as buffers to support a HARQ process by temporarily storing bits prior to transmission or retransmission.

(iii) A Person of Ordinary Skill in the Art Would Have Added a Transmission Buffer to Stewart

117. Alternatively, it would have been obvious to modify the teachings of **Stewart** to use an additional buffer to buffer the interleaved bits for transmission, as discussed further below in Sections IX.B (Ground 2: Stewart in View of 3GPP-Summary (Claims 1-6)), IX.C (Ground 3: Stewart in View of TS25.212 (Claims 1-6)), IX.D (Grounds 4-6: Grounds 1-3 in View of Motorola (Claims 1-6)). One example where this would be advantageous is to facilitate the concurrent loading of bits into the interleaver while transmission of bits from the transmit buffer is occurring. *See, e.g.,* Ex. 1042, 7:43-46, 13:33-39, Figs. 4, 7. This avoids an additional waiting period required while the block matrix either waits for the interleaver process to complete before the stored bits are transmitted, or waits for the transmitting of bits to complete before loading in the next set of bits for interleaving. In such a scenario, it would be advantageous to concurrently load bits into the interleaver, while concurrently transmitting bits from the transmit buffer. Such parallelization of work streams improves the efficiency of processing at the transmitting device, which improves the overall latency of **Stewart's** process for selecting bits for transmission. In light of the foregoing, a person of ordinary skill in the art also would have had a reasonable expectation of success in modifying

Stewart to include an additional buffer to de-couple the interleaver process and HARQ re-transmission process.

2. Analysis (Claims 3-4)

118. As set forth in the below analysis, Challenged Claims 3-4 are anticipated and rendered obvious by **Stewart, Motorola, 3GPP-Summary**, and/or **TS25.212**. In addition to my discussion above providing an overview of Stewart (Section IX.A.1 (Overview of Stewart)), the following discussion identifies example disclosures followed by bulleted excerpts that each disclose and/or render obvious Challenged Claims 3-4.

(a) Element [3.pre]

119. **Element [3.pre]** recites “**A method for use in an apparatus of a wireless communications comprising:**” This element is met by **Stewart**.

120. **Stewart discloses a method** (*e.g.*, “applying IR [Incremental Redundancy]” (3:1-12)) **for use in an apparatus** (*e.g.*, “user equipment (UE)” (3:1-12) or “base station [BS]” (1:44-56)) **of a wireless communications** (*e.g.*, “[3GPP] UTRA (UMTS Terrestrial Radio Access)” (3:1-12)).

121. **Stewart** discloses “applying IR [Incremental Redundancy]” in a transmitting device such as a “user equipment (UE)” or “base station” that implements cellular communications using radio access networks such as Third

Generation Partnership Project (3GPP) UMTS Terrestrial Radio Access (“UMTS”) protocol, also known as “Wideband Code Division Multiple Access” (“WCDMA”). Stewart, 1:44-56, 2:47-67, 3:1-12, 3:25-46, 9:60-10:3. A radio access network, such as 3GPP UTRA and WCDMA, is part of a wireless communications system because it implements radio access technology to send transmissions between wireless devices. Incremental Redundancy (IR) is a type of HARQ process, which entails carrying out retransmissions of systematic bits or parity bits when transmissions that are unsuccessfully received by a recipient. Stewart, 1:57-64. For example, in a scenario where a first transmission of systematic bits was unsuccessfully received, a UE would then send a combination of systematic and/or parity bits, where the numbers of bits transmitted depends on a redundancy version. For example, **Stewart’s** incremental redundancy method selects between systematic bits and two sets of parity bits for transmission based on a redundancy version. *See* Section IX.A.1(Overview of Stewart).

122. *E.g., Stewart* (emphasis added):

- **Stewart 1:44-64** (“Typically, the encoded data is transmitted to a receiver, which uses error detection. If an error is detected, *the receiver can request that the transmitter, such as a base station for example, ...*”) *retransmit the data using an Automatic Repeat Request (ARQ)*. In other words, if a receiver is not able to resolve the data bits in time, the radio can request the transmitter to resend that portion of bits from the block or a portion of a frame of data that failed so as to be properly decoded. There are several known

techniques to provide ARQ. In addition, there can be ARQ combining of different transmissions. Further, the receiver can attempt to provide error correction as well as error detection. This is referred to as a Hybrid Automatic Repeat Request (HARQ).”)

- **Stewart 2:47-67** (“The present invention provides a turbo coder that supports *incremental redundancy (IR)* as a form of ARQ combining, using a single, unified puncturing scheme. In particular, the present invention uses a puncturing scheme based on a block interleaver.”)
- **Stewart 3:1-12** (“In application, The High Speed Downlink Packet Access (HSDPA) feature of the *Third Generation Partnership Project (3GPP) UTRA (UMTS Terrestrial Radio Access) or Wideband Code Division Multiple Access (WCDMA) system details a hybrid-ARQ scheme based on Incremental Redundancy (IR) methods* applied to a rate- $\frac{1}{3}$ turbo-code. The present invention defines the High Speed Downlink Shared Channel (HS-DSCH) coding and modulation scheme to permit the use of incremental redundancy block interleaving in *user equipment (UE), such as a cellular radio communication device*. The present invention describes *a specific method and apparatus for applying IR to HSDPA*.”)
- **Stewart 3:25-46** (“The present invention provides *a flexible IR scheme specifically applicable to HSDPA*. In particular, *the IR scheme of the present invention* supports: a) a flexible method of controlling the instantaneous and variable final code rate of the HARQ process (ranging from Chase combining to rate- $\frac{1}{3}$ expansion), b) general QAM modulation, including 16-QAM, c) a specific set of possible redundancy versions from which can be selected an optimal (or simply preferred) sequence of redundancy versions, based on the specific acknowledge/negative acknowledge (ACK/NACK) signal evolution applicable to HSDPA, and d) a novel implementation of block interleavers. Prior art implementations for IR, such as those of EDGE, do not meet the specific requirements of the current problem since they cannot change the final coding rate according to the available coded symbol memory. The terminal memory requirements of the user equipment are derived based on Chase (soft) combining at the maximum data rate defined by the associated UE capability parameters. In other

words, the UE has memory limitations and can only accept particular code rates. The present invention accounts for these memory limitations and allows the UE to vary coding rates accordingly.”)

- **Stewart 9:60-10:3** (“Although the invention has been described and illustrated in the above description and drawings, it is understood that this description is by way of example only and that numerous changes and modifications can be made by those skilled in the art without departing from the broad scope of the invention. Although the present invention finds particular use in *portable cellular radiotelephones, the invention could be applied to any two-way wireless communication device, including pagers, electronic organizers, and computers*. Applicants' invention should be limited only by the following claims.”)

(b) Element [3.a]

123. **Element [3.a]** recites “**interleaving, by the apparatus, systematic bits.**” This element is met by **Stewart**.

124. **Stewart** discloses **interleaving, by the apparatus (see [3.pre]), systematic bits** (e.g., “load[s]...systematic bits...into [a] systematic...block interleaver[]” (9:39-59, Fig.11); “read[ing] into” (4:14-5:8) a “[systematic] block interleaver” (4:14-5:8, Fig. 11) a “‘Systematic’ stream” (4:14-5:8) consisting of “systematic bits” (9:39-59, Fig. 11)).

125. As I discussed in element [3.pre], **Stewart** discloses an apparatus, e.g., a UE or BS, for use in wireless communications. *See* [3.pre]. **Stewart** also discloses that the apparatus includes a “**first interleaver**” (depicted in Figs 3-4) which is “based on a block matrix interleaver” that contains a “block matrix” with N_{row}

number of rows and N_{col} number of columns; the “block matrix” is also referred to by **Stewart** as a “ $N_{row} \times N_{col}$ block matrix interleaver.” Stewart, 4:10-29, 4:46-55, Fig. 3.

126. **Stewart** further discloses that the “**first interleaver**”/“**1st interleaver**” receives a “codeword” that is separated into multiple streams including a “**‘Systematic’ stream**” (as well as N_{parity} number of parity streams, which I will discuss in detail later). Stewart, 4:14-19, 4:25-29. The “**Systematic**” stream consists of systematic “codeword bits.” Stewart, 4:14-39, 9:39-50. These “codeword bits” are “read into” or “load[ed]...into” the “ $N_{row} \times N_{col}$ block matrix interleaver” and rearranged (e.g., by permuting, or arranging by row) such that they are subsequently read out in a different order. Stewart, 4:14-39, 4:56-5:8, 9:39-50. The process of reading or loading the systematic bits into the interleaver and rearranging the bits in a different order interleaves the bits, creating interleaved bits. This process is depicted or otherwise described in Figs. 5 (*see* the “Input” arrows along each column of the block interleaver) and 11 (*see* box labelled “LOADING THE SYSTEMATIC BITS...INTO...BLOCK INTERLEAVER[] IN A COLUMN-WISE MANNER”).

127. **Stewart** teaches that the systematic bits are interleaved by the “**first interleaver**”/“**1st interleaver**” before they are selected for transmission by a

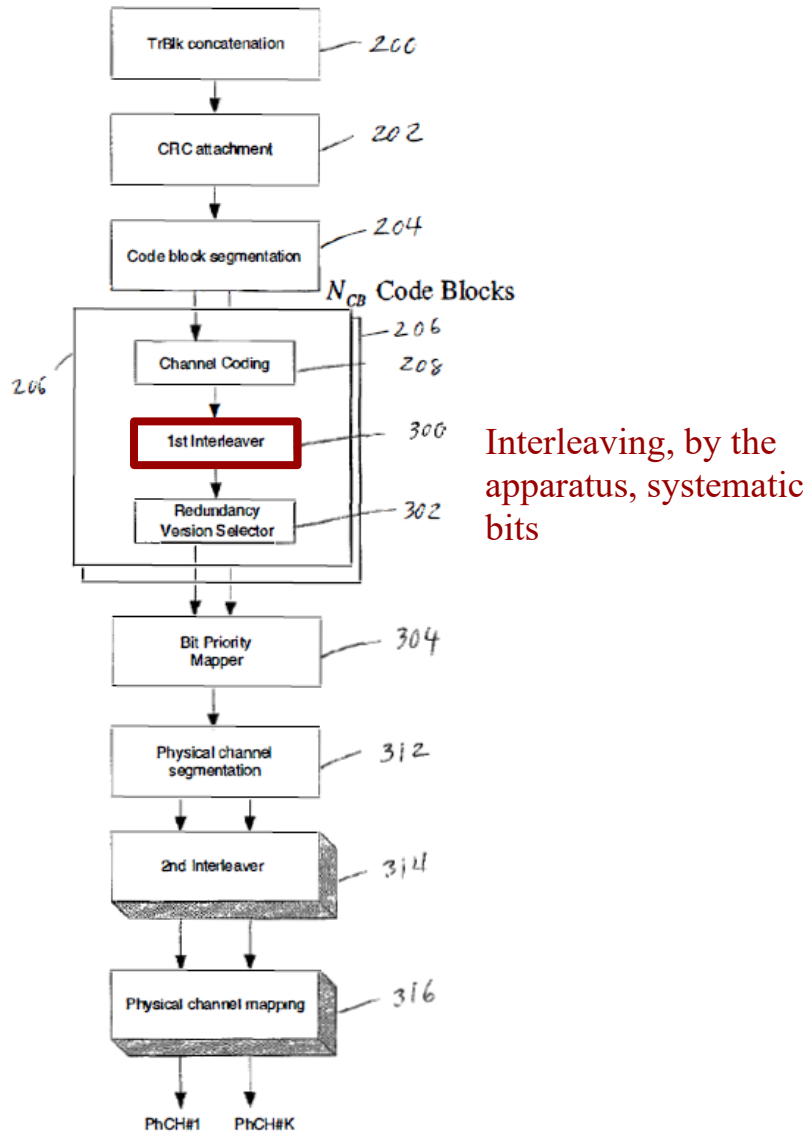
Redundancy Version Selector. Stewart, Fig. 3 (*compare* position of “**1st Interleaver**” (300) relative to the position of “Redundancy Version Selector 302”).

In other words, the input to the Redundancy Version Selection consists of *interleaved* systematic bits.

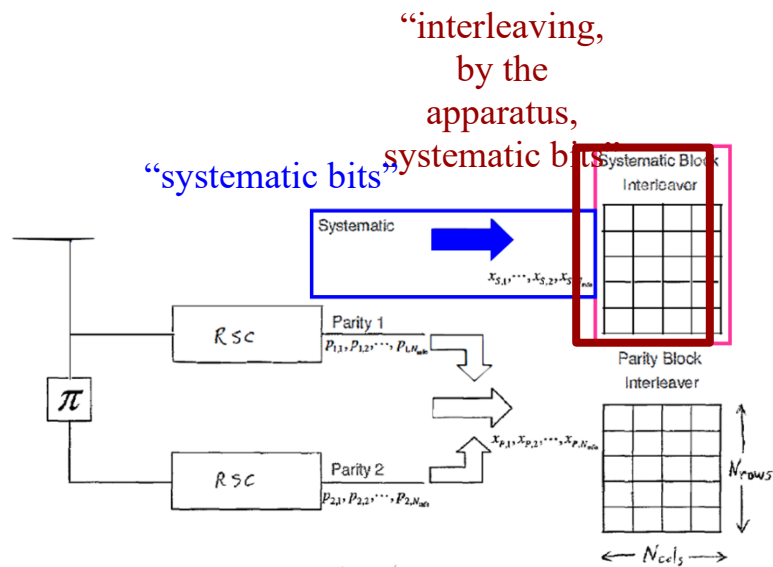
128. *E.g.*, **Stewart** (emphasis added):

- **Stewart Figure 3**

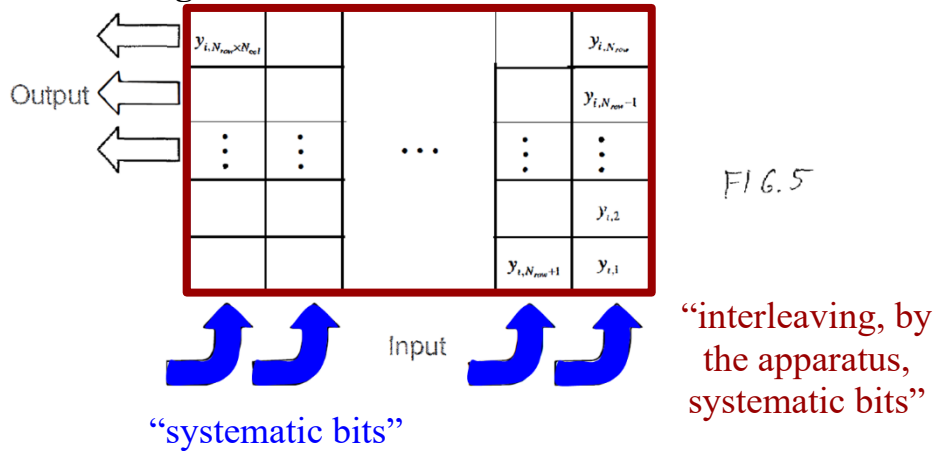
FIG. 3



- Stewart Figure 4



- Stewart Figure 5



- Stewart Figure 11

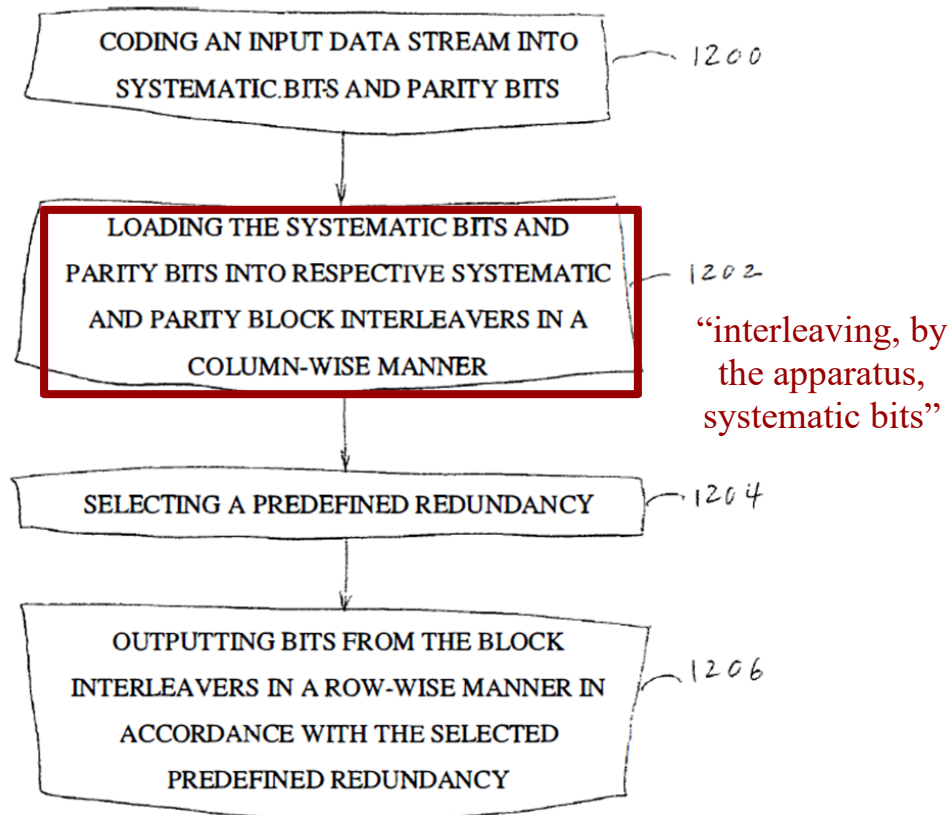


FIG. 11

- **Stewart 2:47-67** (“The present invention provides a turbo coder that supports incremental redundancy (IR) as a form of ARQ combining, using a single, unified puncturing scheme. In particular, the present invention uses a puncturing scheme based on *a block interleaver*. *Codeword bits are read in column-wise while the desired amount of unpunctured data is then read out row-wise after row and column rearrangement*. The block nature of the interleaver ensures a regular puncturing distributed throughout the encoder trellis ensuring good code performance. The block puncturing approach of the present invention has the advantage of ease of implementation as well as retaining the flexibility in adapting to any desired coding rate without a significant increase in complexity. As a result, the present invention provides for flexible and fine-grained support of predefined redundancy versions at each transmission with

progressive reduction in effective coding rates and support for full and partial forms of both Chase combining and IR. Preferably, the present invention also provides for symbol priority mapping onto the most reliable Quadrature Amplitude Modulation (QAM) constellation points to further reduce decoding errors.”)

- **Stewart 4:14-5:8** (“FIG. 4 shows the operation of the *first interleaver* (300 in FIG. 3) in entering a codeword into puncturing interleavers for the preferred turbo encoder. *In the general turbo encoder case a codeword is separated into a “Systematic” stream* and N_{Parity} parity streams denoted by $x_{S,k}$, $p_{1,k}$, $p_{2,k}$, . . . , $p_{N_{\text{Parity}},k}$ where $k \in \{1, \dots, N_{\text{info}}\}$. *Each stream is read into $N_{\text{row}} \times N_{\text{col}}$ block matrix interleavers.* Preferably, the parity bits are combined into one $N_{\text{row}} \times N_{\text{col}}$ puncturing matrix, but separate $N_{\text{row}} \times N_{\text{col}}$ parity block interleavers can be used for each parity stream. In the preferred case of a single parity interleaver $x_{S,k} \in \{1,0\}$ and $x_{P,k}$ is an N_{Parity} bit symbol $x_{P,k} = \{p_{1,k}, p_{2,k}, \dots, p_{N_{\text{Parity}},k}\}$. In the case of the preferred turbo encoder of the present invention, the unpunctured codeword bits are bit separated into respective “Systematic”, “Parity 1” and “Parity 2” streams denoted by $x_{S,k}$, $p_{1,k}$, $p_{2,k}$ where $k \in \{1, \dots, N_{\text{info}}\}$. In the preferred case of a single parity interleaver, $x_{S,k} \in \{1,0\}$ and $x_{P,k} = \{p_{1,k}, p_{2,k}\}$ where $x_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$. The tail bits from the coder are buffered separately and are later appended onto the unpunctured instantaneous codeword transmitted in a specific transmission time interval (TTI). The number of rows, N_{row} , and number of columns, N_{col} , in each interleaver can be variable and allocated dynamically. In a preferred embodiment, the number of rows, N_{row} , is always fixed at thirty, while the number of columns, N_{col} , is variable (dependent on the number of information bits N_{info}) and is determined in the same manner as the turbo code internal interleavers, such as is described in section 4.2.3.2.3.1 of ‘Technical Specification Group Radio Access Network; Multiplexing and Channel Coding (FDD) (Release 1999)’, TS 25.212 v3.5.0 (2000-12), which is hereby incorporated by reference.

FIG. 5 shows the data stream of the interleavers of FIG. 4. A novel aspect of the present invention is having data read in a column-wise fashion into each interleaver. The data includes dummy bits padded if $N_{\text{info}} < N_{\text{row}} \times N_{\text{col}}$, where $y_k = x_k$ for $k = 1, 2, \dots, N_{\text{info}}$ and $y_{S,k} \in \{0,1\}$

and $y_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$ for $k = \{N_{info}+1, \dots, N_{row} \times N_{col}\}$. These dummy bits are later removed when reading the codeword data row-wise from top-to-bottom from the **block matrix**, similar to the description in section 4.2.3.2.3.2 of TS 25.212, incorporated by reference.

To facilitate flexibility in supporting variable coding rates in the present invention, both columns and rows are permuted prior to reading out the block matrix contents. As an example of the benefit of row and column reordering, consider the case where $N_{row}=30$ and $N_{col}=100$. If the first two rows were to be read out without reordering, the codeword bits would correspond to the 29th, 30th, 59th, 60th, 89th, 90th, $\dots$ stages in the encoder trellis. However, by reordering row 29 with row 15, then the transmitted codeword bits become those at the 15th, 30th, 45th, 60th, 75th, 90th, $\dots$ stages in the encoder trellis, a more homogenous and therefore desirable distribution. In permuting the columns, it is ensured that no sub-block section of the trellis is neglected when only a portion of a row is read out to form the transmitted codeword. The row permutation is that defined by Table 7 in section 4.2.1.1 of TS 25.212, hereby incorporated by reference.

After the row and column permutation, the desired number of codeword bits can then be read out in row-wise fashion.”)

- **Stewart 4:46-55** (“**FIG. 5 shows the data stream of the interleavers of FIG. 4.** A novel aspect of the present invention is having data read in a column-wise fashion into each interleaver. The data includes dummy bits padded if $N_{info} < N_{row} \times N_{col}$, where $y_k = x_k$ for $k=1, 2, \dots, N_{info}$ and $y_{S,k} \in \{0,1\}$ and $y_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$ for $k = \{N_{info}+1, \dots, N_{row} \times N_{col}\}$. These dummy bits are later removed when reading the codeword data row-wise from top-to-bottom from the **block matrix**, similar to the description in section 4.2.3.2.3.2 of TS 25.212, incorporated by reference.”)
- **Stewart 9:39-56** (“FIG. 11 shows a flow chart representing a method ... for turbo code based incremental redundancy[]. A first step of the method is coding 1200, such as turbo coding, **an input data stream into systematic bits** and parity bits. A next step is **loading 1202 loading [sic] the systematic bits and parity bits into**

respective systematic and parity *block interleavers* in a column-wise manner, as described previously. A next step is selecting 1204 a predetermined redundancy. This step follows the redundancy rules previously described, and preferably utilizes the specific redundancy version outlined above. A next step is outputting 1206 data from the block interleavers in a row-wise manner in accordance with the selected redundancy. Preferably, a outputting step includes mapping the bits from the systematic and parity block into a symbol mapping array wherein the systematic bits are mapped into the upper rows of the array and the parity bits are mapped into the lower rows of the array.”)

(c) Element [3.b]

129. **Element [3.b]** recites “**interleaving, by the apparatus, a first parity bit stream.**” This element is met by **Stewart**.

130. **Stewart** discloses **interleaving by the apparatus (see [3.pre]), a first parity bit stream** (e.g., “loading...parity bits into [a] respective...parity block interleaver[]” (9:39-59, Fig. 11); “read[ing] into” (4:14-5:8) a “parity block interleaver[]” (4:14-5:8, Fig. 11) a “parity stream[] denoted by ... $p_{l,k}$ ” (4:14-5:8)).

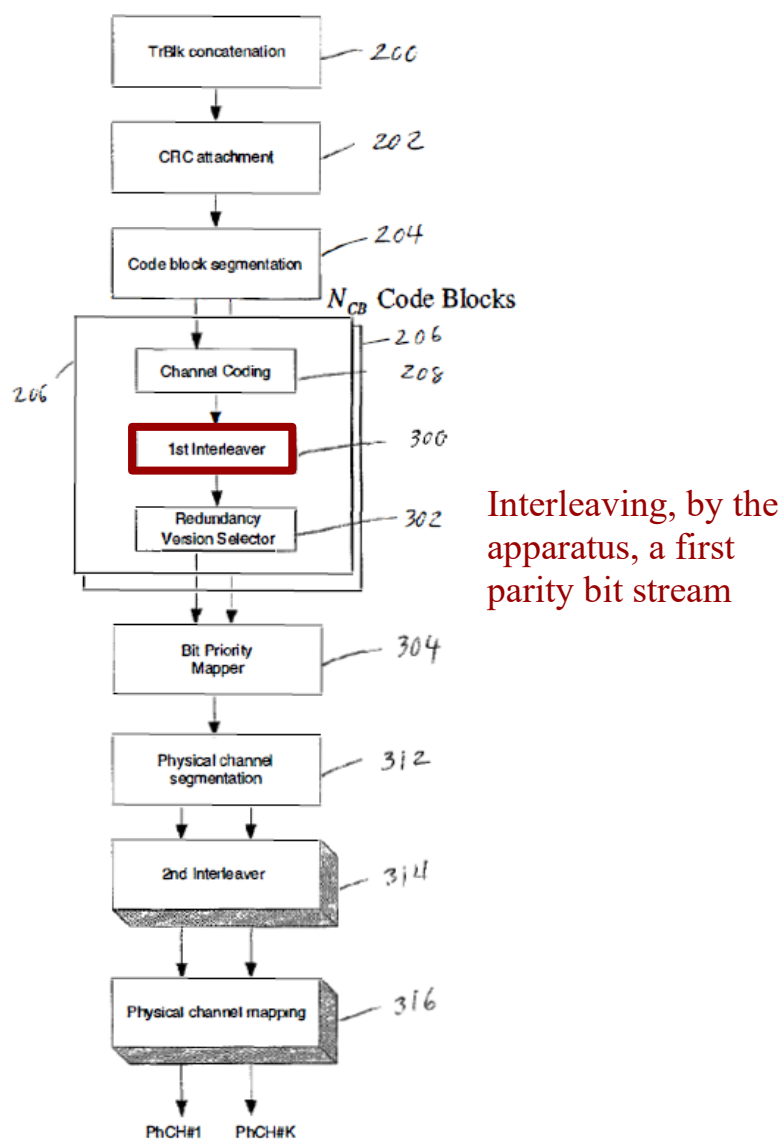
131. As I discussed in element [3.pre], **Stewart** discloses an apparatus, e.g., a UE or BS, for use in wireless communications. See [3.pre]. **Stewart** further discloses that the apparatus includes a “**parity block interleaver[]**” (Fig. 4). As I mentioned in connection with [3.a], the apparatus receives N_{parity} number of parity streams, which includes a “**Parity 1**” stream. See [3.a]. **Stewart** teaches that each parity stream has a “separate $N_{row} \times N_{col}$ parity block interleaver.” Stewart, 4:14-19.

A “**parity block interleaver**” dedicated to the “**Parity 1**” stream receives a codeword that includes the “**Parity 1**” stream, denoted $p_{1,k}$, which consists of parity codeword bits. Stewart, 4:14-19, 4:25-29. These codeword bits are “read into” or “load[ed]...into” the “ $N_{row} \times N_{col}$ **parity block matrix interleaver**” (e.g., column by column), and rearranged (e.g., by permuting) such that they are subsequently be read out in a different order. Stewart, 4:14-29, 9:39-50, Figs. 4, 5, 11. The process of reading or loading the first parity bits into the interleaver and rearranging the bits in a different order interleaves the bits, creating interleaved bits. This process is depicted or otherwise described in Figs. 5 (see the “Input” arrows along each column of the block interleaver) and 11 (see box labelled “LOADING THE...PARITY BITS...INTO RESPECTIVE...BLOCK INTERLEAVER[] IN A COLUMN-WISE MANNER”).

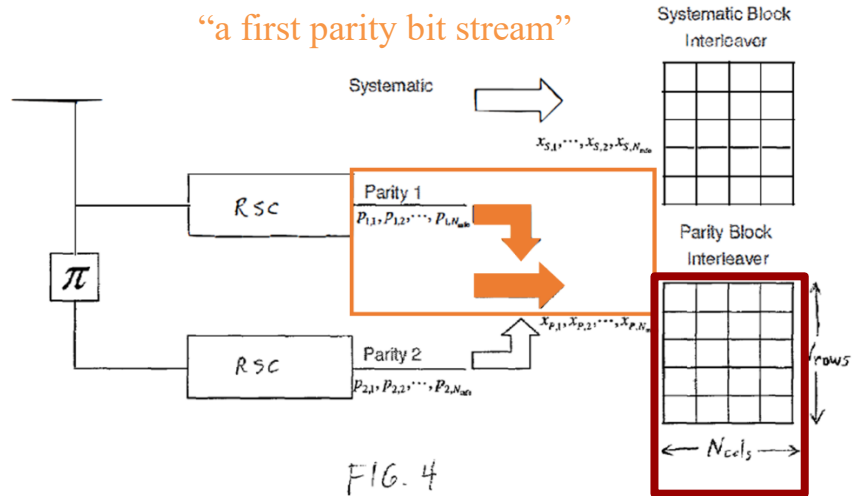
132. E.g., Stewart (emphasis added):

- Stewart Figure 3

FIG. 3



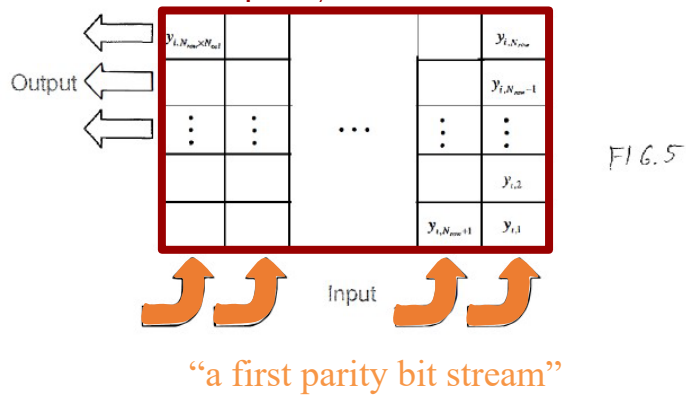
- Stewart Figure 4



“interleaving, by the apparatus, a first parity bit stream”

- Stewart Figure 5

“interleaving, by the apparatus, a first parity bit stream”



- Stewart Figure 11

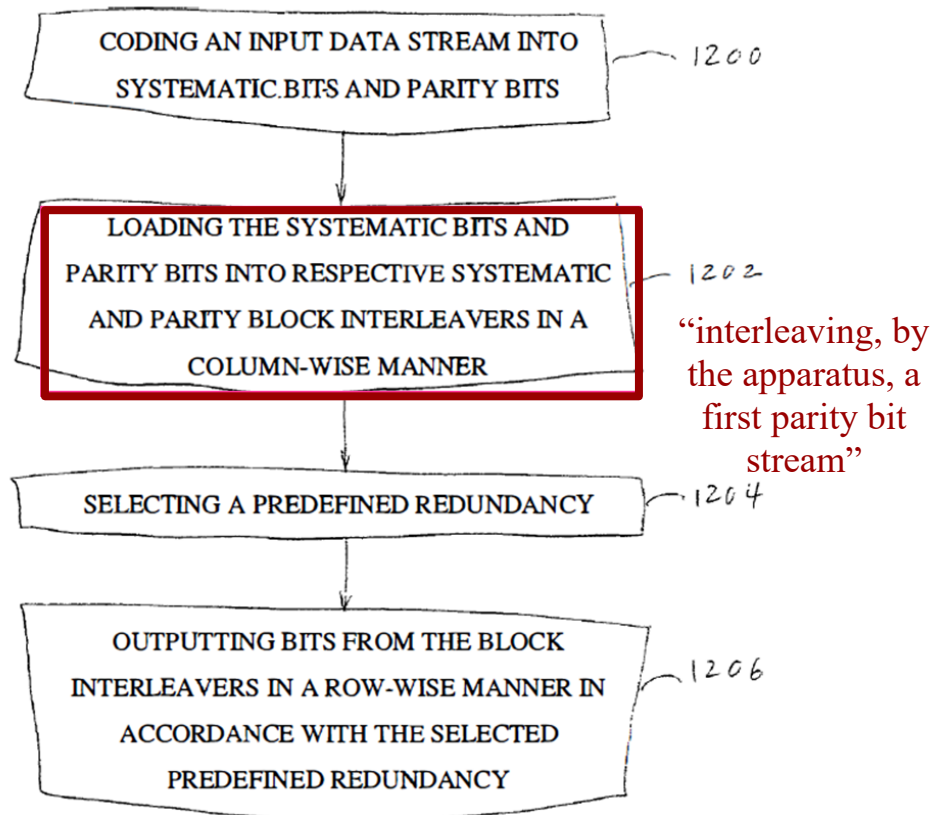


FIG. 11

- Stewart 2:47-67** (“The present invention provides a turbo coder that supports incremental redundancy (IR) as a form of ARQ combining, using a single, unified puncturing scheme. In particular, the present invention uses a puncturing scheme based on a *block interleaver*. *Codeword bits are read in column-wise while the desired amount of unpunctured data is then read out row-wise after row and column rearrangement.* The *block nature of the interleaver* ensures a regular puncturing distributed throughout the encoder trellis ensuring good code performance. The block puncturing approach of the present invention has the advantage of ease of implementation as well as retaining the flexibility in adapting to any desired coding rate without a significant increase in complexity. As a result, the present invention provides for flexible and fine-grained support of predefined redundancy versions at each transmission with progressive reduction in effective coding rates and support for full

and partial forms of both Chase combining and IR. Preferably, the present invention also provides for symbol priority mapping onto the most reliable Quadrature Amplitude Modulation (QAM) constellation points to further reduce decoding errors.”)

- **Stewart 4:14-5:8** (“FIG. 4 shows the operation of the *first interleaver* (300 in FIG. 3) in entering a codeword into puncturing interleavers for the preferred turbo encoder. *In the general turbo encoder case a codeword is separated into* a “Systematic” stream and N_{Parity} *parity streams denoted by* $x_{S,k}, p_{1,k}, p_{2,k}, \dots, p_{N_{parity},k}$ *where* $k \in \{1, \dots, N_{info}\}$. *Each stream is read into* $N_{row} \times N_{col}$ *block matrix interleavers.* Preferably, the parity bits are combined into one $N_{row} \times N_{col}$ puncturing matrix, but *separate* $N_{row} \times N_{col}$ *parity block interleavers can be used for each parity stream.* In the preferred case of a single parity interleaver $x_{S,k} \in \{1,0\}$ and $x_{P,k}$ is an N_{Parity} bit symbol $x_{P,k} = \{p_{1,k}, p_{2,k}, \dots, p_{N_{parity},k}\}$. In the case of the preferred turbo encoder of the present invention, *the unpunctured codeword bits are bit separated into respective* “Systematic”, “Parity 1” and “Parity 2” *streams denoted by* $x_{S,k}, p_{1,k}, p_{2,k}$ *where* $k \in \{1, \dots, N_{info}\}$. In the preferred case of a single parity interleaver, $x_{S,k} \in \{1,0\}$ and $x_{P,k} = \{p_{1,k}, p_{2,k}\}$ where $x_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$. The tail bits from the coder are buffered separately and are later appended onto the unpunctured instantaneous codeword transmitted in a specific transmission time interval (TTI). The number of rows, N_{row} , and number of columns, N_{col} , in each interleaver can be variable and allocated dynamically. In a preferred embodiment, the number of rows, N_{row} , is always fixed at thirty, while the number of columns, N_{col} , is variable (dependent on the number of information bits N_{info}) and is determined in the same manner as the turbo code internal interleavers, such as is described in section 4.2.3.2.3.1 of “Technical Specification Group Radio Access Network; Multiplexing and Channel Coding (FDD) (Release 1999)”, TS 25.212 v3.5.0 (2000-12), which is hereby incorporated by reference.

FIG. 5 shows the data stream of the interleavers of FIG. 4. A novel aspect of the present invention is having data read in a column-wise fashion into each interleaver. The data includes dummy bits padded if $N_{info} < N_{row} \times N_{col}$, where $y_k = x_k$ for $k = 1, 2, \dots, N_{info}$ and $y_{S,k} \in \{0,1\}$

and $y_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$ for $k = \{N_{info}+1, \dots, N_{row} \times N_{col}\}$. These dummy bits are later removed when reading the codeword data row-wise from top-to-bottom from the **block matrix**, similar to the description in section 4.2.3.2.3.2 of TS 25.212, incorporated by reference.

To facilitate flexibility in supporting variable coding rates in the present invention, both columns and rows are permuted prior to reading out the block matrix contents. As an example of the benefit of row and column reordering, consider the case where $N_{row}=30$ and $N_{col}=100$. If the first two rows were to be read out without reordering, the codeword bits would correspond to the 29th, 30th, 59th, 60th, 89th, 90th, $\dots$ stages in the encoder trellis. However, by reordering row 29 with row 15, then the transmitted codeword bits become those at the 15th, 30th, 45th, 60th, 75th, 90th, $\dots$ stages in the encoder trellis, a more homogenous and therefore desirable distribution. In permuting the columns, it is ensured that no sub-block section of the trellis is neglected when only a portion of a row is read out to form the transmitted codeword. The row permutation is that defined by Table 7 in section 4.2.1.1 of TS 25.212, hereby incorporated by reference.

After the row and column permutation, the desired number of codeword bits can then be read out in row-wise fashion.”)

- **Stewart 4:46-55** (“**FIG. 5 shows the data stream of the interleavers of FIG. 4.** A novel aspect of the present invention is having data read in a column-wise fashion into each interleaver. The data includes dummy bits padded if $N_{info} < N_{row} \times N_{col}$, where $y_k = x_k$ for $k=1, 2, \dots, N_{info}$ and $y_{S,k} \in \{0,1\}$ and $y_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$ for $k = \{N_{info}+1, \dots, N_{row} \times N_{col}\}$. These dummy bits are later removed when reading the codeword data row-wise from top-to-bottom from the **block matrix**, similar to the description in section 4.2.3.2.3.2 of TS 25.212, incorporated by reference.”)
- **Stewart 9:39-56** (“FIG. 11 shows a flow chart representing a method ... for turbo code based incremental redundancy[]. A first step of the method is coding 1200, such as turbo coding, **an input data stream** into systematic bits and **parity bits**. A next step is

loading 1202 loading [sic] the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner, as described previously. A next step is selecting 1204 a predetermined redundancy. This step follows the redundancy rules previously described, and preferably utilizes the specific redundancy version outlined above. A next step is outputting 1206 data from the block interleavers in a row-wise manner in accordance with the selected redundancy. Preferably, a outputting step includes mapping the bits from the systematic and parity block into a symbol mapping array wherein the systematic bits are mapped into the upper rows of the array and the parity bits are mapped into the lower rows of the array.”)

(d) Element [3.c]

133. **Element [3.c]** recites “interleaving, by the apparatus, a second parity bit stream.” This element is met by **Stewart**.

134. **Stewart** discloses interleaving by the apparatus (*see* [3.pre]), a second parity bit stream (*e.g.*, “loading...parity bits into [a] respective...parity block interleaver[]” (9:39-59, Fig. 11) or “read[ing] into” (4:14-5:8) a “parity block interleaver[]” (4:14-5:8, Fig. 11) a “parity stream[] denoted by ... $p_{2,k}$ ” (4:14-5:8)).

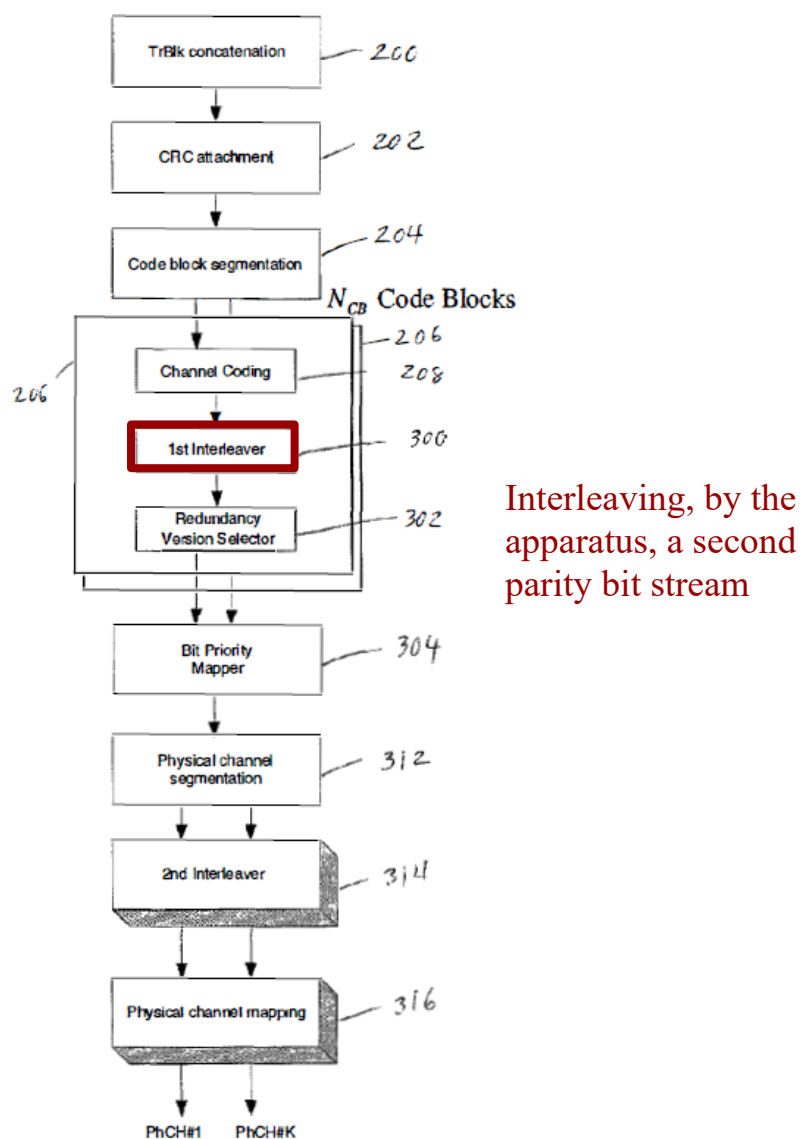
135. As I discuss in element [3.pre], **Stewart** discloses an apparatus, *e.g.* a UE or BS, for use in wireless communications. *See* [3.pre]. **Stewart** further discloses that the apparatus includes a “**parity block interleaver[]**” (Fig. 4). As I mentioned in connection with [3.a], the apparatus receives N_{parity} number of parity streams, which includes a “**Parity 2**” stream. *See* [3.a]. As I mentioned in connection with [3.b], **Stewart** teaches that each parity stream has a “separate

$N_{row} \times N_{col}$ parity block interleaver.” Stewart, 4:14-19; *see also* [3.b]. A “**parity block interleaver[]**” dedicated to the “Parity 2” stream receives a codeword that includes **the “Parity 2” stream**, denoted $p_{2,k}$, which consists of parity codeword bits. Stewart, 4:14-19, 4:25-29. These codeword bits are “read into” or “load[ed]...into” the “ $N_{row} \times N_{col}$ parity block matrix interleaver,” column by column, and rearranged (e.g., by permuting) such that they can subsequently be read out in a different order. Stewart, 4:14-29, 9:39-50, Figs. 4, 5, 11. The process of reading or loading the second parity bits into the interleaver and rearranging the bits in a different order interleaves the bits, creating interleaved bits. This process is depicted or otherwise described in Figs. 5 (*see* the “Input” arrows along each column of the block interleaver) and 11 (*see* box labelled “LOADING THE...PARITY BITS...INTO RESPECTIVE...BLOCK INTERLEAVER[] IN A COLUMN-WISE MANNER”).

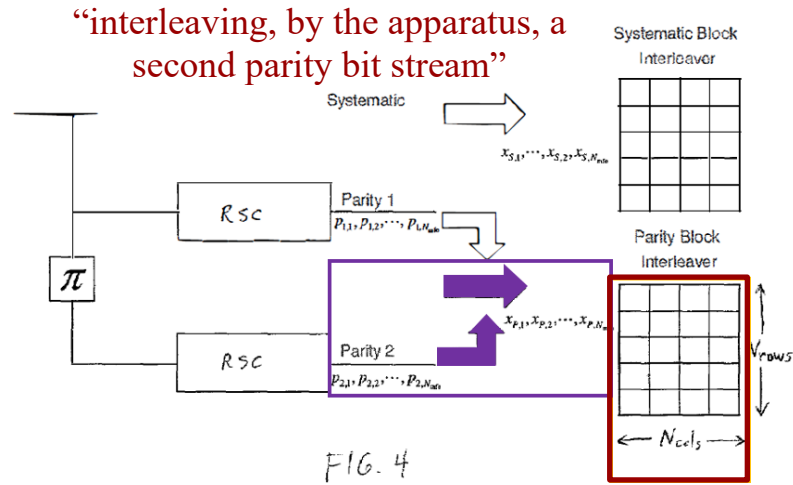
136. *E.g.*, Stewart (emphasis added):

- Stewart Figure 3

FIG. 3

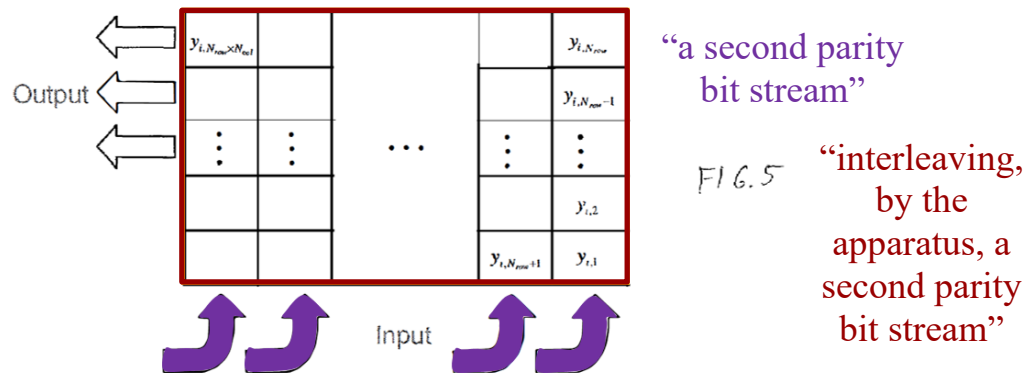


- Stewart Figure 4



“a second parity bit stream”

- Stewart Figure 5



- Stewart Figure 11

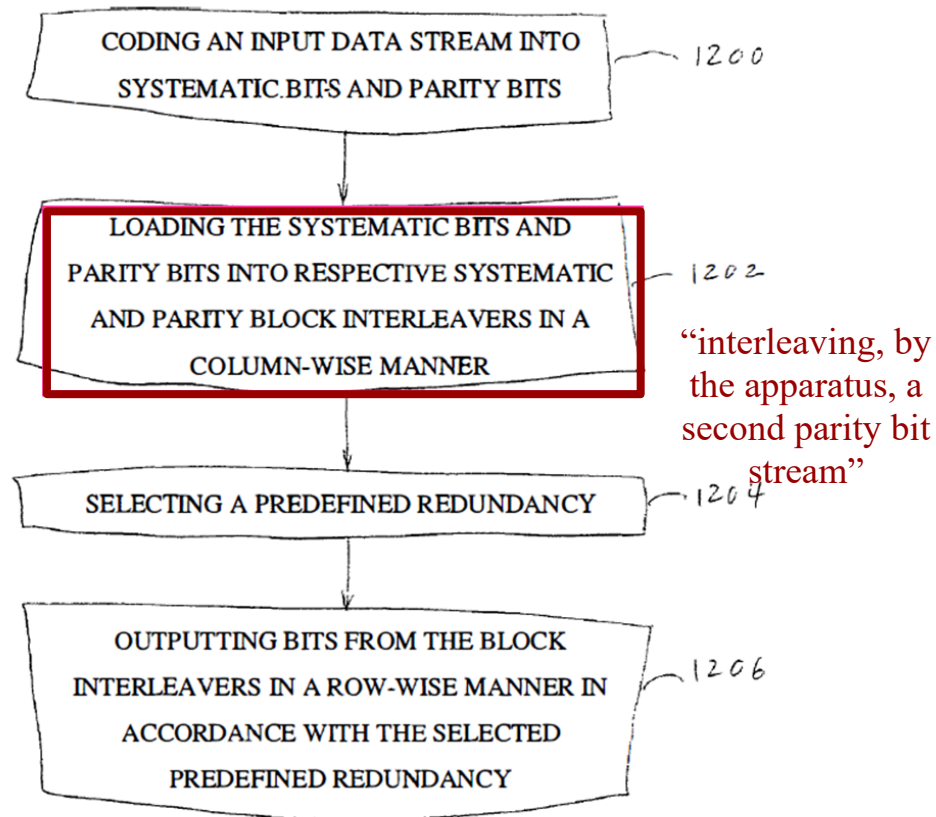


FIG. 11

- Stewart 2:47-56 (“The present invention provides a turbo coder that supports *incremental redundancy (IR)* as a form of ARQ combining, using a single, unified *puncturing scheme*. In particular, *the present invention uses a puncturing scheme based on a block interleaver*. Codeword bits are read in column-wise while the desired amount of unpunctured data is then read out row-wise after row and column rearrangement. The *block nature of the interleaver* ensures a regular puncturing distributed throughout the encoder trellis ensuring good code performance.”)
- Stewart 4:14-5:8 (“FIG. 4 shows the operation of the *first interleaver* (300 in FIG. 3) in entering a codeword into puncturing interleavers for the preferred turbo encoder. *In the general turbo encoder case a codeword is separated* into a “Systematic” stream

and N_{Parity} **parity streams denoted by** $x_{S,k}$, $p_{1,k}$, $p_{2,k}$, $\dots$, $p_{N_{Parity},k}$ **where** $k \in \{1, \dots, N_{info}\}$. **Each stream is read into $N_{row} \times N_{col}$ block matrix interleavers.** Preferably, the parity bits are combined into one $N_{row} \times N_{col}$ puncturing matrix, but **separate $N_{row} \times N_{col}$ parity block interleavers can be used for each parity stream.** In the preferred case of a single parity interleaver $x_{S,k} \in \{1,0\}$ and $x_{P,k}$ is an N_{Parity} bit symbol $x_{P,k} = \{p_{1,k}, p_{2,k}, \dots, p_{N_{Parity},k}\}$. In the case of the preferred turbo encoder of the present invention, **the unpunctured codeword bits are bit separated into respective** “Systematic”, “Parity 1” and **“Parity 2” streams denoted by** $x_{S,k}$, $p_{1,k}$, $p_{2,k}$ **where** $k \in \{1, \dots, N_{info}\}$. In the preferred case of a single parity interleaver, $x_{S,k} \in \{1,0\}$ and $x_{P,k} = \{p_{1,k}, p_{2,k}\}$ where $x_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$. The tail bits from the coder are buffered separately and are later appended onto the unpunctured instantaneous codeword transmitted in a specific transmission time interval (TTI). The number of rows, N_{row} , and number of columns, N_{col} , in each interleaver can be variable and allocated dynamically. In a preferred embodiment, the number of rows, N_{row} , is always fixed at thirty, while the number of columns, N_{col} , is variable (dependent on the number of information bits N_{info}) and is determined in the same manner as the turbo code internal interleavers, such as is described in section 4.2.3.2.3.1 of “Technical Specification Group Radio Access Network; Multiplexing and Channel Coding (FDD) (Release 1999)”, TS 25.212 v3.5.0 (2000-12), which is hereby incorporated by reference.

FIG. 5 shows the data stream of the interleavers of FIG. 4. A novel aspect of the present invention is having data read in a column-wise fashion into each interleaver. The data includes dummy bits padded if $N_{info} < N_{row} \times N_{col}$, where $y_k = x_k$ for $k = 1, 2, \dots, N_{info}$ and $y_{S,k} \in \{0,1\}$ and $y_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$ for $k = \{N_{info}+1, \dots, N_{row} \times N_{col}\}$. These dummy bits are later removed when reading the codeword data row-wise from top-to-bottom from the **block matrix**, similar to the description in section 4.2.3.2.3.2 of TS 25.212, incorporated by reference.

To facilitate flexibility in supporting variable coding rates in the present invention, both columns and rows are permuted prior to

reading out the block matrix contents. As an example of the benefit of row and column reordering, consider the case where $N_{row}=30$ and $N_{col}=100$. If the first two rows were to be read out without reordering, the codeword bits would correspond to the 29th, 30th, 59th, 60th, 89th, 90th, . . . stages in the encoder trellis. However, by reordering row 29 with row 15, then the transmitted codeword bits become those at the 15th, 30th, 45th, 60th, 75th, 90th, . . . stages in the encoder trellis, a more homogenous and therefore desirable distribution. In permuting the columns, it is ensured that no sub-block section of the trellis is neglected when only a portion of a row is read out to form the transmitted codeword. The row permutation is that defined by Table 7 in section 4.2.1.1 of TS 25.212, hereby incorporated by reference.

After the row and column permutation, the desired number of codeword bits can then be read out in row-wise fashion.”)

- **Stewart 4:46-55** (“**FIG. 5 shows the data stream of the interleavers of FIG. 4.** A novel aspect of the present invention is having data read in a column-wise fashion into each interleaver. The data includes dummy bits padded if $N_{info} < N_{row} \times N_{col}$, where $y_k = x_k$ for $k=1, 2, \dots, N_{info}$ and $y_{S,k} \in \{0,1\}$ and $y_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$ for $k=\{N_{info}+1, \dots, N_{row} \times N_{col}\}$. These dummy bits are later removed when reading the codeword data row-wise from top-to-bottom from the **block matrix**, similar to the description in section 4.2.3.2.3.2 of TS 25.212, incorporated by reference.”)
- **Stewart 9:39-56** (“FIG. 11 shows a flow chart representing a method . . . for turbo code based incremental redundancy[]. A first step of the method is coding 1200, such as turbo coding, an input data stream into systematic bits and parity bits. A next step is **loading 1202 loading the systematic bits and parity bits into respective systematic and parity block interleavers** in a column-wise manner, as described previously. A next step is selecting 1204 a predetermined redundancy. This step follows the redundancy rules previously described, and preferably utilizes the specific redundancy version outlined above. A next step is outputting 1206 data from the block interleavers in a row-wise manner in accordance with the selected redundancy. Preferably, a outputting step includes mapping the bits from the systematic and parity block into a symbol

mapping array wherein the systematic bits are mapped into the upper rows of the array and the parity bits are mapped into the lower rows of the array.”)

(e) Element [3.d]

137. **Element [3.d]** recites “**buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream.**” This element is met by **Stewart**.

138. **Stewart** discloses **buffering, by the apparatus** (*see* [3.pre]), **the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream** (*e.g.*, storing “systematic bits” (9:39-59, Fig. 11) in a “systematic ... block interleaver” (9:39-59, Fig. 11) for subsequent read out, storing “parity bits” (4:14-34, Fig. 11) from “parity stream[] denoted by ... $p_{l,k}$ ” (4:14-34) in a “parity block interleaver[]” (4:14-34, Fig. 11) for subsequent read out; and storing “parity bits” (4:14-34, Fig. 11) from “parity stream[] denoted by ... $p_{2,k}$ ” (4:14-34) in a separate “parity block interleaver[]” (4:14-34) for subsequent read out).

139. As I discuss in element [3.pre], **Stewart** discloses an apparatus, a UE, for use in wireless communications. *See* [3.pre]. **Stewart** also discloses that codeword bits are “read into” or “load[ed]...into” block interleavers. **Stewart**, 4:14-29, Fig. 11. Specifically, **Stewart** discloses an apparatus receiving a

“**Systematic’...stream[]**” and N_{parity} number of parity streams, which includes **“Parity 1” stream** and **“Parity 2” stream**” denoted by $\dots p_{1,k}$ ” and “denoted by $\dots p_{2,k}$,” respectively, each having a “separate” block interleaver. *Id;* see also [3.a]-[3.c]. Each of the streams are “read into” and stored in their respective block interleavers (e.g., as shown in Fig. 4) for reading out in a different interleaved order. *Id;* see also Fig. 11 (box labeled “LOADING THE SYSTEMATIC BITS AND PARITY BITS INTO RESPECTIVE SYSTEMATIC AND PARITY BLOCK INTERLEAVERS IN A COLUMN-WISE MANNER”).

140. For the reasons I discussed in Section IX.A.1(a) (Buffering by Stewart), **Stewart** discloses that interleavers buffer interleaved bits, and at minimum renders obvious using interleavers to buffer interleaved bits. Because buffering is a well-known process of temporarily storing information for transmission, a person of ordinary skill in the art would have understood that **Stewart’s** interleavers, by storing interleaved bits, are buffering the interleaved bits. Moreover, as discussed above in Section IX.A.1(a) (Buffering by Stewart), multiple references show that interleavers, such as those disclosed by **Stewart**, include memories that store information and therefore act as a buffer, by using a region of memory to temporarily store information that is to be transmitted. In **Stewart**, bits are loaded into an interleaver along one dimension (e.g., column-by-column), and then rearranged by

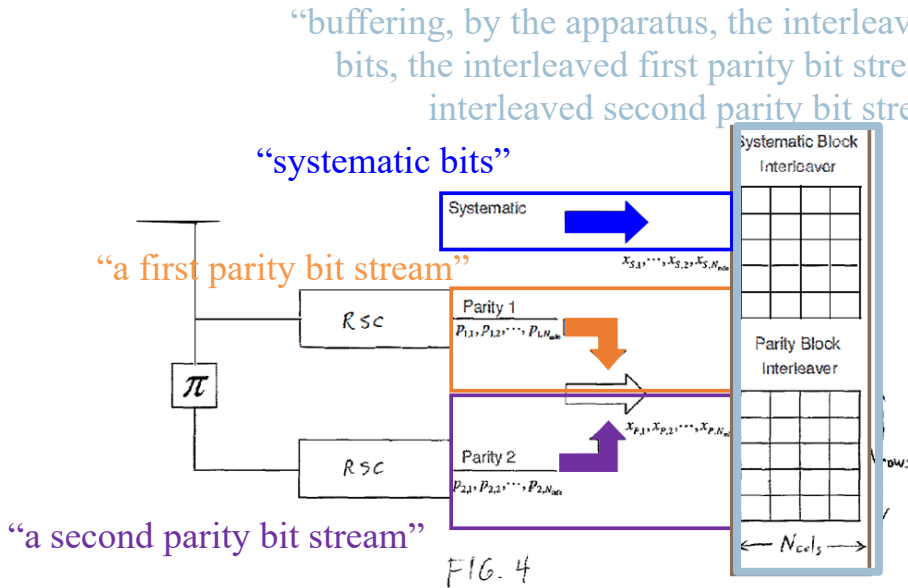
permuting within the interleaver to reorder the bits for output. Stewart, Fig. 5, 2:47-7, 4:46-5:8. As I discussed above in Sections V.A ('486 Patent Overview), VIII.B.1(a) (Interleavers), bits are re-arranged in an interleaving process to avoid continuous sequences in the interleaved arrangement that would be susceptible to burst errors. When the bits are re-arranged, whether by permuting, or by arranging for read-out from a different dimension of the interleaver (*e.g.*, accessed for output in a row-wise fashion when input in a column-wise fashion) and vice versa, the bits are interleaved as stored within the interleaver. Thus, when the bits are stored within the block matrix, after being read in, the bits are interleaved and **buffered** by the block matrix, prior to being read out.

141. Moreover, as I discussed above in Section IX.A.1(a) (Buffering by Stewart), it would have been obvious to use **Stewart's** block interleavers as buffers such that the codewords read into the interleavers are interleaved (*see* [1.a]-[1.c]) and the interleaved bits are temporarily stored in their respective block interleavers before they are selected to be read-out for transmission. Stewart, 6:41-52. A person of ordinary skill in the art would have been motivated to use interleavers as buffers to support retransmission processes, such as HARQ processes that I explained in Section IV (Background of the Technology). For example, **Stewart** discloses a HARQ process that uses Incremental Redundancy (IR) (Stewart, 3:25-30), which I

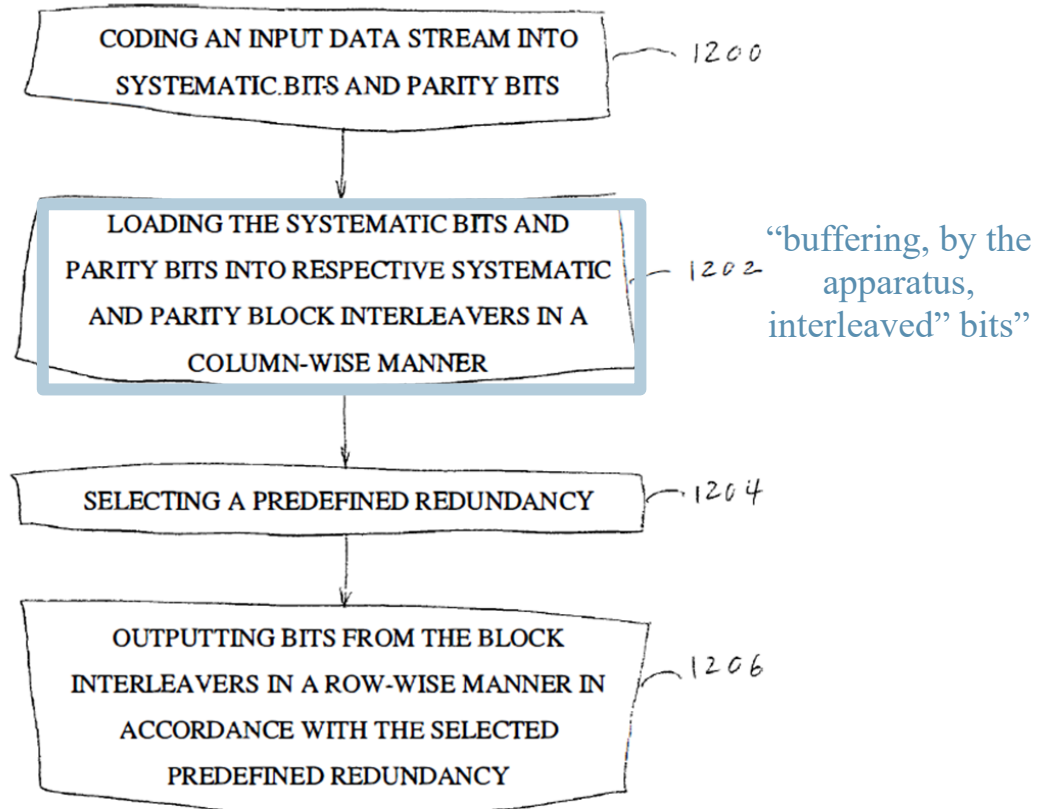
described in more detail in connection with [3.pre]. *See* [3.pre]. To reiterate here, IR entails carrying out retransmissions of systematic bits and/or parity bits when a transmission was unsuccessfully received by a receiving device. The bits associated with an initial transmission, including bits that were not initially transmitted are buffered to facilitate retrieval in the event a transmitting device is requested to carry out a retransmission of all or a portion of those bits associated with the initial transmission. Accordingly, HARQ processes require the use of buffers to store bits to facilitate retransmissions. It would have been obvious to use **Stewart's** interleavers not only to interleave systematic, first parity, and second parity bits, but also to buffer the interleaved systematic bits, first parity bits, and second parity bits to facilitate carrying out retransmissions as part of **Stewart's** HARQ scheme, because each of the interleavers respectively stores systematic bits, first parity bits, or second parity bits.

142. *E.g.*, **Stewart** (emphasis added):

- **Stewart Figure 4**



- Stewart Figure 11



- **Stewart 2:47-67** (“The present invention provides a turbo coder that supports incremental redundancy (IR) as a form of ARQ combining, using a single, unified puncturing scheme. In particular, the present invention uses a puncturing scheme based on *a block interleaver*. *Codeword bits are read in* column-wise while the desired amount of unpunctured data is then read out row-wise after row and column rearrangement. The *block nature of the interleaver* ensures a regular puncturing distributed throughout the encoder trellis ensuring good code performance. The block puncturing approach of the present invention has the advantage of ease of implementation as well as retaining the flexibility in adapting to any desired coding rate without a significant increase in complexity. As a result, the present invention provides for flexible and fine-grained support of predefined redundancy versions at each transmission with progressive reduction in effective coding rates and support for full and partial forms of both Chase combining and IR. Preferably, the present invention also provides for symbol priority mapping onto the most reliable Quadrature Amplitude Modulation (QAM) constellation points to further reduce decoding errors.”)
- **Stewart 3:25-46** (“The present invention provides *a flexible IR scheme specifically applicable to HSDPA*. In particular, *the IR scheme of the present invention* supports: a) a flexible method of controlling the instantaneous and variable final code rate of the HARQ process (ranging from Chase combining to rate- $\frac{1}{3}$ expansion), b) general QAM modulation, including 16-QAM, c) a specific set of possible *redundancy versions* from which can be selected an optimal (or simply preferred) sequence of redundancy versions, based on the specific acknowledge/negative acknowledge (ACK/NACK) signal evolution applicable to HSDPA, and d) a novel implementation of block interleavers. Prior art implementations for IR, such as those of EDGE, do not meet the specific requirements of the current problem since they cannot change the final coding rate according to the available coded symbol memory. The terminal memory requirements of the user equipment are derived based on Chase (soft) combining at the maximum data rate defined by the associated UE capability parameters. In other words, the UE has memory limitations and can only accept particular code rates. The present invention accounts for these

memory limitations and allows the UE to vary coding rates accordingly.”)

- **Stewart 4:14-34** (“FIG. 4 shows the operation of *the first interleaver (300 in FIG. 3) in entering a codeword into puncturing interleavers for the preferred turbo encoder*. In the general turbo encoder case a codeword is separated into a “Systematic” stream and N_{Parity} parity streams denoted by $x_{S,k}$, $p_{1,k}$, $p_{2,k}$, . . . , $p_{N_{\text{Parity}},k}$ where $k \in \{1, \dots, N_{\text{info}}\}$. *Each stream is read into $N_{\text{row}} \times N_{\text{col}}$ block matrix interleavers*. Preferably, the parity bits are combined into one $N_{\text{row}} \times N_{\text{col}}$ puncturing matrix, but *separate $N_{\text{row}} \times N_{\text{col}}$ parity block interleavers can be used for each parity stream*. In the preferred case of a single parity interleaver $x_{S,k} \in \{1,0\}$ and $x_{P,k}$ is an N_{Parity} bit symbol $x_{P,k} = \{p_{1,k}, p_{2,k}, \dots, p_{N_{\text{Parity}},k}\}$. In the case of the preferred turbo encoder of the present invention, the unpunctured codeword bits are bit *separated into respective “Systematic”, “Parity 1” and “Parity 2” streams denoted by $x_{S,k}$, $p_{1,k}$, $p_{2,k}$ where $k \in \{1, \dots, N_{\text{info}}\}$* . . . The tail bits from the coder *are buffered separately* and are later appended onto the unpunctured instantaneous codeword transmitted in a specific transmission time interval (TTI).”)
- **Stewart 6:41-52** (“In general, the predefined redundancy comprises a redundancy version for the coded bits of the block interleavers wherein the redundancy version sets one or more starting rows $\alpha_{i,j}$ for each redundancy version j , where $i \in \{S,P\}$ and $\alpha_{i,j} \in \{1, \dots, N_{i,\text{max_row}}\}$ and *reads the coded bits from the selected starting rows in a pre-defined order and ratio*, wherein if the end of the $N_{i,\text{max_row}}^{\text{th}}$ interleaver is reached, reading shall continue from the first row of a predefined interleaver which includes one of the systematic and parity block interleavers. The set of redundancy versions may be of any size and may be constructed on a static, semi-static or variable basis.”)
- **Stewart 9:39-46** (“FIG. 11 shows a flow chart representing a method of block puncturing for turbo code based *incremental redundancy*, in accordance with the present invention. A first step of the method is coding 1200, such as turbo coding, an input data stream into systematic bits and parity bits. A next step is loading 1202 *loading the systematic bits and parity bits into respective systematic and parity block interleavers* in a column-wise manner, as described previously.”)

- *See also* Stewart 3:64-4:13; 5:38-40.

(f) Element [3.e]

143. Element [3.e] recites “selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.” This element is met by Stewart.

144. Stewart discloses selecting, by the apparatus (*see* [3.pre], including a “redundancy version selector” (5:57-6:41, Fig. 3)), **bits for transmission based on a plurality of redundancy versions** (*e.g.*, “a preferred set of eight redundancy versions for selecting coded bits from the systematic and parity interleavers” (6:53-7:4)); **wherein at least one redundancy version of the set selects systematic bits over first and second parity bits** (*e.g.*, “Redundancy version zero[] ... systematic interleaver is read from its starting row to completion before the remaining coded bits are read from the parity interleaver” (6:53-7:4)) **and at least one redundancy version of the set selects first and second parity bits over systematic bits** (*e.g.*, “Redundancy version one[] ... the coded bits are read from the parity interleaver starting at its starting row” (6:53-7:4); as shown in Fig. 6, systematic bits are not selected).

145. As I discuss in element [3.pre], **Stewart** discloses an apparatus, e.g., a UE or base station, for use in wireless communications comprising. *See* [3.pre]. **Stewart** also discloses that the UE or BS selects between systematic, first parity, and second parity bits which are then read out from the block interleavers in a particular order to form the codeword that is to be transmitted. Stewart, 2:51-53, 5:6-15, Fig. 5; *see* [3.a]-[3.d]. **Stewart** teaches that selecting the type of bits is carried out using a “redundancy version selector,” and that the selection is based on a redundancy version preselected from a set of redundancy versions (e.g., “Redundancy version zero[],” “Redundancy version one[],” “Redundancy version two[],” “Redundancy version[] three,” “Redundancy version four[],” “Redundancy version five[],” and “Redundancy version six[]”). Stewart, 3:25-36, 4:8-10, 5:57-6:13, 6:41-7:24, Figs. 3, 11. Each redundancy version in the set of redundancy versions defines a row in a block interleaver that serves as the starting point to commence reading. *Id*; *see also* Fig. 6 (color-coded, below).

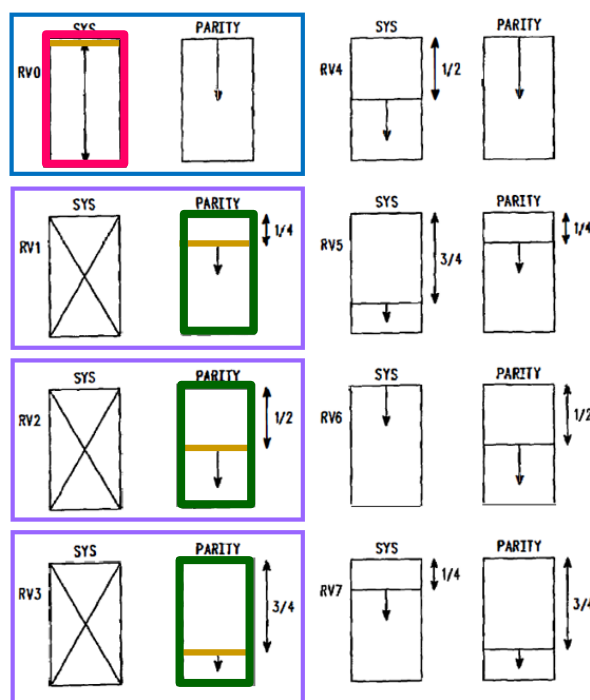


FIG. 6

“at least one redundancy version of the set selects systematic bits over first and second parity bits”

“at least one redundancy version of the set selects first and second parity bits over systematic bits”

146. For example, “Redundancy version zero[]” commences reading at the top row of the parity interleaver. Stewart, Fig. 6, 6:57-61. As another example, “Redundancy version one[]” commences reading at a row that is one-fourth of the way down in the parity interleaver. Stewart, 6:62-64; *see also* Stewart (“Redundancy version two[]” and “Redundancy version three[]”). Stewart, 6:41-52, 6:53-7:24, Fig. 6.

147. Stewart discloses **at least one redundancy version out of the set of redundancy versions that selects systematic bits over first and second parity bits**. For example, “redundancy version zero” entails commencing reading at a **starting point** at the first row of the **systematic interleaver**. After reading through

the **systematic interleaver**, reading wraps around to the first row of **the parity interleaver**. Stewart, 6:41-52, 6:57-61 (“coded bits from the systematic interleaver is read from its starting row to completion before the remaining coded bits are read from the parity interleaver starting at its starting row”); *see also* Fig. 6 (color-coded, above). In such a scenario, the reading of systematic bits from **the systematic interleaver** before **the first and second parity interleaver** meets the claimed systematic bits are selected over the first and second parity bits.

148. **Stewart** discloses **at least one redundancy version out of the set of redundancy versions that selects first and second parity bits over systematic bits**. For example, **Stewart** discloses “redundancy version one” (depicted in Fig. 6) that contains a single arrowed line in **the parity interleaver** and an “X” in the **systematic interleaver**. Stewart, Fig. 6. For this redundancy version, according to **Stewart’s** “Rule 5,” the codeword bits are read from the block interleaver that contains the single arrowed line and according to “Rule 2,” no codeword bits are read out from the interleaver that contains the “X.” Stewart, 6:16-18, 6:25-29. So, reading of the first and second parity bits starts about one-fourth of the way down in the parity interleaver (“1/4” or “ $N_{p,max_row}/4$ ”) and completes at **the parity block interleavers**. Stewart, 6:41-52, 6:62-66, Fig. 6. In such a scenario, the first and

second parity bits are selected to be transmitted but the systematic bits are not, so first and second parity bits are selected over the systematic bits.

149. As another example, **Stewart** discloses “redundancy version two” (depicted in Fig. 6) that contains a single arrowed line in **the parity interleaver** and an “X” in **the systematic interleaver**. Stewart, Fig. 6. For similar reasons, according to **Stewart’s** “Rule 5” and “Rule 2,” the codeword bits are read from the **first and second parity interleavers** and no codeword bits are read out from the **systematic interleaver**. Stewart, 6:16-18, 6:25-29. Reading of the first and second parity bits starts in a row that is half-way down in the parity interleaver (“ $1/2$ ” or “ $N_{p,max_row}/2$ ”) and completes at the parity block interleavers. Stewart, 6:41-52, 6:65-67, Fig. 6. In such a scenario, the first and second parity bits are selected to be transmitted but the systematic bits are not, so first and second parity bits are selected over the systematic bits.

150. As another example, **Stewart** discloses “redundancy version three” (depicted in Fig. 6) that contains a single arrowed line in **the parity interleaver** and an “X” in **the systematic interleaver**. For this redundancy version, reading of the first and second parity bits starts at a row three-fourths of the way down in the parity interleaver (“ $3/4$ ” or “ $3N_{p,max_row}/4$ ”) and completes at **the parity block interleavers**. Stewart, 6:41-52, 7:1-7:4, Fig. 6. In such a scenario, the first and second parity bits

are selected to be transmitted but the systematic bits are not, so first and second parity bits are selected over the systematic bits.

151. In addition, **Stewart** alternatively discloses a scenario that arises if the last row of the interleaver from which reading commenced has been read-out, but that the desired numbers of bits has not yet been obtained and the reading process is not yet completed. Stewart, 5:33-47, 6:41-52, 6:57-61, Fig. 6. In such a scenario, **Stewart** teaches that the reading continues (*i.e.*, “wrap[] around”) starting at the first row of another interleaver. Stewart, 5:33-37. As one example, if reading commences in a **starting row** of a first **parity interleaver** but the desired number of bits has not been read after the last row in the **first parity interleaver** has been read out, reading continues at the first row of another interleaver, such as a **second parity interleaver** or the **systematic interleaver**; if the desired number of bits has not been read after the last row of the second parity interleaver or systematic interleaver has been read, then reading continues at the first row of another interleaver, such as a **systematic interleaver** or **first parity interleaver**. *Id.* Accordingly, not only does **Stewart** render obvious reading the systematic bits after the parity bits, but discloses such a teaching. Stewart, 5:33-37.

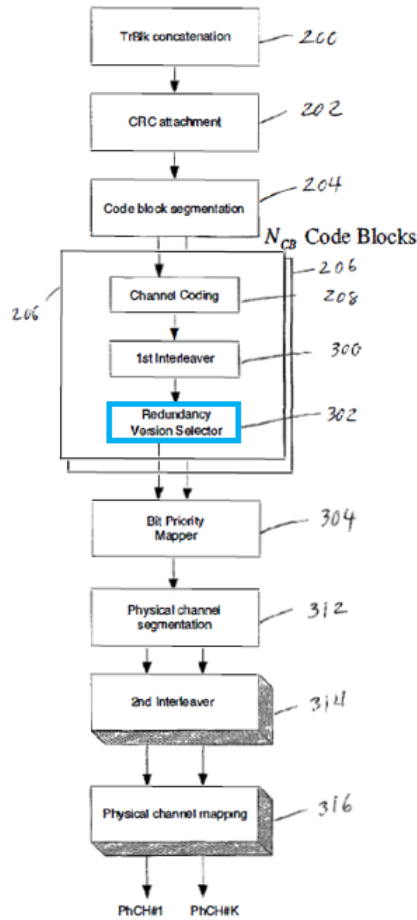
152. As discussed above in Section IX.A.1 (Overview of Stewart) **Stewart** discloses a redundancy version from a set of redundancy versions that results in a

larger total number of systematic bits selected for transmission than the total number of parity bits selected for transmission. For instance, a $3/5$ code rate (which **Stewart** teaches is used with “redundancy version zero”) refers to the case in which 3 out of every 5 of the total bits transmitted are systematic bits, and the remaining 2 out of every 5 of the total bits transmitted are parity bits. Stewart, 7:27-31. Accordingly, to achieve a $3/5$ code rate, a larger number of systematic bits than parity bits (in aggregate) are selected for transmission. A $1/4$ code rate refers to the case in which 1 out of every 4 of the total bits transmitted are systematic bits and the remaining 3 out of every 4 of the total bits transmitted are parity bits. Accordingly, to achieve a $1/4$ code rate (which **Stewart** teaches is desirable for “redundancy version four”), more parity bits than systematic bits (in aggregate) are selected for transmission. Stewart, 7:33-34.

153. *E.g.*, **Stewart** (emphasis added):

- **Stewart Figure 3**

FIG. 3



“selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits”

• **Stewart Figure 5** “bits for transmission”

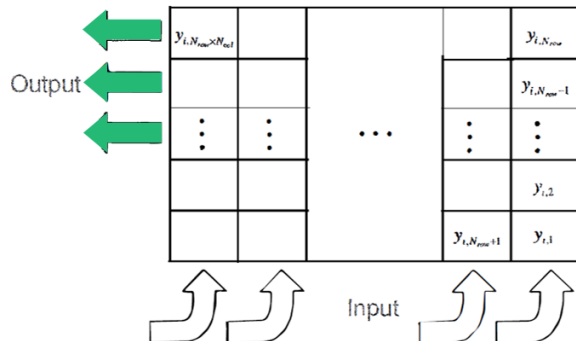


FIG. 5

• **Stewart Figure 6**

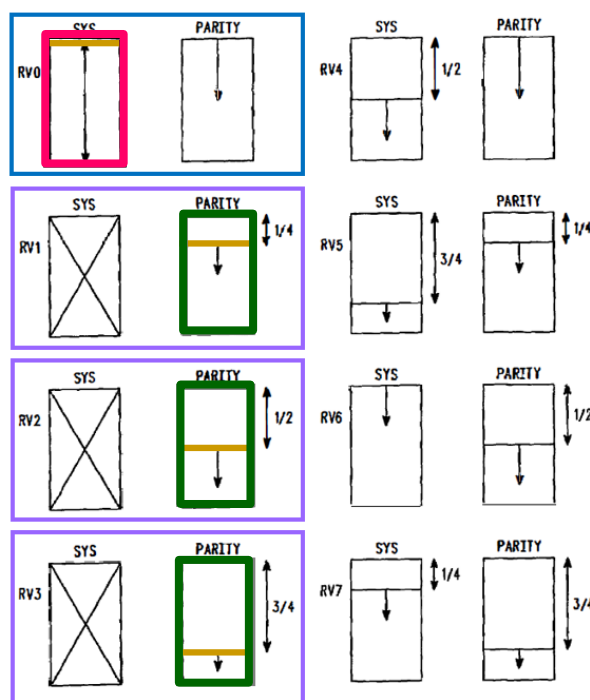


FIG. 6

“at least one redundancy version of the set selects systematic bits over first and second parity bits”

“at least one redundancy version of the set selects first and second parity bits over systematic bits”

- **Stewart 2:51-53** (“Codeword bits are read in column-wise while the desired amount of unpunctured data is then read out row-wise after row and column rearrangement.”)
- **Stewart 3:25-36** (“The present invention provides a flexible IR scheme specifically applicable to HSDPA. In particular, the IR scheme of the present invention supports: a) a flexible method of controlling the instantaneous and variable final code rate of the HARQ process (ranging from Chase combining to rate- $\frac{1}{3}$ expansion), b) general QAM modulation, including 16-QAM, c) *a specific set of possible redundancy versions from which can be selected an optimal (or simply preferred) sequence of redundancy versions*, based on the specific acknowledge/negative acknowledge (ACK/NACK) signal evolution applicable to HSDPA, and d) a novel implementation of block interleavers.”)
- **Stewart 4:8-10** (“The present invention occurs in the first interleaver 300, *redundancy version selection 302*, and the optional bit priority mapper 304.”)
- **Stewart 5:6-15** (“After the row and column permutation, *the desired number of codeword bits can then be read out in row-wise fashion*. Using the notation of FIG. 4, if the desired number of parity

bits is an odd number and if $x_{P,k} = \{p_{1,k}, p_{2,k}\}$ is the last symbol read from the parity interleaver, then the parity bit $p_{1,k}$ is used as a codeword bit while the parity bit $p_{2,k}$ is discarded. In the case of the parity interleaver, the **maximum number of rows that can be transmitted** N_{p,max_row} may be less than N_{row} due to UE memory restrictions, while for the systematic interleaver N_{S,max_row} is always equal to N_{row} .”)

- **Stewart 5:33-37** (“When more coded bits are required than can be obtained by reading to the end of the N_{i,max_row}^{th} row, $i \in \{S,P\}$, **reading may continue by wrapping around to the beginning of the first row of the same or another interleaver**. One consequence of this is to allow coding rates less than $\frac{1}{3}$.”)
- **Stewart 5:57-6:40** (“Referring back to FIG. 3, the present invention also incorporates **a redundancy version selector 302**. Since a different number of codeword bits may be obtained from the systematic and parity block interleavers, the framework of the present invention allows for both Chase and incremental redundancy (IR) coding schemes. **In order to support different redundancy versions, any row of any block puncturing interleaver may be assigned as a starting point at which to commence the readout of codeword bits**. By defining multiple starting points for one redundancy version, the order and/or the ratio in which codeword bits are be read out from the systematic and parity interleavers can provide further degrees of freedom in describing any potential redundancy version. **The set of redundancy versions defined between the Node B and UE can be of any size, and may vary dynamically or semi-statically in size and form (e.g. through explicit signaling of redundancy versions or a subset of a pre-agreed redundancy versions between the Node B and UE) or as in the preferred implementation shown in FIG. 6.be [sic] derived from a pre-defined static set**. Although, smaller or larger sets of redundancy versions can be used, the eight redundancy versions ($RV_i, i \in \{0, \dots, 7\}$) shown require three bits for signaling in the HS-DSCCH with the following preferred rules used to define all the versions shown.

Rule 1: Each rectangle represents rows 1 to N_{i,max_row} for $i \in \{S,P\}$.

Rule 2: The X (e.g. RV1, RV2, RV3) inside an interleaver signifies no bits are used from that interleaver to form the instantaneous codeword.

Rule 3: The double arrowed line inside an interleaver signifies all bits in 1 to N_{i,max_row} in that block interleaver must be transmitted exactly once (e.g. RV0).

Rule 4: In the case there is an X in one interleaver and a single arrowed line in the other, then codeword bits are only read from the block interleaver with the single arrowed line.

Rule 5: In the case there is a double arrowed line in one interleaver and a single arrowed line in the other, then codeword bits are only read from the block interleaver with the single arrowed line once reading from the double arrowed line is complete.

Rule 6: In the case there is a single arrowed line in both interleavers, then codeword bits are read equally from both block interleavers.

Rule 7: If reading from a block interleaver with a single arrowed line has reached the end of line N_{i,max_row} but more codeword bits are required, then reading wraps around to line 1.

Rule 8: A fractional number N_{frac_num} beside the starting row of a single arrowed line indicates that starting row as $N_{frac_num} \times N_{i,max_row}$.”)

- **Stewart 6:41-52** (“In general, the predefined redundancy comprises **a redundancy version for the coded bits of the block interleavers** wherein the redundancy version sets one or more starting rows $\alpha_{i,j}$ for each redundancy version j , where $i \in \{S,P\}$ and $\alpha_{i,j} \in \{1, \dots, N_{i,max_row}\}$ and reads the coded bits from the selected starting rows in a pre-defined order and ratio, wherein **if the end of the N_{i,max_row}^{th} interleaver is reached, reading shall continue from the first row of a predefined interleaver which includes one of the systematic and parity block interleavers.** The **set of redundancy versions** may be of any size and may be constructed on a static, semi-static or variable basis.”)

- **Stewart 6:53-7:4** (“The present invention includes *a preferred set of eight redundancy versions for selecting coded bits from the systematic and parity interleavers* in accordance with the above rules, as shown in FIG. 6 and as described below.

Redundancy version zero: the starting row is the top row of both the systematic and parity interleavers, and coded bits from the systematic interleaver is read from its starting row to completion before the remaining coded bits are read from the parity interleaver starting at its starting row.

Redundancy version one: the starting row is $N_{p,max_row}/4$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.

Redundancy version two: the starting row is $N_{p,max_row}/2$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.

Redundancy version three: the starting row is $3 \times N_{p,max_row} / 4$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.”)

- **Stewart 7:27-34** (“For example, if on the first transmission RV0 is signaled with enough codeword bits to result in *a rate $\frac{3}{5}$ code (exactly one third of the parity bits transmitted, e.g. one third of “Parity 1” and one third of “Parity 2” stream in the preferred turbo encoder case), the scheduler is permitted choose RV2 for the second transmission. Similarly, if in the first transmission, a rate $\frac{1}{4}$ code is desired, RV4 might be selected for the second transmission.”)*

(g) Claim 4

154. Claim 4 recites “The method of claim 3 wherein the selecting of bits for transmission in response to a selected redundancy version changes in response to a location of the bits in the buffer.” This element is met by Stewart.

155. **Stewart discloses that the selecting of bits for transmission in response to a selected redundancy version (see [3.e]) changes in response to a location of the bits (e.g., different “redundancy version[s]” (6:53-7:3, Fig. 3) have different “starting point[s], at which to commence the readout of codeword bits” (5:57-6:41)) in the buffer (see [3.d]).**

156. *See my discussions pertaining to elements [3.pre], [3.d]-[3.e].*

157. As I discuss in relation to element [3.e], **Stewart** discloses that coded bits selected for transmission are read out of their respective block interleavers, at a particular **starting point**. *See [3.e]; see also color-coded Fig. 6 above.* The **starting point**, which varies based on the redundancy version that is selected, indicates the specific row in a **systematic block interleaver** or **[first /second] parity block interleaver** from where reading commences. Stewart, 5:62-6:3. According to **Stewart’s “Rule 8,”** the **starting point** is “ $N_{frac_num} \times N_{i,max_row}$ ”) which is illustrated next to an interleaver in Fig. 6. Stewart, 6:37-39. N_{frac_num} is a “fractional number” and N_{i,max_row} is number of rows in an interleaver. *Id.* For example, bits that are selected for transmission according to “redundancy version zero” are read out starting at the top row of the parity interleaver. Stewart, Fig. 6, 6:57-61. As another example, bits that are selected for transmission according to “Redundancy version

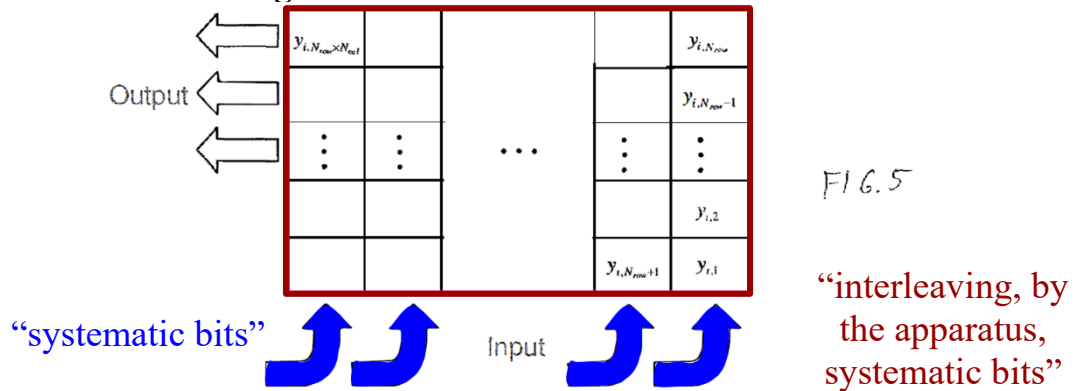
one[]” commences reading at a row that is one-fourth of the way down in the parity interleaver. Stewart, 6:62-64.

158. As I discuss in relation to element [3.d], **Stewart** discloses “read[ing] into” block interleavers the bits from the “‘Systematic’ stream,” first “Parity 1” stream and second “Parity 2” stream. Stewart, 4:14-29; *see* [3.d]. As I discuss in relation to element [3.e], **Stewart** discloses selecting bits from the block interleaver for transmission based on a redundancy version. *See* [3.e]. As I discuss in the paragraph above, **Stewart** discloses that each redundancy version designates a particular row in a block interleaver from which reading commences. So, the bits selected from **Stewart’s** interleavers depend on the redundancy version which dictates the **starting point** (color-coded in Fig. 6 above) within a block interleaver from where the bits are read from. The bits selected for transmission are **located within the buffer** (color-coded in Fig. 6 below) and, accordingly, are located in an area **within the buffer** that depends on the which redundancy version is selected. **Stewart** teaches a dependency of the selected bits on the redundancy version used to select bits for transmission such that varying the redundancy version used accordingly pulls the selected bits from different **locations in the buffer**, and the changes of the bits in those locations affect the selected bits for transmission, and these teachings are consistent with the disclosures of the ’486. Stewart, 5:50-53.

These **Stewart** disclosures regarding the dependency of the selection of bits on the redundancy version and bits located within the block matrix buffer are similar to and consistent with and similar the '486 patent disclosures. *See, e.g.,* '486, 16:10-26, 18:10-19:13.

159. *E.g., Stewart* (emphasis added):

- **Stewart Figure 5**



- **Stewart Figure 6**

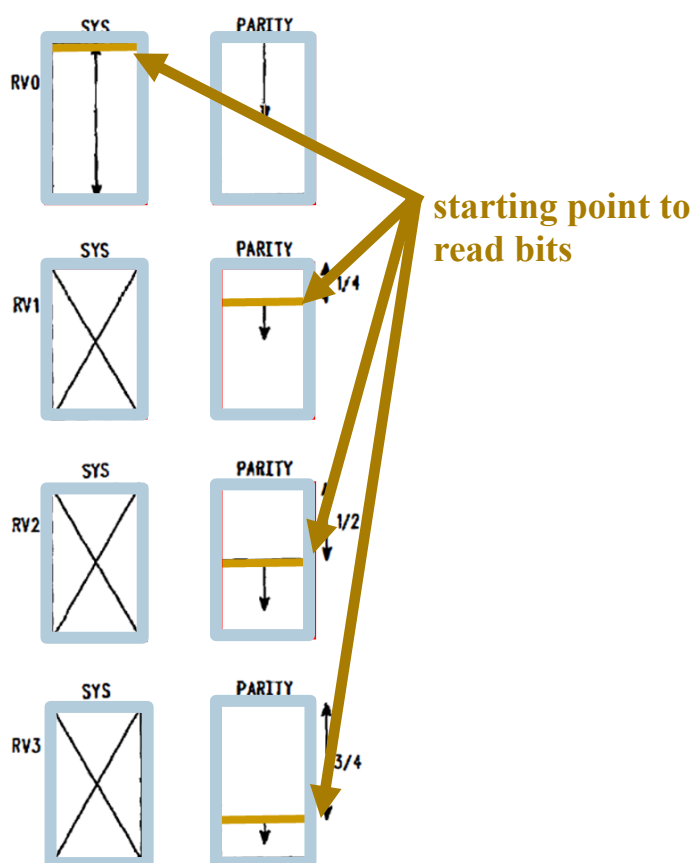


FIG. 6

- **Stewart 4:14-5:8** (“FIG. 4 shows the operation of the *first interleaver* (300 in FIG. 3) in entering a codeword into puncturing interleavers for the preferred turbo encoder. *In the general turbo encoder case a codeword is separated* into a “Systematic” stream and N_{Parity} *parity streams denoted by* $x_{S,k}$, $p_{1,k}$, $p_{2,k}$, $\dots$, $p_{N_{parity},k}$ *where* $k \in \{1, \dots, N_{info}\}$. *Each stream is read into* $N_{row} \times N_{col}$ *block matrix interleavers.* Preferably, the parity bits are combined into one $N_{row} \times N_{col}$ puncturing matrix, but *separate* $N_{row} \times N_{col}$ *parity block interleavers can be used for each parity stream.* In the preferred case of a single parity interleaver $x_{S,k} \in \{1,0\}$ and $x_{P,k}$ is an N_{Parity} bit symbol $x_{P,k} = \{p_{1,k}, p_{2,k}, \dots, p_{N_{parity},k}\}$. In the case of the preferred turbo encoder of the present invention, *the unpunctured codeword bits are bit separated into respective* “Systematic”, “Parity 1” and “Parity 2” *streams denoted by* $x_{S,k}$, $p_{1,k}$, $p_{2,k}$ *where* $k \in \{1, \dots, N_{info}\}$. In the preferred case of a single parity interleaver,

$x_{S,k} \in \{1,0\}$ and $x_{P,k} = \{p_{1,k}, p_{2,k}\}$ where $x_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$. The tail bits from the coder are buffered separately and are later appended onto the unpunctured instantaneous codeword transmitted in a specific transmission time interval (TTI). The number of rows, N_{row} , and number of columns, N_{col} , in each interleaver can be variable and allocated dynamically. In a preferred embodiment, the number of rows, N_{row} , is always fixed at thirty, while the number of columns, N_{col} , is variable (dependent on the number of information bits N_{info}) and is determined in the same manner as the turbo code internal interleavers, such as is described in section 4.2.3.2.3.1 of ‘Technical Specification Group Radio Access Network; Multiplexing and Channel Coding (FDD) (Release 1999)’, TS 25.212 v3.5.0 (2000-12), which is hereby incorporated by reference.

FIG. 5 shows the data stream of the interleavers of FIG. 4. A novel aspect of the present invention is having data read in a column-wise fashion into each interleaver. The data includes dummy bits padded if $N_{info} < N_{row} \times N_{col}$, where $y_k = x_k$ for $k=1, 2, \dots, N_{info}$ and $y_{S,k} \in \{0,1\}$ and $y_{P,k} \in \{\{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}\}$ for $k=\{N_{info}+1, \dots, N_{row} \times N_{col}\}$. These dummy bits are later removed when reading the codeword data row-wise from top-to-bottom from the **block matrix**, similar to the description in section 4.2.3.2.3.2 of TS 25.212, incorporated by reference.

To facilitate flexibility in supporting variable coding rates in the present invention, both columns and rows are permuted prior to reading out the block matrix contents. As an example of the benefit of row and column reordering, consider the case where $N_{row}=30$ and $N_{col}=100$. If the first two rows were to be read out without reordering, the codeword bits would correspond to the 29th, 30th, 59th, 60th, 89th, 90th, $\dots$ stages in the encoder trellis. However, by reordering row 29 with row 15, then the transmitted codeword bits become those at the 15th, 30th, 45th, 60th, 75th, 90th, $\dots$ stages in the encoder trellis, a more homogenous and therefore desirable distribution. In permuting the columns, it is ensured that no sub-block section of the trellis is neglected when only a portion of a row is read out to form the transmitted codeword. The row permutation

is that defined by Table 7 in section 4.2.1.1 of TS 25.212, hereby incorporated by reference.

After the row and column permutation, the desired number of codeword bits can then be read out in row-wise fashion.”

- **Stewart 5:50-53** (“Rate selection therefore occurs as a result of *redundancy version (tells which row to start reading from) and the first interleaver (gives the order bits should be read out).*”)
- **Stewart 5:62-6:40** (“In order to support different redundancy versions, *any row of any block puncturing interleaver may be assigned as a starting point at which to commence the readout of codeword bits.* By defining multiple starting points for one redundancy version, the order and/or the ratio in which codeword bits are be read out from the systematic and parity interleavers can provide further degrees of freedom in describing any potential redundancy version. The set of redundancy versions defined between the Node B and UE can be of any size, and may vary dynamically or semi-statically in size and form (e.g. through explicit signaling of redundancy versions or a subset of a pre-agreed redundancy versions between the Node B and UE) or as in the preferred implementation shown in FIG. 6.be [sic] derived from a pre-defined static set. Although, smaller or larger sets of redundancy versions can be used, the eight redundancy versions ($RV_i, i \in \{0, \dots, 7\}$) shown require three bits for signaling in the HS-DSCCH with the following preferred rules used to define all the versions shown.

Rule 1: Each rectangle represents rows 1 to N_{i,max_row} for $i \in \{S,P\}$.

Rule 2: The X (e.g. RV1, RV2, RV3) inside an interleaver signifies no bits are used from that interleaver to form the instantaneous codeword.

Rule 3: The double arrowed line inside an interleaver signifies all bits in 1 to N_{i,max_row} in that block interleaver must be transmitted exactly once (e.g. RV0).

Rule 4: In the case there is an X in one interleaver and a single arrowed line in the other, then codeword bits are only read from the block interleaver with the single arrowed line.

Rule 5: In the case there is a double arrowed line in one interleaver and a single arrowed line in the other, then codeword bits are only read from the block interleaver with the single arrowed line once reading from the double arrowed line is complete.

Rule 6: In the case there is a single arrowed line in both interleavers, then codeword bits are read equally from both block interleavers.

Rule 7: If reading from a block interleaver with a single arrowed line has reached the end of line N_{i,max_row} but more codeword bits are required, then reading wraps around to line 1.

Rule 8: A fractional number N_{frac_num} beside the starting row of a single arrowed line indicates that starting row as $N_{frac_num} \times N_{i,max_row}$.

- **Stewart 6:53-7:4** (“The present invention includes a preferred *set of eight redundancy versions for selecting coded bits from the systematic and parity interleavers* in accordance with the above rules, as shown in FIG. 6 and as described below.

Redundancy version zero: the starting row is the top row of both the systematic and parity interleavers, and coded bits from the systematic interleaver is read from its starting row to completion before the remaining coded bits are read from the parity interleaver starting at its starting row.

Redundancy version one: the starting row is $N_{p,max_row}/4$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.

Redundancy version two: the starting row is $N_{p,max_row}/2$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.

Redundancy version three: the starting row is $3 \times N_{p,max_row} / 4$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.”)

3. Claims 1-2

160. As I have discussed in Sections IX.A.2(a) (Element [3.pre]) to IX.A.2(g) (Claim 4), **Stewart** not only renders obvious but also anticipates claims 3-4. Claims 1-2 are directed to an apparatus that performs the method of claims 3-4 using hardware components disclosed by **Stewart**. **Stewart** not only renders obvious but also anticipates claims 1-2 for the reasons I discuss in Sections IX.A.2(a) (Element [3.pre]) to IX.A.2(g) (Claim 4). For example, **Stewart** discloses that its incremental redundancy method (*see* Section IX.A.2(a) (Element [3.pre])) is performed in “user equipment (UE), such as a cellular radio communication device,” or a “base station.” *Stewart*, 1:44-64, 3:1-12.

161. Claim 1 generally recites what is recited in claim 3, but claim 1 additionally requires components that perform, respectively, the steps recited in [3.a]-[3.e] of claim 3, *i.e.*, a “first interleaver” ([1.a]), “second interleaver” ([1.b]), “third interleaver,” ([1.c]), “buffer” ([1.d]), and “rate matching unit” ([1.e]).

162. As I articulate in Section VIII.A (Preambles), I have not been asked to formulate any opinion as to whether the preamble of any claim is limiting or not. To the extent that the preamble of claim 1 is limiting, **Stewart** discloses [1.pre], an

apparatus, for the same reasons I discussed in relation to [3.pre] above. Stewart, 1:44-56, 3:1-12.

163. **Stewart** discloses element [1.a], a **first interleaver** (*e.g.*, a “Systematic Block Interleaver” (9:39-59, Figs. 4, 11), “respective systematic ... block interleaver[]” (9:39-59, Fig. 11)) **configured to interleave systematic bits**, for at least the reasons I provided pertaining to element [3.a] in Sections IX.A.2 (Analysis (Claims 3-4)), VIII (Claim Construction). Stewart, Abstract, Fig. 4, 4:14-5:8, 9:39-59.

164. **Stewart** discloses element [1.b], a **second interleaver** (*e.g.*, “separate” (4:14-45) “parity block interleaver[]” (4:14-45, Fig. 11) for “Parity 1” stream (4:14-45)) **configured to interleave a first parity bit stream**, for at least the reasons I provided pertaining to element [3.b] in Sections IX.A.2 (Analysis (Claims 3-4)), VIII (Claim Construction). Stewart, Fig. 4, 4:14-5:8, 9:39-59.

165. **Stewart** discloses element [1.c], a **third interleaver** (*e.g.*, “separate” (4:14-45) “parity block interleaver[]” (4:14-45, Fig. 11) for “Parity 2” (4:14-45) stream) **configured to interleave a second parity bit stream**, for at least the reasons I provided pertaining to element [3.c] in Sections IX.A.2 (Analysis (Claims 3-4)), VIII (Claim Construction). Stewart, Fig. 4, 4:14-5:8, 9:39-59.

166. **Stewart** not only renders obvious but also discloses element [1.d], a **buffer** (*e.g.*, “systematic and parity block interleavers” (Abstract, 5:57-65, 9:39-59)) **configured to buffer** interleaved bits, for at least the reasons I provided pertaining to element [3.d] in Sections IX.A.2 (Analysis (Claims 3-4)), VIII (Claim Construction), and IX.A.1(a) (Buffering by Stewart). Stewart, Fig. 4, 4:14-5:8, 9:39-59. As I discussed in Section IX.A.1(a) (Buffering by Stewart), it was well-known at the earliest priority date of the ’486 patent that buffering is a process of temporarily storing information for transmission. Thus, **Stewart’s** disclosure of temporarily storing interleaved bits within a respective block matrix of a block interleaver is buffering the interleaved bits. It was also well-known that interleavers included memories. Thus, it would have been obvious to use interleavers, which include memories, as buffers to temporarily store interleaved bits. *See* Section IX.A.1(a) (Buffering by Stewart); [3.d]. Moreover, buffering is required to carry out retransmissions as part of a HARQ procedure. *Id.* Accordingly, not only would it have been obvious to a person of ordinary skill in the art to use **Stewart’s** block interleavers to interleave *and* buffer the interleaved systematic, first parity, and second parity bits to facilitate **Stewart’s** HARQ procedure, but **Stewart** discloses that the interleavers buffer interleaved systematic, first parity, and second parity bits. *Id.*

167. **Stewart** not only renders obvious but also discloses element [1.e], a **rate matching unit** (*e.g.*, a “redundancy version selector” (5:57-6:41, Fig. 3)), for at least the reasons I provided pertaining to element [3.e] in Sections IX.A.2 (Analysis (Claims 3-4)), VIII (Claim Construction). **Stewart**, Fig. 3, 4:2-13, 5:50-53, 5:57-7:43. The “redundancy version selector” in **Stewart’s** selects between systematic, first parity, and second parity bits for transmission based on a set of redundancy versions. *See* [3.e]; **Stewart** 5:57-62; Section VIII (Claim Construction). As I discussed above, a subset of redundancy versions selects systematic bits over first and second parity bits; another subset of redundancy versions selects first and second parity bits over systematic bits. *Id.* Accordingly, **Stewart’s** “redundancy version selector” performs the same function as the ’486 patent’s “rate matching unit” recited in element [3.e]. *See* [3.e]; **Stewart** 5:57-62; Section VIII (Claim Construction).

168. Claim 2 is directed to an apparatus that performs the method of claim 4. For at least the reasons I provided pertaining to element [3.e] and [4] in Sections IX.A.2 (Analysis (Claims 3-4)) and VIII (Claim Construction), **Stewart** not only renders obvious but also anticipates claim 2. For example, **Stewart** discloses a component “redundancy version selector” (5:57-6:41, Fig. 3) that performs the method of claim 4. *See* [3.e] and [4] in Section IX.A.2 (Analysis (Claims 3-4)).

4. Claims 5-6

169. Claim 5 (elements [5.a]-[5.e]) generally recites what is recited in claim 3, but claim 5 additionally requires “circuitry” that perform the steps recited in [3.a]-[3.e] of claim 3. **Stewart** not only renders obvious but also anticipates claims 5-6 for the reasons I discuss in Sections IX.A.2(a)-IX.A.2(g) (Element [3.pre])-(Claim 4).

170. As I articulate in Section VIII.A (Preambles), I have not been asked to formulate any opinion as to whether the preamble of any claim is limiting or not. To the extent that the preamble of claim 5 is limiting, **Stewart** discloses [5.pre] that recites a “wireless transmit/receive unit” for at least the reasons I provided pertaining to element [3.pre]. For example, **Stewart** discloses that its incremental redundancy method (*see* Section IX.A.2(a) (Element [3.pre])) is performed in “user equipment (UE), such as a cellular radio communication device” or a “base station” **Stewart**, 1:44-64, 3:9-12, 5:57-62, 9:60-10:3. A UE is a “wireless transmit/receive unit” because it can send/receive wireless communications.

171. **Stewart** not only renders obvious but also discloses the **circuitry** (*e.g.*, computer or phone programmed or configured with “coding structure”) required for claim 5 for at least the reasons I provided pertaining to claims 1 and 3. **Stewart**, 2:25-26, 9:60-10:3. For example, **Stewart** teaches that its Incremental Redundancy

(IR) method (*see* [3.pre]) is implemented as a “coding structure” or “channel coding model,” which are a set of instructions (*e.g.*, code) that “any two-way wireless communications device” would be programmed or configured with such that the device executes the instructions. Stewart, Fig. 3, 2:25-26, 3:64-4:13. Such a communications device is, for example, a cellphone, laptop, UE or base station. A person having ordinary skill in the art would have known that circuitry is used to implement such wireless communications devices. For example, Nickum discloses that a “communication apparatus” is implemented using “circuitry.” Ex. 1034, 4:57-62 (“Two digital signal processors (DSPs) 42 and 44, with *associated circuitry, may be connected or built in to the cellular telephone 14* to assist in the control of the communication.”) (emphasis added). **Stewart** discloses that each element recited in claim 1 is part of the same “coding structuring” or “channel coding model,” thereby **Stewart’s** “interleavers” and “redundancy version selector” not only renders obvious but also discloses elements [5.a]-[5.e] for at least the reasons I discussed above pertaining to claims 1 and 3.

172. Claim 6 generally recites what is recited in claims 2 and 4. For at least the reasons I provided pertaining to claims 2 and 4 in Sections IX.A.2 (Analysis (Claims 3-4)), VIII (Claim Construction), **Stewart** not only renders obvious but also anticipates claim 6.

173. To the extent that the patent owner presents any arguments stating that **Stewart’s** teachings are limited to the downlink, a person having ordinary skill in the art would have been motivated to modify Stewart's teachings to also the uplink for the same reasons I provided above (Section VIII (Claim Construction)). *See also* Kinjo, 6:55-64 (“Although at present there is no real demand to increase the throughput during an uplink transmission, it will be appreciated that the advantages of this invention may also be used during an uplink transmission.”).

B. Ground 2: Stewart in View of 3GPP-Summary (Claims 1-6)

174. In addition to my discussion of Ground 1 above, here, I explain why the teachings from **Stewart** in view of **3GPP-Summary** render obvious each of the Challenged Claims.

1. “buffer[ing]” ([3.d]/[1.d]/[5.d])

175. **Stewart** in view of **3GPP-Summary** teaches further details of the features recited in limitations **[3.d]**, **[1.d]**, and **[5.d]** to the extent they require a hardware component (*i.e.*, a buffer) that is separate from an interleaver: “buffering...the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream” (recited in **[3.d]**); “buffer configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream” (recited in **[1.d]**); and “circuitry...configured

to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream” (recited in [5.d]). Accordingly, **Stewart** in view of **3GPP-Summary** renders obvious limitations [3.d], [1.d], and [5.d], thus renders obvious claims 1-6.

176. **3GPP-Summary** teaches **buffering the interleaved systematic bits, the interleaved first parity bit stream, and the interleaved second parity bit stream** in a separate buffer (*e.g.*, “transmitter buffer” or a “ring buffer” that stores “interleaved systematic bits” and “interleaved parity bits.”). 3GPP-Summary, §2.4. A ring buffer, also referred to as a circular buffer, is a kind of buffer, that is implemented in hardware and buffers bit streams, and is particularly useful when the data in the queue for transmission has a fixed payload size.

177. **3GPP-Summary**, titled “Overview of Proposed Schemes for Incremental Redundancy,” is a submission by Ericsson to the to the 3rd Generation Partnership Project (“3GPP”) Radio Access Network Working Group 1 (“WG1”), which is the primary Standard Setting Organization (SSO) in the wireless communications space responsible for specifying and maintaining cellular telecommunications standards including LTE and UMTS. **3GPP-Summary** was a proposal submitted for a 3GPP meeting, R1-ah-22010, held between November 5-7, 2001 in Sophia Antipolis, France, which is after **Stewart** was filed (October 22,

2001). **3GPP-Summary** served to summarize the plethora of proposals from Ericsson, Texas Instruments, Siemens, Motorola, Nokia, and OKI that were submitted to WG1 at approximately the same period on the topic of incremental redundancy, specifically “implementation of incremental redundancy for HSDPA.” **3GPP-Summary**, §1. In this regard, **3GPP-Summary** is directed to the same field as **Stewart**: applications of incremental redundancy (IR), and because IR is a type of HARQ process, both references generally pertain to HARQ transmissions. *Stewart*, 1:57-64, 2:47-67; **3GPP-Summary**, §§1, 2.4. A person of ordinary skill in the art would have also understood that **3GPP-Summary** and **Stewart** are in the same field as the ’486 (*e.g.*, improvements to coding schemes for wireless communications) and reasonably pertinent to the problems identified in the ’486 (*e.g.*, using redundancy versions to implement an IR process for transmitting information between two wireless devices, such as a user device and a base station). *E.g.*, ’486, Abstract; 4:53-5:13; *Stewart*, Abstract, 2:47-67; **3GPP-Summary**, §§1, 2.4.

178. **3GPP-Summary** summarizes the proposal contained in the Motorola submission (R1-01-1014). *See* **3GPP-Summary**, §§2.4, 4 (reference “[4]”). When summarizing Motorola’s submission, **3GPP-Summary** alludes to a “new ‘ring buffer’ scheme” that entails: (1) “systemic bits and parity bits” that are re

“interleaved separately”; and (2) “stor[ing]” the “interleaved systematic bits” and “interleaved parity bits” in a “transmitter buffer” until they are “transmitted from the buffer.” 3GPP-Summary, §2.4. **3GPP-Summary** also alludes to “UE buffering memory.” *Id.* In this context, a “transmitter buffer” is a type of buffer in a transmitting device, such as a user device or user equipment (“UE”), that temporarily stores bits in memory that have yet to be transmitted. *Id.*

179. A person of ordinary skill in the art would at least have been motivated to modify **Stewart** with **3GPP-Summary**’s teachings of a “transmitter buffer” to buffer interleaved systematic bits and interleaved parity bits prior to transmission in a “transmitter buffer” that is placed at the output of **Stewart**’s interleavers and before **Stewart**’s redundancy version selector, as taught in **3GPP-Summary**. 3GPP-Summary, §2.4; Stewart, 5:29-8:30, Figs. 6-7. Such a modification would have supported the simultaneous loading of bits into an interleaver while bits are transmitted from the buffer. *See* Ex. 1042, 7:43-46, 13:33-39, Figs. 4, 7. And such a modification applies known common hardware component, *e.g.*, a buffer, and application of known engineering, physics, and/or design principles that were used in wireless communication devices to yield predictable results. Buffers are standard, well-known hardware components used in wireless communication systems to buffer bits in order to support retransmission of unsuccessfully received signals as

part of an overall HARQ process that **Stewart** is directed to. *See* Section IX.A.1(a) (Buffering by Stewart); Stewart, 4:14-34, 46-48. Indeed, “buffer” and “buffering” are common terms and defined in technology dictionaries. As I mentioned in Section IX.A.1(a) (Buffering by Stewart), the IEEE 1000 The Authoritative Dictionary of IEEE Standard Terms, defines “buffer” as a “device in which data are stored temporarily, in the course of transmission from one point to another used to compensate for a difference in the flow of data, or time of occurrence of events, when transmitting data from one device to another” or “device or storage area used to store data temporarily to compensate for differences in rates of data flow, time of occurrence of events, or amounts of data that can be handled by the devices or processes involved in the transfer or use of the data.” Ex. 1025. Microsoft Dictionary defines “buffer” as a “region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations or devices,” and “buffering” as “us[ing] a region of memory to hold data that is waiting to be transferred, especially to or from input/output (I/O) devices such as disk drives and serial ports.” Ex. 1026. A person of ordinary skill in the art would have understood that a buffer temporarily stores data so that it could readily be accessed in order to be retransmitted when a transmitting device is requested to carry out a retransmission as part of a HARQ

process. Moreover, many references that predate the '486 invention disclose the use of buffers that performs buffering to facilitate HARQ transmissions. As one example, U.S. Patent Pub. No. 2004/0037224A1 ("Choi") discloses using a "HARQ retransmission buffer" to buffer coded bits as part of a HARQ process. Ex. 1040, [0034]-[0037], [0045]. As another example, U.S. Patent No. 7,286,540 ("Kim") discloses using "a plurality of HARQ channel retransmission buffers" for a similar purpose. Ex. 1041, 4:1-7, 4:32-58, 11:48-57, 15:30-34. Thus, a "buffer" is a well-known component that implements the well-known process of "buffering" which entails using a region of memory to temporarily store information that is to be transmitted in order to facilitate processes such as HARQ such that HARQ can be carried with lower latency and improves the successful delivery of retransmissions to a recipient. **Stewart** discloses interleavers to store bits and using buffers to store bits along with interleaved bits. Stewart, 4:29-34, 5:38-40. **3GPP-Summary** discloses using a type of buffer, a "transmitter buffer," to "store[]" interleaved systematic bits and interleaved parity bits before they are "transmitted...from the buffer." 3GPP-Summary, §2.4. Specifically, **3GPP-Summary's** disclosed "ring buffer" is a circular buffer that supports a wrap-around reading process in which bits are read out for transmission from the end of a buffer to the beginning of another buffer, such that a larger number of coded bits are read out from the buffers for

transmission. 3GPP-Summary, §2.4. Because additional coded bits for transmission are read out from the buffer, the wrap-around functionality allows coded bits that would have otherwise been discarded to be transmitted which also allows for lower coding rates, which are desirable in, for example, particular channel conditions, and allows for greater flexibility in **Stewart's** system. Stewart, 5:33-37.

180. A person of ordinary skill in the art would have had a reasonable expectation of success modifying **Stewart** with the teachings of **3GPP-Summary** that entail using a “transmitter buffer” to store interleaved systematic bits and interleaved parity bits outputted from **Stewart's** System Block Interleaver and Parity Block Interleavers for at least the reason that a transmitter buffer was standard and well-known for storing bits prior to transmission in order to facilitate retransmissions carried out as part of a HARQ process. Ex. 1040, [0034]-[0037], [0045] (“HARQ retransmission buffer”); Ex. 1041, 4:1-7, 4:32-58, 11:48-57, 15:30-34; Ex. 1027, ¶[0034]. Buffers used in a HARQ process, as a person of ordinary skill in the art would have understood, would have improved the latency and reliability of a HARQ process. Additionally, as discussed above, **3GPP-Summary's** “ring buffer” has wrap-around functionality that can support additional coding rates (specifically, lower coder rates) that would be desirable to be used when particular channel conditions are met in wireless communications, and would improve the overall

flexibility of **Stewart's** system. **Stewart**, 5:33-37. Moreover, modifying **Stewart** with **3GPP-Summary's** teachings in this way so that bits are buffered prior to transmission would have been a straightforward application of those teachings, with a reasonable expectation of success, such that the latency, reliability, and flexibility of **Stewart's** system are advantageously improved.

2. “at least one redundancy version of the set selects first and second parity bits over systematic bits” [3.e], [1.e], [5.e]

181. **Stewart** in view of **3GPP-Summary** teaches further detail of the limitations recited in elements **[3.e]**, **[1.e]**, and **[5.e]** (“at least one redundancy version of the set selects first and second parity bits over systematic bits”), and thus renders obvious claims 1-6. **3GPP-Summary** teaches **at least one redundancy version of the set selects first and second parity bits over systematic bits** (*e.g.*, “different initial positions” “defined in the buffer, giving” “eight [] redundancy versions,” where “systematic bits are stored, followed by [] parity bits” and “wrap around is used at the end of the buffer”). **3GPP-Summary**, §2.4.

182. In summarizing the Motorola submission, **3GPP-Summary** discloses “eight [] redundancy versions,” each associated with “[e]ight different initial positions” the indicate the starting point where the reading of bits from the “transmitter buffer” for transmission, and these “initial positions” are “defined in the [transmitter] buffer.” **3GPP-Summary**, §2.4. The “transmitter buffer” stores

“interleaved systematic bits followed by the interleaved parity bits.” *Id.* **3GPP-Summary** discloses that “[a]t transmission, bits are sequentially transmitted from the buffer, starting at the selected initial position” and then the reading of the bits for transmission then “wrap[s] around...at the end of the buffer.” *Id.* So, a person of ordinary skill in the art would have understood that if the “starting point” is located in the area of the “transmitter buffer” that stores the “interleaved systematic bits,” systematic bits are read out from the “transmitter buffer” for transmission before the parity bits are read out. *Id.* If the “starting point,” on the other hand, is located in the area of the “transmitter buffer” that stores the “interleaved parity bits,” the parity bits are read out from the “transmitter buffer,” and then reading wraps around to the systematic bits. *Id.* Accordingly, **3GPP-Summary** teaches reading out for transmission systematic bits followed by interleaved parity bits (*i.e.*, selecting parity bits over systematic bits) and vice versa (reading out for transmission interleaved parity bits and wrapping out to read out interleaved systematic bits, *i.e.*, selecting systematic bits over parity bits).

183. A person of ordinary skill in the art would have understood **3GPP-Summary** and **Stewart** to be in the same field as the '486 and reasonably pertinent to the alleged problems identified in the '486 for at least the reasons I discussed

below, in Section IX.B (Ground 2: Stewart in View of 3GPP-Summary (Claims 1-6)).

184. A person of ordinary skill in that art would have been motivated to modify **Stewart** by using the teachings of **3GPP-Summary's** redundancy versions and “starting points” because **3GPP-Summary's** provides an alternative implementation of redundancy versions for the selection of bits for transmission to the implementation of **Stewart's** redundancy versions for the selection of bits for transmission. 3GPP-Summary, §2.4, Figs. 4-5; Stewart, 5:29-40, 5:57-7:24, Fig. 6. For at least the reasons I discussed pertaining to **Motorola** (see Section IX.D (Grounds 4-6: Grounds 1-3 in Further View of Motorola (Claims 1-6))), **3GPP-Summary's** alternative implementation of redundancy versions (relative to **Stewart's** implementations) provides several advantages for a HARQ process that both references are directed to, these benefits, namely obtaining additional granularity in starting rows of the interleavers. Section IX.D (Grounds 4-6: Grounds 1-3 in Further View of Motorola (Claims 1-6))). A person of ordinary skill in the art would have recognized these advantages and, accordingly, been motivated to modify **Stewart** with **3GPP-Summary's** teachings of using redundancy versions that define different starting points to, *e.g.*, obtain additional granularity in starting rows of interleavers, whereby the “starting point” for reading of bits for transmission varies

between **Stewart's** “systematic bits,” “first parity bits” and “second parity bits,” stored in **Stewart's** Block Interleavers (that act as buffers with memory) or in **3GPP-Summary's** “transmitter buffer.”

185. As I discuss below in connection with **Motorola** (*see* Section IX.D (Grounds 4-6: Grounds 1-3 in Further View of Motorola (Claims 1-6))), a variety of redundancy versions are used to support IR procedures and each redundancy version allows for better reliability under certain conditions, such as the conditions of the channel HARQ transmissions are transmitted on. Having additional (or alternative) redundancy versions allows for more combinations and orderings of systematic and parity bits that improve **Stewart's** incremental redundancy (IR) and HARQ procedures under certain conditions. Section IX.D (Grounds 4-6: Grounds 1-3 in Further View of Motorola (Claims 1-6)). Moreover, implementing a redundancy version that starts allows for reading out redundancy bits for transmission and wrapping around to read out systematic bits (as I discussed above is taught in **3GPP-Summary**) provides benefits such as those explicitly called out in **Motorola**: “allowing coding rates less than $1/3$,” and providing a redundancy version that “adjusts naturally to support” various coding schemes. Motorola, §§2.1(2.1), 2.2(2.2). Thereby, implementing the teachings of **3GPP-Summary** to **Stewart**

would enable **Stewart's** system to better accommodate a larger set of conditions and greater flexibility.

186. In light of the benefits I mentioned above of using additional alternative redundancy versions, a person of ordinary skill in the art would have been motivated to modify **Stewart** with the teachings of **3GPP-Summary** to include another redundancy version in a set of redundancy versions (in which a starting position is defined such that reading out bits for transmission starts where the parity bits are stored, and the parity bits are read out followed by systematic bits) in combination with **Stewart's** “redundancy version zero” (in which systematic bits are first read from the systematic block interleaver and then first and second parity bits are read out from the first and second parity block interleavers. *Stewart*, 5:29-8:30, Fig. 6; *3GPP-Summary*, §2.4. With such modifications, **Stewart's** system would include at least one redundancy version of the set selects systematic bits over first and second parity bits (*e.g.*, **Stewart's** “redundancy version zero”) and at least one redundancy version of the set selects first and second parity bits over systematic bits (*e.g.*, as taught by **3GPP-Summary**).

187. A person of ordinary skill in the art would have had a reasonable expectation of success in modifying **Stewart** to use **3GPP-Summary's** teachings of redundancy versions that have different starting points in **Stewart's** systematic

parity interleaver and first and second parity interleavers to commence reading out of bits for transmission. As discussed above, a person of ordinary skill in the art would have recognized and appreciated that different redundancy versions results in different advantages, such as additional granularity of starting points in each redundancy version, in a system that carries out HARQ transmissions, as I discuss in Section IX.D (Grounds 4-6: Grounds 1-3 in Further View of Motorola (Claims 1-6)). As one example, having additional (or alternative) redundancy versions allows for more combinations and orderings of systematic and parity bits that improve **Stewart's** incremental redundancy (IR) and HARQ procedures under certain conditions. Section IX.D (Grounds 4-6: Grounds 1-3 in Further View of Motorola (Claims 1-6)). **Stewart** discloses using multiple redundancy versions, of which at least one redundancy version that results in reading out of coded bits from a first interleaver and, once all the coded bits have been read out of the first interleaver but the desired number of coded bits read out has not been reached, the reading wraps around to the first row of a second interleaver. Stewart, 5:33-40. Modifying **Stewart** with **3GPP-Summary's** teachings of additional (or alternative) redundancy versions would have been a matter of adding additional steps already implemented in **Stewart**. Accordingly, a person of ordinary skill in the art would have found it straightforward to modify **Stewart** to use **3GPP-Summary's** teachings in order to

improve the performance of **Stewart's** system by using alternative different redundancy versions that can be selected to address wider range of channel conditions. Stewart, 1:57-64, 2:47-51; Ex. 1043, Abstract.

C. Ground 3: Stewart in View of TS25.212 (Claims 1-6)

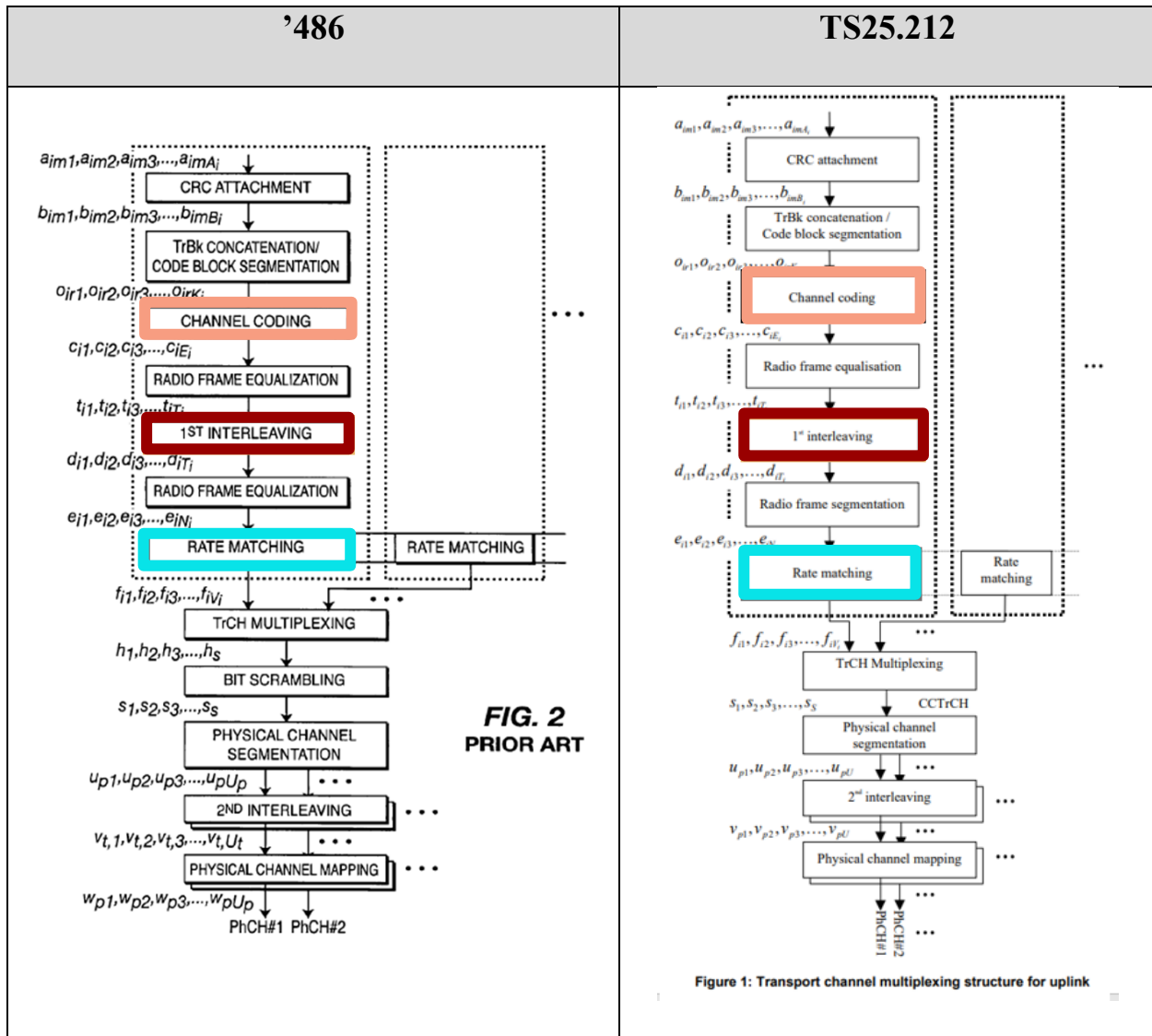
1. “buffer[ing]” ([3.d]/[1.d]/[5.d])

188. In addition to my discussion of **Stewart** in Ground 1, here, I explain why the teachings from **Stewart** in view of **TS25.212** render obvious each of the Challenged Claims. **TS25.212** (Ex. 1008) provides further detail of limitations recited in elements [3.d], [1.d], and [5.d] as required by Grounds 1-3: “buffering...the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream” (recited in [3.d]), “buffer” (recited in [1.d]), and “circuitry...configured to buffer” (recited in [5.d]). Thus, **Stewart** in view of **TS25.212** renders obvious claims 1-6.

189. Specifically, **TS25.212** teaches **buffering the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream** (e.g., a “virtual IR buffer” stores systematic bits, first parity bits and second parity bits). TS25.212, Fig. 17, §4.5.4.

190. **TS25.212** is a 3rd Generation Partnership Project (3GPP) Technical Specification whose scope is to “describe[...]...channel coding” as it relates to UTRA.

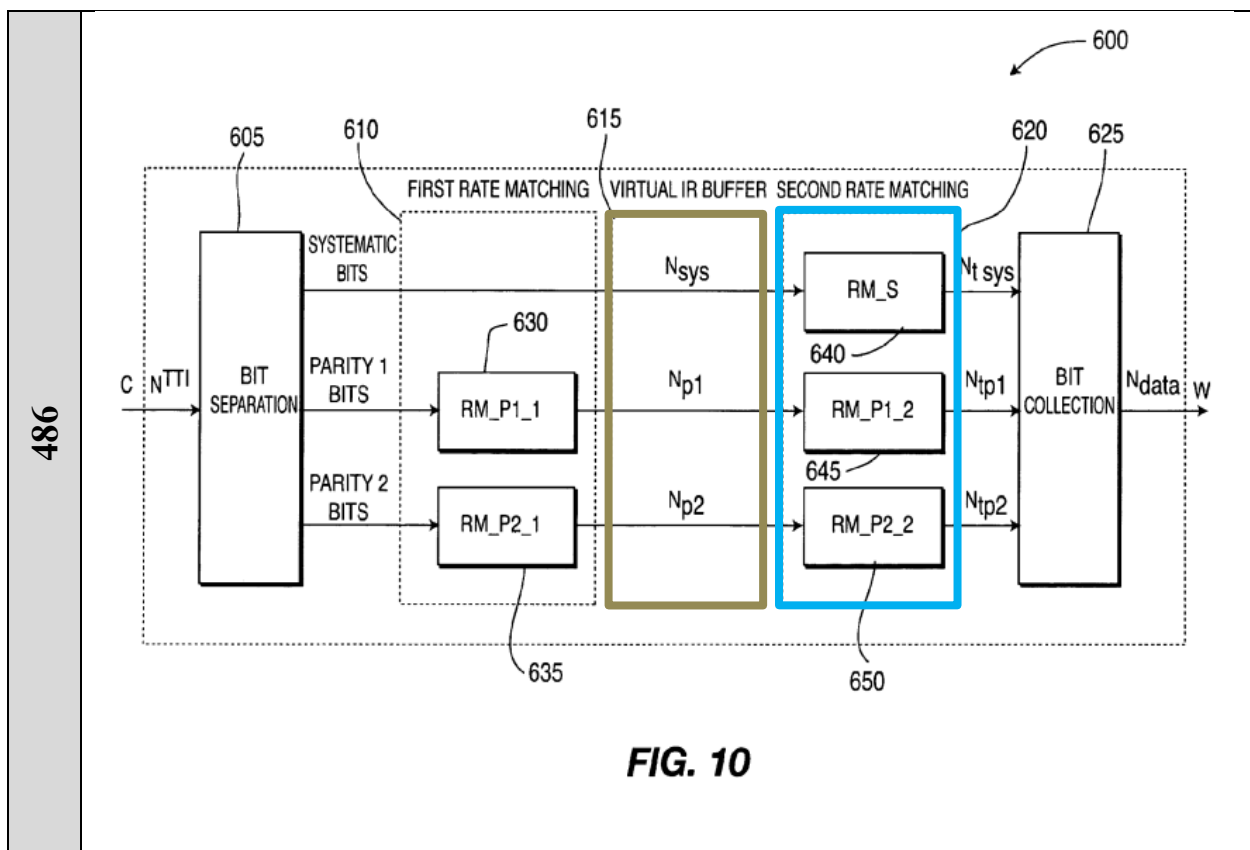
TS25.212, 7. Specifically, **TS25.212** teaches that a **channel coding** process is succeeded by an **interleaving** process and a **rate matching** process. TS25.212, Fig. 1. These processes, in this order, are also disclosed in the '486. '486, Fig. 2; *compare* '486, Fig. 2 *with* TS25.212, Fig. 1. Below, I incorporate a side-by-side color-coded comparison of Fig. 2 from the '486 and Fig. 1 from **TS25.212** to emphasize the similarity between the references. Other references also disclose the ordering of a channel coding, followed by interleaving, followed by a rate matching process. For example, U.S. Patent No. 6,671,851 ("Moulsley"), which I understand to have an effective filing date of 7/7/1999 teaches that "interleaving of data should be performed after coding, but before rate matching of the data stream (*i.e.* before puncturing or bit repetition)." Ex. 1044, 1:5-59. In addition, TS25.222 teaches that this order of processes is applied in both the uplink and downlink directions. TS25.222, Fig. 1.

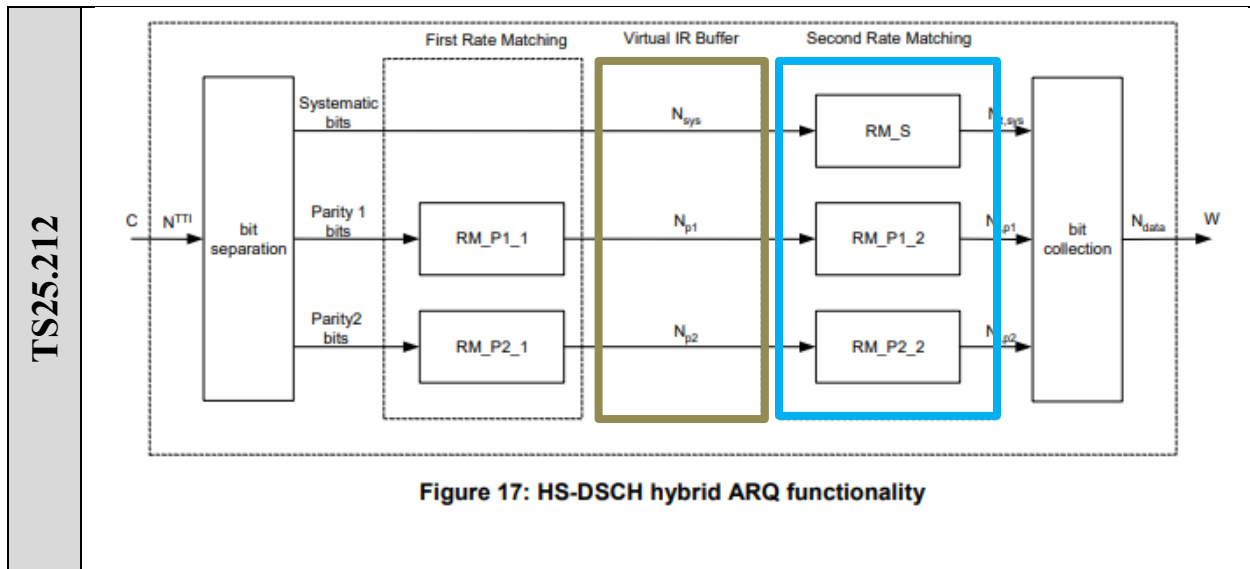


191. TS25.212 teaches that the **rate matching process** entails a “**virtual IR buffer**.” TS25.212, Fig. 17. This buffer is used to store bits prior to a “second rate matching” process. *Id.*; TS25.312, p. 58 (§4.5.4). The “Second Rate Matching” uses redundancy versions (RV) parameters “s” and “r.” TS25.212, p.59 (§4.5.4.3). TS25.212 teaches that when parameter “s” is set to “1,” the second rate matching process “prioriti[zes] systematic bits” over “non systematic bits” (e.g., parity bits);

when parameter “s” is set to “0,” the reverse is true and the second rate matching process “prioriti[z]es” “non systematic bits” (e.g., parity bits) over “systematic bits”

Id. TS25.212’s **virtual IR buffer** and **second rate matching** are depicted in Fig. 17. *Id.* These processes, in this order, are also disclosed in the ’486. ’486, Fig. 10; *compare* ’486, Fig. 10 *with* TS25.212, Fig. 17. Below I included a color-coded, side-by-side comparison of Fig. 10 from the ’486 and Fig. 17 from **TS25.212** to emphasize the similarity between the references.





192. A person of ordinary skill in the art would have understood that **TS25.212** and **Stewart** are in the same field as the '486, which includes improvements to coding schemes for wireless communications, and reasonably pertinent to the alleged problems identified in the '486, *e.g.*, of using redundancy versions to select coded bits for transmission between devices such as a user equipment and base station. *E.g.*, '486, Abstract; 4:53-5:13; Stewart, Abstract, 2:47-67, 9:60-10:3; TS25.212, Fig. 17, pp.58-59 (§§4.5.4, 4.5.4.3).

193. A person of ordinary skill in the art would at least have been motivated to modify **Stewart** to use **TS25.212's** teachings of a “virtual IR buffer” that stores bits for the reasons I discussed above pertaining to combining **Stewart** and **3GPP-Summary**. See Section IX.B (Ground 2: Stewart in View of 3GPP-Summary (Claims 1-6)). Moreover, **Stewart** makes references to (and incorporates by

reference) an earlier version (v3.5.0 from December 2000) of TS25.212 to explain channel coding, rate matching, incremental redundancy (IR), and interleavers. Stewart, 3:4-63, 4:34-5:5. Because TS25.212 is a technical specification, which seeks to standardize wireless communications protocols, it is not only understandable, but expected that a person of ordinary skill in the art, even prior to the earliest alleged priority date of the '486 patent (12/16/2002), would look to one of the later versions of the standards if working in the field of channel coding in wireless communication systems, which the **TS25.212** is generally directed to.⁸ Specifically, **TS25.212** teaches using a “virtual IR buffer” prior to a rate matching step that selects redundancy version parameters that “prioriti[ze]” either “systematic bits” or “non systematic bits” (e.g., parity bits) for transmission based on the selected redundancy version. TS25.212, Fig. 17, pp.58-59 (§§4.5.4, 4.5.4.3). Additionally, the inventors of **Stewart** had access to and evaluated Fig. 17 of from an earlier version of **TS25.212**, which was also publicly available on the 3GPP server and has substantially the same disclosures. *Compare* Ex. 1037, Fig. 1 with TS25.212, Fig. 17. (I understand that each specification is associated with a “version number” and

⁸ By referencing the 12/16/2002 alleged priority date, I do not offer any opinion as to whether the Challenged Claims are entitled to this priority date.

each version of a 3GPP TS document serves to add new disclosures in addition to what was already included in the previous version. 3GPP TS documents are uploaded to a public 3GPP server.) Additionally, as noted during the prosecution of a patent within the same patent family as the '486, *i.e.*, EP Patent Pub. No. 1573923A4, the aforementioned portion of **TS25.212** that included disclosure of a virtual IR buffer was copied into the '486 patent specification without attribution. *Compare* TS25.212 Fig. 17, §§4.5.4, 4.5.4.1-3 *with* '486 at Fig. 10, 16:17-26, 52-17:10, 18:15-19:13; *see* Ex. 1010.

194. Accordingly, a person of ordinary skill in the art would have had a reasonable expectation of success in modifying **Stewart** with **TS25.212**'s virtual IR buffer teachings store interleaved bits from **Stewart**'s System Block Interleaver and Parity Block Interleavers in a "virtual IR buffer" to because a buffer was a standard and well-known hardware component that temporarily "storing" bits that were to be transmitted in order to facilitate retransmissions as part of a HARQ process that **Stewart** is directed to. Ex. 1025, Ex. 1026, Ex. 1040, [0034]-[0037], [0045] ("HARQ retransmission buffer"), Ex. 1041, 4:1-7, 4:32-58, 11:48-57, 15:30-34; Dahlman-667, ¶[0034]. In the modified system, bits would be loaded from the interleavers into the virtual IR buffer. Bits are subsequently selected from the virtual IR buffer for transmission, based on a redundancy version parameter, for example

that is associated with selecting systematic bits over parity bits, or vice versa. A person of ordinary skill in the art would have found modifying **Stewart** with **TS25.212**'s teachings in such a way to have been a straightforward application of those teachings that would advantageously improve the latency and reliability of **Stewart**'s system because bits that are to be read out as part of HARQ retransmissions are buffered and easily accessible to be read out for retransmission.

2. “redundancy version[s]” ([3.e]/[1.e]/[5.e])

195. **TS25.212** provides additional teachings of limitations recited in elements [3.e], [1.e], [5.e] for Grounds 1-3: “at least one redundancy version of the set selects first and second parity bits over systematic bits” and “at least one redundancy version of the set selects systematic bits over first and second parity bits.” Thus, **Stewart** in view of **TS25.212** thus renders obvious claims 1-6.

196. Specifically, **TS25.212** teaches **selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits** (e.g., “RV parameter s” “distinguish[es] between transmissions that prioritize systematic bits (s=1) and non-systematic bits (S=0)).

197. **TS25.212** discloses selecting either systematic bits over parity bits and parity bits over systematic bits based on a redundancy version parameter, *s.* **TS25.212**, §4.5.4.3, Fig. 17. The '486 patent copied this disclosure to support the teachings of selecting systematic and parity bits based on redundancy versions. *See* Section VIII.B.1(c).

198. A person having ordinary skill in the art would have been motivated to modify **Stewart** to use **TS25.212**'s teachings to selectively prioritize systematic bits or parity bits based on a redundancy version for at least the reasons I provide above in Section IX.C.1 (analogous art).

199. Firstly, **Stewart** expressly references **TS25.212** for its discussions on rate matching. *See* Section IX.C.1 (motivation to combine). This would have further motivated a person of ordinary skill in the art to look to **TS25.212**'s teachings. *See* **Stewart**, 2:31-46; *see also* **Stewart**, cover page (listing "TS 25.212" in "OTHER PUBLICATIONS").

200. Secondly, a person having ordinary skill in the art would have understood that modifying **Stewart** with these **TS25.212** teachings is nothing more than applying known methods to achieve predictable results, and would have understood what these predictable results are. For example, **TS25.212** teaches a way of selecting systematic bits or parity bits for transmission "puncturing" (*i.e.*,

deleting) either the systematic bits or priority bits that are not intended to be transmitted. TS25.212, §4.5.4.3, Fig. 17. **Stewart**, too, teaches puncturing bits to achieve desired code rates while maintaining reliable communications. *See, e.g., Stewart*, 5:47-56. A person having ordinary skill in the art would have understood that modifying **Stewart** to use **TS25.212**'s teachings of prioritizing the section of systematic bits and parity bits provides a way of selecting code rates that complements **Stewart**'s approach, for example by puncturing systematic bits or parity bits to achieve a desired code rate.

201. For the reasons I provided above, a person having ordinary skill in the art would have had a reasonable expectation of success in modifying **Stewart**'s rate selection process with **TS25.212**'s teachings of selective prioritization.

D. Grounds 4-6: Grounds 1-3 in Further View of Motorola (Claims 1-6)

202. In addition to my discussions in Grounds 1-3, here, I explain why the teachings from **Stewart**, **3GPP-Summary** and **TS25.212** in view of **Motorola** render obvious each of the Challenged Claims. First, I will provide an overview of **Motorola**.

203. **Motorola** teaches further details of the following features each recited in elements [1.e], [3.e] and [5.e]: (1) “at least one redundancy version of the set selects first and second parity bits over systematic bits” that requires selecting first

and second parity bits before systematic bits are selected; (2) “at least one redundancy version of the set selects systematic bits over first and second parity bit” that requires selecting systematic bits before first and second parity bits are selected. For the reasons I will provide below, **Motorola** teaches **at least one redundancy version of the set that selects first and second parity bits over systematic bits** (*e.g.*, “RV5,” “RV6,” “RV7” (Fig. 5)) **and at least one redundancy version of the set that selects systematic bits over first and second parity bits** (*e.g.*, “RV0,” “RV1,” “RV2” (Fig. 5)). **Motorola**, §2.2(2.2), Figs. 4(4)-5(5). Because **Stewart** in view of **Motorola** discloses elements [1.e], [3.e], and [5.e], **Stewart** in view of **Motorola** renders obvious claims 1-6.

204. **Motorola**, titled “A New Hybrid-ARQ Scheme Using Incremental Redundancy,” is a proposal drafted and submitted by Motorola, Inc. to the 3rd Generation Partnership Project (“3GPP”) Radio Access Network Working Group 1 (“WG1”), which is the primary Standard Setting Organization (SSO) in the wireless communications space responsible for specifying and maintaining cellular telecommunication standards.

205. Like **Stewart**, **Motorola** is directed to an incremental redundancy (IR) scheme “based on block interleaving and symbol priority mapping.” **Motorola**, §1.0. Specifically, **Motorola** teaches receiving systematic, first parity, and second parity

bits streams and selecting between bits of these streams, based on a set of redundancy versions, to form a codeword to be transmitted. Motorola, §§2.1(2.1)-2.2(2.2). **Motorola** teaches that in order “to support different redundancy versions, any row may be assigned as a starting point” to commence reading out bits from a “**Systematic block interleaver**” or “**Parity block interleaver**.” Motorola, §§2.1(2.1)-2.2(2.2). **Motorola** teaches that “each redundancy version...contains a starting row...in either the ‘Systematic’ or ‘Parity’ interleaver” that indicates the row within the interleaver from where the reading out of the bits commences. Motorola, §2.2(2.2). For example, **Motorola** illustrates the redundancy versions in Fig. 5(5) (color-coded, below). The redundancy versions outlined in **brown** (e.g., “RV5,” “RV6,” “RV7”) have a **starting row** in one of the **Parity Block Interleavers** such that the reading begins with the first and second parity bits. Motorola, Fig. 5(5). The redundancy versions outlined in **lime green** (e.g., “RV5,” “RV6,” “RV7”) have a **starting row** is in the **Systematic Block Interleaver** such that the reading begins with the systematic bits. Motorola, Fig. 5(5).

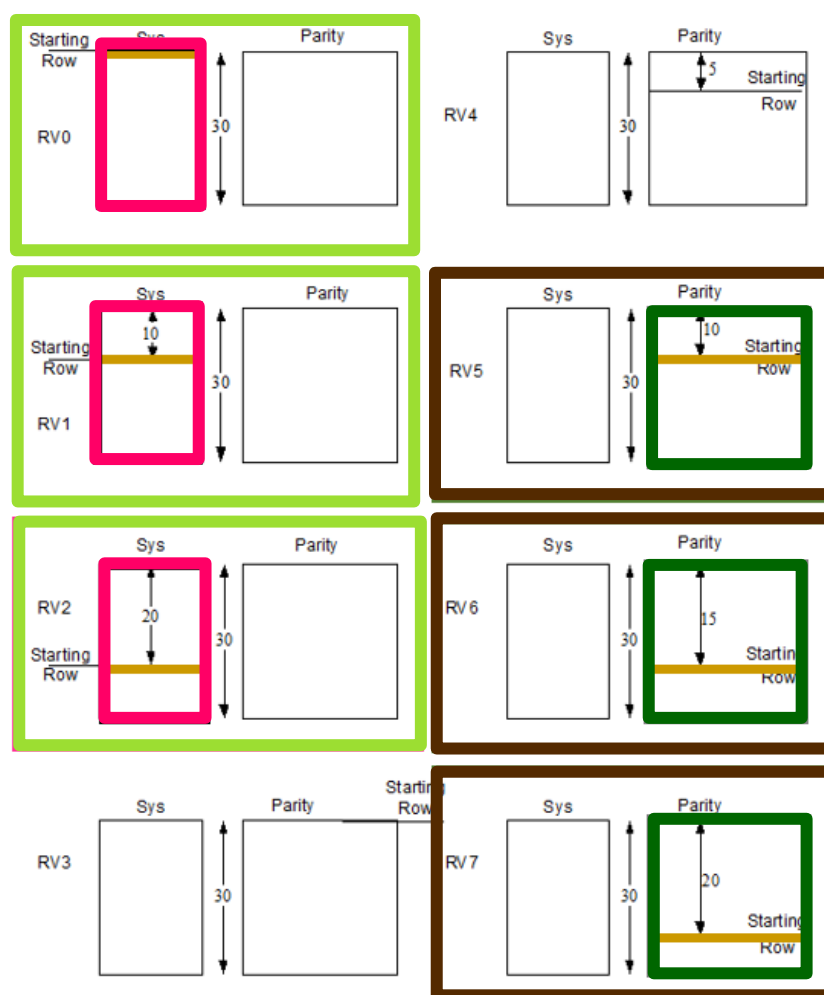


Figure 5 Redundancy versions for rate 1/3

206. **Motorola** also teaches that the “[c]oded bits are read from the selected starting row until either the desired number of bits has been read or the end of the $N_{i,\text{max_row}}$ th row is reached.” **Motorola**, §2.2(2.2). Additionally, **Motorola** teaches that if “the end of the $N_{i,\text{max_row}}$ th row is reached, reading then continues from the first row of the other interleaver.” *Id.* Below is a color-coded version of **Motorola’s** Fig. 4 that illustrates the “[r]edundancy version wrap around” procedure that embodies the above teachings from **Motorola**. In the examples illustrated in Fig. 4, reading

starts at the **starting row** located in one block interleaver and continues to the last row (the N_{i,max_row} th row); because, the desired number of code bits has not been read, the “**reading [] continues [to] the first row of the other interleaver.**” Motorola, Fig. 4(4), §§2.1(2.1), 2.2(2.2).

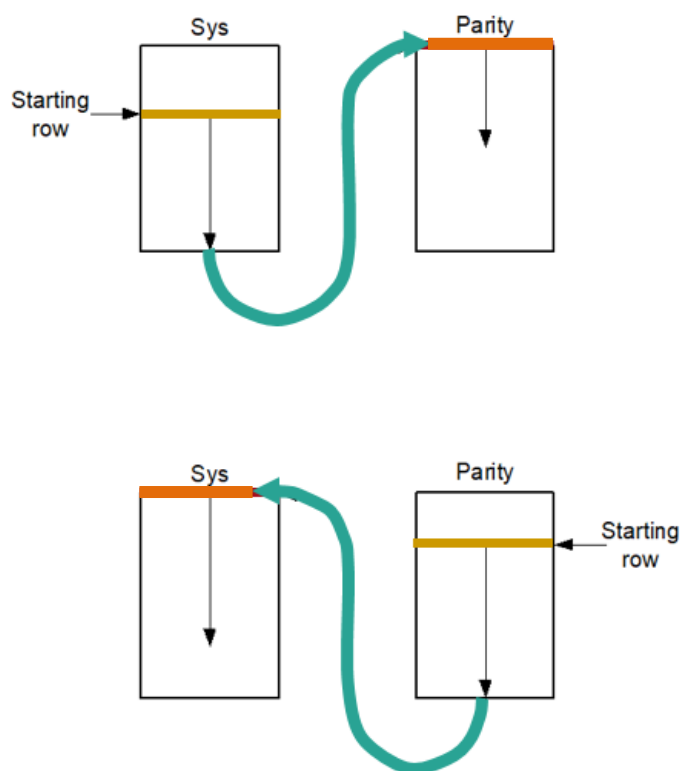


Figure 4 - Redundancy version wrap around

207. The example from the bottom of **Motorola’s** Fig. 4 teaches a subset of redundancy versions for which the starting row is in the “Parity Block Interleaver,” and bits are read starting from the “Parity Block Interleaver” through the last row of the “Parity Block Interleaver” and then continuing on to the first row of the “Systematic Block Interleaver.” When applied to **Stewart’s** disclosures of a first

parity block interleaver and a second parity block interleaver, if the desired number of codeword bits has been not reached after reading from the starting row of the first parity block interleaver through the last row of the first parity block interleaver, the reading would proceed through the rows of the second parity block interleaver, and then through the rows of the systematic block interleaver as needed. Thus, **Motorola** teaches a redundancy version that selects “first and second parity bits” (from a **starting row** of **Motorola’s** Parity Block Interleaver) “over systematic bits” (continuing into **Motorola’s** System Block Interleaver). **Motorola**, §§2.1(2.1)-2.2(2.2), Figs. 4(4), 5(5).

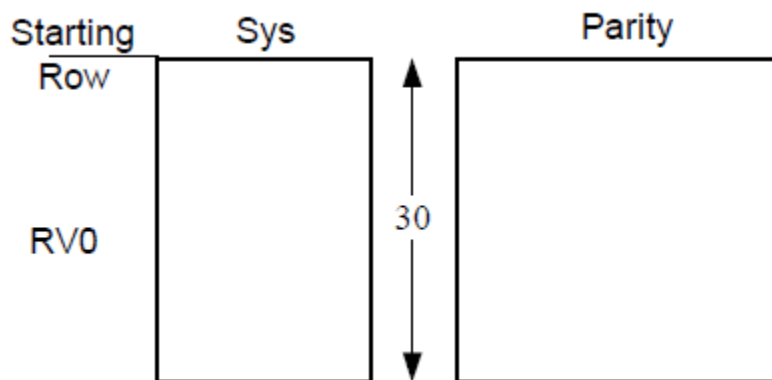
208. **Motorola’s** also teaches the reverse: a subset of redundancy versions for which the starting row is in the “Systematic Block Interleaver,” and bits are read starting from the “Systematic Block Interleaver” and then continuing into the first and second parity block interleavers.” For example, in the case of a **starting row** located in a systematic block interleaver, if the desired number of codeword bits is not yet reached after reading bits from the **starting row** to the last row of the systematic block interleaver, reading would wrap around to the first row of a first parity block interleaver, and then to a second parity block interleaver as needed to read out the desired number of codeword bits. **Motorola**, Figs. 4(4)-5(5), §§2.1(2.1), 2.2(2.2). Thus, **Motorola** also teaches a redundancy version that selects

“systematic bits” (from a **starting row** of **Motorola’s** Systematic Block Interleaver) “over first and second parity bits” (continuing into **Motorola’s** Parity Block Interleaver). Motorola, §§2.1(2.1)-2.2(2.2), Figs. 4(4), 5(5).

209. To the extent the limitation recited in elements [3.e], [1.e], [5.e], “at least one redundancy version of the set selects first and second parity bits over systematic bits,” requires selecting more parity bits for transmission than systematic bits, **Motorola** discloses this limitation, and thus discloses claims 1-6. And to the extent the limitation, recited in elements [3.e], [1.e], [5.e], “at least one redundancy version of the set selects systematic bits over first and second parity bits,” requires selecting a more systematic bits for transmission than parity bits selected for transmission, **Motorola** discloses this limitation, and thus discloses claims 1-6. For example, **Motorola** discloses at least one redundancy version of the set of redundancy versions that selects first and second parity bits over systematic bits (*e.g.*, “RV₅” signaled with a 1/4 code rate). **Motorola** also discloses least one redundancy version of the set of redundancy versions that selects systematic bits over first and second parity bits (*e.g.*, “RV₀” signaled with a 3/5 code rate). Motorola, §2.2(2.2), Figs. 4(4)-5(5).

210. Take for example **Motorola’s** redundancy version “RV₀,” which **Motorola** teaches is “signaled with enough codeword bits to result in a rate 3/5

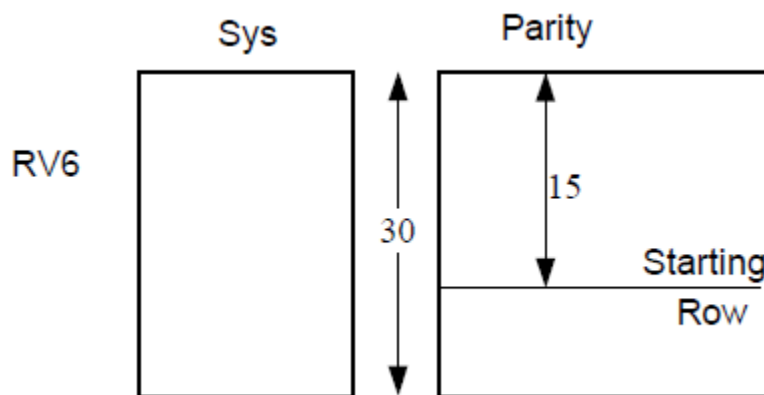
code” so that what gets transmitted is “all systematic bits and first 10 rows of parity interleaver [are] transmitted.” Motorola, 6(6). For this specific example, I provide several reasonable assumptions to illustrate my point. Firstly, assume that for each redundancy version, the same number of bits is selected for transmission with each redundancy version. Secondly, assume that the total number of columns in the systematic block interleaver is 100 per each row of the interleaver and that each column/row position stores a bit. Thirdly, assume that the total number of columns in the parity block interleaver is 200 per each row of the interleaver and that each column /row position stores a bit. Fourthly, assume that no dummy bits are added to the sequence (which is sometimes done in a conventional process called “padding”). Provided below is an excerpt of Fig.5 showing RV₀.



211. In the case of block interleavers having 30 rows (as shown in Fig. 5), and in the specific case of redundancy version “RV₀,” the total number of systematic bits for transmission is 3,000 (the number of rows in the systematic interleaver, 30,

multiplied by the number of columns in the systematic interleaver, 100) and the total number of parity bits for transmission is 2,000 (the remaining number of rows in the parity block interleaver, 10, multiplied by the number of columns in the parity block interleaver, 200). Thus, in the specific case of **Motorola's** redundancy version "RV₀," more systematic bits are selected for transmission than parity bits. Because **Motorola's** Fig. 5 dictates that reading for redundancy version "RV₀" starts in the systematic block interleaver, the 3,000 systematic bits are transmitted before the 2,000 parity bits are. Motorola, Fig. 5(5), §§2.1(2.1)-2.2(2.2).

212. Take as another example **Motorola's** redundancy version "RV₆," depicted below is an excerpt of Fig. 5.



213. In the case of block interleavers having 30 rows as illustrated by Fig. 5, and the specific case of **Motorola's** redundancy version "RV₆," when the same four assumptions I listed above are applied: the total number of parity bits selected for transmission is larger than the total number of systematic bits selected for

transmission. (The total number of parity bits selected for transmission (3,000) is calculated by multiplying the number of rows in the parity block interleaver that are read out following the starting point, 15, by the number of columns in the same interleaver, 200). This number is larger than the total number of systematic bits selected for transmission ((2,000) calculated by multiplying the number of rows in the systematic block interleaver that needs to be read to get to the total number of transmitted bits, 20, by the number of columns in the systematic block interleaver, 100). Motorola, 7(7); Fig. 5(5). Because **Motorola's** Fig. 5 dictates that reading for redundancy version "RV₆" starts in the parity block interleaver, the 3,000 parity bits are transmitted before the 2,000 systematic bits are. Motorola, Fig. 5(5), §§2.1(2.1)-2.2(2.2).

214. **Motorola**, like **Stewart**, **3GPP-Summary**, and **TS25.212**, is analogous art and in the same field as the '486 patent (*e.g.*, improvements to coding schemes for wireless communications) and reasonably pertinent to the alleged problems identified in the '486 patent (*e.g.*, using redundancy versions to implement an incremental redundancy process for transmitting information between a user device and base station). *E.g.*, '486, Abstract; 4:53-5:13; Stewart, Abstract, 2:47-67; Motorola, §§1.0(1.0), 2.2(2.2).

215. A person of ordinary skill in the art would have been motivated to modify **Stewart** alone, or in view of **3-GPP Summary** and/or **TS25.212**, with **Motorola's** teachings of redundancy versions and their respective starting rows for reading bits to **Stewart**. For example, a person of ordinary skill in the art would have understood that **Motorola's** implementations of redundancy versions are alternatives to those in **Stewart**, having different advantages for a Hybrid Automatic Repeat reQuest ("HARQ") process that entails retransmitting transmissions that were unsuccessfully received by a receiving device. **Stewart**, 1:57-2:2, 2:45-49; **Motorola**, §§1.0(1.0), 2.0(2.0). As I discussed above, **Stewart** discloses that its scheme entails using a plurality of redundancy versions, a subset of which entail reading coded bits from a first interleaver and, if the desired number of coded bits has not yet been read out, continuing to read from the first row of a second interleaver. **Stewart**, 5:34-40. **Stewart's** redundancy versions vary starting rows in increments of $\frac{1}{4}$ of the total number of runs as shown in Fig. 6 below.

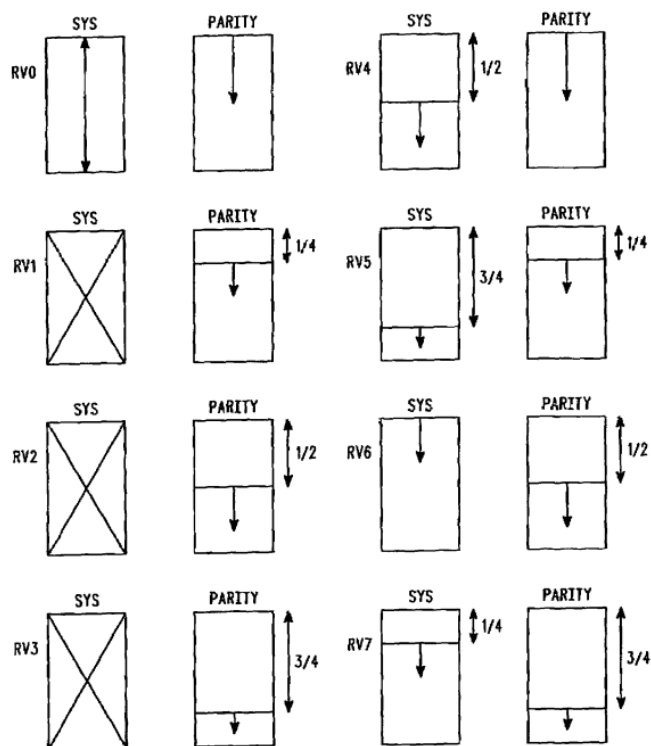
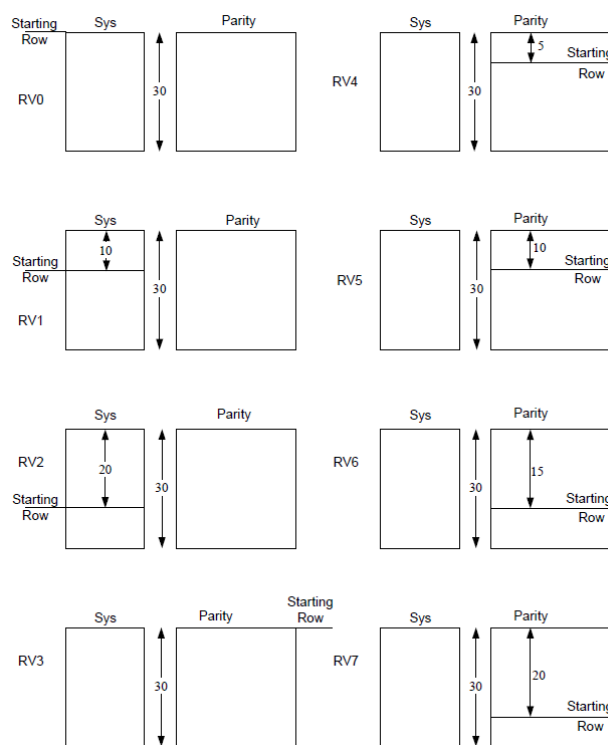


FIG. 6

On the other hand, **Motorola** provides redundancy versions that vary starting rows in increments of $1/3$ of total rows (e.g., 10/30 rows, 20/30 rows, etc.) as shown in Fig. 5 below.



A person of ordinary skill in the art thus would have been motivated to modify **Stewart's** teaching to include one or more of **Motorola's** redundancy versions to obtain additional granularity in starting rows of the interleavers. For example, as shown above, **Stewart** teaches that the starting rows in an interleaver can vary by increments of $1/4$, $1/2$, and $3/4$ (*see Stewart, Fig. 6*), whereas **Motorola** teaches that the start rows in an interleaver can vary by increment of $1/3$ and $2/3$ (*see Motorola, Fig. 5(5)*). Modifying **Stewart's** teachings with **Motorola** would yield a scheme where the starting row for reading bits is $1/4$ th, $1/2$ th, and $3/4$ th in addition to $1/3$ th and/or $2/3$ th of the way down in **Stewart's** Systematic Block Interleaver, First Parity

Bit Interleaver, and Second Parity Bit Interleaver, and wraps around to a second interleaver.

216. In **Stewart**, different redundancy versions are used to support incremental redundancy (IR), which is a type of HARQ procedure that entails a user device being requested to retransmit or transmit additional bits to a base station if the base station did not successfully receive and decode the original transmission. Stewart, 1:57-64, 2:47-51; Ex. 1043, Abstract. There are various scenarios that would cause a base station to not be able to properly receive a transmission; one such case is if the channel in which the transmission is sent is noisy. If a base station receives many transmissions successfully, it suggests the channel conditions are good. To ensure a higher chance that a transmission is successfully received, transmissions may benefit from a varying ratio and ordering of systematic and parity bits. Accordingly, the channel conditions and amount of prior transmissions successfully received by the base station dictate the combination and ordering of systematic bits and parity bits that is desirable to carry out future transmissions. Stewart, 2:47-49, 2:59-64, 3:25-40, 7:44-62, 8:15-18; Ex. 1043, 1830, 1833. For example, if a prior transmission consisted of only systematic bits, the recipient would benefit from receiving a retransmission consisting of only parity bits. Stewart, 8:15-18; Ex. 1043, 1830, 1833. Alternatively, if a portion of systematic bits in the prior

transmission was distorted by the channel due to poor channel conditions, the recipient would benefit from receiving a retransmission consisting of a combination of systematic bits and parity bits, where the systematic bits are sent before the parity bits. As another alternative, the recipient would benefit if the ordering of the bits were “revers[ed]” such that parity bits were transmitted first, followed by systematic bits. Motorola, §2.3(2.3); Stewart, 8:15-30, Fig. 7.

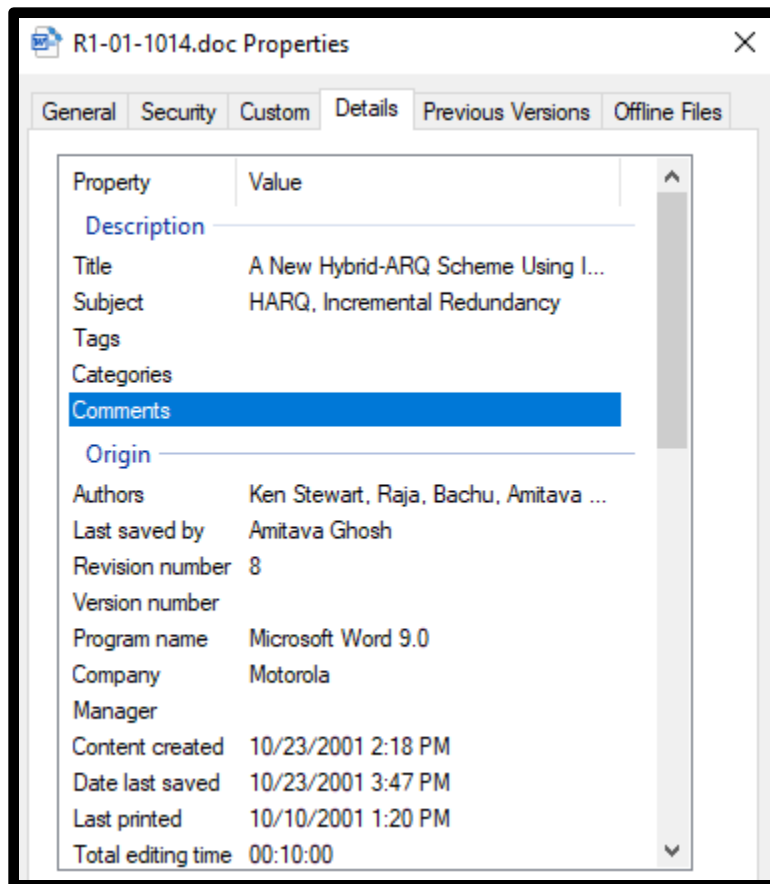
217. Moreover, a person of ordinary skill in the art would understand that different numbers of redundancy versions are included in the set of redundancy versions, and this depends on the number of signaling bits required to indicate a specific redundancy version that the transmitting device is to use. 3GPP-Summary, §3.2. The set of redundancy versions is defined and signaled between the user device and the base station. *See* Stewart, 6:3-9. A set of 2 redundancy versions requires 1-bit for signaling, whereas a set of 4 redundancy versions requires 2-bit signaling, and a set of 8 redundancy versions requires 3-bit signaling. *Id.*

218. In view of the aforementioned benefits of having various alternative redundancy versions, a person of ordinary skill in the art would have been motivated to modify **Stewart** to use **Motorola’s** teachings of different combinations of redundancy version implementations. These benefits being: (1) to obtain additional granularity in starting rows of the interleavers; and (2) having additional (or

alternative) redundancy versions leads to more available combinations and orderings of systematic and parity bits to improve **Stewart's** incremental redundancy (IR) and HARQ procedures. One non-limiting example is: a person of ordinary skill in the art would have been motivated to modify **Stewart's** set of redundancy versions that include a redundancy version that transmits systematic bits followed by first and second parity bits (*e.g.*, “RV₀”) to include **Motorola's** set of redundancy versions that set a starting row in a parity block interleaver, *e.g.*, redundancy versions “RV₅,” “RV₆,” and “RV₇,” where first and second parity bits are transmitted followed by systematic bits. Motorola, §§2.2(2.2)-2.3(2.3), Figs. 4(4)-5(5); Stewart, 6:57-61.

219. Additionally, a person of ordinary skill in the art would have been motivated to modify **Stewart** to use **Motorola's** teachings because of how similar the teachings are and that **Motorola's** authors were also the inventors of **Stewart**. Motorola, §2.2(2.2), Figs. 4(4)-5(5); Stewart, 5:29-40, 5:57-7:24, Fig. 6. *Firstly*, the teachings of **Motorola** and **Stewart** are substantially similar: both references teach an incremental redundancy (IR) scheme that selects between interleaved systematic bits and interleaved parity bits for transmission between wireless communications devices such as user equipment and a base station. Motorola, §§1.0(1.0), 2.0(2.0), 2.2(2.2), 2.3(2.3), Figs. 1(1), 4(4), 5(5), 6(6); Stewart, 3:47-4:13, 5:29-8:36, Figs. 2, 3, 6, 7. The references share multiple figures. *Compare* Motorola, Fig. 1(1) with

Stewart, Figs. 2-3; *compare* Motorola, Fig. 2(2) *with* Stewart, Fig. 4; *compare* Motorola, Fig. 3(3) *with* Stewart, Fig. 5. **Secondly, Motorola's** authors, which are not listed on the face of the reference but can be deduced from the document's metadata, are the named inventors of **Stewart**. Ex. 1045. As shown the below, the authors include Ken Stewart, Raja Bachu, Amitava Ghosh, Ratasuk Rapeepat, and Michael Eoin Buckley, who are the same as the inventors of **Stewart**.



220. For at least the reasons I provided above, a person of ordinary skill in the art would also have had a reasonable expectation of success in modifying **Stewart** alone, or in view of **3GPP-Summary** and/or **TS25.212** with **Motorola's**

teachings to include the combinations of redundancy versions from **Stewart, 3GPP-Summary, TS25.212** and/or **Motorola** in **Stewart's** system. Firstly, owing to the similarities in the teachings (as described above), a person of ordinary skill in the art would have found it straightforward to apply **Motorola's** teaching of redundancy versions. Secondly, alternative redundancy versions that produced different combinations and ordering of systematic bits and parity bits and the inherent advantages of using one combination and/or ordering during a particular channel condition was well known. 3GPP-Summary, §§2.1-2.6. For example, Ericsson proposed two different redundancy versions, one having “all the systematic bits” and “some parity bits” and the other having “parity bits only.” 3GPP-Summary, §2.1; (Ex. R1-01-1045), §2. Texas Instruments proposed three redundancy versions: one version with systematic and parity bits and two with primarily parity bits in differing amounts. 3GPP-Summary, §2.2; (Ex. R1-01-1026), §§3.3.1-3.3.2, Tables 2-3. Siemens proposed multiple redundancy versions, each having all systematic bits with varying parity bits. 3GPP-Summary, §2.3; (Ex. R1-01-1028), §2. Nokia proposed multiple redundancy versions, some having systematic bits and parity bits, and some having parity bits only. 3GPP-Summary, §2.5; (Ex. R1-01-1023), §§2.1, 3.1. OKI proposed four different redundancy versions having different ordering of systematic bits, first and second parity bits (*e.g.*, (S, P1, P2), (P1, P2, S), (P1, S, P2),

and (S, P2, P1)). 3GPP-Summary, §2.6; (Ex. R1-01-1070), §2.1. Accordingly, a person of ordinary skill in the art would have recognized that different redundancy versions existed that could produce different combinations and ordering of parity and systematic bits as well as different increments for starting rows in interleavers from which to select bits for transmission. Moreover, a person of ordinary skill in the art would have recognized that using a particular redundancy version when certain channel conditions are met can result in performance benefits that motivate the implementation of such a system for retransmission of bits from a user device to a base station as part of an overall HARQ, specifically IR, scheme.

X. SECONDARY CONSIDERATIONS

221. I have seen no evidence in the '486 patent's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any Challenged Claim. *See generally* Ex. 1002. Indeed, per my discussion of the prior art referenced herein, any purported solutions to problems or unexpected results in the '486 were already well known. To the extent Pantech asserts the existence of any secondary considerations in its responses, I reserve my right to address any such evidence.

XI. CONCLUSION

222. In summary, I have concluded that the Challenged Claims of the '486 are disclosed and/or rendered obvious over the prior art references I have discussed in this declaration. Specifically, it is my opinion that for at least the reasons above, the Challenged Claims are disclosed and/or rendered obvious as follows:

Ground	Basis	Claims	References
1	§102, §103	1-6	Stewart
2	§103		Stewart in view of 3GPP-Summary
3			Stewart in view of TS25.212
4			Stewart in view of Motorola
5			Stewart in view of 3GPP-Summary and Motorola
6			Stewart in view of TS25.212 and Motorola

223. To the extent it is argued that any further disclosure is required for an element in the Challenged Claims that I have identified as being disclosed, a person of ordinary skill in the art would certainly have found that element obvious to include based on the sample explicit disclosure or inherent disclosures and analysis I have identified above.

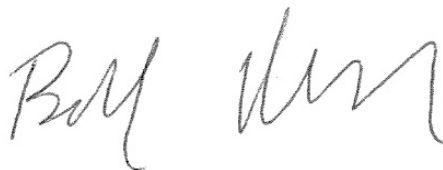
224. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner or its expert(s) may raise and to take into account new information as it becomes available to me.

225. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

226. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 10th day of August 2023, in South Bend, Indiana

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Bertrand Hochwald", written in a cursive style.

Dr. Bertrand Hochwald

Appendix A

Bertrand M. Hochwald

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Home:
1329 E. Jefferson Blvd
South Bend, IN 46617
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Degrees:

BS (Engineering) 1984, Swarthmore College
MS (Electrical Engineering) 1986, Duke University
MA (Statistics) 1993, Yale University
PhD (Electrical Engineering) 1995, Yale University

Experience:

Department of Defense, Fort Meade, Maryland. *Electrical Engineer*, 1986–1989.
Yale University, New Haven, Connecticut. *Teaching assistant*, 1990–1994.
University of Illinois, Urbana-Champaign
Postdoctoral Research Associate in data compression, 1995.
Visiting Faculty in Department of Electrical Engineering, 1996.
Bell Laboratories, Lucent Technologies, Murray Hill, New Jersey
Member of Technical Staff, 1996–2002.
Distinguished Member of Technical Staff, 2002–2005.
Columbia University, New York
Visiting Faculty in Department of Electrical Engineering, 2005.
Beceem Communications, Santa Clara, California
Chief Scientist, 2005–2009,
Vice-President Systems Engineering, 2009–2010.
Stanford University, Palo Alto, California
Consulting Professor of Electrical Engineering, 2006–2010.
University of Notre Dame, Notre Dame, Indiana
Frank M. Freimann Professor of Electrical Engineering, 2011–present.
University of Notre Dame, Notre Dame, Indiana
Co-Director of The Wireless Institute, 2016–present.

Honors:

New York State: *Regents Scholarship*, 1980.
Pennsylvania ACM computer programming competition: *Winner*, 1983.
Duke University: *Eta Kappa Nu engineering honor society*, 1985.
Department of Defense: *Special Achievement Awards*, 1988, 1989.
Yale University: *Prize Teaching Fellowship teaching award*, 1993.
Bell Laboratories: *President's Gold Award*, 2002.
Thomson Essential Science Indicators
Top one-tenth of one percent referenced papers, 2002 and 2003.
IEEE Transactions on Communications
Stephen O. Rice Best Paper Award, 2006.
IEEE
Fellow, 2008.
Thomson Reuters
World's Most Influential Scientific Minds, multiple years.

Honors (cont'd):

IEEE Transactions on Circuits and Systems
Young Author Best Paper Award, 2016 (my PhD student).
IEEE Transactions on Antennas and Propagation
H. A. Wheeler Prize Paper Award, 2018.
The Marconi Society
Paul Baran Young Scholar Award, 2018 (my PhD student).
National Academy of Inventors
Fellow, 2019.

Research Gifts, Grants and Contracts:

Principal Investigator, “NSF EAGER: Multiple Transmitter Chains to Minimize Exposure to Electromagnetic Radiation in Portable Devices,” National Science Foundation CCF-1141868, August 1, 2011–July 31, 2013, \$200,000.
Co-Principal Investigator, “Planning Grant: I/UCRC in Broadband Wireless Technologies and Applications,” National Science Foundation IIP-1266124, April 1, 2013–March 31, 2014, \$14,544.
Co-Principal Investigator, “I/UCRC Phase I: BWAC@NDWI: Broadband Wireless Access and Applications at the Notre Dame Wireless Institute,” National Science Foundation, IIP-1439682, August 1, 2014–July 31, 2019, \$325,000.
Principal Investigator, “Modeling, Analysis, and Code Design for Portable Wireless Transmitters Subject to an Electromagnetic Exposure Constraint,” National Science Foundation, CCF-1403458, September 1, 2014–August 31, 2018, \$1,200,000.
Principal Investigator, “Notre Dame Millimeter-Band Capability,” Equipment Restoration and Renewal Grant, May 31, 2015–May 31, 2016, \$183,000.
Principal Investigator, “Channel Estimation Technologies based on AoA/AoD in High-Frequency Wireless Communication Systems,” Huawei Technologies, June 22, 2015–October 31, 2016, \$181,217.
Principal Investigator, “*Radiohound*: A Low-Cost Spectrum Beacon/Sensor with Millimeter Wave Capability,” Alcatel-Lucent and Interdigital Corporations, June 1, 2015–May 31, 2018, \$240,000.
Principal Investigator, “Low-Complexity High-Bandwidth Multiport Matching Networks for Coupled Loads,” National Science Foundation, ECCS-1509188, August 1, 2015–July 31, 2018, \$400,000.
Principal Investigator, “Notre Dame Coherent RadioHound: A Distributed Spectrum Sensor Network,” Laboratory for Telecommunications Sciences, May 6, 2016–May 5, 2017, \$187,124.
Co-Principal Investigator, “Wideband Time-Domain Millimeter-Wave Device and Channel Characterization Testbed,” Department of the Navy, July 15, 2016–July 14, 2017, \$326,573.
Principal Investigator, “SpecEES: Wideband Wireless Communications with Low-Power Transceiver-Cell Circuits,” National Science Foundation, ECCS-1731056, August 15, 2017–August 14, 2020, \$650,000.
Principal Investigator, “Data Gathering Plan for Radio-Frequency Machine-Learning Systems,” Defense Advanced Research Projects Agency, October 1, 2017–June 1, 2018, \$149,332.
Principal Investigator, “REU Site: AWaRE Advanced Wireless Research Experiences at the University of Notre Dame,” National Science Foundation CNS-1757804, January 15, 2018–December 31, 2020, \$359,789.
Co-Principal Investigator, “Physical Layer Signature Discrimination of Transmitters,” The George J Kostas Research Institute for Homeland Security at Northeastern University (KRI), March 30, 2018–October 29, 2020, \$100,000.

Research Gifts, Grants and Contracts (cont'd):

Co-Principal Investigator, "An Infrastructure-less and Heterogeneous Distributed Sensor for Electromagnetic Spectrum Sensing and Emitter Geolocation," Department of the Army, June 15, 2018–June 14, 2019, \$370,234.

Co-Principal Investigator, "Improving STEM Retention Through Hands-On Implementation and Red-Teaming," Office of Naval Research, August 15, 2018–August 14, 2021, \$735,830.

Principal Investigator, "Ultra Low Cost/Power Massive MIMO Architecture and Algorithm," Futurewei Technologies, Inc, Gift, September 13, 2018, \$200,000.

Principal Investigator, "Ultra Low-Cost Low-Power Millimeter-Wave Transceiver," AT&T Innovation Lab, September 15, 2018–September 14, 2020, \$220,000.

Principal Investigator, "MLWiNS: Quality Versus Quantity in Spectrum Sensing with Distributed Sensors," National Science Foundation jointly with Intel Corporation, July 1, 2020–June 30, 2023, \$665,000.

Principal Investigator, "Low-Cost Low-Power Millimeter-Wave Transceiver," AT&T Innovation Lab, January 1, 2021–December 31, 2021, \$110,000.

Co-Principal Investigator, "Stationary and Aerial-Based RF/Radar Detection of Drones, Concealed Threats and Anomalous Communications," Department of Homeland Security, October 1, 2021–September 30, 2031, \$1,000,000.

Senior Personnel, "SpectrumX - An NSF Spectrum Innovation Center," National Science Foundation, September 15, 2021–September 14, 2026, \$25,000,000.

Co-Principal Investigator, "Self-Powered Wireless Sensor System for Health Monitoring of Liquid-Sodium Cooled Fast Reactors," Department of Energy, October 1, 2021–September 30, 2024, \$640,000.

Principal Investigator, "Ultra Low-Cost Low-Power Millimeter-Wave Transceiver," AT&T Innovation Lab, January 1, 2022–December 31, 2022, \$110,000.

Patents:

- “Multiple Antenna Communication System and Method Thereof,” #6058105, May 2, 2000.
- “Wireless Transmission Method for Antenna Arrays, Having Improved Resistance to Fading,” #6327310, December 4, 2001.
- “Antenna Array Having Reduced Sensitivity to Frequency-Shift Effects,” #6349219, February 19, 2002.
- “Wireless Transmission Method for Antenna Arrays Using Unitary Space-Time Signals,” #6363121, March 26, 2002.
- “Space-Time Spreading Method of CDMA Wireless Communication,” #6452916, September 17, 2002.
- “Method of Wireless Communication Using Structured Unitary Space-Time Signal Constellations,” #6693976, February 17, 2004.
- “Method for Wireless Differential Communication Using Multiple Transmitter Antennas,” #6724842, April 20, 2004.
- “Method for Wireless Communication using Unitary Space-Time Signal Constellations,” #6801579, October 5, 2004.
- “Method of Multiple-Antenna Wireless Communication Using Space-Time Codes,” #6944236, September 13, 2005.
- “Cayley-Encoding of Unitary Matrices for Differential Communication,” #7170954, January 30, 2007.
- “Method and Apparatus for Detection and Decoding of Signals Received from a Linear Propagation Channel,” #7236536, June 26, 2007.
- “Method of Signal Transmission to Multiple Users From a Multi-Element Array,” #7317764, January 08, 2008.
- “Downlink Coordinated Transmission in OFDMA Systems,” #7706335, April 27, 2010.
- “Downlink Coordinated Transmission in OFDMA Systems, Including WiMax Systems,” #7764658, July 27, 2010.
- “Spherical Decoder for Wireless Communications,” #7822150, October 26, 2010.
- “Method for Estimating Frequency Offset at a Subscriber Station Receiver in a Multi-Carrier System,” #7916800, March 29, 2011.
- “Estimating Frequency Offset at a Subscriber Station Receiver,” #7929595, April 19, 2011.
- “Method of a Receiver Estimating a Plurality of Channels,” #8194774, June 5, 2012.
- “Method of Aiding Uplink Beamforming Transmission,” #8259672, September 4, 2012.
- “Multi-Stream Priority-Based Space-Time Coding,” #8284693, October 9, 2012.
- “Estimating a Subscriber Location,” #8290508, October 16, 2012.
- “Selecting a Transmission Mode Between a Subscriber and a Base Station,” #8311003, November 13, 2012.
- “Noninvasive Characterization of Electrical Power Distribution Systems,” #8427169, April 23, 2013.
- “Method and System of Beamforming a Broadband Signal Through a Multiport Network,” #8432997, April 30, 2013.
- “Estimating a Subscriber Location,” #8611925, December 17, 2013.
- “Characterization of Electrical Power Distribution Systems,” #8633705, January 21, 2014.
- “Allocating Antennas for Cyclic Delay Diversity,” #8675761, March 18, 2014.
- “Wireless Transceivers with Filter Arrangement for WiFi and WiMax coexistence,” #8681748, March 25, 2014.
- “Multiple Antenna Signal Transmission,” #8737529, May 27, 2014.
- “Selecting a Transmission Mode Between a Subscriber and a Base Station,” #8750236, June 10, 2014.
- “Multiple Antenna Transceiver,” #8761694, June 24, 2014.

Patents (cont'd):

- “Characterization of Electrical Power Distribution Systems Using Characterization Matrices,” #8810253, August 19, 2014.
- “Method and System of Beamforming a Broadband Signal Through a Multiport Network,” #8811530, August 19, 2014.
- “Distribution of Transmit Signal to Multiple Transmit Antennas for Reduction, of Measured Specific Absorption Rate,” #8811918, August 19, 2014.
- “Method of Transmission from Multiple Transmit Chains Based on a Cost Function” for Electromagnetic Radiation,” #8818294, August 26, 2014.
- “Method and System for Uplink Coordinated Reception in Orthogonal Frequency Division Multiple Access Systems,” #8855046, October 7, 2014.
- “Method of Coding Using Multiple Transmit Chains for Reduced Exposure to Electromagnetic Radiation,” #8929828, January 6, 2015.
- “Method and Apparatus for Link Adaptation in a Wireless Communication Network,” #8942184, January 27, 2015.
- “Method and Apparatus for Managing Uplink Communication in Wireless Network,” #9026123, May 5, 2015.
- “Method of Updating Transmission of Channel Information Based on Eaves-Dropping of Beamformed Signals,” #9178597, December 8, 2015.
- “Adaptive Transmit Beamforming,” #9209876, December 8, 2015.
- “Method and Apparatus for Managing Uplink Communication in a Wireless Communication Network,” #9210716, December 8, 2015.
- “Wireless Transceivers with Filter Arrangement for WiFi and LTE coexistence,” #9232564, January 5, 2016.
- “Mobile Subscriber Information Transmission Over Multiple Uplink Frames,” #9236975, January 12, 2016.
- “Method of Aiding Uplink Beamforming Transmission,” #9344178, May 17, 2016.
- “Adaptive Transmit Beamforming for Frequency Division Duplexing Systems,” #9537684, January 3, 2017.
- “Mitigating Beam Squint in Millimeter Wave Wireless Communication Systems,” #10819405, October 27, 2020.
- “Low-Resolution, Low-Power, Radio-Frequency Receiver,” #11121896, September 14, 2021.
- “Ultra-Low-Power Millimeter-Wave to Baseband Receiver Module for Scalable Massive MIMO,” #11296742, April 5, 2022.
- “Low-Power, Self-Referenced Receiver,” #11303347, April 12, 2022.

Professional Feature Videos, Projects, Web-pages, and Plenary Talks

“Multiple Antennas: How a Point-to-Point Advantage Becomes a Multi-user Advantage.” Plenary Speaker at the *22nd Biennial Symposium on Communications*, Queens University, Kingston, Ontario, June 2004.

“A Random-Channel Graph-Theoretic Perspective of Wireless Networks.” Plenary Speaker at the *2006 Seventh Annual IEEE Workshop on Signal Processing Advances in Wireless Communication*, Cannes, France, July 2006.

“The Role of MIMO in Fourth-Generation Mobile Wireless Systems and Beyond.” Plenary Speaker at the *2009 IEEE Communication Theory Workshop*, Napa, California, May 2009.

“What Have We Learned So Far About MIMO in Mobile Wireless Systems?” Plenary Speaker at the *2009 Tenth Annual IEEE Workshop on Signal Processing Advances in Wireless Communication*, Perugia, Italy, June 2009.

“Bandwidth of Large-Scale Multiport Radio-Frequency Systems.” Plenary Speaker at the *20th International ITG Workshop on Smart Antennas*, Munich, Germany, March 2016.

“Building a Better Phone,” University of Notre Dame web page feature story, 2016:
<https://www.nd.edu/stories/building-a-better-phone/>

“Notre Dame Researchers Target Cell Phone Radiation,” WSBT television feature story, 2016:
<https://wsbt.com/news/local/notre-dame-researchers-target-cell-phone-radiation>.
<https://engineering.nd.edu/news-publications/engineering-in-the-news/notre-dame-researchers-target-cell-phone-radiation>

Principle Investigator for the *RadioHound Spectrum Sensing System*, 2015–present:
<https://wireless.nd.edu/research/radiohound-distributed-spectrum-sensing>

Editorial, Panelist, and Professional Service Activities

Owner and Editor of <http://mars.bell-labs.com>, the *Multiple-Antenna Research and Solutions* web-site dedicated to promoting research into space-time techniques, 1998–2005. (800 subscribers)

Guest Associate Editor, *IEEE Transactions on Signal Processing Special Issue on Signal Processing for Communications*, with N. Al-Dhahir, G. Giannakis, B. Hughes and T. Marzetta, vol. 50, October 2002.

Guest Editor, *IEEE Transactions on Information Theory Special Issue on Space-Time Transmission, Reception, Coding and Signal Design*, with G. Caire, B. Hassibi and T. Marzetta, vol. 49, October 2003.

Associate Editor for MIMO Techniques, *IEEE Transactions on Communications*, November 2003–2005.

Associate Editor for *IEEE Transactions on Information Theory*, 2011–2012.

IEEE Fellows Committee for the Information Theory Society, 2016–2017.

Panelist, National Science Foundation Signal Processing Systems Faculty Early Career Development Program (CAREER), November 2002; Computer and Information Science Communications/Signal-Processing Research Program, April 2004; Theoretical Foundations of Communications and Signal-Processing Research Program, May 2007; Computing and Communication Foundations (CCF): Core Programs, February 2010; Communications and Information Foundations (CIF), December 2011; Communications and Signal Processing, April 2014; Computer and Network Systems Research Experience for Undergraduates (CNS-REU), November 2018.

Technical Program Chair, *2018 IEEE Communication Theory Workshop*, Miramar Beach, Florida, May 2018.

University Service Activities

Graduate Admissions Committee, 2012–present.

Graduate Committee, 2012–2013, 2016–2018.

College Council, 2014–2017.

Committee for Appointments and Promotions, 2016–2017.

CRADA (Cooperative Research and Development Agreement) between University of Notre Dame and Crane Naval Base, Crane, Indiana, 2016–present.

Co-Director, University of Notre Dame Wireless Institute, 2016–present. In 2017–2018, approximately \$4M/yr in expenditures was routed through the Institute in various projects, including *RadioHound*.

Principal Investigator of an ongoing (2018–) National Science Foundation-funded Research Experience for Undergraduates (REU), sponsoring ten undergraduates from around the United States that visit the University of Notre Dame Wireless Institute for a ten-week research program every summer.

Past Co-Advised PhD Students:

Ibrahim Abou-Faycal (Massachusetts Institute of Technology), 1998
Sriram Vishwanath (Stanford University), 2002
Christian Peel (Brigham-Young University), 2003
Radhika Gowaikar (Caltech), 2005
Heunchul Lee and Kyoung Jae Lee (Korea University), 2007

MS and PhD Students at University of Notre Dame:

Luyu Zhao, MS 2013
Ding Nie, PhD 2015
Kang Gao, PhD 2020
Arash EbadiShahrivar, PhD 2021
Abbas Termos, PhD 2022
Mir Sahariat, MS 2022
Xiangbo Meng, PhD
Christopher Wahl, PhD

Courses, Book Chapters, Tutorials

- “Probabilistic Methods in Signal and System Analysis.” Senior-level undergraduate course, University of Illinois, Urbana-Champaign, January–May 1996.
- “Multi-Antenna Wireless Communications—from Theory to Algorithms,” with B. Hassibi and T. Marzetta. Tutorial at *IEEE Conference on Acoustics, Speech and Signal Processing*, Orlando, FL, May 2002.
- “Communication Theory.” Senior-level undergraduate course, Columbia University, September–December 2005.
- “Linear and Dirty-Paper Techniques for the Multiuser MIMO Downlink,” with Christian B. Peel, Quentin H. Spencer, A. Lee Swindlehurst and Martin Haardt. Book chapter in *Space-Time Processing for MIMO Communications*, A. B. Gershman and N. D. Sidiropoulos (editors), Chichester: John Wiley & Sons, 2005.

Theses and Journal Papers

- “Aspects of Vector-Sensor Processing.” PhD thesis, Yale University, 1995.
- B. Hochwald and A. Nehorai, “Concentrated Cramér-Rao bound expressions,” *IEEE Transactions on Information Theory*, vol. 40, pp. 363–371, March 1994.
- B. Hochwald and A. Nehorai, “Minimum bias priors for estimating additive terms in state-space models,” *IEEE Transactions on Automatic Control*, vol. 40, pp. 684–693, April 1995.
- B. Hochwald and A. Nehorai, “Polarimetric modeling and parameter estimation with applications to remote sensing,” *IEEE Transactions on Signal Processing*, vol. 43, pp. 1923–1935, August 1995.
- B. Hochwald and A. Nehorai, “Identifiability in array processing models with vector-sensor applications,” *IEEE Transactions on Signal Processing*, vol. 44, pp. 83–95, January 1996.
- B. Hochwald and A. Nehorai, “On identifiability and information-regularity in parameterized normal distributions,” *Circuits, Systems, and Signal Processing*, vol. 16, pp. 83–89, January 1997.
- B. Hochwald and A. Nehorai, “Magnetoencephalography with diversely-oriented and multi-component sensors,” *IEEE Transactions on Biomedical Engineering*, vol. 44, pp. 40–50, January 1997.
- B. Hochwald and K. Zeger, “Tradeoff between source and channel coding,” *IEEE Transactions on Information Theory*, vol. 43, pp. 1412–1424, September 1997.
- B. Hochwald, “Tradeoff between source and channel coding on a Gaussian channel,” *IEEE Transactions on Information Theory*, vol. 44, pp. 3044–3055, November 1998.
- B. Hochwald and P. Jelenković, “State Learning and Mixing in Entropy of Hidden Markov Processes and the Gilbert-Elliott Channel,” *IEEE Transactions on Information Theory*, vol. 45, pp. 128–138, January 1999.
- T. Marzetta and B. Hochwald, “Capacity of a mobile multiple-antenna communication link in Rayleigh flat fading,” *IEEE Transactions on Information Theory*, vol. 45, pp. 139–157, January 1999.
- B. Hochwald and T. Marzetta, “Unitary space-time modulation for multiple-antenna communications in Rayleigh flat fading,” *IEEE Transactions on Information Theory*, vol. 46, pp. 543–564, March 2000.
- B. Hochwald, T. Marzetta, T. Richardson, W. Sweldens, and R. Urbanke, “Systematic design of unitary space-time constellations,” *IEEE Transactions on Information Theory*, vol. 46, pp. 1962–1973, September 2000.
- B. Hochwald and W. Sweldens, “Differential unitary space-time modulation,” *IEEE Transactions on Communications*, vol. 48, pp. 2041–2052, December 2000.
- B. Hochwald and T. Marzetta, “Adapting a downlink array from uplink measurements,” *IEEE Transactions on Signal Processing*, vol. 49, pp. 642–653, March 2001.
- B. Hochwald, T. Marzetta, and C. Papadias, “A transmitter diversity scheme for wideband CDMA systems based on space-time spreading,” *IEEE Journal on Selected Areas of Communication: Special Issue on Wideband CDMA*, vol. 19, pp. 48–60, March 2001.
- A. Shokrollahi, B. Hassibi, B. Hochwald, and W. Sweldens, “Representation theory for high-rate multiple-antenna code design,” *IEEE Transactions on Information Theory*, vol. 47, pp. 2335–2367, September 2001.

Journal Papers (cont'd)

- B. Hochwald, T. Marzetta, and B. Hassibi, "Space-time autocoding," *IEEE Transactions on Information Theory*, vol. 47, pp. 2761–2781, November 2001.
- T. Marzetta, B. Hassibi, and B. Hochwald, "Structured unitary space-time autocoding constellations," *IEEE Transactions on Information Theory*, vol. 48, pp. 942–950, April 2002.
- B. Hassibi and B. Hochwald, "Cayley differential unitary space-time codes," *IEEE Transactions on Information Theory*, vol. 48, pp. 1485–1503, June 2002.
- B. Hassibi and B. Hochwald, "High-rate codes that are linear in space and time," *IEEE Transactions on Information Theory*, vol. 48, pp. 1804–1824, July 2002.
- N. Al-Dhahir, G. Giannakis, B. Hochwald, B. Hughes, and T. Marzetta, "Guest editorial," *IEEE Transactions on Signal Processing*, vol. 50, pp. 2381–2384, October 2002.
- B. Hochwald and S. ten Brink, "Achieving near-capacity on a multiple-antenna channel," *IEEE Transactions on Communications*, vol. 53, pp. 389–399, March 2003.
- B. Hassibi and B. Hochwald, "How much training is needed in multiple-antenna wireless links?" *IEEE Transactions on Information Theory*, vol. 49, pp. 951–963, April 2003.
- B. Hochwald, G. Caire, B. Hassibi, and T. Marzetta, "The academic and industrial embrace of space-time methods," *IEEE Transactions on Information Theory: Special Issue on Space-Time Transmission, Reception, Coding and Signal Processing*, vol. 49, pp. 2329–2331, October 2003.
- B. Hochwald, T. Marzetta, and V. Tarokh, "Multiple-antenna channel hardening and its implications for rate-feedback and scheduling," *IEEE Transactions on Information Theory*, vol. 50, pp. 1893–1909, September 2004.
- H. Vikalo, B. Hassibi, B. Hochwald, and T. Kailath, "On the capacity of frequency-selective channels in training-based transmission schemes," *IEEE Transactions on Signal Processing*, vol. 52, pp. 2572–2583, September 2004.
- D. Garrett, L. Davis, S. ten Brink, B. Hochwald, and G. Knagge, "Silicon complexity for maximum-likelihood MIMO detection using spherical decoding," *IEEE Journal of Solid State Circuits*, vol. 39, pp. 1544–1552, September 2004.
- A. Alexiou, D. Avidor, P. Bosch, S. Das, P. Gupta, B. Hochwald, T. Klein, J. Ling, A. Lozano, T. Marzetta, S. Mukherjee, C. Papadias, R. Valenzuela, and H. Viswanathan, "Duplexing, resource allocation, and inter-cell coordination: design recommendations for next-generation wireless systems," *Wireless Communications and Mobile Computing*, vol. 5, pp. 77–93, May 2005.
- T. Marzetta and B. Hochwald, "Fast transfer of channel state information in wireless systems," *IEEE Transactions on Signal Processing*, vol. 54, pp. 1268–1278, April 2006.
- R. Gowaikar, B. Hochwald, and B. Hassibi, "Communication over a wireless network with random connections," *IEEE Transactions on Information Theory*, vol. 52, pp. 2857–2871, July 2006.
- C. Peel, B. Hochwald and A. L. Swindlehurst, "A vector-perturbation technique for near-capacity multi-antenna multi-user communication—Part I: Channel inversion and regularization," *IEEE Transactions on Communications*, vol. 53, pp. 195–202, January 2005. **Winner of the 2006 IEEE Transactions on Communications Stephen O. Rice Best Paper Award.**

Journal Papers (cont'd)

- B. Hochwald, C. Peel, and A. L. Swindlehurst, "A vector-perturbation technique for near-capacity multi-antenna multi-user communication—Part II: Perturbation," *IEEE Transactions on Communications*, vol. 53, pp. 537–544, March 2005. **Winner of the 2006 IEEE Transactions on Communications Stephen O. Rice Best Paper Award.**
- A. Ashikhmin, A. van Wijngaarden, Z. Haibo, B. Hochwald, T. Marzetta, V. Purohit, C. Qinghong, P. Wilford, S-R. Zhou, M. Zuniga, E. Zuranski, "Design and development of a terrestrial digital video broadcast demodulation core: An international collaborative effort," *Bell Labs Technical Journal*, vol. 12, pp. 97–118, 2007.
- B. Hochwald and H. Artés, "Orthogonalizing beams to train unscheduled terminals," *IEEE Transactions on Signal Processing*, vol. 57, pp. 3063–3074, August 2009.
- E. Stauffer and B. Hochwald, "Low-complexity multi-stream space-time codes—Part I: Direct-sum codes and design criteria," *IEEE Transactions on Communications*, vol. 60, pp. 81–88, January 2012.
- B. Hochwald and E. Stauffer, "Low-complexity multi-stream space-time codes—Part II: Unitary-transform codes," *IEEE Transactions on Communications*, vol. 60, pp. 375–383, February 2012.
- D. Nie, B. Hochwald, and E. Stauffer, "Systematic design of large-scale multiport decoupling networks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, pp. 2172–2181, July 2014.
- B. Hochwald, D. Love, S. Yan, P. Fay, J-M. Jin, "Incorporating specific absorption rate constraints into wireless signal design," *IEEE Communications Magazine*, vol. 52, pp. 126–133, September, 2014.
- D. Nie and B. Hochwald, "Broadband matching bounds for coupled loads," *IEEE Transactions of Circuits and Systems I: Regular Papers*, vol. 62, pp. 995–1004, April 2015. **Winner of the 2016 IEEE Transactions on Circuits and Systems Best Paper Award by a Young Author.**
- D. Ying, D. Love, and B. Hochwald, "Closed-loop precoding and capacity analysis for multiple antenna wireless systems with user radiation exposure constraints," *IEEE Transactions on Wireless Communications*, vol. 14, pp. 5859–5870, October 2015.
- D. Nie and B. Hochwald, "Bandwidth analysis of multiport radio-frequency systems—Part I," *IEEE Transactions on Antennas and Propagation*, vol. 65, pp. 1081–1092, March 2017. **Winner of the 2018 IEEE Transactions on Antennas and Propagation H. A. Wheeler Prize Paper Award.**
- D. Nie and B. Hochwald, "Bandwidth analysis of multiport radio-frequency systems—Part II," *IEEE Transactions on Antennas and Propagation*, vol. 65, pp. 1093–1107, March 2017.
- D. Ying, D. Love, and B. Hochwald, "Sum-rate analysis for multi-user MIMO systems with user exposure constraints," *IEEE Transactions on Wireless Communications*, vol. 16, pp. 7376–7388, November 2017.
- D. Nie and B. Hochwald, "Improved broadband matching bound," *IEEE Transactions on Antennas and Propagation*, vol. 65, pp. 5878–5885, November 2017.
- J. Li, S. Yan, Y. Liu, B. Hochwald, and J-M. Jin, "A high-order model for fast estimation of electromagnetic absorption induced by multiple transmitters in portable devices," *IEEE Transactions on Antennas and Propagation*, vol. 65, pp. 6768–6778, December 2017.
- A. Ebadi-Shahrivar, P. Fay, D.J. Love, and B. Hochwald, "Determining electromagnetic exposure compliance of multi-antenna devices in linear time," *IEEE Transactions on Antennas and Propagation*, vol. 67, pp. 7585–7596, December 2019.

Journal Papers (cont'd)

- M. Castellanos, Y. Liu, D. Love, B. Peleato, J.-M. Jin, and B. Hochwald, "Signal-level models of pointwise electromagnetic exposure for millimeter-wave communication," *IEEE Transactions on Antennas and Propagation*, pp. 3963–3977, May 2020.
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Appendix B

List of Materials Considered

Exhibit ("Ex.")	Description
Ex. 1001	U.S. Patent No. 9,065,486 ("486")
Ex. 1002	File History of U.S. Patent No. 9,065,486 ("486 FH)
Ex. 1004	Declaration of Friedhelm Rodermund in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 9,065,486 ("Rodermund")
Ex. 1005	U.S. Patent No. 7,260,770 ("Stewart")
Ex. 1006	R1-01-1014, "A New Hybrid-ARQ Scheme Using Incremental Redundancy," submitted by Motorola for 3GPP Meeting R1-ah-22010 (Nov 5-7, 2001) ("Motorola")
Ex. 1007	R1-01-1047, "Overview of Proposed Schemes for Incremental Redundancy," submitted by Ericsson for 3GPP Meeting R1-ah-22010 (Nov 5-7, 2001) ("3GPP-Summary")
Ex. 1008	Universal Mobile Telecommunications System (UMTS); Multiplexing and channel coding (FDD) (3GPP TS 25.212 version 5.1.0 Release 5)
Ex. 1009	Lin et al., "Error Control Coding: Fundamentals and Applications"
Ex. 1010	File History of E.P. No. 1573923
Ex. 1011	3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (TDD) (3GPP TS 25.222 version 3.8.0 Release 1999)
Ex. 1012	U.S. Patent No. 6,631,491 ("Shibutani")
Ex. 1013	U.S. Patent No. 5,537,420 ("Huang")

Exhibit ("Ex.")	Description
Ex. 1014	E.P. No. 0865172 ("Honkasalo")
Ex. 1015	U.S. Patent No. 6,356,601 ("Chen")
Ex. 1016	File History of U.S. Patent No. 7,293,217
Ex. 1017	File History of U.S. Patent No. 8,074,143
Ex. 1018	File History of U.S. Patent No. 8,359,520
Ex. 1019	File History of U.S. Patent No. 8,788,920
Ex. 1025	The Authoritative Dictionary of IEEE Standard Terms, 7 th Edition
Ex. 1026	Microsoft Computer Dictionary, 5 th Edition
Ex. 1027	U.S. Patent Application Publication No. 2005/0094667 ("Dahlman-667")
Ex. 1028	U.S. Patent No. 7,372,837 ("Kinjo")
Ex. 1029	U.S. Patent No. 7,000,173 ("Buckley")
Ex. 1030	U.S. Patent No. 7,020,455 ("Krishnarajah")
Ex. 1031	U.S. Patent No. 6,760,365 ("Demir")
Ex. 1032	E.P. Patent No. 1209856 ("Miya")
Ex. 1033	U.S. Patent No. 6,754,253 ("Guey")
Ex. 1034	U.S. Patent No. 6,760,600 ("Nickum")
Ex. 1035	U.S. Patent No. 6,515,980 ("Bottomley")
Ex. 1036	3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD) (3GPP TS 25.212 version 3.5.0 Release 1999)

Exhibit ("Ex.")	Description
Ex. 1037	Ghosh et al., "Incremental Redundancy (IR) Schemes for W-CDMA HS-DSCH"
Ex. 1038	U.S. Patent No. 6,744,744 ("Tong")
Ex. 1039	U.S. Patent No. 7,170,849 ("Arivoli")
Ex. 1040	U.S. Patent Application Publication No. 2004/0037224 ("Choi")
Ex. 1041	U.S. Patent No. 7,286,540 ("Kim-540")
Ex. 1042	U.S. Patent No. 7,362,733 ("Kim-733")
Ex. 1043	Frenger et. al., "Performance Comparison of HARQ with Chase Combining and Incremental Redundancy for HSDPA"
Ex. 1044	U.S. Patent No. 6,671,851 ("Moulsley")
Ex. 1045	R1-01-1014 Metadata
Ex. 1046	U.S. Patent No. 8,074,143 ("143 patent")
Ex. 1047	Joint Claim Construction and Prehearing Statement, <i>Pantech Corp. et al. v. LG Electronics Inc. et al.</i> , Case 5:22-cv-00113-RWS-JBB (E.D. Texas), Dkt. No. 118.
Ex. 1051	Webpage, available at https://archive.org/legal/affidavit.php
Ex. 1052	Internet Archive Capture, available at https://web.archive.org/web/20020126155238/http://www.3gpp.org:80/TB/home.htm
Ex. 1053	Internet Archive Capture, available at https://web.archive.org/web/20020926134824/http://www.3gpp.org:80/

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Ex. 1054	Internet Archive Capture, available at https://web.archive.org/web/20021015011140/http://www.3gpp.org:80/TB/RAN/RAN1/RAN1.htm
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Ex. 1056	Internet Archive Capture, available at https://web.archive.org/web/20020403145941/http://www.3gpp.org:80/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/HSDPA_Ad_Hoc/
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Ex. 1058	Webpage, available at ftp.3gpp.org/Specs
Ex. 1059	Internet Archive Capture, available at https://web.archive.org/web/20020806115924/http://www.3gpp.org/Default.htm
Ex. 1060	Internet Archive Capture, available at https://web.archive.org/web/20020802092436/http://www.3gpp.org/specs/specs.htm
Ex. 1061	Internet Archive Capture, available at https://web.archive.org/web/20020806054349/http://www.3gpp.org/specs/numbering.htm
Ex. 1062	Internet Archive Capture, available at https://web.archive.org/web/20020806092102/http://www.3gpp.org/specs/titles-numbers.htm

Exhibit ("Ex.")	Description
Ex. 1063	Word file entitled "3GPP specifications - List of all specification numbers and titles," retrieved from https://web.archive.org/web/20071101043800/http://www.3gpp.org/specs/3GPP-Spec-Titles.zip (3GPP-Spec-Titles.doc in 3GPP-Spec-Titles.zip)
Ex. 1064	Internet Archive Capture, available at https://web.archive.org/web/20021015011140/http://www.3gpp.org/TB/RAN/RAN1/RAN1.htm
Ex. 1065	Internet Archive Capture, available at https://web.archive.org/web/20021022011153/http://www.3gpp.org/TB/RAN/RAN1/specs.htm
Ex. 1066	Internet Archive Capture, available at https://web.archive.org/web/20020628215611/http://www.3gpp.org/ftp/specs/archive/
Ex. 1067	Internet Archive Capture, available at https://web.archive.org/web/20020701091801/http://www.3gpp.org:80/ftp/specs/archive/25_series/
Ex. 1068	Internet Archive Capture, available at https://web.archive.org/web/20020912200940/http://www.3gpp.org:80/ftp/Specs/archive/25_series/25.212/
Ex. 1069	Internet Archive Capture, available at https://web.archive.org/web/20020803112613/http://www.3gpp.org/ftp/Specs/latest/
Ex. 1070	Internet Archive Capture, available at https://web.archive.org/web/20020804015202/http://www.3gpp.org/ftp/Specs/latest/Rel-5/
Ex. 1071	Internet Archive Capture, available at https://web.archive.org/web/20020812090150/http://www.3gpp.org:80/ftp/Specs/latest/Rel-5/25_series/

Exhibit ("Ex.")	Description
Ex. 1072	Internet Archive Capture, available at https://web.archive.org/web/20051103081215/http://list.3gpp.org/scripts/wa.exe?SUBED1=3gpp_tsg_ran_wg1&A=1
Ex. 1073	Webpage, available at https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Docs/Zips/
Ex. 1074	R1-01-1014, retrieved from https://list.etsi.org/scripts/wa.exe?A3=ind0110&L=3GPP_TSG_RAN_WG1&E=base64&P=2072790&B=-----%3D_NextPart_000_01C15C16.5D43E0D0&T=application%2Foctet-stream;%20name=%22R1-01-1014.zip%22&N=R1-01-1014.zip&attachment=q&X=6DEE3DFAFC65AFF81C&Y=friedhelm.roderrmund%40iotecc.com (R1-01-1014.doc in R1-01-1014.zip)
Ex. 1075	Webpage, available at https://list.etsi.org/scripts/wa.exe?A2=3GPP_TSG_RAN_WG1;84332eeb.0110&S=
Ex. 1076	Webpage, available at https://web.archive.org/web/20010518052528/http://list.etsi.org/
Ex. 1077	Internet Archive Capture, available at https://web.archive.org/web/20020604215730/http://list.etsi.org:80/
Ex. 1078	Internet Archive Capture, available at https://web.archive.org/web/20050824015238/http://www.3gpp.org:80/ftp/tsg_ran/WG1_RL1/
Ex. 1079	Internet Archive Capture, available at https://web.archive.org/web/20051123162134/http://www.3gpp.org:80/ftp/tsg_ran/WG1_RL1/
Ex. 1080	Internet Archive Capture, available at https://web.archive.org/web/20011223090820/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/

Exhibit ("Ex.")	Description
Ex. 1081	Internet Archive Capture, available at https://web.archive.org/web/20020619173234/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/
Ex. 1082	Internet Archive Capture, available at https://web.archive.org/web/20020415205129/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/HSDPA_Ad_Hoc/Docs/
Ex. 1083	Internet Archive Capture, available at https://web.archive.org/web/20040519152539/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/HSDPA_Ad_Hoc/Docs/Zips/
Ex. 1084	R1-01-1014 in R1-01-1014.zip, retrieved from https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Docs/Zips/R1-01-1014.zip
Ex. 1085	Webpage, available at https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Report
Ex. 1086	R1-01-1081 in R1-01-1105.zip, retrieved from https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Report/R1-01-1105.zip
Ex. 1087	R1-01-1081, in R1-01-1081.zip, retrieved from https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Docs/Zips/R1-01-1081.zip
Ex. 1088	Redline comparing disclosures of R1-01-1014 and R1-01-1081
Ex. 1089	U.S. Patent No. 7,210,089
Ex. 1090	U.S. Patent App. No. 10/193,144
Ex. 1091	R1-01-1047, in R1-01-1047.zip, retrieved from https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Docs/Zips/R1-01-1047.zip

Exhibit ("Ex.")	Description
Ex. 1092	Webpage, available at https://www.3gpp.org/ftp/Specs/archive/25_series/25.212
Ex. 1093	Webpage, available at https://www.etsi.org/deliver/etsi_ts/125200_125299/125212/05.01.00_60/
Ex. 1094	ETSI TS 125 212 V5.1.0 (2002-06), retrieved from https://www.etsi.org/deliver/etsi_ts/125200_125299/125212/05.01.00_60/ts_125212v050100p.pdf
Ex. 1095	Internet Archive Capture, available at https://web.archive.org/web/20020202222234/http://etsi.org/getastandard/home.htm
Ex. 1096	Internet Archive Capture, available at https://web.archive.org/web/20020202222234/http://etsi.org/getastandard/home.htm
Ex. 1097	Internet Archive Capture, available at https://web.archive.org/web/20020912200940/http://www.3gpp.org/ftp/Specs/archive/25_series/25.212/
Ex. 1098	3GPP TS 25.212 V5.1.0 (2002-06), retrieved from https://www.3gpp.org/ftp/Specs/archive/25_series/25.212/25212-510.zip (25212-510.doc in 25212-510.zip)
Ex. 1099	Internet Archive Capture, available at https://web.archive.org/web/20020626102256/http://www.3gpp.org/TB/ran/ran1/specs.htm
Ex. 1100	Kumar, Ratnam V. Raja, "Development of a CDMA system with RAKE receiver for the third generation wireless communication systems," 2002 IEEE International Conference on Personal Wireless Communications, December 15-17, 2002

Exhibit ("Ex.")	Description
Ex. 1101	Webpage, available at https://ieeexplore.ieee.org/abstract/document/1177299
Ex. 1102	Webpage, available at https://www.3gpp.org/ftp/Specs/archive/25_series/25.222
Ex. 1103	Webpage, available at https://www.etsi.org/deliver/etsi_ts/125200_125299/125222/03.08.00_60/
Ex. 1104	ETSI TS 125 222 V3.8.0 (2002-03), retrieved from https://www.etsi.org/deliver/etsi_ts/125200_125299/125222/03.08.00_60/ts_125222v030800p.pdf
Ex. 1105	Internet Archive Capture, available at https://web.archive.org/web/20020613173206/http://webapp.etsi.org:80/key/key.asp?full_list=y
Ex. 1106	Internet Archive Capture, available at https://web.archive.org/web/20020531000359/http://www.3gpp.org:80/ftp/specs/archive/25_series/25.222/
Ex. 1107	Internet Archive Capture, available at https://web.archive.org/web/20020225110409/http://www.3gpp.org:80/TB/ran/ran1/specs.htm
Ex. 1108	Webpage, available at https://www.etsi.org/deliver/etsi_ts/125200_125299/125212/03.05.00_60/
Ex. 1109	ETSI TS 125.212 V3.5.0 (2000-12), retrieved from https://www.etsi.org/deliver/etsi_ts/125200_125299/125212/03.05.00_60/ts_125212v030500p.pdf
Ex. 1110	Internet Archive Capture, available at https://web.archive.org/web/20011020025720/http://etsi.org/getastandard/home.htm

Exhibit ("Ex.")	Description
Ex. 1111	Internet Archive Capture, available at https://web.archive.org/web/20011124215727/http://www.3gpp.org/ftp/Specs/archive/25_series/25.212/
Ex. 1112	Internet Archive Capture, available at https://web.archive.org/web/20020111012800/http://www.3gpp.org:80/ftp/Specs/archive/25_series/25.212/
Ex. 1113	3GPP TS 25.212 V3.5.0. (2000-12), in 25212-350.zip, retrieved from https://www.3gpp.org/ftp/Specs/archive/25_series/25.212/25212-350.zip
Ex. 1114	Internet Archive Capture, available at https://web.archive.org/web/20020802173135/http://www.3gpp.org/ftp/Specs/
Ex. 1115	Internet Archive Capture, available at https://web.archive.org/web/20020806031707/http://www.3gpp.org/ftp/Specs/archive/
Ex. 1116	Internet Archive Capture, available at https://web.archive.org/web/20020701091801/http://www.3gpp.org/ftp/specs/archive/25_series/
Ex. 1117	Internet Archive Capture, available at https://web.archive.org/web/20020531003232/http://www.3gpp.org/ftp/specs/latest/Rel-6/25_series/
Ex. 1118	Internet Archive Capture, available at https://web.archive.org/web/20020812090150/http://www.3gpp.org/ftp/Specs/latest/Rel-5/25_series/
Ex. 1119	TS 25.222 V3.8.0 (2002-03), in 25222-380.zip, retrieved from https://www.3gpp.org/ftp/Specs/archive/25_series/25.222/25222-380.zip

Appendix C

LIST OF CHALLENGED CLAIMS:

[1.pre] An apparatus for use in wireless communications comprising:

- [1.a] a first interleaver configured to interleave systematic bits;
- [1.b] a second interleaver configured to interleave a first parity bit stream;
- [1.c] a third interleaver configured to interleave a second parity bit stream;
- [1.d] a buffer configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and
- [1.e] a rate matching unit configured to select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.

Claim 2: The apparatus of claim 1 wherein selecting of bits by the rate matching unit in response to a selected redundancy version changes in response to a location of the bits in the buffer.

[3.pre] A method for use in an apparatus of a wireless communications comprising:

- [3.a] interleaving, by the apparatus, systematic bits;
- [3.b] interleaving, by the apparatus, a first parity bit stream;

[3.c] interleaving, by the apparatus, a second parity bit stream;

[3.d] buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and

[3.e] selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.

Claim 4: The method of claim 3 wherein the selecting of bits for transmission in response to a selected redundancy version changes in response to a location of the bits in the buffer.

[5.pre] A wireless transmit/receive unit comprising:

[5.a] circuitry configured to interleave systematic bits;

[5.b] circuitry is further configured to interleave a first parity bit stream;

[5.c] circuitry is further configured to interleave a second parity bit stream;

[5.d] circuitry is further configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and

[5.e] circuitry is further configured to select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.

Claim 6: The wireless transmit/receive unit of claim 5 wherein selecting of bits based on a selected redundancy version changes in response to a location of the bits in the buffer.