

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS INC.,

Petitioner,

v.

PANTECH WIRELESS, LLC,

Patent Owner.

Case IPR2023-01272

U.S. Patent No. 9,065,486

PETITION FOR *INTER PARTES* REVIEW

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EXHIBIT LIST

Exhibit ("Ex.")	Description
Ex. 1001	U.S. Patent No. 9,065,486 ("486")
Ex. 1002	File History of U.S. Patent No. 9,065,486 ("486 FH)
Ex. 1003	Declaration of Dr. Bertrand Hochwald in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 9,065,486 ("Hochwald")
Ex. 1004	Declaration of Friedhelm Rodermund in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 9,065,486 ("Rodermund")
Ex. 1005	U.S. Patent No. 7,260,770 ("Stewart")
Ex. 1006	R1-01-1014, "A New Hybrid-ARQ Scheme Using Incremental Redundancy," submitted by Motorola for 3GPP Meeting R1-ah-22010 (Nov 5-7, 2001) ("Motorola")
Ex. 1007	R1-01-1047, "Overview of Proposed Schemes for Incremental Redundancy," submitted by Ericsson for 3GPP Meeting R1-ah-22010 (Nov 5-7, 2001) ("3GPP-Summary")
Ex. 1008	3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD) (Release 5) (3GPP TS 25.212 version 5.1.0)
Ex. 1009	Lin et al., "Error Control Coding: Fundamentals and Applications"
Ex. 1010	File History of E.P. No. 1573923
Ex. 1011	3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (TDD) (Release 1999) (3GPP TS 25.222 version 3.8.0)
Ex. 1012	U.S. Patent No. 6,631,491 ("Shibutani")
Ex. 1013	U.S. Patent No. 5,537,420 ("Huang")

Exhibit ("Ex.")	Description
Ex. 1014	E.P. No. 0865172 ("Honkasalo")
Ex. 1015	U.S. Patent No. 6,356,601 ("Chen")
Ex. 1016	File History of U.S. Patent No. 7,293,217
Ex. 1017	File History of U.S. Patent No. 8,074,143
Ex. 1018	File History of U.S. Patent No. 8,359,520
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Ex. 1020	[Reserved]
Ex. 1021	[Reserved]
Ex. 1022	Third Amended Docket Control Order, <i>Pantech Corp. et al. v. LG Electronics Inc. et al.</i> , Case 5:22-cv-00113-RWS-JBB (E.D. Texas), Dkt. No. 98.
Ex. 1023	Docket Navigator "Time to Trial" report for Judge Robert W. Schroeder
Ex. 1024	USCourts.gov "U.S. District Court – Judicial Caseload Profile" for Eastern District of Texas
Ex. 1025	The Authoritative Dictionary of IEEE Standard Terms, 7 th Edition
Ex. 1026	Microsoft Computer Dictionary, 5 th Edition
Ex. 1027	U.S. Patent Application Publication No. 2005/0094667 ("Dahlman-667")
Ex. 1028	U.S. Patent No. 7,372,837 ("Kinjo")
Ex. 1029	U.S. Patent No. 7,000,173 ("Buckley")
Ex. 1030	U.S. Patent No. 7,020,455 ("Krishnarajah")

Exhibit ("Ex.")	Description
Ex. 1031	U.S. Patent No. 6,760,365 ("Demir")
Ex. 1032	E.P. Patent No. 1209856 ("Miya")
Ex. 1033	U.S. Patent No. 6,754,253 ("Guey")
Ex. 1034	U.S. Patent No. 6,760,600 ("Nickum")
Ex. 1035	U.S. Patent No. 6,515,980 ("Bottomley")
Ex. 1036	3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD) (3GPP TS 25.212 version 3.5.0 Release 1999)
Ex. 1037	Ghosh et al., "Incremental Redundancy (IR) Schemes for W-CDMA HS-DSCH"
Ex. 1038	U.S. Patent No. 6,744,744 ("Tong")
Ex. 1039	U.S. Patent No. 7,170,849 ("Arivoli")
Ex. 1040	U.S. Patent Application Publication No. 2004/0037224 ("Choi")
Ex. 1041	U.S. Patent No. 7,286,540 ("Kim-540")
Ex. 1042	U.S. Patent No. 7,362,733 ("Kim-733")
Ex. 1043	Frenger et. al., "Performance Comparison of HARQ with Chase Combining and Incremental Redundancy for HSDPA"
Ex. 1044	U.S. Patent No. 6,671,851 ("Moulsley")
Ex. 1045	R1-01-1014 Metadata
Ex. 1046	U.S. Patent No. 8,074,143 ("143 patent")

Exhibit ("Ex.")	Description
Ex. 1047	Joint Claim Construction and Prehearing Statement, <i>Pantech Corp. et al. v. LG Electronics Inc. et al.</i> , Case 5:22-cv-00113-RWS-JBB (E.D. Texas), Dkt. No. 118.
Ex. 1048	Declaration of Jonathan Bradford
Ex. 1049 to Ex. 1050	Reserved
Ex. 1051	Webpage, available at https://archive.org/legal/affidavit.php
Ex. 1052	Internet Archive Capture, available at https://web.archive.org/web/20020126155238/http://www.3gpp.org:80/TB/home.htm
Ex. 1053	Internet Archive Capture, available at https://web.archive.org/web/20020926134824/http://www.3gpp.org:80/
Ex. 1054	Internet Archive Capture, available at https://web.archive.org/web/20021015011140/http://www.3gpp.org:80/TB/RAN/RAN1/RAN1.htm
Ex. 1055	Internet Archive Capture, available at https://web.archive.org/web/20020806041024/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/
Ex. 1056	Internet Archive Capture, available at https://web.archive.org/web/20020403145941/http://www.3gpp.org:80/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/HSDPA_Ad_Hoc/
Ex. 1057	Excel file "work_plan_3gpp_020926.xls," retrieved from https://web.archive.org/web/20060625054352/http://www.3gpp.org/ftp/Information/WORK_PLAN/older_versions/work_plan_3gpp_020926.zip (work_plan_3gpp_020926.xls in work_plan_3gpp_020926.zip)

Exhibit ("Ex.")	Description
Ex. 1058	Webpage, available at ftp.3gpp.org/Specs
Ex. 1059	Internet Archive Capture, available at https://web.archive.org/web/20020806115924/http://www.3gpp.org/Default.htm
Ex. 1060	Internet Archive Capture, available at https://web.archive.org/web/20020802092436/http://www.3gpp.org/specs/specs.htm
Ex. 1061	Internet Archive Capture, available at https://web.archive.org/web/20020806054349/http://www.3gpp.org/specs/numbering.htm
Ex. 1062	Internet Archive Capture, available at https://web.archive.org/web/20020806092102/http://www.3gpp.org/specs/titles-numbers.htm
Ex. 1063	Word file entitled "3GPP specifications - List of all specification numbers and titles," retrieved from https://web.archive.org/web/20071101043800/http://www.3gpp.org/specs/3GPP-Spec-Titles.zip (3GPP-Spec-Titles.doc in 3GPP-Spec-Titles.zip)
Ex. 1064	Internet Archive Capture, available at https://web.archive.org/web/20021015011140/http://www.3gpp.org/TB/RAN/RAN1/RAN1.htm
Ex. 1065	Internet Archive Capture, available at https://web.archive.org/web/20021022011153/http://www.3gpp.org/TB/RAN/RAN1/specs.htm
Ex. 1066	Internet Archive Capture, available at https://web.archive.org/web/20020628215611/http://www.3gpp.org/ftp/specs/archive/

Exhibit ("Ex.")	Description
Ex. 1067	Internet Archive Capture, available at https://web.archive.org/web/20020701091801/http://www.3gpp.org:80/ftp/specs/archive/25_series/
Ex. 1068	Internet Archive Capture, available at https://web.archive.org/web/20020912200940/http://www.3gpp.org:80/ftp/Specs/archive/25_series/25.212/
Ex. 1069	Internet Archive Capture, available at https://web.archive.org/web/20020803112613/http://www.3gpp.org/ftp/Specs/latest/
Ex. 1070	Internet Archive Capture, available at https://web.archive.org/web/20020804015202/http://www.3gpp.org/ftp/Specs/latest/Rel-5/
Ex. 1071	Internet Archive Capture, available at https://web.archive.org/web/20020812090150/http://www.3gpp.org:80/ftp/Specs/latest/Rel-5/25_series/
Ex. 1072	Internet Archive Capture, available at https://web.archive.org/web/20051103081215/http://list.3gpp.org/scripts/wa.exe?SUBED1=3gpp_tsg_ran_wg1&A=1
Ex. 1073	Webpage, available at https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Docs/Zips/
Ex. 1074	R1-01-1014, retrieved from https://list.etsi.org/scripts/wa.exe?A3=ind0110&L=3GPP_TSG_RAN_WG1&E=base64&P=2072790&B=-----%3D_NextPart_000_01C15C16.5D43E0D0&T=application%2Foctet-stream;%20name=%22R1-01-1014.zip%22&N=R1-01-1014.zip&attachment=q&X=6DEE3DFAFC65AFF81C&Y=friedhelm.roderrmund%40iotecc.com (R1-01-1014.doc in R1-01-1014.zip)

Exhibit ("Ex.")	Description
Ex. 1075	Webpage, available at https://list.etsi.org/scripts/wa.exe?A2=3GPP_TSG_RAN_WG1;84332eeb.0110&S=
Ex. 1076	Webpage, available at https://web.archive.org/web/20010518052528/http://list.etsi.org/
Ex. 1077	Internet Archive Capture, available at https://web.archive.org/web/20020604215730/http://list.etsi.org:80/
Ex. 1078	Internet Archive Capture, available at https://web.archive.org/web/20050824015238/http://www.3gpp.org:80/ftp/tsg_ran/WG1_RL1/
Ex. 1079	Internet Archive Capture, available at https://web.archive.org/web/20051123162134/http://www.3gpp.org:80/ftp/tsg_ran/WG1_RL1/
Ex. 1080	Internet Archive Capture, available at https://web.archive.org/web/20011223090820/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/
Ex. 1081	Internet Archive Capture, available at https://web.archive.org/web/20020619173234/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/
Ex. 1082	Internet Archive Capture, available at https://web.archive.org/web/20020415205129/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/HSDPA_Ad_Hoc/Docs/
Ex. 1083	Internet Archive Capture, available at https://web.archive.org/web/20040519152539/http://www.3gpp.org/ftp/tsg_ran/WG1_RL1/R1_Ad_Hocs/HSDPA_Ad_Hoc/Docs/Zips/

Exhibit ("Ex.")	Description
Ex. 1084	R1-01-1014 in R1-01-1014.zip, retrieved from https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Docs/Zips/R1-01-1014.zip
Ex. 1085	Webpage, available at https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Report
Ex. 1086	R1-01-1081 in R1-01-1105.zip, retrieved from https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Report/R1-01-1105.zip
Ex. 1087	R1-01-1081, in R1-01-1081.zip, retrieved from https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Docs/Zips/R1-01-1081.zip
Ex. 1088	Redline comparing disclosures of R1-01-1014 and R1-01-1081
Ex. 1089	U.S. Patent No. 7,210,089
Ex. 1090	U.S. Patent App. No. 10/193,144
Ex. 1091	R1-01-1047, in R1-01-1047.zip, retrieved from https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_AH/HSDPA_Ad_Hoc/Docs/Zips/R1-01-1047.zip
Ex. 1092	Webpage, available at https://www.3gpp.org/ftp/Specs/archive/25_series/25.212
Ex. 1093	Webpage, available at https://www.etsi.org/deliver/etsi_ts/125200_125299/125212/05.01.00_60/
Ex. 1094	ETSI TS 125 212 V5.1.0 (2002-06), retrieved from https://www.etsi.org/deliver/etsi_ts/125200_125299/125212/05.01.00_60/ts_125212v050100p.pdf

Exhibit ("Ex.")	Description
Ex. 1095	Internet Archive Capture, available at https://web.archive.org/web/20020202222234/http://etsi.org/getastandard/home.htm
Ex. 1096	Internet Archive Capture, available at https://web.archive.org/web/20020202222234/http://etsi.org/getastandard/home.htm
Ex. 1097	Internet Archive Capture, available at https://web.archive.org/web/20020912200940/http://www.3gpp.org/ftp/Specs/archive/25_series/25.212/
Ex. 1098	3GPP TS 25.212 V5.1.0 (2002-06), retrieved from https://www.3gpp.org/ftp/Specs/archive/25_series/25.212/25212-510.zip (25212-510.doc in 25212-510.zip)
Ex. 1099	Internet Archive Capture, available at https://web.archive.org/web/20020626102256/http://www.3gpp.org/TB/ran/ran1/specs.htm
Ex. 1100	Kumar, Ratnam V. Raja, "Development of a CDMA system with RAKE receiver for the third generation wireless communication systems," 2002 IEEE International Conference on Personal Wireless Communications, December 15-17, 2002
Ex. 1101	Webpage, available at https://ieeexplore.ieee.org/abstract/document/1177299
Ex. 1102	Webpage, available at https://www.3gpp.org/ftp/Specs/archive/25_series/25.222
Ex. 1103	Webpage, available at https://www.etsi.org/deliver/etsi_ts/125200_125299/125222/03.08.00_60/

Exhibit ("Ex.")	Description
Ex. 1104	ETSI TS 125 222 V3.8.0 (2002-03), retrieved from https://www.etsi.org/deliver/etsi_ts/125200_125299/125222/03.08.00_60/ts_125222v030800p.pdf
Ex. 1105	Internet Archive Capture, available at https://web.archive.org/web/20020613173206/http://webapp.etsi.org:80/key/key.asp?full_list=y
Ex. 1106	Internet Archive Capture, available at https://web.archive.org/web/20020531000359/http://www.3gpp.org:80/ftp/specs/archive/25_series/25.222/
Ex. 1107	Internet Archive Capture, available at https://web.archive.org/web/20020225110409/http://www.3gpp.org:80/TB/ran/ran1/specs.htm
Ex. 1108	Webpage, available at https://www.etsi.org/deliver/etsi_ts/125200_125299/125212/03.05.00_60/
Ex. 1109	ETSI TS 125.212 V3.5.0 (2000-12), retrieved from https://www.etsi.org/deliver/etsi_ts/125200_125299/125212/03.05.00_60/ts_125212v030500p.pdf
Ex. 1110	Internet Archive Capture, available at https://web.archive.org/web/20011020025720/http://etsi.org/getastandard/home.htm
Ex. 1111	Internet Archive Capture, available at https://web.archive.org/web/20011124215727/http://www.3gpp.org/ftp/Specs/archive/25_series/25.212/
Ex. 1112	Internet Archive Capture, available at https://web.archive.org/web/20020111012800/http://www.3gpp.org:80/ftp/Specs/archive/25_series/25.212/

Exhibit ("Ex.")	Description
Ex. 1113	3GPP TS 25.212 V3.5.0. (2000-12), in 25212-350.zip, retrieved from https://www.3gpp.org/ftp/Specs/archive/25_series/25.212/25212-350.zip
Ex. 1114	Internet Archive Capture, available at https://web.archive.org/web/20020802173135/http://www.3gpp.org/ftp/Specs/
Ex. 1115	Internet Archive Capture, available at https://web.archive.org/web/20020806031707/http://www.3gpp.org/ftp/Specs/archive/
Ex. 1116	Internet Archive Capture, available at https://web.archive.org/web/20020701091801/http://www.3gpp.org/ftp/specs/archive/25_series/
Ex. 1117	Internet Archive Capture, available at https://web.archive.org/web/20020531003232/http://www.3gpp.org/ftp/specs/latest/Rel-6/25_series/
Ex. 1118	Internet Archive Capture, available at https://web.archive.org/web/20020812090150/http://www.3gpp.org/ftp/Specs/latest/Rel-5/25_series/
Ex. 1119	TS 25.222 V3.8.0 (2002-03), in 25222-380.zip, retrieved from https://www.3gpp.org/ftp/Specs/archive/25_series/25.222/25222-380.zip

TABLE OF ABBREVIATIONS

3GPP-Summary	R1-01-1047, Ericsson 3GPP Submission (Ex. 1007)
'486	U.S. Patent No. 9,065,486 (Ex. 1001)
'486 FH	File History of U.S. Patent No. 9,065,486 (Ex. 1002)
Claims	Claims 1-6 of U.S. Patent No. 9,065,486
Hochwald	Declaration of Dr. Bertrand Hochwald in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 9,065,486 (Ex. 1003)
IDS	Information Disclosure Statement
IPR	<i>Inter Partes</i> Review
Motorola	R1-01-1014, Motorola 3GPP Submission (Ex. 1006) and R1-01-1081, Revised Motorola 3GPP Submission (Ex. 1087)
Petitioner	Petitioner LG Electronics Inc.
PO	Patent Owner Pantech Wireless, LLC
POSITA	Person of Ordinary Skill in the Art
PTAB	Patent Trial and Appeal Board
Rodermund	Declaration of Friedhelm Rodermund in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 9,065,486 (Ex. 1004)
Stewart	U.S. Patent No. 7,260,770 (Ex. 1005)
TS25.212	3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD) (Release 5) (3GPP TS 25.212 version 5.1.0) (Ex. 1008)
TS25.212-v3.5.0	3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD) (Release 1999) (3GPP TS 25.212 version 3.5.0) (Ex. 1036)
TS25.222	3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (TDD) (Release 1999) (3GPP TS 25.222 version 3.8.0) (Ex. 1011)
USPTO	United States Patent and Trademark Office

LIST OF CHALLENGED CLAIMS

[1.pre] An apparatus for use in wireless communications comprising:

[1.a] a first interleaver configured to interleave systematic bits;

[1.b] a second interleaver configured to interleave a first parity bit stream;

[1.c] a third interleaver configured to interleave a second parity bit stream;

[1.d] a buffer configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and

[1.e] a rate matching unit configured to select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.

[2] The apparatus of claim 1 wherein selecting of bits by the rate matching unit in response to a selected redundancy version changes in response to a location of the bits in the buffer.

[3.pre] A method for use in an apparatus of a wireless communications comprising:

[3.a] interleaving, by the apparatus, systematic bits;

[3.b] interleaving, by the apparatus, a first parity bit stream;

[3.c] interleaving, by the apparatus, a second parity bit stream;

[3.d] buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and

[3.e] selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.

[4.] The method of claim 3 wherein the selecting of bits for transmission in response to a selected redundancy version changes in response to a location of the bits in the buffer.

[5.pre] A wireless transmit/receive unit comprising:

[5.a] circuitry configured to interleave systematic bits;

[5.b] circuitry is further configured to interleave a first parity bit stream;

[5.c] circuitry is further configured to interleave a second parity bit stream;

[5.d] circuitry is further configured to buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and

[5.e] circuitry is further configured to select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.

[6.] The wireless transmit/receive unit of claim 5 wherein selecting of bits based on a selected redundancy version changes in response to a location of the bits in the buffer.

Pursuant to §§311-319 and §42.1,¹ Petitioner petitions for *inter partes* review (“IPR”) of claims 1-6 (“Claims”) of U.S. Patent No. 9,065,486 (Ex. 1001, “’486”), assigned to Pantech Wireless, LLC (“PO”). Petitioner requests review of the Claims, and judgment finding them unpatentable under §102 and §103.

I. INTRODUCTION

The ’486 Claims are directed to a technique for selecting between systematic bits or parity bits of cellular data for transmission. ’486, 4:60-5:13, 6:4-12, 6:26-51, 10:20-28, 18:15-55, 20:50-59. Systematic bits, also referred to as information bits, include data that is transmitted from a sending device to a receiving device. Hochwald, ¶46. A turbo coding process is applied to the systematic bits to generate parity bits that contain error correction information (“ECI”) about the data transmitted in systematic bits. The ECI is used to recover data corrupted during transmission. ’486, Fig. 2, 1:59-2:6; 6:13-19. The ’486 Claims additionally require interleaving the systematic bits and parity bits, and buffering the bits prior to selection to achieve a certain code rate for transmission. A higher code rate—

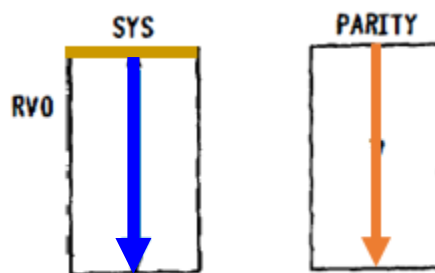
¹ Section cites reference 35 U.S.C. (pre-AIA) or 37 C.F.R. as context indicates. All emphasis/color annotations added unless noted. Figure annotations herein generally quote the Claims for reference. Citations herein are exemplary and not meant to be limiting.

e.g., using more systematic bits than parity bits—increases transmission bit rate at the expense of reliability. *Id*; Hochwald, ¶48.

The '486 “Summary of the Invention” describes a “two stage” rate matching process that implements an “incremental redundancy” (“IR”) process ('486, 4:60-5:8), which sends different amounts of data bits to achieve different code rates—i.e., different ratios of systematic bits to total (parity and systematic) bits. Ex. 1009; Hochwald, ¶47. This IR supports a hybrid automatic repeat request (“HARQ”) process that resends portions of systematic bits and parity bits to a receiver to facilitate delivery of information. '486, 4:60-5:8; Hochwald, ¶48. HARQ uses different “code rates” based on the quality of a channel—lower code rates for poor channel conditions with more errors, and higher code rates for better channel conditions with fewer errors. '486, Figs. 1-2, 1:35-2:36, 3:10-32, 8:28-58, 13:17-36; Hochwald, ¶48.

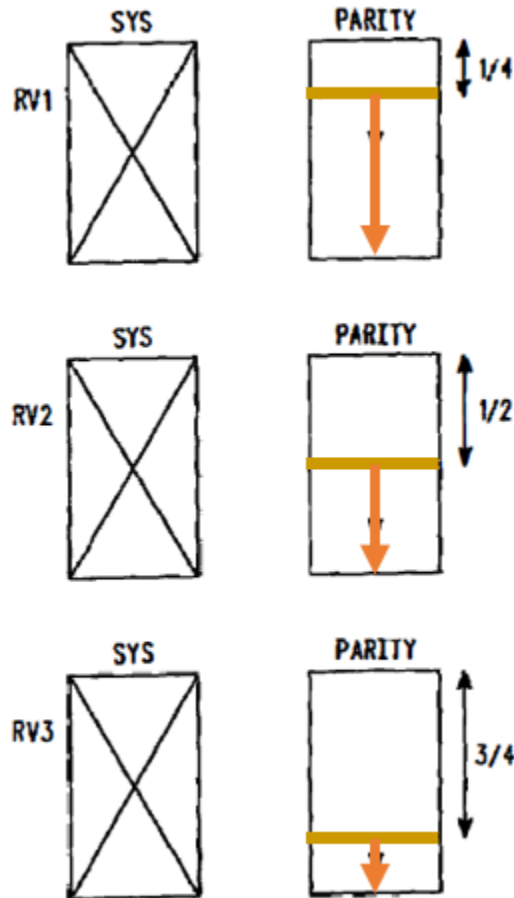
Based on the '486's summary, the purportedly novel aspect of the Claims is selecting between systematic bits and parity bits to obtain different code rates during transmissions to support IR. See '486, 4:60-5:8; Hochwald, ¶49. Different numbers of systematic and parity bits are transmitted based on whether systematic bits were successfully recovered from a prior transmission. *Id*.

But this selecting process was known in the art. Indeed, the European Patent Office previously rejected similar claims in a counterpart application over **TS25.212** (Ex. 1008), observing that “large parts” of the ’486 had been copied from **TS25.212** without attribution. Ex. 1010, 14-16; **TS25.212**, Fig. 17, §4.5.4(58-60); ’486, Fig. 10, 16:10-26, 16:52-17:10, 18:10-19:13. Additionally, **Stewart** (Ex. 1005) discloses selecting between a “Systematic” bit stream and two “Parity” bit streams based on a redundancy version parameter. Stewart, Figs. 3-4, 6, 3:1-12, 3:64-4:45, 5:57-7:24, 9:65-10:1. For example, **Stewart** discloses a redundancy version (“RV0”) that selects **systematic bits** over **parity bits** by either selecting **systematic bits** before **parity bits** for transmission (e.g., as indicated by the **starting point** in a systematic interleaver), or by selecting more **systematic bits** than **parity bits** for transmission:



Stewart, Fig. 6, 6:57-61; Hochwald, ¶49. Such selection of **systematic bits** over **parity bits** is used, for example, in good channel conditions with fewer errors. **Stewart** further teaches additional redundancy versions (“RV1”-“RV3”) that select

parity bits over systematic bits by either selecting parity bits starting from different starting points in a parity interleaver, or selecting more parity bits than systematic bits:



Stewart, Fig. 6, 5:33-36, 6:5-52, 6:62-7:4; Hochwald, ¶50.

If additional detail is required, **Motorola** (Ex. 1006/Ex.1087), **3GPP-Summary** (Ex. 1007), and **TS25.212** provide additional detailed teachings of, e.g., buffering systematic bits and parity bits in a “buffer,” and selecting between systematic bits and parity bits based on redundancy versions. Hochwald, ¶¶51-54.

Claims 1-6 are thus anticipated and rendered obvious by **Stewart** alone and/or in view of **Motorola**, **3GPP-Summary**, and/or **TS25.212**. Petitioner requests that the Board institute trial and find the Claims unpatentable.

II. MANDATORY NOTICES

A. Real Parties-in-Interest

Petitioner LG Electronics Inc. and LG Electronics U.S.A., Inc. are the real parties-in-interest. No other party had access to or control over the present Petition, and no other party funded or participated in preparation of the present Petition.

B. Related Matters

The '486 is the subject of the following co-pending civil action: *Pantech Corporation et al. v. LG Electronics Inc. et al.*, No. 5:22-cv-00113-RWS-JBB (E.D. Tex.) (“Texas Case”).

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Petitioner consents to electronic service of documents to the email addresses
of the counsel identified above.

III. PAYMENT OF FEES

The undersigned authorizes the Office to charge the fee required by
§42.15(a) and any additional fees that might be due to Deposit Account No. 18-
1945, under Order No. 104537-0034-652.

IV. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Pursuant to §42.104(a), Petitioner certifies that the '486 is available for IPR. Petitioner and any real parties-in-interest are not barred or estopped from requesting IPR challenging the claims on the grounds identified herein.

B. Identification of Challenge

Pursuant to §§42.104(b)-(b)(1), Petitioner requests IPR of claims 1-6, and that the Board cancel the same as unpatentable.

1. Specific Art on Which the Challenge Is Based

Petitioner relies on the following prior art:

Name	Publication/ Title	Ex.	Filed	Published/ Issued	Prior art under at least
Stewart	US7,260,770	1005	10/22/2001	8/21/2007	§102(e)
Motorola ²	R1-01-1014/ R1-01-1081	1006		By 1/2002	§§102(a)/(b)
3GPP- Summary	R1-01-1047	1007		By 1/2002	§§102(a)/(b)

² While both are publicly accessible, this petition relies on two versions of Motorola that are substantively the same. See Ex. 1088. Citations below apply equally to R1-01-1014 (Ex. 1006) and R1-01-1081 (Ex. 1087).

Name	Publication/ Title	Ex.	Filed	Published/ Issued	Prior art under at least
TS25.212	TS25.212 v5.1.0	1008		By 12/15/2002	§102(a)

Hochwald, ¶¶93-101.

Each of **Motorola**, **3GPP-Summary**, and **TS25.212** was publicly accessible to, and accessed by POSITAs and interested persons well before the '486's earliest alleged priority date, 12/16/2002.³ Ex. 1004 (“**Rodermund**”), ¶¶1-181; Exs. 1051-1119. **Motorola** and **3GPP-Summary** are proposals submitted to the 3rd Generation Partnership Project (“3GPP”) Working Group 1 (“WG1”) that helped develop the Universal Mobile Telecommunications System (“UMTS”) or 3G standard. Motorola, 1; 3GPP-Summary, 1; Rodermund, ¶¶84-118. **TS25.212** and related TS25.212-v3.5.0 (Ex. 1036), and TS25.222 (Ex. 1011) are technical specifications maintained by 3GPP that describe UMTS/3G. As summarized below, each reference was published and publicly available on 3GPP's ftp server and/or the ETSI server, cited by multiple publications, presented publicly, and/or

³ All prior art in the Grounds predates the earliest provisional to which the '486 claims priority (60/434,232 filed 12/16/2002). Exs. 1002, 1016-1019.

distributed via email reflector or meeting without restriction or expectation of confidentiality. Rodermund, ¶¶119-179; *see Apple v. Uniloc 2017 LLC*, IPR2019-00222, Pap. 28, *13-18; *LG Electronics, Inc. v. Core Wireless Licensing S.A.R.L.*, IPR2015-01986, Pap. 34, *26-31; *Samsung Electronics Co., Ltd. v. Ibex PT Holdings Co., Ltd.*, IPR2018-00011, Pap. 33, *4.

Reference	3GPP Published	ETSI Published	3GPP Meeting Availability	Email Distribution	Citing Pubs.
Motorola	1/28/2002 ⁴		By 11/7/2001 ⁵	10/23/2001 ⁶	7/2002 ⁷
3GPP-Summary	1/28/2002 ⁸		By 11/7/2001 ⁹		
TS25.212	6/28/2002 ¹⁰	7/9/2002 ¹¹			By 12/15/2002

⁴ Ex. 1073.

⁵ *See* substantively similar R1-01-1081 (presented at meeting). Exs. 1087-1088; Rodermund, ¶¶100-102.

⁶ Ex. 1075.

⁷ Ex. 1089.

⁸ Ex. 1073.

⁹ Ex. 1086 (presented at meeting); Rodermund, ¶¶115-117.

¹⁰ Ex. 1092.

Reference	3GPP Published	ETSI Published	3GPP Meeting Availability	Email Distribution	Citing Pubs.
					¹²
TS25.212- v3.5.0	1/2/2001 ¹³	2/12/2001 ¹⁴			
TS25.222	3/29/2002 ¹⁵	4/22/2002 ¹⁶			

¹¹ Ex. 1093; See ETSI's substantively identical TS 125.212. Ex. 1094; Rodermund, ¶122-125.

¹² Exs. 1100-1101.

¹³ Ex. 1092.

¹⁴ Ex. 1108.

¹⁵ Ex. 1102.

¹⁶ Ex. 1103; See ETSI's substantively identical TS 125.222. Ex. 1104; Rodermund, ¶¶164-167.

2. Statutory Grounds on Which the Challenge Is Based

Ground	Basis	Claims	References
1	§102, §103	1-6	Stewart
2	§103		Stewart in view of 3GPP-Summary
3			Stewart in view of TS25.212
4-6			Grounds 1-3 in further view of Motorola

V. '486 PATENT AND PROSECUTION HISTORY

As discussed in §I, the '486 Claims are directed to selecting between systematic and parity bits for transmission in a user device or base station. '486, 1:40-46, 4:60-5:13, 6:4-51, 10:20-28, 18:15-55, 20:50-59; Hochwald, ¶55. Whereas systematic bits carry data, parity bits are generated from the systematic bits through a channel coding process and carry data and error control information ("ECI"). A receiver uses the ECI to detect and correct errors in received data. '486, 2:59-67, 14:54-64; Hochwald, ¶55.

The '486 describes selecting systematic bits over parity bits for transmission or vice-versa based on a redundancy version. '486, 6:31-47, 10:20-28, 18:15-55, 20:50-59; Hochwald, ¶56.

The Claims also require interleaving the systematic bits and parity bits, and buffering the bits. '486, Figs. 2, 10, 1:59-2:49, 6:26-47, 11:7-25, 20:32-41. Interleaving is a conventional process of rearranging the order of bits prior to transmission in a known manner that is reversed at a receiver. '486, Fig. 2, 1:59-2:6, 3:18-32, 11:7-25, 20:38-21:2; Ex. 1012 ("Shibutani"), 1:9-16, 44-48, Figs. 1-50; Ex. 1013 ("Huang"), 1:7-9, 26-48; Hochwald, ¶57. Rearranging the order of bits makes interference during transmission less likely to affect continuous portions of the data by spreading out effects of interference across the pre-interleaved sequence, improving the effectiveness of error correction. '486, 3:18-32, 6:64-7:3, 10:20-28, 11:7-25, 11:26-42, 12:10-19, 21:53-22:30; Shibutani, 1:9-16, 44-48, Figs. 1-50; Huang, 1:7-9, 26-48; Hochwald, ¶57.

Fig. 2, which the '486 concedes is prior art copied from TS25.222 (Ex. 1011) ('486, 1:59-2:6), and Fig. 10, which the '486 copied from **TS25.212** (Fig. 17; §IX.C) illustrate a claimed embodiment. Hochwald, ¶58. Fig. 2 shows prior art processing of data that includes **channel coding**, **interleaving**, and **rate matching**. '486, Fig. 2; Hochwald, ¶58. The **channel coding** outputs a systematic bit stream and two parity bit streams generated from the systematic bit stream. *Id.*; '486, 1:59-3:5, 14:61-64. The systematic and parity bit streams are processed by

interleaving. *Id.*; '486, 20:39-21:2. The interleaved bits are then passed to **rate matching**. '486, 1:59-2:6; Hochwald, ¶158.

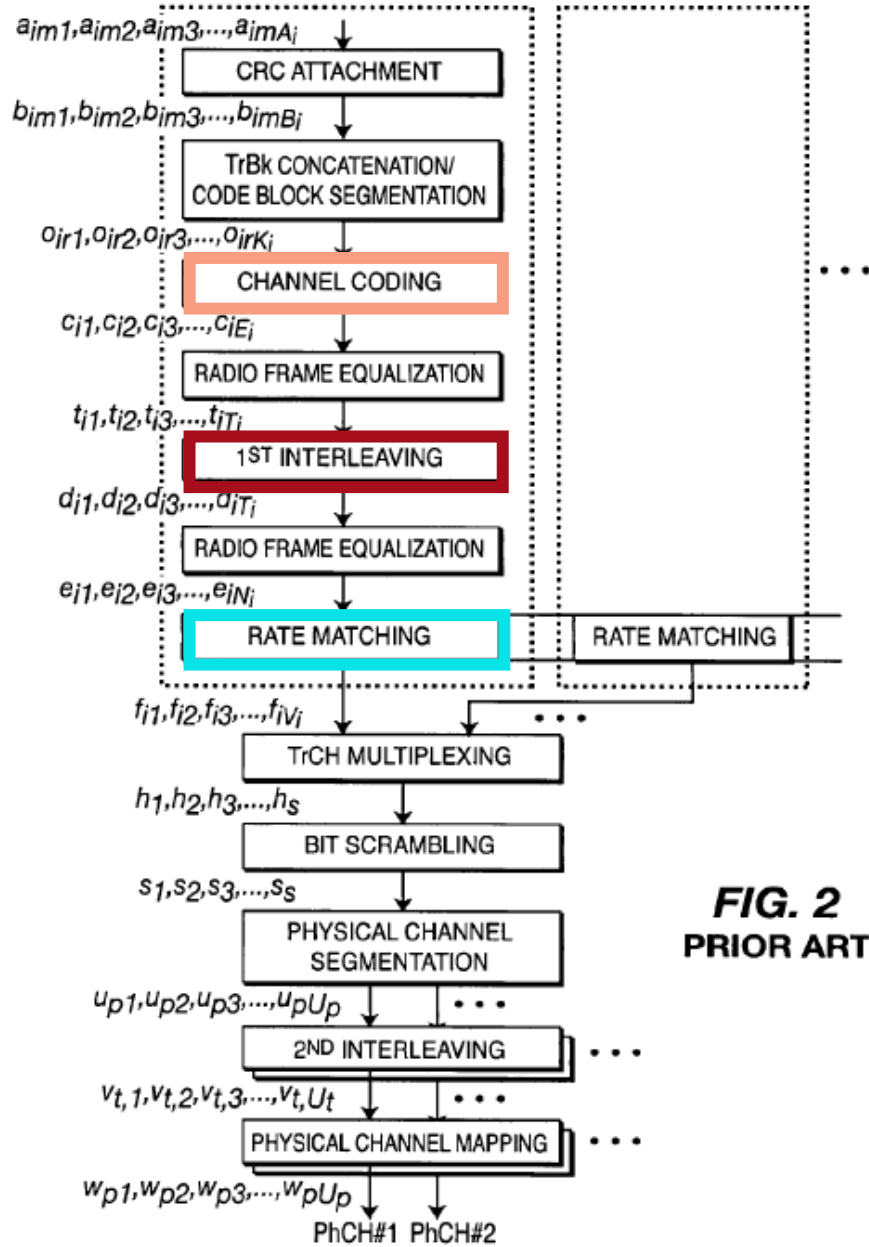


Fig. 10, which the '486 copied from prior art TS25.212¹⁷, shows the claimed rate matching:

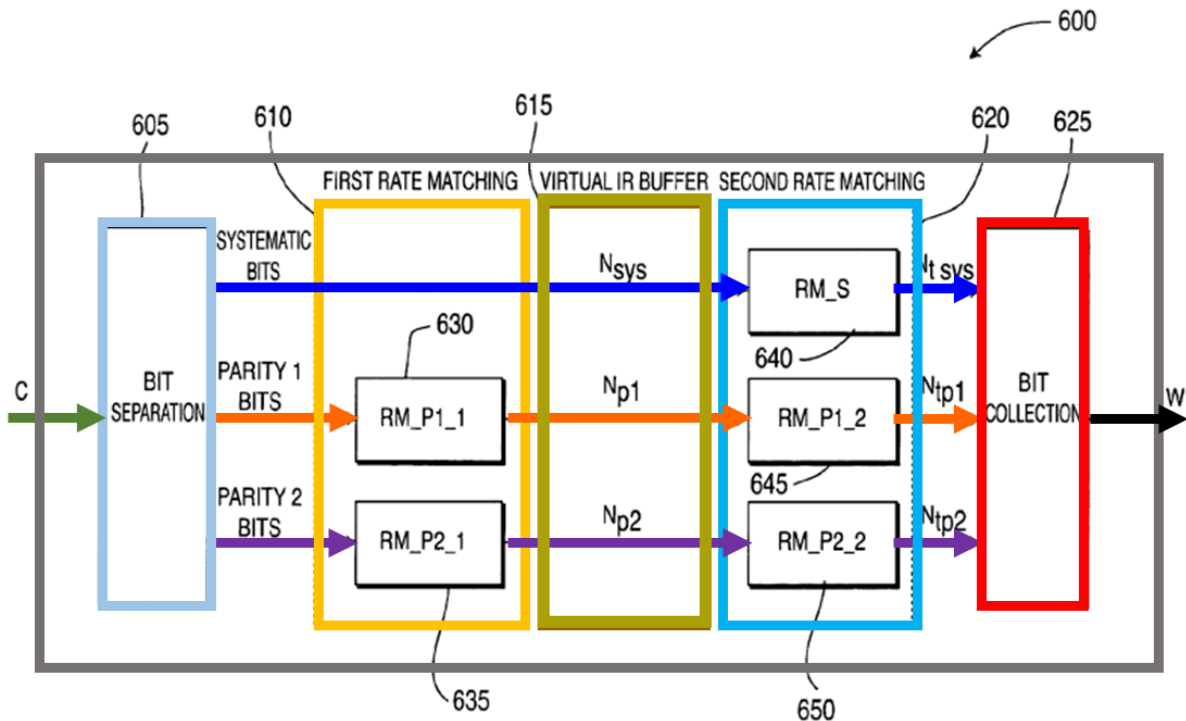


FIG. 10

A **bit separation circuit** separates a **signal** input into a **systematic bit stream**, a **first parity bit stream**, and a **second parity bit stream**. '486, 6:31-45, Fig. 10; Hochwald, ¶59. The **first rate-matching stage** performs a first puncturing operation (e.g., dropping of bits) on the parity bit streams, if needed, to fit the bit streams into the size of the **virtual incremental redundancy (IR) buffer**. '486,

¹⁷ Compare Fig. 10 of '486 with Fig. 17 of TS25.212.

5:5-7, 6:26-51, 8:16-20, 12:30-36, 16:19-23, Fig. 10; *see also* Honkasalo (Ex. 1014), [0039]; Chen (Ex. 1015), 4:50-56; Hochwald, ¶60. The three bit streams are then buffered in the **virtual IR buffer**. '486, Fig. 10, 4:60-5:8, 6:23-51, 8:16-27, 12:1-9, 12:30-36; Hochwald, ¶¶60-61. The **second rate matching stage** selects either systematic bits over parity bits for transmission, or vice-versa, based on a redundancy version setting. '486, 6:26-40, 16:24-26, 18:15-20:20, Tables 1-2, Fig.10; Hochwald, ¶61. The selected bits from the **second rate matching stage** are combined in the **bit collection circuit** into an **output** for transmission. '486, 6:40-47, 16:38-39, Fig. 10; Hochwald, ¶61.

The '486 Claims thus recite features described in disclosures copied from the prior art, and recite implementing these features in only a conventional manner. Hochwald, ¶62. Accordingly, **Stewart** alone or in view of **Motorola, 3GPP-Summary** and/or **TS25.212** therefore anticipates and renders obvious the '486 Claims. Stewart, 3:47-63, Fig. 2; Hochwald, ¶62.

The sole rejection of the Claims was on double-patenting grounds, and was overcome via a terminal disclaimer, resulting in allowance. *See* Ex. 1002

(“’486FH”), 86-91 (O.A.), 103-109 (Resp.), 118-119 (Allowance); Hochwald, ¶¶63-64; Ex. 1046.¹⁸

VI. §325(D) AND §314(A) DISCRETION DOES NOT APPLY

A. §325(d)

Under the two-part *Advanced Bionics* framework, the Board should not exercise discretion.

The grounds raised by this Petition are not the same or substantially the same as the art and arguments raised during ’486’s prosecution. Stewart, Motorola, and 3GPP-Summary were not substantively considered during prosecution. Though the Applicant identified **TS25.212** in an IDS, the Examiner did not substantively discuss or rely on **TS25.212** in any rejection of the Claims, or consider its teachings in the combinations set forth in this Petition—indeed, there were no prior-art based rejections at all. *See* ’486FH, 76, 100; *Sony v. MZ Audio Scis., LLC*, IPR2022-01544, Pap. 12, *7 (§325(d) discretion improper where “Examiner did not consider the specific combination of references asserted”). The specification’s citations to additional references (’486, 1:35-4:30) do not include

¹⁸ Parent prosecution histories likewise did not discuss features relevant to the Claims. *See* Exs. 1016-1019.

the same teachings discussed in the Grounds. As explained below, the Claims are anticipated and obvious under the identified Grounds. *See* §IX.

Even if the art or arguments were substantially the same, the Examiner would have erred in a manner material to the patentability of the Claims. Because the Examiner did not issue any rejections based on any of the cited art in this petition it is “impossible ... to determine the consideration the Examiner gave” to any cited reference; “the absence of further evidence of the Examiner’s consideration of” the art supports finding that “the Office erred in a manner material to patentability.” *Ecobee Techs. v. Causam Enterprises, Inc.*, IPR2022-01339, Pap. 20, *20-21 (declining §325(d) discretion); *Liquidia Techs., Inc. v. United Therapeutics Corp.*, IPR2021-00406, Pap. 18, *19 (cited prior art “was not the basis for a rejection and was not evaluated substantively at all during examination,” favoring a finding of “material error by the Office”). Even if any of the art considered by the USPTO was substantially similar to these references (none is), the Examiner would have erred in allowing the Claims. Had the Examiner considered references that taught (as these references do) interleaving systematic and parity bits, buffering said bits, and selecting the systematic bits over parity bits or vice versa based on a redundancy version, the Examiner would have erred in failing to reject the Claims over such art.

Accordingly, the Board should not exercise its §325(d) discretion to deny institution.

B. §314(a)

The co-pending litigation also does not warrant exercising discretion under §314(a) based on the *Fintiv* factors.

1: Following institution, Petitioner intends to seek a stay of the Texas Case pending the outcome of this IPR.

2: Though the Texas Case's trial is currently set for 7/29/2024¹⁹, based on median time to trial before the presiding judge over the last 5 years, trial is expected 26 months²⁰ from the 9/2/2022 filing date, in late 11/2024 (median time to trial in the district varies between 19 and 24 months over the last few years)²¹.

3: The Texas Case is in its early stages; the court has not ruled on the initial motion to dismiss and discovery has just begun.

¹⁹ Ex. 1022.

²⁰ Ex. 1023.

²¹ Ex. 1024.

4: This IPR challenges claims 1-2 and 5-6, which are unasserted in the Texas Case. Moreover, after the final written decision, the same grounds and arguments could not be presented in the litigation.

5: The litigation and PTAB parties are the same.

6: The merits of this Petition are compelling as shown herein—e.g., **Stewart** anticipates and renders obvious the Claims and the PO copied portions of **TS25.212** into the specification without attribution. See §IX.

VII. LEVEL OF ORDINARY SKILL

For purposes of this Petition only, Petitioner assumes the Claims are entitled to the '486's earliest provisional application filing date, 12/16/2002. Regardless of whether the '486 is entitled to a 12/16/2002 priority date based on its earliest provisional application, each of **Stewart**, **Motorola**, **3GPP-Summary**, and **TS25.212** are prior art to the Claims in any event. Hochwald, ¶65.

A person of ordinary skill in the art ("POSITA") as of the alleged priority date of the '486, 12/16/2002, would have had a bachelor's degree in electrical and computer engineering, computer science, or the equivalent thereof, and at least two years of experience with networking and wireless communication systems. Hochwald, ¶¶66-68. More education can supplement practical experience, and

vice-versa. '486, 1:26-4:49. PO has not yet provided a level of skill of a POSITA for the '486.

VIII. CLAIM CONSTRUCTION

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). §42.100(b). Only terms necessary to resolve the controversy need construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Because the prior art asserted herein discloses embodiments within the Claims' indisputable scope, the Board need not construe the Claims' outer bounds. All claim terms should be construed according to their plain and ordinary meaning. Neither party has proposed constructions for the '486. Ex. 1047; Hochwald, ¶¶69-70.

Regardless of whether the preambles are limiting, the prior art discloses the preambles. See §IX; Hochwald, ¶71. The limitations of [1.e] and [5.a]-[5.e] are not written in means-plus-function format and are not means-plus-function limitations covered by §112 ¶6, but are disclosed in the prior art for the reasons discussed in §IX, based on disclosures of **Stewart** alone and in view of **Motorola, 3GPP Summary**, and/or **TS25.212**. Moreover, [1.e] includes components that connote structure (e.g., “rate matching unit”), and a POSITA would have understood that the “circuitry” required by [5.a]-[5.e] were implemented using

well-known components (e.g., “interleaver,” “buffer,” or “rate matching unit”), or alternatively connoted structure. See ’486, 6:26-58, 18:15-22, Figs. 2, 10; *Interleavers* (U.S. 6,631,491, (Shibutani) 1:9-16, 44-48, 27:47-28:5, Figs. 1-50; U.S. 5,537,420, (Huang) 1:7-9, 26-48, 5:58-6:40, 8:51-60, Fig. 2); *Buffers* (Ex. 1025; Ex. 1026; 3GPP-Summary, §2.4; Ex. 1010, 14-16; TS25.212, Fig. 17, 59-60; U.S. 2005/0094667A1 (“Dahlman-667”, Ex. 1027) Fig. 9, [0030]); *Rate Matching* (U.S. 7,372,837 (“Kinjo,” Ex. 1028) 2:12-43, 2:62-3:7, 14:41-15:3; TS25.212, p.59; U.S. 7,000,173 (“Buckley,” Ex. 1029) 4:17-34); *Circuitry* (U.S. 7,020,455 (“Krishnarajah,” Ex. 1030) Fig. 7A, 7:5-22; U.S. 6,760,365 (“Demir”, Ex. 1031) Fig. 3; 2:50-59, 3:4-24, 4:11-44; E.P. 1209856A1 (“Miya”, Ex. 1032) Fig. 7, [0039]-[0051]); Hochwald, ¶¶72-84. Additionally, the PTAB has construed “circuit configured to” claim limitations according to their plain and ordinary meaning, rather than as means-plus-function limitations. *Diablo Techs., Inc. v. Netlist, Inc.*, IPR2014-00882, Pap.11, *11-12.

Out of an abundance of caution, if limitations [1.e] and [5.a]-[5.e] were determined to be means-plus-function terms (they are not) and additional specification structure were necessary to meet these limitations, Petitioner identifies corresponding structure and function for said limitations in order to comply with §42.104(b)(3). Summarized in the table below are the corresponding

structure and equivalents, and function of each limitation as disclosed by the '486. Hochwald, ¶85.

Limitation (with function emphasized)	Structure
[5.a] circuitry configured to <i>interleave systematic bits;</i>	interleaver (1:66-2:3, 11:12-25, Fig. 2)
[5.b] circuitry is further configured to <i>interleave a first parity bit stream;</i>	
[5.c] circuitry is further configured to <i>interleave a second parity bit stream;</i>	
[5.d] circuitry is further configured to <i>buffer the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and</i>	buffer (6:26-52, 16:17-26, Fig. 10)
[1.e]/[5.e] [a rate matching unit/circuitry is further] configured to <i>select bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.</i>	second rate matching stage (6:26-52, Fig. 10) / “microprocessor circuitry” (6:26-58) with algorithm for selecting systematic bits and parity bits (18:10-55)

If PO attempts to improperly read additional structure from the specification beyond that disclosed by the art discussed herein into each of the Claims' limitations, that additional structure would also go beyond the claimed structure required to perform the recited function. Regardless, the art discloses the claimed structure expressly, and under the doctrine of equivalents by performing substantially the same functions, in substantially the same way, to achieve the

same result as shown in §IX, and the table below. Hochwald, ¶85. With respect to each of **Stewart**, **3GPP-Summary** and **TS25.212**, a POSITA would have understood, or at least found it obvious that a UE, mobile station, BS, or other device operating in a wireless environment includes a processor, in the same manner as the '486. '486, 4:60-5:12; Ex. 1033, 3:41-45; Ex. 1034, 2:63-67, 4:57-5:5; Ex. 1035, 7:51-67, Fig. 3; Hochwald, ¶85. To the extent PO argues that the disclosures of **Stewart**, **3GPP-Summary** and **TS25.212** are limited to downlink functionality, a POSITA would have found it obvious to modify the teachings of **Stewart**, **3GPP-Summary** and **TS25.212** for an uplink, and would have had a reasonable expectation of success in doing so. A POSITA would have been motivated to use the aforementioned teachings that support incremental redundancy in an uplink connection because incremental redundancy also improves performance in an uplink direction. For example, Kinjo teaches that the advantages of a rate matching process that supports IR in a downlink “may also be used during an uplink transmission” even though “there is no real demand to increase the throughput during an uplink transmission” and that such process was “equally applicable to an uplink transmission.” Kinjo, 6:55-64. Hochwald, ¶¶86-92.

Limitation	Stewart (Express Disclosure)	DOE Analysis
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[5.a]	“systematic block interleaver” (Figs. 4-5, 4:14-5:5);	Stewart’s “[systematic / parity] block interleaver” performs the same interleaving function (<i>see</i> ’486 [5.a]-[5.c]) in substantially the same way (e.g., reading data in and reorganizing the bits) as the ’486 to achieve the same result of interleaved bits.
[5.b]	“parity block interleaver” (Fig. 4-5, 4:14-5:5)	
[5.c]		
[5.d]	“block matrix” (4:14-5:5; Fig. 5)	Stewart’s “block matrix” performs the same buffering function (<i>see</i> ’486 [5.d]) in substantially the same way (e.g., storing bits) as the ’486 to achieve the same result of stored bits.
[1.e]/[5.e]	“redundancy version selector” (2:25-26, 3:64-4:13, 5:57-13:13, Fig. 3) UE processor performing selecting algorithm (2:25-26; 3:64-4:13, 5:57-9:13; Fig. 3)	Stewart’s “redundancy version selector” and UE processor perform the same selecting function (<i>see</i> ’486 [1.e]/[5.e]) in substantially the same way (e.g., by selecting systematic and parity bits for transmission based on a redundancy version) as the ’486 to achieve the same result of selected bits for transmission.

Limitation	3GPP-Summary	DOE Analysis
[5.d]	“buffering memory,” “buffer,” “ring buffer,” “transmitter buffer” that stores “interleaved [systematic/parity] bits” (§2.4)	3GPP-Summary’s “buffer” performs the same buffering function (<i>see</i> ’486 [5.d]) in substantially the same way (e.g., by storing bits) as the ’486 to achieve the same result of stored bits.

Limitation	TS25.212 ²²	DOE Analysis
[5.d]	“Virtual IR buffer” (§4.5.4, Fig. 17)	TS25.212’s “Virtual IR buffer” performs the same buffering function (see ’486 [5.d]) in substantially the same way (e.g., by storing bits) as the ’486 to achieve the same result of stored bits.
[1.e]/[5.e]	“second rate matching stage” circuitry (§4.5.4, Fig. 17); UE processor performing selecting algorithm (§4.5.4.3)	TS25.212’s “second rate matching stage” and UE processor perform the same selecting function (see ’486 [1.e]/[5.e]) in substantially the same way (e.g., selecting systematic and parity bits for transmission based on a redundancy version) as the ’486 to achieve the same result of selected bits for transmission.

IX. GROUNDS OF UNPATENTABILITY

This Petition is supported by the Declaration of Dr. Bertrand Hochwald, which describes the prior art’s scope and content at the time of the ’486. The prior art renders the Claims unpatentable based on six grounds. Hochwald, ¶¶1-45.

A. Ground 1: Stewart

Stewart anticipates and renders obvious each of the Claims. Hochwald, ¶102.

²² The ’486’s disclosures of [5.d] and [1.e]/[5.e] (16:10-26, 16:66-17:2, 18:15-19:13, Fig. 10) are copied from **TS25.212** (§§4.5.4, 4.5.4.2–4.5.4.3, Fig. 17).

1. Overview of Stewart

Stewart is directed to a process that selects between systematic bits and parity bits for transmission based on a “redundancy” version parameter. Stewart, 1:44-64, 3:25-36, 4:14-19, 5:57-7:24; Hochwald, ¶103. Stewart discloses channel coding in Fig. 1 (excerpted below) and Fig. 4 (discussed further below) that outputs **systematic bits** (e.g., b_k), and **first parity bits** (e.g., p_{1k}) and **second parity bits** (e.g., p_{2k}) that are generated from the **systematic bits**. Stewart, 1:32-43, Fig. 1; Hochwald, ¶103.

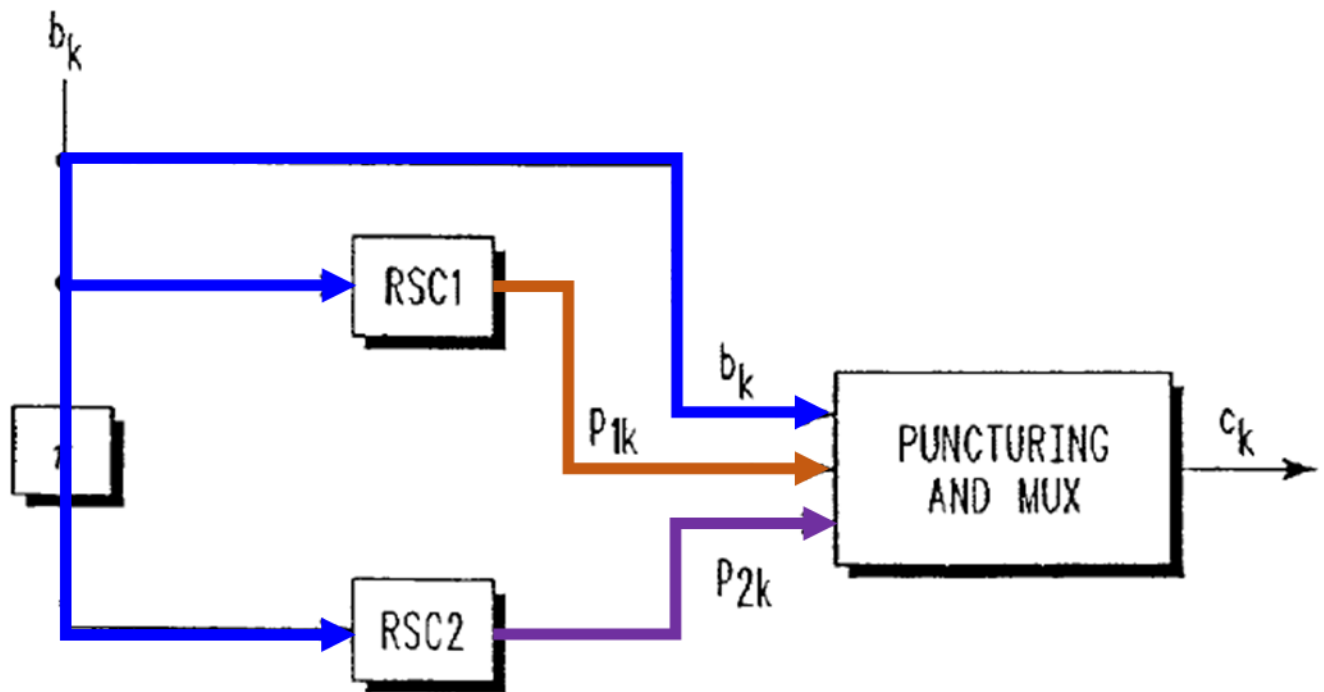
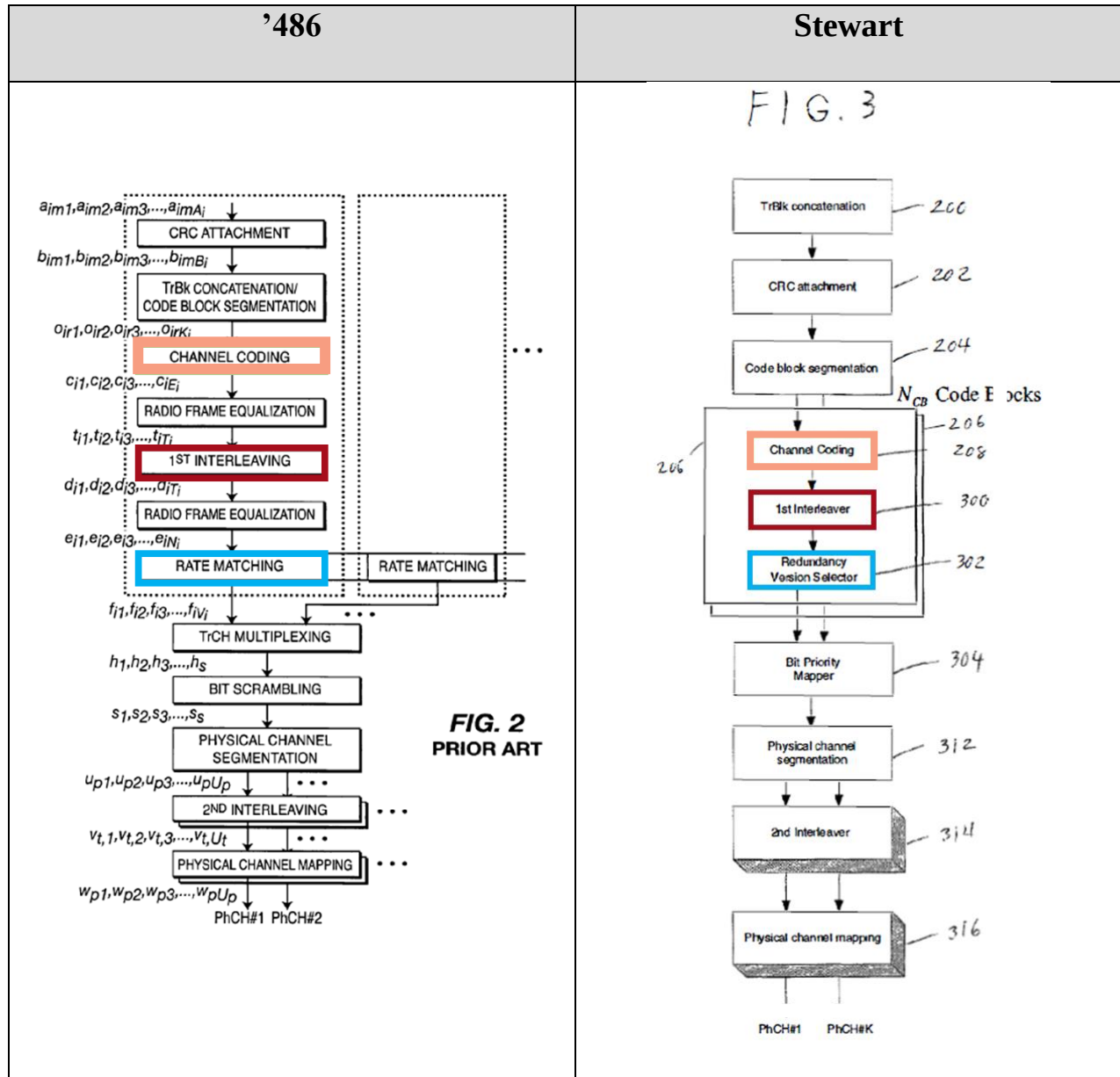


FIG. 1
- PRIOR ART -

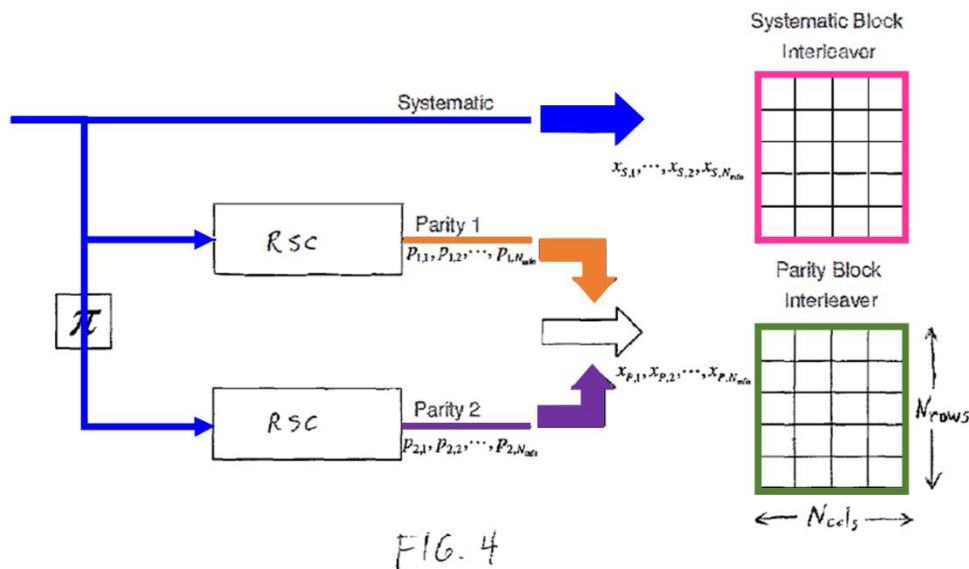
The parity bits support error correction in an IR process to transmit different numbers of systematic bits and parity bits to achieve different code rates. Stewart, 1:32-64, 2:60-64, 3:25-30, 5:6-8, 5:33-40, 7:55-62. The numbers of selected systematic bits and parity bits depend on a starting point in memory from which the systematic bits and parity bits are read, and how many of those bits are punctured (e.g., dropped). Stewart, Fig. 3, Abstract, 1:32-64, 2:45-67, 3:64-4:13, 4:56-5:5, 5:62-65, 6:41-49, 6:56-7:24; Hochwald, ¶104.

Stewart, like the '486, is based on a version of 3GPP TS 25.212 (v3.5.0) and related disclosures. Stewart, 3:47-63, Fig. 2; Ex. 1036, Fig. 1; '486, Fig. 2; TS25.212, Fig. 1; Hochwald, ¶105. As shown in the comparison of **Stewart's** Fig. 3 and the '486's Fig. 2, **Stewart** discloses to a POSITA processes and structure that support selection of systematic bits and parity bits for transmission that are substantially the same as the '486 including: (1) interleaving **systematic bits**, **first parity bits** and **second parity bits** output from a **channel coding** process, (2) buffering the bits in the **interleaver** and (3) selecting by a **redundancy version selector** portions of **systematic bits**, **first parity bits** and **second parity bits** to form a codeword for transmission based on a set of redundancy versions. Stewart, Abstract, 3:7-12, 3:64-4:55, 5:57-6:56, Figs. 3-6; Hochwald, ¶106.



As shown in Fig. 4, **Stewart** discloses that an input data stream is processed into **systematic bits** and a **“Parity 1” bit stream** and a **“Parity 2” bit stream** generated from the **systematic bits**. Hochwald, ¶107. The bits are read into corresponding block interleavers: a **“Systematic Block Interleaver”** for the

systematic bits and a “**Parity Block Interleaver**” for each parity bit stream. Stewart, 4:14-29, Fig. 4; Hochwald, ¶107. Although **Stewart’s** Fig. 4 illustrates one parity block interleaver, **Stewart** expressly teaches an instance where “separate ... parity block interleavers are used for each parity stream.” Stewart, 4:19-23. Interleaving (as depicted in Fig. 4) includes at least loading the bits into the block matrix, and rearranging the bits within the block matrix to reorder the bits for output. Stewart, 4:56-5:5. The interleaved bit streams are stored in the block matrix of the corresponding block interleaver. Stewart, 4:14-5:8, 5:47-56, Figs. 4, 5, 11; Hochwald, ¶107.



Following the interleaving and buffering in storage, different numbers of systematic bits and parity bits are selected from **Stewart’s** interleavers for transmission based on one of several redundancy version parameters set at the

transmitting device. Stewart, Figs. 5, 11, 5:6-8, 9:39-56; Hochwald, ¶108. **Stewart** discloses that each redundancy version specifies a **starting point** within a block matrix memory of the **systematic block interleaver**, or **parity block interleavers** from which to read bits for transmission. Stewart, 5:62-65, 6:52-7:25; Hochwald, ¶108.

For example, with reference to Fig. 6, Stewart teaches redundancy versions associated with a **starting point** located inside a **systematic block interleaver** (e.g., “RV0”) or one of a **[first/second] parity block interleaver** (e.g., “RV1,” “RV2,” and “RV3”).²³ Stewart, 6:62-7:24, Fig. 6; Hochwald, ¶109. **Stewart** teaches that if the desired number of bits to be read out is not reached when reading approaches the last row in an interleaver, reading wraps around to the first line of another block interleaver. Stewart, 5:6-15, 5:33-40. 5:50-52, 5:57-6:52; Hochwald, ¶109.

²³ Although Fig. 6 illustrates one parity interleaver, Stewart discloses using two “separate” “parity block interleavers” “for each parity [1 and 2] stream” as an alternative. Stewart, 4:19-23.

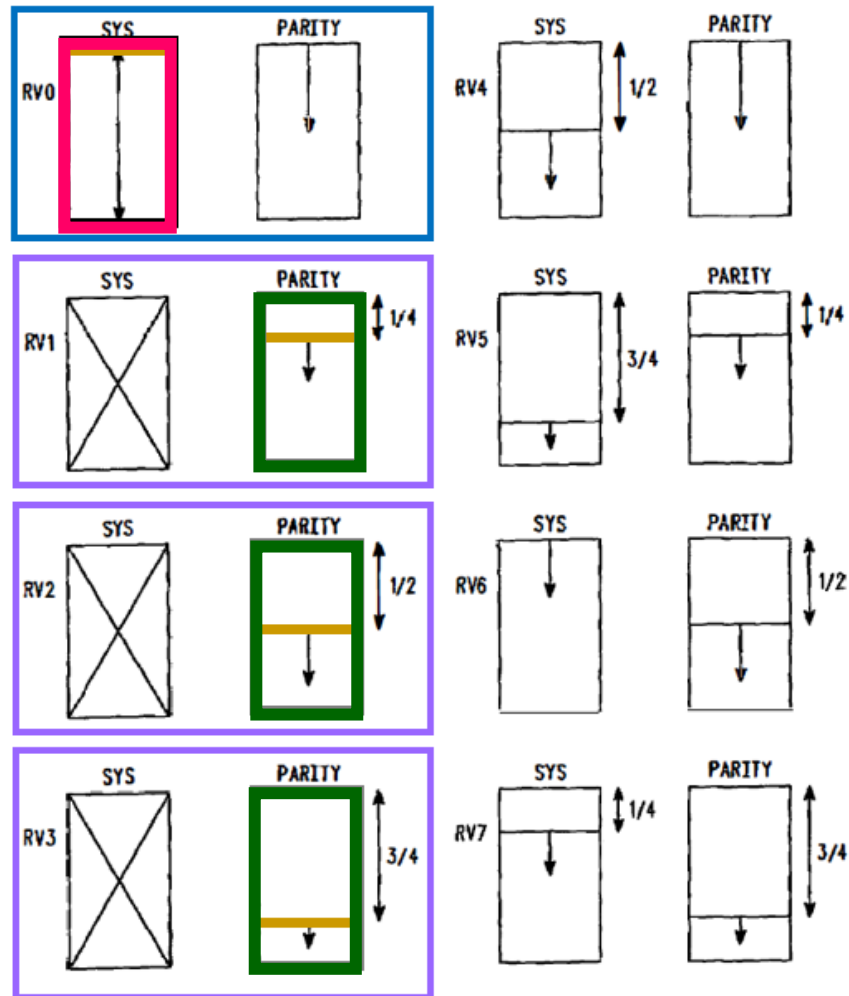
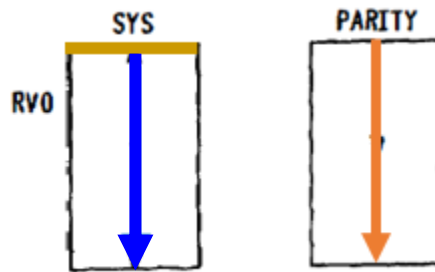


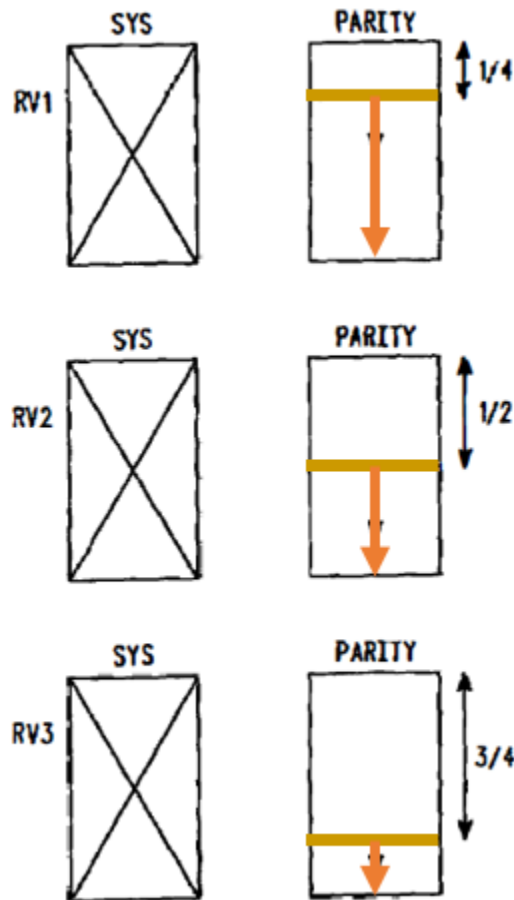
FIG. 6

Stewart teaches a redundancy version in which systematic bits are transmitted before parity bits. As shown below, in RV0, all **systematic bits** are first read before reading **parity bits**. Stewart, 6:57-61; Hochwald, ¶110.



Stewart also teaches selecting more systematic bits for transmission than parity bits—for example when RV_0 , is “signaled with enough codeword bits to result in a rate 3/5 code.” Stewart, 7:27-33. Here, code rate refers to a number of information bits (also referred to as systematic bits) divided by the total number of bits in a transmission. Ex. 1037, §IV; Ex. 1009, 3-4; Hochwald, ¶111. **Stewart** therefore discloses **redundancy versions that select systematic bits over first and second parity bits** (e.g., “RV0”). Hochwald, ¶111.

Stewart also teaches a redundancy version in which parity bits are sent first. As shown below, in RV1-RV3, **Stewart** teaches first reading **parity bits**, starting from **starting points** within one of the interleavers. Stewart, 5:62-65, 6:62-7:4; Hochwald, ¶112.



Stewart also teaches that reading “wrap[s] around” to “the beginning of the first row of the same or another interleaver” when more bits are needed for readout, and thus reading would continue in the systematic interleaver after reading completes in the parity interleaver (*e.g.*, when reading completes in the first and second parity interleavers). *Stewart*, 5:33-40. **Stewart** further teaches that more parity bits are selected for transmission than systematic bits—for example when a rate 1/4 code is desired with RV4. *Stewart*, 7:33-34; *Hochwald*, ¶112. To achieve such a code rate, more parity bits than systematic bits are transmitted in aggregate.

Therefore, **Stewart** discloses **redundancy versions that select first and second parity bits over systematic bits** (e.g., “RV1,” “RV2,” “RV3”); Stewart, Fig. 6; Hochwald, ¶112.

(a) Buffering by Stewart

A POSITA would have (1) understood that **Stewart** disclosed buffering, (2) been motivated to use **Stewart’s** interleavers as buffers, and (3) been motivated to modify **Stewart** to use an additional buffer. Hochwald, ¶113.

(i) Stewart Discloses Buffering

Buffering is a well-known process of temporarily storing information for transmission. Ex. 1025; Ex. 1026; 3GPP-Summary, §2.4; Hochwald, ¶¶114-115. Consequently, a POSITA would have understood that **Stewart** discloses buffering the **systematic bits**, **“Parity 1” stream**, and **“Parity 2” stream** in a block matrix of respective block interleavers because they temporarily store bits in the respective block matrices for transmission. Stewart, 4:14-34, 4:46-48; ’486, 6:26-51. That interleavers are known to include memories or buffers, further supports that **Stewart’s** interleavers are buffers. Ex. 1038 (“Tong”), 7:6- 14 (“the interleaver ... further includes a FIFO (first-in, first-out) memory”); Ex. 1039] (“Arivoli”), 1:53-60 (“A typical interleaver implementation uses a memory as a buffer.”); Hochwald, ¶¶114-115.

(ii) A POSITA Would Have Used Stewart's Interleavers as Buffers

Additionally, a POSITA would have found it obvious to use the block matrices of **Stewart's** interleavers to buffer bits. A POSITA would have been motivated to use **Stewart's** interleavers as buffers to advantageously store information to support transmission and retransmission processes. For example, as discussed above in §I, a HARQ process resends portions of systematic and parity bits to ensure delivery of information at a receiver. **Stewart** discloses such a retransmission process in its incremental redundancy (IR) process. 3:25-30, 4:10-13. The various retransmissions in a HARQ process rely upon buffers to provide stored bits for transmission, as confirmed by multiple references. Ex. 1040, [0034]-[0037], [0045] ("HARQ retransmission buffer"); Ex. 1041, 4:1-7, 4:32-58, 11:48-57, 15:30-34; Ex. 1027, ¶[0034]; Hochwald, ¶116. In view of the foregoing, a POSITA would have had a reasonable expectation of success in using **Stewart's** interleavers as buffers to temporarily store bits prior to transmission or retransmission. Hochwald, ¶116. Using interleavers as buffers to support a HARQ process improves the throughput of communications within a network. *Id.*

(iii) A POSITA Would Have Added a Transmission Buffer to Stewart

Alternatively, a POSITA would have found it obvious to modify **Stewart** to use an additional buffer and would have had a reasonable expectation of success, as discussed further below in §§IX.B (Ground 2) and IX.C (Ground 3), for example to support concurrent loading of bits to an interleaver’s block matrix while bits are transmitted from a transmit buffer. Ex. 1042, 7:43-46, 13:33-39, Figs. 4, 7; Hochwald, ¶117.

2. Claim Chart (Claims 3-4)

This Petition analyzes **Stewart**, **Motorola**, **3GPP-Summary**, and **TS25.212** beginning with claims 3-4, which are asserted in the Texas Case. Claims 1-2 and 5-6 are anticipated and rendered obvious for similar reasons as shown below. In addition to §IX.A.1, the following identifies example disclosures followed by bulleted excerpts that each disclose and/or render obvious the Claims. Hochwald, ¶118.

'486 Claim	Stewart
[3.pre] A method for use in an apparatus of a wireless communications [sic] comprising:	Stewart discloses a method (e.g., “applying IR [Incremental Redundancy]”) for use in an apparatus (e.g., “user equipment (UE)” or “base station [BS]”) of a wireless communications (e.g., “[3GPP] UTRA (UMTS Terrestrial Radio Access)”). <u>E.g., Stewart:</u> Stewart discloses “applying IR [Incremental Redundancy]” in “user equipment (UE)” or “base station” that implements cellular communications such as “UMTS Terrestrial Radio

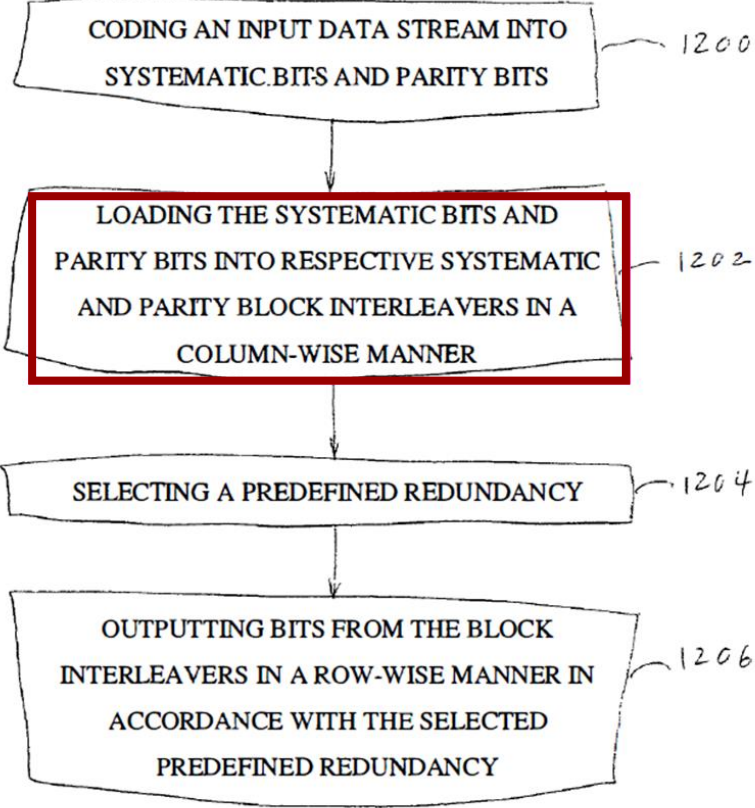
'486 Claim	Stewart
	Access”/“UTRA” or “Wideband Code Division Multiple Access”/“WCDMA”—the incremental redundancy uses different redundancy versions to select among systematic bits and parity bits for transmission. Stewart, 1:44-64, 2:47-67, 3:1-12, 3:25-46, 9:60-10:3. Hochwald, ¶¶119-122. • 1:44-64 (“Typically, the encoded data is transmitted to a receiver, which uses error detection. If an error is detected, the <i>receiver can request that the transmitter, such as a base station</i> for example, retransmit the data using an <i>Automatic Repeat Request (ARQ)</i>.”) • 2:47-67 (“The present invention provides a turbo coder that supports <i>incremental redundancy (IR)</i> as a form of ARQ combining, using a single, unified puncturing scheme. In particular, the present invention uses a puncturing scheme based on a block interleaver. <i>Codeword bits</i> are read in column-wise while the desired amount of unpunctured data is then <i>read out</i> row-wise <i>after row and column rearrangement</i>. The <i>block nature of the interleaver</i> ensures a regular puncturing distributed throughout the encoder trellis ensuring good code performance.”) • 3:1-12 (“In application, The High Speed Downlink Packet Access (HSDPA) feature of the <i>Third Generation Partnership Project (3GPP) UTRA (UMTS Terrestrial Radio Access) or Wideband Code Division Multiple Access (WCDMA)</i> system details a <i>hybrid-ARQ scheme based on Incremental Redundancy (IR)</i> methods applied to a rate-$\frac{1}{3}$ turbo-code. The present invention ... permit[s] the use of incremental redundancy block interleaving in <i>user equipment (UE), such as a cellular radio communication device</i>. The present invention describes a specific method and apparatus for

'486 Claim	Stewart
	<i>applying IR</i> to HSDPA.”) • 3:25-46 (“The present invention provides <i>a flexible IR scheme specifically applicable to HSDPA</i>. In particular, <i>the IR scheme of the present invention</i> supports: a) a flexible method of controlling the instantaneous and variable final code rate of the HARQ process (ranging from Chase combining to rate-$\frac{1}{3}$ expansion), b) general QAM modulation, including 16-QAM, c) a specific set of possible redundancy versions from which can be selected an optimal (or simply preferred) sequence of redundancy versions, based on the specific acknowledge/negative acknowledge (ACK/NACK) signal evolution applicable to HSDPA, and d) a novel implementation of block interleavers...”) • 9:60-10:3 (“Although the present invention finds particular use in <i>portable cellular radiotelephones, the invention could be applied to any two-way wireless communication device, including pagers, electronic organizers, and computers.</i>”)
[3.a] interleaving, by the apparatus, systematic bits;	Stewart discloses interleaving, by the apparatus (<i>see</i> [3.pre]), systematic bits (e.g., “load[s]...systematic bits...into [a] systematic...block interleaver[]”; “read[ing] into” a “[systematic] block interleaver” a “Systematic stream” consisting of “systematic bits”). <u>E.g., Stewart:</u> <i>See</i> [3.pre]. Stewart also discloses a “first interleaver,” which contains a “block matrix interleaver,” which contains a “block matrix.” Hochwald, ¶¶123-125; Stewart, 4:10-29, 4:46-55, Fig. 3.

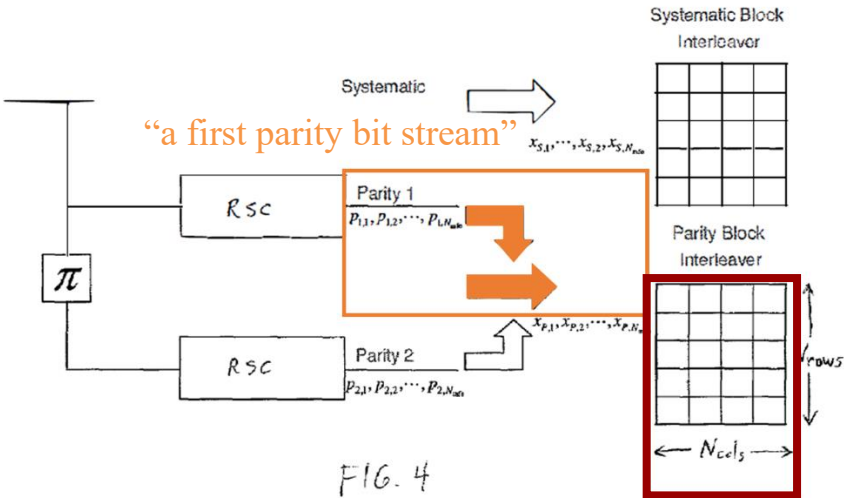
'486 Claim	Stewart
	Stewart further discloses that the “first interleaver” (Figs. 3-4) receives a “codeword,” which includes a “Systematic stream.” Stewart, 4:14-19, 4:25-29. This “Systematic stream” is made up of systematic “codeword bits” that are “read into” or “load[ed]...into” a “systematic block interleaver” and reordered (Figs. 5 and 11). Hochwald, ¶126; Stewart, 4:14-39, 4:56-5:8, 9:39-50. Stewart teaches that interleaving by a “1st Interleaver” takes place prior to the selecting by a Redundancy Version Selector. Stewart, Fig. 3. <i>Compare</i> “1st Interleaver” (300) with “Redundancy Version Selector 302”; Hochwald, ¶¶127-128. • Figure 3

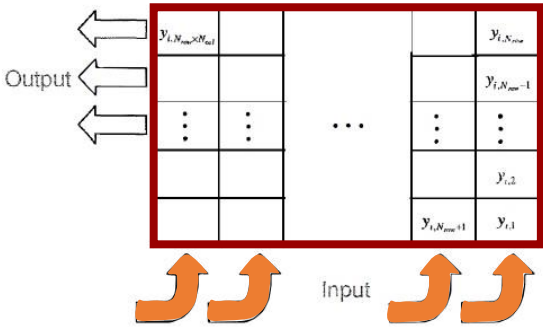
'486 Claim	Stewart
	FIG. 3 <pre> graph TD 200[TrBlk concatenation] --> 202[CRC attachment] 202 --> 204[Code block segmentation] 204 --> 206 subgraph 206 [] 208[Channel Coding] --> 300[1st Interleaver] 300 --> 302[Redundancy Version Selector] end 206 --> 304[Bit Priority Mapper] 304 --> 312[Physical channel segmentation] 312 --> 314[2nd Interleaver] 314 --> 316[Physical channel mapping] 316 --> PhCH1[PhCH#1] 316 --> PhCHK[PhCH#K] </pre> “interleaving, by the apparatus, systematic bits” • Figure 4

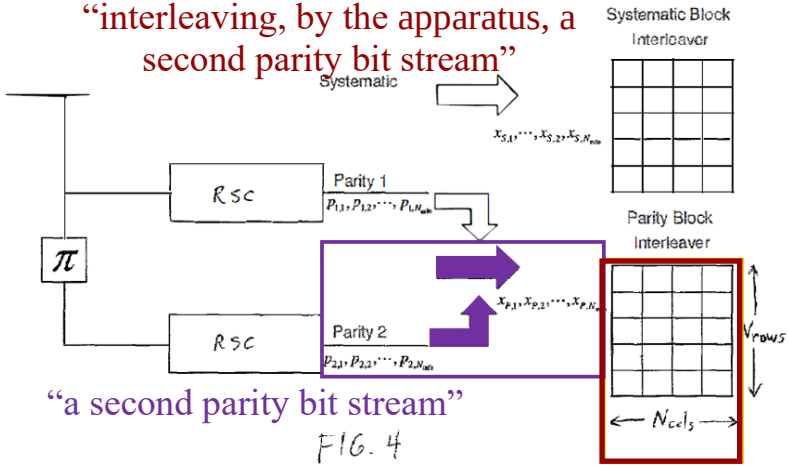
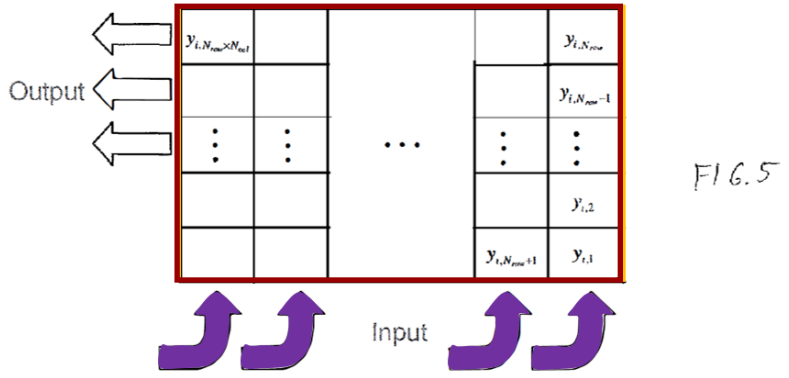
'486 Claim	Stewart
	FIG. 4 Figure 5 FIG. 5 Figure 11

'486 Claim	Stewart
	 FIG. 11 • 2:47-67 ([3.pre]) • 4:14-5:8 (“FIG. 4 shows the operation of the <i>first interleaver</i> (300 in FIG. 3) in entering a codeword into puncturing interleavers for the preferred turbo encoder. <i>In the general turbo encoder case a codeword is separated into a “Systematic” stream</i> and N_{Parity} parity streams denoted by $x_{S,k}$, $p_{1,k}$, $p_{2,k}$, . . . , $p_{N_{\text{Parity}},k}$ where $k \in \{1, \dots, N_{\text{info}}\}$. <i>Each stream is read into $N_{\text{row}} \times N_{\text{col}}$ block matrix interleavers.</i> Preferably, the parity bits are combined into one $N_{\text{row}} \times N_{\text{col}}$ puncturing matrix, but separate

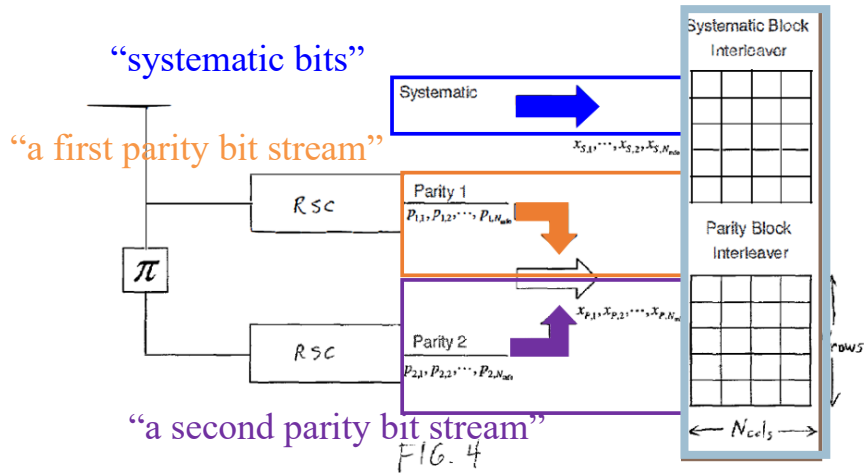
'486 Claim	Stewart
	$N_{\text{row}} \times N_{\text{col}}$ parity block interleavers can be used for each parity stream. ... In the case of the preferred turbo encoder of the present invention, the unpunctured codeword bits are bit separated into respective “Systematic”, “Parity 1” and “Parity 2” streams denoted by $x_{S,k}$, $p_{1,k}$, $p_{2,k}$ where $k \in \{1, \dots, N_{\text{info}}\}$. ... The tail bits from the coder are buffered separately and are later appended onto the unpunctured instantaneous codeword transmitted in a specific transmission time interval (TTI). ... FIG. 5 shows the data stream of the interleavers of FIG. 4. A novel aspect of the present invention is having data read in a column-wise fashion into each interleaver. The data includes dummy bits padded if $N_{\text{info}} < N_{\text{row}} \times N_{\text{col}}$, where $y_k = x_k$ for $k = 1, 2, \dots, N_{\text{info}}$ and $y_{S,k} \in \{0,1\}$ and $y_{P,k} \in \{1,0\}, \{0,1\}, \{1,0\}, \{1,1\}$ for $k = \{N_{\text{info}} + 1, \dots, N_{\text{row}} \times N_{\text{col}}\}$. These dummy bits are later removed when reading the codeword data row-wise from top-to-bottom from the block matrix, similar to the description in section 4.2.3.2.3.2 of TS 25.212, incorporated by reference. ... After the row and column permutation, the desired number of codeword bits can then be read out in row-wise fashion.”) 9:39-59 (“FIG. 11 shows a flow chart representing a method of block puncturing for turbo code based incremental redundancy, in accordance with the present invention. A first step of the method is coding 1200, such as turbo coding, an input data stream into systematic bits and parity bits. A next step is loading 1202 loading [sic] the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner, as described previously.”)
[3.b] interleaving,	Stewart discloses interleaving by the apparatus (see

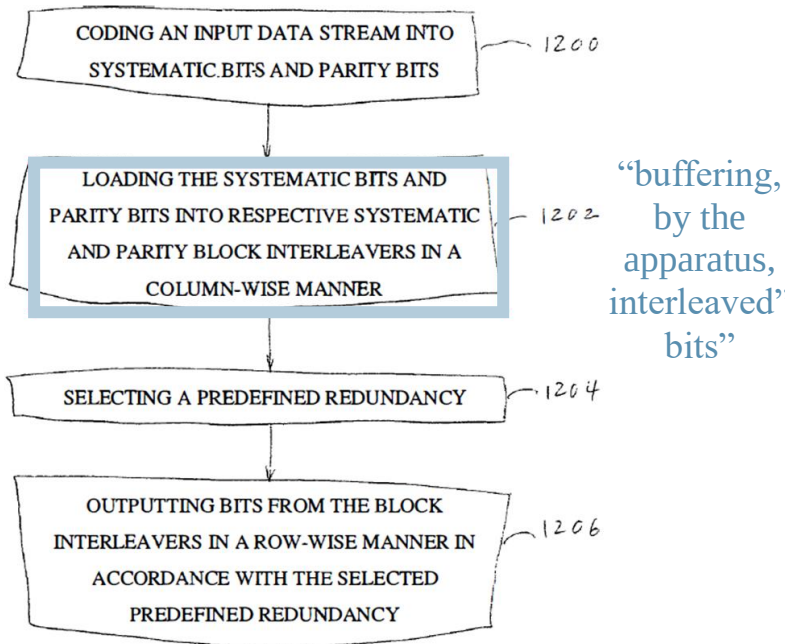
'486 Claim	Stewart
by the apparatus, a first parity bit stream;	[3.pre]), a first parity bit stream (e.g., “loading...parity bits into [a] respective...parity block interleaver[]”; “read[ing] into” a “parity block interleaver[]” a “parity stream[] denoted by $p_{1,k}$”). <u>E.g., Stewart:</u> See [3.pre]-[3.a]. Stewart further discloses that a “separate” “parity block interleaver[]” (Fig. 4) receives a codeword, which includes a first “Parity 1” stream, which is denoted $p_{1,k}$. Stewart, 4:14-19, 4:25-29. This first “Parity 1” stream is “read into” or “load[ed]...into” a “parity block interleaver[]” of N_{row} number of rows and N_{column} number of columns in a column-wise fashion. Hochwald, ¶¶129-132; Stewart, 4:14-29, 9:39-50, Figs. 4, 5, 11. • Figure 3 ([3.a]) • Figure 4  FIG. 4 “interleaving, by the apparatus, a first parity bit stream”

'486 Claim	Stewart
	• Figure 5  FIG. 5 • Figure 11 ([3.a]) • 2:47-67 ([3.pre]) • 4:14-5:8 ([3.a]) • 9:39-59 ([3.a])
[3.c] interleaving, by the apparatus, a second parity bit stream;	Stewart discloses interleaving by the apparatus (see [3.pre]), a second parity bit stream (e.g., “loading...parity bits into [a] respective...parity block interleaver[]” or “read[ing] into” a “parity block interleaver[]” a “parity stream[] denoted by $p_{2,k}$”). <u>E.g., Stewart:</u> See [3.pre]-[3.b]. Stewart further discloses that a “separate” “parity block interleaver[]” (Fig. 4) receives a codeword, which includes a second “Parity 2” stream, which is denoted $p_{2,k}$. Stewart, 4:14-19, 4:25-29. This second “Parity 2” stream is “read

'486 Claim	Stewart
	into” or “load[ed]...into” a “parity block interleaver[].” Stewart, 4:14-39, 9:39-50, Figs. 4, 5, 11. Hochwald, ¶¶133-136. • Figure 3 ([3.a]) • Figure 4 “interleaving, by the apparatus, a second parity bit stream”  FIG. 4 • Figure 5  FIG. 5 • Figure 11 ([3.a]) • 4:14-5:8 ([3.a]) • 2:47-67 ([3.pre])

'486 Claim	Stewart
	• 9:39-59 ([3.a])
[3.d] buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and	Stewart discloses buffering, by the apparatus (see [3.pre]), the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream (e.g., storing “systematic bits” in a “systematic block interleaver” for subsequent read out, storing “parity bits” from “parity stream[] denoted by $p_{1,k}$” in a “parity block interleaver” for subsequent read out; and storing “parity bits” from “parity stream[] denoted by $p_{2,k}$” in a separate “parity block interleaver” for subsequent read out). <u>E.g., Stewart:</u> See [3.pre]-[3.c]. Stewart also discloses that the systematic bits from “‘Systematic’...stream[],” parity bits from first “Parity 1” stream “denoted by...$p_{1,k}$” and second “Parity 2” stream “denoted by...$p_{2,k}$” are “read into” and stored in their “respective” block interleavers (Figs. 4,11) for subsequent read out in a different interleaved order. Stewart, 4:14-29; Hochwald, ¶¶137-139. As discussed in §I.A.1(a), Stewart discloses to a POSITA that the process of storing codeword bits into the block matrix of a block interleaver (Fig. 5) entails buffering because buffering is a well-known process of temporarily storing bits for transmission. In Stewart, the respective bits are read into an interleaver (e.g., column-by-column) and permuted within the interleaver at which point the bits are interleaved, prior to being read out. Stewart, 2:47-67, 4:46-5:8. When the bits are stored after being read into and interleaved in the block matrix, and prior to read out, the bits are being buffered by the block matrix. Hochwald, ¶140. Stewart, as discussed in §I.A.1(a), also renders obvious using interleavers as buffers, for example, to support a

'486 Claim	Stewart
	retransmission process. Stewart discloses a HARQ process that is used to support retransmission of signals. Stewart, 3:25-30. HARQ processes use buffers to facilitate the retransmission of signals, and interleavers are known to include buffers or memory. It would have been obvious to use the interleaver to buffer the interleaved systematic bits, first parity bits, and second parity bits in order to facilitate the HARQ retransmission. Hochwald, ¶¶141-142. Figure 4  The diagram illustrates a HARQ process. An input signal is split into three paths. The top path, labeled "systematic bits" in blue, passes through a permutation block π and then a Rate-Splitting (RSC) block to produce a "Systematic" stream of bits $x_{S,1}, \dots, x_{S,2}, \dots, x_{S,N_{tot}}$. The middle path, labeled "a first parity bit stream" in orange, passes through an RSC block to produce a "Parity 1" stream of bits $p_{1,1}, p_{1,2}, \dots, p_{1,N_{tot}}$. The bottom path, labeled "a second parity bit stream" in purple, passes through an RSC block to produce a "Parity 2" stream of bits $p_{2,1}, p_{2,2}, \dots, p_{2,N_{tot}}$. These three streams are then fed into two interleavers: a "Systematic Block Interleaver" and a "Parity Block Interleaver". The interleavers are represented as grids. The "Systematic Block Interleaver" has a width of N_{colS} and a height of N_{rows}. The "Parity Block Interleaver" also has a width of N_{colS} and a height of N_{rows}. The interleaved streams are then combined for transmission. Figure 11

'486 Claim	Stewart
	 FIG. 11 • 2:47-67 ([3.pre]) • 3:25-46 ([3.pre]) • 4:14-34 ([3.a]) • 6:41-52 (“[P]redefined redundancy comprises a redundancy version for the coded bits of the block interleavers ... [that] sets one or more starting rows $\alpha_{i,j}$ for each redundancy version j, where $i \in \{S,P\}$... and reads the coded bits from the selected starting rows in a pre-defined order and ratio, wherein if the end of the N_{i,max_row}th interleaver is reached, reading shall continue from the first row of a predefined interleaver which includes one of the systematic and parity block interleavers.”) • 9:39-59 ([3.a])

'486 Claim	Stewart
	• <i>See also</i> 3:64-4:13; 5:38-40.
[3.e] selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.	Stewart discloses selecting, by the apparatus (<i>see</i> [3.pre], including a “redundancy version selector”), bits for transmission based on a plurality of redundancy versions (<i>e.g.</i>, “a preferred set of eight redundancy versions for selecting coded bits from the systematic and parity interleavers”); wherein at least one redundancy version of the set selects systematic bits over first and second parity bits (<i>e.g.</i>, “Redundancy version zero[] ... systematic interleaver is read from its starting row to completion before the remaining coded bits are read from the parity interleaver”) and at least one redundancy version of the set selects first and second parity bits over systematic bits (<i>e.g.</i>, “Redundancy version one[] ... the coded bits are read from the parity interleaver starting at its starting row”). <u>E.g., Stewart:</u> <i>See</i> [3.pre]-[3.d]. Stewart also discloses that, <i>e.g.</i>, a UE or BS reads out “codeword bits” from the systematic and parity block interleavers for transmission. Stewart, 2:51-53, 5:6-15, Fig.

'486 Claim	Stewart
	5. A “redundancy version selector” selects a redundancy version from a set of redundancy versions (“zero” to “seven”) that selects “a starting point at which to commence the readout of codeword bits” from the interleavers. Stewart, 3:25-36, 4:8-10, 5:57-6:13, 6:41-7:24, Figs. 3, 11. Hochwald, ¶¶143-145. Stewart also discloses at least one redundancy version (e.g., “zero”) in which “coded bits from the systematic interleaver is read from its starting row to completion before the remaining coded bits are read from the parity interleaver starting at its starting row,” which entails selecting systematic bits from the systematic interleaver to be transmitted over the first and second parity bits from the first and second parity interleavers. Stewart, 6:41-52, 6:57-61, Fig. 6. Hochwald, ¶146. Stewart also discloses at least one redundancy version (e.g., “one”, “two”, “three”) in which first and second parity bits are read from, respectively, a first parity interleaver and a second parity interleaver, “starting at starting row” $N_{p,max_row}/4$. Stewart, 6:41-52, 6:62-7:4, Fig. 6; Hochwald, ¶147. As shown in Fig. 6, “[r]edundancy version one[,]” the systematic interleavers have an “X” inside them, which “signifies no bits are used from that interleaver” and transmitted. Stewart, 6:16-18, Fig. 6; Hochwald, ¶148. Stewart also discloses a similar process for redundancy versions “two” and “three.” <i>Id.</i>, 6:62-7:4; Hochwald, ¶¶149-150. Because no systematic bits from systematic block interleavers are selected to be transmitted, but first and second parity bits are, then the first and second parity bits are selected over the systematic bits. Hochwald, ¶¶149-150. In addition, Stewart alternatively discloses that “[w]hen more coded bits are required than can be obtained by reading to the end of the N_{i,max_row}^{th} row, $i \in \{S,P\}$, reading may continue by wrapping around to the beginning of the first row of the same or another interleaver.” Stewart, 5:33-

'486 Claim	Stewart
	47, 6:41-52, 6:57-61; Hochwald, ¶151. Consequently, if more bits are required after reading a first interleaver, such as the parity interleaver, the reading continues in another interleaver, such as the systematic interleaver. <i>Id.</i>; Hochwald, ¶151. Thus, not only does Stewart render obvious reading the systematic bits after the parity bits, but it expressly teaches doing so. Stewart, 5:33-37. Hochwald, ¶¶147-151. As discussed above in §IX.A.1, Stewart teaches a redundancy version in which more systematic bits are selected for transmission than parity bits—for example when RV_0 is “signaled with enough codeword bits to result in a rate 3/5 code”; and a redundancy version in which more parity bits are selected for transmission than systematic bits—for example when a rate 1/4 code is desired with RV_4. Stewart, 7:27-34; Hochwald, ¶¶152-153. • Figure 3

'486 Claim	Stewart
	FIG. 3 “selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits” - Figure 5 “bits for transmission” FIG. 5 - Figure 6

'486 Claim	Stewart
	“at least one redundancy version of the set selects systematic bits over first and second parity bits” “at least one redundancy version of the set selects first and second parity bits over systematic bits” FIG. 6 • Figure 11 ([3.a]) • 2:47-67 ([3.pre]) • 3:25-46 ([3.pre]) • 4:8-10 (“The present invention occurs in the first interleaver 300, redundancy version selection 302, and the optional bit priority mapper 304.”) • 5:6-15 (“After the row and column permutation, the desired number of codeword bits can then be read out in row-wise fashion. Using the notation of FIG. 4, if the desired number of parity bits is an odd number and if $x_{p,k}=\{p_{1,k}, p_{2,k}\}$ is the last symbol read from the parity interleaver, then the parity bit $p_{1,k}$ is used as a codeword bit while the parity bit $p_{2,k}$ is discarded. In the case of the parity interleaver, the maximum number of rows that can be transmitted N_{p,max_row} may be less than N_{row} due to UE memory

'486 Claim	Stewart
	restrictions, while for the systematic interleaver N_{S,max_row} is always equal to N_{row}.”) 5:33-37 (“When more coded bits are required than can be obtained by reading to the end of the N_{i,max_row}^{th} row, $i \in \{S,P\}$, <i>reading may continue by wrapping around to the beginning of the first row of the same or another interleaver.</i> One consequence of this is to allow coding rates less than $\frac{1}{3}$.”) 5:57-6:41 (“Referring back to FIG. 3, the present invention also incorporates <i>a redundancy version selector 302.</i> Since <i>a different number of codeword bits may be obtained from the systematic and parity block interleavers,</i> the framework of the present invention allows for both Chase and incremental redundancy (IR) coding schemes. <i>In order to support different redundancy versions, any row of any block puncturing interleaver may be assigned as a starting point at which to commence the readout of codeword bits.</i> By defining multiple starting points for one redundancy version, the order and/or the ratio in which codeword bits are be read out from the systematic and parity interleavers can provide further degrees of freedom in describing any potential redundancy version. <i>The set of redundancy versions defined between the Node B and UE can be of any size, and may vary dynamically or semi-statically in size and form (e.g. through explicit signaling of redundancy versions or a subset of a pre-agreed redundancy versions between the Node B and UE) or as in the preferred implementation shown in FIG. 6.be [sic] derived from a pre-defined static set. ...</i> Rule 1: Each rectangle represents rows 1 to N_{i,max_row} for $i \in \{S,P\}$. <i>Rule 2: The X (e.g. RV1, RV2, RV3) inside an interleaver signifies no bits are used from that</i>

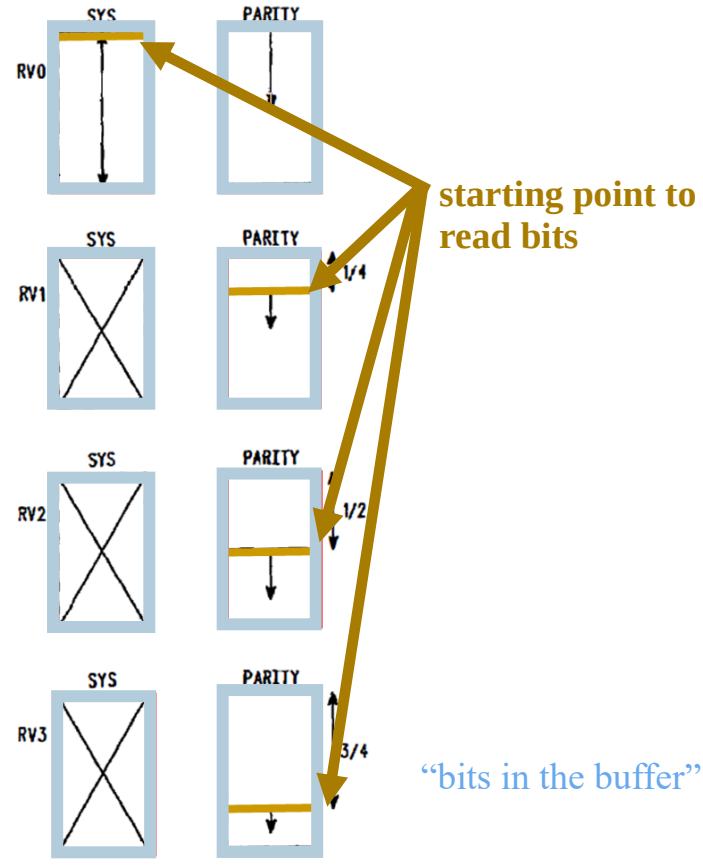
'486 Claim	Stewart
	<i>interleaver to form the instantaneous codeword.</i> Rule 3: The double arrowed line inside an interleaver signifies all bits in 1 to N_{i,max_row} in that block interleaver must be transmitted exactly once (e.g. RV0). <i>Rule 4: In the case there is an X in one interleaver and a single arrowed line in the other, then codeword bits are only read from the block interleaver with the single arrowed line.</i> <i>Rule 5: In the case there is a double arrowed line in one interleaver and a single arrowed line in the other, then codeword bits are only read from the block interleaver with the single arrowed line once reading from the double arrowed line is complete.</i> Rule 6: In the case there is a single arrowed line in both interleavers, then codeword bits are read equally from both block interleavers. <i>Rule 7: If reading from a block interleaver with a single arrowed line has reached the end of line N_{i,max_row} but more codeword bits are required, then reading wraps around to line 1.</i> Rule 8: A fractional number N_{frac_num} beside the starting row of a single arrowed line indicates that starting row as $N_{frac_num} \times N_{i,max_row}$.”) • <i>6:41-52 (“In general, the predefined redundancy comprises a redundancy version for the coded bits of the block interleavers wherein the redundancy version sets one or more starting rows $\alpha_{i,j}$ for each redundancy version j, where $i \in \{S,P\}$ and $\alpha_{i,j} \in \{1, \dots, N_{i,max_row}\}$ and reads the coded bits from the selected starting rows in a pre-defined order and ratio, wherein if the end of the N_{i,max_row}th interleaver is reached, reading shall continue from the first row of</i>

'486 Claim	Stewart
	<i>a predefined interleaver which includes one of the systematic and parity block interleavers. The set of redundancy versions may be of any size and may be constructed on a static, semi-static or variable basis.”)</i> 6:53-7:24 (“The present invention includes <i>a preferred set of eight redundancy versions for selecting coded bits from the systematic and parity interleavers</i> in accordance with the above rules, as shown in FIG. 6 and as described below. <i>Redundancy version zero: the starting row is the top row of both the systematic and parity interleavers, and coded bits from the systematic interleaver is read from its starting row to completion before the remaining coded bits are read from the parity interleaver starting at its starting row.</i> <i>Redundancy version one: the starting row is $N_{p,max_row}/4$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.</i> <i>Redundancy version two: the starting row is $N_{p,max_row}/2$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.</i> <i>Redundancy version three: the starting row is $3 \times N_{p,max_row}/4$ for the parity interleaver, and the coded bits are read from the parity interleaver starting at its starting row.”)</i> 7:27-34 (“For example, if on the first transmission RV0 is signaled with enough codeword bits to result in <i>a rate $\frac{3}{5}$ code (exactly one third of the parity bits transmitted, e.g. one third of “Parity 1” and one third of “Parity 2” stream in the preferred turbo encoder case), the scheduler is permitted choose RV2 for the</i>

'486 Claim	Stewart
	<i>second transmission. Similarly, if in the first transmission, a rate $\frac{1}{4}$ code is desired, RV4 might be selected for the second transmission.”)</i>
[4] The method of claim 3 wherein the selecting of bits for transmission in response to a selected redundancy version changes in response to a location of the bits in the buffer.	See [3]. Stewart discloses that the selecting of bits for transmission in response to a selected redundancy version (see [3.e]) changes in response to a location of the bits (e.g., different “redundancy version[s]” have different “starting point[s] at which to commence the readout of codeword bits”) in the buffer (see [3.d]). <u>E.g., Stewart:</u> See [3.pre], [3.d]-[3.e]. Stewart also discloses that the “select[ed] coded bits from the systematic and parity interleavers” for transmission are read out starting at “a starting row” in the systematic and parity interleaver. Stewart, 5:62-6:3, 6:37-39, 6:41-50, 6:53-56, Fig. 6; Hochwald, ¶¶154-157. The starting point indicates the position within the interleaver “at which to commence the readout of codeword bits.” Stewart, 5:62-6:3; Hochwald, ¶¶158-159. In some redundancy versions, this starting point is a “fractional number” ($N_{frac_num} \times N_{i,max_row}$) that indicates a row within the block interleaver matrix as shown in Fig. 6. Stewart, 6:38-64. Hochwald, ¶157. Stewart also discloses that bits from the “‘Systematic’ stream,” first “Parity 1” stream and second “Parity 2” stream are “read into” their respective block interleavers. Stewart, 4:14-29. The bits selected from Stewart’s interleavers therefore depend on the redundancy version (which sets a starting point within a block interleaver to

'486 Claim	Stewart
	read out bits (see Fig. 6)), and changes based on the bits that are located within the buffer (see Fig. 6).²⁴ Stewart, 5:50-53. • Figure 5, 4:46-55 (see [3.a]) • Figure 6

²⁴ Indeed, these disclosures of **Stewart** regarding the dependence of the selected bits on the redundancy version and bits located within the block matrix buffer are consistent with and similar to the disclosures of the '486. See '486, 16:10-26, 18:10-19:13; Hochwald, ¶158.

'486 Claim	Stewart
	 The diagram illustrates a data storage layout with four rows (RV0, RV1, RV2, RV3) and two columns (SYS, PARITY). Each row is represented by a box. In the SYS column, RV0 has a horizontal yellow bar at the top, while RV1, RV2, and RV3 have an 'X' mark. In the PARITY column, RV0 has a vertical arrow pointing down, while RV1, RV2, and RV3 have horizontal yellow bars at the 1/4, 1/2, and 3/4 positions respectively. A yellow arrow originates from the top of the RV0 PARITY box and points to the top of the RV0 SYS box, labeled 'starting point to read bits'. A blue arrow originates from the bottom of the RV3 PARITY box and points to the bottom of the RV3 SYS box, labeled 'bits in the buffer'. FIG. 6 • 4:14-5:8 ([3.a]) • 5:50-53 (“Rate selection therefore occurs as a result of <i>redundancy version (tells which row to start reading from)</i> and the <i>first interleaver (gives the order bits should be read out).</i>”) • 5:57-6:41 ([3.e]) • 6:41-50 ([3.e]) • 6:53-7:24 ([3.e])

As shown above, **Stewart** not only renders obvious but also anticipates claims 3-4. **Stewart** renders obvious and anticipates claims 1-2, and 5-6 for the same reasons because those claims are directed to apparatuses that perform the method of claims 3-4 using components disclosed by **Stewart**.

3. Claims 1-2

Compared with claim 3, claim 1 additionally requires [1.a] a “first interleaver,” [1.b] a “second interleaver,” [1.c] a “third interleaver,” [1.d] a “buffer,” and [1.e] a “rate matching unit,” each configured to perform the respective steps of claim 3 ([3.a]-[3.e]). Hochwald, ¶¶160-161.

Regardless of whether the preamble of claim 1 is limiting **Stewart** discloses [1.pre], an apparatus, for the same reasons discussed above in [3.pre] and §VIII. Stewart, 1:44-56, 3:1-12. Hochwald, ¶162.

Stewart discloses [1.a], a **first interleaver** (*e.g.*, “Systematic Block Interleaver”, “respective systematic ... block interleaver[.]”) **configured to interleave systematic bits**, for the same reasons discussed above in [3.a] and §VIII. Stewart, Abstract, Fig. 4, 4:14-5:8, 9:39-59; Hochwald, ¶163.

Stewart discloses [1.b], a **second interleaver** (*e.g.*, “separate” “parity block interleaver[.]” for “Parity 1” stream) **configured to interleave a first parity bit**

stream, for the same reasons discussed above in [3.b] and §VIII. Stewart, Fig. 4, 4:14-5:8, 9:39-59; Hochwald, ¶164.

Stewart discloses [1.c], a **third interleaver** (*e.g.*, “separate” “parity block interleaver[]” for “Parity 2” stream) **configured to interleave a second parity bit stream**, for the same reasons discussed above in [3.c] and §VIII. Stewart, Fig. 4, 4:14-5:8, 9:39-59; Hochwald, ¶165.

Stewart not only renders obvious but also discloses [1.d], a **buffer** (*e.g.*, “systematic and parity block puncturing block interleavers”) **configured to buffer** interleaved bits, for the same reasons discussed above in [3.d] and §§VIII and I.A.1(a). Stewart, Abstract, Fig. 4, 4:14-5:8, 5:57-65, 9:39-59; Hochwald, ¶166.

Stewart not only renders obvious but also discloses [1.e], a **rate matching unit** (*e.g.*, redundancy version selector), for the same reasons discussed above in [3.e] and §VIII. Stewart, Fig. 3, 4:2-13, 5:50-53, 5:57-7:43. For example, **Stewart’s** “redundancy version selector”—which selects bits for transmission based on a plurality of redundancy versions performs the same function as the ’486 claimed rate matching unit. See [3.e]; Stewart 5:57-62; §VIII; Hochwald, ¶167.

Claim 2 is substantively the same as claim 4, except that claim 2 requires a “rate matching unit.” Therefore, **Stewart** not only renders obvious but also

anticipates claim 2 for the same reasons discussed above in claim 4, and [1.e].
Hochwald, ¶168.

4. Claims 5-6

Compared with claim 3, claim 5 ([5.a]-[5.e]) additionally requires “circuitry” configured to perform the respective steps of claim 3 ([3.a]-[3.e]). Hochwald, ¶169.

Regardless of whether the preamble of claim 5 is limiting, **Stewart** discloses [5.pre], a “wireless transmit/receive unit” for the same reasons discussed above in [3.pre], where the ’486 claimed “wireless transmit/receive unit” is disclosed by **Stewart’s** BS and/or UE. Stewart, 1:44-64, 3:9-12, 5:57-62, 9:60-10:3; Hochwald, ¶170.

Stewart not only renders obvious but also discloses the **circuitry** required for claim 5 at least for the same reasons discussed above for claims 1 and 3. Stewart, 2:25-26, 9:60-10:3; Hochwald, ¶171. A POSITA would have known that circuitry is used to implement wireless communications devices such as a UE or BS. For example, “Nickum” discloses that a “communication apparatus” is implemented using “circuitry.” Ex. 1034. The “interleaver[s]” and “redundancy version selector” meet the requirements of claims [5.a]-[5.e] in the same way as discussed above for claims 1 and 3. Regardless of whether each circuitry of claim

5 must be part of the same circuitry, **Stewart** discloses that each element of claim 1 (*e.g.*, interleavers and redundancy version selector) is part of the same “coding structure” or “channel coding model”— disclosing or at minimum rendering obvious the claimed circuitry. Stewart Fig. 3; 2:25-26, 3:64-4:13; Hochwald, ¶171.

Claim 6 is substantively the same as claims 4 and 2. Therefore **Stewart** not only renders obvious but also anticipates claim 6 for the same reasons discussed above with respect to claims 4 and 2. Hochwald, ¶¶172-173.

B. Ground 2: Stewart in view of 3GPP-Summary

Stewart in view of **3GPP-Summary** renders obvious each of the Claims. Hochwald, ¶174.

1. **“buffer[ing]” ([3.d]/[1.d]/[5.d])**

3GPP-Summary teaches further details of “[buffering.../buffer configured to buffer/circuitry...configured to buffer] the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream” as required by ([3.d]/[1.d]/[5.d]) and thus render obvious claims 1-6, where said limitations require a buffer hardware component that is separate from an interleaver. Hochwald, ¶175.

Specifically, **3GPP-Summary** teaches **[a buffer] buffering the interleaved systematic bits, the interleaved first parity bit stream and the interleaved**

second parity bit stream in a separate buffer (*e.g.*, “transmitter buffer” or a “ring buffer” that stores “interleaved systematic bits” and “interleaved parity bits.”). 3GPP-Summary, §2.4; Hochwald, ¶176.

Like **Stewart**, **3GPP-Summary** teaches applications of incremental redundancy (IR) and HARQ retransmissions. Stewart, 1:57-64, 2:47-67; 3GPP-Summary, §§1, 2.4; Hochwald, ¶¶176-178. Specifically, **3GPP-Summary** teaches a “‘ring buffer’ scheme” in which a “transmitter buffer” stores “interleaved systematic bits” and “interleaved parity bits.” 3GPP-Summary, §2.4; Hochwald, ¶¶176-178.

3GPP-Summary and **Stewart** are analogous prior art and in the same field as the ’486, including improvements to coding schemes for wireless communications, and reasonably pertinent to the alleged problems identified in the ’486 of using redundancy versions to implement an IR process for transmitting information between a user device and BS. *E.g.*, ’486, Abstract; 4:53-5:13; Stewart, Abstract, 2:47-67; 3GPP-Summary, §§1, 2.4; Hochwald, ¶177.

A POSITA would have been motivated to modify **Stewart** by **3GPP-Summary’s** teachings of a “transmitter buffer” to buffer **Stewart’s** interleaved systematic bits and interleaved parity bits prior to selection for transmission as taught in **3GPP-Summary**. 3GPP-Summary, §2.4; Stewart, 5:29-8:30, Figs. 6-7;

Hochwald, ¶179. Based on **3GPP-Summary**'s teachings that the "transmitter buffer" is placed after the interleavers, and that bits are selected from the transmitter buffer based on the redundancy versions, a POSITA would have modified **Stewart** to include a "transmitter buffer" at the output of **Stewart**'s interleavers, and before **Stewart**'s redundancy version selector. 3GPP-Summary, §2.4. Doing so supports concurrent loading of bits into an interleaver while bits are transmitted from a buffer. Ex. 1042, 7:43-46, 13:33-39, Figs. 4, 7; Hochwald, ¶179. Doing so also applies the teachings of known methods to yield predictable results. Buffers are well-known components used in communication systems to support retransmission of incorrectly received signals in an ARQ process. See §§VIII, I.A.1(a); Stewart, 4:14-34, 46-48; Ex. 1025; Ex. 1026; Ex. 1040, [0034]-[0037], [0045] ("HARQ retransmission buffer"), Ex. 1041, 4:1-7, 4:32-58, 11:48-57, 15:30-34, Ex. 1027, ¶[0034]; Hochwald, ¶179. Buffers improve successful delivery of information in an ARQ process by storing the signals for retransmission. *Id.* **Stewart** teaches using interleavers to store bits, and using buffers to store bits that are combined with interleaved bits. See §I.A.1(a); Stewart, 4:29-34, 5:38-40. **3GPP-Summary** teaches using a "transmitter buffer" where interleaved systematic and parity bits are "stored" prior to transmission. 3GPP-Summary, §2.4. **3GPP-Summary**'s "ring buffer" supports a wrapping

around process in which bits continue to be accessed from the beginning of a buffer after reaching the end of the buffer. 3GPP-Summary, §2.4. The wrapping around functionality provides additional coded bits for transmission in positions that would otherwise be unused, and additionally facilitates lower coding rates. Stewart, 5:33-37; Hochwald, ¶179.

In light of the above teachings, a POSITA would have had a reasonable expectation of success in modifying **Stewart** with **3GPP-Summary**'s teachings by using a "transmitter buffer" to store interleaved systematic and parity bits from **Stewart**'s System and Parity Block Interleavers, because a transmitter buffer was well known for "storing" bits to facilitate retransmission in an ARQ process. Ex. 1040, [0034]-[0037], [0045]; Ex. 1041, 4:1-7, 4:32-58, 11:48-57, 15:30-34; Ex. 1027, ¶[0034]; Hochwald, ¶180. In the modified **Stewart** system, bits are selected from the "transmitter" buffer" for transmission. **3GPP-Summary**'s "ring buffer" with wrap around functionality in particular further supports additional coding rates that would be used in wireless communications. **Stewart**, 5:33-37; Hochwald, ¶180. Modifying **Stewart** with **3GPP-Summary**'s teachings would have been a straightforward application of those teachings in a manner that advantageously improves the reliability of the system by buffering the bits prior to transmission. Hochwald, ¶180.

2. **“at least one redundancy version of the set selects first and second parity bits over systematic bits” ([3.e]/[1.e]/[5.e])**

3GPP-Summary teaches further detail of “at least one redundancy version of the set selects first and second parity bits over systematic bits” as required by ([3.e]/[1.e]/[5.e]) and thus renders obvious claims 1-6. Hochwald, ¶181. **3GPP-Summary** teaches **at least one redundancy version of the set selects first and second parity bits over systematic bits** (*e.g.*, “different initial positions” “defined in the buffer, giving” “eight [] redundancy versions,” where “systematic bits are stored, followed by [] parity bits” and “wrap around is used at the end of the buffer”). 3GPP-Summary, §2.4; Hochwald, ¶181.

3GPP-Summary teaches “eight [] redundancy versions” associated with “[e]ight different initial positions” “defined in the [transmitter] buffer,” to select a starting point from which to read bits from the transmission buffer. 3GPP-Summary, §2.4; Hochwald, ¶182. **3GPP-Summary** teaches that “at transmission, bits are sequentially transmitted from the buffer, starting at the selected initial position” and that “(wrap around is used at the end of the buffer).” *Id.* Depending on the “starting point” of the transmitter buffer from which bits are read for transmission, **3GPP-Summary** teaches either reading interleaved parity bits (*e.g.*, from the parity bits section) followed by wrapping around to interleaved systematic bits (*e.g.*, selecting parity bits over systematic bits), or reading interleaved

systematic bits followed by interleaved parity bits (e.g., selecting systematic bits over parity bits). *Id.*; Hochwald, ¶182.

3GPP-Summary and **Stewart** are analogous prior art and in the same field as the '486 for the reasons discussed in §IX.B.1. Hochwald, ¶183.

A POSITA would have been motivated to modify **Stewart** with the teachings of **3GPP-Summary**'s redundancy versions and “starting points” because **3GPP-Summary**'s implementations of redundancy versions is an alternative to the implementations of redundancy versions in **Stewart** with associated benefits discussed herein. 3GPP-Summary, §2.4, Figs. 4-5; Stewart, 5:29-40, 5:57-7:24, Fig. 6; Hochwald, ¶184. Because **3GPP-Summary**'s implementation of redundancy versions are an alternative to **Stewart**'s implementations with different advantages for an ARQ process, a POSITA would have been motivated to modify **Stewart** with **3GPP-Summary**'s teachings of different starting points to obtain additional granularity in the starting rows of interleavers, whereby the “starting point” for reading of bits is varied between **Stewart**'s “systematic bits,” “first parity bits” and “second parity bits,” whether accessed from **Stewart**'s Block Interleavers, or from a “transmitter buffer,” as taught by **3GPP-Summary**. Hochwald, ¶184.

As discussed below with respect to **Motorola** (see §IX.D), different redundancy versions support incremental redundancy procedures to adapt to varying reliability of channel conditions. Hochwald, ¶185. Moreover, implementing a redundancy version that starts from redundancy bits and wraps back to systematic bits provides benefits such as “allowing coding rates less than 1/3,” and providing a “redundancy version sequence” that “adjusts naturally to support” various coding schemes. Motorola, §§2.1, 2.2; Hochwald, ¶185.

In view of the benefits of various alternative redundancy versions, a POSITA would have been motivated to modify **Stewart** to use a redundancy version taught by **3GPP-Summary**, in which an initial position is set in the parity bits portion of stored systematic bits and parity bits, and bits are read from parity bits followed by systematic bits, in combination with **Stewart’s** redundancy version 0 in which systematic bits are read from the systematic block interleaver followed by parity bits from parity block interleavers. Stewart, 5:29-8:30, Fig. 6; 3GPP-Summary, §2.4; Hochwald, ¶186. In this modified system of **Stewart**, at least one redundancy version of the set selects systematic bits over first and second parity bits (e.g., **Stewart’s** RV0) and at least one redundancy version of the set selects first and second parity bits over systematic bits (e.g., redundancy version taught by **3GPP-Summary**) for the reasons discussed above. *Id.*

In light of the above teachings, a POSITA would have had a reasonable expectation of success in modifying **Stewart** with **3GPP-Summary**'s teachings to use redundancy versions associated with different starting points across Stewart's systematic bits and parity bits. Hochwald, ¶187. A POSITA would have recognized that the use of different redundancy versions results in various advantages, including granularity of redundancy version, that will implement a system for retransmission of bits from a user device to a base station. Hochwald, ¶187. **Stewart** discloses that its system uses multiple redundancy versions, including those in which reading of coded bits from a first interleaver wraps around to the first row of a second interleaver after all coded bits have been read out from the first interleaver. Stewart, 5:33-40. Modifying **Stewart** with **3GPP-Summary**'s teachings would have been a straightforward application of those teachings in a manner that advantageously improves the performance of the system by using different redundancy versions that are selected to address a variety of different channel conditions and required retransmission of information. Stewart, 1:57-64, 2:47-51; Ex. 1043, Abstract; Hochwald, ¶187.

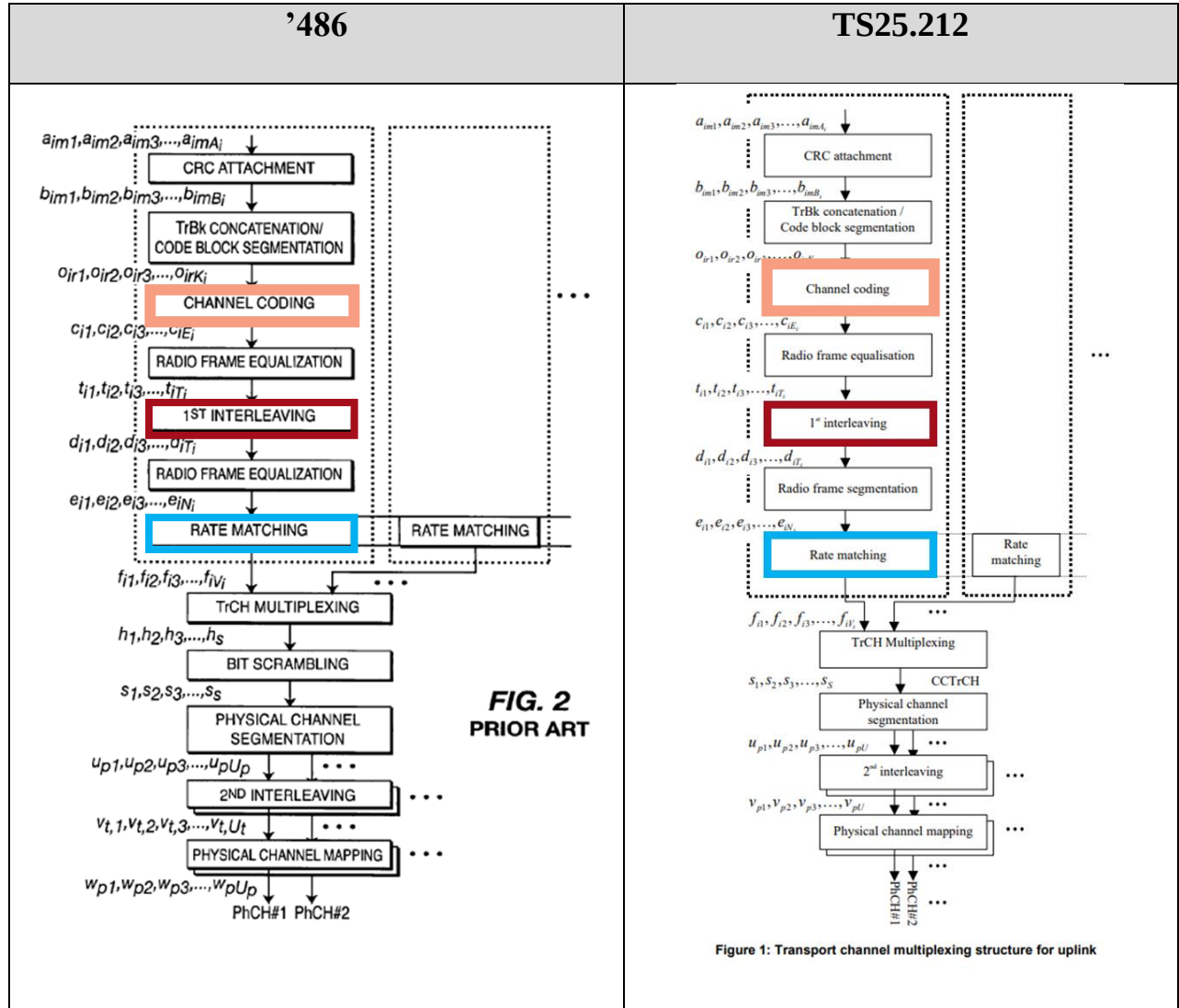
C. Ground 3: Stewart in View of TS25.212

1. “buffer[ing]” ([3.d]/[1.d]/[5.d])

TS25.212 teaches further details of “[buffering.../buffer configured to buffer/circuitry...configured to buffer] the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream” as required by ([3.d]/[1.d]/[5.d]), and thus renders obvious claims 1-6. Hochwald, ¶188.

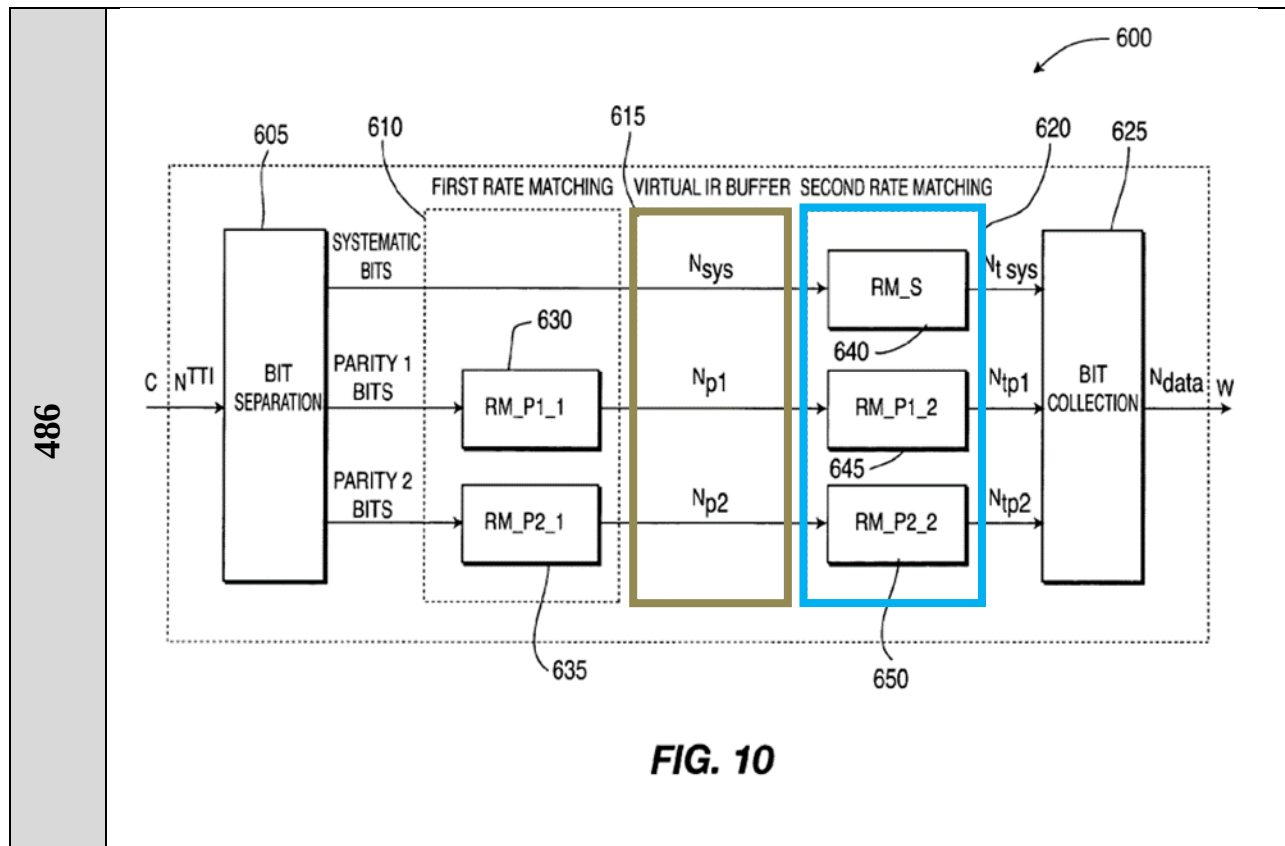
Specifically, **TS25.212** teaches **buffering the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream** (e.g., a “virtual IR buffer” stores systematic bits, first parity bits and second parity bits). TS25.212, Fig. 17, §4.5.4. Hochwald, ¶189.

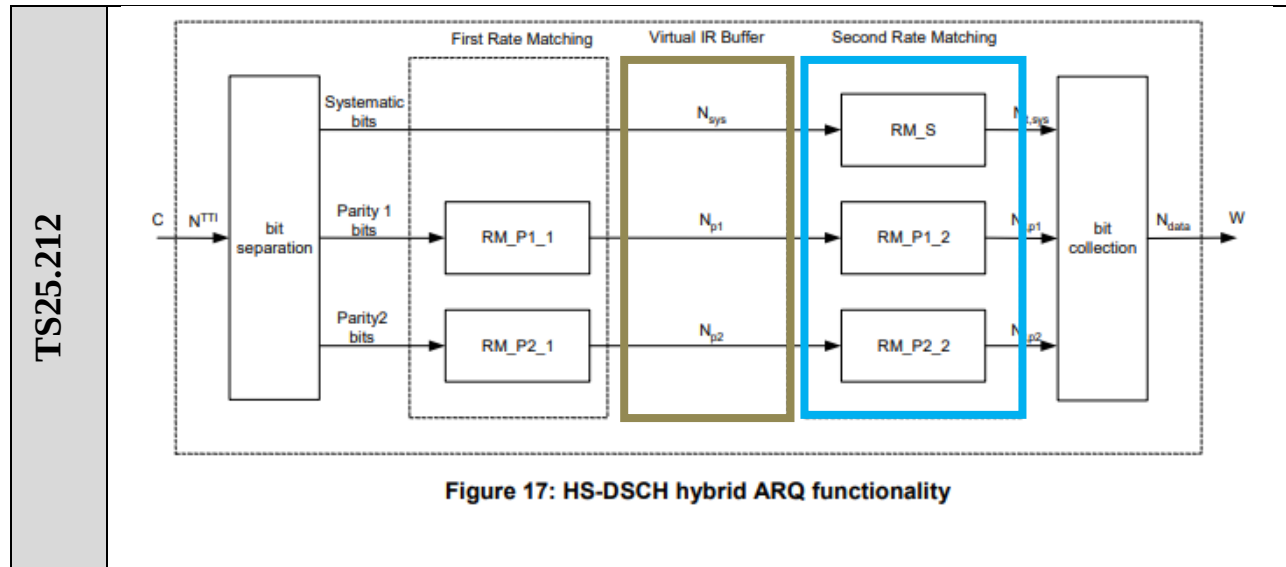
TS25.212 teaches that a **channel coding** process is followed by an **interleaving** process and a **rate matching process**, which is admitted prior art in the '486. Hochwald, ¶190. Other references also disclose this ordering, showing that it was known to a POSITA to implement interleaving before a rate matching process. US6671851 teaches that “interleaving of data should be performed after coding, but before rate matching of the data stream.” Ex. 1044. TS25.222 also teaches that such order of steps applies in the downlink and uplink. TS25.222, Fig. 1; Hochwald, ¶190.



TS25.212 teaches using a “**virtual IR buffer**” to store bits prior to a “**second rate matching**” process that “prioritise[s] systematic bits” over “non systematic bits” (e.g., parity bits) when an “RV” (redundancy version) parameter “s=0”, and that “prioritise[s]” “non systematic bits” (e.g., parity bits) over “systematic bits” when an “RV” parameter “s=1.” TS25.212, 58-59 (§§4.5.4,

4.5.4.3), Fig. 17; Hochwald, ¶191. The arrangement of the **virtual IR buffer** and **second rate matching** are annotated below in a comparison of TS25.212 Fig. 17 and the '486 Fig. 17, showing the same disclosure. Hochwald, ¶191.





TS25.212 and **Stewart** are analogous prior art and in the same field as the '486, including improvements to coding schemes for wireless communications, and reasonably pertinent to the alleged problems identified in the '486 of using redundancy versions to implement an incremental redundancy process for transmitting information between a user device and base station. *E.g.*, '486, Abstract; 4:53-5:13; Stewart, Abstract, 2:47-67, 9:60-10:3; TS25.212, Fig. 17, 58-59 (§§4.5.4, 4.5.4.3); Hochwald, ¶192.

A POSITA at least would have been motivated to modify **Stewart** with **TS25.212**'s teachings of a "virtual IR buffer" for the same reasons discussed above with respect to the combination of **Stewart** and **3GPP-Summary**. Hochwald, ¶193. Moreover, **Stewart** cites to a prior version of TS 25.212 v3.5.0 for discussions of channel coding, rate matching, and incremental redundancy and

discussions regarding structures of interleavers. Stewart, 3:4-63, 4:34-5:5. Prior to the earliest priority date of the '486 patent, 12/16/2002, a POSITA would have looked to the then published version of the technical specification, which was **TS25.212**,²⁵ which taught using a “virtual IR buffer” prior to rate matching operations that select a redundancy version and then “prioritise[s]” “systematic bits” or “non systematic bits” (e.g., parity bits) for transmission based on the redundancy version. TS25.212, Fig. 17, 58-59 (§§4.5.4, 4.5.4.3); Hochwald, ¶193. The inventors of **Stewart** also had access to and evaluated Fig. 17 from an earlier version of **TS25.212** with similar disclosure. Compare Ex. 1037, Fig. 1 with TS25.212, Fig. 17. Moreover, **3GPP-Summary** teaches using a buffer positioned after interleavers to store interleaved bits, and then selecting bits from the buffer based on redundancy versions. 3GPP-Summary, §2.4. As the '486 concedes, it was known to perform rate matching steps (e.g., shown in **TS25.212** Fig. 10) after interleaving, and thus the buffering of **TS25.212** would have been performed after **Stewart's** interleaving. '486, Fig. 2. Additionally, as noted during the prosecution of '486 counterpart EP1573923A4, the aforementioned and other portions of

²⁵ By referencing the 12/16/2002 priority date, Petitioner does not concede that any Challenged Claim is entitled to such priority date.

TS25.212 discussing the virtual IR buffer was copied into the '486 patent specification without attribution. Compare **TS25.212** Fig. 17, §§4.5.4, 4.5.4.1-3 with '486, Fig. 10, 16:17-26, 52:17:10, 18:15-19:13; see Ex. 1010, 14-16; Hochwald, ¶193.

In light of the above teachings, a POSITA would have had a reasonable expectation of success in modifying **Stewart** with **TS25.212**'s teachings by using a “virtual IR buffer” to store bits from Stewart's System Block Interleaver and Parity Block Interleavers, because a transmitter buffer was well known for “storing” bits to facilitate retransmission in an ARQ process. Ex. 1040, [0034]-[0037], [0045], Ex. 1041, 4:1-7, 4:32-58, 11:48-57, 15:30-34; Ex. 1027, ¶[0034]; Hochwald, ¶194. In the modified system, bits would be loaded from the interleavers into the virtual IR buffer to prepare for transmission, and bits would be selected from the virtual IR buffer for transmission, based on a redundancy version parameter. Modifying **Stewart** with **TS25.212**'s teachings would have been a straightforward application of those teachings in a manner that advantageously improves the reliability of the system by buffering the bits prior to transmission. Hochwald, ¶194.

2. “redundancy version[s]” ([3.e]/[1.e]/[5.e])

TS25.212 provides further details of “at least one redundancy version of the set selects first and second parity bits over systematic bits” and “at least one

redundancy version of the set selects systematic bits over first and second parity bits” as required by ([3.e], [1.e], [5.e]) for Grounds 1-3, and thus renders obvious claims 1-6. Hochwald, ¶195.

Specifically, TS25.212 teaches **selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits** (e.g., “RV parameter” “distinguish[es] between transmissions that prioritize systematic bits (s=1) and non-systematic bits (S=0)”). Hochwald, ¶196.

TS25.212 discloses selectively prioritizing systematic bits or parity bits based on an RV parameter *s*, and ’486 copied this same disclosure to support its selecting of systematic bits and parity bits based on redundancy versions. See §VIII; TS25.212, §4.5.4.3, Fig. 17; Hochwald, ¶197.

A POSITA would have been motivated to modify **Stewart** with TS25.212’s teachings of selective prioritization of systematic or parity bits based on a redundancy version for several reasons. See §IX.C.1 (analogous art). Hochwald, ¶198. First, **Stewart** cites TS25.212 for discussions of rate matching. See §IX.C.1 (motivation to combine). Hochwald, ¶199.

Second, modifying **Stewart** with these teachings is nothing more than applying known methods to yield predictable results. Hochwald, ¶200. **TS25.212** teaches a way to select systematic bits or parity bits for transmission, by dropping or “puncturing” systematic bits or priority bits that are not intended for transmission. TS25.212, §4.5.4.3, Fig. 17; Hochwald, ¶200. **Stewart** likewise teaches puncturing bits to achieve target code rates while maintaining reliable communications. Stewart, 5:47-56. A POSITA would have been motivated to modify **Stewart** with **TS25.212**’s teachings of prioritization of systematic bits and parity bits, which provides a way of selecting code rates that complements **Stewart**’s approach, for example by dropping systematic bits or parity bits to achieve a target code rate. Hochwald, ¶200.

In light of the above teachings, a POSITA would have had a reasonable expectation of success in modifying **Stewart**’s rate selection process with **TS25.212**’s teachings of selective prioritization. Hochwald, ¶201.

D. Grounds 4-6: Grounds 1-3 in further view of Motorola

Motorola teaches further details of “at least one redundancy version of the set selects first and second parity bits over systematic bits” and “at least one redundancy version of the set selects systematic bits over first and second parity

bits” as required by ([3.e], [1.e], [5.e]) for Grounds 1-3, and thus renders obvious claims 1-6. Hochwald, ¶¶202-203.

Motorola discloses the redundancy version limitations where they require selecting systematic bits before parity bits are selected, and vice-versa. Motorola, §2.2, Figs. 4-5; Hochwald, ¶¶203-204.

Motorola teaches that “to support different redundancy versions, any row may be assigned as a starting point” from which to read out bits from a “**Systematic block interleaver**” or “**Parity block interleaver**.” Motorola, §§2.1-2.2; Hochwald, ¶205. Motorola teaches, in the annotated Figure 5 below, redundancy versions boxed in **brown** in which the **starting row** is in one of the **Parity Block Interleavers** (e.g., “RV5,” “RV6,” “RV7”) and the redundancy version first selects first and second **parity bits** followed by **systematic bits**, and redundancy versions boxed in **lime green** in which the starting row is in the **Systematic Block Interleaver** (e.g., “RV0,” “RV1,” “RV2”) and the redundancy version first selects **systematic bits** followed by first and second **parity bits**. Motorola, Figure 5; Hochwald, ¶205.

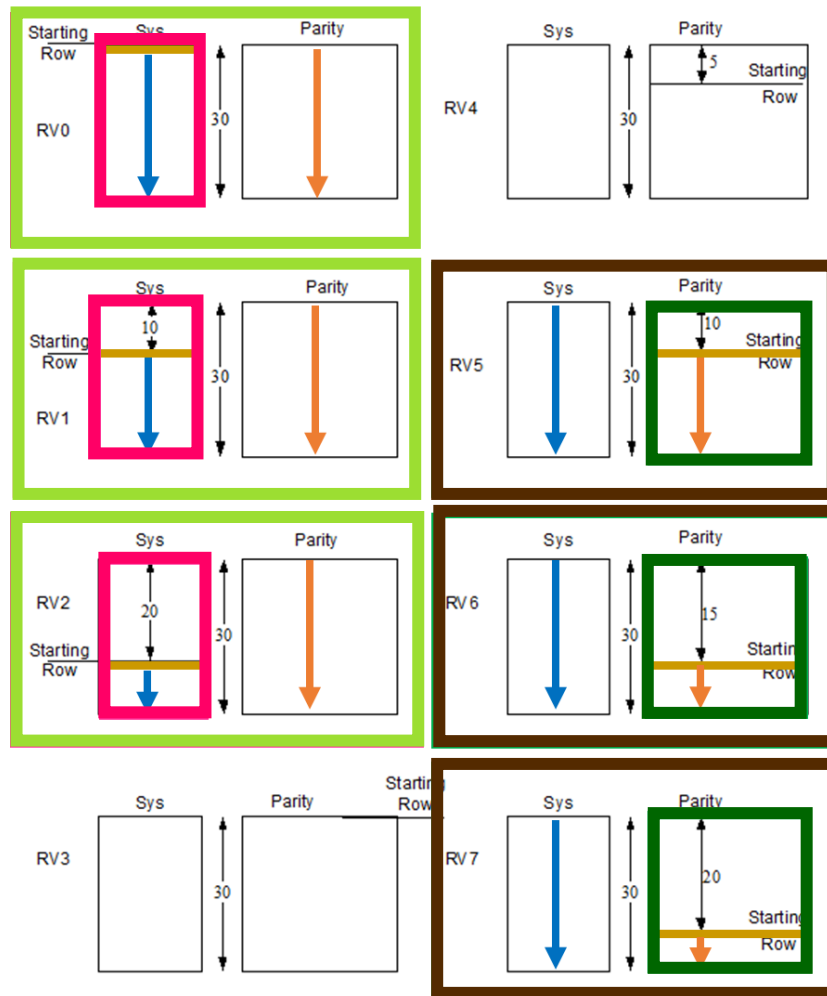


Figure 5 Redundancy versions for rate 1/3

Motorola additionally teaches a “Redundancy version wrap around” in the annotated excerpt of Figure 4(4) below, where “**reading [] continues from the first row of the other interleaver**” after all bits are read from a first interleaver starting from the **starting row**. *Id.*, §§2.1, 2.2; Hochwald, ¶206.

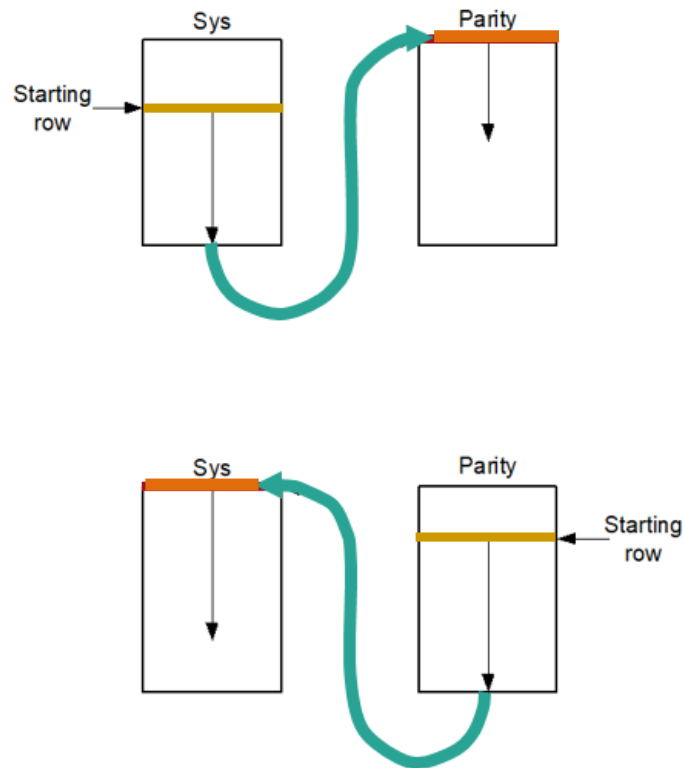


Figure 4 - Redundancy version wrap around

Motorola thus teaches a redundancy version that selects the claimed “first and second parity bits” (from a **starting row** of **Motorola’s** Parity Block Interleaver) “over systematic bits” (continuing into **Motorola’s** System Block Interleaver). *Motorola*, §§2.1-2.2, Figs. 4, 5; Hochwald, ¶207. **Motorola** likewise teaches the reverse: a redundancy version that selects the claimed “systematic bits” (from a **starting row** of **Motorola’s** Systematic Block Interleaver) “over first and second parity bits” (continuing into **Motorola’s** Parity Block Interleaver). *Id.*; Hochwald, ¶208.

Motorola additionally discloses the redundancy version limitations where they require selecting more parity bits than systematic bits for transmission and vice-versa. Hochwald, ¶209. For example, **Motorola** discloses at least one redundancy version that selects parity bits over systematic bits (*e.g.*, “RV₅” signaled with a 1/4 code rate) and at least one redundancy version that selects systematic bits over parity bits (*e.g.*, “RV₀” signaled with a 3/5 code rate), per the aforementioned requirement. Motorola, §2.2, Figs. 4-5; Hochwald, ¶209.

As another example, **Motorola** discloses “RV₀” transmits more systematic bits than parity bits “in a rate 3/5 code [such that] all systematic bits and first 10 rows of parity interleave [are] transmitted.” Motorola, 6; Hochwald, ¶210. Assuming for that (1) a same number of bits (5000) is selected for transmission with each redundancy version; (2) a number of columns of the systematic block interleaver is 100/row and each column/row position holds a bit; (3) a number of columns of the parity block interleaver is 200/row and each column/row position holds a bit; and (4) no dummy bits are added: for RV₀ and 30 systematic interleaver rows, 3,000 systematic bits (30 rows x 100 columns) are transmitted followed by 2,000 parity bits (10 rows x 200 columns). Motorola, 7; Fig. 5; Hochwald, ¶¶210-211.

As another example, “RV₆” transmits more parity bits than systematic bits when applying the same assumptions, and starting from the parity block interleaver: 3,000 parity bits (15 rows x 200 columns) followed by 2,000 systematic bits (20 rows x 100 columns). Motorola, 7; Fig. 5; Hochwald, ¶¶212-213.

Motorola, like **Stewart**, **3GPP-Summary**, and **TS25.212**, is analogous prior art and in the same field as the ’486, including improvements to coding schemes for wireless communications, and reasonably pertinent to the alleged problems identified in the ’486 of using redundancy versions to implement an incremental redundancy process for transmitting information between a user device and BS. *E.g.*, ’486, Abstract; 4:53-5:13; Stewart, Abstract, 2:47-67; Motorola, §§1, 2.2; Hochwald, ¶214.

A POSITA would have been motivated to modify **Stewart** alone, or in view of **3GPP-Summary** and/or **TS25.212**, by **Motorola’s** redundancy versions teachings. Hochwald, ¶215. **Stewart’s** redundancy versions vary starting rows in increments of $\frac{1}{4}$ of the total. Stewart, Fig. 6. **Motorola’s** redundancy versions vary starting rows in different increments (e.g., $\frac{1}{3}$ total, 10/30 rows, 20/30 rows, etc.). Motorola, Fig. 5. A POSITA would have been motivated to modify **Stewart** alone, or with **3GPP-Summary** and/or **TS25.212** to use **Motorola’s** redundancy

versions to obtain additional granularity in starting row increments (e.g., from 1/3 to 2/3 of maximum rows (in addition to Stewart's 1/4 to 3/4 increments)) between **Stewart's** Systematic Block Interleaver, First Parity Bit Interleaver, and Second Parity Bit Interleaver, that wraps around from a first interleaver to a second interleaver. Hochwald, ¶215.

Different redundancy versions support IR and HARQ procedures. Stewart, 1:57-64, 2:47-51; Ex. 1043, Abstract. Depending on the channel conditions and whether a base station correctly recovered a prior transmission, the base station benefits from a retransmission of a varying combination and ordering of systematic bits and parity bits. Stewart, 2:47-49, 2:59-64, 3:25-40, 7:44-62, 8:15-18; Ex. 1043, 1830, 1833. For example, a retransmission consists of a combination of systematic bits, followed by parity bits, in cases where a prior transmission of systematic bits was distorted. Hochwald, ¶216. As another example, in some instances a “revers[ed]” ordering of parity bits followed by systematic bits improves performance. Motorola, §§1.0, 2.0-2.2; Stewart, 8:15-30, Fig. 7. Hochwald, ¶216.

Moreover, different numbers of redundancy versions are included in a set, depending on the number of signaling bits to be used to indicate a specific redundancy version—a set of 2 requires 1 bit signaling, a set of 4 requires 2 bit

signaling, and a set of 8 requires 3 bit signaling. 3GPP-Summary, §3.2. Hochwald, ¶217.

In view of the benefits of various alternative redundancy versions, a POSITA would have been motivated to modify **Stewart**, **3GPP-Summary** and/or **TS25.212** by **Motorola's** teachings of redundancy versions. Hochwald, ¶218. For example, a POSITA would have been motivated to modify **Stewart's** set that includes a redundancy version that first transmits systematic bits followed by parity bits (*e.g.*, “RV₀”) to include **Motorola's** redundancy versions that set a starting row in a parity block interleaver (*e.g.*, “RV₅,” “RV₆,” “RV₇”) where parity bits are transmitted followed by systematic bits. Motorola, §2.2, Figs. 4-5; Stewart, 6:57-61, Hochwald, ¶218.

Additionally, a POSITA would have been motivated to modify **Stewart**, **3GPP-Summary** and/or **TS25.212** by **Motorola's** teachings in light of the similarity of the teachings and commonality of the authors and inventors. **Motorola** and **Stewart** share many of the same teachings relating to an incremental redundancy process that selects of systematic bits and parity bits. Motorola, §§1.0, 2.0-2.2, Figs. 1, 4-6; Stewart, 3:47-4:29, 5:29-8:36, Figs. 2, 3, 6, 7; *Compare* Motorola, Fig. 2 with Stewart, Fig. 4; Hochwald, ¶219. **3GPP-Summary** cites to and summarizes **Motorola**. 3GPP-Summary, §2.4, citation [4].

Moreover, **Motorola's** authors as reflected by its metadata are the same as **Stewart's** inventors. (Ex. 1045); Hochwald, ¶219.

In light of the above teachings, a POSITA would have had a reasonable expectation of success in modifying **Stewart** alone, or view of **3GPP-Summary** and/or **TS25.212** with **Motorola's** teachings to include the combinations of redundancy versions from **Stewart**, **3GPP-Summary**, **TS25.212** and/or **Motorola** in **Stewart's** system. Hochwald, ¶220. As discussed above in §IX.B, a POSITA would have recognized that the use of different redundancy versions with different starting rows from which to select bits for transmission provides additional granularity and control. Hochwald, ¶220.

If PO argues that **Motorola's** teachings are limited to a downlink, a POSITA would have been motivated to modify **Motorola's** teachings to an uplink for the same reasons discussed above in §VIII for **Stewart**, **3GPP-Summary** and **TS25.212**. See Kinjo, 6:55-64; Hochwald, ¶173.

X. SECONDARY CONSIDERATIONS

There is no evidence in the '486's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any challenged Claim. See *generally* '486 FH. Indeed, as demonstrated by the prior art referenced herein, any purported solutions to problems or unexpected results in the

'486 were already well known. Hochwald, ¶221. To the extent PO asserts the existence of any secondary considerations in its responses, Petitioner reserves the right to address any such evidence.

XI. CONCLUSION

Substantial, new, and noncumulative technical teachings have been presented for '486 Claims 1-6, which are obvious for the reasons set forth above. Hochwald, ¶¶222-226. There is a reasonable likelihood that Petitioner will prevail as to the Claims. *Inter partes* review of claims 1-6 is accordingly requested.

Respectfully submitted,

Dated: Aug. 11, 2023

By: /James L. Davis, Jr./
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CERTIFICATE OF COMPLIANCE

Pursuant to §42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,065,486 contains, as measured by the word-processing system used to prepare this paper, 13,505 words. This word count does not include the items excluded by §42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: Aug. 11, 2023

By: / Shong Yin /
Name: Shong Yin
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CERTIFICATE OF SERVICE

I hereby certify that on August 11, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,065,486 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on Patent Center:

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