

APPENDIX 7: PRELIMINARY INFRINGEMENT CONTENTIONS OF U.S. PATENT NO. 9,065,486

The Accused LGE '486 Products are those that are compatible with the LTE standard, and specifically with 3GPP TS 36.212. An exemplary identification of the Accused LGE '486 Products, based on the information presently available, is set forth in Plaintiff Pantech Corporation's Patent Rule 3-1 and 3-2 Infringement Contentions, at Section A.

The Exemplary Evidence of Infringement disclosed herein establishes that asserted claims 3 and 4 of U.S. Patent No. 9,065,486 are essential to mandatory sections of the LTE standard (i.e., 3GPP TS 36.212). If "a patent covers mandatory aspects of a standard," it is "enough to prove infringement by showing standard compliance." *Godo Kaisha IP Bridge 1 v. TCL Commun. Tech. Holdings Ltd.*, 967 F.3d 1380, 1383-84 (Fed. Cir. 2020) ("In cases involving standard essential patents, we have endorsed standard compliance as a way of proving infringement"). Based on publicly available information, the Accused LGE '486 Products comply with the LTE standard, which requires compliance with LTE cellular communication protocols including at least 3GPP TS 36.212 and perform cellular communications in compliance with the aforementioned LTE cellular communication standards. *See* Appendix 1: LGE Products Compliance with Standards.

The Exemplary Evidence of Infringement also establishes that each of the Accused LGE '486 Products contains a chipset, application processor, SoC, or system-on-chip (referred to herein as the "chipset") that incorporates a processor and/or modem. Each such chipset (and thus each accused device) complies with one or more of LTE cellular communication protocols including at least 3GPP TS 36.212. *See* Appendix 1: LGE Products Components. Furthermore, each of the Accused LGE '486 Products contains an antenna or antennas, memory, and transceiver or combination of transmitter and receiver that assist performing cellular communications in accordance with the LTE Release 10 or later cellular communication standard. *See* Appendix 1: LGE Products Components.

Thus, Appendix 1, taken together with the showing made herein, demonstrates infringement of U.S. Patent No. 9,065,486 by the Accused LGE '486 Products.

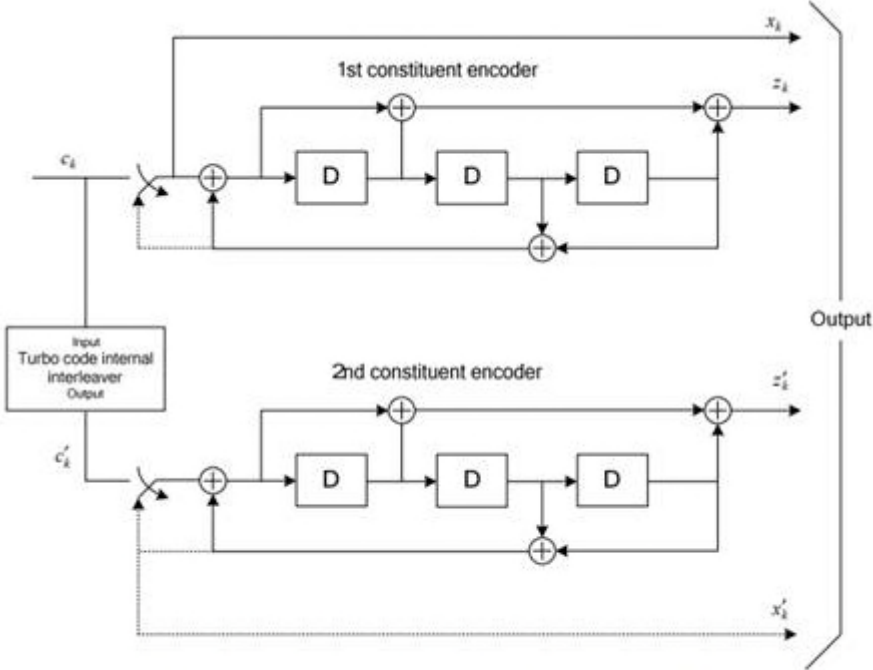
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U.S. Patent No. 9,065,486	Exemplary Evidence of Infringement
[3.pre] A method for use in an apparatus of a wireless communications comprising:	To the extent the preamble is construed as a limitation, each of the Accused LGE '486 is a smartphone for wireless communication. As shown in Appendix 1, each of the Accused LGE '486 Products incorporates a chipset, antenna or antennas, modem, and transceiver that operate in accordance with LTE cellular standard. <3GPP TS 36.212 v 10.0.0> 5.1.3 Channel coding The bit sequence input for a given code block to channel coding is denoted by $c_0, c_1, c_2, c_3, \dots, c_{K-1}$, where K is the number of bits to encode. After encoding the bits are denoted by $d_0^{(i)}, d_1^{(i)}, d_2^{(i)}, d_3^{(i)}, \dots, d_{D-1}^{(i)}$, where D is the number of encoded bits per output stream and i indexes the encoder output stream. The relation between c_k and $d_k^{(i)}$ and between K and D is dependent on the channel coding scheme. The following channel coding schemes can be applied to TrCHs: - tail biting convolutional coding; - turbo coding. TS 36.212 v10.0.0 at 11. The bits input to the turbo encoder are denoted by $c_0, c_1, c_2, c_3, \dots, c_{K-1}$, and the bits output from the first and second 8-state constituent encoders are denoted by $z_0, z_1, z_2, z_3, \dots, z_{K-1}$ and $z'_0, z'_1, z'_2, z'_3, \dots, z'_{K-1}$, respectively. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \dots, c'_{K-1}$, and these bits are to be the input to the second 8-state constituent encoder. TS 36.212 v10.0.0 at 12.

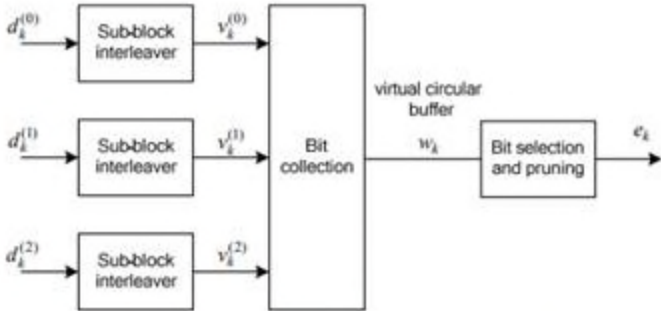
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	The output from the turbo encoder is $d_k^{(0)} = x_k$ $d_k^{(1)} = z_k$ $d_k^{(2)} = z'_k$ for $k = 0, 1, 2, \dots, K-1$. TS 36.212 v10.0.0 at 12.

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	 Figure 5.1.3-2: Structure of rate 1/3 turbo encoder (dotted lines apply for trellis termination only). TS 36.212 v10.0.0 at 13.

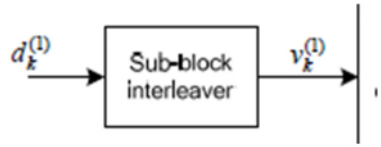
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U.S. Patent No. 9,065,486	Exemplary Evidence of Infringement
	5.1.4.1 Rate matching for turbo coded transport channels The rate matching for turbo coded transport channels is defined per coded block and consists of interleaving the three information bit streams $d_k^{(0)}$, $d_k^{(1)}$ and $d_k^{(2)}$, followed by the collection of bits and the generation of a circular buffer as depicted in Figure 5.1.4-1. The output bits for each code block are transmitted as described in section 5.1.4.1.2.  Figure 5.1.4-1. Rate matching for turbo coded transport channels. TS 36.212 v10.0.0 at 15.
[3.a] interleaving, by the apparatus, systematic bits;	Each of the Accused LGE '486 Products is a user equipment that implements interleaving systematic bits. As shown in Appendix 1, each of the Accused LGE '486 Products incorporates a chipset, memory, and modem that operate in accordance with LTE cellular standard. Each of the Accused LGE '486 Products complies with one or more of LTE Release 10 or later cellular communication protocols including at least 3GPP TS 36.212, and implements interleaving systematic bits. <3GPP TS 36.212 v 10.0.0> The bit stream $d_k^{(0)}$ is interleaved according to the sub-block interleaver defined in section 5.1.4.1.1 with an output sequence defined as $v_0^{(0)}, v_1^{(0)}, v_2^{(0)}, \dots, v_{K_{\Pi}-1}^{(0)}$ and where K_{Π} is defined in section 5.1.4.1.1.

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	<pre> graph LR A["d_k^(0)"] --> B["Sub-block interleaver"] B --> C["v_k^(0)"] </pre> TS 36.212 v10.0.0 at 15. The output from the turbo encoder is $d_k^{(0)} = x_k$ $d_k^{(1)} = z_k$ $d_k^{(2)} = z'_k$ for $k = 0, 1, 2, \dots, K-1$. TS 36.212 v10.0.0 at 12. 5.1.4.1.1 Sub-block interleaver The bits input to the block interleaver are denoted by $d_0^{(i)}, d_1^{(i)}, d_2^{(i)}, \dots, d_{D-1}^{(i)}$, where D is the number of bits. The output bit sequence from the block interleaver is derived as follows: (1) Assign $C_{subblock}^{TC} = 32$ to be the number of columns of the matrix. The columns of the matrix are numbered 0, 1, 2, ..., $C_{subblock}^{TC} - 1$ from left to right. (2) Determine the number of rows of the matrix $R_{subblock}^{TC}$, by finding minimum integer $R_{subblock}^{TC}$ such that: $D \leq (R_{subblock}^{TC} \times C_{subblock}^{TC})$ The rows of rectangular matrix are numbered 0, 1, 2, ..., $R_{subblock}^{TC} - 1$ from top to bottom.

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	TS 36.212 v10.0.0 at 15. For $d_k^{(0)}$ and $d_k^{(1)}$: (4) Perform the inter-column permutation for the matrix based on the pattern $\langle P(j) \rangle_{j \in \{0,1,\dots,C_{subblock}^{TC}-1\}}$ that is shown in table 5.1.4-1, where $P(j)$ is the original column position of the j-th permuted column. After permutation of the columns, the inter-column permuted $(R_{subblock}^{TC} \times C_{subblock}^{TC})$ matrix is equal to $\begin{bmatrix} y_{P(0)} & y_{P(1)} & y_{P(2)} & \dots & y_{P(C_{subblock}^{TC}-1)} \\ y_{P(0)+C_{subblock}^{TC}} & y_{P(1)+C_{subblock}^{TC}} & y_{P(2)+C_{subblock}^{TC}} & \dots & y_{P(C_{subblock}^{TC}-1)+C_{subblock}^{TC}} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ y_{P(0)+(R_{subblock}^{TC}-1) \times C_{subblock}^{TC}} & y_{P(1)+(R_{subblock}^{TC}-1) \times C_{subblock}^{TC}} & y_{P(2)+(R_{subblock}^{TC}-1) \times C_{subblock}^{TC}} & \dots & y_{P(C_{subblock}^{TC}-1)+(R_{subblock}^{TC}-1) \times C_{subblock}^{TC}} \end{bmatrix}$ TS 36.212 v10.0.0 at 16.
[3.b] interleaving, by the apparatus, a first parity bit stream;	Each of the Accused LGE '486 Products is a user equipment that implements interleaving a first parity bit. As shown in Appendix 1, each of the Accused LGE '486 Products incorporates a chipset, memory, and modem that operate in accordance with LTE cellular standard. Each of the Accused LGE '486 Products complies with one or more of LTE Release 10 or later cellular communication protocols including at least 3GPP TS 36.212, and implements interleaving a first parity bit. <3GPP TS 36.212 v 10.0.0> The bit stream $d_k^{(1)}$ is interleaved according to the sub-block interleaver defined in section 5.1.4.1.1 with an output sequence defined as $v_0^{(1)}, v_1^{(1)}, v_2^{(1)}, \dots, v_{K_{II}-1}^{(1)}$. 

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	5.1.4.1.1 Sub-block interleaver The bits input to the block interleaver are denoted by $d_0^{(i)}, d_1^{(i)}, d_2^{(i)}, \dots, d_{D-1}^{(i)}$, where D is the number of bits. The output bit sequence from the block interleaver is derived as follows: (1) Assign $C_{subblock}^{TC} = 32$ to be the number of columns of the matrix. The columns of the matrix are numbered 0, 1, 2, ..., $C_{subblock}^{TC} - 1$ from left to right. (2) Determine the number of rows of the matrix $R_{subblock}^{TC}$, by finding minimum integer $R_{subblock}^{TC}$ such that: $D \leq (R_{subblock}^{TC} \times C_{subblock}^{TC})$ The rows of rectangular matrix are numbered 0, 1, 2, ..., $R_{subblock}^{TC} - 1$ from top to bottom. TS 36.212 v10.0.0 at 15. The output from the turbo encoder is $d_k^{(0)} = x_k$ $d_k^{(1)} = z_k$ $d_k^{(2)} = z'_k$ for $k = 0, 1, 2, \dots, K-1$. TS 36.212 v10.0.0 at 12.

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	For $d_k^{(0)}$ and $d_k^{(1)}$: (4) Perform the inter-column permutation for the matrix based on the pattern $\langle P(j) \rangle_{j \in \{0, 1, \dots, C_{subblock}^{TC} - 1\}}$ that is shown in table 5.1.4-1, where $P(j)$ is the original column position of the j-th permuted column. After permutation of the columns, the inter-column permuted $(R_{subblock}^{TC} \times C_{subblock}^{TC})$ matrix is equal to $\begin{bmatrix} y_{P(0)} & y_{P(1)} & y_{P(2)} & \dots & y_{P(C_{subblock}^{TC}-1)} \\ y_{P(0)+C_{subblock}^{TC}} & y_{P(1)+C_{subblock}^{TC}} & y_{P(2)+C_{subblock}^{TC}} & \dots & y_{P(C_{subblock}^{TC}-1)+C_{subblock}^{TC}} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ y_{P(0)+(R_{subblock}^{TC}-1) \times C_{subblock}^{TC}} & y_{P(1)+(R_{subblock}^{TC}-1) \times C_{subblock}^{TC}} & y_{P(2)+(R_{subblock}^{TC}-1) \times C_{subblock}^{TC}} & \dots & y_{P(C_{subblock}^{TC}-1)+(R_{subblock}^{TC}-1) \times C_{subblock}^{TC}} \end{bmatrix}$ TS 36.212 v10.0.0 at 16.
[3.c] interleaving, by the apparatus, a second parity bit stream;	Each of the Accused LGE '486 Products is a user equipment that implements interleaving a second parity bit. As shown in Appendix 1, each of the Accused LGE '486 Products incorporates a chipset, memory, and modem that operate in accordance with LTE cellular standard. Each of the Accused LGE '486 Products complies with one or more of LTE Release 10 or later cellular communication protocols including at least 3GPP TS 36.212, and implements interleaving a second parity bit. <3GPP TS 36.212 v 10.0.0> The bit stream $d_k^{(2)}$ is interleaved according to the sub-block interleaver defined in section 5.1.4.1.1 with an output sequence defined as $v_0^{(2)}, v_1^{(2)}, v_2^{(2)}, \dots, v_{K_{\Pi}-1}^{(2)}$. <pre> graph LR A["d_k^(2)"] --> B["Sub-block interleaver"] B --> C["v_k^(2)"] style C fill:none,stroke:none </pre>

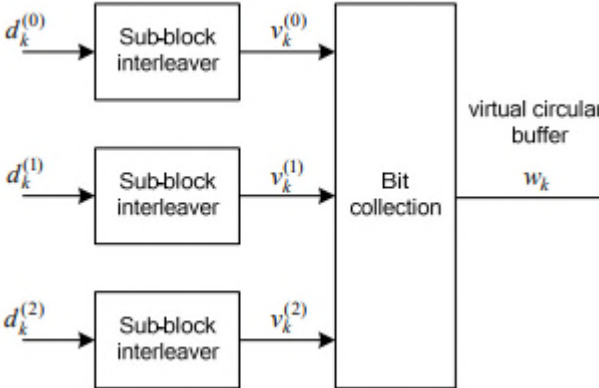
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	5.1.4.1.1 Sub-block interleaver The bits input to the block interleaver are denoted by $d_0^{(i)}, d_1^{(i)}, d_2^{(i)}, \dots, d_{D-1}^{(i)}$, where D is the number of bits. The output bit sequence from the block interleaver is derived as follows: (1) Assign $C_{subblock}^{TC} = 32$ to be the number of columns of the matrix. The columns of the matrix are numbered 0, 1, 2, ..., $C_{subblock}^{TC} - 1$ from left to right. (2) Determine the number of rows of the matrix $R_{subblock}^{TC}$, by finding minimum integer $R_{subblock}^{TC}$ such that: $D \leq (R_{subblock}^{TC} \times C_{subblock}^{TC})$ The rows of rectangular matrix are numbered 0, 1, 2, ..., $R_{subblock}^{TC} - 1$ from top to bottom. TS 36.212 v10.0.0 at 15. The output from the turbo encoder is $d_k^{(0)} = x_k$ $d_k^{(1)} = z_k$ $d_k^{(2)} = z'_k$ for $k = 0, 1, 2, \dots, K-1$. TS 36.212 v10.0.0 at 12.

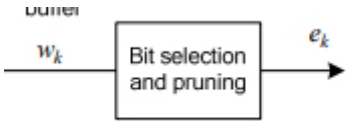
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U.S. Patent No. 9,065,486	Exemplary Evidence of Infringement				
	For $d_k^{(2)}$: (4) The output of the sub-block interleaver is denoted by $v_0^{(2)}, v_1^{(2)}, v_2^{(2)}, \dots, v_{K_{\Pi}-1}^{(2)}$, where $v_k^{(2)} = y_{\pi(k)}$ and where $\pi(k) = \left(P \left(\left\lfloor \frac{k}{R_{subblock}^{TC}} \right\rfloor \right) + C_{subblock}^{TC} \times (k \bmod R_{subblock}^{TC}) + 1 \right) \bmod K_{\Pi}$ The permutation function P is defined in Table 5.1.4-1. Table 5.1.4-1 Inter-column permutation pattern for sub-block interleaver. <table border="1" data-bbox="726 656 1673 789"> <thead> <tr> <th data-bbox="726 656 1058 732">Number of columns $C_{subblock}^{TC}$</th><th data-bbox="1058 656 1673 732">Inter-column permutation pattern $\langle P(0), P(1), \dots, P(C_{subblock}^{TC} - 1) \rangle$</th></tr> </thead> <tbody> <tr> <td data-bbox="726 732 1058 789" style="text-align: center;">32</td><td data-bbox="1058 732 1673 789" style="text-align: center;">$\langle 0, 16, 8, 24, 4, 20, 12, 28, 2, 18, 10, 26, 6, 22, 14, 30, 1, 17, 9, 25, 5, 21, 13, 29, 3, 19, 11, 27, 7, 23, 15, 31 \rangle$</td></tr> </tbody> </table> TS 36.212 v10.0.0 at 16.	Number of columns $C_{subblock}^{TC}$	Inter-column permutation pattern $\langle P(0), P(1), \dots, P(C_{subblock}^{TC} - 1) \rangle$	32	$\langle 0, 16, 8, 24, 4, 20, 12, 28, 2, 18, 10, 26, 6, 22, 14, 30, 1, 17, 9, 25, 5, 21, 13, 29, 3, 19, 11, 27, 7, 23, 15, 31 \rangle$
Number of columns $C_{subblock}^{TC}$	Inter-column permutation pattern $\langle P(0), P(1), \dots, P(C_{subblock}^{TC} - 1) \rangle$				
32	$\langle 0, 16, 8, 24, 4, 20, 12, 28, 2, 18, 10, 26, 6, 22, 14, 30, 1, 17, 9, 25, 5, 21, 13, 29, 3, 19, 11, 27, 7, 23, 15, 31 \rangle$				
[3.d] buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and	Each of the Accused LGE '486 Products is a user equipment that implements buffering the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream. As shown in Appendix 1, each of the Accused LGE '486 Products incorporates a chipset, memory, and modem that operate in accordance with LTE cellular standard. Each of the Accused LGE '486 Products complies with one or more of LTE Release 10 or later cellular communication protocols including at least 3GPP TS 36.212, and implements buffering the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream. <3GPP TS 36.212 v 10.0.0> The bits are collected in a circular buffer.				

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	The rate matching for turbo coded transport channels is defined per coded block and consists of interleaving the three information bit streams $d_k^{(0)}$, $d_k^{(1)}$ and $d_k^{(2)}$, followed by the collection of bits and the generation of a circular buffer as depicted in Figure 5.1.4-1. The output bits for each code block are transmitted as described in section 5.1.4.1.2.  TS 36.212 v10.0.0 at 15. The circular buffer of length $K_w = 3K_\Pi$ for the r-th coded block is generated as follows: $w_k = v_k^{(0)} \quad \text{for } k = 0, \dots, K_\Pi - 1$ $w_{K_\Pi + 2k} = v_k^{(1)} \quad \text{for } k = 0, \dots, K_\Pi - 1$

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	$w_{K_{II}+2k+1} = v_k^{(2)} \text{ for } k = 0, \dots, K_{II} - 1$ Denote the soft buffer size for the transport block by N_{IR} bits and the soft buffer size for the r-th code block by N_{cb} bits. The size N_{cb} is obtained as follows, where C is the number of code blocks computed in section 5.1.2: - $N_{cb} = \min\left(\left\lfloor \frac{N_{IR}}{C} \right\rfloor, K_w\right)$ for DL-SCH and PCH transport channels - $N_{cb} = K_w$ for UL-SCH and MCH transport channels TS 36.212 v10.0.0 at 16-17
[3.e] selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.	Each of the Accused LGE '486 Products is a user equipment that implements selecting bits for transmission based on a plurality of redundancy versions where at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits. As shown in Appendix 1, each of the Accused LGE '486 Products incorporates a chipset, memory, and modem that operate in accordance with LTE cellular standard. Each of the Accused LGE '486 Products complies with one or more of LTE Release 10 or later cellular communication protocols including at least 3GPP TS 36.212, and implements selecting bits for transmission based on a plurality of redundancy versions where at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits. <3GPP TS 36.212 v 10.0.0> A bit selection and pruning is performed  <pre> graph LR wk[w_k] --> BSP[Bit selection and pruning] BSP --> ek[e_k] </pre> TS 36.212 v10.0.0 at 15.

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	Denoting by E the rate matching output sequence length for the r-th coded block, and rv_{idx} the redundancy version number for this transmission ($rv_{idx} = 0, 1, 2$ or 3), the rate matching output bit sequence is $e_k, k = 0, 1, \dots, E-1$. Set $k_0 = R_{subblock}^{TC} \cdot \left(2 \cdot \left\lceil \frac{N_{cb}}{8R_{subblock}^{TC}} \right\rceil \cdot rv_{idx} + 2 \right)$, where $R_{subblock}^{TC}$ is the number of rows defined in section 5.1.4.1.1. Set $k = 0$ and $j = 0$ while $\{ k < E \}$ if $w_{(k_0+j) \bmod N_{cb}} \neq \text{NULL}$ $e_k = w_{(k_0+j) \bmod N_{cb}}$ $k = k + 1$ end if $j = j + 1$ end while TS 36.212 v10.0.0 at 17-18.
4. The method of claim 3 wherein the selecting of bits for transmission in response to a selected redundancy version changes in response to a location of the bits in the buffer.	Each of the Accused LGE '486 Products is a user equipment that implements selecting of bits for transmission in response to a selected redundancy version changes in response to a location of the bits in the buffer. As shown in Appendix 1, each of the Accused LGE '486 Products incorporates a chipset, memory, and modem that operate in accordance with LTE cellular standard. Each of the Accused LGE '486 Products complies with one or more of LTE Release 10 or later cellular communication protocols including at least 3GPP TS 36.212, and implements selecting of bits for transmission in response to a selected redundancy version changes in response to a location of the bits in the buffer. <3GPP TS 36.212 v 10.0.0>

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	$\text{Set } k_0 = R_{subblock}^{TC} \cdot \left(2 \cdot \left\lceil \frac{N_{cb}}{8R_{subblock}^{TC}} \right\rceil \cdot rv_{idx} + 2 \right), \text{ where } R_{subblock}^{TC} \text{ is the number of rows defined in section 5.1.4.1.1.}$ TS 36.212 v10.0.0 at 17. $e_k = w_{(k_0+j) \bmod N_{cb}}$ TS 36.212 v10.0.0 at 18.