

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS INC.,
Petitioner,

v.

PANTECH WIRELESS LLC,
Patent Owner

Case: IPR2023-01272

U.S. Patent No. 9,065,486

PATENT OWNER PRELIMINARY RESPONSE

Mail Stop **Patent Board**
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. BACKGROUND	3
A. Overview of the '486 Patent Invention	3
B. Relevant '486 Patent Prosecution History	5
C. Summary of Petitioner's Proposed Grounds of Unpatentability and the References Cited.....	8
D. Petitioner's Relied-Upon References.....	9
1. Overview of Stewart (Ex. 1005)	9
2. Overview of Motorola (Ex. 1006)	10
3. Overview of 3GPP-Summary (Ex. 1007).....	11
4. Overview of TS 25.212 (Ex. 1008).....	11
III. CLAIM CONSTRUCTION	12
IV. LEGAL STANDARDS FOR INVALIDITY	12
V. DISCRETIONARY FACTORS FAVOR DENIAL OF INSTITUTION	14
A. Application of <i>Fintiv</i> Factors Weighs in Favor of Denying Institution.....	15
1. The Court Has Not Stayed The Underlying Litigation Nor Has a Motion to Stay Been Filed.....	16
3. The Parties Have Invested Substantial Efforts in Litigating the Grounds Presented in this Petition in the District Court Action.....	19
4. Petitioner Fails To Offer A Sotera Stipulation And There Is Significant Overlap Between Issues Raised In The Petition And In The District Court Litigation.....	20
5. LGE is Both Petitioner and Defendant	21

6.	Other Circumstances Also Weigh in Favor of Discretionary Denial	21
VI.	THE PETITION DOES NOT SHOW A REASONABLE likelihood OF PREVAILING WITH RESPECT TO ANY CHALLENGED CLAIM.....	23
A.	Ground 1: Petitioner Fails To Establish That Claims 1-6 are Anticipated AND/OR Rendered Obvious By Stewart.....	23
1.	Stewart fails to disclose claim element [3.d] “buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream”	23
2.	Stewart fails to disclose claim element [3.e] “selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions...”	26
B.	Grounds 2: Petitioner Failed To Establish That Claims 1-6 are Rendered Obvious By Stewart in View of 3GPP-Summary	28
C.	Grounds 3: Petitioner Failed To Establish That Claims 1-6 are Rendered Obvious Over Stewart in view of TS 25.212.....	30
D.	Ground 4-6: Petitioner Failed To Establish That Claims 1-6 are Rendered Obvious Over Stewart in view of Motorola	32
VII.	CONCLUSION.....	35

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020)	14
<i>Cuozzo Speed Techs., LLC v. Lee</i> , 136 S. Ct. 2131 (2016)	15
<i>Gen. Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha</i> , IPR2016-01357, Paper 19 (PTAB Sept. 6, 2017)	1, 14
<i>Graham v. John Deere Co.</i> , 383 US 1 (1966)	13
<i>Harmonic Inc. v. Avid Tech.</i> , 815 F.3d 1356 (Fed. Cir. 2016)	15
<i>Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.</i> , 821 F.3d 1359 (Fed. Cir. 2016)	13
<i>InTouch Techs., Inc. v. VGo Commc'ns, Inc.</i> , 751 F.3d 1327 (Fed. Cir. 2014)	14
<i>Kirsch Research and Development LLC v. DuPont de Nemours, Inc.</i> , Dkt. 269, No. 5-20-cv-00057-RWS (E.D. Tex. July 7, 2021)	17
<i>KSR Int'l Co. v. Teleflex Inc.</i> , 550 US 398 (2007)	13
<i>Maxell Ltd. v. Apple Inc.</i> , No. 5:19-CV-00036-RWS, 2020 U.S. Dist. LEXIS 257531 (E.D. Tex. April 27, 2020)	17
<i>Medichem, S.A. v. Rolabo, S.L.</i> , 437 F.3d 1157 (Fed. Cir. 2006)	13
<i>Pantech Corp. v. LG Electronics Inc.</i> , No. 5:22-cv-00113-RWS, Dkt. 131 (E.D. Tex., July 19, 2023)	17

Case IPR2023-01272
Patent No. 9,065,486
Patent Owner Preliminary Response

<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005)	12
<i>Sand Revolution II, LLC v. Continental Intermodal Group-Trucking LLC</i> , IPR 2019-01393, Paper 24 (PTAB June 16, 2020)	16
<i>Schering Corp. v. Geneva Pharms.</i> , 339 F.3d 1373 (Fed. Cir. 2003)	12
Statutes	
35 U.S.C. § 103(a)	12

PATENT OWNER’S EXHIBIT LIST

Exhibit No.	Description
2001	January 13, 2023 Declaration of Jamie B. Beaber (Confidential)
2002	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 1 (Complaint).
2003	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 15 (LGE SEALED Motion to Disqualify) (Confidential).
2004	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 93 (Magistrate Order Regarding LGE’s Motion for Disqualification) (Confidential).
2005	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 160 (Order Regarding LGE’s Motion for Disqualification) (Confidential).
2006	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 102 (SEALED Defendants’ Rule 72 Objections to the Order Regarding Disqualification) (Confidential).
2007	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 103 (SEALED Pantech Objections to Order Denying DQ) (Confidential).
2008	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 111 (SEALED Pantech Response to LGE Objections to Order Denying Disqualification) (Confidential).
2009	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 113 (SEALED LGE’s Opposition to Plaintiffs’ Rule 72 Objections) (Confidential).

Case IPR2023-01272
Patent No. 9,065,486
Patent Owner Preliminary Response

2010	(Reserved)
2011	November 18, 2019 Declaration of Juseong Ryu (Confidential)
2012	ABA Formal Opinion #05-436
2013	3GPP TS 36.321
2014	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 45 (Pantech’s Response to LGE’s Motion to Disqualify) (Confidential).
2015	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 54 (SEALED Reply ISO Motion to Disqualify) (Confidential).
2016	<i>Pantech Corp. v. LG Electronics Inc.</i> , Case No. 5:22-cv-00113 (E.D. Tex.), Dkt. 60 (SEALED Sur-reply ISO Response to Motion to Disqualify Mayer Brown) (Confidential).
2017	Scheduling Order from <i>Pantech Corp. v. LG Electronics, Inc.</i> , No. 5:22-cv-00113-RWS, Dkt. 240 (E.D. Tex., Jan. 22, 2024)
2018	Invalidity Contentions from <i>Pantech Corp. v. LG Electronics Inc.</i> , No. 5:22-cv-00113-RWS (E.D. Tex. April 13, 2023)

I. INTRODUCTION

Patent Owner Pantech Wireless LLC (“Patent Owner”) respectfully requests that the United States Patent and Trademark Office (“USPTO” or the “Office”) Patent Trial and Appeal Board (“PTAB” or the “Board”) deny institution of claims 1-6 (the “challenged claims”) of U.S. Patent No. 9,065,486 (“the ’486 Patent”).

First, discretionary denial pursuant to 35 U.S.C. § 314(a) is appropriate. Petitioner LG Electronics, Inc. (hereinafter “Petitioner” or “LGE”) has failed to account for the advanced stage of the co-pending district court litigation between the parties or the fact that the very same grounds of alleged invalidity are being challenged in that matter. In fact, trial in *Pantech Corp. v. LG Electronics Inc.*, No. 5:22-cv-00113-RWS (E.D. Tex.) is scheduled for September 2024, before even a reply would be due from Petitioner (late October 2024), and expert discovery will conclude prior to any institution decision. Petitioner has not offered any *Sotera*-type stipulation to alleviate concerns of duplicative litigation, nor is a stay likely in the district court. Accordingly, institution would not provide an “effective and efficient alternative” to litigation, as is the goal of *inter partes* review. See *Gen. Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16-17 (PTAB Sept. 6, 2017) (precedential).

Additionally, there is no reasonable likelihood that Petitioner would prevail on any Ground. Petitioner seems to at least implicitly recognize that its primary reference for every ground, Stewart, fails to at least explicitly disclose at least the claimed “buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream” required for every challenged claim. Petitioner attempts to fill the gaps with the supposed knowledge of a POSITA and/or teachings of secondary references. *See* Petition at 35. But at best, Petitioner has only offered conclusory arguments or unsupported statements from its expert simply parroting these arguments, which fail to meet the requisite burden of showing anticipation or obviousness. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”). As addressed below, the references cited by Petitioner simply do not support its arguments, and thus there is no reasonable likelihood that Petitioner will be successful as to any challenged claim.

Accordingly, for at least these reasons, the Board should decline to institute *inter partes* review.

II. BACKGROUND

A. Overview of the '486 Patent Invention

The '486 Patent has a priority date of December 16, 2002, and is titled “Detection, avoidance and/or correction of problematic puncturing patterns in parity bit streams used when implementing turbo codes.” *See* Ex. 1001.

The '486 Patent generally relates to wireless communications within radio networks, and specifically relates to detecting, avoiding and/or correcting problematic puncturing patterns in parity bit streams when implementing punctured turbo codes without having to avoid desirable code rates. '486 Patent at Abstract. Specifically, the '486 Patent provides a method for detecting and correcting performance degradation in punctured turbo codes using a turbo encoder. *Id.* at 1:28-31.

Turbo codes are a form of parallel, recursive systematic convolution codes, which can be used for channel coding and decoding in order to detect and correct errors that may occur in the transmission of digital data through different channels. *Id.* at 2:64-67. Turbo codes are particularly useful for data transfers in which, under certain conditions, the data transfer rate can approach the theoretical limits of Shannon’s Law. *Id.* at 3:1-3.

Prior to the invention of the '486 Patent, high-rate turbo codes were created by puncturing, such that eliminating parity bits of lower-rate code until the desired code rate is attained. *Id.* at 3:10-12. But conventional turbo encoding had performance problems. As discussed by the '486 Patent,

Particular codes created by puncturing exhibit poorer than expected performance due to certain punctured bit patterns. Because the recursive encoding blocks in a Turbo encoder have an infinite impulse response, information about each systematic bit is distributed across many of the parity bits. In any error control coding scheme that employs puncturing, the location of the punctured bits will have an impact on performance. This is because puncturing strings of successive bits can be viewed as burst errors by the decoder. All error control mechanisms can only correct burst errors that are less than some threshold.

Id. at 3:12-23. In other words, it is important when designing the puncturing scheme for turbo codes that the burst error correcting abilities of the code be considered. *Id.* at 3:23-25.

The '486 Patent addresses these problems by disclosing methods and apparatus in which the “degradations in quality of punctured error correction coded transmissions are identified and the code transmissions are modified accordingly. A

puncturing pattern which approximates a particular code rate is identified, and a value for anticipated degradation is adjusted in accordance with a matching of the puncturing pattern and the particular code rate.” *Id.* at 4:53-59.

B. Relevant ’486 Patent Prosecution History

The patent application that led to the issuance of the ’486 Patent was quickly approved. In the only notable office action, the Examiner merely rejected claims 1-6 based on double patenting. Ex. 1002 (’486 Patent File History) at 87-90. The Patent Owner subsequently filed a terminal disclaimer, and as a result, the Examiner issued a notice of allowance on February 17, 2015. *Id.* at 118.

Family members of the ’486 Patent have also been examined, setting the foundations for the patentable subject matter in the ’486 Patent. Specifically, the applications of several related patents (U.S. Patent Nos. 8,359,520; 8,074,143; and 7,293,217) of ’486 Patent were thoroughly examined by the same Examiner prior to examination of the application that led to the ’486 Patent.

This prior history shows close consideration of the prior art. For example, during the prosecution of the application that led to U.S. Patent No. 7,293,217 (“the ’217 Patent”), the Examiner issued an office action on December 18, 2006, rejecting various claims under 35 U.S.C. § 102, citing U.S. Pat. No. 6,622,281 (“Yun”). *See* Ex. 1016 (’217 Patent File History), Non-Final Rejection (Dec. 18, 2006) at 2.

Case IPR2023-01272
Patent No. 9,065,486
Patent Owner Preliminary Response

Along with Yun, the Examiner specifically cited the following references in the rejection:

Notice of References Cited	Application/Control No. 10/725,779	Applicant(s)/Patent Under Reexamination PIETRASKI ET AL.	
	Examiner Fritz Alphonse	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,601,214	07-2003	Hammons, Jr., A. Roger	714/790
*	B	US-6,665,813	12-2003	Forsman et al.	714/15
*	C	US-6,622,281	09-2003	Yun et al.	714/790
*	D	US-2002/0027956	03-2002	Lee et al.	375/262
*	E	US-7,076,726	07-2006	Yun et al.	714/790
*	F	US-2002/0141433	10-2002	Kwon et al.	370/441
*	G	US-2003/0007476	01-2003	Kim et al.	370/342
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

See '217 Patent File History, List of references cited by examiner (Dec. 18, 2006).

In response, the Applicant amended the claims to incorporate the allowable subject matter by the Examiner into independent claims. On June 12, 2007, the Examiner specifically cited the following references in the notice of allowance:

Case IPR2023-01272
Patent No. 9,065,486
Patent Owner Preliminary Response

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				ATTY. DOCKET NO. I-2-0526.1US		SERIAL NO. 10/725,779	
				APPLICANT Pietraski et al.			
				FILING DATE December 2, 2003		GROUP 2133	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
FA	6,370,669	04/2002	Eroz et al.				
FA	6,601,214	07/2003	Hammons, Jr.				
FA	6,622,281	09/2003	Yun et al.				
FA	6,665,813	12/2003	Forsman et al.				
FA	7,076,726	07/2006	Yun et al.				
FA	2002/0027956	03/2002	Lee et al.				
FA	2002/0141433	10/2002	Kwon et al.				
FA	2003/0007476	01/2003	Kim et al.				
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO	
FA	* 00/11791	03/2000	WO			X ¹	
FA	* 00/41343	07/2000	WO			X ²	
FA	* 02/33910	04/2002	WO			X ³	
FA	* 03/069784	08/2003	WO			X ⁴	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
FA	Mo et al., "Analysis of Puncturing Pattern for High Rate Turbo Codes," IEEE International, 0-7803-5538-5/99, 1999, pgs. 547-550.						
FA	3GPP TS 25.212 v6.1.0 (2004-03), 3 rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD) (Release 6).						
FA	3GPP TS 25.222 v6.0.0 (2003-12), 3 rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (TDD) (Release 6).						
FA	3GPP TS 25.944 v4.1.0 (2001-06), 3 rd Generation Partnership Project; Technical Specification Group Radio Access Network; Channel coding and multiplexing examples (Release 4).						
X ¹	Equivalent to RU 2190296						
X ²	Equivalent to RU 2185025						
X ³	Equivalent to RU 2239292						
X ⁴	Equivalent to RU 2004127246						
EXAMINER /Fritz Alphonse/				DATE CONSIDERED 05/17/2007			

See '217 Patent File History, List of References cited by applicant and considered by examiner (June 12, 2007). In addition, these references were also considered by the same Examiner during the prosecution of other related patents, namely U.S.

Patent No. 8,359,520 and U.S. Patent No. 8,074,143. *See* Ex. 1017 at 49; Ex. 1018 at 5.

Thus, as evidenced by the prosecution history of the '486 Patent and related patents, there was careful consideration by the Office of substantially the same prior art prior as cited in the Petition.

C. Summary of Petitioner's Proposed Grounds of Unpatentability and the References Cited

Petitioner contends that claims 1-6 would have been anticipated under pre-AIA 35 U.S.C. § 102. Petitioner further contends that claims 1-6 would have been obvious under pre-AIA 35 U.S.C. § 103. The Petition raises these grounds of alleged anticipation and/or obviousness based on four separate references:

1. US 7,260,770 ("Stewart");
2. R1-01-1014/R1-01-1081 ("Motorola");
3. R1-01-1047 ("3GPP-Summary");
4. TS25.212 v5.1.0 ("TS 25.212")

Specifically, the Petition asserts the following grounds of alleged invalidity:

Ground	Basis	Claims	References
1	§§102/103	1-6	Stewart

2	§103	1-6	Stewart in view of 3GPP-Summary
3	§103	1-6	Stewart in view of TS 25.212
4	§103	1-6	Stewart in view of Motorola
5	§103	1-6	Stewart in view of 3GPP-Summary and Motorola
6	§103	1-6	Stewart in view of TS 25.212 and Motorola

D. Petitioner’s Relied-Upon References

The four references relied upon by Petitioner to challenge the patentability of claims 1-6 of the ’486 Patent are summarized as follows:

1. Overview of Stewart (Ex. 1005)

U.S. Patent No. 7,260,770 (“Stewart”) is entitled “Block puncturing for turbo code based incremental redundancy” and was published on August 21, 2007.

Stewart is directed to “a method of block puncturing for turbo code based incremental redundancy includes a first step (1200) of coding an input data stream into systematic bits and parity bits” and includes “loading the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner” and “outputting bits from the block interleavers in a row-wise manner in accordance with the selected predefined redundancy.” *See* Ex. 1005 at Abstract.

Stewart discloses channel coding that outputs systematic bits and parity bits that are generated from the systematic bits. Stewart at 1:32-43. Stewart also discloses

interleaving of systematic and parity bits and outputting these bits for transmission. Stewart 1:44-48.

However, as explained below, Stewart does not disclose buffering the systematic bits and the parity bits. In contrast, Stewart discloses buffering tail bits for subsequent transmission and not the interleaved systematic and parity bits. *See* Stewart at 4:31-34.

2. Overview of Motorola (Ex. 1006)

3GPP submission entitled “A New Hybrid-ARQ Scheme Using Incremental Redundancy,” (“Motorola”) was allegedly submitted by Motorola for 3GPP Meeting R1-ah-22010 (Nov 5-7, 2001).

Motorola provides a simple incremental redundancy (IR) scheme based on block interleaving and symbol priority. *See* Ex. 1006 at 1. The scheme includes a flexible and fine-grained support of predefined redundancy versions at each transmission with progressive reduction in effective coding rates. *Id.*

As explained below, Motorola does not disclose buffering the systematic bits and the parity bits. Specifically, Figure 1 of Motorola is substantially the same as Figure 3 of Stewart, and does not provide a different method of transmission.

3. Overview of 3GPP-Summary (Ex. 1007)

3GPP submission entitled “Overview of Proposed Schemes for Incremental Redundancy,” (“3GPP-Summary”) was allegedly submitted by Ericsson for 3GPP Meeting R1-ah-22010 (Nov 5-7, 2001).

3GPP-Summary is directed to providing a summary of proposals related to the IR scheme to be used for HSDPA. It compares the IR schemes and does not address the modulation aspects as these are covered by other contributions. *See* 3GPP-Summary at 1.

As explained below, 3GPP-Summary does not explain what specific structure constitutes the buffer. Moreover, to the extent that bits are selected from the buffer of the 3GPP-Summary for purpose of transmission, the selection of bits for transmission is not based on redundancy versions.

4. Overview of TS 25.212 (Ex. 1008)

TS 25.212 is a 3GPP Technical Specification titled “Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD)” and bearing a date of June, 2002. Ex. 1008.

TS 25.212 describes the characteristics of the Layer 1 multiplexing and channel coding in the FDD mode of UTRA. *Id.* at 7. This include describing data stream from/to MAC and higher layers that is encoded/decoded to offer transport

services over the radio transmission link. *Id* at 9. TS 25.212 also discloses a channel coding scheme that is a combination of error detection, error correcting, rate matching, interleaving and transport channels mapping splitting from physical channels. *Id*.

III. CLAIM CONSTRUCTION

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). §42.100(b). Neither party is proposing constructions for the '486 Patent, and none were issued in the related District Court proceeding; therefore, at least for purposes of this Preliminary Response, all claim terms should be construed according to their plain and ordinary meaning.

IV. LEGAL STANDARDS FOR INVALIDITY

Anticipation under 35 U.S.C. § 102 (pre-AIA)¹ requires that a single prior art reference disclose each and every limitation of the claimed invention. *Schering Corp. v. Geneva Pharms.*, 339 F.3d 1373, 1379-80 (Fed. Cir. 2003).

Additionally, a claim is not patentable if the differences between it and the prior art are such that the subject matter as a whole would have been obvious to a

¹ The pre-American Invents Act (“AIA”) statute controls here because the '486 Patent was filed and issued prior to the AIA’s implementation.

person of ordinary skill in the art at the time of the invention. 35 U.S.C. § 103(a) (pre-AIA). Obviousness requires assessing (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) “secondary considerations” of non-obviousness such as “commercial success, long felt but unsolved needs, failure of others, etc.” *KSR Int’l Co. v. Teleflex Inc.*, 550 US 398, 406 (2007) (quoting *Graham v. John Deere Co.*, 383 US 1, 17-18 (1966)).

It is Petitioner’s burden “to demonstrate both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367-68 (Fed. Cir. 2016) (quotations and citations omitted). However, a petitioner must first show that all of the claimed elements are disclosed in the prior art. *See Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1164 (Fed. Cir. 2006) (considering motivation to combine and reasonable expectation of success only “if all the elements of an invention are found in a combination of prior art references”).

Obviousness of a patent cannot properly be established by mere conclusory statements. Instead, there must be some articulated reasoning with some rational

underpinning to support the legal conclusion of obviousness. A reason for combining disparate prior art references is a critical component of an obviousness analysis. The obviousness analysis should be made explicit and needs to provide an articulated reasoning with some rational underpinning to identify the reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. *See InTouch Techs., Inc. v. VGo Commc'ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014).

V. DISCRETIONARY FACTORS FAVOR DENIAL OF INSTITUTION

The Petition should be denied pursuant to the Director's discretion to deny institution of petitions pursuant to 35 U.S.C. § 314(a) according to the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020). The PTAB has the authority, where warranted, to exercise discretion to deny institution in view of the *Fintiv* factors particularly where, as here, the merits of the challenge are not compelling (*see infra*, Section VI). *See* "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation," issued June 21, 2022 ("Director's Guidance").

Thus, the Petition would be neither an "effective [nor] efficient alternative" to the ongoing litigation, would not be an efficient use of Board resources, and on these

bases should be discretionarily denied. *See Gen. Plastic Indus.*, IPR2016-01357, Paper 19 at 16-17.

A. Application of *Fintiv* Factors Weighs in Favor of Denying Institution

There is no requirement to institute an IPR. *See, e.g., Harmonic Inc. v. Avid Tech.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016); *see also Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016); 37 C.F.R. § 42.108(a). The latest applicable guidance from the Director states that the purpose of discretionary denial is to “limit unnecessary and counterproductive litigation costs” and avoid gamesmanship. *See Memorandum on Interim Procedure for Discretionary Denial* from Katherine K. Vidal, Director of the USPTO, at 1 (June 21, 2022). This guidance has also clarified the application of the so-called *Fintiv* factors to circumstances such as these, where there is a co-pending District Court Action.² *Id.*

For the Grounds presented in this Petition, instituting an IPR would not be an effective or efficient alternative to litigation because, most notably, the co-pending District Court Action (1) involves the substantially the same prior art that LGE relies on here, and (2) will be complete well before a final written decision in this

² Here, the co-pending District Court Action is *Pantech Corp. v. LG Electronics Inc.*, No. 5:22-cv-00113-RWS (E.D. Tex.).

proceeding. When considered within a thorough analysis of the *Fintiv* factors, any slim (if any) merits of this Petition fail to weigh in favor of institution. Rather, the merits of LGE’s invalidity challenge are best addressed in the District Court Action, and therefore, the Board should exercise its discretion to deny institution.

1. *The Court Has Not Stayed The Underlying Litigation Nor Has a Motion to Stay Been Filed*

Regarding the first *Fintiv* factor (“whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted”), a stay has not been granted in the District Court Action, and Petitioner has not filed a motion to stay in view of this Petition. And while Petitioner has made the bare statement that it “intends to seek a stay” if this IPR is granted (*see* Petition at 18), there is no evidence that Petitioner’s not-yet-made request would be granted even if made—and Petitioner has offered absolutely none.

While the Board “will not attempt to predict” how the district court will proceed in the absence of specific evidence (*Sand Revolution II, LLC v. Continental Intermodal Group-Trucking LLC*, IPR 2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative)), it bears mentioning that the evidence indicates that a stay will not be granted. First, even if this IPR is instituted, the projected final written decision will not occur until April, 2025—approximately seven months after the scheduled

trial date in the District Court Action.³ In similar circumstances, this district court routinely denies motions to stay. The District Court’s decision in *Maxell Ltd. v. Apple Inc.*, No. 5:19-CV-00036-RWS, 2020 U.S. Dist. LEXIS 257531, at *7-9 (E.D. Tex. April 27, 2020), explained that a stay should not be granted because the case was filed “more than a year ago” (as would be true with this litigation) and because trial is scheduled for six months after the order (the September trial date would be even closer to any decision on institution). *See also Kirsch Research and Development LLC v. DuPont de Nemours, Inc.*, Dkt. 269, No. 5-20-cv-00057-RWS (E.D. Tex. July 7, 2021) (similar analysis following *Maxell* and noting the advanced stage of litigation). Second, the District Court has already denied a different request by Petitioner to stay the litigation (for reasons unrelated to any *inter partes* review), stating that a stay “would unjustly delay the progress of the case and harm Pantech’s interests in timely resolution.” *See Pantech Corp. v. LG Electronics Inc.*, No. 5:22-cv-00113-RWS, Dkt. 131 at 1 (E.D. Tex., July 19, 2023). The Court has thus demonstrated its intent to proceed to trial in a timely manner. As such, there has been

³ Jury trial is scheduled for September 23, 2024. *See Pantech Corp. v. LG Electronics Inc.*, No. 5:22-cv-00113-RWS, Dkt. 240 at 2 (E.D. Tex., Jan. 22, 2024) (attached as Ex. 2017).

no suggestion that the trial would not occur as currently scheduled in September 2024.

As such, the evidence indicates that a stay will not be granted in the future even if Petitioner requests one, and this *Fintiv* factor weighs in favor of denial.

2. *The Trial Date in the District Court Action Precedes the Projected Final Written Decision Date*

Regarding the second *Fintiv* factor (“the proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision”), the projected final written decision date is in late April, 2025, well after the scheduled September 23, 2024 trial date in the District Court Action. In fact, the trial date is even before any reply would be due from Petitioner (late October, 2024) and prior to the final oral hearing, should *inter partes* review be granted.

While Petitioner correctly states that the median time to trial in the Eastern District of Texas “varies between 19 and 24 months” (see Petition at 18, citing Ex. 1028), 24 months after the filing date is September 2, 2024. That is **before** the currently-scheduled trial date (meaning the current schedule is already longer than the average). Petitioner’s alternative citation to privately gathered statistics from *Docket Navigator* indicating a median time to trial of 26 both exceeds the guidance from the USPTO Director of what statistics will be considered (see Memo from Katherine K. Vidal at 9 n. 12 (June 21, 2022)) and also does not meaningfully change

the analysis—November 11, 2024 (the date using these statistics) would still be many months before the projected statutory deadline for a final written decision. Regardless, the statistics about averages are irrelevant here because a trial date has been set and there has been no indication that it would move in any significant way beyond the currently scheduled date.

Accordingly, this *Fintiv* factor also weighs in favor of denial.

3. *The Parties Have Invested Substantial Efforts in Litigating the Grounds Presented in this Petition in the District Court Action*

Regarding the third *Fintiv* factor (“investment in the parallel proceeding by the court and the parties”), the parties have significantly invested in the District Court Action. For example, the parties have served and responded to discovery including making large document productions, engaged in early motion briefing, a hearing on a motion to dismiss (with related briefing and a denied motion for reconsideration), engaged in full claim construction briefing and depositions of experts relating to claim construction, and received a claim construction order. Fact discovery has concluded.

Most notably, expert reports on invalidity are due to be served on February 21, 2024, with expert discovery on validity concluding by April 10, 2024—expert discovery will therefore be complete by the time of any institution decision. As

addressed below in the context of the fourth *Fintiv* factor, the grounds of invalidity disputed by the parties in the District Court Action are substantially the same as Petitioner presents here. Thus, the parties have already (or shortly will have) invested many of the same resources into the District Court Action that Petitioner seeks to bring into this dispute. Institution would be a waste of party and judicial resources, precisely what discretionary denial seeks to avoid. See Memo from Katherine K. Vidal at 1 (June 21, 2022).

This *Fintiv* factor also weighs in favor of denial.

4. *Petitioner Fails To Offer A Sotera Stipulation And There Is Significant Overlap Between Issues Raised In The Petition And In The District Court Litigation*

Regarding the fourth *Fintiv* factor (“overlap between issues raised in the petition and in the parallel proceeding”), each of the six grounds of alleged invalidity asserted in this Petition are already being litigated in the District Court Action.

Specifically, each of Stewart, TS 25.212, 3GPP-Summary, and Motorola (*i.e.*, every reference relied upon in this Petition) is being asserted as a basis of invalidity in the District Court Action. Ex. 2018 (LGE’s Invalidity Contentions) at 86-97. The same combinations of references are also being litigated. *Id.*

Moreover, Petitioner has not offered any *Sotera*-type stipulation or made any effort to avoid duplicative proceedings.

Given that the Petition is directed toward the same claims, same references, substantially similar arguments, and significantly overlapping evidence at issue in the parallel District Court Action, and since Petitioner has not sought to mitigate any of these concerns through a *Sotera* stipulation, this *Fintiv* factor favors denial of institution.

5. *LGE is Both Petitioner and Defendant*

Regarding the fifth *Fintiv* factor (“whether the petitioner and the defendant in the parallel proceeding are the same party”), LG Electronics Inc. is both Petitioner here and a defendant in the District Court Action. The Petition acknowledges this. *See* Petition at 3. This *Fintiv* factor thus also weighs in favor of denial.

6. *Other Circumstances Also Weigh in Favor of Discretionary Denial*

Regarding the sixth *Fintiv* factor (“other circumstances that impact the Board’s exercise of discretion, including the merits”), while petitioner avers that “[t]he merits of this Petition are compelling as shown herein” (*see* Petition at 19), as set forth below in Section VI, the weakness of the proposed grounds weighs strongly in favor of denial of institution.

But even if there are some merits to Petitioner’s shotgun, six-ground challenge (and there are not), “[w]here the information presented at the institution stage is merely sufficient to meet the statutory institution threshold [a reasonable likelihood

of success], the PTAB has the authority, where warranted, to exercise discretion to deny institution in view of the other *Fintiv* factors.” Memo from Katherine K. Vidal at 4 (June 21, 2022). Petitioner has certainly failed to meet the higher threshold of a “compelling” unpatentability challenge.

Furthermore, the sheer number of grounds asserted, six, increases substantially the duplicative litigation sought by Petitioner. Asking both the USPTO and the district court to independently consider at least six asserted grounds of invalidity, without any *Sotera* stipulation, surpasses any reasonable threshold of “counterproductive litigation costs” limited by the Director’s guidance on discretionary denial (not to mention gamesmanship).

Accordingly, the sixth *Fintiv* factor also weighs against institution.

* * *

As described above, every single one of the six *Fintiv* factors weighs against institution of this Petition. The USPTO should exercise its discretion not to institute an *inter partes* review in view of the advanced stage of the District Court Action on the same grounds, as well as the other considerations described herein.

**VI. THE PETITION DOES NOT SHOW A REASONABLE
LIKELIHOOD OF PREVAILING WITH RESPECT TO ANY
CHALLENGED CLAIM**

The Petition should be denied because it does not establish a reasonable likelihood of prevailing on any of the asserted grounds against any of the challenged claims.

**A. Ground 1: Petitioner Fails To Establish That Claims 1-6 are
Anticipated AND/OR Rendered Obvious By Stewart**

Petitioner has not shown a likelihood of prevailing with respect to Ground 1 because Stewart does not teach each and every element of Claims 1-6. Specifically, Stewart does not teach elements [3.d] and [3.e] (or substantially similar elements [1.d]-[1.e], and [5.d]-[5.e]), as required for each of these claims.

1. Stewart fails to disclose claim element [3.d] “buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream”

Petitioner fails to show that Stewart discloses UE **buffering** the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream, as required by claim element [3.d].

In particular, claim element [3.d] requires a buffer into which the interleaved systematic and the parity bits are collected. *See* '486 patent at cl. 3 (“buffering...”); *see also id.* at 6:45-47 (“The systematic bits, Parity 1 (P1) and Parity 2 (P2) bits are combined at the bit collection circuit 625 to provide a single data output Ndata”). In

contrast, Stewart does not disclose buffering the systematic bits and the parity bits, and no secondary reference cures this deficiency.

Even in the context of alleged anticipation, Petitioner appears to acknowledge that Stewart does not disclose a UE buffering the interleaved systematic and parity bits, because it only argues, in a cursory fashion, that “a POSITA would have found it obvious to use the block matrices of Stewart’s interleavers to buffer bits.” Petition at 35. However, Stewart discloses buffering tail bits for subsequent transmission and not the interleaved systematic and parity bits. See Stewart at 4:31-34. For example, Stewart only discloses that the “tail bits from the coder are buffered.” *Id.* And, that “the buffered tail bits are then appended completing the desired instantaneous codeword.” Stewart at 5:38-40.

Petitioner argues, without evidence, that the interleavers (systematic bit interleaver and parity bit interleavers) include buffering. See Petition at 48-49. But this is not the case. As shown below in Fig. 11 of Stewart, step 1202 of Stewart does not disclose buffering any of the interleaved systematic bits, the interleaved first parity bit stream, and the interleaved second parity bit stream. *Id.*

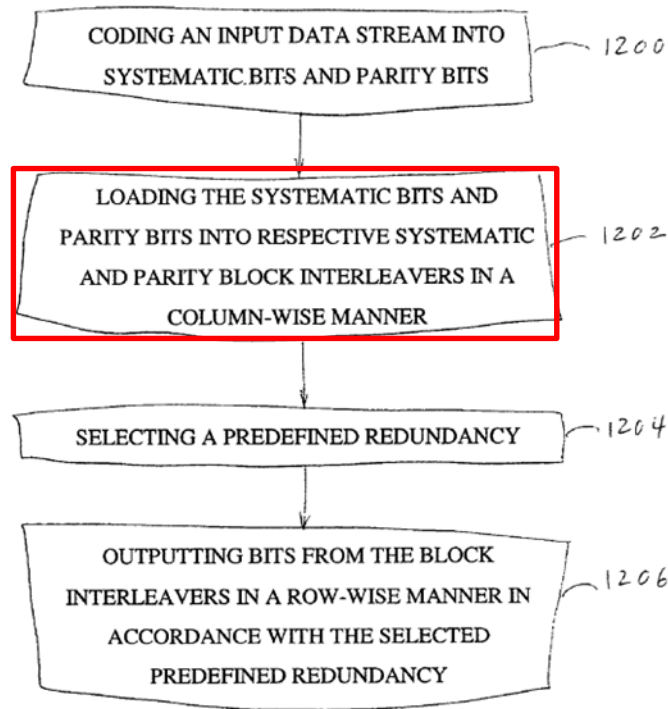


FIG. 11

Stewart at Figure 11 (annotated).

At best, step 1202 of Figure 11 shown above, suggests that Stewart loads systematic bits and/or parity bits in the interleavers. *See id.* at Fig. 11 (“loading the systematic bits and the parity bits into respective systematic and parity block interleavers”). But “loading the systematic bits and the parity bits into respective systematic and parity block interleavers” is different from buffering already-interleaved bits because a standalone buffer provides a single data output for

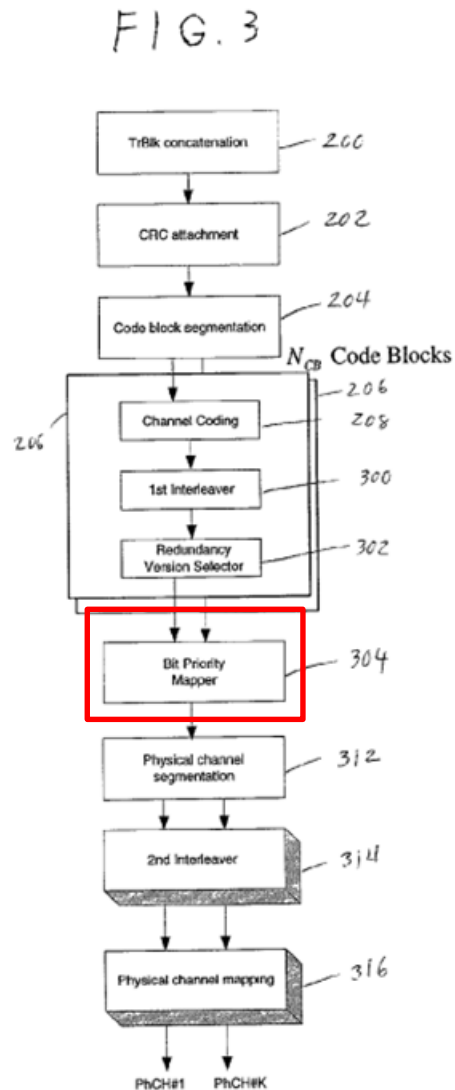
transmission. *See* '486 Patent at 6:45-47. Even if Figure 11 of Stewart teaches a buffer component that is part of the interleaver (and it does not), this would still not provide a separate buffer for “the interleaved systematic bits” as required by the method claimed in the '486 Patent. *See* '486 Patent at claim element [3.d]. Hence, loading the systematic and parity bits in the interleaver is not the same as loading interleaved systematic bits in a buffer that collects interleaved bits, as required by the claim element [3.d].

Further, for the same reasons as stated above, Petitioner has failed to disclose that Stewart teaches each and every element of Claims 1-2 and 5-6, because comparable elements [1.d] and [5.d] also require a buffer into which the interleaved systematic and the parity bits are collected.

Therefore, Petitioner has failed to establish a reasonable likelihood of success of any claim challenged in Ground 1.

2. Stewart fails to disclose claim element [3.e] “selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions...”

Petitioner also fails to show that Stewart discloses UE selecting bits for **transmission based on a plurality of redundancy versions**, as required by claim element [3.e]. At most, Stewart appears to disclose collecting the interleaved bits for transmission in the Bit Priority Mapper (BMP) 304 of Fig. 3, as shown below:



Stewart at Figure 3 (annotated). In particular, Stewart discloses that prior to transmission, the systematic and parity bits are read into a BPM (bit priority mapper) array. *See* Stewart at 8:10-18.

However, the BPM gives priority to bits in a manner unrelated to the redundancy version. As taught by Stewart, the BPM priority is based on “placing systematic bits in positions of high reliability,” not based on plurality of redundancy

version as required by claim element [3.e]. *See* Stewart at 7:55-62. This is a separate and distinguishable teaching from the system claimed by the '486 Patent.

Additionally, for these same reasons, Petitioner has failed to disclose that Stewart teaches each and every element of Claims 1-2 and 5-6, elements [1.e] and [5.e] are substantially similar to element [3.e] and also require selecting bits for transmission based on a plurality of redundancy versions.

Therefore, for this reason too, Petitioner has failed to establish a reasonable likelihood of success of any claim in Ground 1.

B. Grounds 2: Petitioner Failed To Establish That Claims 1-6 are Rendered Obvious By Stewart in View of 3GPP-Summary

For Ground 2, Petitioner attempts to use the 3GPP-Summary reference to fill in the various gaps of the teachings of Stewart with regard to the claims of the '486 Patent, as shown above with regard to Ground 1. *See generally* Petition at 64-71. However, the 3GPP-Summary also does not overcome the deficiencies of Stewart. Specifically, the combination of Stewart and the 3GPP-Summary does not render obvious the claimed “buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream” as required by claim element [3.d], nor does it render obvious “selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions...” as

required by claim element [3.e]. Therefore, the 3GPP-Summary does not cure the deficiencies of Stewart. *Id.*

Regarding claim element [3.d], while the 3GPP-Summary discloses the existence of a certain transmitter buffer in which the interleaved bits are stored (*see* 3GPP-Summary at 2), this teaching does not meet the requirements of the claim language. Namely, the 3GPP Summary does not explain what specific structure constitutes the buffer or how it could be used in accordance with the disclosures of Stewart. This matters, because as disclosed above, the only location disclosed in Stewart for collecting bits from the interleavers is the BPM, which would not lead to the use of any buffers from the 3GPP-Summary reference.

And regarding claim element [3.e], as stated in the 3GPP-Summary, “[a]t transmission, bits are sequentially transmitted from the buffer, **starting at the selected initial position** (wrap around is used at the end of the buffer).” *Id.* (emphasis added). Accordingly, even if a hypothetical combination of Stewart with the 3GPP-Summary would teach that bits are selected from a buffer for purpose of transmission, the selection of bits for transmission from such a combination would not be based on redundancy versions as required by claim element [3.e] (and comparable claim elements [1.e] and [5.e]), but rather based on a selected initial position. *See* ’486 Patent at cl. 3.

Therefore, because the 3GPP-Summary cannot overcome the deficiencies of Stewart with respect to the challenged independent claims of the '486 Patent, Petitioner failed to establish a reasonable likelihood of success of any claim in Ground 2.

C. Grounds 3: Petitioner Failed To Establish That Claims 1-6 are Rendered Obvious Over Stewart in view of TS 25.212

For Ground 3, Petitioner attempts to use TS25.212 to fill in the various gaps of the teachings of Stewart with regard to the claims of the '486 Patent, as shown above with regard to Ground 1. *See generally* Petition at 72-79. However, Petitioner's proposed combination of Stewart and TS 25.212 would be contradictory and simply would not work.

Specifically, TS 25.212 uses the same transport channel multiplexing structure of an earlier version of TS 25.212 (v3.5.0) that was expressly rejected by Stewart. Figure 2 of Stewart discloses the transport channel multiplexing structure of an earlier version of TS 25.212 (v3.5.0). *See* Stewart at 3:47-51 ("FIG. 2 shows the existing reference channel coding model for High Speed Downlink Packet Access (HSDPA) in accordance with... TS 25.212 v3.5.0"). Critically, both the earlier version of TS 25.212 (v3.5.0) shown in Stewart and Petitioner's TS 25.212 reference lack the generalized rate matching function in the first interleaver critical to Stewart's teaching. *See* Ex. 1008 at 3:64-4:13 ("FIG. 3 shows... [that] [t]he first

interleaver includes the generalized rate matching function of the present invention based on a block interleaver that is easily implementable and offers good performance for all HARQ scenarios”).

FIG. 2 — PRIOR ART — Stewart at Figure 2 (lacking generalized rate matching function in the first interleaver).	Figure 2: Transport channel multiplexing structure for downlink TS 25.212 (Ex. 1008) at Figure 2 (lacking generalized rate matching function in the first interleaver).	FIG. 3 Stewart at Figure 3 (providing a generalized rate matching function in the first interleaver)
---	---	--

By proposing an alleged improvement to this prior system now advanced by Petitioner, Stewart has proposed a system incompatible with the transport channel multiplexing structure of TS 25.212. See Stewart at 3:57-63 (“At this point, each of

the code blocks are individually subjected to channel coding 208 and rate matching 210 according to the puncturing and incremental redundancy used. The blocks are then subject to physical channel segmentation 212, interleaving 214, and physical channel mapping 216, where physical channels 1 through K are output.”). Thus, Stewart uses a different structure in which the first interleaver includes a generalized matching function, as shown above in Figure 3 of Stewart. See Stewart at 4:10-13, Fig. 3.

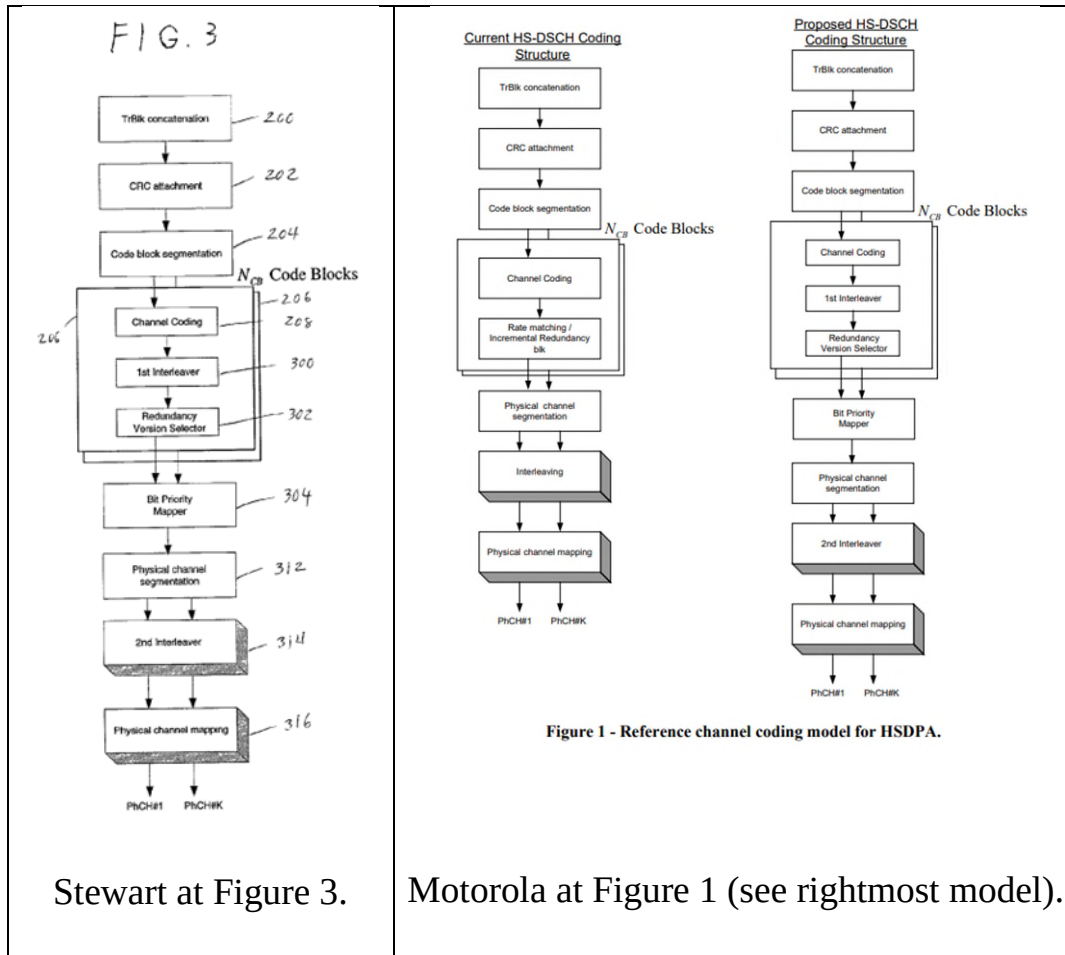
Petitioner has not shown any reason why a POSITA would look to Stewart but then reject its teachings in order to adopt the transport channel multiplexing structure of TS 25.212. Therefore, Petitioner failed to establish that its proposed combination of Stewart and TS 25.212 would have been obvious, and thus failed to establish a reasonable likelihood of success on any claim in Grounds 3.

D. Ground 4-6: Petitioner Failed To Establish That Claims 1-6 are Rendered Obvious Over Stewart in view of Motorola

For Grounds 4-6, Petitioner attempts to address the various deficiencies with Grounds 1-3 with the addition of Motorola. See *generally* Petition at 79-87. Specifically, Petitioner alleges that Motorola may be used to address the failures of Stewart, alone or in combination with 3GPP-Summary or TS 25.212, to teach claim elements [1.e], [3.e], and [5.e]. But this does not address each of the issues with Grounds 1-3.

First, regarding Grounds 4 and 5, Petitioner does not even allege that Motorola addresses the deficiencies of Stewart either alone (*i.e.*, Ground 1) or in combination with 3GPP Summary (*i.e.*, Ground 2) with respect to claim element [3.d] and analogous limitations [1.d] and [5.d]. *Id.* Moreover, regarding claim element [3.e] and analogous limitations [1.e] and [5.e], Motorola suffers a similar deficiency as Stewart and teaches that, prior to any transmission, the systematic and parity bits are read into a BPM (bit priority mapper) array. *See* Motorola at 8. Indeed, as taught by Motorola, the BPM priority is based on “placing systematic bits in positions of high reliability,” not “based on a plurality of redundancy versions” as required by claim element [3.e]. *See id.* Grounds 4-5 thus fail for the same reasons with respect to claim elements [3.d] and [3.e] (and analogous elements in the other independent claims) as described above for Grounds 1-2, as Motorola does not and cannot cure the deficiencies of the other references relied upon.

Second, regarding Ground 6, the addition of Motorola in no way remedies the incongruous combination of Stewart and TS 25.212 as explained with regard to Ground 3, nor does Petitioner even allege that it could. *Id.* Indeed, the “Proposed “HS-DSCH Coding Structure” of Figure 1 of Motorola is substantially the same as Figure 3 of Stewart:



Hence, Motorola suffers the same inability to be combined with TS 25.212 as Stewart itself does. Thus, Ground 6 fails as a result of the same failings with respect to the combination of Stewart and TS 25.212, as explained above with regard to Ground 3.

Therefore, for the same reasons as discussed above for Grounds 1-3, Petitioner's Grounds 4-6 obviousness combinations also fail. Petitioner has not shown a likelihood of success with respect to any Ground or any challenged claim.

VII. CONCLUSION

For the reasons set forth above, the Board should not institute *inter partes* review on any of the Grounds set forth in the Petition. As Patent Owner has shown, Petitioner has not established a reasonable likelihood of success on any of the challenged claims of the '486 Patent.

Dated: January 29, 2024

Respectfully submitted,

/Amanda S Bonner Reg No 65224 /

Amanda S. Bonner
Registration No. 65,224
Mayer Brown LLP
71 S. Wacker Drive
Chicago, IL 60606
Telephone: 312-782-0600
Facsimile: 312-706-8157
asbonner@mayerbrown.com

James A. Fussell, III
Registration No. 54,885
Clark S. Bakewell
Registration No. 71,615
Baldine B. Paul
Registration No. 54,369
Tariq Javed
Mayer Brown LLP
1999 K Street NW
Washington, D.C. 20006
Telephone: 202-263-3000
Facsimile: 202-263-3300
jfussell@mayerbrown.com
cbakewell@mayerbrown.com

Case IPR2023-01272
Patent No. 9,065,486
Patent Owner Preliminary Response

bpaul@mayerbrown.com
tjaved@mayerbrown.com

Attorneys for Pantech Wireless LLC

Case IPR2023-01272
Patent No. 9,065,486
Patent Owner Preliminary Response

CERTIFICATE OF SERVICE

I hereby certify that on this 29th day of January, 2024, a copy of the attached **PATENT OWNER PRELIMINARY RESPONSE** was served by electronic mail to the attorneys of record, at the following addresses:

James L. Davis, Jr.
James.l.davis@ropesgray.com
Daniel W. Richards
Daniel.richards@ropesgray.com
Abed R. Balbaky
Abed.balbaky@ropesgray.com
LGE-Pantech-Ropes-IPR-Service@ropesgray.com

Respectfully submitted,

Date: January 29, 2024

By: /Amanda S Bonner Reg No 65224/
Amanda S. Bonner (Reg. No. 65,224)

MAYER BROWN LLP

Case IPR2023-01272
Patent No. 9,065,486
Patent Owner Preliminary Response

CERTIFICATION PURSUANT TO 37 C.F.R. § 42.24(d)

Pursuant 37 CFR 42.24(d), the undersigned certifies that this Preliminary Response complies with the type-volume limitation of 37 CFR §42.24(a). The word count application of the word processing program used to prepare this Preliminary Response indicates that the Preliminary Response contains 6,349 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(a).

Respectfully submitted,

Date: January 29, 2024

By: /Amanda S Bonner Reg No 65224/
Amanda S. Bonner (Reg. No. 65,224)

MAYER BROWN LLP