

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS INC.,
Petitioner,

v.

PANTECH WIRELESS, LLC,
Patent Owner.

IPR2023-01272
Patent 9,065,486 B2

Before DANIEL J. GALLIGAN, CHRISTOPHER L. OGDEN, and
SCOTT B. HOWARD, *Administrative Patent Judges*.

HOWARD, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

LG Electronics Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–6 (“the challenged claims”) of U.S. Patent No. 9,065,486 B2 (Ex. 1001, “the ’486 patent”). Pantech Wireless, LLC (“Patent Owner”) filed a Patent Owner Preliminary Response (Paper 22, “Preliminary Response,” “Prelim. Resp.”). With our authorization, Petitioner filed a Preliminary Reply to Patent Owner’s Preliminary Response. Paper 23.

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). *Inter partes* review may not be instituted unless “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). “When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” 37 C.F.R. § 42.108(a) (2022).

For the reasons set forth below, upon considering the briefing and the evidence of record, we determine that the information presented in the Petition establishes a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims, and we institute *inter partes* review on all of the challenged claims based on all of the grounds identified in the Petition.

B. Real Parties in Interest

Petitioner identifies itself and LG Electronics U.S.A., Inc. as real parties in interest. Pet. 5.

Patent Owner identifies itself and Pantech Corporation as real parties in interest. Paper 3, 1 (Patent Owner’s Mandatory Notices).

C. Related Matters

The parties identify the following district court proceeding in which the ’486 patent is being asserted: *Pantech Corporation v. LG Electronics Inc.*, No. 5:22-cv-00113-RWS (E.D. Tex.). Pet. 5; Paper 3, 1.

D. The ’486 Patent

The ’486 patent is titled “Detection, Avoidance and/or Correction of Problematic Puncturing Patterns in Parity Bit Streams Used When Implementing Turbo Codes.” Ex. 1001, code (54).

The ’486 patent describes wireless communication systems, such as Code Division Multiple Access (CDMA) systems specified by the Third Generation Partnership Project (3GPP), and relates “particularly to a method for detecting and correcting performance degradation in punctured Turbo codes using a Turbo encoder.” Ex. 1001, 1:35–46, 1:29–31. According to the ’486 patent, “the turbo coding of the data being processed for wireless transmission plays a significant role for both [Time Division Duplex (TDD)] and [Frequency Division Duplex (FDD)] communications in a 3GPP system.” *Id.* at 2:55–58; *see also id.* at 1:49–50, 2:51–52. The ’486 patent describes turbo codes as follows:

Turbo codes are a form of parallel, recursive systematic convolution codes, which can be used for channel coding and decoding in order to detect and correct errors that may occur in the transmission of digital data through different channels. Turbo codes are particularly useful for data transfers in which,

under certain conditions, the data transfer rate can approach the theoretical limits of Shannon's Law. These favorable conditions generally include large block size transfers, which are particularly useful in mobile communications.

Id. at 2:64–3:5.

The '486 patent describes that typical Turbo codes created by puncturing parity bits show poor performance:

Typically, high-rate Turbo codes are created by puncturing (i.e., eliminating) parity bits of a lower-rate code until the desired code rate is attained. Particular codes created by puncturing exhibit poorer than expected performance due to certain punctured bit patterns. Because the recursive encoding blocks in a Turbo encoder have an infinite impulse response, information about each systematic bit is distributed across many of the parity bits.

Ex. 1001, 3:10–17. According to the '486 patent, “[i]n order to obtain adequate performance, it is necessary to detect, avoid and/or correct the problematic puncturing patterns in the parity bit streams without having to avoid code rates. Typically, problematic interactions occur between the Turbo coder output and puncturing in the rate matching stages.” *Id.* at 4:41–46. The '486 patent is directed to solving that problem in turbo coding as follows:

According to the present invention, degradations in quality of punctured error correction coded transmissions are identified and the code transmissions are modified accordingly. A puncturing pattern which approximates a particular code rate is identified, and a value for anticipated degradation is adjusted in accordance with a matching of the puncturing pattern and the particular code rate.

Id. at 4:53–59. The '486 patent further explains:

One can achieve the desired overall code rate while avoiding problematic puncturing patterns by adjusting the amount of puncturing performed in each stage. This method,

when placed in the context of the 3GPP [High Speed Downlink Packet Access (HSDPA)] Turbo Code/Rate Matching algorithm leads to artificially reducing the size of the virtual Incremental Redundancy (IR) buffer. In general the approach implies a modification to the individual puncturing rates of each of the stages such that a desirable overall puncturing pattern results.

Id. at 11:51–59; *see also id.* at 5:21–22. The '486 patent also explains that “[t]he effect of the periodicity of the puncturing pattern can also be mitigated by interleaving the parity bits before rate-matching occurs” so that “after de-interleaving, periodic sampling of the parity bits is avoided even when periodic sampling is done in rate-matching.” *Id.* at 11:7–11.

Figure 10 of the '486 patent is reproduced below:

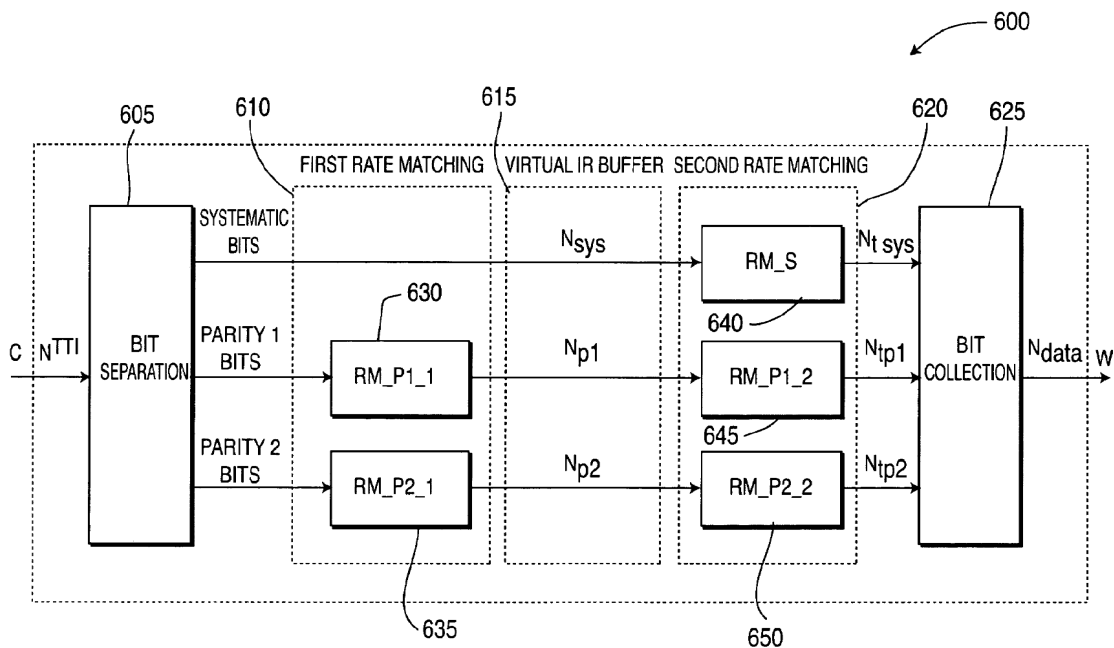


FIG. 10

Figure 10 is “a schematic block diagram showing circuitry 600 for 3GPP rate matching for HSDPA, using a Turbo coded [High Speed Downlink Shared Channel (HS-DSCH)].” *Id.* at 6:27–29; *see also id.* at 5:21–22. The '486 patent describes the circuitry 600 as follows:

The circuitry 600 implements a 3GPP rate-matching scheme for HSDPA. The circuitry 600 includes a bit separation circuit 605, a first rate matching stage 610, a virtual incremental redundancy (IR) buffer 615, a second rate matching stage 620 and a bit collection circuit 625. The first rate matching stage 610 includes a Parity 1 (P1) bit rate matching circuit 630 and Parity 2 (P2) bit rate matching circuit 635. The second rate matching stage 620 includes a systematic bit rate matching circuit 640, a Parity 1 (P1) bit rate matching circuit 645 for the second rate matching and a Parity 2 (P2) bit rate matching circuit 650 for the second rate matching. In operation, the systematic bits, Parity 1 (P1) and Parity 2 (P2) bits are processed through the first rate matching stage 610, virtual [incremental redundancy (IR)] buffer 615, second rate matching stage 620 and bit collection circuit 625.

Id. at 6:29–44. According to the '486 patent, the two stages of rate matching and puncturing operations provide substantial benefits:

For both FDD and TDD, two stages of rate matching and two puncturing operations are included, and this is done because of a certain technique called, incremental redundancy, which allows for a wireless transmit/receive unit (WTRU) to receive and soft combine multiple transmissions of the same [Transport Blocks (TB)] from the base station [(BS)]. If the transmission fails the first time, the signal is retransmitted with more data in an attempt to obtain a successful communication the second time. In order to do that, two different stages of puncturing are used because the WTRU has certain capabilities, certain buffer sizes that it can support, and in order to be able to fit the retransmissions that are combined into the buffer, there are two stages of puncturing. The first stage of rate matching punctures enough bits such that the surviving bits fit into a buffer, and the second stage of puncturing (or repetition) is to achieve the desired overall code rate. When the two stages of rate matching are combined, a plot of problematic regions of coding rate is a multidimensional plot. Thus, there are two rates now involved, which are a rate in a first stage of puncturing and a rate in a second stage of puncturing.

Id. at 4:60–5:12.

E. Illustrative Claim

Claims 1, 3, and 5 are independent. Claim 3, which is illustrative of the claimed invention, is reproduced below with annotations (brackets) inserting Petitioner's identifiers of claim limitations and the disputed claim limitations emphasized.

3. [3.pre] A method for use in an apparatus of a wireless communications comprising:

[3.a] interleaving, by the apparatus, systematic bits;

[3.b] interleaving, by the apparatus, a first parity bit stream;

[3.c] interleaving, by the apparatus, a second parity bit stream;

[3.d] *buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream; and*

[3.e] *selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.*

Ex. 1001, 23:4–17 (emphasis added).

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–6 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
1–6	102(e)	Stewart ²
1–6	103(a) ³	Stewart
1–6	103(a)	Stewart, 3GPP-Summary ⁴
1–6	103(a)	Stewart, TS25.212 ⁵
1–6	103(a)	Stewart, Motorola ⁶
1–6	103(a)	Stewart, 3GPP-Summary, Motorola
1–6	103(a)	Stewart, TS25.212, Motorola

Petitioner also relies on the testimony of Bertrand Hochwald, Ph.D.
(Ex. 1003).

¹ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the ’486 patent claims the benefit of the filing date from an application filed before March 16, 2013 and neither party argues that the claims are not entitled to claim the benefit of the earlier filing date, we apply the pre-AIA version of the statutory basis for unpatentability. *See* Ex. 1001, codes (60), (63).

² US 7,260,770 B2, filed Oct. 22, 2001, and issued Aug. 21, 2007 (Ex. 1005).

³ Petitioner treats anticipation and obviousness based on Stewart as a single ground. *See* Pet. 11. Because anticipation and obviousness involve a different analysis, we identify them separately.

⁴ Ericsson, “Overview of Proposed Schemes for Incremental Redundancy,” submission to TSG-RAN Working Group 1 Ad Hoc on HSDPA (Tdoc R1-01-1047) (Sophia Antipolis, France Nov. 5–7, 2001) (Ex. 1007).

⁵ 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD) (Release 5) (Technical Specification: 3GPP TS 25.212 version 5.1.0) (Ex. 1008).

⁶ Motorola, “A New Hybrid-ARQ Scheme Using Incremental Redundancy,” submission to TSG-RAN HSDPA Ad-Hoc (TSGR1-01-1014) (Sophia Antipolis, France Nov. 5–7, 2001) (Ex. 1006).

II. ANALYSIS

A. *Legal Standards*

1. *Anticipation*

A patent claim is unpatentable under 35 U.S.C. § 102 if “the four corners of a single, prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation.”

Advanced Display Sys., Inc. v. Kent State Univ., 212 F.3d 1272, 1282 (Fed. Cir. 2000). “A single prior art reference may anticipate without disclosing a feature of the claimed invention if such feature is necessarily present, or inherent, in that reference.” *Allergan, Inc. v. Apotex Inc.*, 754 F.3d 952, 958 (Fed. Cir. 2014). Moreover, the reference must also “disclose[] within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim.” *Net MoneyIN, Inc. v. Verisign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). However, “the reference need not satisfy an *ipsissimis verbis* test.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

2. *Obviousness*

In *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness under 35 U.S.C. § 103 that requires consideration of four factors: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) if in evidence, objective evidence of non-obviousness such as “commercial success, long-felt but unsolved needs, failure of others, etc.” *Id.* at 17–18. “While the sequence of these questions might be reordered in any particular case,” “it is error to reach a conclusion of obviousness until all

those factors are considered.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 407 (2007) (first quote); *WBIP, LLC v. Kohler*, 829 F.3d 1317, 1328 (Fed. Cir. 2016) (second quote). Because Patent Owner does not address objective evidence of non-obviousness, we focus solely on the first three *Graham* factors.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the time of the invention is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham*, 383 U.S. at 17–18.

Factors pertinent to a determination of the level of ordinary skill in the art include “(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). “Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case.” *Id.*

Petitioner argues that a person having ordinary skill in the art would have had “a bachelor’s degree in electrical and computer engineering, computer science, or the equivalent thereof, and at least two years of experience with networking and wireless communication systems.” Pet. 19 (citing Ex. 1003 ¶¶ 66–68).

Petitioner’s recitation of the level of skill is consistent with the invention disclosed in the ’486 patent, which claims an apparatus and method for use in wireless communications and a wireless transmit/receive unit. It is also not disputed by Patent Owner at this time. *See* Prelim. Resp. Accordingly, for purposes of this Decision, we adopt Petitioner’s formulation of the person having ordinary skill in the art, with the exception of the open-ended phrase “at least.”⁷

C. Claim Construction

We apply the same claim construction standard used in the federal courts, in other words, the claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips*, 415 F.3d 1303. *See* 37 C.F.R. § 42.100(b). Under the *Phillips* standard, the “words of a claim ‘are generally given their ordinary and customary meaning,’” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1312–13.

Petitioner argues that “[a]ll claim terms should be construed according to their plain and ordinary meaning.” Pet. 20.

⁷ If Patent Owner disagrees with Petitioner’s formulation of the level of skill in the art, it must raise that disagreement in its Response. If a different level of skill would affect the outcome in this case, the parties must brief that issue as well. The failure of Patent Owner to describe how the different level of skill in the art is determinative will be a forfeiture of that argument. The parties are also encouraged to submit evidence, other than conclusory expert testimony, that supports their position.

Patent Owner argues that “at least for purposes of this Preliminary Response, all claim terms should be construed according to their plain and ordinary meaning.” Prelim. Resp. 12.

For the purposes of this Decision, we need not expressly construe any claim terms. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Discretionary Denial – Parallel Proceedings

Patent Owner argues that we should exercise our discretion and deny institution based on the district court proceeding. *See* Prelim. Resp. 14–22. Petitioner disagrees. *See* Pet. 18–19; Pet. Prelim. Reply 1.

Under § 314(a), the Director has discretion to deny institution of an *inter partes* review. *See Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an [*inter partes* review] proceeding.”).

In *NHK*, the Board denied institution relying, in part, on § 314(a) because the parallel district court proceeding was scheduled to finish before the Board reached a final decision. *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential) (Decision on Institution). “*NHK* applies to the situation where the district court has set a trial date to occur earlier than the Board’s deadline to issue a final written decision in an instituted proceeding.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 3 (PTAB Mar. 20, 2020) (precedential) (Order).

When determining whether to exercise discretion to deny institution under *NHK* due to an earlier trial date, we consider the following factors (“*Fintiv* factors”):

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board’s exercise of discretion, including the merits.

Id. at 6. “These factors relate to whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding.” *Id.* In evaluating these factors, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* (citing CTPG 58 (November 2019)).

The Director issued an Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation (“Interim *Fintiv* Guidance”).⁸ The Interim *Fintiv* Guidance provides “several clarifications” to “the PTAB’s current application of *Fintiv* to

⁸ Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

discretionary denial where there is parallel litigation” in response to comments received from stakeholders in response to a Request for Comments. Interim *Fintiv* Guidance 2. For example, “the PTAB will not discretionarily deny institution of an IPR or PGR in view of parallel district court litigation where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” Interim *Fintiv* Guidance 7.

Petitioner filed a *Sotera*-type stipulation. Ex. 1300. Specifically, Petitioner stipulates that if we institute this proceeding, “Petitioner will not pursue in *Pantech Corp. v. LG Elecs. Inc.*, No. 5:22-cv-00113 (E.D. Tex.), the grounds of invalidity asserted in the IPR, or any other ground that was raised or could have reasonably been raised in the IPR.” *Id.*

In view of the *Sotera*-type stipulation, we decline to exercise our discretion to deny institution. Interim *Fintiv* Guidance 7–8.

*E. Obviousness over Stewart and 3GPP-Summary*⁹

Petitioner argues that claims 1–6 would have been obvious in light of Stewart and 3GPP-Summary. Pet. 36–47, 64–71. Based on the current record we are sufficiently persuaded that the Petitioner has shown a reasonable likelihood that at least one of the challenged claims is unpatentable on this ground.

1. Overview of Stewart

Stewart is titled “Block Puncturing for Turbo Code Based Incremental Redundancy” and is directed “generally to communication systems, and more particularly to coding in a turbo coded communication system.”

⁹ We exercise our discretion to consider Petitioner’s grounds out of order.

Ex. 1005, code (54) (first quote), 1:6–8 (second quote). Stewart “defines the High Speed Downlink Shared Channel (HS-DSCH) coding and modulation scheme to permit the use of incremental redundancy block interleaving in user equipment (UE), such as a cellular radio communication device.” *Id.* at 3:7–11. More specifically, as shown in the flowchart of Stewart Figure 11 (not reproduced), Stewart describes “a method of block puncturing for turbo code based incremental redundancy.” *Id.* at 9:39–41. The method includes

a first step (1200) of coding an input data stream into systematic bits and parity bits. A next step (1202) includes loading the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner. A next step (1204) includes selecting a predefined redundancy. A next step (1206) includes outputting bits from the block interleavers in a row-wise manner in accordance with the selected predefined redundancy.

Id. at code (57); *see also id.* at 9:41–59.

2. Overview of 3GPP-Summary

3GPP-Summary is a submission for discussion and decision to the “TSG-RAN Working Group 1 Ad Hoc on HSDPA” at a meeting in Sophia Antipolis, France on November 5–7, 2001. Ex. 1007, 1. 3GPP-Summary is titled “Overview of Proposed Schemes for Incremental Redundancy” and “attempt[s] to summarize the different proposals and to propose a way forward for a decision on the IR scheme to be used for HSDPA.” *Id.* 3GPP-Summary compares the IR schemes, focusing on the following aspects:

- Generation, properties and the number of different redundancy versions.
- Signaling of puncturing scheme used, i.e., whether the parameters necessary for a decoding attempt depends on previous transmission attempts or not.

- UE buffering requirements, i.e., if and how the schemes adjust to the buffering memory available.
- Support for a variable number of channel bits (N_{chan}). According to the current working assumptions, the modulation scheme and the number of spreading codes can change between retransmissions.

Id.; see also *id.* at 4 (Table 1 providing a brief summary of the different proposals).

3. *Analysis of Claim 3*

a) *Limitation 3.d*

Limitation 3.d recites “buffering, by the apparatus, the interleaved systematic bits, the interleaved first parity bit stream and the interleaved second parity bit stream.” Ex. 1001, 23:9–11. Petitioner argues that the combination of Stewart and 3GPP-Summary teaches that limitation.

Pet. 64–67. For the reasons set forth below, we agree.

3GPP-Summary sets forth a proposal by Motorola “on the implementation of incremental redundancy for HSDPA” using a “new ‘ring-buffer’ scheme.” Ex. 1007, §§ 1, 2.4. 3GPP-Summary describes Motorola’s proposed improvement as interleaving separately systematic bits and parity bits and that the separately interleaved bits (systematic bits followed by parity bits) are then stored in a buffer. *Id.* § 2.4 (“The systematic bits and the parity bits from the R=1/3 mother code are interleaved separately. A transmitter buffer is defined, where the interleaved systematic bits are stored, followed by the interleaved parity bits.”). When combined with Stewart, the output of the different interleavers (which in Stewart are for the systematic bits, first parity bit stream, and the second parity bit stream (Ex. 1005, 4:14–19, 4:25–29, Fig. 4)) are buffered in a single buffer prior to transmission. See Ex. 1003 ¶¶ 175–178.

Patent Owner argues “the 3GPP Summary does not explain what specific structure constitutes the buffer or how it could be used in accordance with the disclosures of Stewart.” Prelim. Resp. 29. According to Patent Owner, “[t]his matters, because as disclosed above, the only location disclosed in Stewart for collecting bits from the interleavers is the [bit priority mapper (BMP)], which would not lead to the use of any buffers from the 3GPP-Summary reference.” *Id.*

We do not agree. Petitioner, citing the testimony of Dr. Hochwald, argues that a person having ordinary skill in the art would have “modif[ied] Stewart by 3GPP-Summary’s teachings of a ‘transmitter buffer’ to buffer Stewart’s interleaved systematic bits and interleaved parity bits prior to selection for transmission as taught in 3GPP-Summary.” Pet. 65¹⁰ (citing Ex. 1007 § 2.4; Ex. 1005, 5:29–8:30, Figs. 6, 7; Ex. 1003 ¶ 179). Petitioner further argues that the buffer would have been placed between the output of the interleavers and the redundancy version selector:

Based on 3GPP-Summary’s teachings that the “transmitter buffer” is placed after the interleavers, and that bits are selected from the transmitter buffer based on the redundancy versions, a [person having ordinary skill in the art] would have modified Stewart *to include a “transmitter buffer” at the output of Stewart’s interleavers, and before Stewart’s redundancy version selector.*

Id. at 66 (emphasis added) (citing Ex. 1007 § 2.4; Ex. 1003 ¶ 179). That is, Petitioner persuasively argues, with supporting evidence, that it would have been obvious to place the buffer between 1st interleaver 300 and redundancy

¹⁰ Petitioner color codes various limitations in the Petition. Petitioner also bolds the name of prior art references. Here and elsewhere, we omit the colors and bold characters.

version selector 302, which is before the bit priority mapper Patent Owner focuses on.

As for the structure of the buffer, buffers are well known in the art. *See* Ex. 1040 ¶¶ 34–37, 45; Ex. 1041, 4:1–7, 4:32–58, 11:48–57, 15:30–34; Ex. 1027, ¶ 34; Ex. 1003 ¶ 180. Given this evidence and the ubiquity of buffers, choosing the correct structure of a buffer would not be “uniquely challenging or difficult for one of ordinary skill in the art.” *See Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. at 418).

b) Limitation 3.e

Limitation 3.e recites “selecting, by the apparatus, bits for transmission based on a plurality of redundancy versions; wherein at least one redundancy version of the set selects systematic bits over first and second parity bits and at least one redundancy version of the set selects first and second parity bits over systematic bits.” Ex. 1001, 23:12–17. Petitioner argues that the combination of Stewart and 3GPP-Summary teaches that limitation. *See* Pet. 68–71. For the reasons set forth below, we are sufficiently persuaded by Petitioner’s argument.

3GPP-Summary teaches eight different redundancy versions: “Eight different initial positions are defined in the buffer, giving at maximum eight (non-self-decodable) redundancy versions.” Ex. 1007 § 2.4. The eight different redundancy versions are defined by their different initial positions. *Id.* 3GPP-Summary further teaches that “at transmission, bits are sequentially transmitted from the buffer, starting at the selected initial position” and that “(wrap around is used at the end of the buffer).” *Id.* A person having ordinary skill in the art would have understood, based on specific initial positions, that either systematic bits would have been selected

over parity bits or parity bits selected over the systematic bits depending on the initial starting point (or redundancy version):

So, a person of ordinary skill in the art would have understood that if the “starting point” is located in the area of the “transmitter buffer” that stores the “interleaved systematic bits,” systematic bits are read out from the “transmitter buffer” for transmission before the parity bits are read out. If the “starting point,” on the other hand, is located in the area of the “transmitter buffer” that stores the “interleaved parity bits,” the parity bits are read out from the “transmitter buffer,” and then reading wraps around to the systematic bits. Accordingly, 3GPP-Summary teaches reading out for transmission systematic bits followed by interleaved parity bits (*i.e.*, selecting parity bits over systematic bits) and vice versa (reading out for transmission interleaved parity bits and wrapping out to read out interleaved systematic bits, *i.e.*, selecting systematic bits over parity bits).

Ex. 1003 ¶ 182 (citing Ex. 1007 § 2.4).

Patent Owner argues that “the selection of bits from such a combination would not be based on redundancy versions as required by claim element [3.e] (and comparable claim elements [1.e] and [5.e]), but rather based on a selected initial position.” Prelim. Resp. 29.

Based on the current record, we disagree. As discussed above, 3GPP-Summary links the initial position to the redundancy version: “Eight different initial positions are defined in the buffer, giving at maximum eight (non-self-decodable) redundancy versions.” Ex. 1007, § 2.4. Therefore, selecting an initial position is the same as selecting based on a redundancy version. *See* Ex. 1003 ¶ 182.

c) Undisputed Limitations of Claim 3

Petitioner argues that Stewart discloses the undisputed limitations of claim 3¹¹ and that a person having ordinary skill in the art would have combined the features of Stewart and 3GPP-Summary. Pet. 36–47; Ex. 1003 ¶ 174. After reviewing Petitioner’s arguments and information regarding the limitations identified above, including the Hochwald Declaration, which are not addressed by Patent Owner at this stage (*see* Prelim. Resp.), we are persuaded that Petitioner sufficiently demonstrates, for purposes of this Decision, that the combination of Stewart and 3GPP-Summary discloses limitations 3.pre and 3.a–3.c and that a person having ordinary skill in the art would have combined the teachings of Stewart and 3GPP-Summary in the manner set forth in the Petition.

d) Conclusion Regarding Claim 3

Based on the current record, there is a reasonable likelihood that Petitioner will prevail in demonstrating that claim 3 is unpatentable as obvious in view of Stewart and 3GPP-Summary

4. Claims 1, 2, and 4–6

Because Petitioner demonstrates a reasonable likelihood of success in proving that at least one claim of the ’486 patent is unpatentable, we institute on all grounds and all claims raised in the Petition. *See* 37 C.F.R. § 42.108(a). Therefore, at this stage of the proceeding, it is not necessary for us to provide an assessment of every challenge raised by Petitioner, especially, as in this case, when Patent Owner does not separately argue

¹¹ The undisputed limitations are limitations 3.pre and 3.a–3.c, which includes the preamble. Because Petitioner has sufficiently shown that the prior art teaches the preamble, we need not determine at this time whether the preamble is limiting. *See Nidec*, 868 F.3d at 1017.

those claims. *See* Prelim. Resp. 28–30. Those challenges, in our view, are best left for trial after full development of the record.

F. Anticipation and Obviousness over Stewart

Because Petitioner demonstrates a reasonable likelihood of success in proving that at least one claim of the ’486 patent is unpatentable, we institute on all grounds and all claims raised in the Petition. *See* 37 C.F.R.

§ 42.108(a). Therefore, at this stage of the proceeding, it is not necessary for us to provide an assessment of every challenge raised by Petitioner.

However, to provide guidance to the parties, we address Patent Owner’s additional arguments.

1. Analysis of Claim 3

a) Limitation 3.d

Petitioner argues that Stewart discloses limitation 3.d. Pet. 34, 47–50. Alternatively, Petitioner argues that a person having ordinary skill in the art would have found it obvious to add the claimed buffer. *Id.* at 35–36, 47–50. We provide guidance on the parties’ arguments below.

(1) Anticipation

With regard to anticipation, Petitioner argues that “[b]uffering is a well-known process of temporarily storing information for transmission.” Pet. 34 (citing Ex. 1025; Ex. 1026; Ex. 1007 § 2.4; Ex. 1003 ¶¶ 114–115). “[C]onsequently,” according to Petitioner, “a [person having ordinary skill in the art] would have understood that Stewart discloses buffering the systematic bits, ‘Parity 1’ stream, and ‘Parity 2’ stream in a block matrix of respective block interleavers because they temporarily store bits in the respective block matrices for transmission.” *Id.* (citing Ex. 1005 4:14–34, 4:46–48; Ex. 1001, 6:26–51); *see also id.* at 47 (“Stewart discloses to a [person having ordinary skill in the art] that the process of storing codeword

bits into the block matrix of a block interleaver (Fig. 5) entails buffering because buffering is a well-known process of temporarily storing bits for transmission.”); *id.* at 48–49 (discussing Stewart Figures 4 and 11). In further support of this, Petitioner argues that “interleavers are known to include memories or buffers.” *Id.* (citing Ex. 1038, 7:6- 14; Ex. 1039, 1:53-60; Hochwald, ¶¶114-115).

Petitioner does not specifically point to buffers in Stewart. Instead, Petitioner focuses on what a person having ordinary skill in the art would have understood. *See* Pet. 34 (“a [person having ordinary skill in the art] would have understood”), 47 (“Stewart discloses to a [person having ordinary skill in the art]”). We note that anticipation does not require an explicit statement of a limitation; rather, “[a]nticipation is established when one skilled in the art would reasonably understand or infer from the prior art reference’s teaching that every claim [limitation] was disclosed in that single reference.” *Genentech, Inc. v. Hospira, Inc.*, 946 F.3d 1333, 1340 (Fed. Cir. 2020) (quotations and citations omitted; second alteration in original). It is not clear, however, on this record that simply because buffering was well-known it follows that a person having ordinary skill in the art would have understood that Stewart discloses buffering. To the extent, however, that buffering, as recited in the ’486 patent, encompasses temporarily storing bits, Petitioner’s anticipation contentions may have merit.

(2) Obviousness

In the alternative, Petitioner argues that limitation 3.d would have been obvious in view of Stewart. *See* Pet. 35, 47–48. Specifically, Petitioner argues that a person having ordinary skill in the art “would have found it obvious to use the block matrices of Stewart’s interleavers to buffer

bits . . . to advantageously store information to support transmission and retransmission processes.” *Id.* Petitioner directs us to a retransmission in a HARQ (hybrid automatic repeat request) process that uses buffers to improve the throughput of communications. *Id.* (citing Ex. 1040 ¶¶ 34–37, 45; Ex. 1041, 4:1–7, 4:32–58, 11:48–57, 15:40–34; Ex. 1027 ¶ 34; Ex. 1003 ¶ 116).

We understand Petitioner’s argument as using each of the individual interleavers as a buffer. *See* Pet. 47–48 (“Stewart, as discussed in §I.A.1(a), also renders obvious using interleavers as buffers, for example, to support a retransmission process.”). This would result in one buffer for the interleaver of the systematic bits, one buffer for the interleaver of the first parity bit stream, and one buffer for the interleavers of the second parity bit stream. To the extent the claim limitation encompasses using three separate buffers, this argument has some merit. However, if the claim is construed to require a single buffer for interleaved systematic bits, interleaved first parity bits, and interleaved second parity bits, then we would question the sufficiency of Petitioner’s argument. We note that the parties have not explicitly construed limitation 3.d. We decline to offer any more guidance in light of the lack of briefing on the meaning of the term.

In this regard, we request that the parties address whether the claim is limited to a single buffer or can encompass multiple buffers. In briefing the issue, the parties should address similar limitations in independent claims 1 and 5. Failure to offer an explicit construction of the limitations with detailed reasoning to support that construction in the Patent Owner’s Response and the Petitioner’s Reply will be deemed a forfeiture of any claim construction argument.

(3) Limitation 3.e

Petitioner argues that Stewart discloses limitation 3.e. Pet. 50–58. For the reasons set forth below, we are sufficiently persuaded by Petitioner’s argument.

Based on the current record, we are persuaded that Stewart discloses that the UE or BS reads out “codeword bits” from the systematic and parity block interleavers for transmission. Ex. 1003 ¶¶ 143–145; Ex. 1005, 2:51–53, 5:6–15, Fig. 5. As shown in Figure 3, a “redundancy version selector” selects one of eight redundancy levels (numbered zero through seven) that selects a starting point to commence reading. Ex. 1005, 3:25–36, 4:8–10, 5:57–6:13, 6:41–7:24, Figs. 3, 11; Ex. 1003 ¶¶ 143–145.

For at least one of the redundancy versions (version zero), the coded bits of the systematic interleaver are read to completion prior to the bits being read from either of the parity interleavers. Ex. 1005, 6:41–51, 6:57–61, Fig. 6; Ex. 1003 ¶ 146.

For at least one of the redundancy versions (versions one, two, and three), the first and second parity bits are read from the respective interleaver while no bits are read from the systematic interleaver. Ex. 1005, 6:41–52, 6:62–7:4, Fig. 6; Ex. 1003 ¶¶ 147–148. Because no systematic bits from systematic block interleavers are selected to be transmitted, the first and second parity bits are selected over the systematic bits. Ex. 1003 ¶¶ 149–150.

Patent Owner argues that “[a]t most, Stewart appears to disclose collecting the interleaved bits for transmission in the Bit Priority Mapper (BPM) 304 of Fig[ure] 3.” Prelim. Resp. 26. Patent Owner further argues that “prior to transmission, the systematic and parity bits are read into a BPM (bit priority mapper) array.” *Id.* at 27 (citing Ex. 1005, 8:10–18).

According to Patent Owner, “the BPM gives priority to bits in a manner unrelated to the redundancy version.” Prelim. Resp. 27. Instead, Patent Owner argues, “the BPM priority is based on ‘placing systematic bits in positions of high reliability,’ not based on plurality of redundancy version as required by claim element [3.e].” *Id.* at 27–28 (citing Ex. 1005, 7:55–62).

We do not agree with Patent Owner’s argument, which does not address the features Petitioner relies on. Although, as Patent Owner points out, Stewart uses a Bit Priority Mapper, this is used after the Redundancy Version Selector. *See* Ex. 1005, Fig. 3. It is therefore of no moment that the Bit Priority Mapper does not select a redundancy level as that selection was already performed.

G. Stewart and TS25.212

As discussed above, because Petitioner demonstrates a reasonable likelihood of success in proving that at least one claim of the ’486 patent is unpatentable, we institute on all grounds and all claims raised in the Petition. *See* 37 C.F.R. § 42.108(a). However, to provide guidance to the parties, we address the additional arguments Patent Owner made on this ground.

1. Overview of TS25.212

TS25.212 is a technical specification titled “3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Multiplexing and channel coding (FDD) (Release 5).” Ex. 1008, 1. TS25.212 “describes the characteristics of the Layer 1 multiplexing and channel coding in the FDD mode of UTRA.” *Id.* at 7. According to TS25.212:

Data stream from/to MAC and higher layers (Transport block / Transport block set) is encoded/decoded to offer transport services over the radio transmission link. Channel coding scheme is a combination of error detection, error correcting . . .

rate matching, and interleaving and transport channels mapping onto/splitting from physical channels.

Id. at 9.

Figure 17 of TS25.212 is reproduced below:

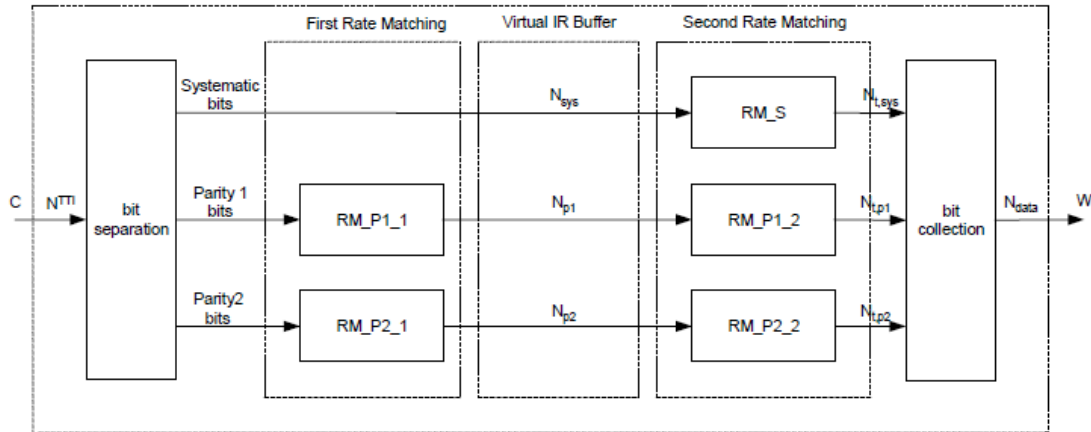


Figure 17: HS-DSCH hybrid ARQ functionality

Figure 17 of TS25.212 shows the HS-DSCH hybrid ARQ functionality. *Id.* at 58; *see also id.* at 8 (“ARQ Automatic Repeat Request”). TS25.212 explains the hybrid ARQ functionality as follows:

The hybrid ARQ functionality matches the number of bits at the output of the channel coder to the total number of bits of the HS-PDSCH set to which the HS-DSCH is mapped. The hybrid ARQ functionality is controlled by the redundancy version (RV) parameters. The exact set of bits at the output of the hybrid ARQ functionality depends on the number of input bits, the number of output bits, and the RV parameters.

The hybrid ARQ functionality consists of two rate-matching stages and a virtual buffer as shown in [Figure 17].

The first rate matching stage matches the number of input bits to the virtual IR buffer, information about which is provided by higher layers. Note that, if the number of input bits does not exceed the virtual IR buffering capability, the first rate-matching stage is transparent.

The second rate matching stage matches the number of bits after first rate matching stage to the number of physical channel bits available in the HS-PDSCH set in the TTI.

Id. at 58.

2. *Reason to Combine Stewart and TS25.212*

Petitioner argues that a person having ordinary skill in the art would have combined the relevant teachings of Stewart and TS25.212.¹² Pet. 65–67, 75–77, 78–79. For the reason set forth below, we are sufficiently persuaded by Petitioner’s argument.

TS25.212 teaches a “hybrid ARQ functionality consist[ing] of two rate-matching stages and a virtual buffer.” Ex. 1008 § 4.5.4. “The first rate matching stage matches the number of input bits to the virtual IR buffer, information about which is provided by higher layers. . . . The second rate matching stage matches the number of bits after first rate matching stage to the number of physical channel bits available in the HS-PDSCH set in the TTI.” *Id.* We are sufficiently persuaded that a person having ordinary skill in the art would have been motivated to use TS25.212’s buffering scheme with Stewart to support the simultaneous loading of bits into an interleaver while bits are transmitted from the buffer. *See* Ex. 1003 ¶ 193 (testifying that “[a] person [having] ordinary skill in the art would at least have been motivated to modify Stewart to use TS25.212’s teachings of a ‘virtual IR buffer’ that stores bits for the reasons I discussed above pertaining to combining Stewart and 3GPP-Summary”); *see also id.* ¶ 179 (explanation for combining Stewart and 3GPP-Summary). A person having ordinary skill in the art “would have understood that a buffer temporarily stores data so

¹² Petitioner describes the combination at pages 72 through 75 and 77 through 78 of the Petition.

that it could readily be accessed in order to be retransmitted when a transmitting device is requested to carry out a retransmission as part of a HARQ.” *Id.* ¶ 179. “Because additional coded bits for transmission are read out from the buffer, the wrap-around functionality allows coded bits that would have otherwise been discarded to be transmitted which also allows for lower coding rates, which are desirable in, for example, particular channel conditions, and allows for greater flexibility in Stewart’s system.” *Id.*

Patent Owner argues that the “proposed combination of Stewart and TS 25.212 would be contradictory and simply would not work.” Prelim. Resp. 30. Specifically, Patent Owner argues that “TS 25.212 uses the same transport channel multiplexing structure of an earlier version of TS 25.212 (v3.5.0) that was expressly rejected by Stewart.” *Id.* Patent Owner further argues that “[b]y proposing an alleged improvement to this prior system now advanced by Petitioner, Stewart has proposed a system incompatible with the transport channel multiplexing structure of TS 25.212.” *Id.* at 31.

We do not agree with Patent Owner’s argument. First, based on the current record, Patent Owner has not shown there that TS25.212 v3.5.0 (2000-12)—which is described in Stewart (Ex. 1005, 3:47–63) and shown in Stewart Figure 2—is materially the same as the version of TS25.212 Petitioner is relying on here (v5.1.0 (2002-06)). *See* Prelim. Resp. 30–32. Specifically, Patent Owner fails to direct us to any discussion of TS25.212. Although Exhibit 1008 (TS25.212) is cited on page 30 of the Preliminary Response, that is a typo and the quoted material actually comes from Stewart (Exhibit 1005), not TS25.212 (Exhibit 1008). Thus, we are left only with attorney argument unsupported by evidence, which is not enough to rebut Petitioner’s showing. *See Johnston v. IVAC Corp.*, 885 F.2d 1574, 1581 (Fed. Cir. 1989) (“Attorney’s argument is no substitute for evidence.”); *Elbit*

Systems of America, LLC v. Thales Visionix, Inc., 881 F.3d 1354, 1359 (Fed. Cir. 2018) (“[a]ttorney argument is not evidence’ and cannot rebut other admitted evidence” (quoting *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017)); *Gemtron Corp. v. Saint-Gobain Corp.*, 572 F.3d 1371, 1380 (Fed. Cir. 2009) (unsworn attorney argument is not evidence)).

Second, based on the current record, we see significant differences between Stewart Figure 2, which shows TS25.212 v.3.5.0, and TS25.212. On the one hand, Stewart Figure 2 shows only a single stage rate matching stage 210. *See* Ex. 1005, 3:47–63, Figure 2. On the other hand, TS25.212 shows two rate matching steps, just like the improvement in Stewart. *Compares* Ex. 1005, Fig. 3, *with* Ex. 1008 § 4.5.4.

Third, we note that Kenneth Stewart, the primary inventor of Stewart, did exactly what Petitioner argues would have been obvious. In a later paper on incremental redundancy schemes, Mr. Stewart uses a version TS25.212 (version 5.0.0) and that includes a figure that is identical to the one shown in TS25.212. *See* Ex. 1037,¹³ 1, 5. That figure is the basis for Petitioner’s argument. *See* Pet. 72–77.¹⁴ This suggests that, contrary to Patent Owner’s argument, a person having ordinary skill in the art at the relevant time would

¹³ Ghosh, A., Stewart, K., Ratasuk, R., Buckley, E., & Bachu, R. (2002). Incremental redundancy (IR) schemes for W-CDMA HS-Dsch. *The 13th IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, 1078–1082. <https://doi.org/10.1109/pimrc.2002.1045193>.

¹⁴ We note that it appears that Patent Owner included a copy of that figure, TS25.212 Figure 17, as Figure 10 of the ’486 patent. *See* Ex. 1003 ¶ 191. Patent Owner did not identify that figure as prior art. *See* Ex. 1001, Fig. 10.

have considered the most recent version of TS25.212. And it contradicts Patent Owner's argument that Stewart rejected later versions of TS25.212.

H. Stewart/Stewart and 3GPP-Summary/Stewart and TS25.212 in view of Motorola

Petitioner argues that claims 1–6 would have been obvious over Stewart/Stewart and 3GPP-Summary/Stewart and TS25.212 in view of Motorola. Pet. 79–87.

1. Overview of Motorola

Motorola is a submission for discussion and decision to “TSG-RAN HSDPA Ad-Hoc” at a meeting in Sophia Antipolis, France on November 5–7, 2001. Ex. 1006, 1. Motorola is titled “A New Hybrid-ARQ Scheme Using Incremental Redundancy” and proposes “a simple IR scheme based on block interleaving and symbol priority mapping.” *Id.* The proposed scheme provides, *inter alia*, “flexible and fine-grained support of predefined redundancy versions at each transmission with progressive reduction in effective coding rates.” *Id.*

According to Motorola, “[t]he preferred approach is to pre-define a static set of eight redundancy versions,” wherein each redundancy version contains a starting row in either the “Systematic” or “Parity” interleaver. Ex. 1006, 5.

Coded bits are read from the selected starting row until either the desired number of bits has been read or the end of the $N_{i,\max_row}$ th row is reached. In the case the end of the $N_{i,\max_row}$ th row is reached, reading then continues from the first row of the other interleaver as shown in Figure 4 [(not reproduced)]. Starting rows are computed such that they are equally spaced throughout the lowest rate codeword supported by the UE.

Id. Motorola explains that “if the lowest supported coding rate by the UE for a particular transmission is 1/3 then the redundancy versions shown in Figure 5 apply.” *Id.* at 6.

2. *Analysis*

Besides relying on the arguments addressed above and further arguing that the additional references do not cure the alleged deficiencies, Patent Owner does not address these grounds. *See* Prelim. Resp. 32–34. Accordingly, further discussion of these grounds is best left for trial after full development of the record.

III. CONCLUSION

Following § 314, we have determined that the totality of the information presented at this stage shows there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition, and we institute on all grounds raised and all claims challenged in the Petition. Additionally, we decline to exercise our discretion under §§ 314(a) to deny institution.

Our factual findings, conclusions of law, and determinations at this stage of the proceeding are preliminary, and based on the evidentiary record developed thus far. This is not a final decision as to the patentability of claims for which *inter partes* review is instituted. Our final decision will be based on the record as fully developed during trial.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1–6 of the ’486 patent on the unpatentability grounds asserted in the Petition; and

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FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision.

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Patent 9,065,486 B2
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