

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,

Petitioner

v.

LONGITUDE LICENSING LTD.,

Patent Owner

IPR2023-01286
U.S. Patent No. RE43,539

PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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PETITIONER’S EXHIBIT LIST

August 8, 2023

EX1001	U.S. Patent No. RE43,539 to Takahashi (“’539 patent”)
EX1002	Reissue Application File History of the ’539 patent (“’773 Reissue App”)
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EX1004	CV of Dr. Scott E. Thompson
EX1005	Prosecution File History of the Original Patent of ’539 patent (“’059 App”)
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EX1008	U.S. Patent No. 4,975,598 to Borkar (“Borkar”)
EX1009	U.S. Patent No. 3,356,858 to Wanlass (“Wanlass”)
EX1010	U.S. Patent No. 6,288,563 to Muljono et al. (“Muljono”)
EX1011	Order Granting Motion to Stay (Lenovo) (05-16-23)
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EX1014	U.S. Patent No. 5,194,765 to Dunlop et. al (“Dunlop”)
EX1015	U.S. Patent No. 4,612,466 to Stewart (“Stewart”)
EX1016	Dabral et al., Basic ESD and IO Design (1998) (“Dabral”)

LISTING OF CHALLENGED CLAIMS

Claim 1	
[1.0]	1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:
[1.1]	a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [N1] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];
[1.2.1]	a predriver with outputs for driving only said first n-channel MOS transistor [N1] and only said first p-channel MOS transistor [P1]
[1.2.2]	[the predriver]having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data,
[1.2.3]	[the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]; and
[1.3]	a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2],

[1.4]	wherein the output of the predriver is directly connected only to said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1] of said main driver.
Claim 2	
[2.0]	2. The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are equal to each other.
Claim 3	
[3.0]	The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are different from each other.
Claim 4	
[4.0]	The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor [P2] and said second n-channel MOS transistor [N2] have a smaller device size with a smaller gate width than said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1], and have a small effect on rise and fall times of pulses output from said main driver.
Claim 5	
[5.0]	5. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:
[5.1]	a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [P2] for driving a load according to said data, and at least a pair of a second p-channel MOS

	transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];
[5.2.1]	a predriver with outputs for driving only said first n-channel MOS transistor [P1] and only said first p-channel MOS transistor [N1]
[5.2.2]	[the predriver] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data,
[5.2.3]	[the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3],
[5.2.4]	[the predriver having] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]; and
[5.3]	a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2],
[5.4]	wherein the output of the predriver is directly connected only to said

	first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1] of said main driver.
Claim 6	
[6.0]	6. The output buffer circuit according to claim 5, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistor [P5], said sixth n-channel MOS transistor [N6], and said sixth p-channel MOS transistor [P6] are equal to each other.
Claim 7	
[7.0]	7. The output buffer circuit according to claim 5, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistors [P5], said sixth n-channel MOS transistors [N6], and said sixth p-channel MOS transistors [P6] are different from each other.
Claim 8	
	8. The output buffer circuit according to claim 5, wherein said second p-channel MOS transistor [P2] and said second n-channel MOS transistor [N2] have a smaller device size with a smaller gate width than said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1], and have a small effect on rise and fall times of pulses output from said main driver.
Claim 9	
[9.0]	9. An integrated semiconductor circuit device comprising:
[9.1]	an output buffer circuit according to claim 1;
[9.2]	a delay monitor circuit identical in circuit arrangement to said output buffer circuit and having transistors controlled according to said

	control signals in the same manner as with said output buffer circuit,
[9.3]	said delay monitor circuit having an output terminal connected to a dummy load determined from an actual load of said output buffer circuit based on a transistor size ratio between said output buffer circuit and said delay monitor circuit.
Claim 10	
[10.0]	10. An integrated semiconductor circuit device comprising:
[10.1]	an output buffer circuit according to claims 5; and
[10.2]	a delay monitor circuit identical in circuit arrangement to said output buffer circuit and having transistors controlled according to said control signals in the same manner as with said output buffer circuit,
[10.3]	said delay monitor circuit having an output terminal connected to a dummy load determined from an actual load of said output buffer circuit based on a transistor size ratio between said output buffer circuit and said delay monitor circuit.
Claim 11	
[11.0]	11. The integrated semiconductor circuit device according to claim 9, wherein said delay monitor circuit has transistors having a smaller device size with a smaller gate width than the transistors of said output buffer circuit.
Claim 12	
[12.0]	12. The integrated semiconductor circuit device according to claim 10, wherein said delay monitor circuit has transistors having a smaller device size with a smaller gate width than the transistors of said output buffer circuit.

I. INTRODUCTION

U.S. Patent No. RE43,539 (the “’539 patent”) relates to “an output buffer circuit for use in an integrated semiconductor circuit device.” EX1001, Title, 1:14-20. Western Digital Technologies, Inc. (“Petitioner” or “WDT”) respectfully requests that the Board review and cancel as unpatentable under (pre-AIA) 35 U.S.C. §103(a) claims 1-12 (“Challenged Claims”) of the ’539 patent, which is all the claims of the patent.

II. GROUNDS FOR STANDING

Petitioner certifies that the ’539 patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims. 37 C.F.R. § 42.104(a).

III. TECHNOLOGY BACKGROUND

Dr. Thompson’s declaration provides a background of the relevant technology, including transistors, primitive logic functions, CMOS, and output buffer circuits. EX1003, ¶¶21-37 (citing EX1009).

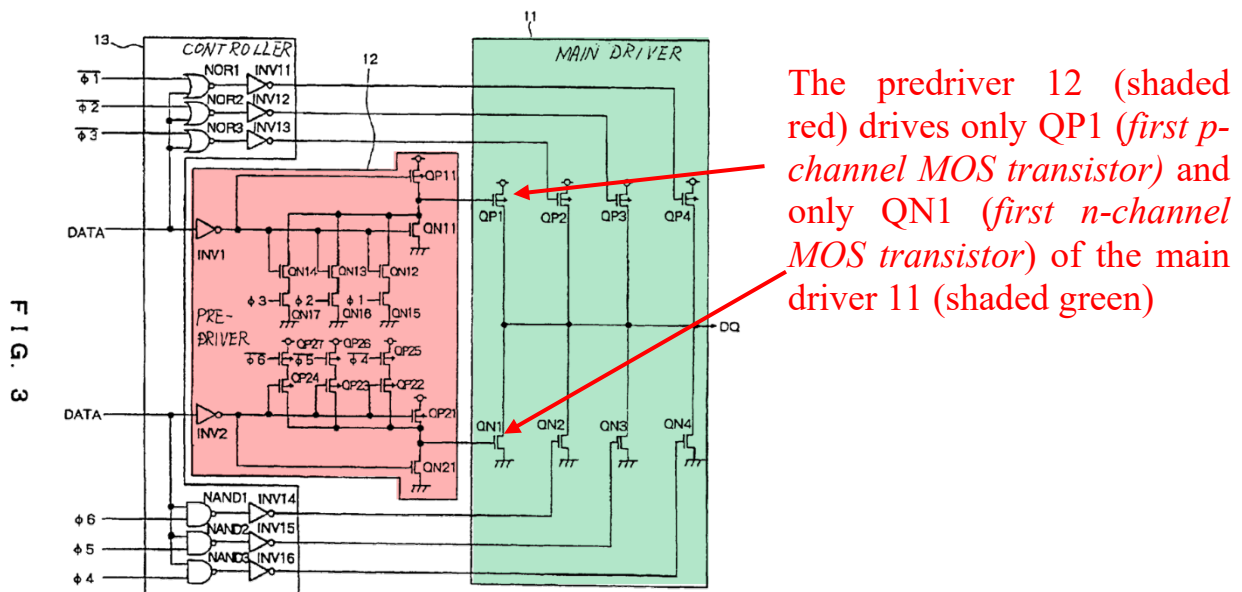
III. THE ’539 PATENT

A. Summary of the ’539 patent

The ’539 patent asserts that it provides an output buffer circuit “capable of sufficiently compensating for variations in the cross-point between rising and falling waveforms of output pulses and variations in the slew rate against variations in the power supply voltage and the ambient temperature even when the

output buffer circuit is incorporated in a system.” EX1001, 2:54-60. The ’539 patent then describes an output buffer circuit having a main driver 11 for driving a load, a predriver 12 for driving the main driver, and a controller 13 for generating signals to change the output impedance of main driver 11 and the slew rate according to control signals. EX1001, 2:61-63; EX1003, ¶¶38-43.

During prosecution, after multiple anticipation rejections, the amendment “*a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor*” resulted in allowance (emphasis original). This feature is annotated in FIG. 3 below. This feature, just like the other elements of the claims, was well-known to POSITA before its earliest claimed priority date. EX1003, ¶¶41-43.



EX1001, FIG. 3, annotated

B. Prosecution History

1. '059 App (Original)

The Office rejected claims as anticipated by Atsushi (JPub 2001-068986, cited by Applicant) in multiple office actions. EX1005, 91-95, 80, 53, 38; EX1003, ¶¶44-50.

Notice of Allowance issued, with Examiner Amendment of “a predriver with outputs for driving only said first in-channel MOS transistor and only said first p-channel MOS transistor output.” EX1005, 23 (emphasis original).

2. '773 Reissue

Applicant filed a reissue application with new claims, and cancelled them after multiple rejections. EX1002, 148, 128-140, 95, 57-58, 26; EX1003, ¶¶51-56.

IV. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art may be reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Here, a Person of Ordinary Skill in the Art (“POSITA”) at the time of the claimed invention would have a bachelor’s or the equivalent degree in electrical or computer engineering or a related field, and 2-3 years of professional experience relating to integrated circuit design. EX1003, ¶13. Furthermore, a person with less formal education but more experience, or more formal education but less experience, could have also met the relevant standard for POSITA. *Id.* However,

Petitioner does not imply that a person having an extraordinary level of skill should be regarded as POSITA.

V. CLAIM CONSTRUCTION

During IPR, claims are construed according to the standard as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b) (Nov. 13, 2018). Petitioner believes that, for the purposes of this proceeding and the analysis presented herein, no claim term requires express construction. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). Accordingly, this Petition analyzes the claims consistent with ordinary and customary meaning as would be understood by POSITA in light of the specification. *Phillips*, 415 F.3d at 1314-17; EX1003, ¶¶57-58.

VI. REQUESTED RELIEF

Petitioner asks the Board to institute trial and cancel the Challenged Claims.

VII. OVERVIEW OF CHALLENGES

A. Challenged Claims

Claims 1-12 (“Challenged Claims”) of the ’539 patent are challenged.

B. Statutory Grounds for Challenges

Ground	Claims	Basis
#1	1-3 and 5-7	§103(a) over Itoh in view of Skorup
#2	1-8	§103(a) over Itoh
#3	1-8	§103(a) over Itoh in view of Muljono

#4	9-12	§103(a) over Itoh in view of Skorup and Borkar
#5	9-12	§103(a) over Itoh in view of Borkar
#6	9-12	§103(a) over Itoh in view of Muljono and Borkar

Itoh was filed December 14, 2000, published October 4, 2001, and issued August 2, 2005. Muljono was filed December 31, 1998 and issued September 11, 2001. Itoh and Muljono are prior art under at least §§102(a) and 102(e).

Skorup issued March 9, 1976. Borkar issued December 4, 1990. Skorup and Borkar each are prior art under at least §§102(a) and 102(b).

C. Discretionary Denial is Not Warranted

Petitioner respectfully submits that the Board should not exercise its discretion under 35 U.S.C. §§314(a) or 325(d) to deny this Petition.

1. The Fintiv factors favor institution.

Denial would be improper based on factors in *Apple v. Fintiv*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential).

Factor 1: Stay in District Court Favors Institution

Six litigations concerning the '539 Patent are pending in CDCA, all involving the Patent Owner and WDT's customers. *See* X.B. WDT's motion to intervene was granted in the Amazon Action. EX1012. All litigations are stayed pending the resolution of the Amazon Action with respect to WDT. EX1011. This weighs strongly in favor of institution. *Snap, Inc. v. SRK Tech. LLC*, IPR2020-

00820, Paper 15 at 9 (PTAB Oct. 21, 2020) (precedential) (granting stay allays concerns about inefficiency and duplication efforts).

Factor 2: Unscheduled Trial Date Favors Institution.

In the Amazon Action with respect to WDT, the litigation is in its early stages. The Court has not set a case schedule. No claim construction briefing has been scheduled. No trial date has been set.

Factor 3: Lack of Investment in Parallel Proceedings Favors Institution.

The co-pending litigations are either stayed or in early stages. The lack of investment in the parallel proceedings favors institution.

Factor 4: No Overlapping Issues with the Parallel Proceeding Favors Institution.

There is no overlap of prior art issues at this time. If the Board institutes trial, Petitioner will not assert in the co-pending litigation the combination of references on which trial is instituted for the claims on which trial is instituted, to the extent Petitioner even asserts the same combination in the district court. *See Verizon v. Huawei*, IPR2020-01079, Paper 10 at 38 (finding a similar stipulation “mitigates the concern about overlapping issues” and weighs “against discretionary denial of the Petition”).

Factor 5: Whether Petitioner is Defendant Is Neutral.

Petitioner is an intervener in the Amazon Action with respect to WDT. This factor is neutral and should not be a basis for denying institution. *See HP Inc. v.*

Slingshot Printing LLC, IPR2020-01084, Paper 13 at 9 (having the “same parties as parallel proceeding” makes factor 5 “neutral”).

Factor 6: Other Circumstances Including Merits Favors Institution.

As detailed below, every element of the Challenged Claims is expressly shown in or obvious in view of well-known art, and as such, this petition “presents compelling evidence of unpatentability.” Director Vidal’s Guidance Memorandum, EX1013, 2. Even if the Board determines that the other *Fintiv* factors favor a discretionary denial—which they do not—the Director’s *Fintiv* Guidance strongly supports institution of this challenge. See *CommScope Technologies LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4-5 (PTAB Feb. 27, 2023) (precedential).

In short, investments in the parallel proceeding is minimal, and *Fintiv* factors are either neutral or weigh against discretionary denial. Thus, the *Fintiv* factors weigh in favor of institution.

2. Advanced Bionics Test Favors Institution.

In determining whether to institute an IPR, the Board may consider whether “the same or substantially the same prior art or arguments previously were presented to the Office.” §325(d); *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7 (PTAB Feb. 13, 2020).

The Advanced Bionics test regarding the prior art references favors institution because they were not the same or substantially the same art presented to the Office. The Examiner did not consider Itoh, Skorup, Muljono, or Borkar during the prosecution. Moreover, they are non-cumulative, because they teach the claimed features including those provided by the reasons for allowance of the '539 patent. *See* EX1005, 23.

VIII. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Overview of Prior Art

1. Itoh

Itoh is directed “an output buffer circuit that outputs an output signal having gentle rising and falling edges and a slew-rate control type output buffer circuit,” which provides an output signal with “less variation in transition time,” and can “cope with a high or low operational frequency.” EX1006, Title, 1:5-8, 4:60-65; EX1003, ¶¶59-67.

To achieve these objects, Itoh provides Embodiments 1-5 in two categories:

a. Category 1 (Embodiments 1-3): first method of slew rate control and additional pair(s) of output transistors for output impedance control

In the main driver, Embodiments 1, 2, and 3 each use a single pair of PMOS and NMOS transistors for achieving slew-rate control. They each include additional pair(s) of PMOS and NMOS transistors for output impedance control.

Embodiment 1 (FIGS. 5-7) has advantages including a small variation in the transition time of VOUT. EX1006, 9:40-67.

Embodiment 2 (FIG. 8) includes a plurality of pairs of additional PMOS and NMOS transistors that may be selected for output impedance control. EX1006, 10:36-42.

Embodiment 3 (FIG. 9) provides an inversion output buffer circuit. EX1006, 10:44-48.

b. Category 2 (Embodiments 4-5): second method of slew rate control and no additional pair(s) of output transistors for output impedance control

Each of Embodiments 4 and 5 use a single pair of PMOS and NMOS transistors for both slew-rate control and output impedance control.

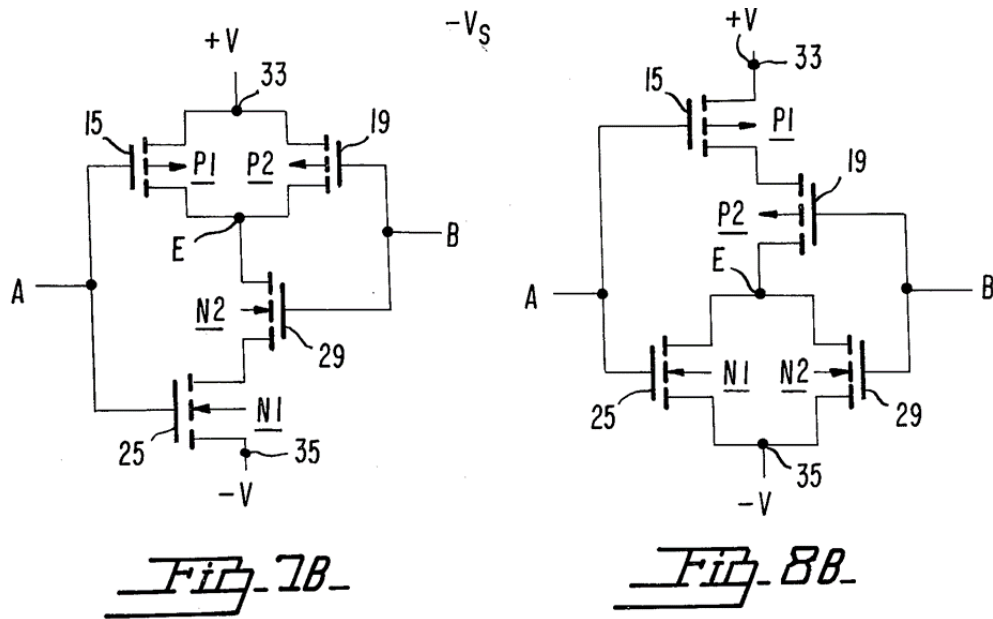
Embodiment 4 (FIGS. 10, 11, 12(a)-12(c)) provides a slew-rate control type output buffer circuit, which controls a slew rate of the output signal by controlling slew rates of the control signals applied to the output transistors. EX1006, 11:11-13. Advantages include reduced current consumption, a wide frequency band, and reduced noise. EX1006, 14:19-62.

Embodiment 5 (FIGS. 13-14) is similar to Embodiment 4 other than using a Schmitt inverter circuit. EX1006, 15:54-64.

2. Skorup

Skorup describes very fundamental schematic diagrams of CMOS implementation of logic gates (e.g., NAND gate, NOR gate). *See, e.g.*, EX1007,

FIGS. 7B and 8B; EX1003, ¶¶68-69.



EX1007, FIGS. 7B and 8B¹

3. *Muljono*

Muljono recognizes there is a need for output buffer addressing variations in process, supply voltage, and temperature (PVT), and as shown in FIG. 1 below, describes a compensation circuit that receives temperature detection and voltage detection signals. Impedance control signal is generated in response to the PVT for driver circuit 105, and slew rate control signal for predriver circuit 103 is generated in response to the PVT and impedance control signal. EX1010, 4:1-19.

¹ Below, some of the labels in FIGS. 7B and 8B are removed for clarity.

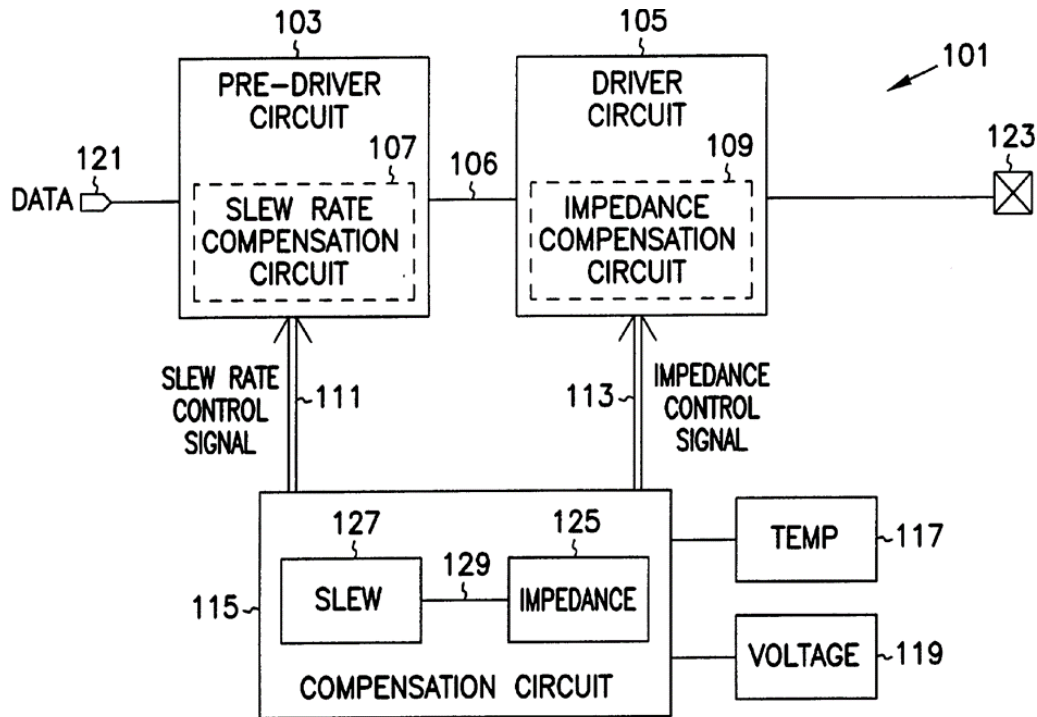


FIG. 1

EX1010, FIG. 1

4. Borkar

Borkar describes an output driver that “dynamically compensates for variations in temperature, voltage, and process.” EX1008, Abstract. To achieve this, “a **scaled down version** of an output driver is used to monitor speed variations due to temperate, process, and voltage,” which is “**compensated the same way the actual driver is,**” and the output “is fed back to the output driver which then performs the necessary compensation.” EX1008, Abstract; 7:5-15; EX1003, ¶¶72-73.

B. Ground 1: Claims 1-3 and 5-7 are Rendered Obvious under §103(a) over Itoh and Skorup.

Claims 1-3 and 5-7 are obvious under Itoh combined with Skorup. Limitations [1.1], [1.2.3], [1.3], [5.1], [5.2.3], [5.2.4], and [5.3] each recite the term “*in coaction with*.” The analysis below is based on POSITA’s understanding of its ordinary and customary meaning, which is consistent across these limitations. The analysis is further supported by the examples in ’539 patent. *See, e.g.*, EX1001, FIGS. 3 and 4 (illustrating that a pair of P2 and N2 (e.g., QP2 and QN2) drives the load using output DQ in coaction with a pair of P1 and N1 (QP1 and QN1) as recited in [1.1] because they work together to generate DQ); FIG. 3 (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction, and illustrating QP21 and QP27 connected in series for driving QN1 in coaction as recited in [1.2.3]); FIGS. 3, 4, and 7 (illustrating driving QN17 in coaction with QP2 and illustrating driving QP27 in coaction with QN2). EX1003, ¶74.

1. Reasons to Combine Itoh and Skorup

A POSITA would have been motivated to apply Skorup’s teaching of implementing various logic gates using CMOS (complementary and symmetrical pairs of p-channel MOSFET (PMOS) and n-channel MOSFET (NMOS) transistors in embodiments of Itoh. EX1003, ¶¶75-78.

Itoh describes an output buffer circuit using CMOS process, using PMOS and NMOS transistors and CMOS logic gates. *See, e.g.*, EX1006, FIGS. 5, 8, 9,

6:59-8:5.

In view of Itoh's need to implement the various logic gates in CMOS, a POSITA would have implemented the fundamental and well-known teachings of Skorup of CMOS implementation of logical gates in embodiments of Itoh, to achieve the benefits of the CMOS technology including high noise immunity and low static power consumption. EX1009, 1:22-63.

2. Claim 1

[1.0] 1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

Itoh teaches the preamble to the extent that it's limiting. EX1003, ¶¶79-82.

First, Itoh describes an output buffer circuit that receives data (VIN) in the form of an input pulse train and then drives a corresponding output signal VOUT. EX1006, FIGS. 3 and 6 (illustrating generally VIN and VOUT); 3:15-17.

Second, Itoh describes outputting data at a predetermined output impedance and slew rate. For example, referring to FIG. 5, Itoh describes that “the first drive circuit 22 causes the external output signal VOUT to gently rise and fall, and the second drive circuit 23 secures the low-output impedance characteristics.” EX1006, 8:2-5, FIG. 6. Furthermore, a POSITA would have understood by securing the low-output impedance characteristics, the second drive circuit of FIG. 5 performs output impedance control to provide an output having a relatively low impedance.

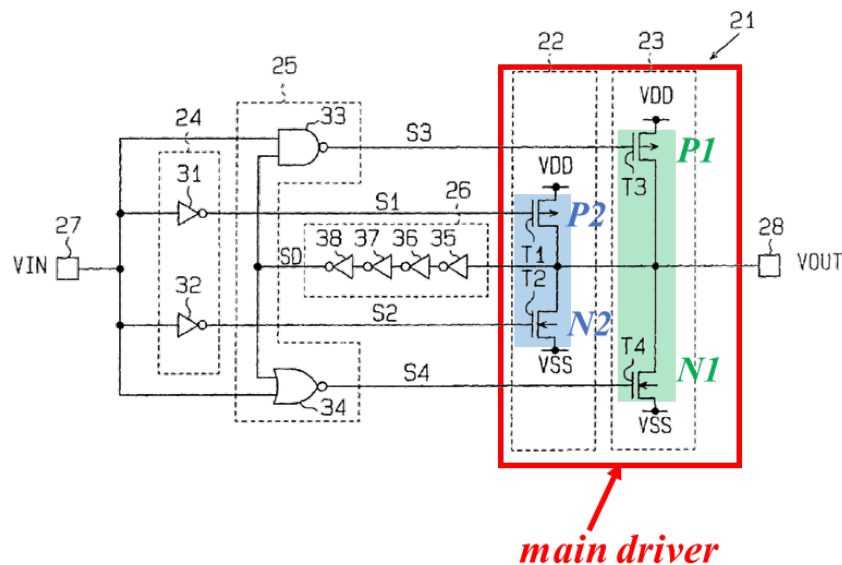
Therefore, Itoh teaches the preamble.

[1.1] a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [N1] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];

Itoh teaches this element. EX1003, ¶¶83-89.

Specifically, Embodiment 2 teaches this element. As shown in annotated FIG. 5 of Itoh below, Itoh describes that an output driver circuit 21 includes a main driver (circuits 22 and 23) for driving a load at VOUT 28.

Fig.5



EX1006, FIG. 5, annotated

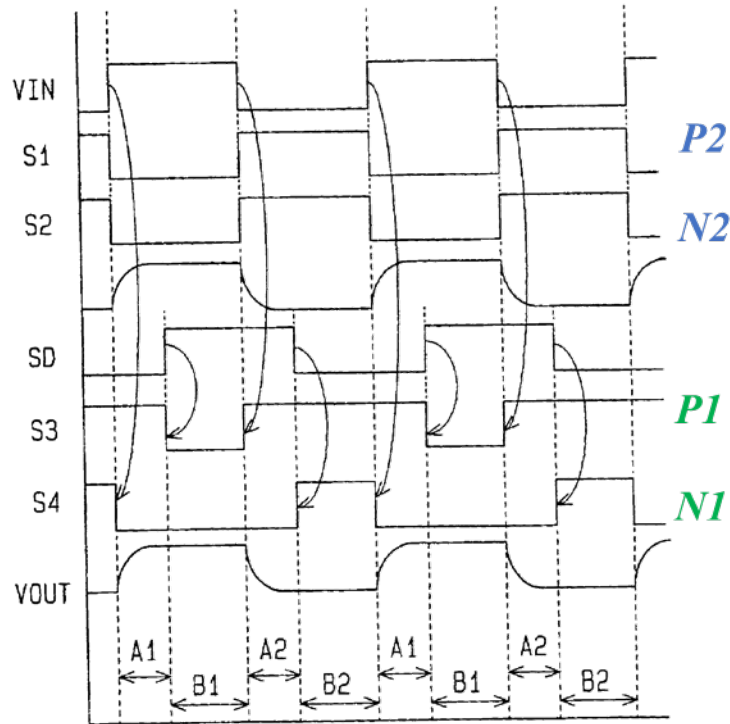
The main driver includes circuit 23, which includes a pair of a first p-channel MOS transistor (transistor T3 annotated in green as P1) and a first n-

channel MOS transistor (transistor T4 annotated in green as N1) for driving a load at VOUT according to said input data (VIN). *See, e.g.*, EX1008, 1:51-53.

The main driver further includes circuit 22, which includes a pair of a second p-channel MOS transistor (transistor T1 annotated in blue as P2) and a second n-channel MOS transistor (transistor T2 annotated in blue as N2). This pair of P2 and N2 works together and therefore, in coaction with the pair of P1 and N2 for generating the VOUT for driving the load. *See, e.g.*, EX1001, '539 patent, FIGS. 3 and 4 (illustrating a similar configuration, where a pair of QP2 and QN2 drives the load in coaction with a pair of QP1 and QN1 by providing DQ).

Referring to annotated FIG. 6 of Itoh below, Dr. Thompson describes in detail the operation and how transistors P1, N1, P2, N2 work in coaction with the corresponding control signals for providing the VOUT for drive the load. EX1006, 8:6-9:39.

Fig.6



EX1006, FIG. 6, annotated

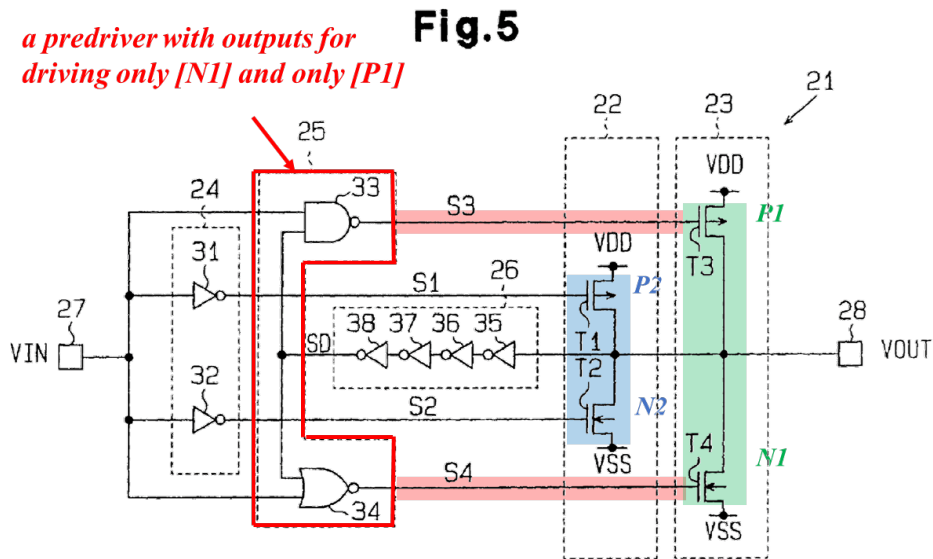
Therefore, Itoh teaches this element.

[1.2.1] a predriver with outputs for driving only said first n-channel MOS transistor [N1] and only said first p-channel MOS transistor [P1]

Itoh teaches this element. EX1003, ¶¶90-92.

As shown in annotated FIG. 5 of Itoh below, Itoh describes a predriver circuit 25 positioned before the main driver 23, and with outputs (S3 and S4) for driving only said first n-channel MOS transistor (T4, annotated as N1) and only said first p-channel MOS transistor (T3, annotated as P1). While Itoh refers to circuit 25 as “control circuit 25,” a POSITA would have understood that circuit 25

is a predriver because it is a stage positioned before and provides signals to drive the main driver. EX1006, 7:28-34, FIG. 6; *see* similarly EX1006, FIGS. 8 and 9.



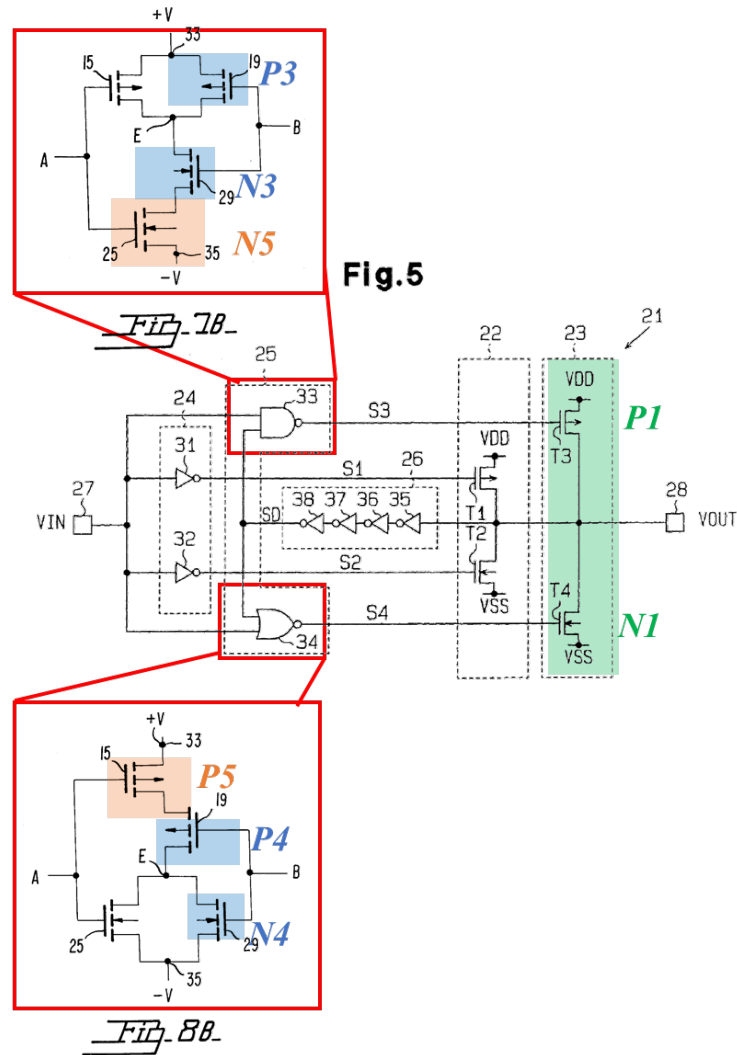
EX1006, FIG. 5, annotated

Therefore, Itoh teaches this element.

[1.2.2] [a predriver...] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data,

Itoh in view of Skorup renders obvious this element. EX1003, ¶¶93-103.

Itoh teaches NAND gate 33 and NOR gate 34. *See* Itoh Embodiment 1 (FIG. 5). As shown in Example 1.1 illustrated below, Itoh's NAND gate 33 and NOR gate 34 are shown as being implemented using Skorup's teachings of CMOS logic gates using complementary pairs of PMOS and NMOS transistors. *See* EX1007, FIGS. 7B and 8B.



Example 1.1
Itoh Embodiment 1 (FIG. 5) Combined with Skorup

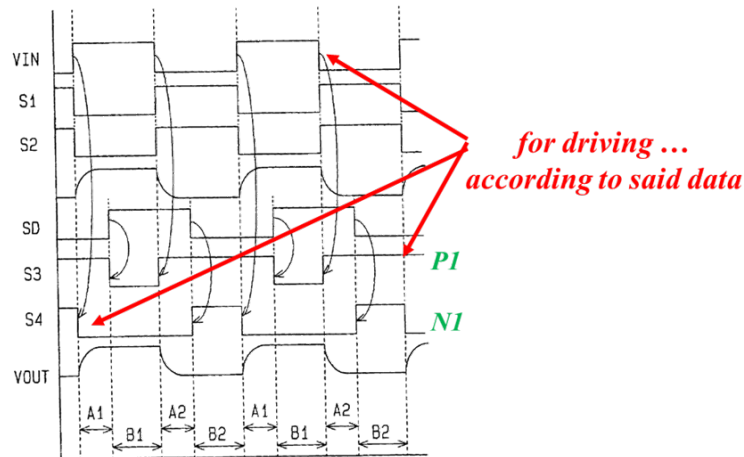
A POSITA would have applied Skorup's implementation of NAND and NOR gates to Itoh which uses CMOS, because Skorup teaches the well-known fundamental knowledge of CMOS technology for implementing logic gates (e.g., NOT, NAND, and NOR), and a POSITA would have implemented it in output driver circuits. EX1007, 2:29-32, 2:33-36; 2:49-52; *see also, e.g.*, EX1009, FIG. 6; EX1015, FIGS. 1, 2B, and 2C; EX1009, 22-63; Ground 1: Reasons to Combine

Itoh and Skorup.

As shown in the figure above, in the combination, the NAND gate includes a p-channel transistor 19 (annotated in blue as P3), which corresponds to the claimed “third p-channel transistor,” and an n-channel transistor 29 (annotated in blue as N3), which corresponds to the claimed “third n-channel transistor.” These two transistors, P3, N3, drive Itoh’s p-channel transistor T3 (annotated in green as P1) according to VIN, because Itoh’s NAND gate 33 receives VIN as an input and generates signal S3 for driving Itoh’s main driver transistor P1. *See e.g.*, EX1006, FIG. 6 (S3 generated based on VIN for driving P1), 7:41-51.

Further, in the Example 1.1 illustrated above, the NOR gate 34 of Itoh’s predriver circuit 25 is implemented with another pair of p-channel transistors and another pair of n-channel transistors as taught by Skorup. As shown in the figure above, Skorup’s NOR gate includes a p-channel transistor 19 (annotated in blue as P4), which corresponds to the claimed “third p-channel transistor.” Skorup’s NOR gate also includes an n-channel transistor 29 (annotated in blue as N4), which corresponds to the claimed “third n-channel transistor”. These two transistors, P4, N4, drive Itoh’s n-channel transistor T4 (annotated in green as N1) according to VIN, because signal S4 from NOR gate 34 is used for driving Itoh’s main driver transistor N1. Also, Itoh’s NOR gate 34 includes as one of its inputs, the input data signal VIN. *See also*, EX1006, FIG. 6.

Fig.6



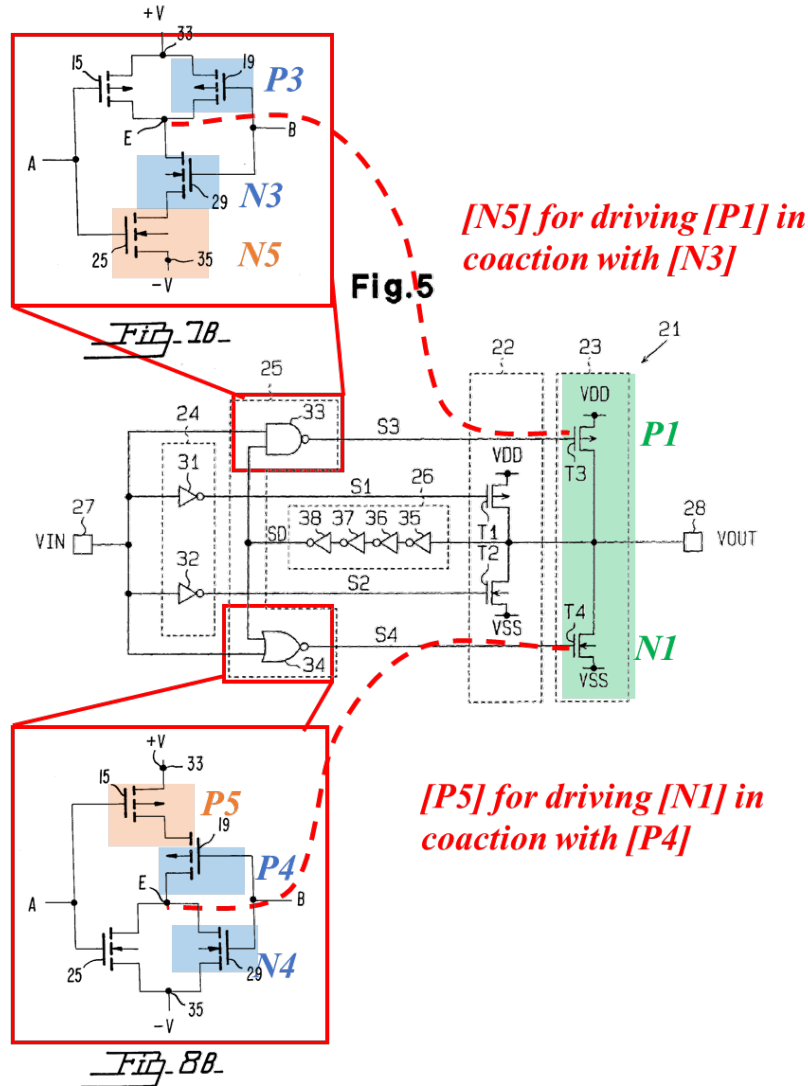
EX1006, FIG. 6, Annotated

Therefore, Itoh in view of Skorup renders obvious this element.

[1.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]; and

Itoh in view of Skorup renders obvious this element. EX1003, ¶¶104-111.

Continuing with the Example 1.1 (Itoh Embodiment 1 (FIG. 5) combined with Skorup), the combination further includes the claimed fifth n-channel MOS transistor and fifth p-channel MOS transistor.



Example 1.1 Itoh Embodiment 1 (FIG. 5) combined with Skorup

In Example 1.1 as illustrated above, Skorup's NAND gate further includes an n-channel transistor 25 (annotated in orange with N5) that teaches the claimed fifth n-channel MOS transistor. Skorup's NAND gate, including transistor N5, is used for driving the main driver transistor P1 by sending the signal S3 generated at output terminal E of the NAND gate. N5 drives P1 in coaction with N3, because

N3 and N5 are connected in series and work together for generating the output signal S3 at output terminal E of FIG. 7B.

Likewise, Skorup's NOR gate further includes a p-channel transistor 15 (annotated in orange with P5) that teaches the claimed fifth p-channel MOS transistor. Skorup's NOR gate, including transistor P5, is used for driving the main driver transistor N1 by sending the signal S3 generated at output terminal E of the NAND gate. P5 drives N1 in coaction with P4, because P5 and P4 are connected in series and work together for generating the output signal S4 at output terminal E of FIG. 8B.

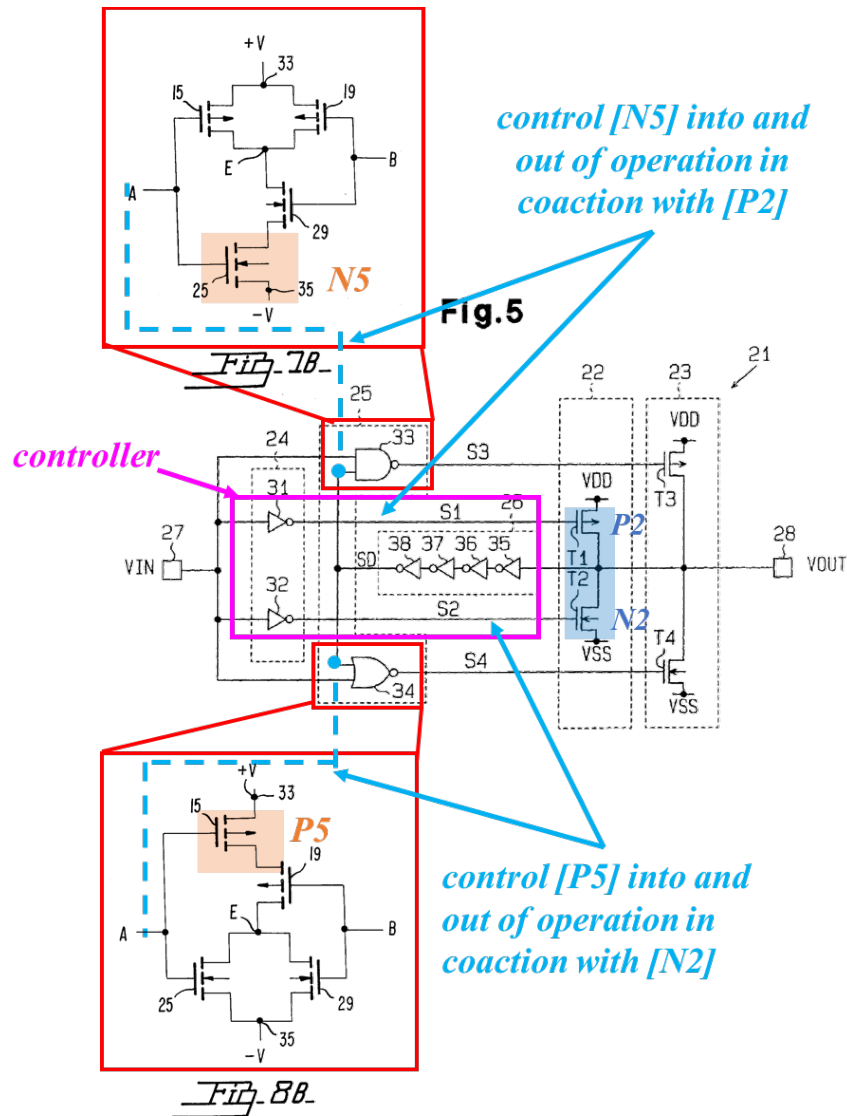
In the Example 1.1, the configuration of N5 for driving P1 in coaction with N3 (where N3 and N5 are connected in series for generating S3 for driving P1) and the configuration of P5 for driving N1 in coaction with P4 (where P4 and P5 are connected in series for generating S4 for driving N1) are similar to configurations of those corresponding transistors in the '539 patent. *See, e.g.,* EX1001, FIG. 3 (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction).

Therefore, Itoh in view of Skorup renders obvious this element.

[1.3] a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2],

Itoh in view of Skorup renders obvious this element. EX1003, ¶¶112-122.

Continuing with the Example 1.1 (combination of Itoh Embodiment 1 of FIG. 5 and Skorup) as illustrated below, a controller (including inverter 24 and delay circuit 26) is supplied with the external output signal VOUT, and outputs the control signals (including SD, S1, and S2). Signal SD is split into two signals, one for NAND gate 33 and another for NOR gate 34. The delay circuit 26 was a well-known self-timed control circuit for providing a control signal based on the feedback VOUT (which by itself is considered a control signal) by adjusting the number of pairs of inverters.



Example 1.1 Itoh Embodiment 1 (FIG. 5) combined with Skorup

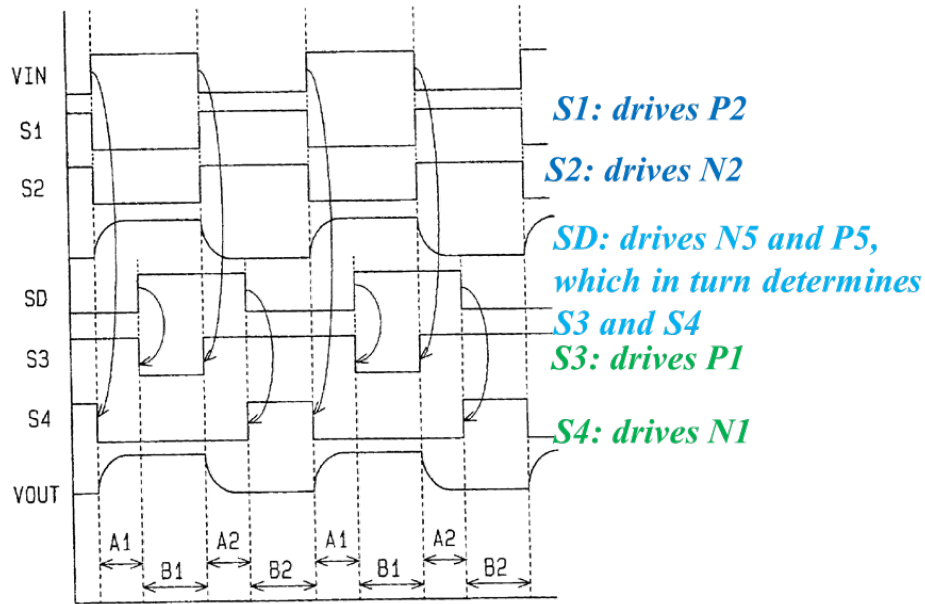
Referring to the delay circuit 26, Itoh describes “the first drive circuit 22 causes the external output signal VOUT to gently rise and fall, and the second drive circuit 23 secures the low-output impedance characteristic,” using a delay circuit 26. Itoh, 7:51:8-5. The technique for using a delay circuit receiving VOUT and generating a control signal using VOUT was well-known in the art as a “self-

timed control signal.” Itoh further describes the generation of control signals S1 and S2. EX1006, 7:34-40.

In Example 1.1 as illustrated, a POSITA would have been motivated to supply control signal SD to NAND gate 33 (e.g., through terminal A of 7B to gate of N5), which drives N5 into and out of operation, and supply the control signal SD to NOR gate 34 (e.g., through terminal A of FIG. 8B to gate of P5), which drives P5 into and out of operation.

Referring to FIG. 6 of Itoh and providing a table of corresponding operation states of the signals and transistors, Dr. Thompson explains in detail that, in Example 1.1, signals (e.g., S1, S2, SD, S3, and S4) drive transitions (e.g., P1, N1, P5, N5, P2, N2) work in coaction to provide VOUT with the desired slew rate and impedance during periods A1, A2, B1, and B2. For example, control signal SD, together with control signal S1, controls N5 into and out of operation in coaction with P2. Further, control signal SD, working together with control signal S2, controls P5 into and out of operation in coaction with N2.

Fig.6



EX1006, FIG. 6, annotated

	A1	B1	A2	B2
VIN	L→H	H	H→L	L
S1/P2	L/On	L/On	H/Off	H/Off
SD/N5	L/Off	H/On	H/On	L/Off
S3/P1	H/Off	L/On	H/Off	H/Off
S2/N2	L/Off	L/Off	H/On	H/On
SD/P5	L/On	H/Off	H/Off	L/On
S4/N1	L/Off	L/Off	L/Off	H/On
VOUT	Rising	VPP	Falling	VSS

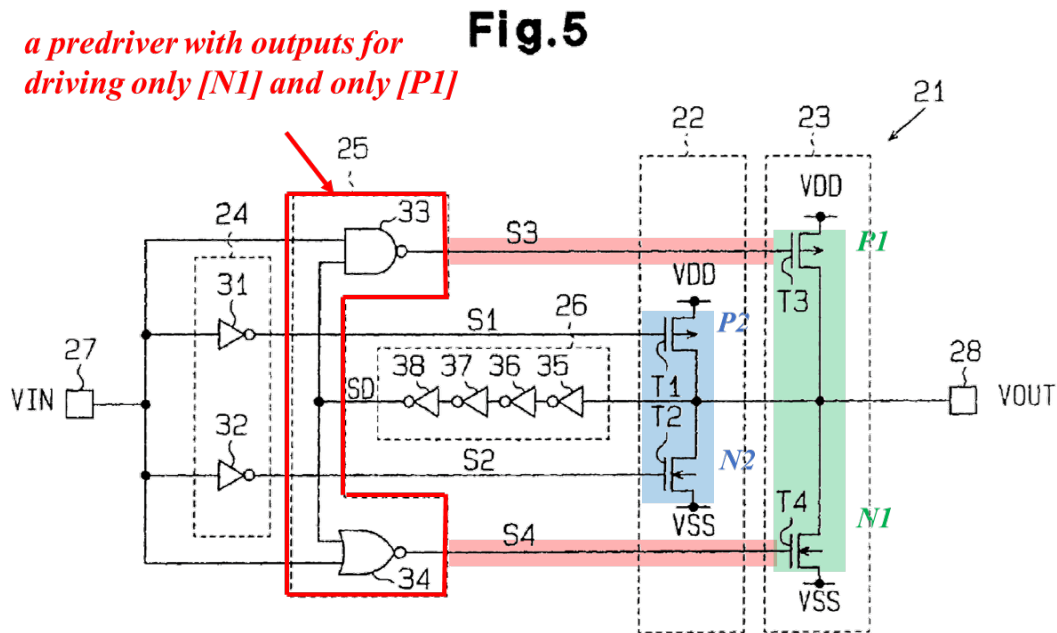
Example 1.1, Operation States
Itoh Embodiment 1 (FIG. 5) combined with Skorup

Accordingly, Itoh in view of Skorup renders obvious this element.

[1.4] wherein the output of the predriver is directly connected only to said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1] of said main driver.

Itoh teaches this element. EX1003, ¶¶123-126.

As shown in annotated FIG. 5 of Itoh below, Itoh teaches the output of the predriver (S3 from NAND gate 33 and S4 from NOR gate 34 of predriver 25) is directly connected only to P1 and N1 of said main driver. *See also* Ground 1:[1.2.1].



Example 1.1
Itoh Embodiment 1 (FIG. 5) combined with Skorup

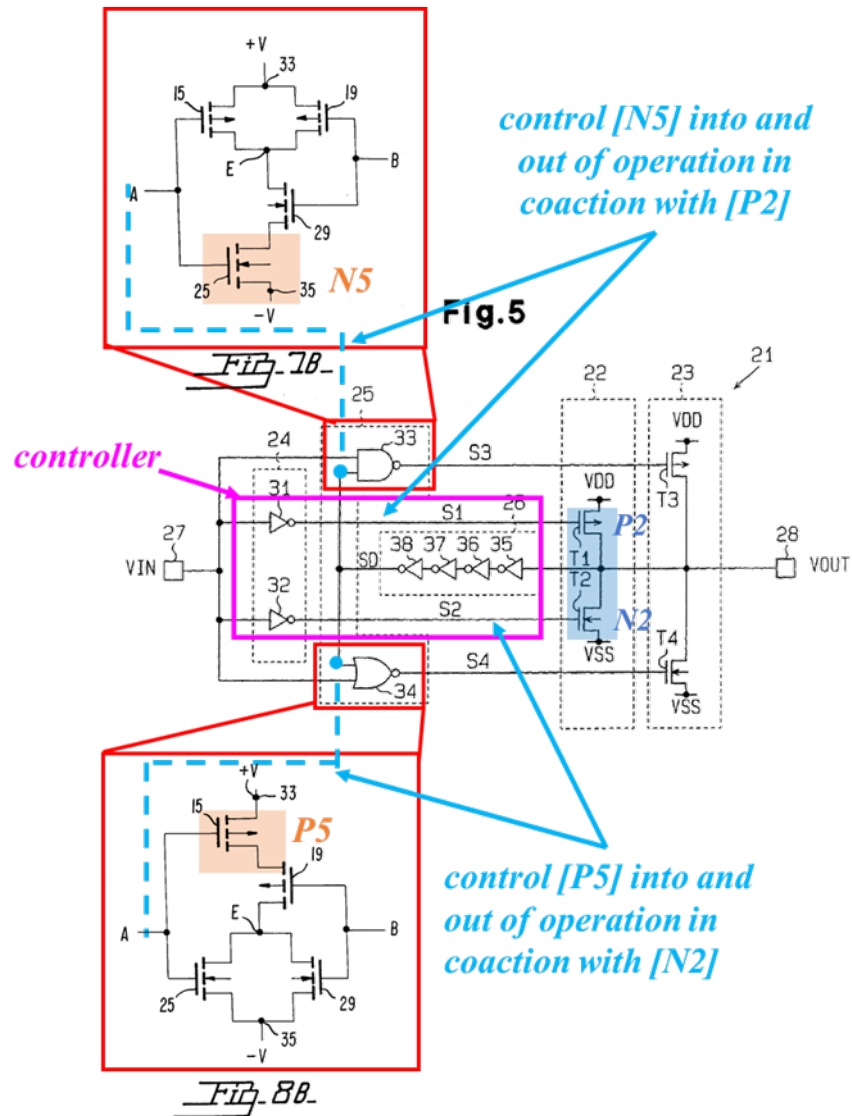
3. Claim 2

[2.0] 2. The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are equal to each other.²

Itoh in view of Skorup renders obvious this element. EX1003, ¶¶127-129.

Specifically, as shown in Example 1.1 illustrated below, the number (2) of P2 and N2 equals the number (2) of N5 and P5.

² There is no antecedent basis for the term “*transistors*” in claims 2, 3, 6, and 7, and as such, a POSITA would have understood that the term “*transistors*” as recited includes “at least a transistor.”



Example 1.1 Itoh Embodiment 1 (FIG. 5) combined with Skorup

4. Claim 3

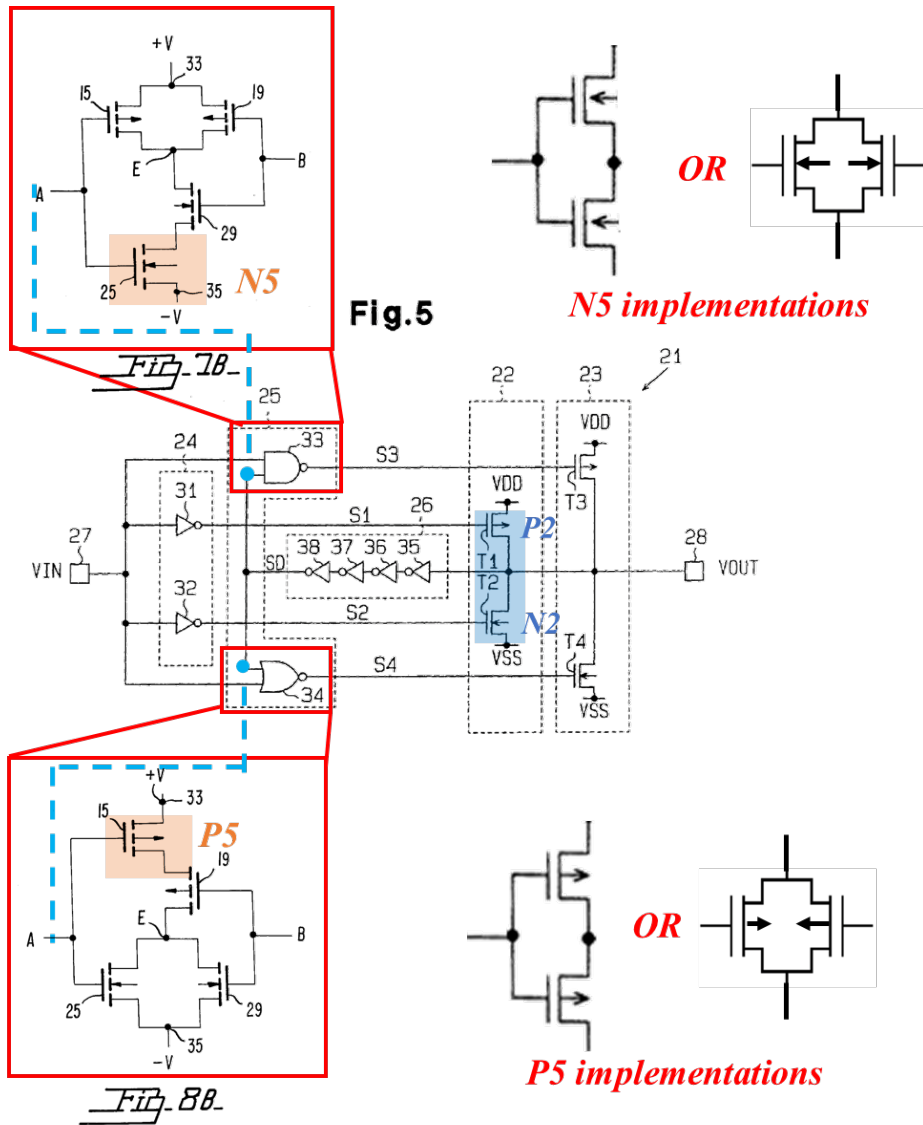
Itoh in view of Skorup, in further view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element. EX1003, ¶¶130-138.

It is important to understand the basic, fundamental knowledge of a

POSITA. For example, it is fundamental that a resistor shown in a circuit diagram as a single resistor can be physically implemented using multiple resistors in series.

Similarly, a POSITA would have been motivated to implement a transistor (e.g., P5 or N5) using two or more unit transistors connected in series or parallel, to achieve desired properties (e.g., a desired transistor size using either fixed configuration or digitally controlled element sizing), for the benefits of design flexibility and element sizing control. *See, e.g.*, EX1014, Abstract, 5:7-12, FIG. 3, 4:59-60, 5:7-12; EX1008, FIG. 3.

As shown in Example 1.1 illustrated below, in Example 1.1, a POSITA would have been motivated to implement one or more transistors (e.g., P5 or N5) each using two or more MOS transistors (e.g., connected in series or parallel). In such examples, the number (2) of P2 and N2 is different from the number (e.g., 3, 4, etc.) of N5 and P5.



Example 1.1
Itoh Embodiment 1 (FIG. 5) combined with Skorup

Similar analysis applies to the case where one or more of P2 and N2 is implemented with two or more unit transistors.

5. Claim 5

[5.0]-[5.2.2]

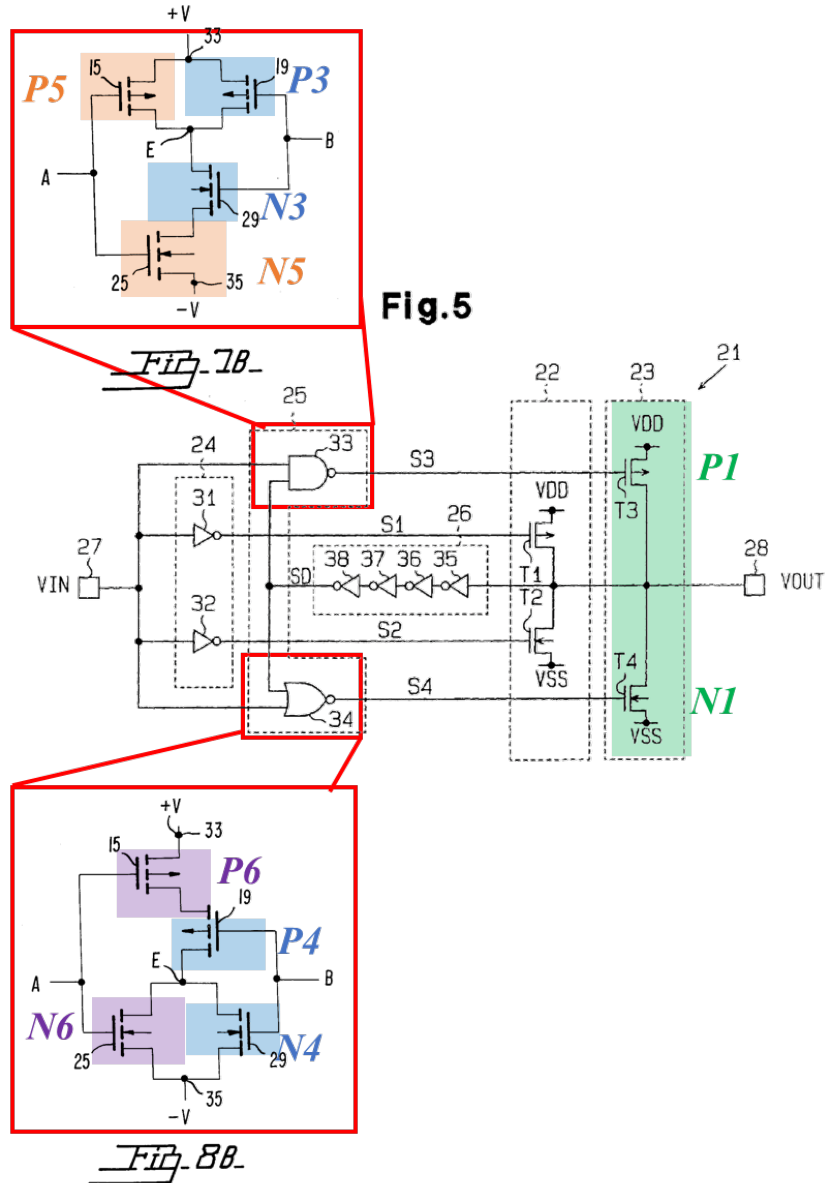
Itoh in view of Skorup renders obvious these elements for the reasons

discussed at Ground 1:[1.0]-[1.2.2]. EX1003, ¶¶139-142.

[5.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3],

Itoh in view of Skorup renders obvious this element. EX1003, ¶¶143-148.

As shown in Example 1.1 below and discussed at [1.2.2], in the combination, the predriver 25 includes NAND gate 33 and NOR gate 34, each implemented with complementary PMOS and NMOS transistors. The predriver 25 has N5 (EX1007, FIG. 7B, 25) for driving P1 (by sending S3 generated at output terminal E of FIG. 7B to the gate of P1) in coaction with N3 (EX1007, FIG. 7B, 29), because N3 and N5 are connected in series and work together for generating the output signal S3 at output terminal E of FIG. 7B.



Example 1.1 Itoh Embodiment 1 (FIG. 5) Combined with Skorup

Further, the predriver 25 has P5 (EX1007, FIG. 7B, 15) for driving P1 (by sending S3 generated at output terminal E of FIG. 7B to the gate of P1) in coaction with P3 (EX1007, FIG. 7B, 19), because P3 and P5 are connected in parallel and work together for generating the output signal S3 at output terminal E of FIG. 7B.

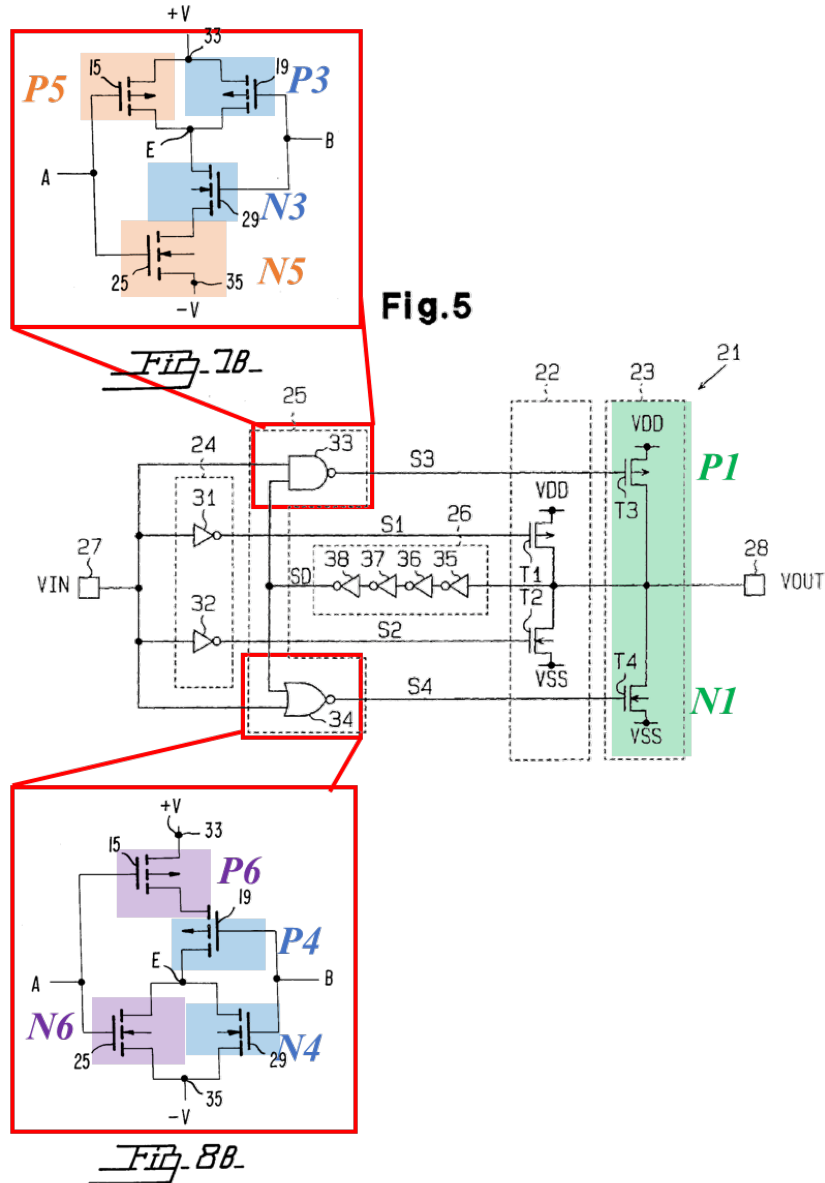
In the combination, the configuration of P5 for driving P1 in coaction with P3 (where P3 and P5 are connected in parallel) and the configuration of N5 for driving P1 in coaction with N3 (where N3 and N5 are connected in series) are similar to configurations of those corresponding transistors in the '539 patent. *See, e.g.,* EX1001, FIG. 3 (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction).

Therefore, Itoh in view of Skorup renders obvious this element.

[5.2.4] [the predriver having] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]; and

Itoh in view of Skorup renders obvious this element. EX1003, ¶¶149-154.

Continuing with the Example 1.1 illustrated below, the predriver 25 includes NAND gate 33 and NOR gate 34, each implemented with complementary PMOS and NMOS transistors as taught by Skorup. The predriver 25 has P6 (EX1007, FIG. 8B, 15) for driving P1 (by sending S4 generated at output terminal E of FIG. 8B to the gate of N1) in coaction with P4 (EX1007, FIG. 8B, 19), because P6 and P4 are connected in series and work together for generating the output signal 43 at output terminal E of FIG. 8B.



Example 1.1 Itoh Embodiment 1 (FIG. 5) Combined with Skorup

Further, the predriver 25 has N6 (EX1007, FIG. 8B, 25) for driving N1 (by sending S4 generated at output terminal E of FIG. 8B to the gate of N1) in coaction with N4 (EX1007, FIG. 8B, 29), because N6 and N4 are connected in parallel and work together for generating the output signal S4 at output terminal E of FIG. 8B.

As shown in the figure above, in the combination, the configuration of N6 for driving N1 in coaction with N4 (where N6 and N4 are connected in parallel for generating S4 for driving N1) and the configuration of P6 for driving N1 in coaction with P4 (where P4 and P5 are connected in series for generating S4 for driving N1) are similar to configurations of those corresponding transistors in the '539 patent. *See, e.g.,* EX1001, FIG. 3 (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction). A POSITA would have understood that two transistors connected either in series or in parallel are working in coaction for generating the output signal.

Accordingly, Itoh in view of Skorup renders obvious this element.

[5.3] a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2],

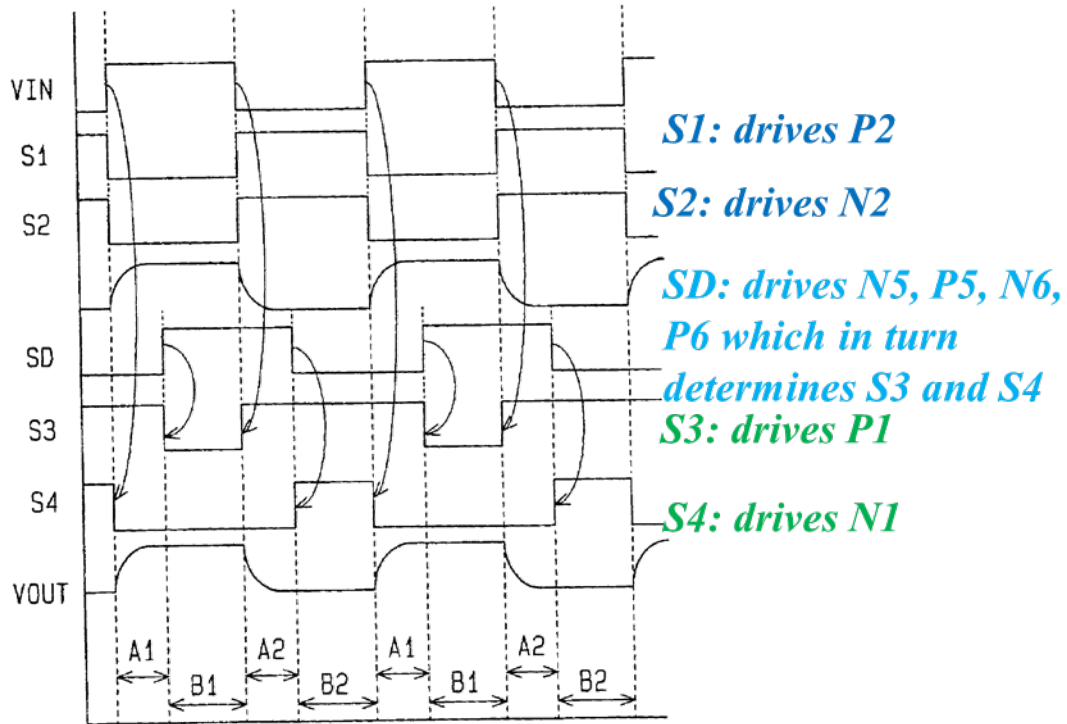
Itoh in view of Skorup renders obvious this element. EX1003, ¶¶155-161.

As shown in Example 1.1 illustrated below, a controller (including inverter 24 and delay circuit 26) is supplied with the external output signal VOUT, and outputs control signals (including SD, S1, and S2). The delay circuit 26 was a well-known self-timed control circuit for providing a control signal based on the feedback VOUT (which by itself is considered a control signal) by adjusting the number of pairs of inverters. EX1006, 7:51:8-5.

signal SD to NOR gate 34, by supplying the control signal SD to the gates of P6 and N6 (e.g., through terminal A of FIG. 8B), which turns N6 and P6 into and out of operation.

Referring to annotated FIG. 6 of Itoh and providing a table of operation states of the signals and transistors, Dr. Thompson explains in detail how signals (e.g., S1, S2, SD, S3, and S4) drive transitions (e.g., P1, N1, P5, N5, P2, N2, P6, N6) in coaction to provide VOUT with the desired slew rate and impedance during periods A1, A2, B1, and B2. Control signal SD, working together with control signal S1, controls P5 and N5 into and out of operation in coaction with P2. Further, control signal SD, working together with control signal S2, controls P6 and N6 into and out of operation in coaction with N2.

Fig.6



EX1006, FIG. 6, annotated

	A1	B1	A2	B2
VIN	L→H	H	H→L	L
S1/P2	L/On	L/On	H/Off	H/Off
SD/N5	L/Off	H/On	H/On	L/Off
SD/P5	L/On	H/Off	H/Off	L/On
S3/P1	H/Off	L/On	H/Off	H/Off
S2/N2	L/Off	L/Off	H/On	H/On
SD/P6	L/On	H/Off	H/Off	L/On
SD/N6	L/Off	H/On	H/On	L/Off
S4/N1	L/Off	L/Off	L/Off	H/On
VOUT	Rising	VPP	Falling	VSS

Example 1.1, Operation States

Itoh Embodiment 1 (FIG. 5) combined with Skorup

Accordingly, Itoh in view of Skorup renders obvious this limitation.

[5.4]

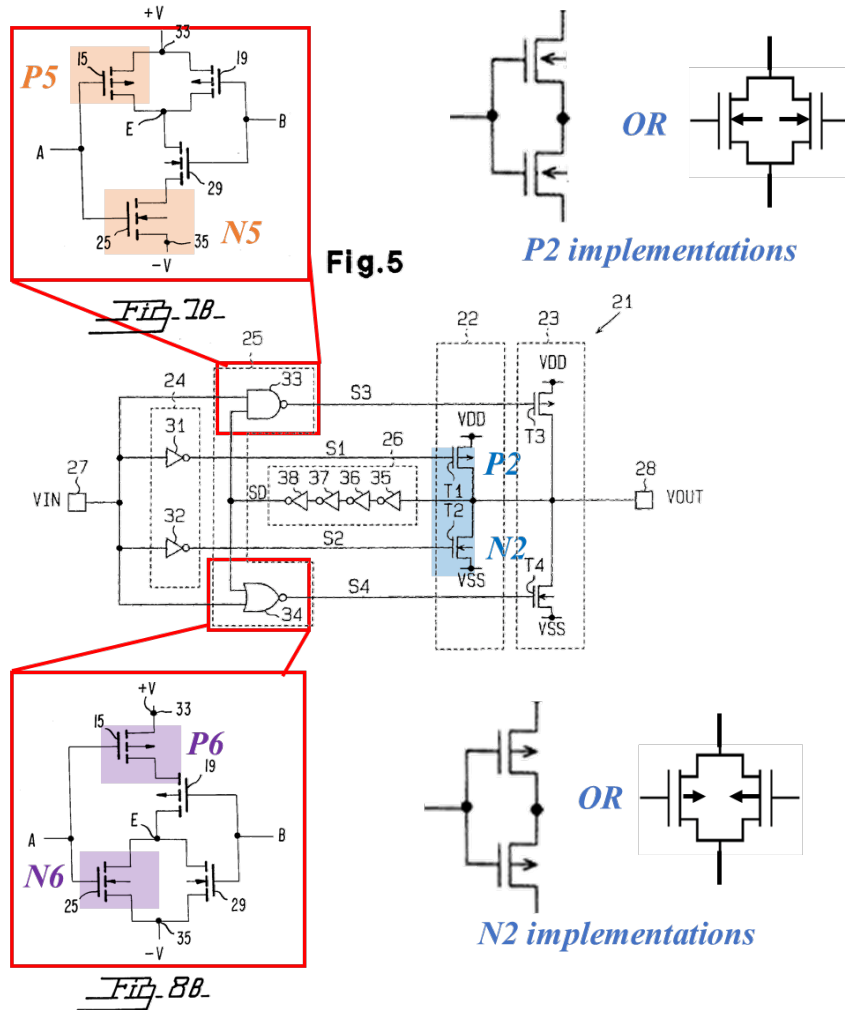
Itoh teaches this element for the reasons discussed at Ground 1:[1.4].

EX1003, ¶162.

6. Claim 6

Itoh in view of Skorup, in further view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element. EX1003, ¶¶163-166.

As discussed at [3.0] above, it is the basic, fundamental knowledge of a POSITA that a single transistor in circuit diagram can be physically implemented using multiple transistors in series or in parallel. As shown in Example 1.1 illustrated below, a POSITA would have been motivated to implement a transistor (e.g., P2 and N2) using two or more unit transistors connected in series or parallel, to achieve desired properties including desired transistor size.



Example 1.1 Itoh Embodiment 1 (FIG. 5) combined with Skorup

In the case where P2 and N2 each are implemented using two unit transistors, the number (4) of P2 and N2 equals the number (4) of N5, P5, N6, and P6.

7. Claim 7

Itoh in view of Skorup renders obvious this element. EX1003, ¶¶167-169.

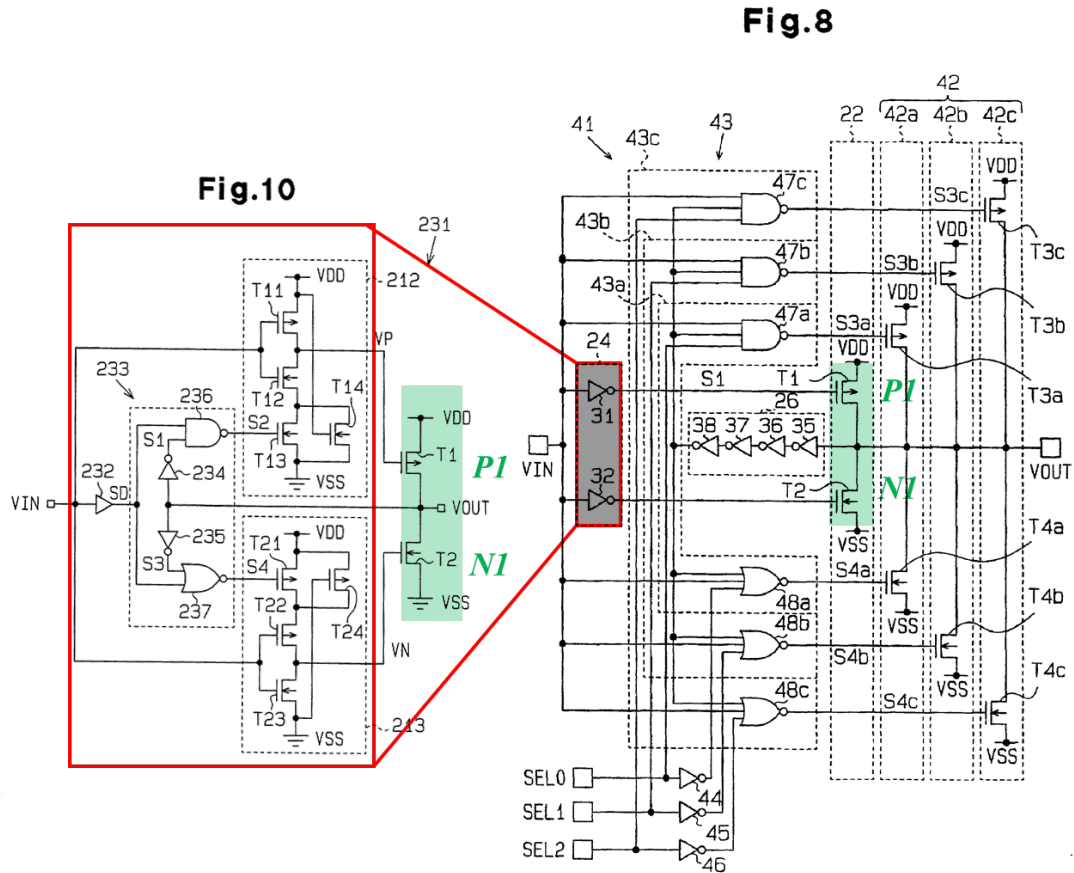
As shown in Example 1.1 illustrated below, in the output buffer circuit, the

control. *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F. 3d 982, 991

(“Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.”). EX1003, ¶¶170-177.

As discussed at VIII.A.1, Itoh describes two categories of embodiments. A POSITA would have been motivated to combine an embodiment from Category 1 and another from Category 2 to achieve the obvious, beneficial, and predictable results of an output buffer circuit having improved slew rate control (e.g., by using the slew-rate control type circuit taught by Category 2) and improved impedance control (e.g., by using the additional pair(s) of output transistors for output impedance control taught by Category 1).

Example 2.1 (Embodiments 2 and 4 of Iton combined) is illustrated below. While the analysis below focuses on Example 2.1, it similarly applies to other Category 1 and Category 2 combinations, a POSITA would have been motivated to select corresponding embodiments for combination based on its design needs.



Example 2.1 (Combination of Itoh Embodiments 2 and 4)

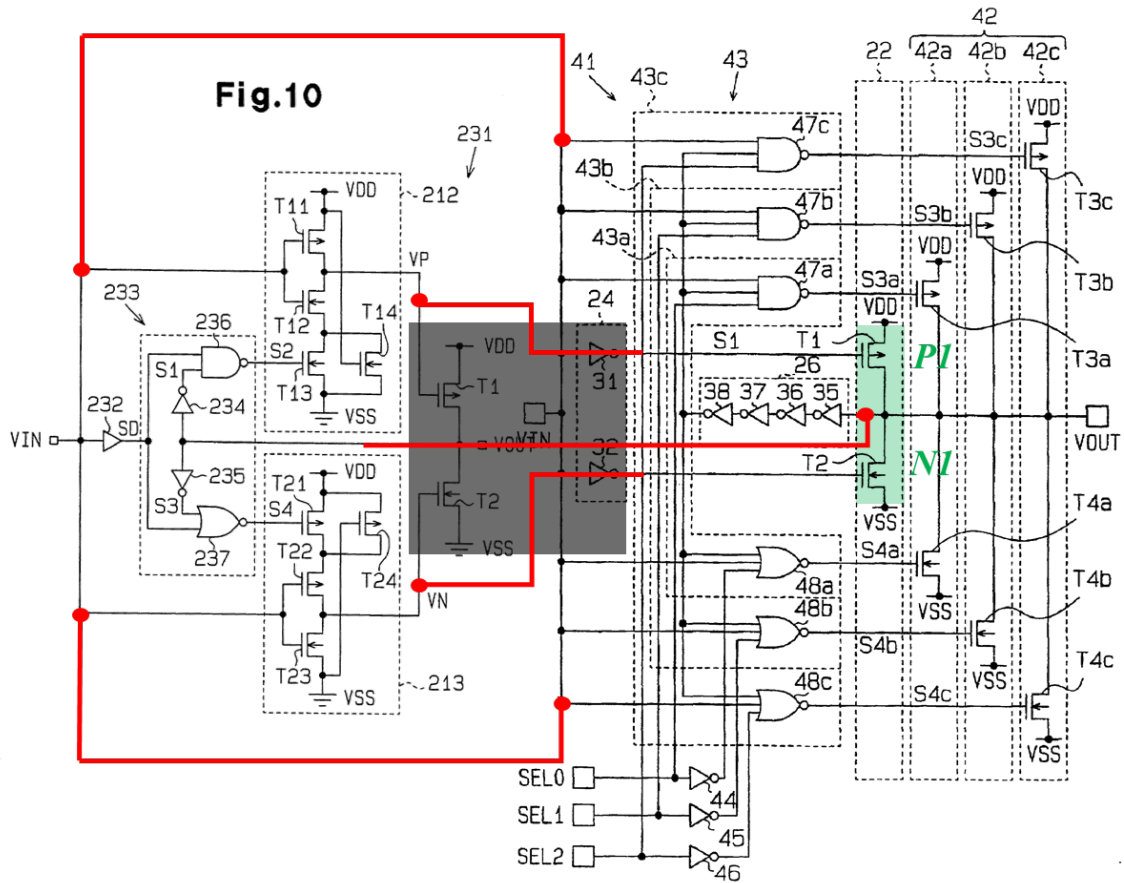
As shown in Example 2.1 illustrated above, a POSITA would have been motivated to combine Embodiment 2 (FIG. 8) with Embodiment 4 (FIG. 10) to achieve improved output impedance control and slew rate control. It would have been obvious to apply FIG. 10's slew-rate control type circuit for driving the pair of output transistors T1 and T2 (annotated as P1 and N1) to drive the same pair of output transistors T1 and T2 (also annotated as P1 and N1) in FIG. 8. Example 2.1 achieves improved output impedance control (provided by circuit 42 of FIG. 8 with the selectable pairs of output transistors) and improved slew rate control (provided

by the slew-rate control type circuit of FIG. 10), with various advantages of FIG. 10 including reduced current consumption, a wide frequency band, and reduced noise. EX1006, 14:19-62.

As shown in an implementation of Example 2.1 below³, combining Embodiments of Itoh would have been no more than the combination of known elements (well-known components of an output driver) according to known methods (performing basic IC design).

³ In analysis below, the grayed area indicating circuits not used in the combination is removed to avoid any confusion.

Fig.8



Example 2.1
(Combination of Itoh Embodiments 2 and 4)

Any modification required for the combination would have been within the skills of a POSITA. For example, it would have obvious to include various connections, adjust the delay time of delay circuit 26, and/or adjust the sizes of the transistors based on the design needs (e.g., required output impedance and slew rate).

2. Claim 1

[1.0] An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

To the extent that this preamble is limiting, Itoh teaches the preamble.

EX1003, ¶¶178-181.

First, as discussed at Ground 1:[1.0], embodiments of Itoh teach the preamble.

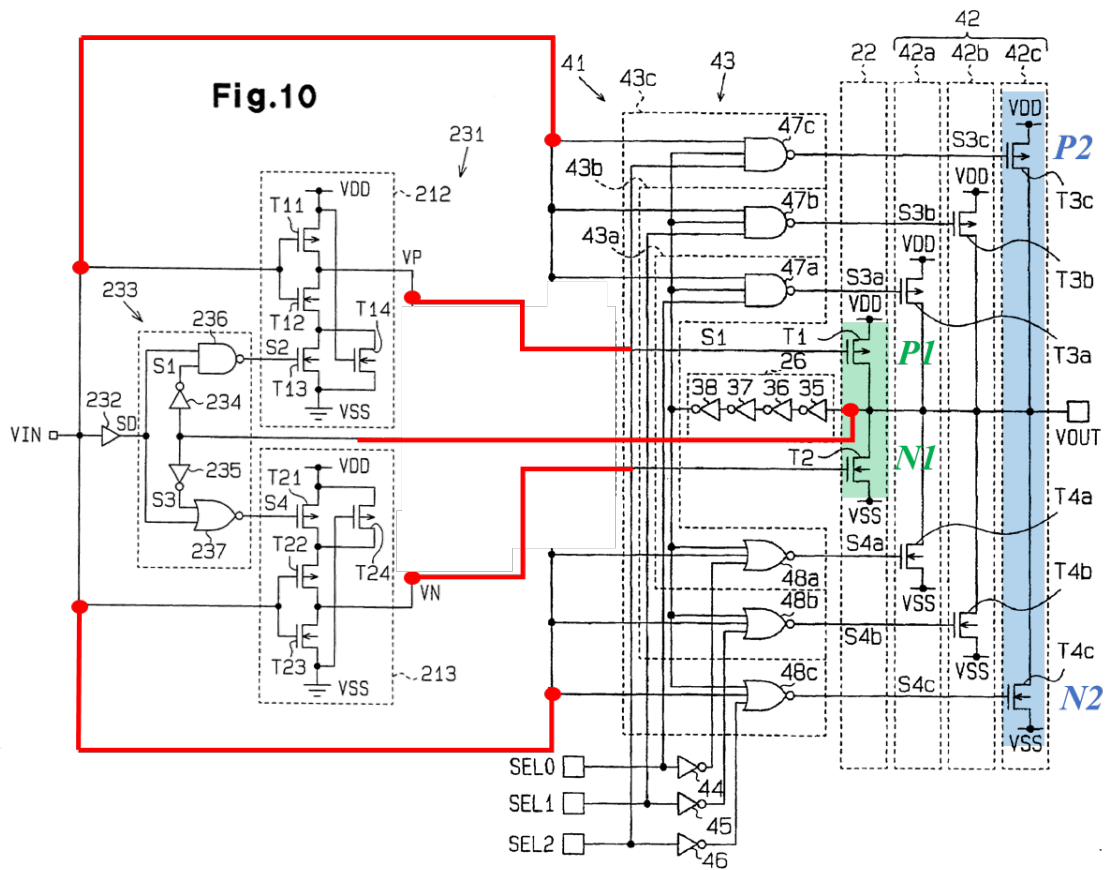
Second, as discussed in detail below, combinations of embodiments of Itoh, e.g, Exmple Embodiment 2.1 (Embodiments 2 and 4 combined), similarly provide an output buffer circuit that outputting data (VIN) in the form of an input pulse train, with output impedance control and slew rate control.

[1.1] a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [N1] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];

Itoh teaches this element. EX1003, ¶¶182-188.

As discussed at Ground 2: Reasons to Combine and as shown in Example 2.1 below, it would have been obvious to combine embodiments of Itoh to provide an output driver circuit with improved slew rate and output impedance control.

Fig.8



Example 2.1
(Combination of Itoh Embodiments 2 and 4)

As shown in Example 2.1, Itoh describes a main driver including circuits 22 and 42 with pairs of p-channel MOS transistor and n-channel MOS transistors for driving a load according to VIN by providing a VOUT. It was well-known that an output driver circuit generates an output signal (e.g., VOUT) that drives an external load. *See, e.g., EX1008, 1:51-53.*

Specifically, the main driver includes circuit 22, which includes a pair of a

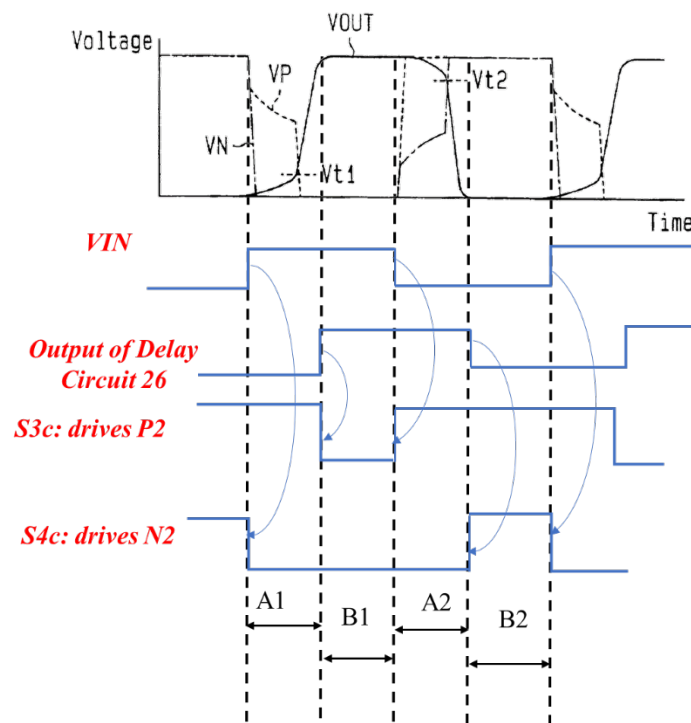
first p-channel MOS transistor (transistor T1 in Fig. 8, annotated in green above as P1) and a first n-channel MOS transistor (transistor T2 in Fig. 8, annotated in green as N1) for driving a load at output VOUT according to the input data VIN. Specifically, P1 and N1 are controlled by VP and VN to achieved desired rising/falling times. EX1006, 12:48-13:62.

The main driver further includes circuit 42, which includes a pair of a second p-channel MOS transistor (transistor T3c in Fig. 8, annotated in blue above as P2) and a second n-channel MOS transistor (transistor T4c in Fig. 8, annotated in blue above as N2). This pair of P2 and N2 works together with the pair of P1 and N2 for generating the VOUT for driving the load, and as such, drives the load in coaction with the pair of P1 and N1. EX1006, 10:1-15; 10:37-42.

The waveforms of Example 2.1⁴ below illustrate the details of how the pair of P2 and N2 (driven by signals S3c and S4c) drives the load in coaction with the pair of P1 and N1. Specifically, P2 and N2 are turned off during periods A1 and A2, during which period P1 and N1 are controlled by VP and VN (generated based on VOUT) for slew rate control. During B1 and B2 when VOUT is substantially stable, P2 and N2 are turned on for output impedance control. Each of VP, VN, S3c, and S4c for controlling P1, N1, P2, N2 are generated based on both VIN and

⁴ Illustrating the case where P2 and N2 are selected.

VOUT.



**Waveforms of Example 2.1
(Annotated using EX1006, FIG. 11)**

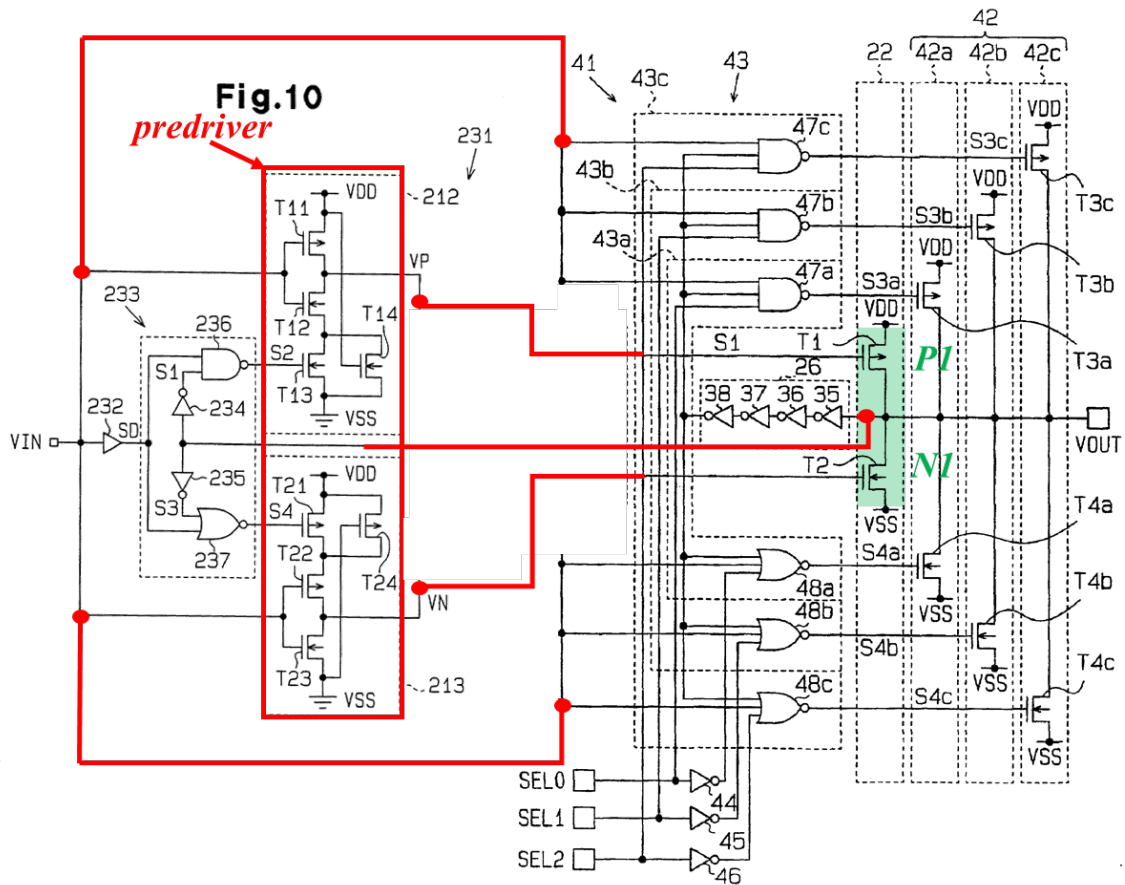
Therefore, Itoh teaches this element.

[1.2.1] a predriver with outputs for driving only said first n-channel MOS transistor [N1] and only said first p-channel MOS transistor [P1]

Itoh teaches this element. EX1003, ¶¶189-192.

Continuing with Example 2.1 as illustrated below, Itoh teaches a predriver (circuits 212 and 213) positioned before the main driver (circuits 22 and 42), and provides signals VP and VN for driving only P1 and only N1 in the main driver.

Fig.8



Example 2.1
(Combination of Itoh Embodiments 2 and 4)

Referring to FIG. 10, Itoh describes a predriver (including circuits 212 and 213) with outputs (VP and VN) for driving only a first in-channel p-channel MOS transistor (T1) and only a first n-channel MOS transistor (T2). EX1006, 11:11-20. As shown in Example 2.1, in the combination, these functions remain the same, where the predriver's output (VP and VN) is for driving only said first n-channel MOS transistor (T1 annotated as P1) and only said first p-channel MOS transistor

(T2 annotated as P2) of the main driver.

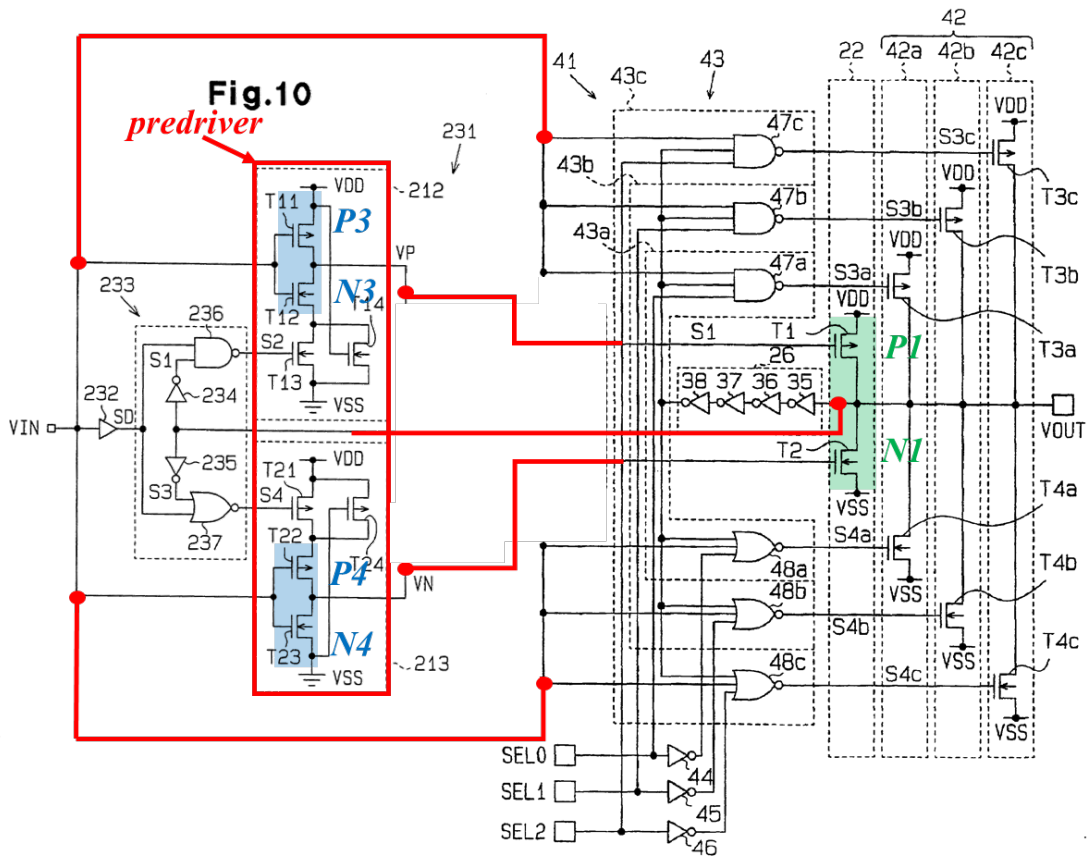
Therefore, Itoh teaches this limitation.

[1.2.2] [the predriver] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data,

Itoh teaches this element. EX1003, ¶¶193-196.

Continuing with Example 2.1 as illustrated below, Itoh discloses a predriver (circuits 212 and 213), where circuit 212 includes at least a pair of a third p-channel MOS transistor (T11 annotated as P3) and a third n-channel MOS transistor (T12 annotated as N3) for driving P1 according to said data (VIN). EX1006, 13:24-30.

Fig.8



Example 2.1
(Combination of Itoh Embodiments 2 and 4)

Further, circuit 213 of the predriver includes has at least a pair of a fourth p-channel MOS transistor (T22 annotated as P4) and a fourth n-channel MOS transistor (T23 annotated as N4) for generating VN, which drives N1 according to said data (VIN). EX1006, 12:50-56.

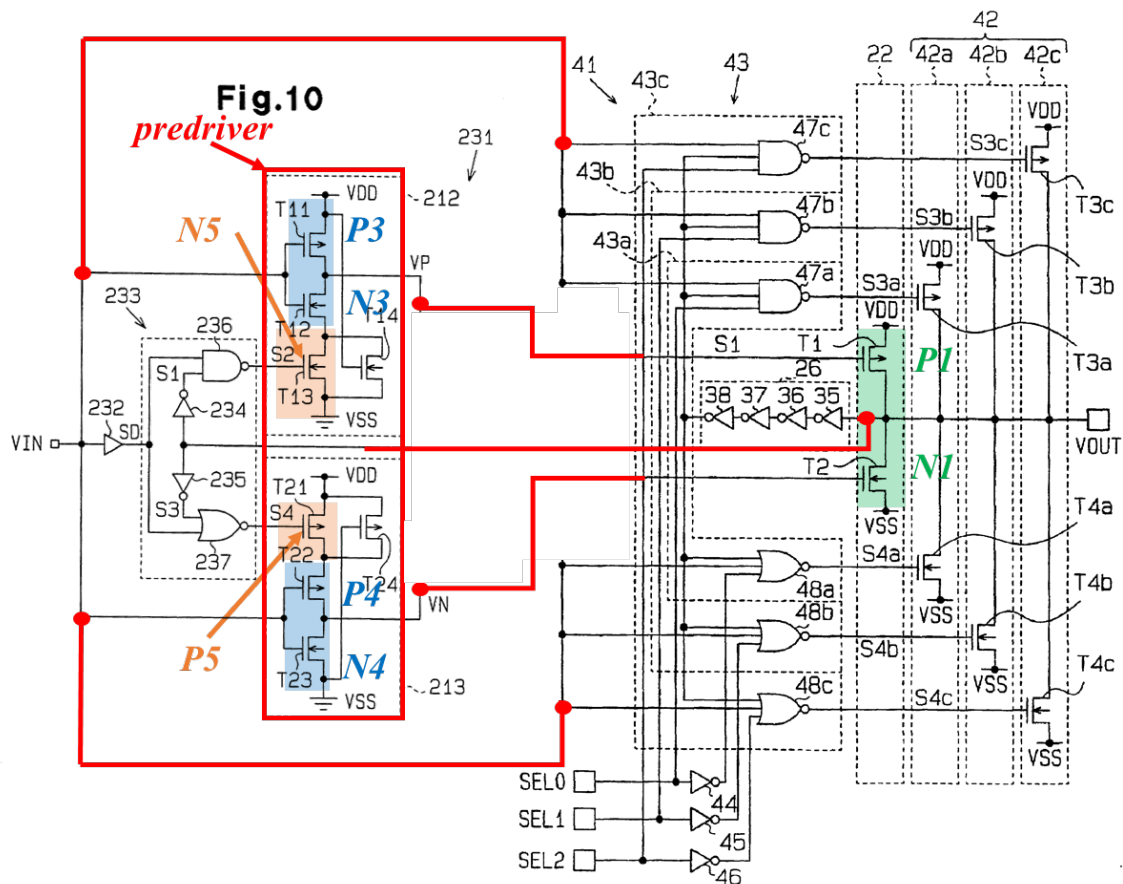
Therefore, Itoh teaches this element.

[1.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]; and

Itoh teaches this element. EX1003, ¶¶193-197.

Continuing with Example 2.1 as illustrated below, predriver's circuit 212 includes at least one fifth n-channel MOS transistor (T13 annotated as N5) for driving said first p-channel MOS transistor (T1 annotated as P1) in coaction with said third n-channel MOS transistor (T12 annotated as N3).

Fig.8



Example 2.1

(Combination of Itoh Embodiments 2 and 4)

Specifically, N5 and N3 are connected in series and work together to generate VP (e.g., working together to control how fast VP rises and falls), where VP drives P1. EX1006, 11:51-12:4.

Similarly, circuit 213 of the predriver includes at least one fifth p-channel MOS transistor (T21 annotated as P5) for driving said first n-channel MOS transistor (T2 annotated as N1) in coaction with said fourth p-channel MOS transistor (T22 annotated as P4). Specifically, P5 and P4 are connected in series and work together to generate VN (e.g., working together to control how fast VN rises and falls), which drives N1. EX1006, 12:28-47 (explaining turning on and off T21 to control the rising and falling edges of VOUT).

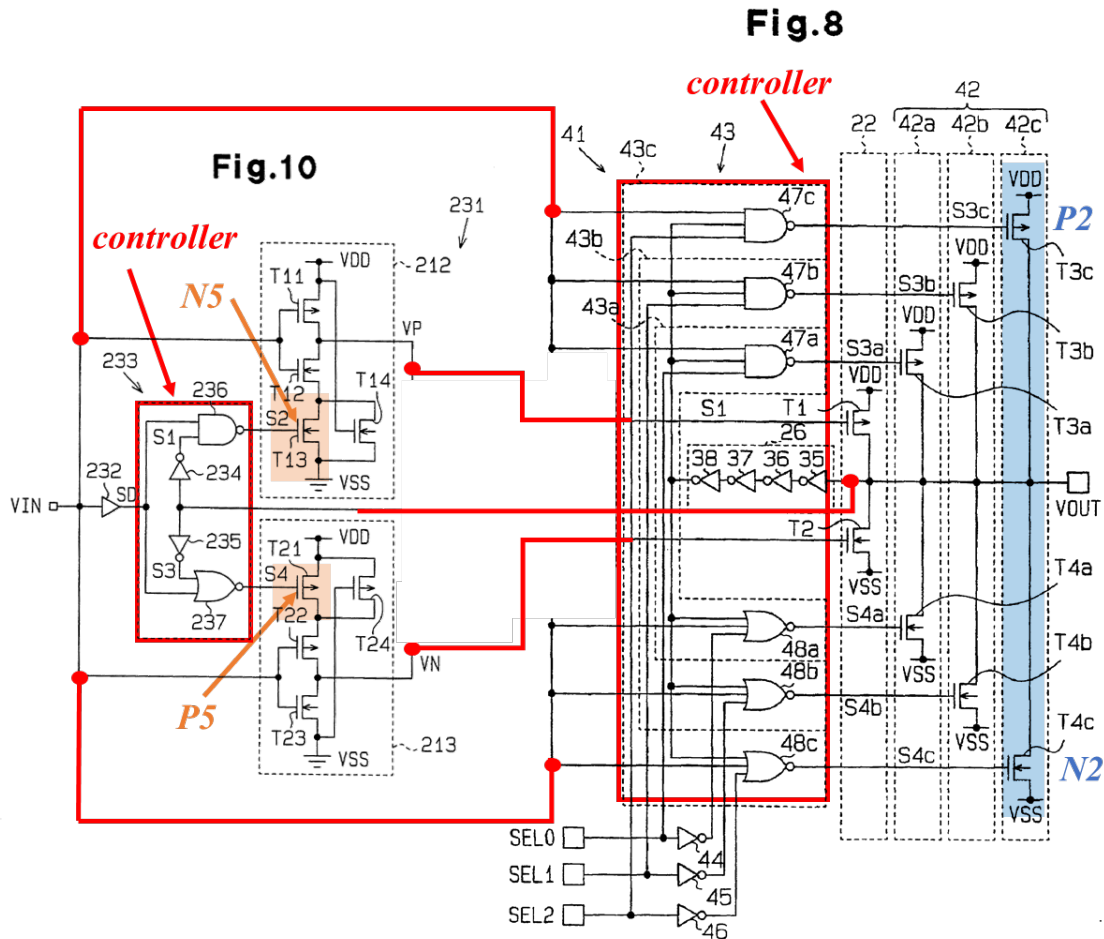
Therefore, Itoh teaches this element.

[1.3] a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2],

Itoh teaches this element. EX1003, ¶¶202-205.

Continuing with Example 2.1 as illustrated below, a controller (including signal generator 233 of FIG. 10 and control circuits 26 and 43 of FIG. 8) receives VOUT as a feedback signal and VIN, and generates control signals (e.g., S2 for driving N5 in coaction with S3c for driving P2, and S4 for driving P5 in coaction

with S4c for driving N2) based on VOUT and VIN. The delay circuit 26 was a well-known self-timed control circuit for providing a control signal based on the feedback VOUT (which by itself is considered a control signal) by adjusting the number of pairs of inverters.



Example 2.1 (Combination of Itoh Embodiments 2 and 4)

As shown in Example 2.1 illustrated above, a controller generates control signals S2 to control said fifth n-channel MOS transistor N5 into and out of operation in coaction with said second p-channel MOS transistor P2, because the

control signal S4 (driving N5 into and out of operation) and control signal S3c (driving P2) are generated using the same feedback VOUT (which itself is also considered a control signal) and VIN, and therefore are in coaction with each other. This configuration of controlling N5 into and out of operation in coaction with P2 is similar to the configuration in the '539 patent. *See, e.g.*, EX1001, FIGS. 3, 4, and 7 (illustrating controlling N5 (e.g., QN17) into and out of operation in coaction with P2 (e.g., QP2) where the control signals for N5 and P2 are each generated using the same signals $\phi 3$ and VIN).

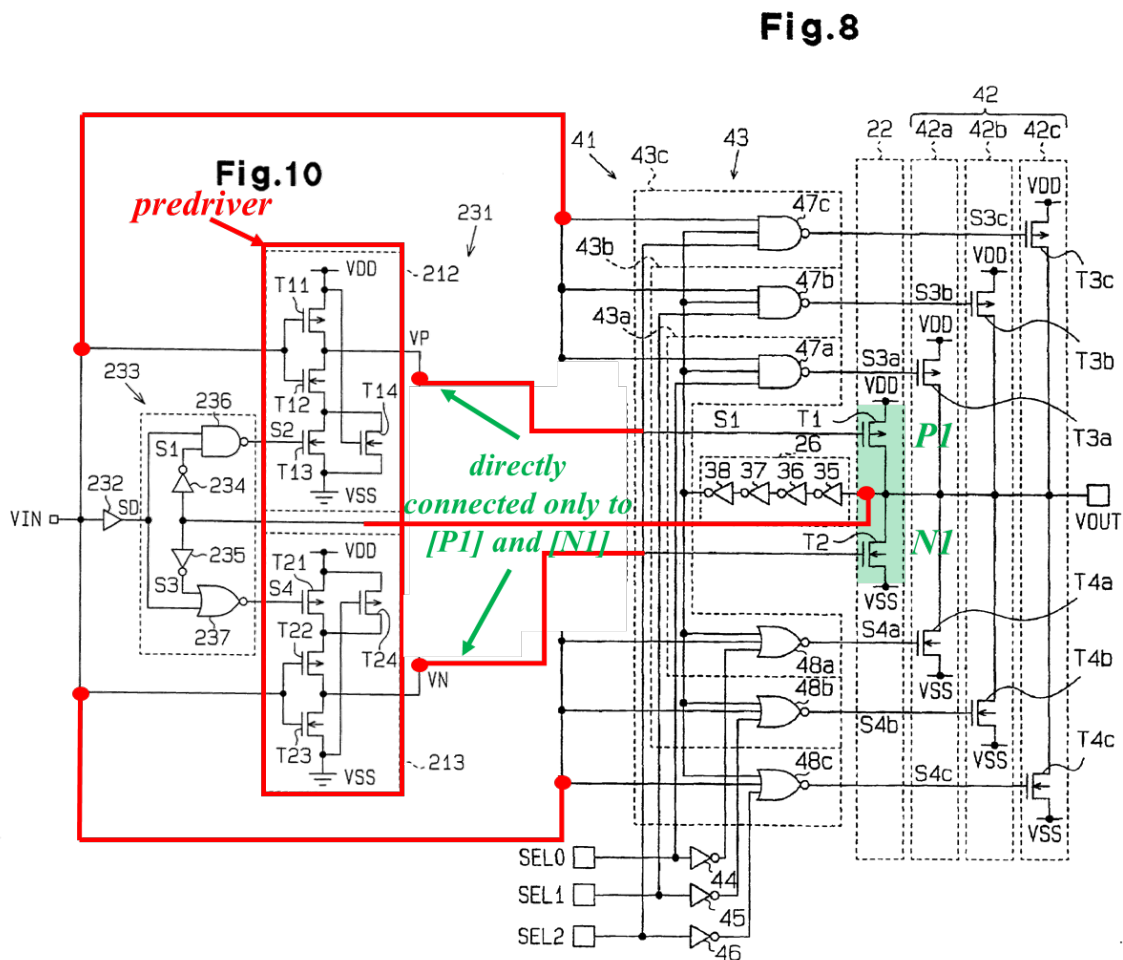
Further, in the combination, the controller generates signal S4 to control P5 into and out of operation in coaction with N2, because the control signal S4 (driving P5) and control signal S4c (driving N2) are generated using the same feedback VOUT (which itself is also considered a control signal) and VIN, and therefore are in coaction with each other. This configuration of controlling P5 into and out of operation in coaction with N2 is similar to the configuration in the '539 patent. *See, e.g.*, EX1001, FIGS. 3, 4, and 7 (illustrating controlling P5 (e.g., QP27) into and out of operation in coaction with N2 (e.g., QN2) where the control signals for P5 and N2 are each generated using the same signals $\phi 6$ and VIN).

Therefore, Itoh teaches this element.

[1.4] wherein the output of the predriver is directly connected only to said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1] of said main driver.

Itoh teaches this element. EX1003, ¶¶207-209.

Continuing with Example 2.1 as illustrated below, Itoh teaches the output (control signals VP and VN) of the predriver (circuits 212 and 213) is directly connected only to said first p-channel MOS transistor (T1 annotated as P1) and said first n-channel MOS transistor (T2 annotated as N1) of said main driver.

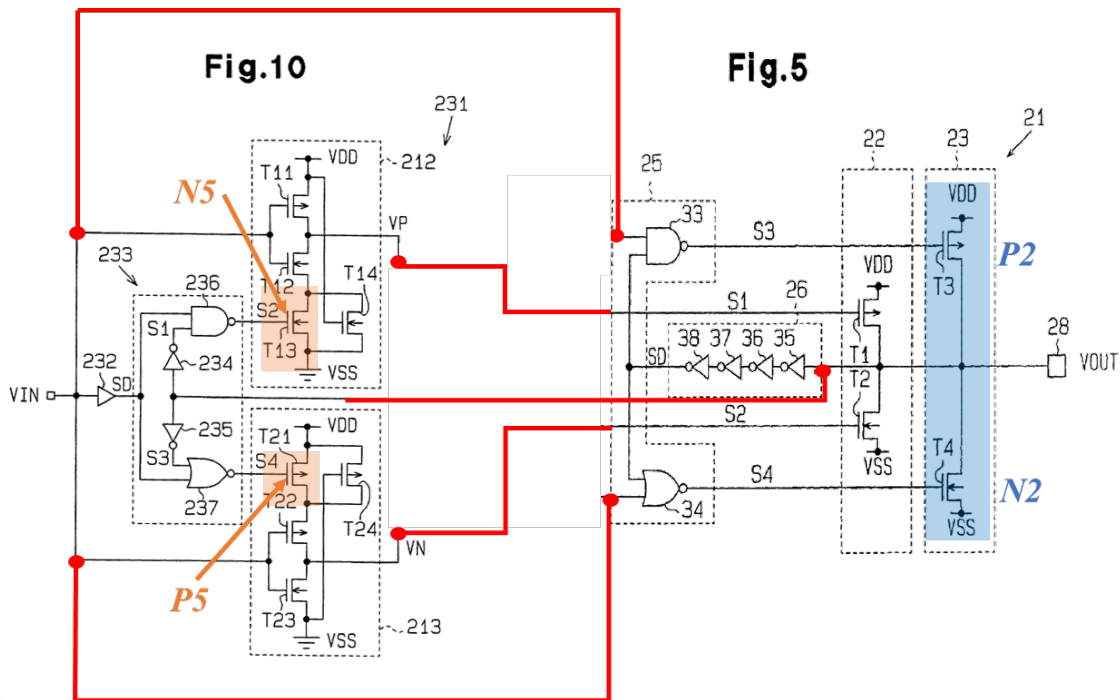


Example 2.1
(Combination of Itoh Embodiments 2 and 4)

3. Claim 2

Itoh teaches this element. EX1003, ¶¶210-212.

Specifically, Example 2.2 (Combination of Embodiments 1 and 4) illustrated below teaches this element. First, Example 2.2 teaches claim 1 for the reasons discussed above at Ground 1:Claim 1. Furthermore, in Example 2.2, the number of P2 and N2 is two, which equals to the number (two) of N5 and P5.



Example 2.2
(Combination of Embodiments 1 and 4 of Itoh)

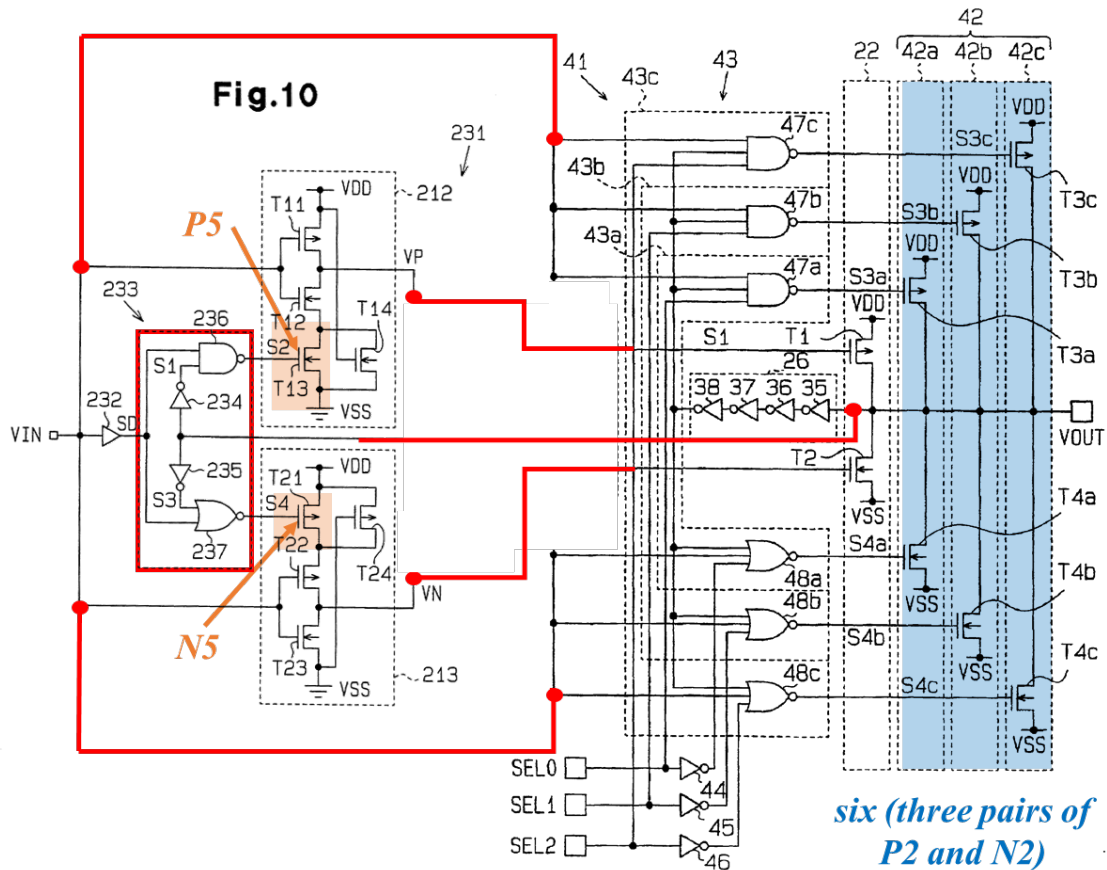
4. Claim 3

Itoh teaches this element. EX1003, ¶¶213-215.

Specifically, as shown in the Example 2.1 below, the number (6) of P2 (T3a, T3b, and T3c) and N2 (T4a, T4b, and T4c) is different from the number (2) of N5

(T21) and P5 (T13).

Fig.8



Example 2.1
(Combination of Itoh Embodiments 2 and 4)

5. Claim 4

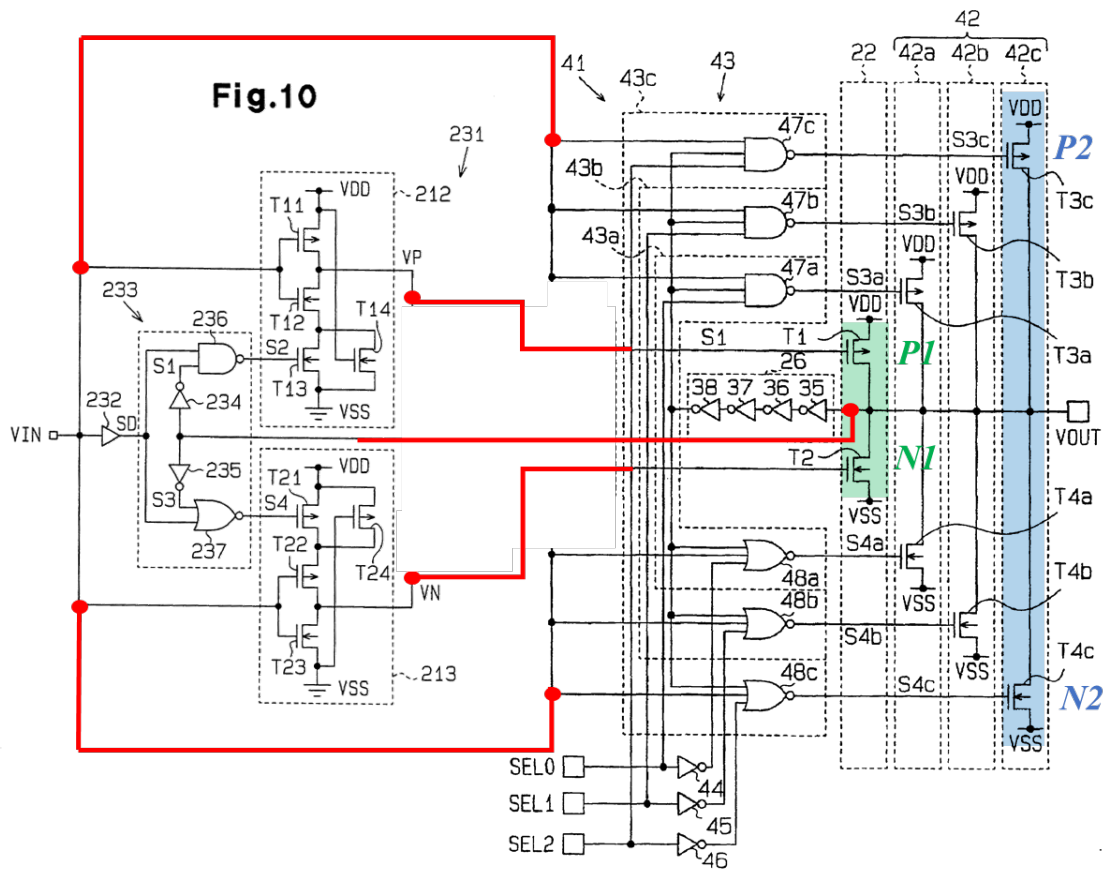
[4.0] The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor [P2] and said second n-channel MOS transistor [N2] have a smaller device size with a smaller gate width than said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1], and have a small effect on rise and fall times of pulses output from said main driver.

Itoh teaches this element. EX1003, ¶¶216-222.

Continuing with Example 2.1 as illustrated below, Itoh teaches that T3c and

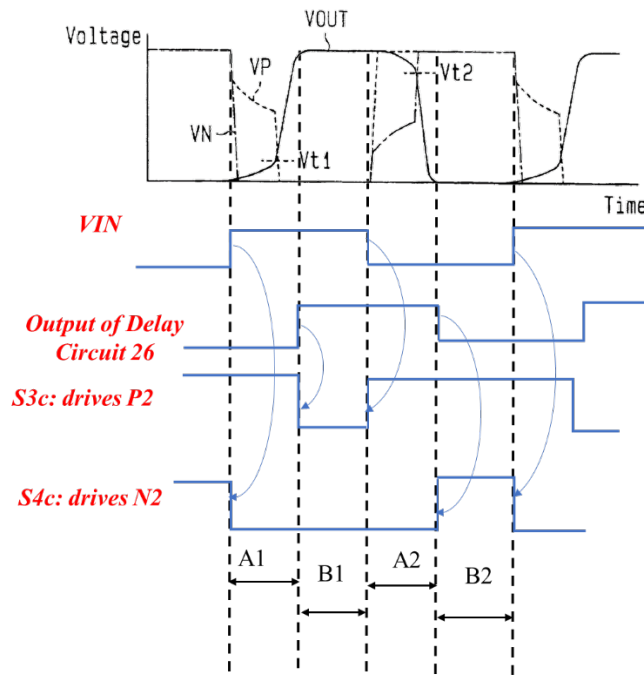
T4c (P2 and N2) have a small effect on rise and fall times of pulses output from said main driver.

Fig.8



Example 2.1
(Combination of Itoh Embodiments 2 and 4)

As shown in the waveforms of Example 2.1 below, during A1 and A2 where the slew rate is controlled, P2 and N2 are turned off (by control signals S3c and S4c), and as such, have small effect on rise and fall times of VOUT.



Waveforms of Example 2.1
(Annotated using EX1006, Itoh, FIG. 11)

Further, Example 2.1 teaches that P2 and N2 have a smaller device size with a smaller gate width than P1 and N1. In the Example 2.1, second-drive circuit 42 include a plurality of pairs of P2 and N2 each having different impedances and are selectable to for controlling the output impedance. For each pair of P2 and N2 of the second-drive circuit 42, selecting a smaller device size with a smaller gate width than P1 and N1 is one of the two well-known design choices (the other is having a greater size), and a POSITA would have used this design option based on corresponding design needs (e.g., specific contribution by this particular pair of P2 and N2 to the overall output impedance). *See, e.g.*, EX1008, 5:8-9 (“[The transistors’] relative contribution depends on their sizes.”).

It is noted that the requirement of Embodiment 1 (FIG. 5) of Itoh that T1 and T2 have a higher impedance characteristic than T3 and T4 does not apply to Example 2.1, because unlike FIG. 5, circuit 42 of FIG. 8 uses a plurality of pairs of P2 and N2, and further, in the combination, T1 (annotated as P1) and T2 (annotated as N1) are controlled using a different method for slew rate control by the slew rate control circuit of FIG. 10, and as such, no longer needs the size requirement of Embodiment 1 for slow rate control.

Therefore, Itoh teaches the limitation.

6. Claim 5

The analysis for claim 5 relies on the same analysis and evidence as provided for claim 1, except for the differences provided below. Specifically, in the analysis for claim 5 below, the predriver includes circuits 212, 213, 236, and 237 (while in Ground 2: Claim 1, the predriver does not include circuits 236 and 237), and the controller includes circuits 234, 235, 43, and 26 (while in Ground 2: Claim 1, the controller includes circuits 233, 43, and 26). EX1003, ¶¶219-254.

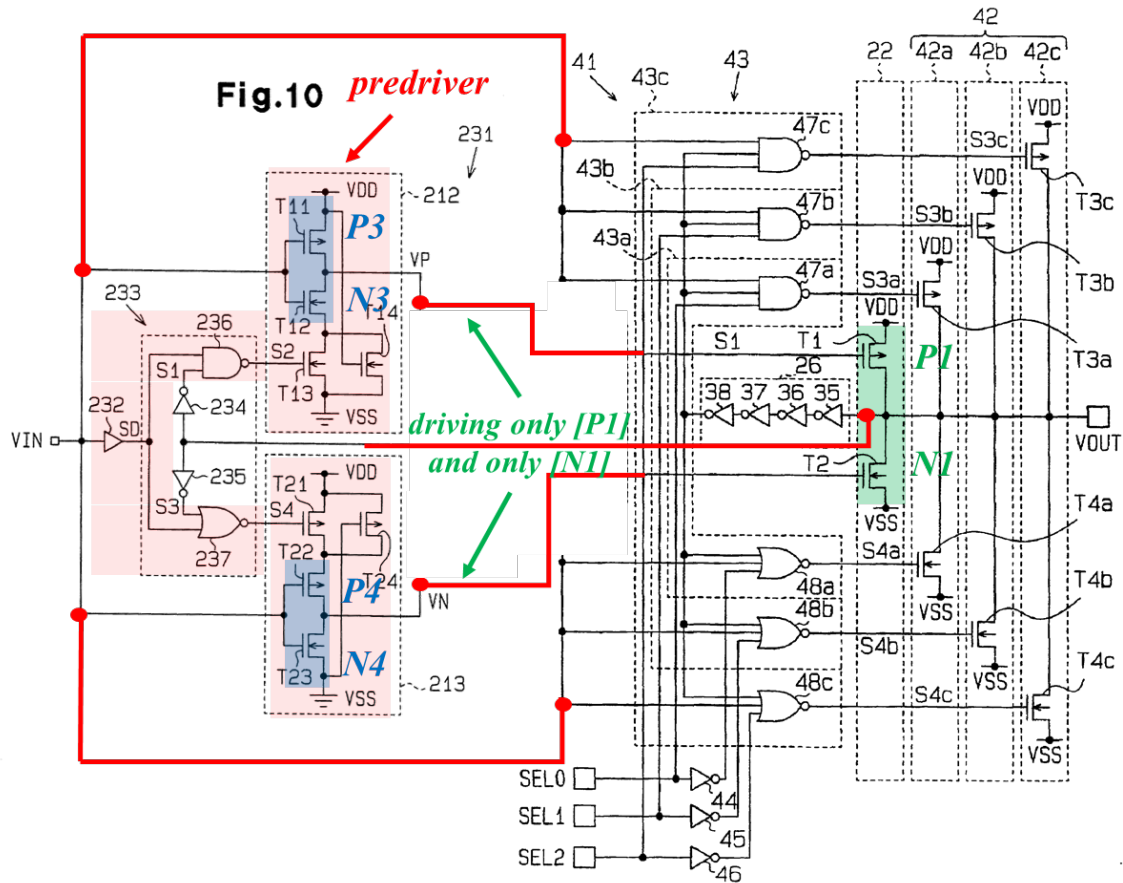
[5.0]/[5.2.2]

Itoh teaches these element for the reasons discussed at Ground 2:[1.0]-[1.2.2]. EX1003, ¶¶224-232.

For [5.2.1] and [5.2.2], while the mapping for predriver includes additional circuits 236 and 237, such difference does not change the analysis as provided in

Ground 2:[1.2.1] and [1.2.2].

Fig.8



Example 2.1
(Combination of Itoh Embodiments 2 and 4)

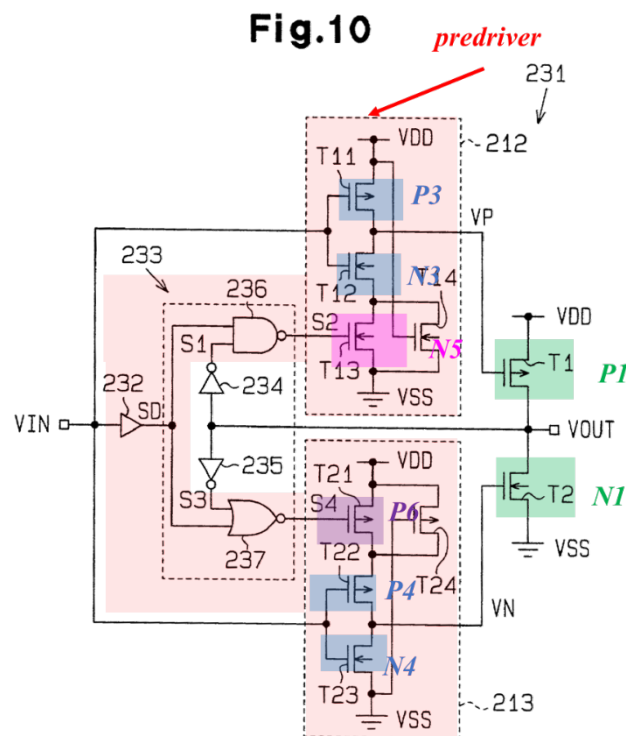
[5.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3],

Itoh in view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element. EX1003, ¶¶233-240.

Continuing with Example 2.1, the combination of Embodiments 2 and 4 in

view of a POSITA's general knowledge teaches this element. For simplicity and clarity, only FIG. 10 as implemented in Example 2.1 is illustrated below, and the analysis applies to Example 2.1.

First, as discussed above at Ground 2:[1.2.3] and as shown in annotated FIG. 10 of Itoh below, Example 2.1 includes a predriver (pink area including circuits 212, 213, 236, and 237), which includes N5 for driving for driving T1/P1 in coaction with N3, by working together to generate a signal VP for driving T1/P1.



EX1006, Itoh, FIG. 10, annotated

Second, it is important to understand the basic, fundamental knowledge of a

POSITA. For example, it is fundamental that in CMOS process as used in Itoh, basic implementation of logic gates including NAND gates and NOR gates include at least a pair of PMOS transistor and NMOS transistor. *See* EX1009, FIGS. 5, 6, and 7.

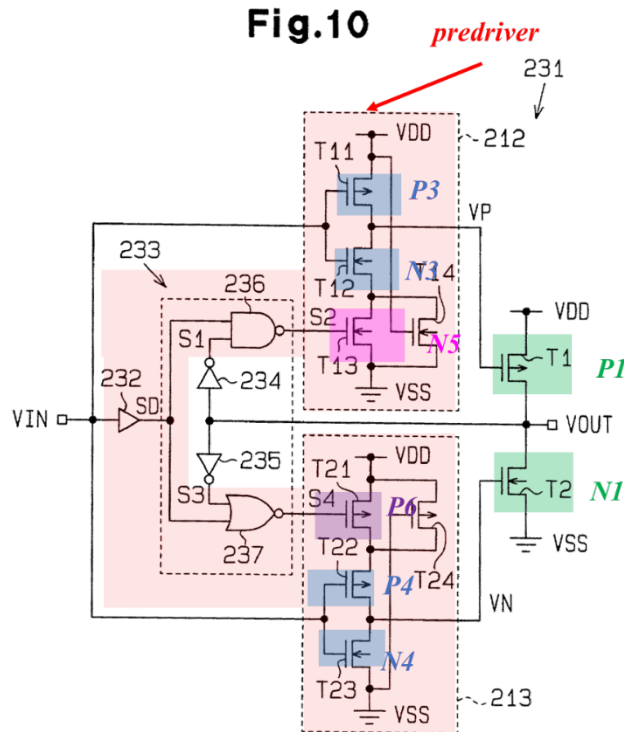
As such, the NAND gate 236 of the predriver in Example 2.1 would have been implemented using at least one PMOS transistor, which teaches the fifth p-channel MOS transistor [P5] as claimed.

The figure below illustrates the CMOS implementation of NAND gate 236, where FIG. 7B of Skorup is used as an example to illustrate the fundamental knowledge that the basic CMOS implementation of NAND gate includes at least a PMOS transistor.

[5.2.4] [the predriver having] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]; and

Itoh in view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element. EX1003, ¶¶241-247.

First, as shown in annotated FIG. 10 of Itoh below, the predriver (pink area including circuits 212, 213, 236, and 237) includes at least one sixth p-channel MOS transistor T21 (annotated as P6) for driving T2 (annotated N1) in coaction with said fourth p-channel MOS transistor T22 (annotated as P4), by working together to generate a signal VN for driving T2/N1. Specifically, P6 and P4 are connected in series and work together to generate VN (e.g., working together to control how fast VN rises and falls), which drives N1. EX1006, 12:28-47 (describing the operation of T21/P5).



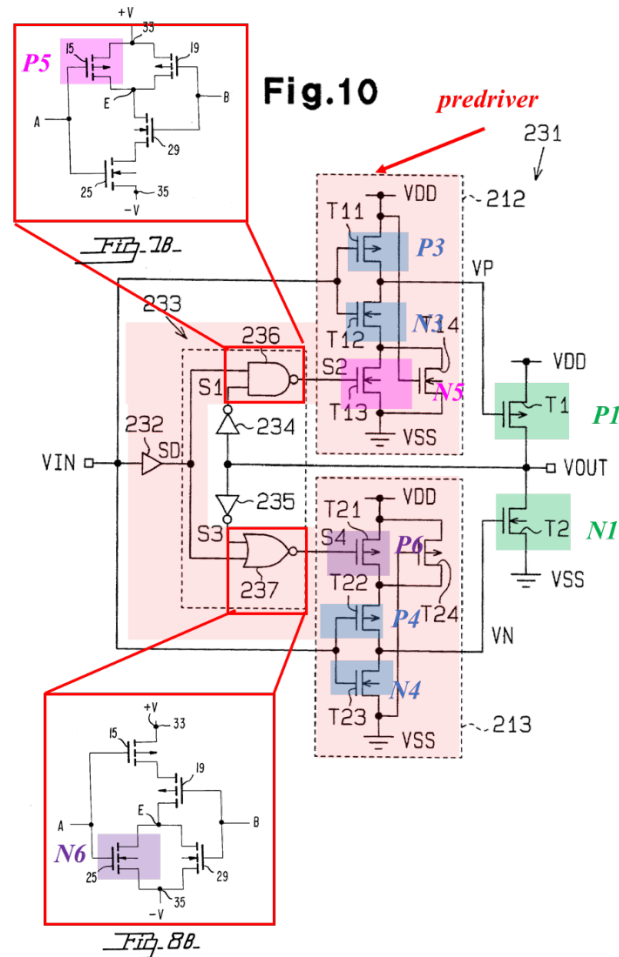
EX1006, FIG. 10, annotated

Second, it is important to understand the basic, fundamental knowledge of a POSITA. For example, it is fundamental that in CMOS process as used in Itoh, basic implementation of logic gates (e.g., NAND or NOR gates) include at least a pair of PMOS transistor and NMOS transistor.

As such the NOR gate 237 of the predriver in Example 2.1 would have been implemented using at least one NMOS transistor, which teaches the fifth n-channel MOS transistor [N5] as claimed.

The figure below illustrates the CMOS implementation of NAND gate 236, where FIG. 8B of Skorup is used as an example to illustrate the fundamental

knowledge that the basic CMOS implementation of NOR gate includes at least a NMOS transistor.



EX1006, FIG. 10, annotated

With such implementation, Example 2.1 teaches that the predriver includes one sixth p-channel MOS transistor (e.g., EX1007, FIG. 8B, 25, annotated as P6) for driving said second p-channel MOS transistor (T2/P2) in coaction with the fourth n-channel MOS transistor (T23, annotated as N4). Specifically, N6 is turned on and off by control signal S3 (which is a delayed inverted VOUT), which

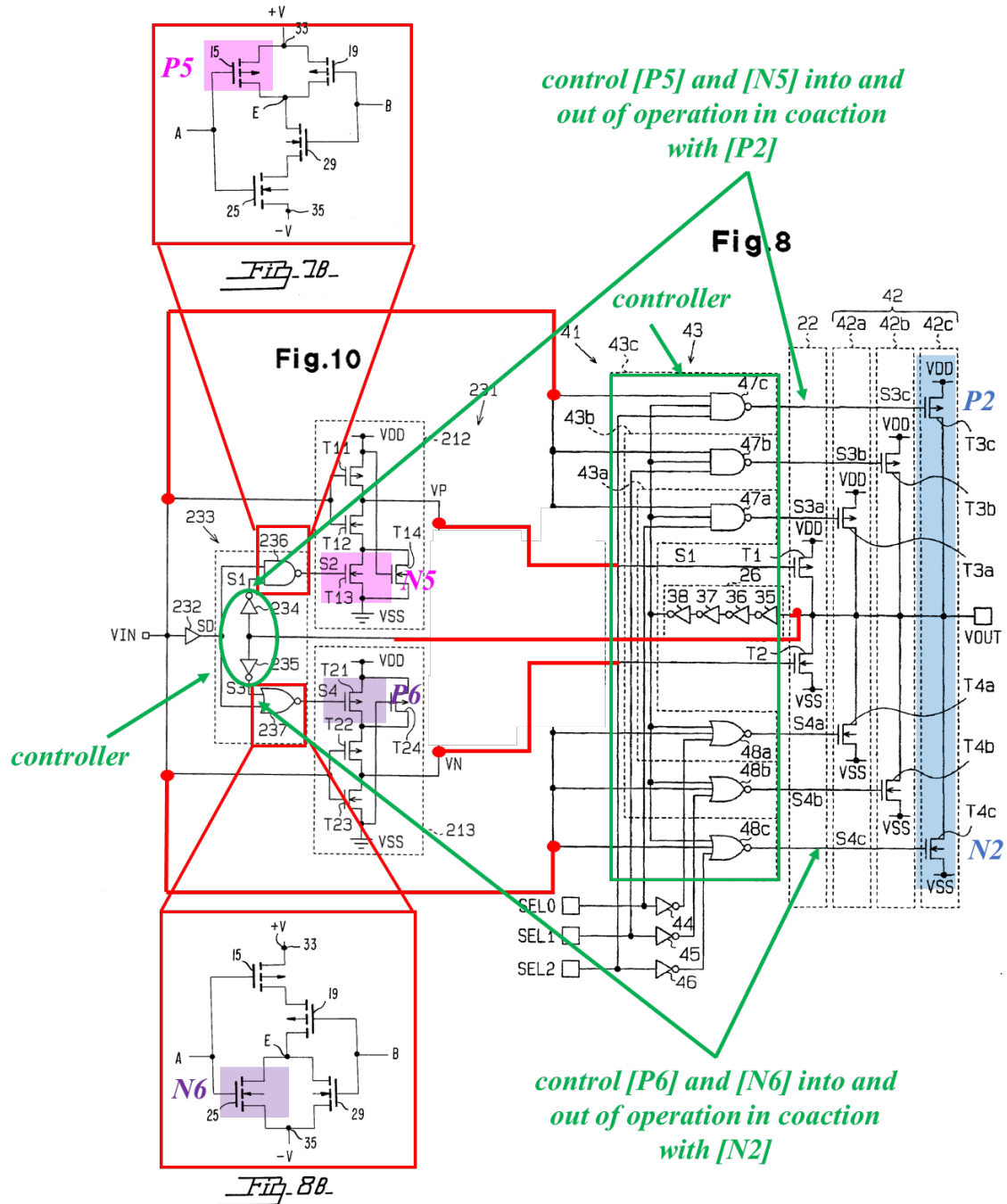
in turn determines S4 that controls P6. P6 connects in series with N4 and works in coaction to generate VP for controlling N1. As such, in Example 2.1, N6 and N4 work in coaction to generate the control signal for N1.

Accordingly, Itoh in view of a POSITA's general knowledge of basic transistors and logic design renders obvious this element.

[5.3] a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2],

Itoh in view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element. EX1003, ¶¶248-255.

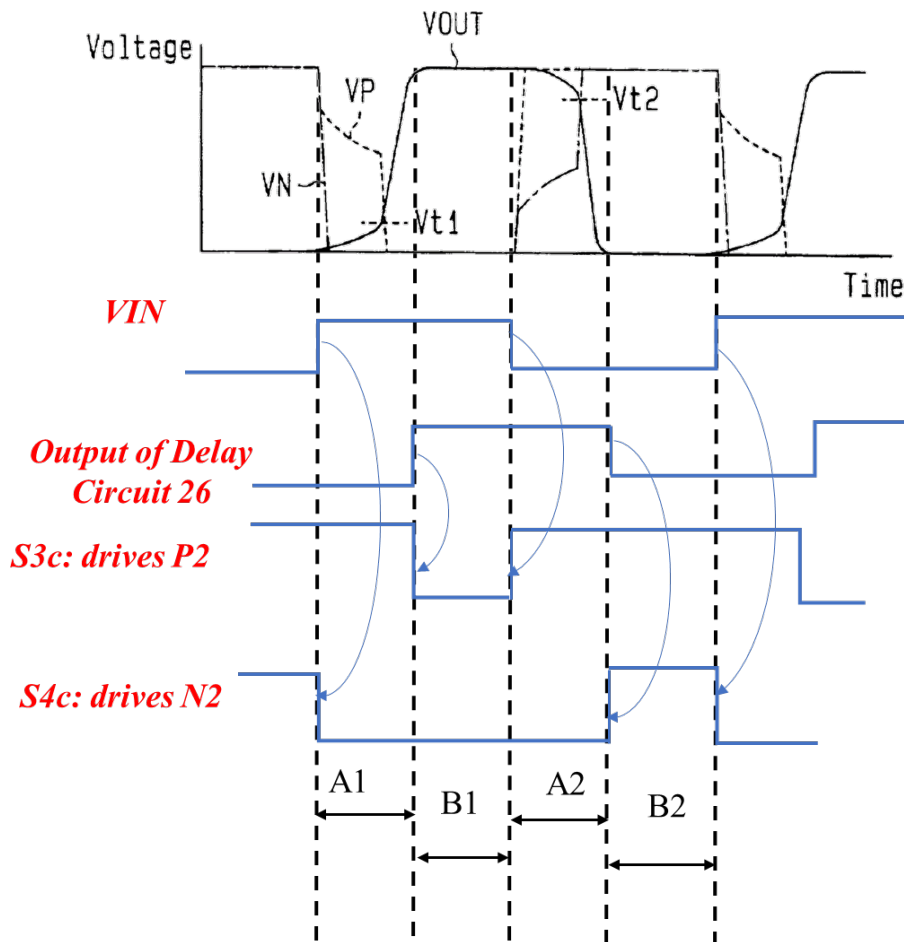
Continuing with Example 2.1, the combination of Embodiments 2 and 4 teaches this element. As shown in Example 2.1 as illustrated below, the combination teaches a controller (including circuits 234, 235, 43, and 26) for generating control signals (including S1, S3, S3c, and S4c). S1 is used to drive P5, S3 is used to drive N6, S3c is used to drive P2, and S4c is used to drive N2.



Example 2.1 (Combination of Itoh Embodiments 2 and 4)

In Example 2.1 with the CMOS implementation of NAND and NOR gates, a POSITA would have been motivated to supply S1 (the output of controller 234) to

the gate of P5 (e.g., through terminal A of FIG. 7B of Skorup), which controls said fifth p-channel MOS transistor (PMOS transistor 15 annotated as P5) and fifth n-channel MOS transistor (NMOS transistor 13 annotated as N5 controlled by control signal S2) into and out of operation in coaction with said second p-channel MOS transistor P2, because S1 (controlled by VOUT and used to generate VP through S2) and S3c (also controlled by VOUT and used to control P2) work in coaction, as shown in the waveforms of Example 2.1 below.



Waveforms of Example 2.1

(Annotated using EX1006, FIG. 11)

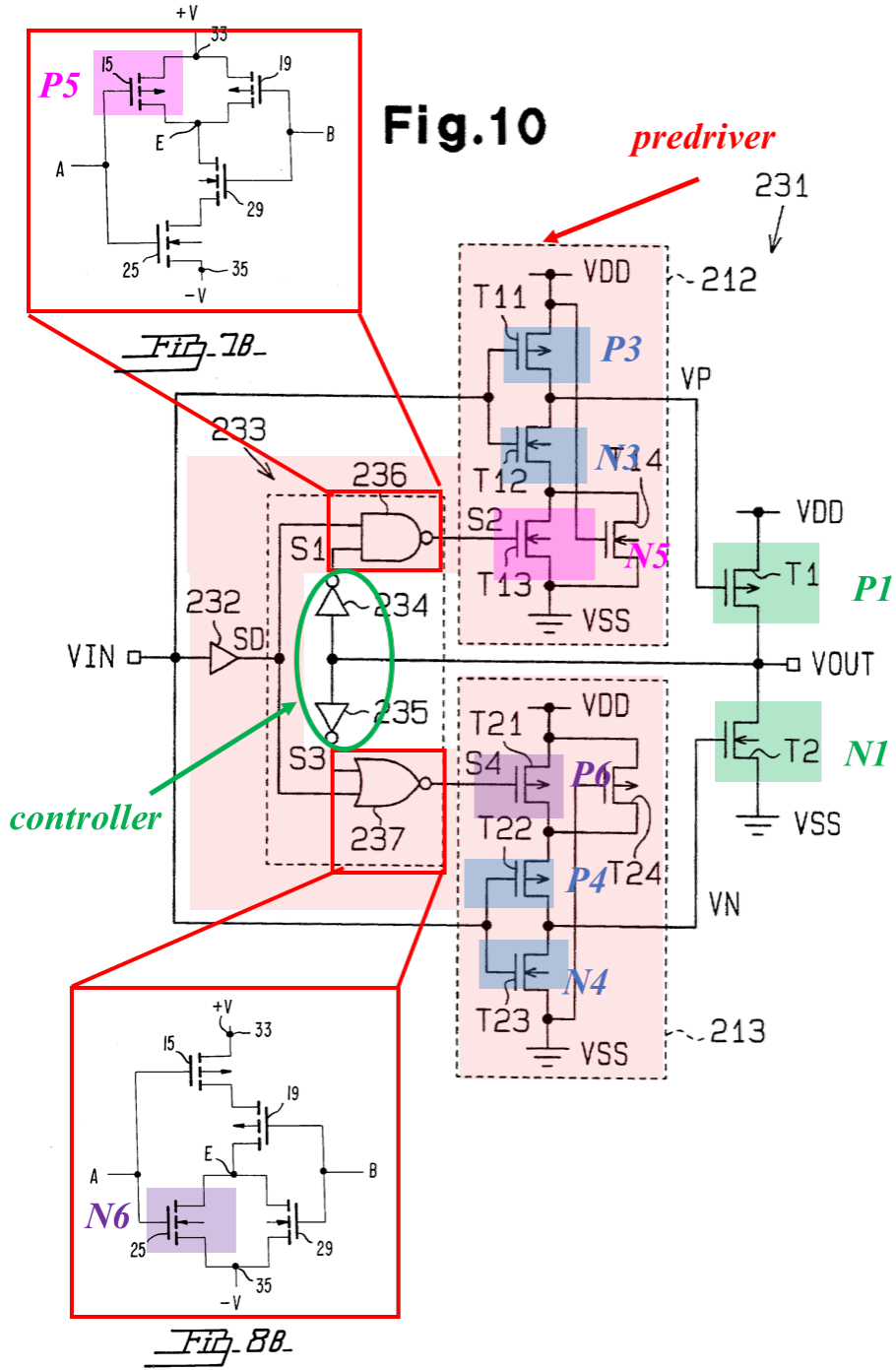
Referring to FIG. 10, Itoh explains that the inverter circuit 234 is used to generate the switching control signal S2 (by turning P5 in and out of operation), which determines VP, and sequentially controlling VOUT. S1 with P5 is used to control the slew rate during A1, while P1 works in coaction and is only turned on during B1 for output impedance control. EX1006, Itoh, 13:15-23. As shown in the waveforms illustrated above, P2 is also controlled by S3c that determined by VOUT (through delay circuit 26).

As such, in the combination, P5 and N5 is controlled into and out of operation in coaction with P2, because P5, N5, and P2 are controlled using signals both generated based on the same VIN and feedback input VOUT signal. This configuration is similar to the configurations in the '539 patent. *See, e.g.*, EX1001, FIG. 7 (illustrating controlling P5 (QP36) into and out of operation in coaction with P2 (e.g., QP2) where the control signals for P5 and P2 are each generated using the same signals ϕ_3 and VIN.

Further, in the combination, a POSITA would have been motivated to supply S3 (the output of controller 235) to terminal A of FIG. 8B of Skorup, which controls said sixth n-channel MOS transistor (NMOS transistor 25 annotated as N6) and P6 into and out of operation in coaction with said second n-channel MOS transistor N2, because S2 (controlled by VOUT and is used to generate VN) and

S4c (also controlled by VOUT and is used to control N2) work in coaction, as shown in the waveforms of Example 2.1 above. S3 with N6 is used to control the slew rate during A2, while N2 works in coaction and is only turned on during B2 for output impedance control. EX1006, Itoh, 13:56-64 (“When the external output signal VOUT falls to the threshold voltage V_{t2} of the inverter circuit 235 thereafter, the inverted signal from the inverter circuit 235 changes to the H level from the L level and the Switching control signal S4 changes to the L level from the H level. This turns on the PMOS transistor T21. The turned-on PMOS transistor T21 causes the control signal VN to sharply rise to the H level. Accordingly, the external output signal VOUT sharply falls to the L level.”).

As such, in the combination, N6 and P6 are controlled into and out of operation in coaction with N2, because N6, P6, and N2 are controlled using signals both generated based on the same VIN and feedback input VOUT signal. This configuration is similar to the configurations in the '539 patent. *See, e.g.*, EX1001, FIG. 7 (illustrating controlling N6 (e.g., QN36) into and out of operation in coaction with N2 (e.g., QN2) where the control signals for N6 and P2 are each generated using the same signals $\phi 6$ and VIN).



EX1006, Itoh, FIG. 10, annotated

Accordingly, Itoh teaches this limitation.

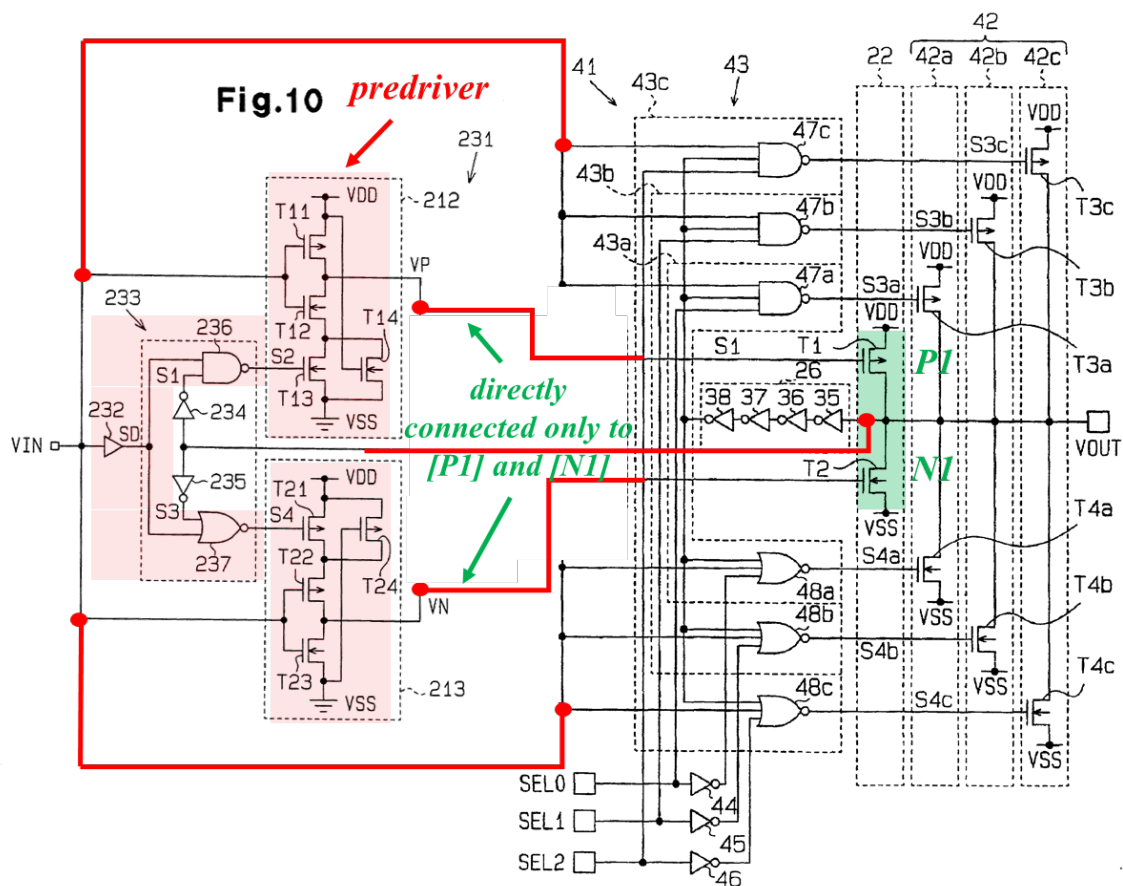
[5.4] wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.

Itoh teaches this element for the reasons discussed at Ground 2:[1.4].

EX1003, ¶¶256-258.

Continuing with Example 2.1 as illustrated below, Itoh teaches the output (control signals VP and VN) of the predriver (circuits 212 and 213) is directly connected only to said first p-channel MOS transistor (T1 annotated as P1) and said first n-channel MOS transistor (T2 annotated as N1) of said main driver.

Fig.8



Example 2.1

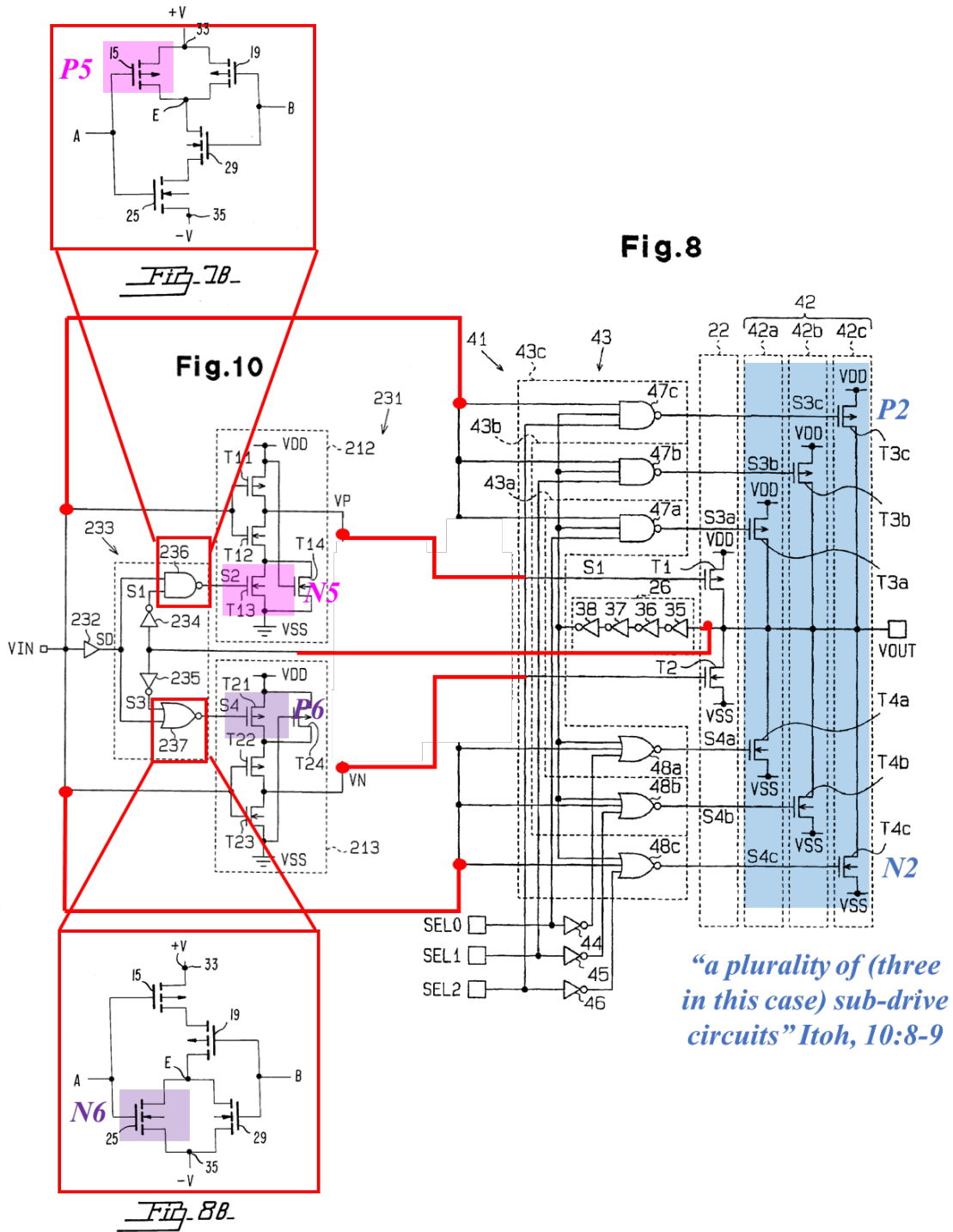
(Combination of Itoh Embodiments 2 and 4)

7. Claim 6

Itoh teaches this element. EX1003, ¶¶259-264.

Continuing with Example 2.1 as illustrated below, the combination of Embodiments 2 and 4 teaches this element.

First, in Example 2.1, the number of N5, P5, N6, and P6 is four.



Example 2.1
(Combination of Itoh Embodiments 2 and 4)

Second, Itoh describes that "[t]he second drive circuit 42 [of FIG. 8]

includes **a plurality of (three in this case)** sub-drive circuits 42a, 42b and 42c.”

EX1006, 10:8-9. As such, in Example 2.1, a POSITA would have been motivated to implement any suitable plurality (including 2) of pairs of P2 and N2 in the second drive circuit 42 based on design needs (e.g., number of selection signals, output impedance configuration requirements, etc.). *See also*, EX1006, 18:3-5.

In the case where circuit 42 is implemented with two pairs of P2 and N2, the number of P2 and N2 is four, which is equal to the number (four) of N5, N6, P5, and P6.

8. Claim 7

Itoh teaches this element. EX1003, ¶¶265-268.

Specifically, as discussed above at Ground 2:[6.0] and as shown in the Example 2.1, second drive circuit 42 of the main driver includes 3 sub-drive circuits 42a, 42b, and 42c, and as such, the number of said second p-channel MOS transistors (T3a, T3b, and T3c annotated as P2) and said second n-channel MOS transistors (T4a, T4b, and T4c, annotated as N2) is six (3+3).

On the other hand, the number of N5, P5, N6, and P6 is four. As such, these numbers are different from each other.

9. Claim 8

Itoh teaches this element for the reasons discussed at Ground 2:[4.0].
EX1003, ¶269.

D. Ground 3: Claims 1-8 are Rendered Obvious under §103(a) over Itoh in view of Muljono.

The analysis for Ground 3 relies on the analysis and evidence as provided for Ground 2, except for where additional analysis is provided below. EX1003, ¶¶270-299.

1. Reasons to Combine Itoh and Muljono

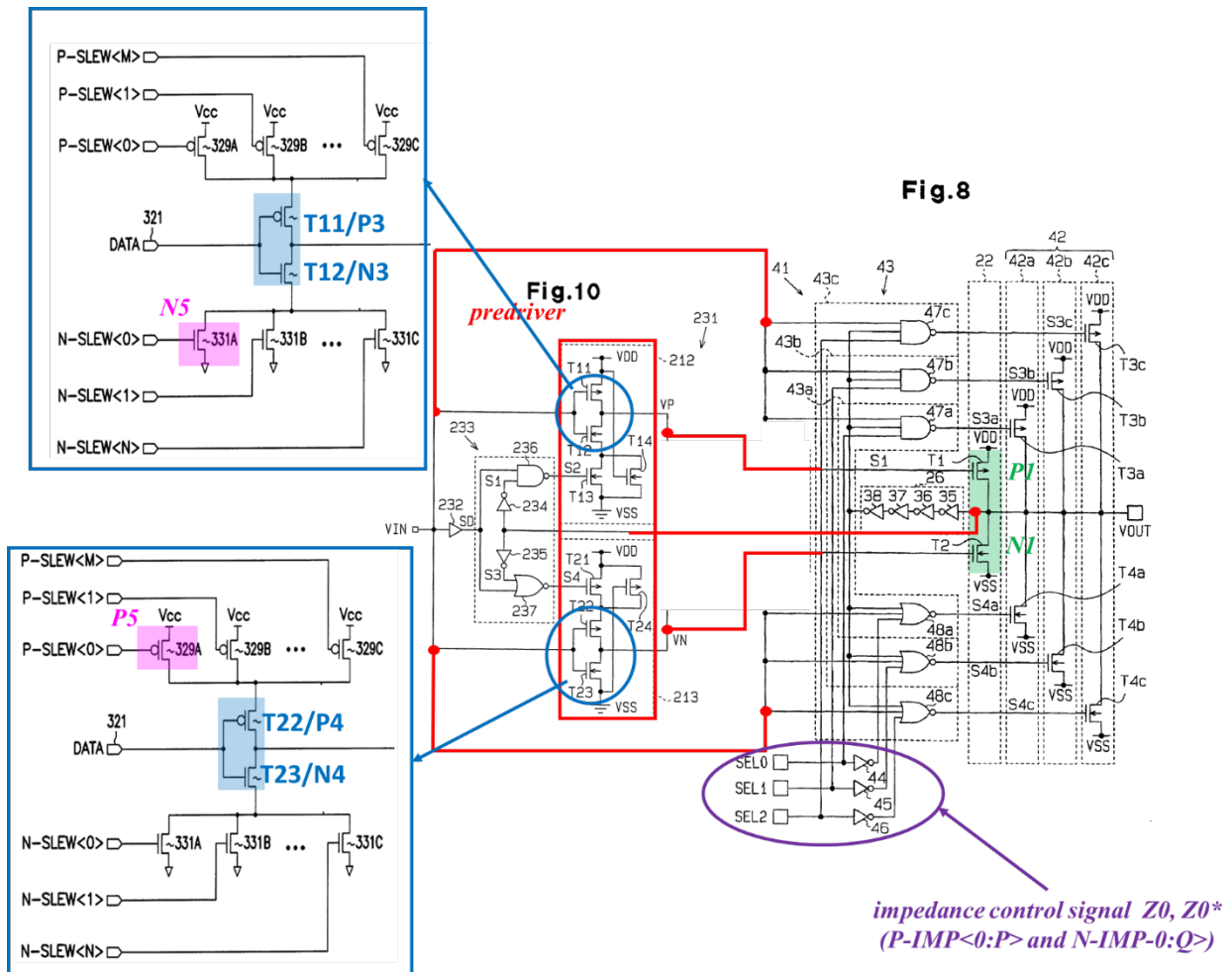
A POSITA would have been motivated to combine Muljono's teaching of a compensation circuit in Itoh to achieve the obvious, beneficial, and predictable results of an output buffer circuit having "an approximately uniform output impedance and slew rate independent of variations in process skew, supply voltage and temperature" as taught by Muljono. EX1010, 2:23-27; EX1003, ¶¶270-275.

First, Itoh and Muljono are analogous art to the '539 patent. *See, e.g.*, EX1001, 1:15-19; EX1006, Title, 1:6-7; EX1010, Abstract.

Second, Itoh and Muljono share the same goal of providing an output buffer circuit that generates an output signal with less variation. EX1006, 14:38-53; EX1010, 2:24-28.

Finally, applying Muljono's teachings in embodiments of Itoh would have been no more than the combination of known elements according to known methods (e.g., incorporating compensations circuits and control signals to the predriver circuit and main driver circuit in an output buffer circuit according to the known IC design steps) obvious to a POSITA.

An example implementation of Example Combination 3.1 (Muljono combined with Example Combination 2.1) is illustrated below.



Example 3.1
(Combination of Example 2.1 (Embodiments 2 and 4 of Itoh) and Muljono)

2. Claim 1

[1.0]-[1.2.2]

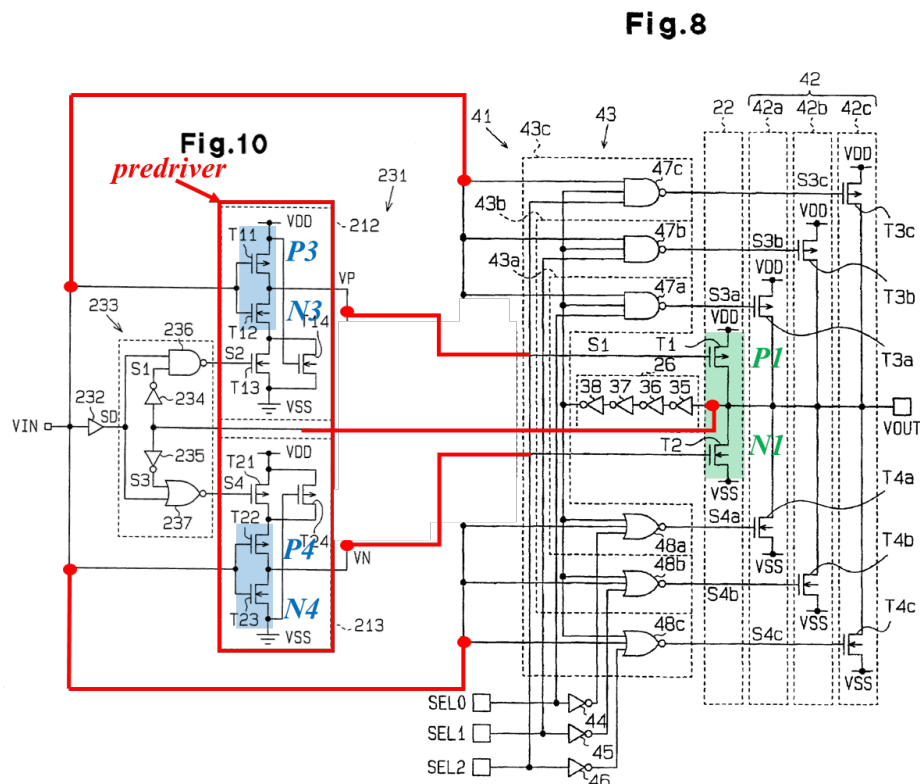
Itō teaches this element for the reasons discussed at Ground 2:[1.0]-[1.2.2].

EX1003, ¶276.

[1.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]; and

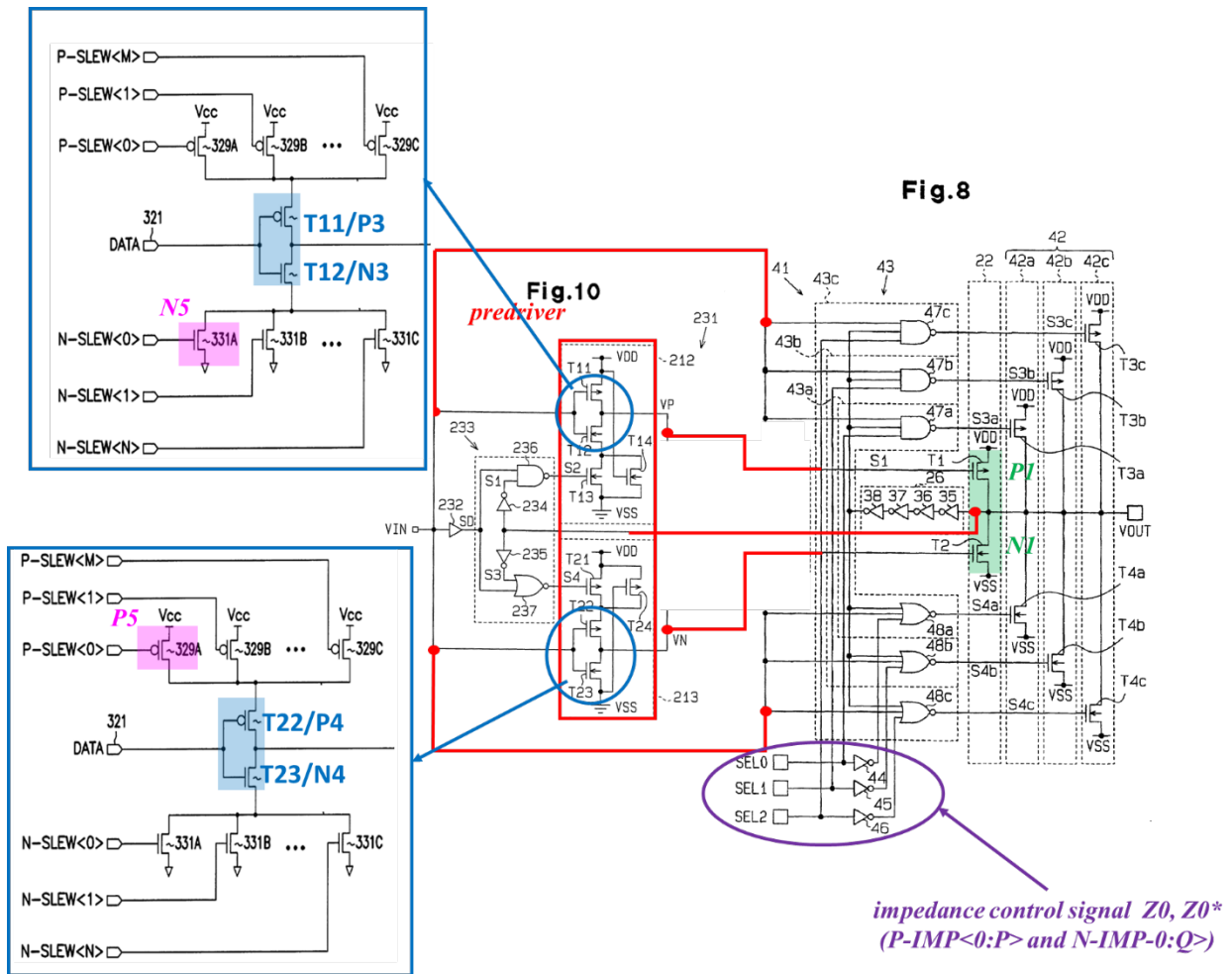
Itoh in view of Muljono renders obvious this element. EX1003, ¶¶278-280.

As shown in Example 2.1 as illustrated below, Example 2.1 teaches an output buffer circuit including a predriver circuit (e.g., circuits 212 and 213) and a main circuit (e.g., circuits 22 and 42). A POSITA would have been motivated to apply the compensation circuit taught by Muljono in Example 2.1 for PVT compensation.



Example 2.1
(Combination of Example Embodiments 2 and 4 of Itoh)

Example Combination 3.1 (Muljono combined with Example 2.1) is provided below, which is referred to as Example 3.1 below. Specifically, a POSITA would have been motivated to, for slew rate control, apply Muljono's slew rate compensation circuit (e.g., EX1010, FIGS. 1, 3) for the inverter pairs with the pairs T11/T12 (P3/N3) and T22/T23 (P4/N4) in FIG. 10 of Itoh, because FIG. 10 of Itoh controls a slew rate of the output signal by controlling slew rates of the control signals VP and VN applied to the output transistors. Further, for output impedance control, it would have been obvious for a POSITA to apply Muljono's impedance control signals (e.g., EX1010, FIGS. 1, 2) to select signals SEL0-SEL2 of FIG. 8, for selecting the sub-driver circuits for output impedance control.



Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

As shown in Example 3.1, circuit 212 of the predriver includes at least one fifth n-channel MOS transistor (331A annotated as N5) for driving said first p-channel MOS transistor (T1 annotated as P1) in coaction with said third n-channel MOS transistor (T12 annotated as N3) for controlling the slew rate. EX1010, 5:67-6:21 (explaining a plurality of n-channel transistors 331A-C coupled in parallel for slew rate control). Specifically, N5 and N3 are connected in series and work together to generate VP, which drives P1.

Similarly, circuit 213 of the predriver includes at least one fifth p-channel MOS transistor (transistor 329A annotated as P5) for driving said first n-channel MOS transistor (T2 annotated as N1) in coaction with said fourth p-channel MOS transistor (T22 annotated as P4). Specifically, P5 and P4 are connected in series and work together to generate VN, which drives N1. EX1010, 5:67-6:21.

Therefore, Itoh in view of Muljono renders obvious this element.

[1.3] a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2],

Itoh in view of Muljono renders obvious this element. EX1003, ¶¶281-283.

First, as discussed at Ground 2:[1.3], Example 2.1 renders this element obvious.

Second, additionally, continuing with Example 3.1, as shown in annotated Muljono FIG. 1 below, Example Combination 3.1 includes a controller (compensation circuit 115 as taught by Muljono) that generates control signals including slew rate control signal impedance control signal, which control the transistors in the pre-driver circuit (including N5 and P5) in coaction with the transistors in the main driver (including N2 and P2).

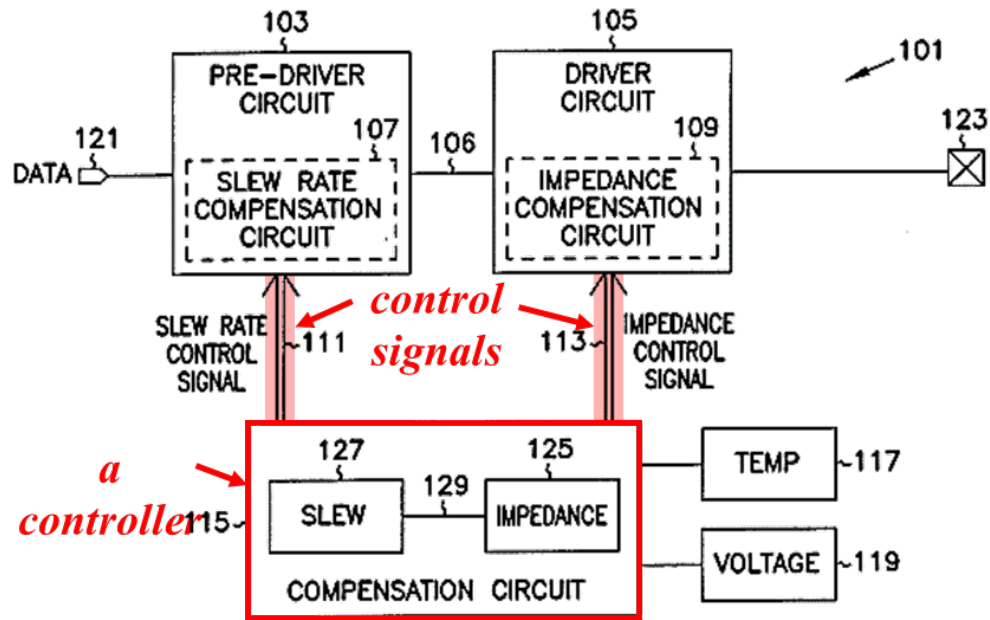
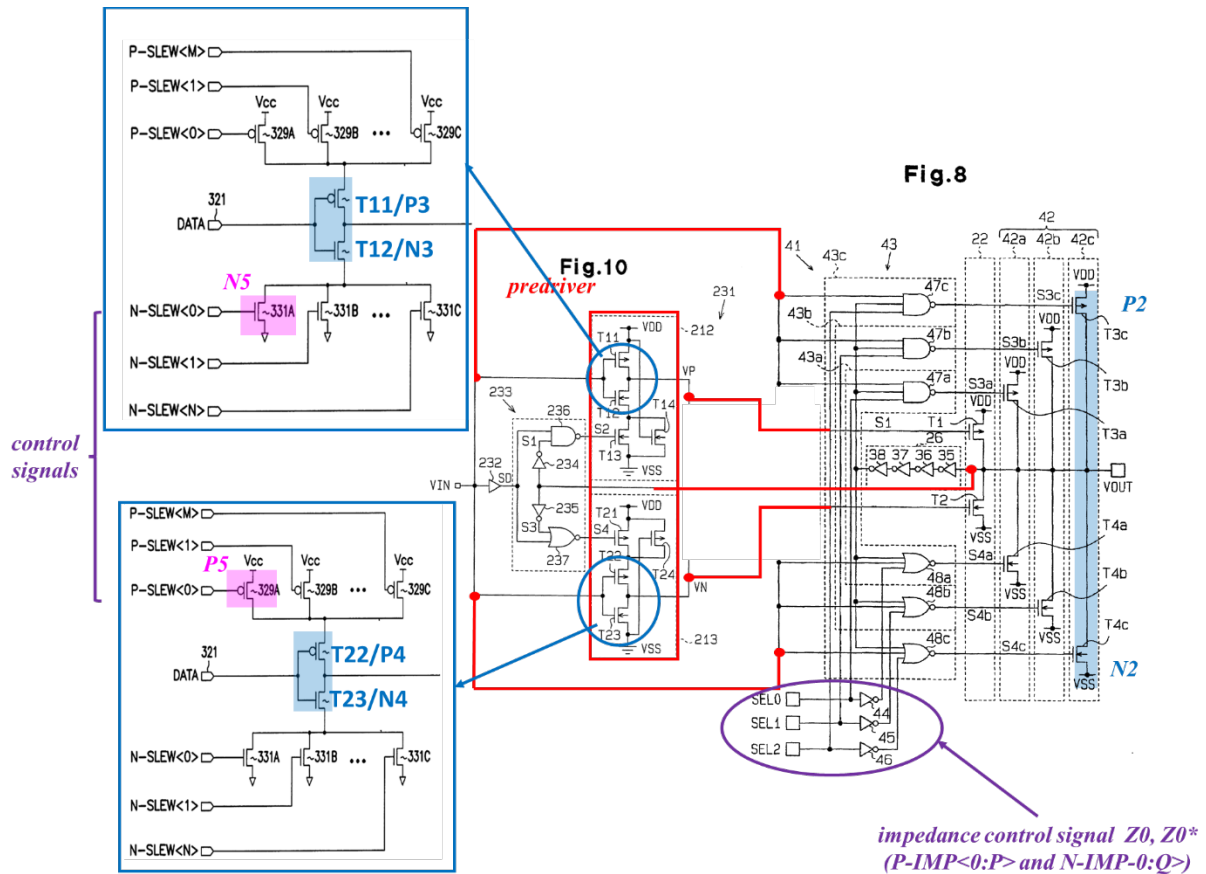


FIG. 1

EX1010, FIG. 1, annotated

As shown in Example 3.1 as illustrated below, the control signals control N5 (using control signal N-SLEW) into and out of operation in coaction with P2 (using control signal P-IMP provided to the SEL0-SEL2), and control P5 (using control signal P-SLEW) into and out of operation in coaction N2 (using control signal P-IMP provided to SEL0-SEL2 and inverter, or directly providing to SEL0-SEL2).



Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

In Example 3.1, N5 is controlled into and out of operation in coaction with P2, because the slew rate control signal for controlling N5 (N-SLEW for generating VP to drive P1) is generated in response to the impedance control signal for controlling P2. EX1010, 6:36-45 (describing that the slew rate control signals are generated **in response to** the impedance control signals Z0, Z0*). Similarly, P5 is controlled into and out of operation in coaction with N2, because the slew rate control signal for controlling P5 (P-SLEW for generating VN to drive N1) is generated in response to the impedance control signal for controlling N2. *See also*

EX1001, FIGS. 3, 4, and 7 (illustrating similar configuration for controlling QN17 and QP2).

Therefore, Itoh in view of Muljono renders obvious this this element.

[1.4]

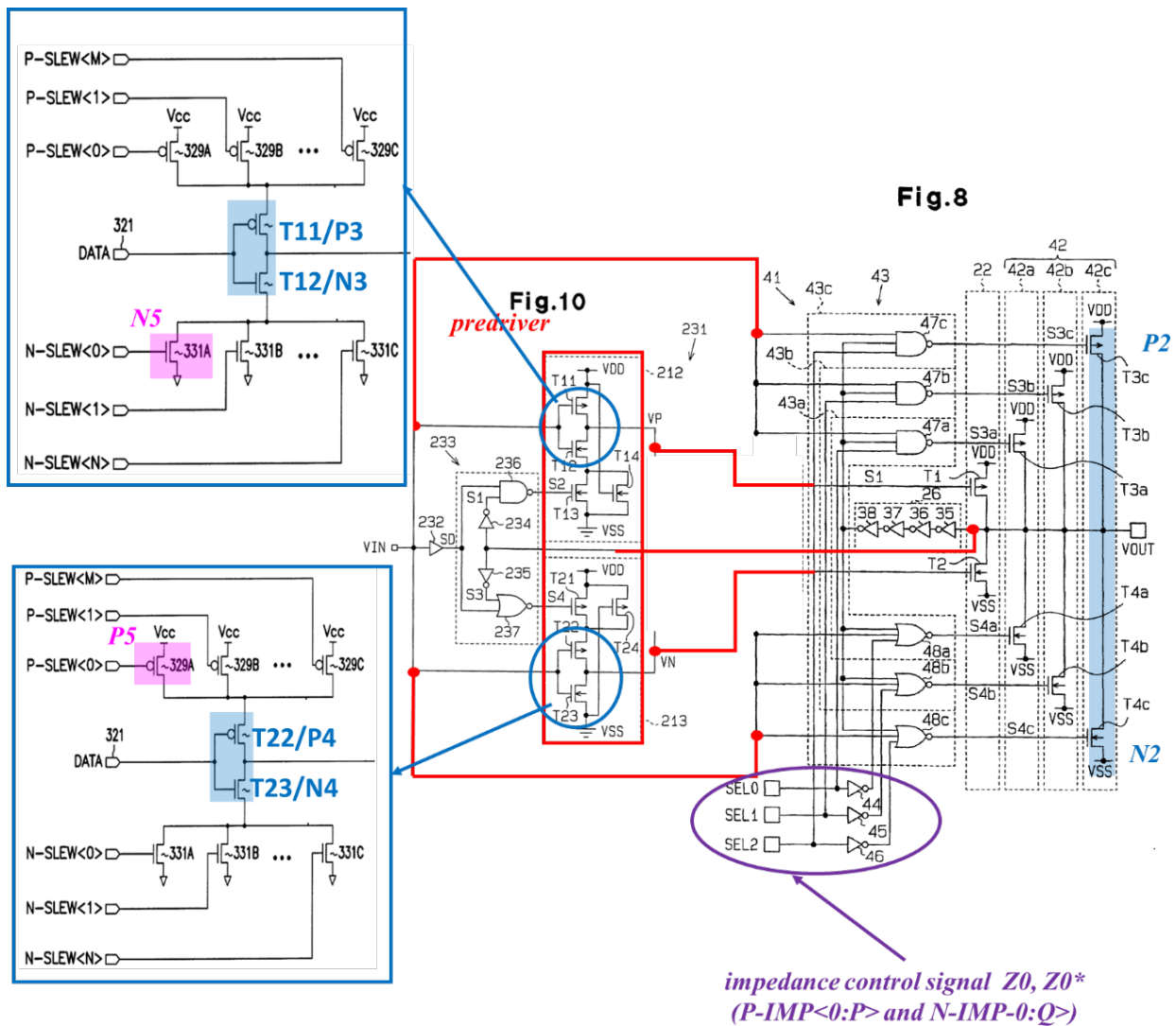
Itoh teaches this element for the reasons discussed at Ground 2:[1.4].

EX1003, ¶284.

3. Claim 2

Itoh in view of Muljono renders obvious this element. EX1003, ¶¶285-286.

As shown in Example 3.1 illustrated below, the number of each P2 and N2 corresponds to impedance control signals, and the number of each N5 and P5 corresponds to slew rate control signals, each would have been implemented with any suitable number (e.g., 2, 3, 4, etc.) based on design needs.



Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

Accordingly, in a case where there are three N5 (NMOS transistors 331A, 331B, and 331C) and three P5 (PMOS transistor 329A, 329B, and 329C), and three pairs of P2 and N2, then the number (6) of N5 and P5 equals to the number (6) of P2 and N2.

4. Claim 3

Itoh in view of Muljono renders obvious this element. EX1003, ¶¶287-289.

As discussed at Ground 3:[2.0], the number of P2, N2, P5, and N5 may be implemented with any suitable numbers. In a case where the number of P2, N2, P5, and N5 are 3, 3, 4, and 4 respectively, the number (6) of P2 and N2 is different from the number (8) of N5 and P5.

5. Claim 4

Itoh teaches this element for the reasons discussed at Ground 2:[4.0].
EX1003, ¶290.

6. Claim 5

[5.0]-[5.2.2]

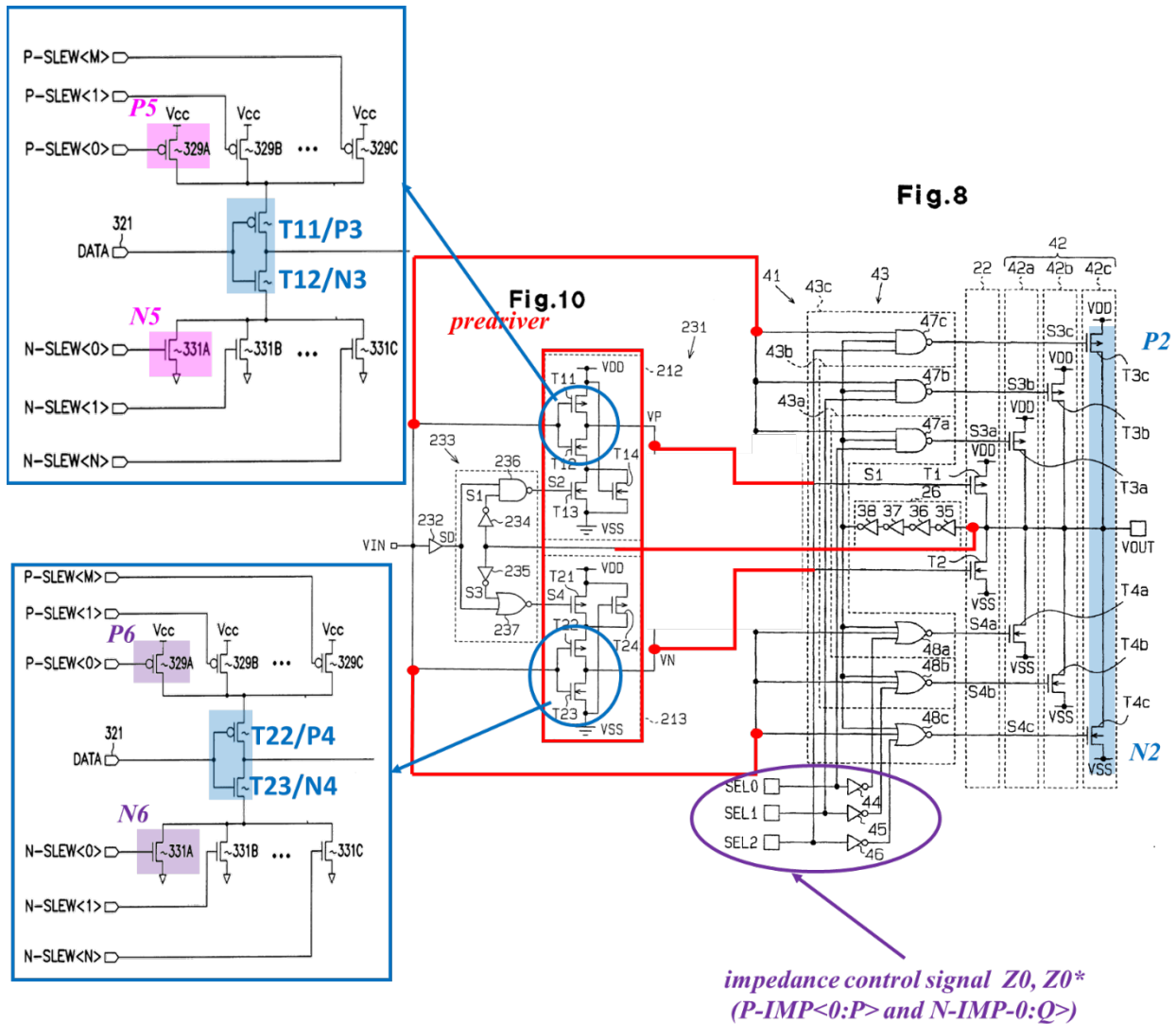
Itoh teaches these element for the reasons discussed at Ground 3:[1.0]-
[1.2.2]. EX1003, ¶291.

[5.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3],

Itoh in view of Muljono renders obvious this element. EX1003, ¶¶292-293.

Continuing with Example 3.1 as illustrated below, circuit 212 in the predriver has one fifth n-channel MOS transistor (transistor 331A, annotated as N5) for driving the first p-channel MOS transistor (T1, annotated as P1) using VP in coaction with said third n-channel MOS transistor (transistor T12, annotated as

N3), because N5 and N3 are connected in series to generate VP.



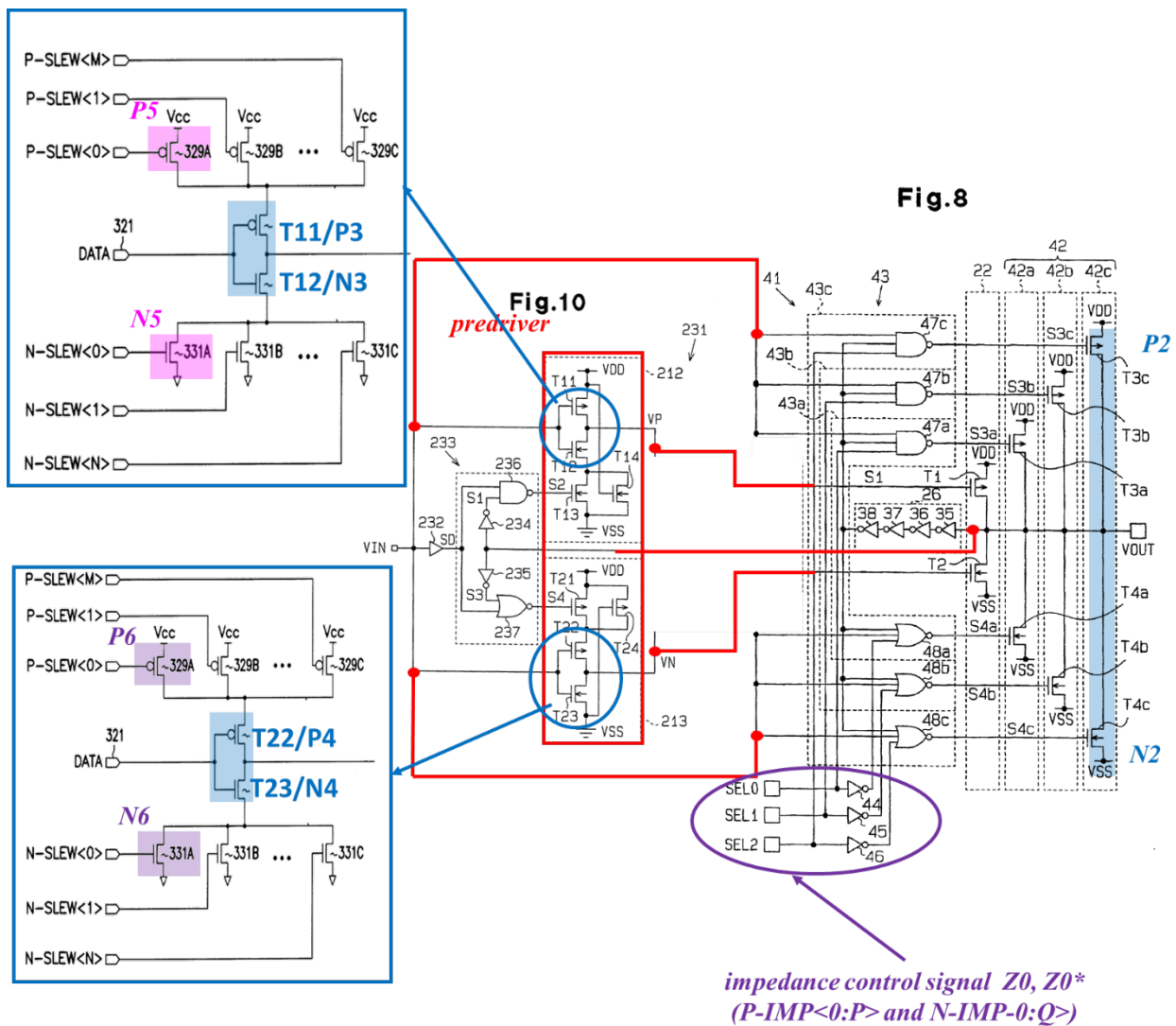
Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

Further, circuit 212 has at least one fifth p-channel MOS transistor (transistor 329A, annotated as P5) for driving T1/P1 using VP in coaction with said third p-channel MOS transistor (T11/P3), because P5 and P3 are connected in series to generate VP.

[5.2.4] [the predriver having] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]; and

Itoh in view of Muljono renders obvious this element. EX1003, ¶¶294-296.

Continuing with Example 3.1 as illustrated below, circuit 213 in the predriver has at least one at least one sixth p-channel MOS transistor (transistor 329A, annotated as P6) for driving said first n-channel MOS transistor (T2/N1) in coaction with said fourth p-channel MOS transistor (T22/P4), because P6 and P4 are connected in series and work in coaction to generate VN for driving N1.



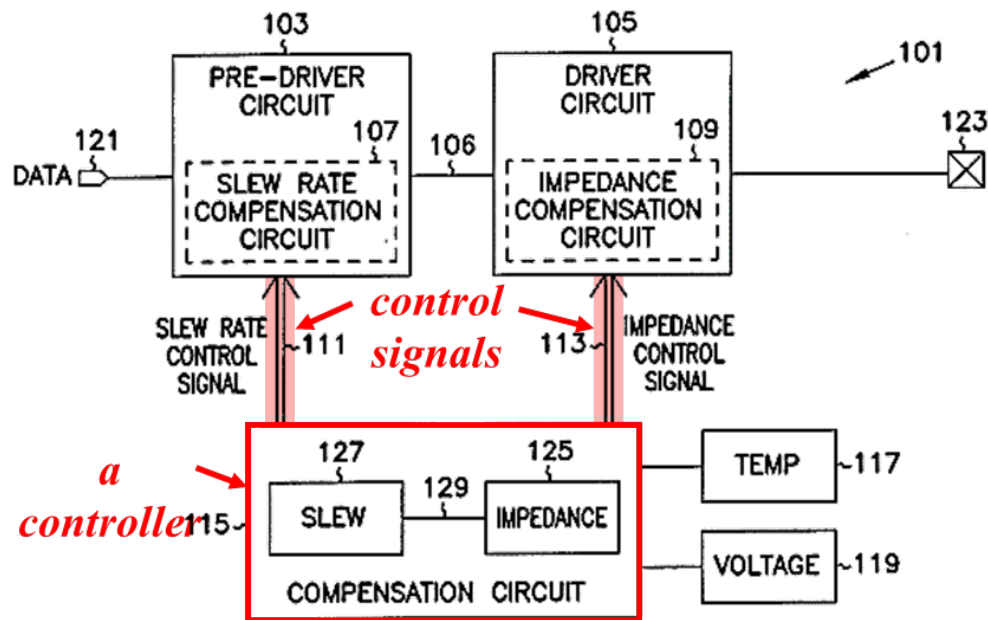
Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

Circuit 213 further includes at least one sixth n-channel MOS transistor (transistor 331A, annotated as N6) for driving T2/N1 in coaction with said fourth n-channel MOS transistor (T23/N4), because N6 and N4 are connected in series and work in coaction to generate VN for driving N1.

[5.3] a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2],

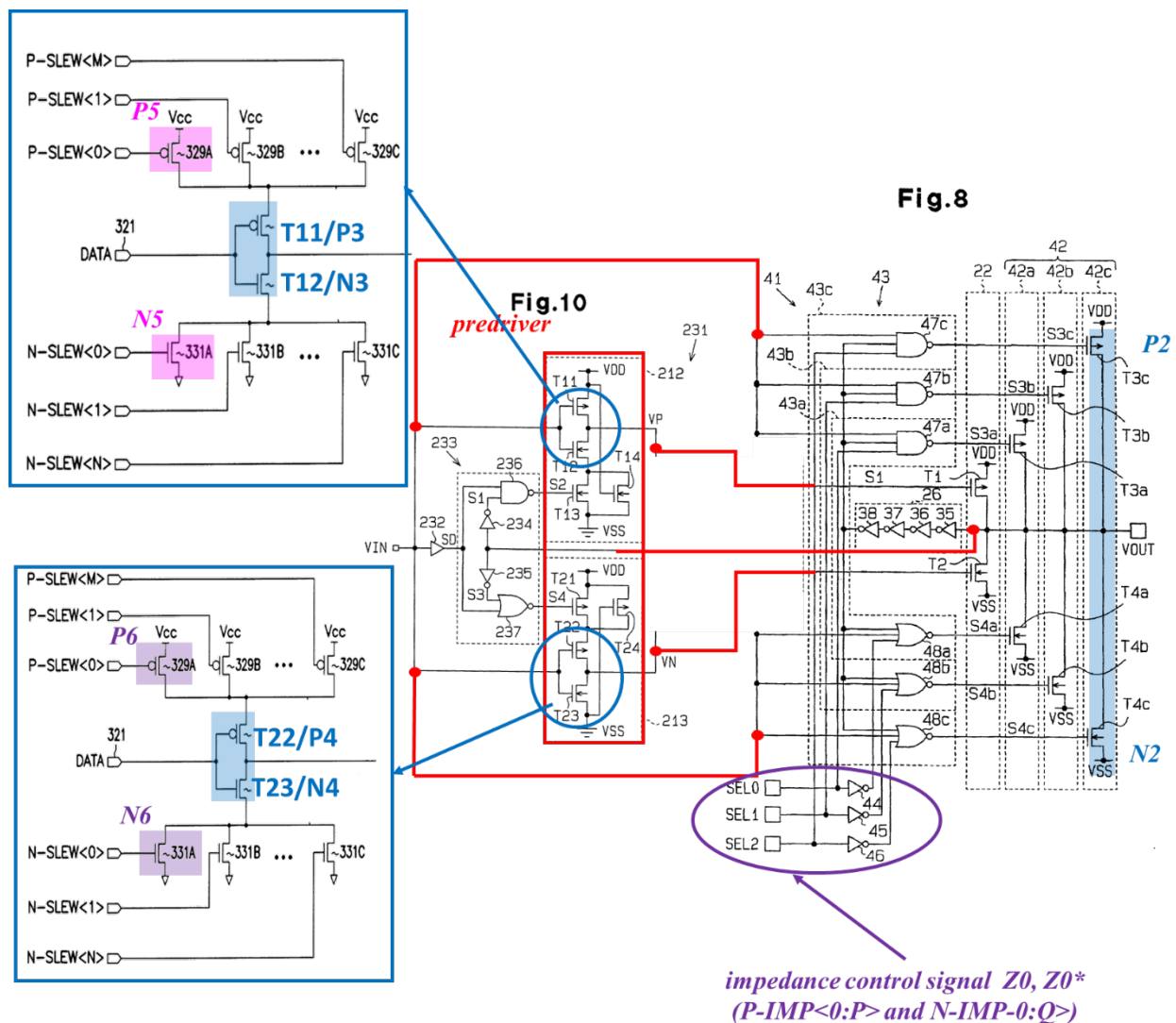
Itoh in view of Muljono renders obvious this element. EX1003, ¶¶297-298.

Continuing with Example 3.1, as discussed at Ground 3:[1.3], Example 3.1 includes a controller (compensation circuit 115 as taught by Muljono) that generates control signals including slew rate control signal impedance control signal, which control the transistors in the pre-driver circuit in coaction with the transistors in the main driver.



EX1010, FIG. 1, annotated

As shown in Example 3.1 as illustrated below, the control signals control N5 and P5 (using slew rate control signals for generating VP to control P1) into and out of operation in coaction with P2 (using control signal P-IMP provided to the SEL0-SEL2 for controlling P2), and control P6 and N6 (using slew rate control signals for generating VP to control N1) into and out of operation in coaction N2 (using impedance control signal provided to SEL0-SEL2 and inverter, or directly providing to gates 48a, 48b, 48c).



Example 3.1
(Combination of Example Embodiment 2.1 and Muljono)

In Example 3.1, N5 and P5 in circuit 212 are controlled into and out of operation in coaction with P2, because the slew rate control signal for controlling N5 and P5 (for generating VP to drive P1) is generated in response to the impedance control signal for controlling P2. EX1010, 6:36-45 (describing that the slew rate control signals are generated in response to the impedance control signals Z0, Z0*). Similarly, P5 is controlled into and out of operation in coaction with N2, because the slew rate control signal for controlling P5 (P-SLEW for generating VN to drive N1) is generated in response to the impedance control signal for controlling N2. *See also* EX1001, FIGS. 3, 4, and 7 (illustrating similar configuration for controlling QN17 and QP2).

This configuration of controlling N5 in coaction with P2 and controlling P5 in coaction with N2 is similar to the configuration in the '539 patent. *See, e.g.,* EX1001, FIGS. 3, 4, and 7 (illustrating controlling N5 (e.g., QN17) into and out of operation in coaction with P2 (e.g., QP2) where the control signals for N5 and P2 are each generated using the same signals $\phi 3$ and VIN).

Accordingly, Itoh in view of Muljono renders obvious this limitation.

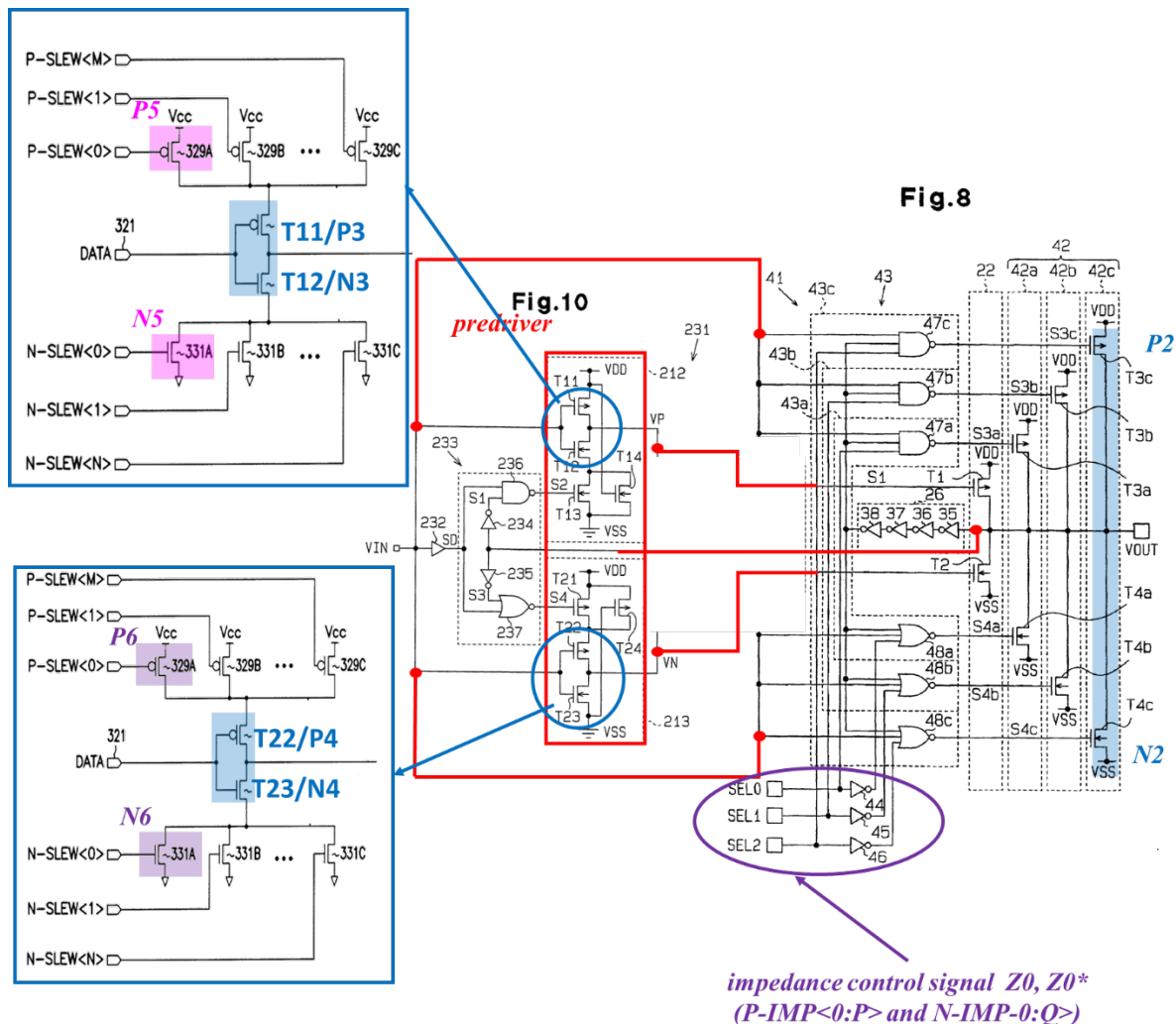
[5.4]

Itoh teaches this element for the reasons discussed at Ground 3:[1.4]. EX1003, ¶299.

7. Claim 6

Itoh in view of Muljono renders obvious this element. EX1003, ¶¶300-303.

As shown in Example 3.1 illustrated below, the number of P2 and N2 corresponds to impedance control signals, and the number of N5, P5, N6, and P6 corresponds to slew rate control signals, each would have been implemented with any suitable number (e.g., 2, 3, 4, etc.) based on design needs.



Example 3.1
(Combination of Example Embodiment 2.1 and Muljono)

Accordingly, in a case where there are there are two for each N5, P5, N6, P6, and there are four for each P2 and N2, the number (8) of N5, P5, N6, and P6 is equal to the number (8) of P2 and N2.

8. Claim 7

Itoh in view of Muljono renders obvious this element. EX1003, ¶¶304-306.

As discussed at Ground 3:[6.0], the numbers of P2, N2, N5, P5, N6, and P6 would have been implemented with any suitable numbers. Accordingly, in a case where there are three for each of P2, N2, N5, P5, N6, and P6, the number (12) of N5, P5, N6, and P6 is different from the number (6) of P2 and N2.

9. Claim 8

Itoh teaches this element for the reasons discussed at Ground 3:[4.0].

EX1003, ¶307.

E. Grounds 4, 5, and 6: Combination of Itoh, Skorup, and Borkar (Ground 4), Combination of Itoh and Borkar (Ground 5), and Combination of Itoh, Muljono, and Borkar (Ground 6) Render Obvious Claims 9-12 Under §103(a)

Claims 9-12 are very similar to claims 1 and 5, with one new element—a delay monitor. The analysis for Grounds 4-6 is the same as the analysis for Grounds 1-3, respectively, with further reference to Borkar to show that the claimed delay monitor was obvious. EX1003, ¶¶308-335. For all the discussions below regarding Itoh, the analysis applies to Itoh's embodiments (e.g., Fig. 5) as used in Ground 1, or a combination of Itoh's embodiments (e.g., combination of

Figs. 8 and 10) as applied in Grounds 2 and 3.

1. Reasons to Combine Itoh and Borkar

A POSITA would have been motivated to apply Borkar's teaching of a delay monitor, specifically a scaled down version of an output driver to monitor speed variations, in the output driver circuit taught by Itoh (as applied at Grounds 1-3 above) to produce the obvious, beneficial, and predictable results of an improved "output driver design which is compensated to give steady performance for changes" in PVT as taught by Borkar. EX1008, 1:11-33; EX1003, ¶¶309-314.

First, Itoh and Borkar are analogous prior art to the '539 patent and in the same field of endeavor pertaining to output buffer circuits. *See, e.g.*, EX1001, 1:15-19; EX1006, Title, 1:6-7; EX1008, Abstract.

Second, Itoh and Borkar share the same goal of providing an output buffer circuit that generates an output signal with less variation. EX1006, 14:38-53; EX1008, 1:11-34.

Finally, applying Borkar's teachings in Itoh would have been no more than the combination of known elements according to known methods (e.g., incorporating compensations circuits with a scaled down version of an output driver) obvious to a POSITA.

2. Claim 9

[9.0] 9. An integrated semiconductor circuit device comprising:

To the extent that the preamble is limiting, Itoh and Borkar renders the preamble obvious. EX1003, ¶¶315-318.

Specifically, Itoh describes an integrated semiconductor circuit device. *See, e.g.,* EX1006, 7:9-13 (describing that output driver circuits including PMOS and NMOS transistors, which are devices of an integrated semiconductor circuit device). *See also* EX1008, Abstract, 1:11-32 (describing an integrated semiconductor circuit device).

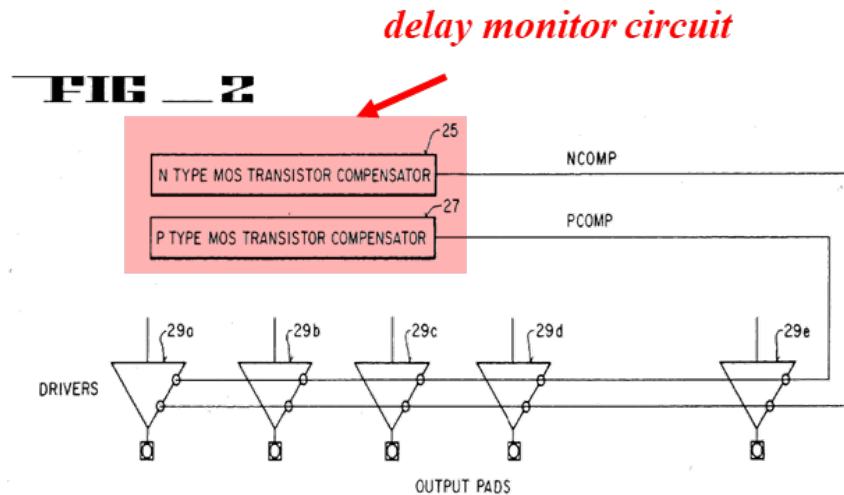
[9.1] an output buffer circuit according to claim 1;

See Grounds 1-3:Claim 1. EX1003, ¶319.

[9.2] a delay monitor circuit identical in circuit arrangement to said output buffer circuit and having transistors controlled according to said control signals in the same manner as with said output buffer circuit,

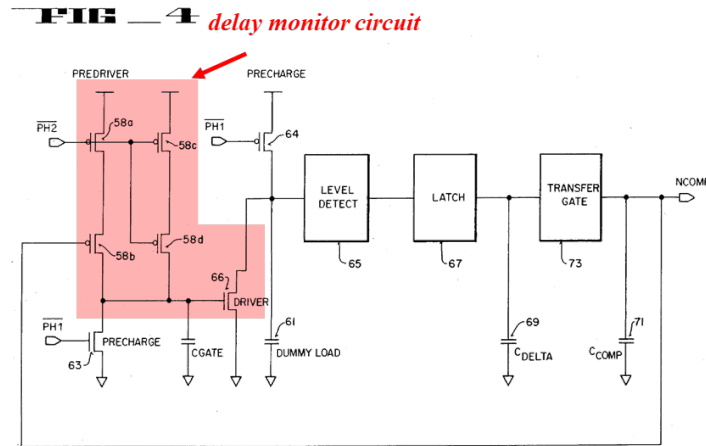
Itoh in view of Borkar renders obvious this element. EX1003, ¶¶320-324.

Specifically, as shown in annotated FIG. 2 of Borkar below, Borkar teaches a delay monitor circuit (compensator including NMOS transistor compensator 25 and PMOS transistor 27) that “tracks overall performance of the transistors.” EX1008, 5:10-19.



EX1008, FIG. 2, annotated

As shown in annotated FIG. 4 of Borkar (corresponding to compensator 25 of FIG. 2) below, Borkar's compensator circuit includes a delay monitor circuit (including dummy driver 66 and predriver including transistors 58c-58d) that is identical in circuit arrangement to the output buffer circuit (**"a scaled down version of the driver, and a predriver"**) and having transistors controlled according to said control signals in the same manner as with said output buffer circuit. EX1008, 7:5-15 (**"This dummy driver 66 is also compensated the same way the actual driver is."**).



EX1008, Borkar, FIG. 4, annotated

A POSITA would have been motivated to apply Borkar's teaching of dynamic compensation in the output driver circuit taught by Itoh (individual embodiment or as combined) for an improved output driver design compensated for changes in PVT. EX1008, 1:11-33; *see also* Grounds 3 and 4: Reasons to Combine.

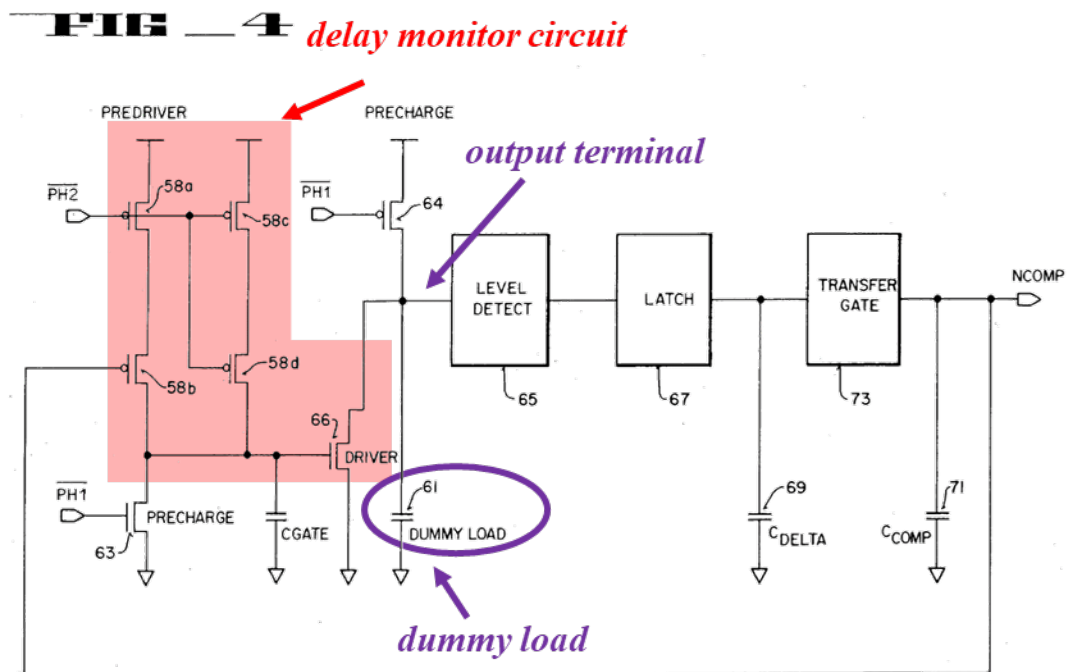
As such, in the combination of Itoh and Borkar, a delay monitor that is a scaled-down version of the output buffer circuit is used to generate compensation signals for compensating the PTV variations and control the speed of the output driver. *See, e.g.*, EX1008, FIG. 3.

Therefore, Itoh in view of Borkar renders obvious this element.

[9.3] said delay monitor circuit having an output terminal connected to a dummy load determined from an actual load of said output buffer circuit based on a transistor size ratio between said output buffer circuit and said delay monitor circuit.

Itoh in view of Borkar renders obvious this limitation. EX1003, ¶¶325-327.

Specifically, as shown in annotated FIG. 5 of Borkar below, Borkar teaches that its delay monitor circuit (including predriver and dummy driver 66) having an output terminal connected to a dummy load 61, which “duplicates a **scaled down version of a load that a driver usually drives.**” EX1008, 7:5-9. It was well-known that such scaled down version is determined based on a transistor size ratio between said output buffer circuit and said delay monitor circuit.



EX1008, FIG. 4, annotated

3. Claim 10

[10.0]-[10.3]

Itoh in view of Borkar renders obvious the elements for the reasons discussed at [9.0], Grounds 1-3:Claim 5, and [9.2]-[9.3]. EX1003, ¶¶330-331.

4. Claim 11

[11.0] The integrated semiconductor circuit device according to claim 9, wherein said delay monitor circuit has transistors having a smaller device size with a smaller gate width than the transistors of said output buffer circuit.

Itoh in view of Borkar renders obvious this element. EX1003, ¶¶332-334.

As discussed at [9.2], Itoh combined with Borkar includes a delay monitor circuit, which is “a **scaled down version** of an output driver.” EX1008, 4:14-19.

A POSITA would have understood that such a scaled down version uses transistors having a smaller device size (with a smaller gate width) than the transistors of the output buffer circuit, with the benefit of using less area.

5. Claim 12

Itoh in view of Borkar renders obvious this limitation for the reasons discussed at [11.0]. EX1003, ¶¶335.

IX. CONCLUSION

Petitioner has established a reasonable likelihood that Challenged Claims of the '539 patent are unpatentable, and requests institution of *inter partes* review.

Respectfully submitted,

Dated: August 8, 2023

/ *David O'Dell* /
David M. O'Dell
Lead Counsel for Petitioner
Registration No. 42,044

X. MANDATORY NOTICES

A. Real Party-in-Interest

The real party-in-interest is Western Digital Technologies, Inc. (“Petitioner” or “WDT”).

As shown in X.B below, six litigations concerning the ’539 Patent are pending, all involving WDT’s customers as defendants. Petitioner submits that WDT is the only real party-in-interest, but regardless of whether any defendant should be named as an RPI, no RPI analysis is necessary because there are no time bar or estoppel implication for any defendant. *SharkNinja Operating LLC v. iRobot Corp.*, IPR2020-00734, Paper 11 (Oct. 6, 2020) (precedential) (no RPI analysis necessary at institution absent allegation of time bar or estoppel based on unnamed RPI).

B. Related Matters

As of the filing date of this Petition and to the best knowledge of Petitioner, the ’539 Patent has been asserted in the following matters:

Case Heading	Number	Court	Filed	Status
<i>Longitude Licensing Limited v. ASUSTeK Computer Inc. et al.</i>	8-23-cv-00033	CDCA	Jan. 09, 2023	stayed pending the resolution of the Amazon Action with respect to WDT
<i>Longitude Licensing Limited v. Lenovo Group Limited et al.</i>	8-23-cv-00035	CDCA	Jan. 09, 2023	

Case Heading	Number	Court	Filed	Status
<i>Longitude Licensing Limited v. Acer Inc. et al.</i>	8-23-cv-00036	CDCA	Jan. 09, 2023	
<i>Longitude Licensing Limited v. HP Inc.</i>	8-23-cv-00038	CDCA	Jan. 09, 2023	
<i>Longitude Licensing Limited v. Dell Technologies Inc. et al.</i>	8-22-cv-02312	CDCA	Dec. 23, 2023	
<i>Longitude Licensing Limited v. Amazon.com, Inc. (Amazon Action)</i>	8-23-cv-00039	CDCA	Jan. 09, 2023	WDT's motion to intervene granted; stayed pending the resolution of the Amazon Action with respect to WDT

C. Lead and Back-up Counsel and Service Information

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Please address all correspondence to lead and back-up counsel. Petitioner consents to electronic service and asks Patent Owner to do the same.

XI. CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, the undersigned attorney for Petitioner declares that the argument section of this Petition (Sections I–IX) has 13,987 words, according to the word count tool in Microsoft Word™.

/ *David O'Dell* /

David M. O'Dell

Lead Counsel for Petitioner

Registration No. 42,044

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, service was made on Patent Owner as detailed below.

Date of service August 8, 2023

Manner of service FEDERAL EXPRESS

Documents served Petition for *Inter Partes* Review, including Exhibit List;
Exhibits EX1001–EX1016

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