

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

Case IPR2023-01286
U.S. Patent No. RE43,539

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

No.	Description
2001	Listing of possible size values for device size and gate width for each of four transistors P1, N1, P2, and N2

I. Introduction

To simplify issues for the Board, the district court, and the parties, Patent Owner intends to disclaim claims 1-3 and 5-12 of the U.S. Patent No. RE43,539 (the “539 Patent”) shortly after the filing of this Preliminary Response, leaving claim 4 as the only remaining claim challenged by the Petition.¹ Because the Board may not institute an *inter partes* review based on disclaimed claims,² institution of this proceeding is appropriate only if the Petition can demonstrate a reasonable likelihood of prevailing with respect to claim 4. The Petition, however, cannot demonstrate a reasonable likelihood of prevailing with respect to claim 4, because no prior art discloses the dependent limitation of claim 4, and the Petition does not present any evidence that a POSITA would have been motivated to modify the prior art to incorporate that limitation.

¹ Patent Owner does not concede the merits of any of the grounds identified by Petitioner as to any of the claims; disclaimer of the referenced claims is merely to simplify proceedings.

² 37 C.F.R. § 42.107(e) (“No *inter partes* review will be instituted based on disclaimed claims.”).

By way of background, claim 4 requires that each of two specific transistors (P2 and N2) have a smaller device size and a smaller gate width than each of two other specific transistors (P1 and N1).

The Petition acknowledges that no prior art reference of record actually discloses the transistor size requirements of claim 4. Instead, the Petition alleges that the dependent limitation of claim 4 is merely one of “two-well known design choices.” Pet. at 62. But the Petition is wrong—there are *hundreds* of possible ways (not simply two) to configure the relative sizes of eight variables (the device size and gate width for each of P1, N1, P2, and N2). And the Petition does not identify any specific benefit to implementing the claim 4 size requirements. Indeed, the Petition acknowledges that the one instance where its lead reference *does* provide details of the relevant sizes of the transistors, P2 and N2 are *larger* than P1 and N1, contrary to the claim requirement. *See* Pet. at 63 (arguing that this “size requirement of Embodiment 1” should be disregarded because other embodiments do not “need[]” that size requirement). Accordingly, the Petition cannot establish that the transistor size requirements of claim 4 would have been obvious in view of the prior art, and institution should be denied.

II. Background

A. Western Digital's Petition

Petitioner Western Digital Technologies, Inc. (“Petitioner” or “Western Digital”) challenges claims 1-12 of the '539 Patent. The Petition's six asserted grounds for unpatentability are structured as follows:

- Ground 1: Obviousness of claims 1-3 and 5-7 over Itoh and Skorup.
- Ground 2: Obviousness of claims 1-8 over Itoh.
- Ground 3: Obviousness of claims 1-8 over Itoh in view of Muljono.
- Ground 4: Obviousness of claims 9-12 over Itoh in view of Skorup and Borkar.
- Ground 5: Obviousness of claims 9-12 over Itoh in view of Borkar.
- Ground 6: Obviousness of claims 9-12 over Itoh in view of Muljono and Borkar.

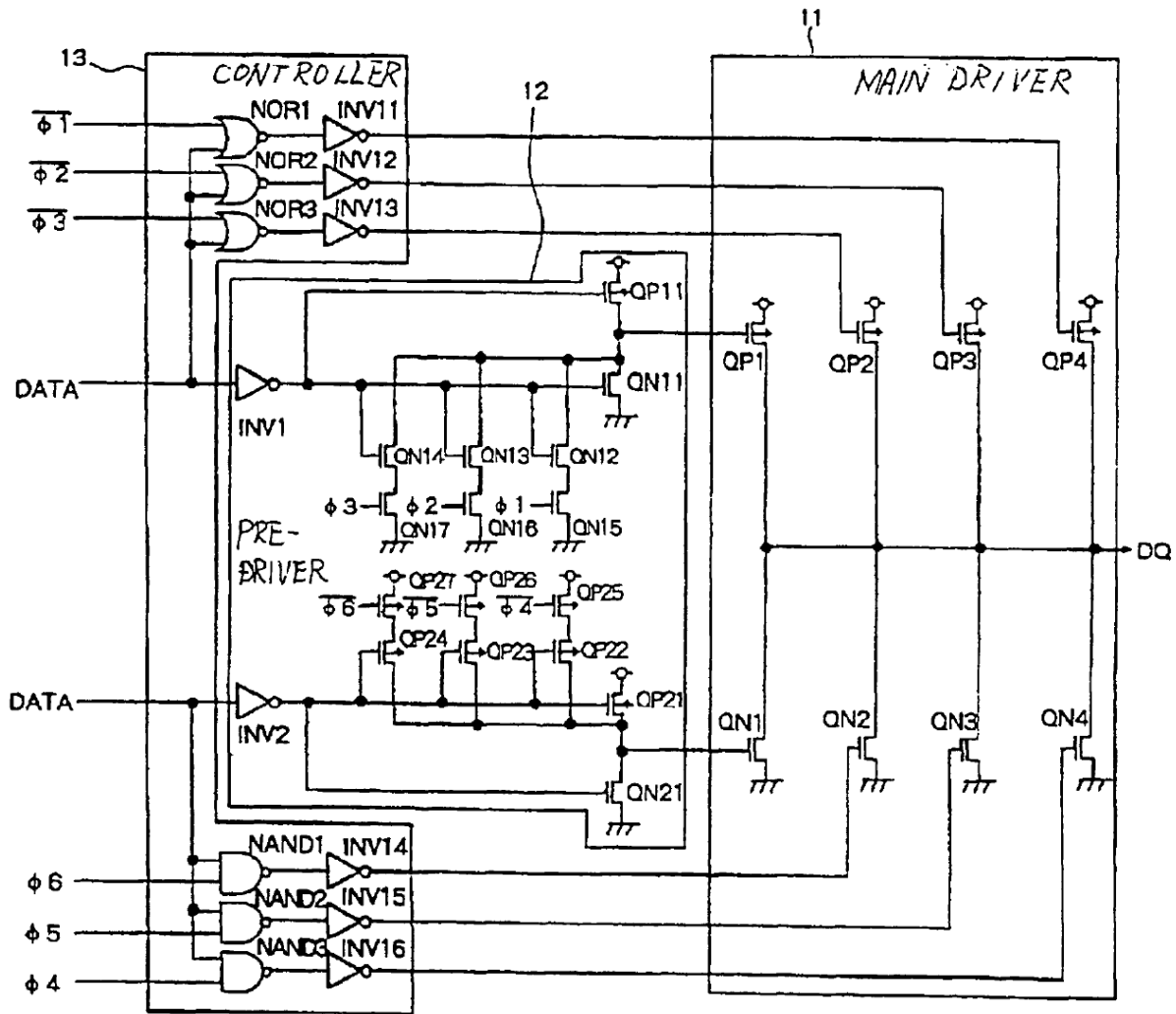
Notably, only Grounds 2 and 3 challenge claim 4 of the '539 Patent. Because Patent Owner is in process of filing a disclaimer of all challenged claims of the '539 Patent other than claim 4, institution should be denied if the Board finds that the Petition has not established a reasonable likelihood of prevailing with respect to claim 4 in either of Grounds 2 or 3.

B. Overview of the '539 Patent

At a high level, the '539 Patent is directed generally to an output buffer circuit having low variation in slew rate. *See* Ex. 1001 ('539 Patent) at 2:54-60 (“It is therefore an object of the present invention to provide an output buffer circuit which

is capable of sufficiently compensating for variations in the cross-point between rising and falling waveforms of output pulses and variations in the slew rate against variations in the power supply voltage and the ambient temperature even when the output buffer circuit is incorporated in a system.”); *id.* at Claim 1, preamble (reciting an “output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate”).

More specifically, as depicted in FIG. 3 (reproduced below), the '539 Patent teaches that multiple transistor pairs (e.g., pairs QP1 / QN1, QP2 / QN2, QP3 / QN3, and QP4 / QN4) can be beneficially used to drive a load. *See id.* at FIG. 3 & 5:59-61, 6:13-35.



'539 Patent at FIG. 3.

The '539 Patent teaches that slew rate of the output signal is impacted by device size (which in the '539 Patent is taught to be correlated with gate width) of transistors. For example, the '539 Patent teaches that if the first pair of transistors QP1 and QN1 have larger device sizes and gate widths than the additional pairs of transistors such as QP2 and QN2, the additional pairs of transistors will have a relatively small effect on slew rate. *See id.* at 6:36-40 ("pMOS transistors QP2

through QP4 and QN2 through QN4 comprise transistors having a small device size (a narrow gate width) whose effect on the ratio t_r/t_f of output pulses is smaller than pMOS transistor QP1 and nMOS transistor QN1.”); *see also id.* at 1:39-43 (explaining that “slew rate” is adjusted “by changing the ratio of t_r (rise time) / t_f (fall time) of an output pulse waveform”); *id.* at 7:59-63 (discussing “adjusting the ratio t_r/t_f (slew rate) of output pulses”). This relationship is specifically claimed in claim 4, which recites that a “second p-channel MOS transistor [e.g., QP2] and [a] second n-channel MOS transistor [e.g., QN2] have a smaller device size with a smaller gate width than said first p-channel MOS transistor [e.g., QP1] and said first n-channel MOS transistor [e.g., QN1], and have a small effect on rise and fall times of pulses output from said main driver.”

As noted above, Patent Owner is in the process of disclaiming all challenged claims but claim 4 (which depends from claim 1). Claims 1 and 4 recite:

1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor;

a predriver with outputs for driving only said first n-channel in channel MOS transistor and only said first p-channel MOS transistor having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor; and

a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor,

wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.

4. The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor, and have a small effect on rise and fall times of pulses output from said main driver.

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '539 Patent “would have a bachelor’s or the equivalent degree in electrical or computer engineering or a related field, and 2-3 years of professional experience relating to integrated circuit design.” Pet. 3. For purposes of this Preliminary Response only, Patent Owner does not challenge that definition.

IV. Claim Construction

The Petition states that “for purposes of this proceeding and the analysis presented herein, no claim term requires express construction.” Pet. 4. For purposes of this Preliminary Response, Patent Owner agrees that no express construction of any term is necessary.

V. The Petition’s challenges of claim 4 fail.

Claim 4 of the '539 Patent recites (using the Petition’s annotations P1, N1, P2, and N2): “The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor [P2] and said second n-channel MOS transistor [N2] have a smaller device size with a smaller gate width than said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1], and have a small effect on rise and fall times of pulses output from said main driver.” *See* '539 Patent at Claim 4; Pet. at 60-61 (annotating the claim language and proposed prior art modification with P1, N1, P2, and N2).

Claim 4 thus requires that each of two specific transistors (P2 and N2) have a smaller device size *and* a smaller gate width than each of two other specific transistors (P1 and N1). Put differently, claim 4 requires eight different relationships between eight different variables: (1) P2 device size < P1 device size; (2) P2 device size < N1 device size; (3) P2 gate width < P1 gate width; (4) P2 gate width < N1 gate width; (5) N2 device size < P1 device size; (6) N2 device size < N1 device size; (7) N2 gate width < P1 gate width; and (8) N2 gate width < N1 gate width.

Although the Petition states that “Itoh teaches this [requirement]” (*see* Pet. 60), the Petition does not point to any teaching in Itoh that discloses that *any* of the above eight inequalities are satisfied. *See generally* Pet. at 60-63. Instead, the Petition alleges that “selecting a smaller device size with a smaller gate width than P1 and N1 is one of the two-well known design choices (the other is having a greater size),” and from that starting premise contends that there would be “corresponding design needs” that would lead a POSITA to choose that the design choice where P1 and N1 have a smaller device size with a smaller gate width. *See* Pet. at 62. Thus, the Petition’s theory regarding the obviousness of claim 4 relies on the premise that claim 4’s size requirements constitute one of only two design choices.

The Petition is wrong that the claim 4 configuration of sizes and widths is only one of two design choices. As an initial matter, the Petition is obviously wrong because it neglects the possibility that two sizes could be *equal* to one another. For

example, if the device size of P2 is the *same* as the device size of N2, claim 4 is clearly not met, and the Petition does not even address this possibility or explain why a POSITA would have implemented the claim 4 configuration over an equal-size alternative.

The Petition is additionally incorrect because there are *hundreds* of possible ways (rather than merely two ways) to configure the relative sizes of eight variables (the device size and gate width for each of P1, N1, P2, and N2). An example of each of the possible ways to arrange the sizes of these variables, in selecting between two options of sizes (“small” and “large”) is provided in Exhibit 2001. As shown in Exhibit 2001, there are 256 different ways to assign “small” and “large” to the device size (“DS”) and gate width (“GW”) for each of P1, N1, P2, and N2. The result of 256 combinations occurs because there are two possible combinations of eight variables, for $2^8 = 256$ possible combinations. As further shown in Exhibit 2001, only *one* of those possible 256 combinations (entry number 241 on page 7) satisfies

the requirements of claim 4, where the gate widths and device sizes of P2 and N2 are less than the gate widths and device sizes of P1 and N1.³

As noted above, the Petition's only argument that a POSITA would arrive at the configuration recited by claim 4 relies on the false premise that claim 4's configuration is only one of two possible design choices. And while the Petition conclusorily asserts that a POSITA would have selected the claim 4 configuration "based on corresponding design needs (e.g., specific contribution by this particular pair of P2 and N2 to the overall output impedance)," the Petition does not provide

³ The Petition does not provide any evidence or allegation that a smaller gate width for a transistor necessarily equals a smaller device size for that transistor. However, the '539 Patent does teach that in the context of its invention, gate width and device size are correlated. *See* '539 Patent at 6:35-40 (teaching that "QP2 through QP4" and "QN2 through QN4 comprise transistors having a small device size (a narrow gate width)"). Of course, a patent's specification cannot be the basis for a finding of obviousness, but even if a POSITA *were* to take into account the '539 Patent's teachings regarding correlation between device size and gate width, the requirements of claim 4 would still only be satisfied by one out of 16 (2^4) possible combinations of the four size variables for each of P1, N1, P2, and N2.

any evidence of this assertion.⁴ For example, the Petition does not explain why a POSITA might have recognized that the configuration of claim 4 would have helpfully contributed “to the overall input impedance,” or otherwise identify even a hypothetical scenario in which a POSITA would have recognized that the claim 4 configuration (out of many possible configurations) would have been viewed as desirable by a POSITA.

⁴ The Petition does cite for this assertion expert testimony that repeats, verbatim, the Petition’s assertion. *See* Ex. 1003 at ¶ 220 (repeating verbatim the Petition’s assertion that “selecting a smaller device size with a smaller gate width than P1 and N1 is one of the two well-known design choices (the other is having a greater size), and a POSITA would have used this design option based on corresponding design needs (e.g., specific contribution by this particular pair of P2 and N2 to the overall output impedance).”). However, “[e]xpert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.” 37 C.F.R. § 42.65; *see Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper No. 9 at 15 (Aug 24, 2022) (precedential) (denying institution and giving “little weight” to “cited declaration testimony [that] is conclusory and unsupported” and “adds little to the conclusory assertion for which it is offered to support”).

The failure to identify any motivation to arrive at the configuration recited by claim 4 is not a trivial oversight; rather, it likely results from the fact that the alleged claim 4 configuration in the Petition's proposed modification to Itoh would not have had the benefit (reduced impact on slew rate) taught by the '539 Patent itself. Specifically, the inventor of the '539 Patent recognized the effect that selection of transistor size has on slew rate, and thus disclosed the importance of selecting appropriate transistor sizes to minimize impact on slew rate. *See* '539 Patent at 6:36-40 (“pMOS transistors QP2 through QP4 and QN2 through QN4 comprise transistors having a small device size (a narrow gate width) whose effect on the ratio t_r/t_f of output pulses is smaller than pMOS transistor QP1 and nMOS transistor QN1.”). In contrast, the Petition acknowledges that the transistor size of P2 and N2 in its proposed modification of Itoh would be *irrelevant* to slew rate. For instance, the Petition acknowledges that its modification “uses a different method for slew rate control,”⁵ such that P2 and N2 are turned off “whe[n] the slew rate is controlled,”

⁵ Specifically, the Petition proposes modifying Itoh's Figure 8 to accommodate a “slew-rate control type circuit” depicted in Itoh's Figure 10, which controls slew rate solely through interaction with P1 and N1, while P2 and N2 are disabled entirely.

such that those transistors would have **no** effect on slew rate. *See* Pet. 61 (“[D]uring A1 and A2 where the slew rate is controlled, P2 and N2 are turned off (by control signals S3c and S4c), and as such, have small effect on rise and fall times of VOUT.”). A POSITA would thus have been completely indifferent to the gate width and device size of P2 and N2 as variables to impact slew rate. *See Tris Pharma, Inc. v. Actavis Lab'ys FL, Inc.*, No. 2021-1495, 2022 WL 2525318, at *4 (Fed. Cir. July 7, 2022) (upholding a finding of no motivation to combine where the evidence showed a POSITA “would have been indifferent to” a required claim element). Accordingly, if the size requirements of claim 4 were applied to the Petition’s Ground 2 combination, those size requirements would **not** have had the same

See Pet. 44 (discussing “apply[ing] FIG. 10’s slew-rate control type circuit for driving [P1 and N1] to drive [P1 and N1] in FIG. 8.”); *id.* at 63 (“[I]n the combination, T1 (annotated as P1) and T2 (annotated as N1) are controlled using a different method for slew rate control by the slew rate control circuit of FIG. 10”); *id.* at 61 (“[D]uring A1 and A2 where the slew rate is controlled, **P2 and N2 are turned off** (by control signals S3c and S4c), **and as such, have [a] small effect on rise and fall times of VOUT.**”) (emphases added).

benefits recognized by the inventor of the '539 Patent, and those same benefits could not have motivated the Petition's proposed combination.

Finally, the Petition acknowledges that Itoh itself suggests that P2 and N2 should have a ***larger*** device size than P1 and N1, contrary to the claim 4 requirements. *See* Pet. 63 (discussing “the requirement of Embodiment 1 (FIG. 5) of Itoh that [P1] and [N1] have a higher impedance characteristic [and implicitly, a smaller gate width]⁶ than [P2] and [N2]”).⁷ While the Petition does not provide any

⁶ A POSITA would understand, as Petitioner recognizes, that a “higher impedance characteristic” is generally indicative of a smaller gate width, because a smaller gate width provides a narrower path through which current can flow.

⁷ For the Petition's Ground 2 analysis of claims 1 and 4, the Petition refers to Itoh's T1 as P1, Itoh's T2 as N1, Itoh's T3c as P2, and Itoh's T4c as N2. *See* Pet. at 48 (showing “Example 2.1” which annotates transistors T1, T2, T3c, and T4c as P1, N1, P2, and N2, respectively); *id.* at 48-50 (referring to “a first p-channel MOS transistor” as “T1” and “P1,” “a first n-channel MOS transistor” as “T2” and “N1,” “a second p-channel MOS transistor” as “T3c” and “P2,” and “a second n-channel MOS transistor” as “T4c” and “N2”; *id.* at 60 (depicting same annotated Example

motivation to deviate from this teaching of Itoh, the Petition does assert that this teaching of Itoh is not *necessary* as applied to the Petition’s combination. *See id.* (alleging that “the requirement of Embodiment 1 does not apply to Example 2.1, because . . . circuit 42 of FIG. 8 . . . no longer *needs* the size requirement of Embodiment 1 for sl[e]w rate control”) (emphasis added). Setting aside whether the Petition’s combination *needs* the size requirement of Embodiment 1 (which is contrary to the size requirements of claim 4), the Petition provides no evidence that a POSITA would have had any motivation to deviate from the size requirement of Embodiment 1. Put simply, a showing that the prior art does not *need to be configured in a manner contrary to the claim language* is not evidence that a POSITA *would have been motivated to modify the prior art in a manner consistent with the claim language*. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073

2.1); *id.* at 61 (referring to “T3c and T4c (P2 and N2),” and further noting that “P2 and N2 are turned off (by control signals S3c and S4c)”). It is not clear why the Petition additionally refers to “a plurality of pairs of P2 and N2” (*id.* at 62-63) in its claim 4 analysis, because the Petition only alleges that T3c and T4c (controlled by S3c and S4c) satisfy the “small effect on rise and fall times” limitation. *See id.* at 60-61.

(Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”) (emphases in original).

In sum, the Petition provides no evidence that a POSITA would have been motivated to arrive at the specific relationships between transistor gate widths and device sizes required by claim 4. Instead, the Petition incorrectly asserts that the claim 4 configuration is one of only two possible options that would be selected under (unspecified) circumstances, and fails to acknowledge that the claim 4 configuration is one out of many possible configurations. The Petition also fails to allege *any* specific benefit that a POSITA would have recognized by pursuing the claim 4 configuration in the context of the Petition’s combination, in stark contrast to the ’539 Patent itself, which teaches that smaller gate widths and device sizes should be selected to achieve a desired, small effect on slew rate. And the Petition’s failure to articulate any motivation to pursue the claim 4 configuration is especially problematic for the Petition, given Itoh’s own teachings that the claim 4 requirement is *not* satisfied.

Accordingly, the Petition fails to set forth a prima facie case of invalidity with respect to its Ground 2 challenge of claim 4. And because the Petition’s Ground 3 challenge of claim 4 merely incorporates by reference its Ground 2 challenge (*see* Pet. at 91), that challenge fails for the same reasons.

VI. Conclusion

Because the Petition fails to establish invalidity of the sole remaining challenged claim 4 of the '539 Patent, institution should be denied.

Date: November 24, 2023

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 3,753 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

Date: November 24, 2023

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on November 24, 2023, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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