

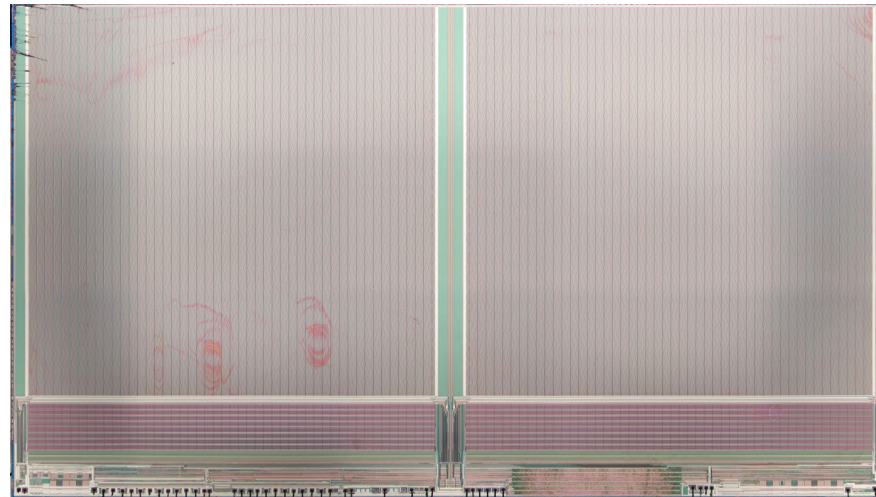
Exhibit B – Infringement of U.S. Patent No. RE43,539E1 vs. Accused Instrumentalities

Western Digital Technologies, Inc. (“Western Digital”) infringes at least the identified claims below of U.S. Patent No. RE43,539E1 (“’539 Patent”) by selling, offering to sell, and/or importing the following products: Western Digital PC SN530 NVMe SSDs, Western Digital SSDs, and/or Western Digital NAND memory chips and all versions and variations of them offered for sale since the issuance of the ’539 patent (collectively the “Accused Instrumentalities”). The Accused Instrumentalities further includes all Western Digital products incorporating these SSDs or memory chips, and all memory chips with similar die corners, I/Os and peripheral circuits, and products that include memory chips with a similar layout and functionality to the memory chips used in Western Digital PC SN530 NVMe SSDs. Longitude is informed and believes that identifying the full list of Accused Instrumentalities requires the production of confidential information from Western Digital. Longitude has requested such information but it has not yet been produced. Longitude reserves the right to amend these contentions to include such additional Accused Instrumentalities at a later date. The below chart shows infringement by the Western Digital PC SN530 NVMe SSD. Longitude asserts that this product is representative of all Accused Instrumentalities because as all are SSDs with similar memory chips and with a similar layout and design.

Issued Claims	Accused Instrumentalities
1[pre] An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:	The Western Digital PC SN530 NVMe SSD includes an output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate comprising a main driver. The Western Digital PC SN530 NVMe SSD includes a SanDisk memory chip:



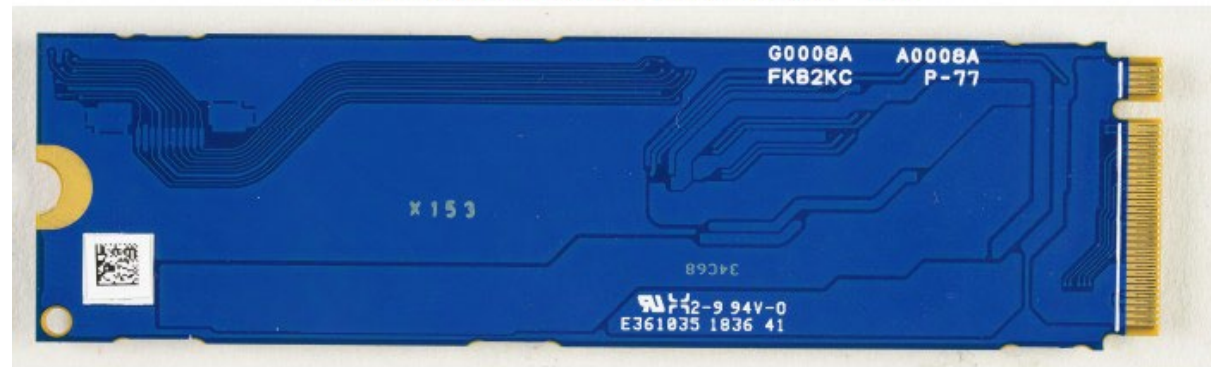
The below image shows the pin layout and corners of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD:



On information and belief, the Western Digital PC SN530 NVMe SSD is substantially similar to the Toshiba KXG60ZNV256G SSD Package (“Toshiba SSD”) for all matters relevant to this complaint. The Toshiba SSD is depicted below:



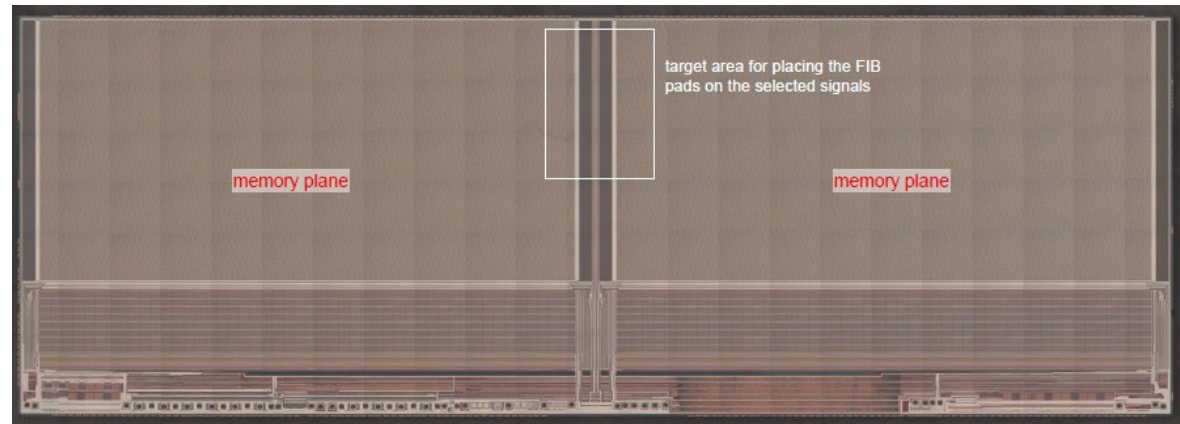
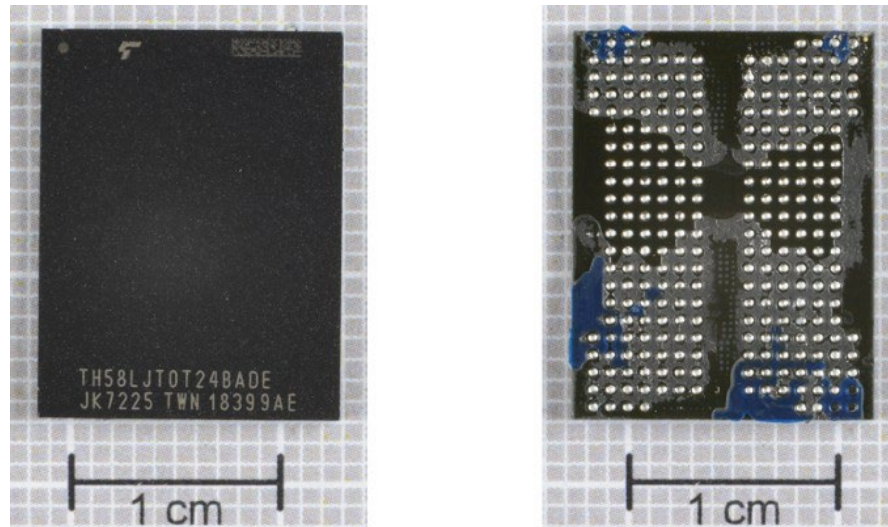
Toshiba KXG60ZNV256G SSD Package – Top



Toshiba KXG60ZNV256G SSD Package – Bottom

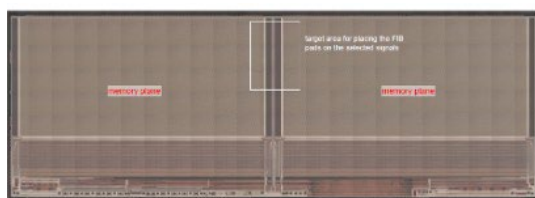
The memory chip of the Toshiba SSD, the Toshiba TH58LJT0T24BADE Package is depicted in the images below:

Exhibit B to Infringement Contentions

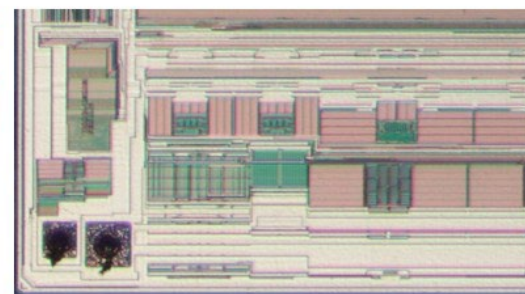
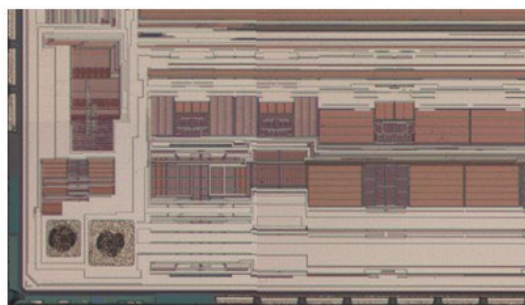
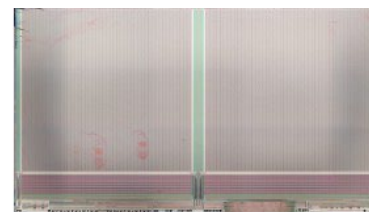


Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph

A side-by-side comparison of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package used in the Toshiba SSD is depicted below:



Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph



Based at least on the above, Longitude is informed and believes, that the corners of the dies of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package are substantially the same. Among other things, the corners are substantially the same. Accordingly, Longitude is informed and believes that the various I/Os and peripheral circuits are the same between the Toshiba and Western Digital/SanDisk chips. Furthermore, Longitude is informed and believes that Toshiba and Western Digital shared the designs for 96 layer chips. Accordingly, the SanDisk memory chip is substantially the same as the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package. For this reason, Longitude is informed and believes that technical documents and other analysis concerning the Toshiba TH58LJT0T24BADE Package also describe the layout and functionality of the Western Digital PC SN530 NVMe SSD.

The Western Digital PC SN530 NVMe SSD includes an output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate comprising a main driver:

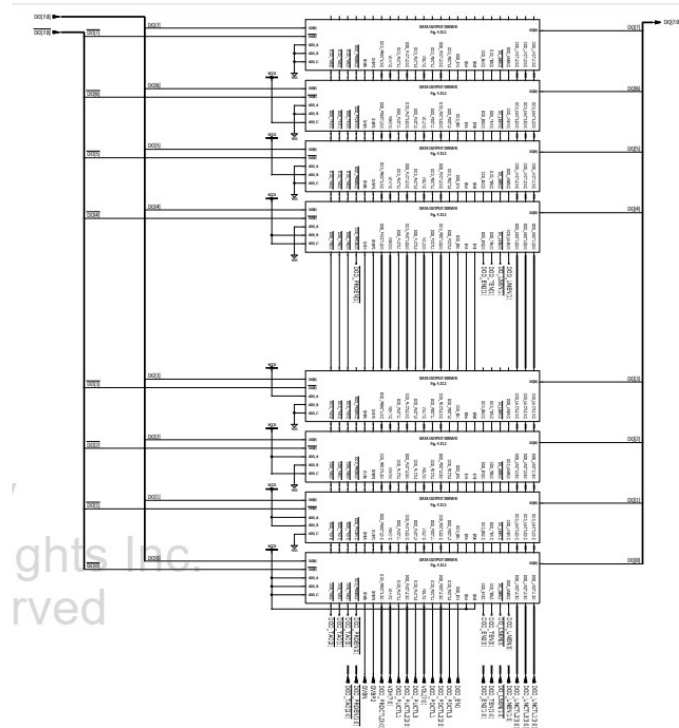


Figure 4.11 DATA OUTPUT DRIVERS

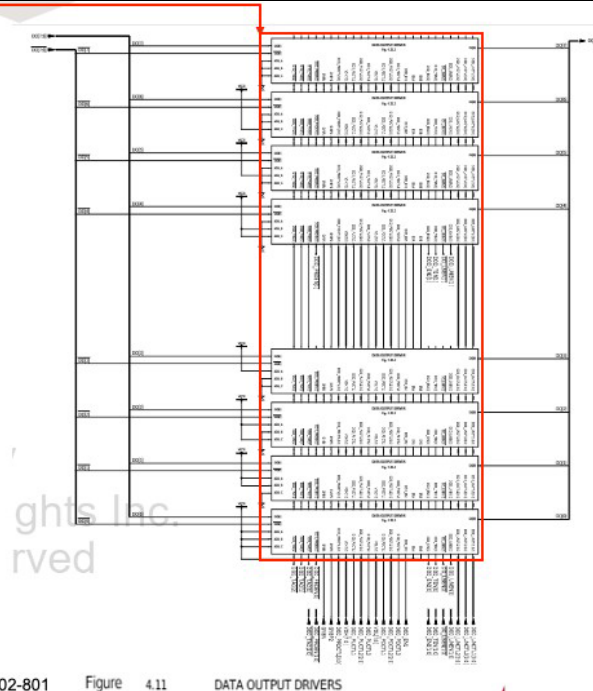
Source: TechInsights Report ID#: CAR-1902-801

1[a] a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for

The Western Digital PC SN530 NVMe SSD includes a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor :

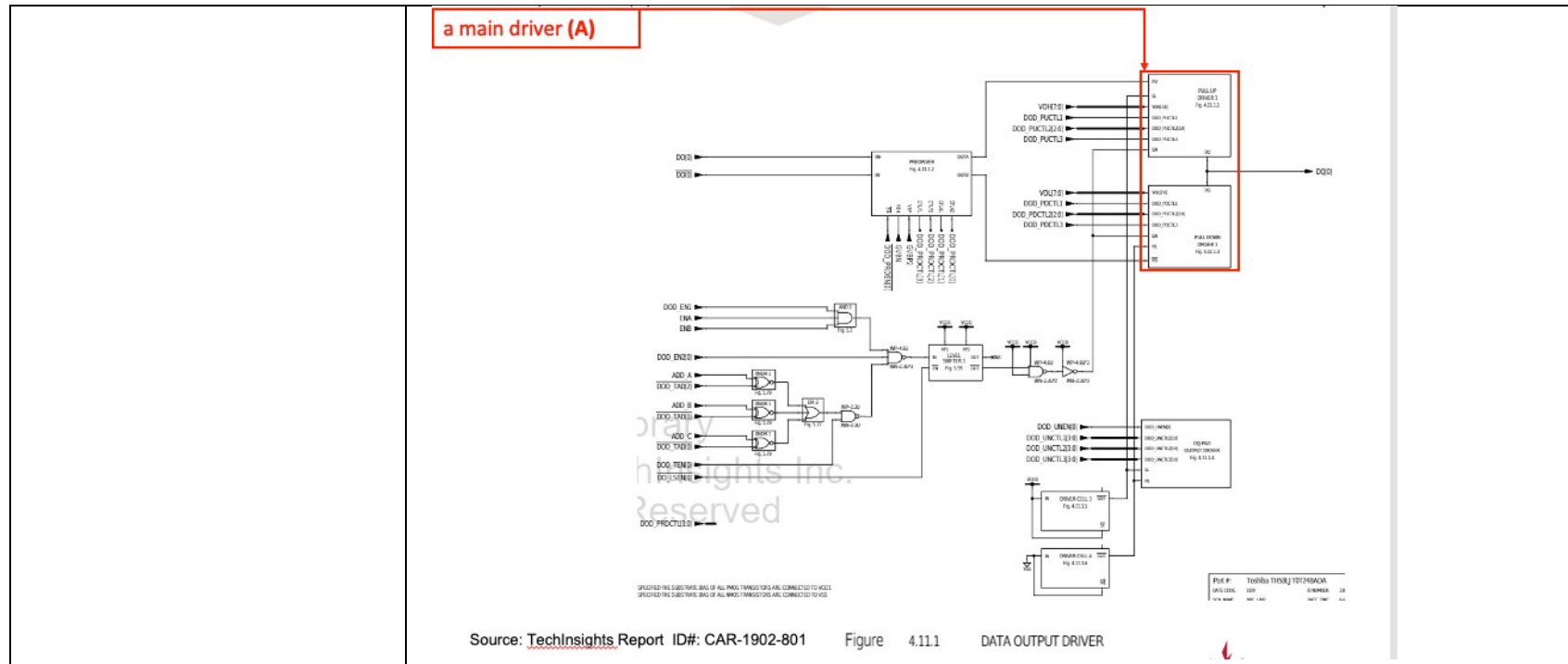
driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor;

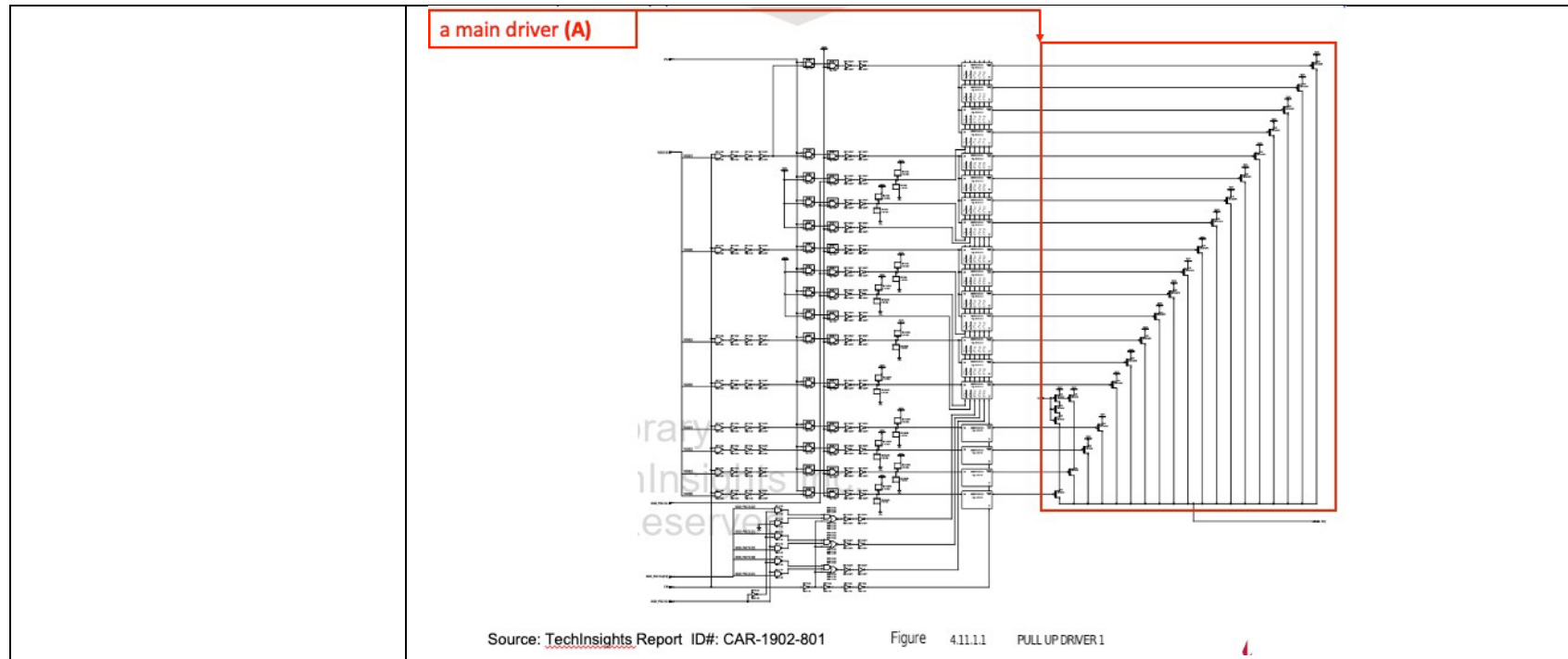
a main driver (A)

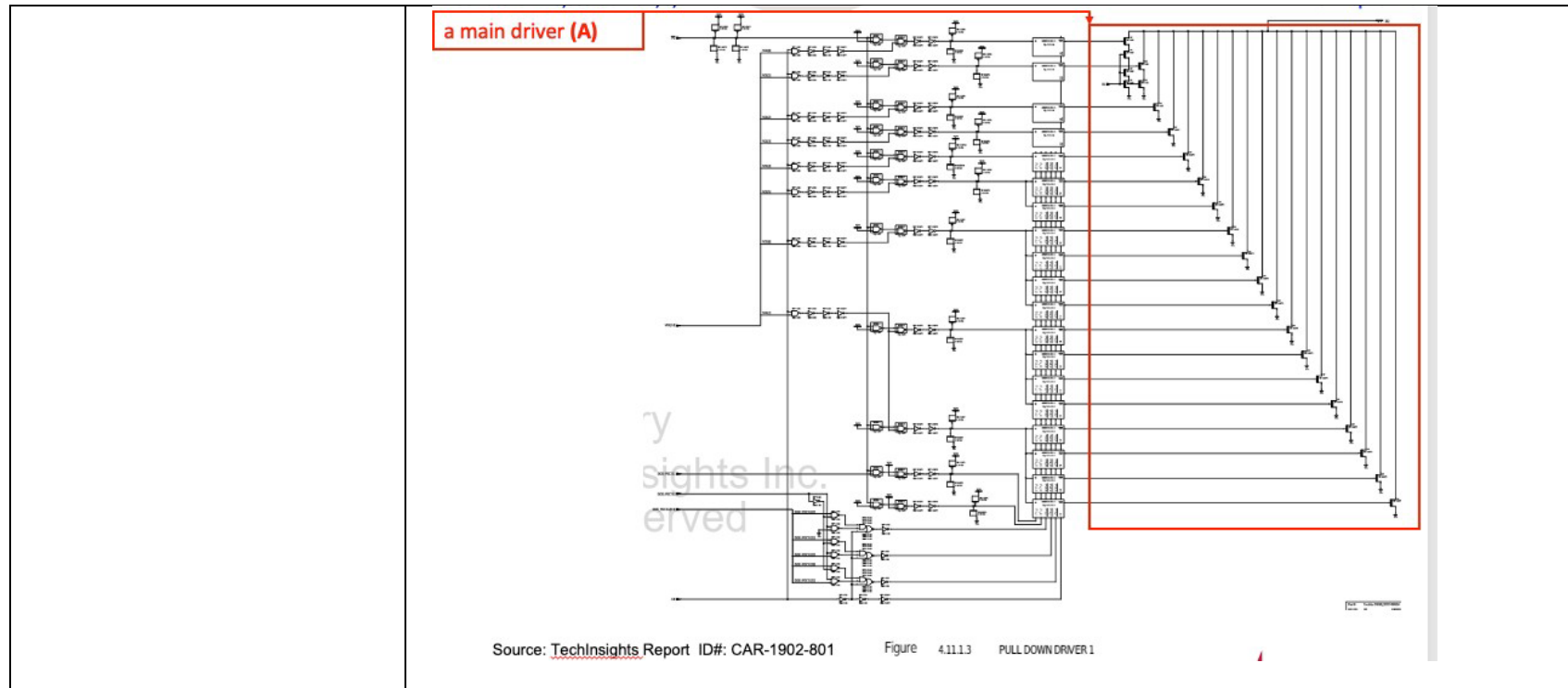


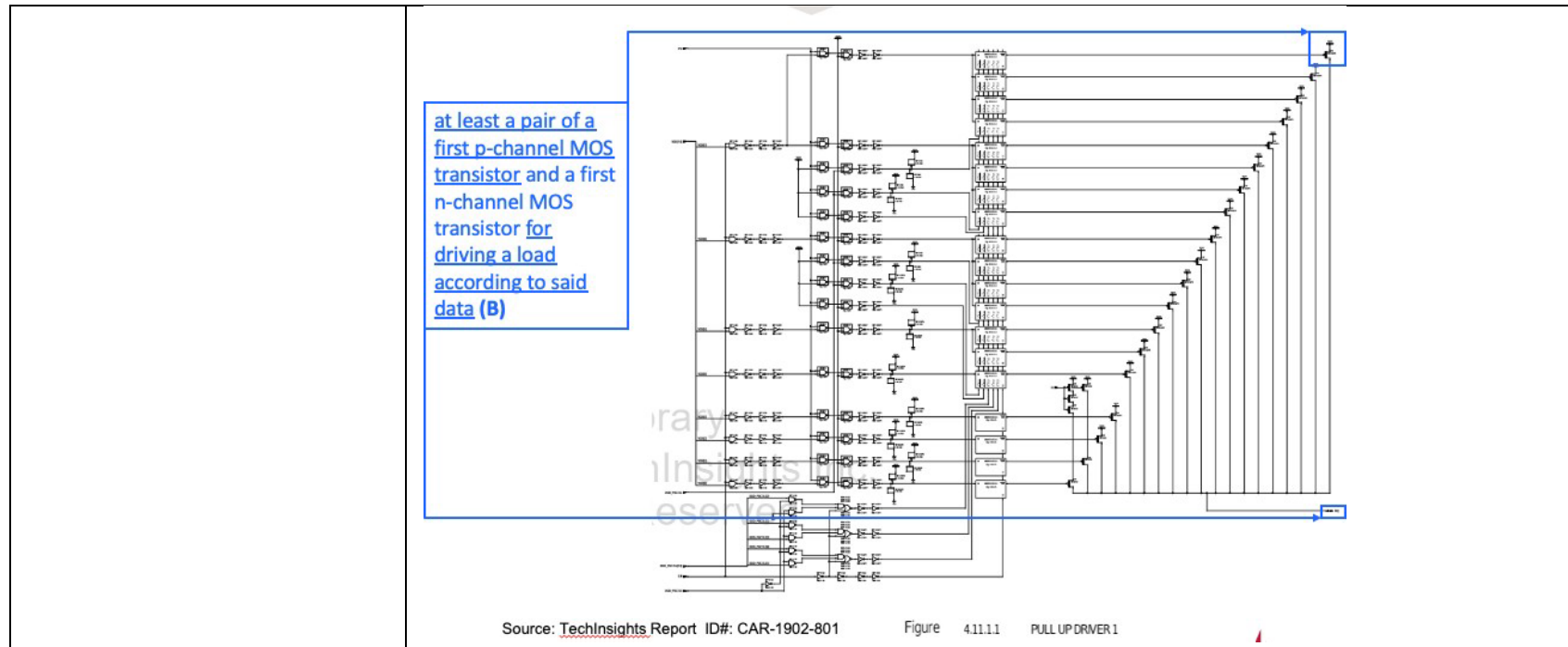
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11 DATA OUTPUT DRIVERS

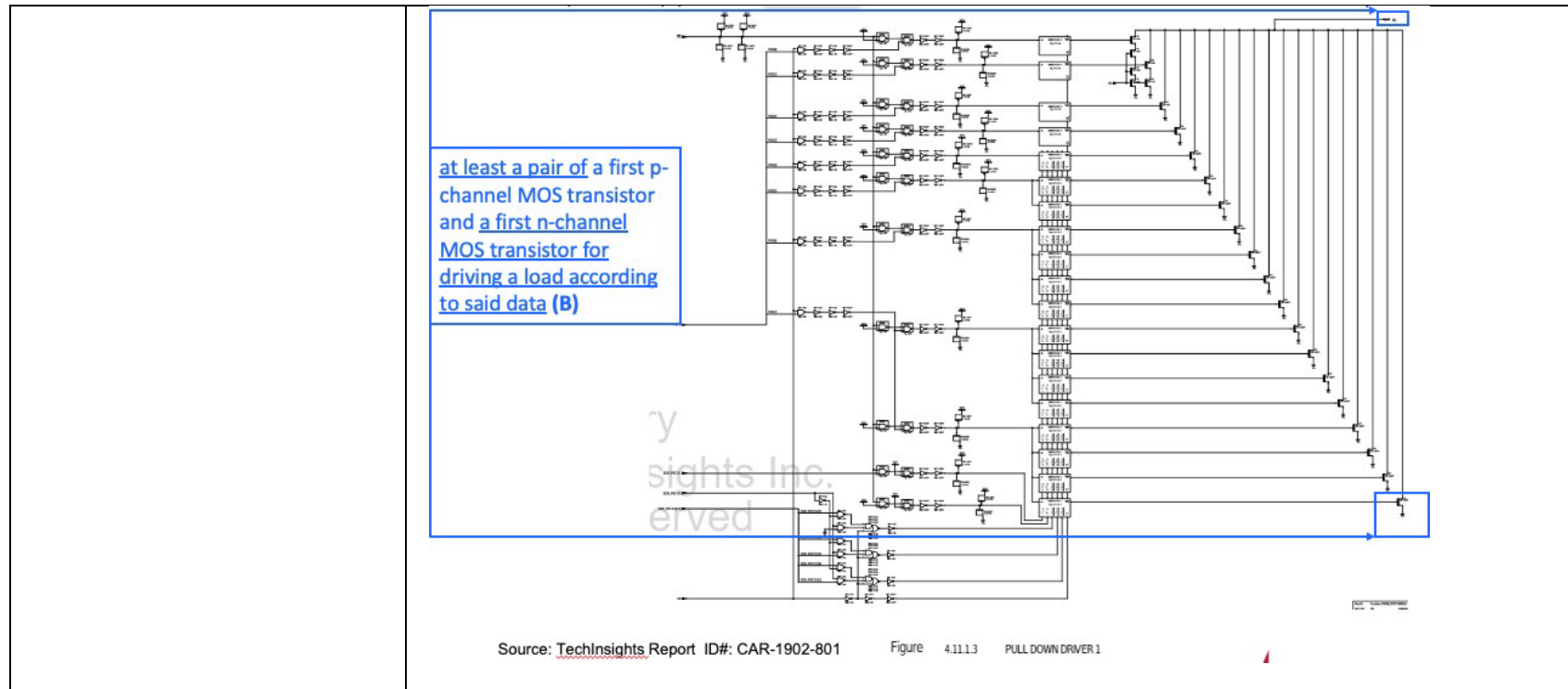
Exhibit B to Infringement Contentions



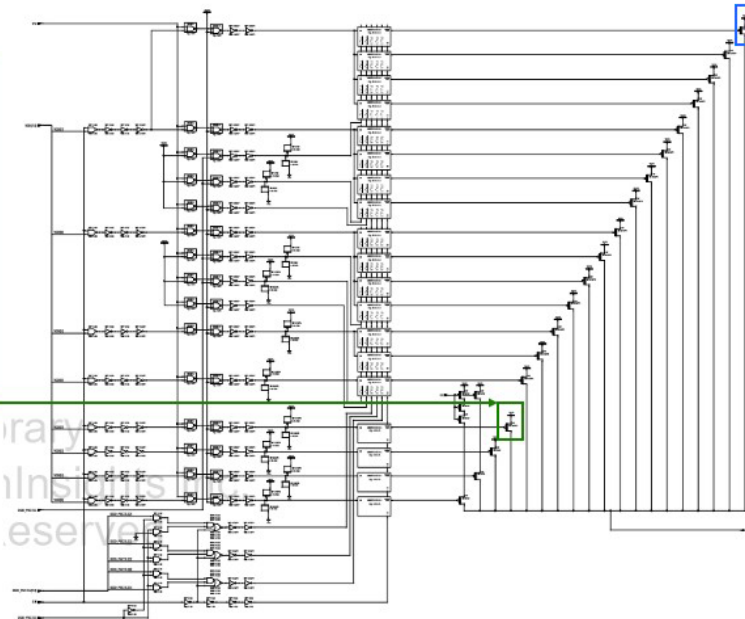






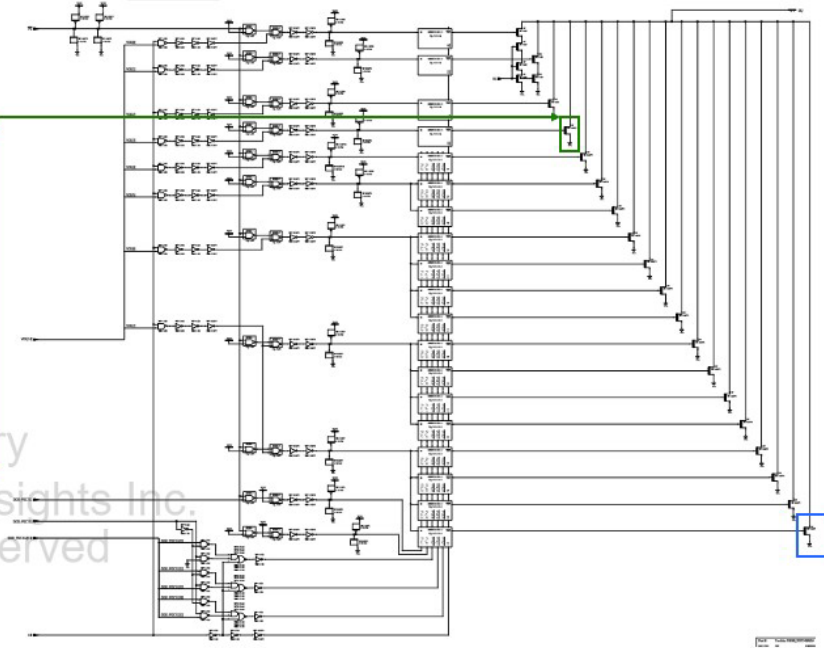


at least a pair of a
second p-channel
MOS transistor and
a second n-channel
MOS transistor for
driving said load in
coaction with said
first p-channel
MOS transistor and
said first n-channel
MOS transistor (C)



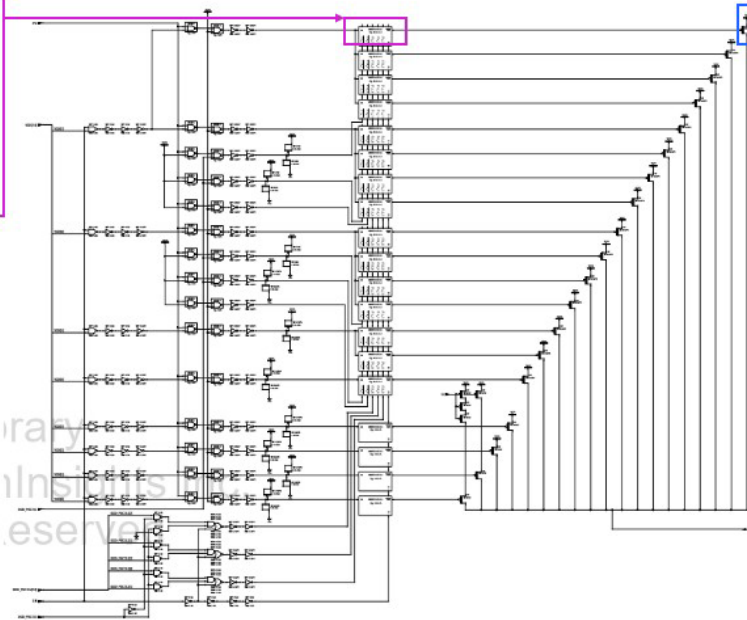
Source: TechInsights Report ID#: CAR-1902-801

Figure 4.11.1.1 PULL UP DRIVER 1

	 at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor (C) Source: TechInsights Report ID#: CAR-1902-801 Figure 4.111.3 PULL DOWN DRIVER 1
1[b] a predriver with outputs for driving only said first in-channel in channel MOS transistor and only said first p-channel MOS transistor having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor:	The Western Digital PC SN530 NVMe SSD includes a predriver with outputs for driving only said first in-channel in channel MOS transistor and only said first p-channel MOS transistor having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor:

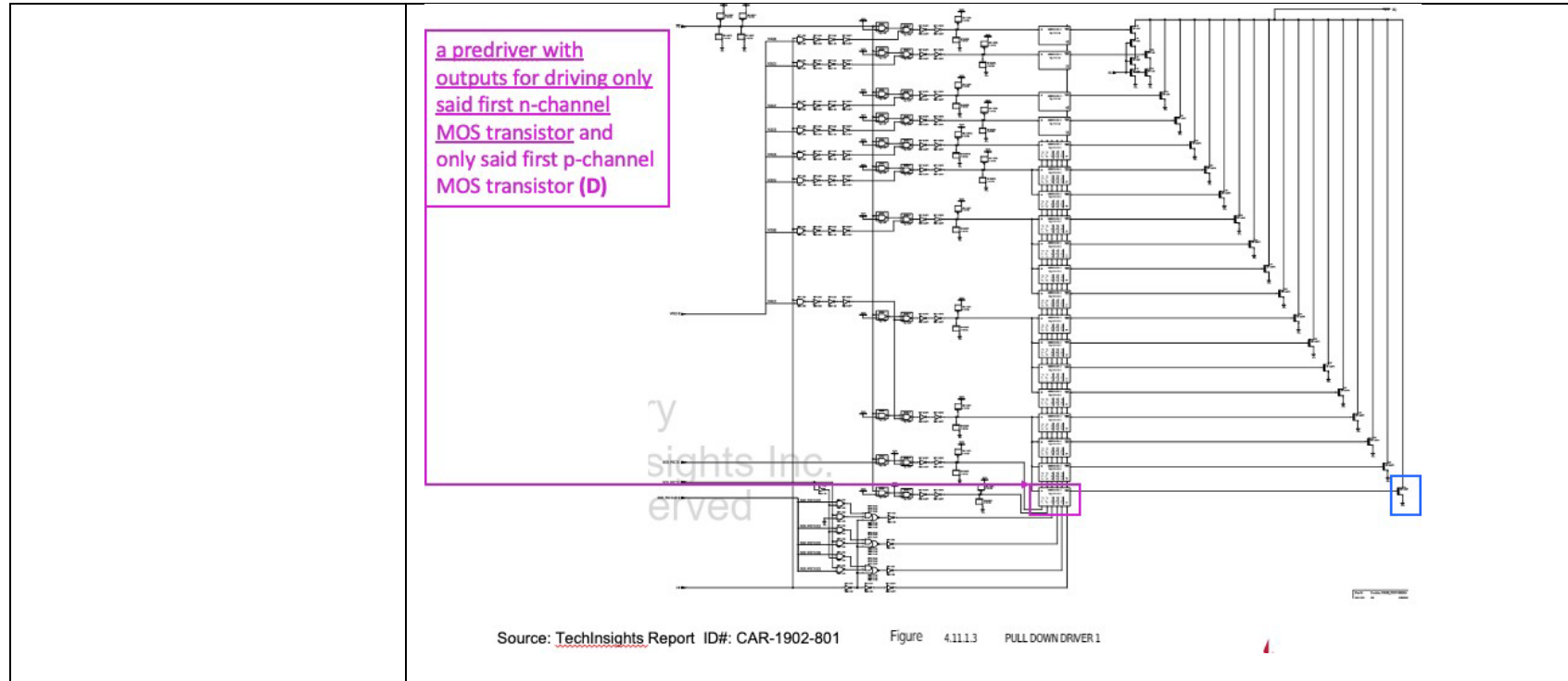
transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor; and

a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor (D)

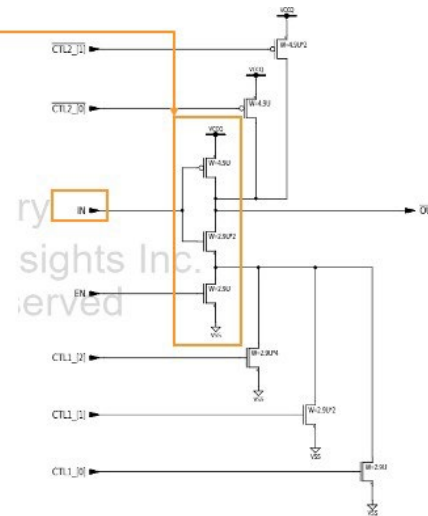


Source: TechInsights Report ID#: CAR-1902-801

Figure 4.11.1.1 PULL UP DRIVER 1

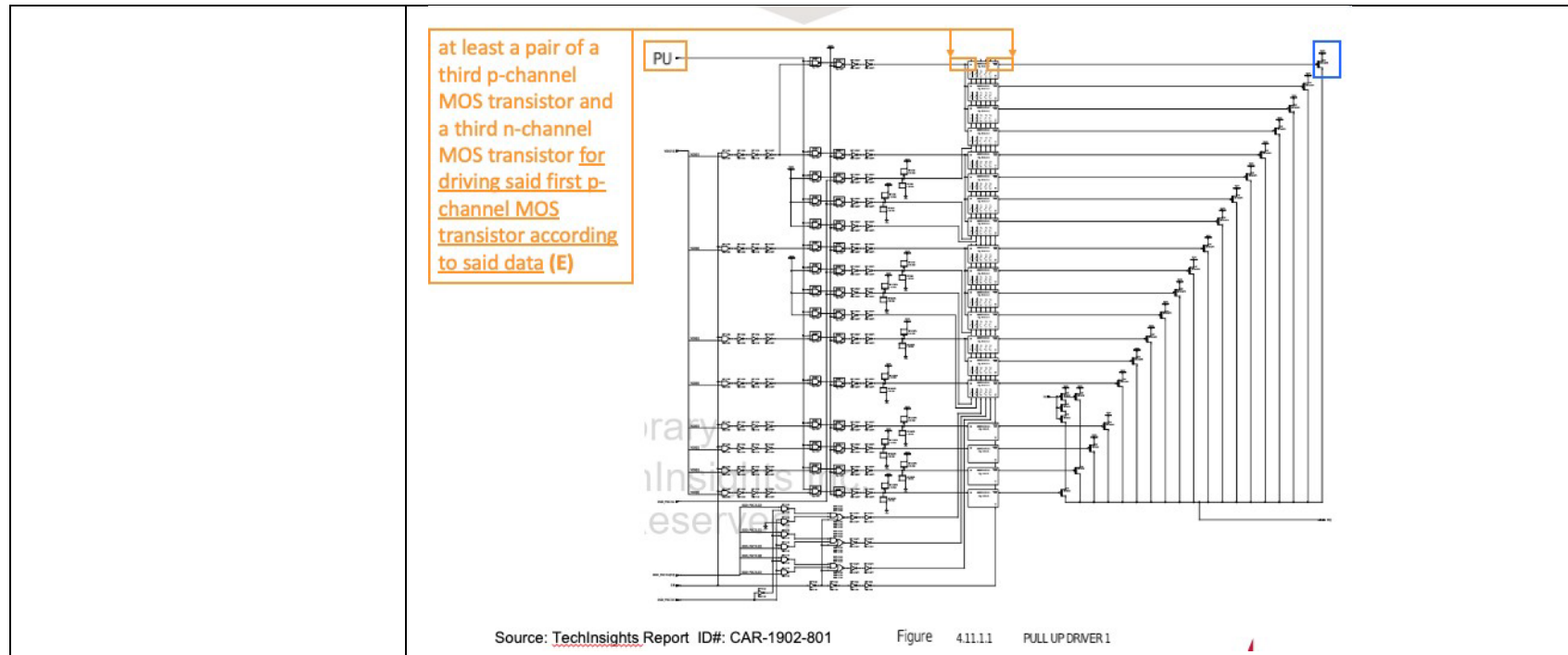


at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data (E)



Source: TechInsights Report ID#: CAR-1902-801

Figure 4.11.1.1 DRIVER CELL 1



at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data (E)

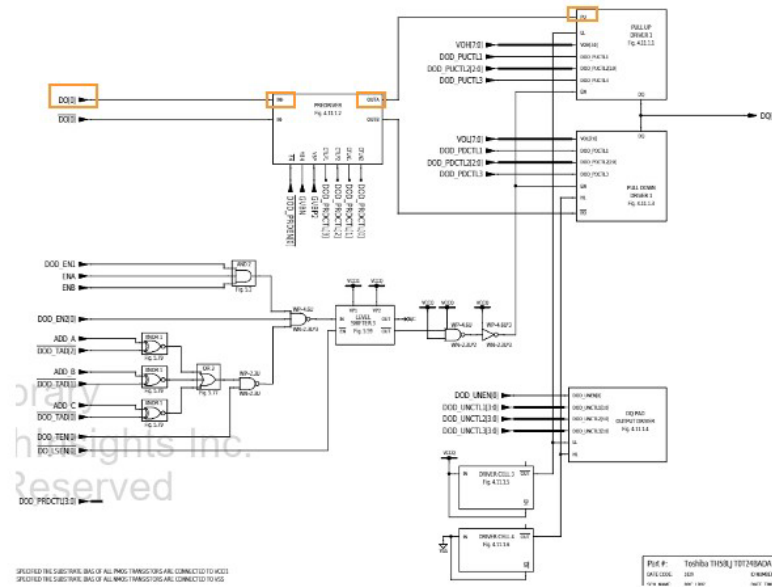
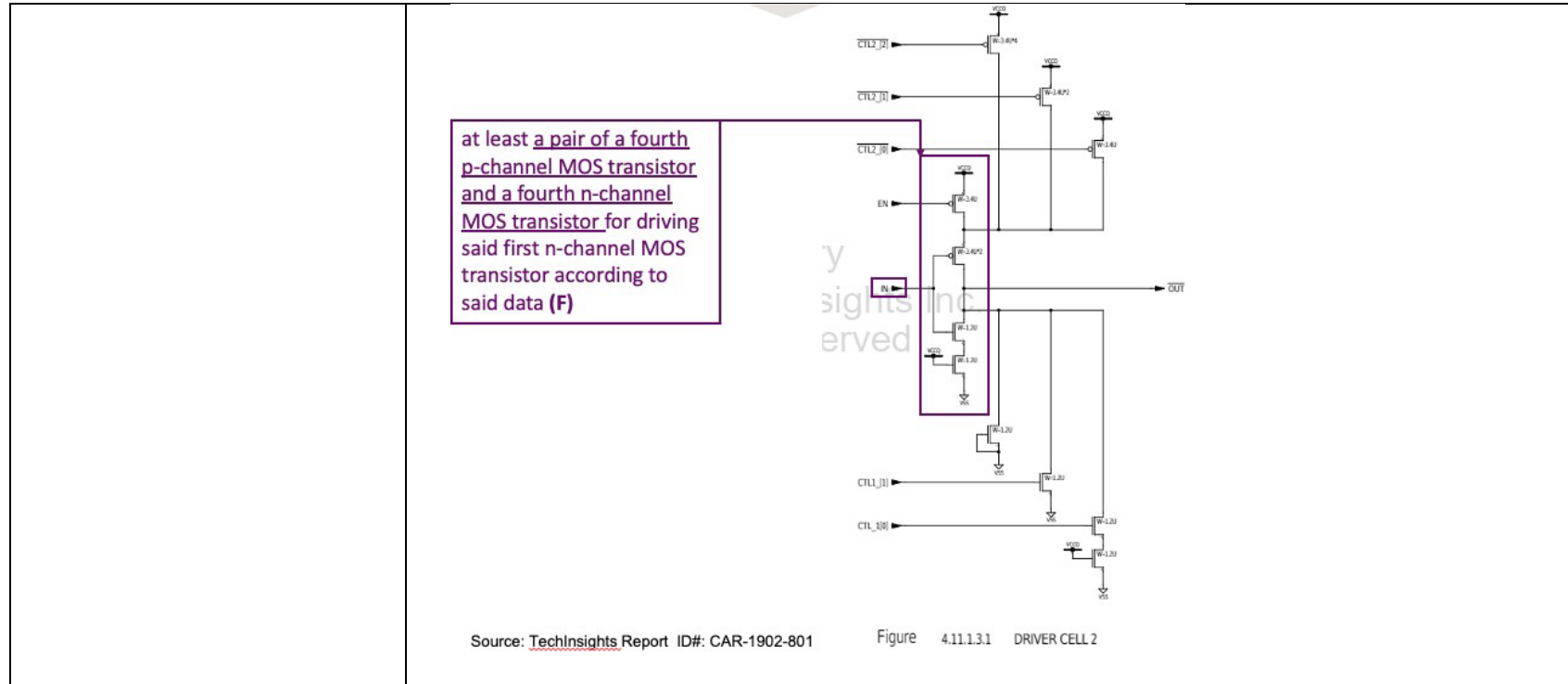
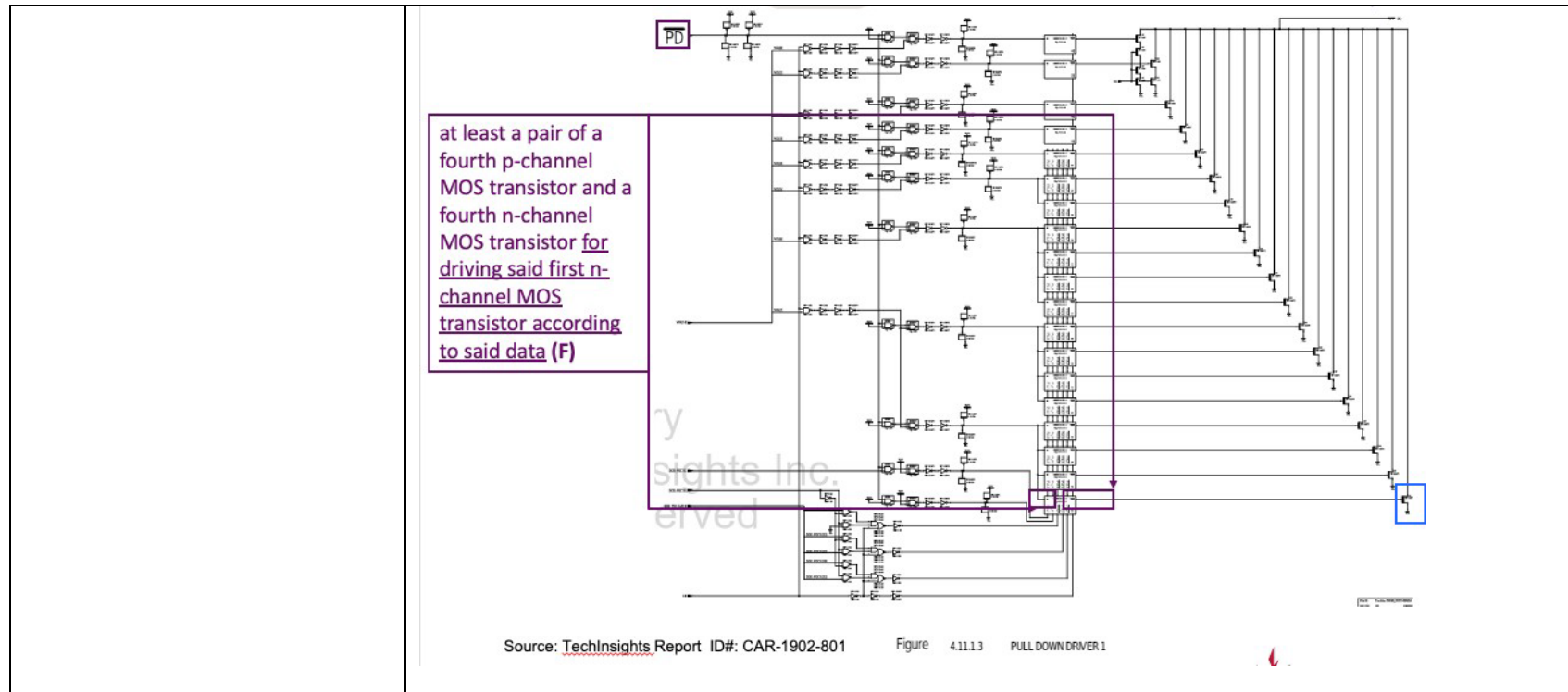
Source: TechInsights Report ID#: CAR-1902-801

Figure 4.11.1.1 PULL UP DRIVER 1





at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data (F)

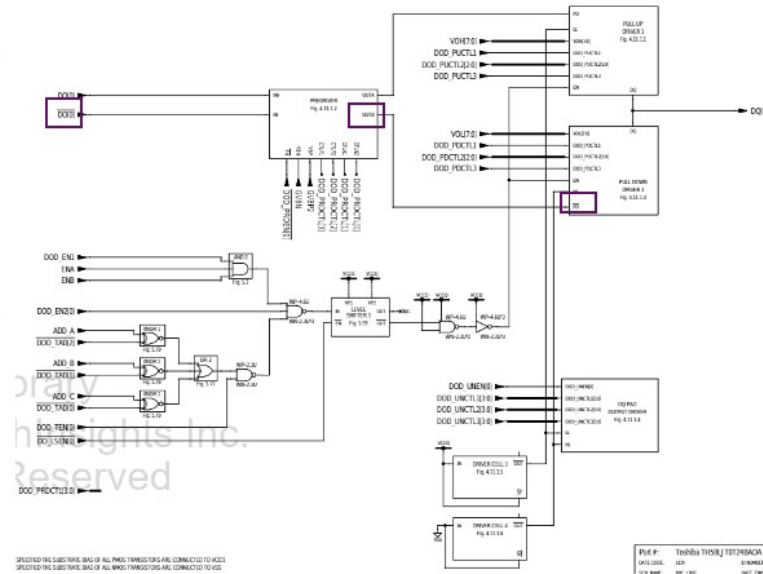
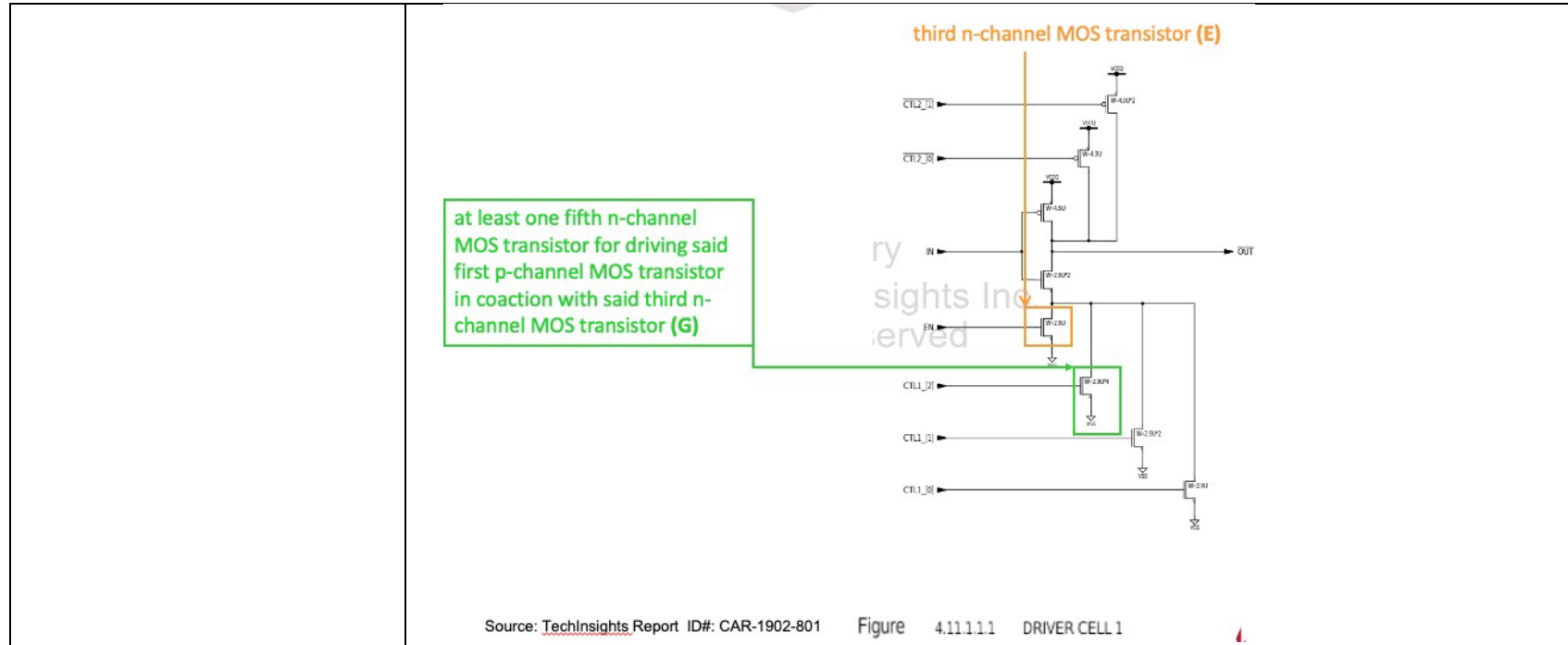
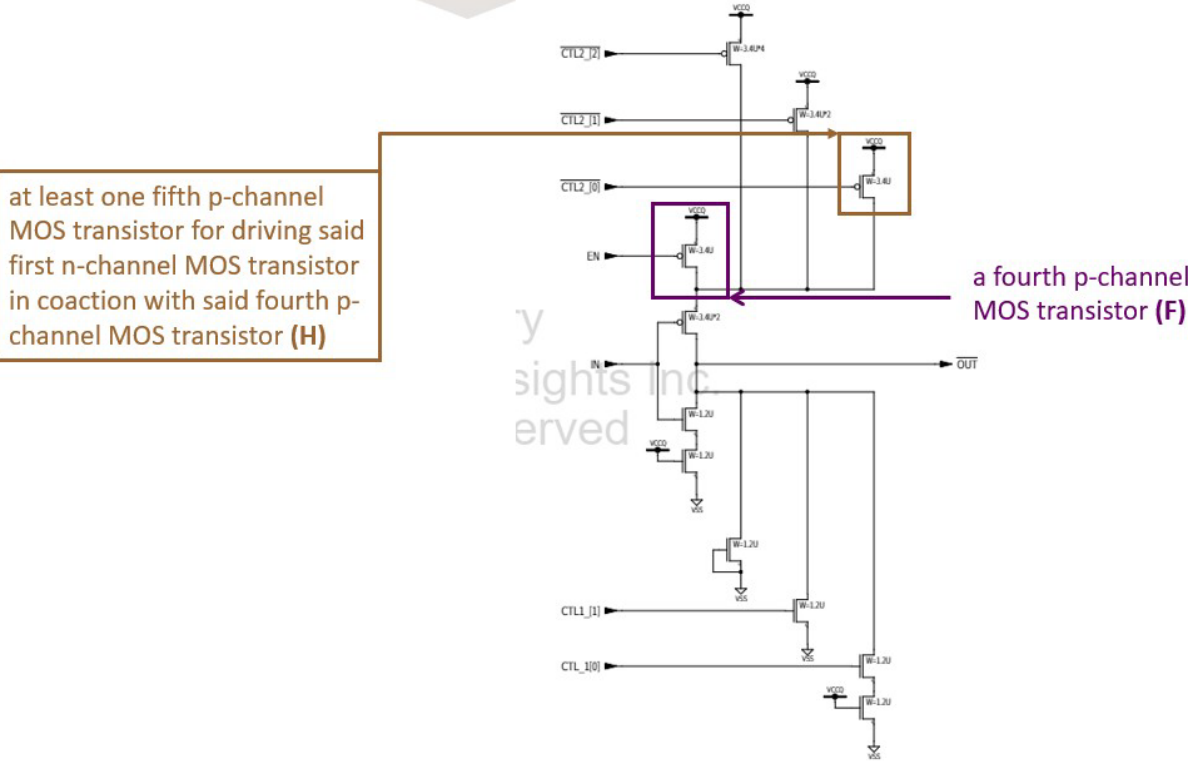
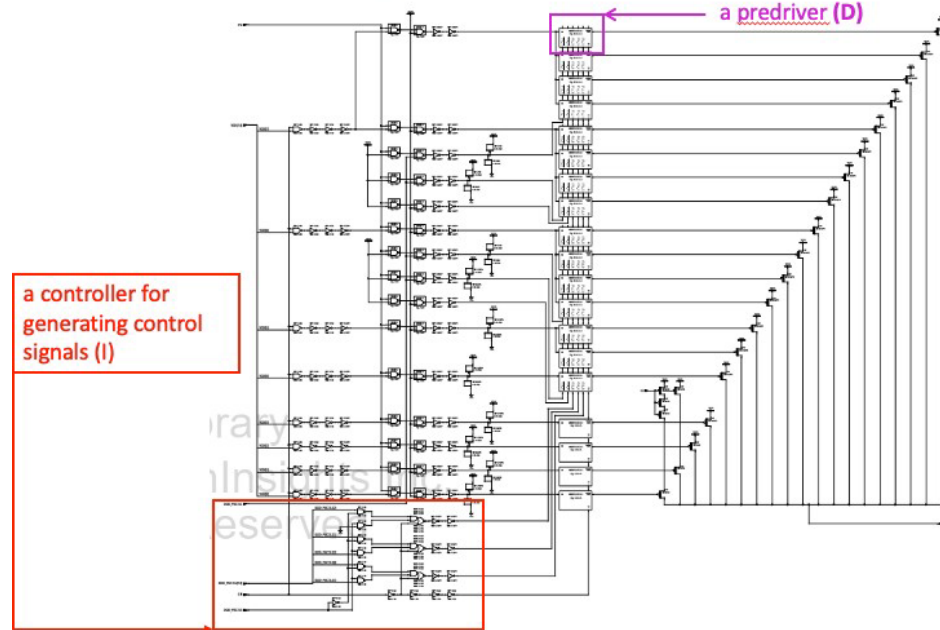
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Figure 4.11.1.1 PULL UP DRIVER 1



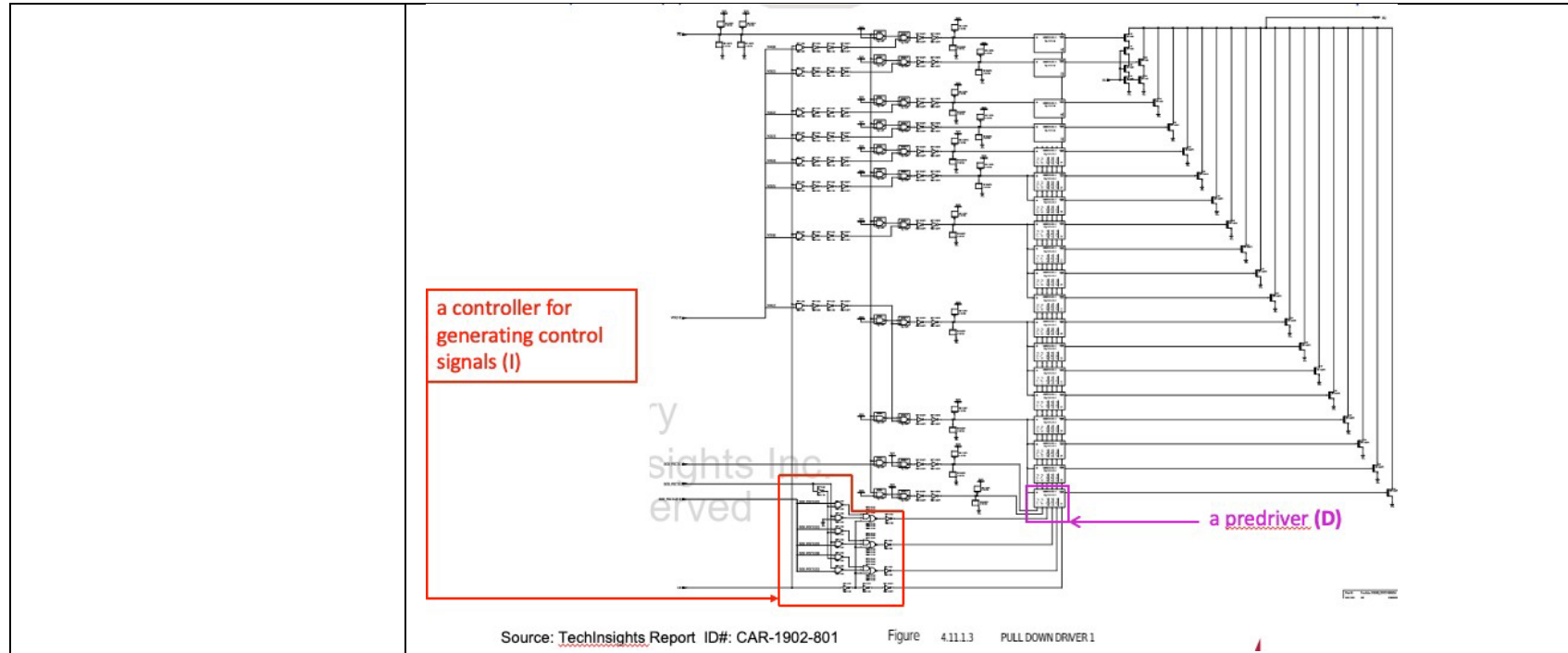
	 at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor (H) a fourth p-channel MOS transistor (F) Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3.1 DRIVER CELL 2
1[c] a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said	The Western Digital PC SN530 NVMe SSD further includes a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor:

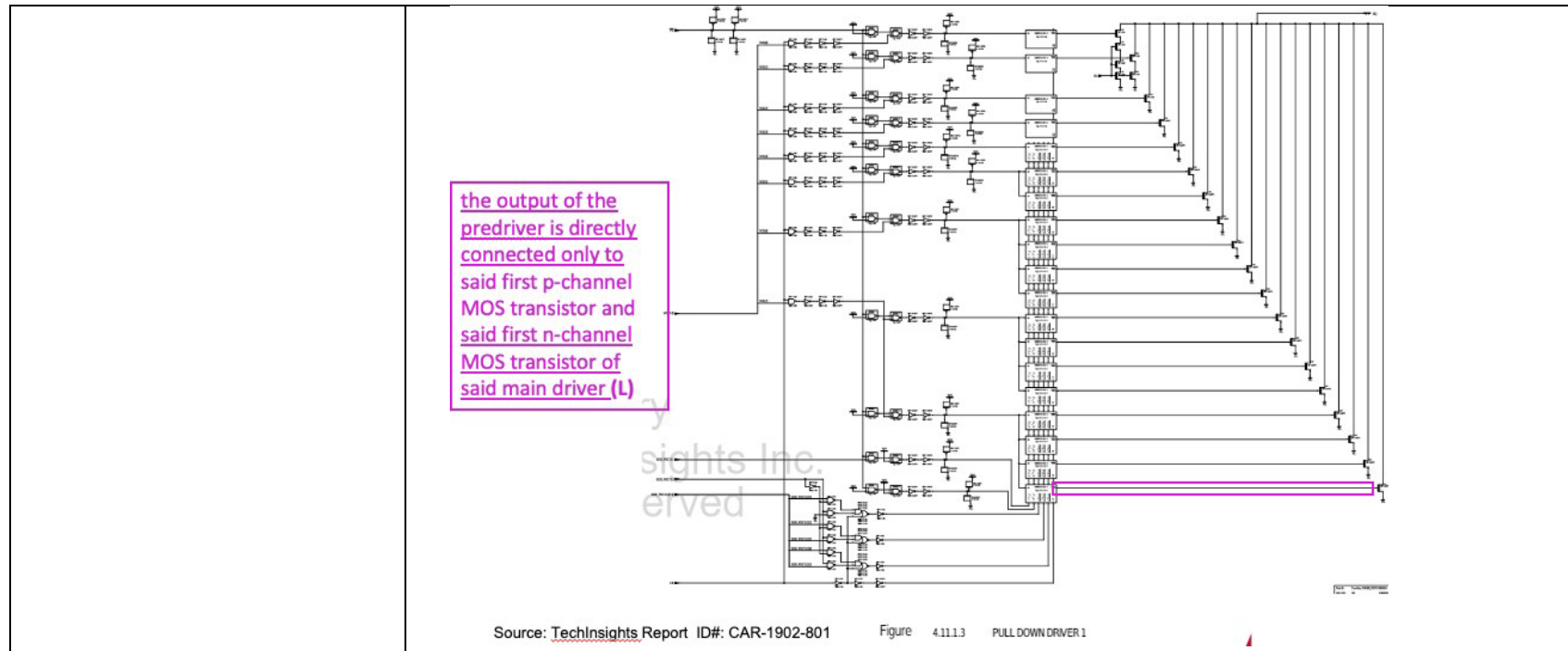
second n-channel MOS transistor,

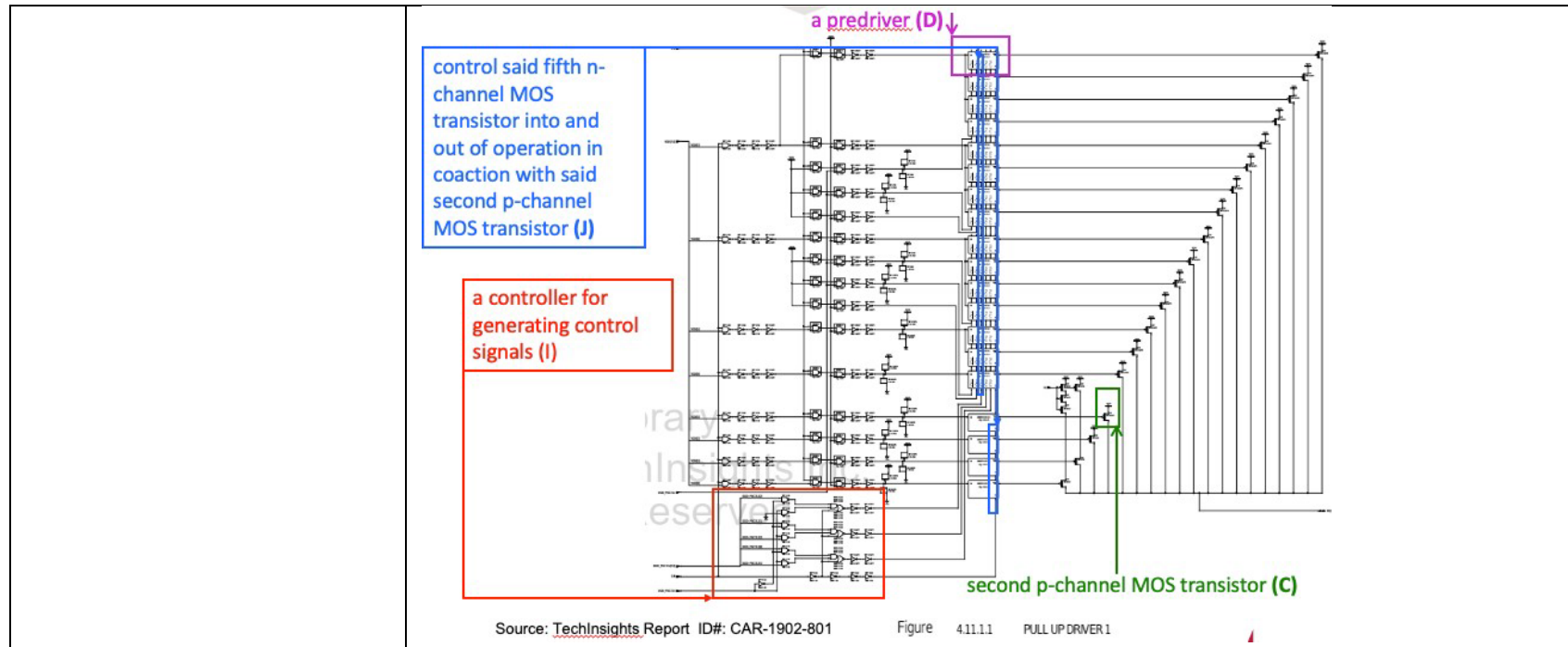


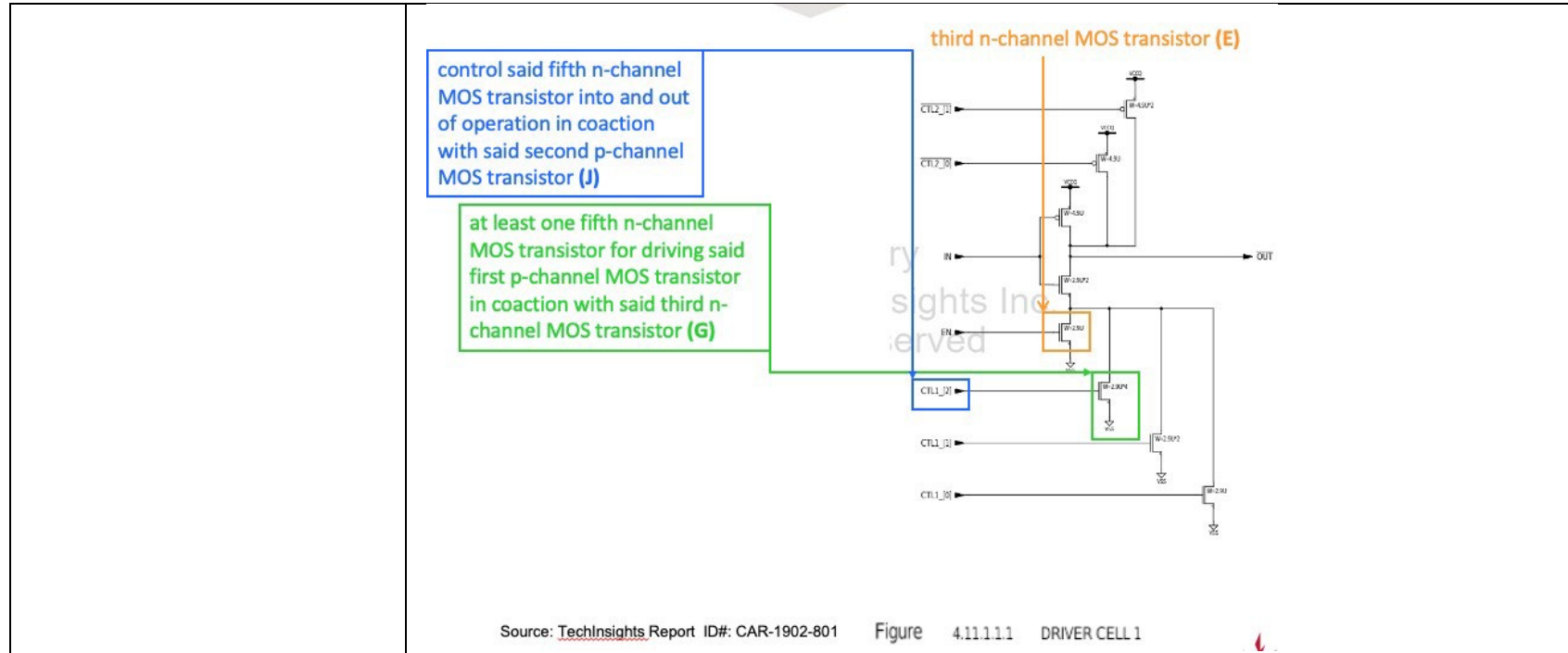
Source: TechInsights Report ID#: CAR-1902-801

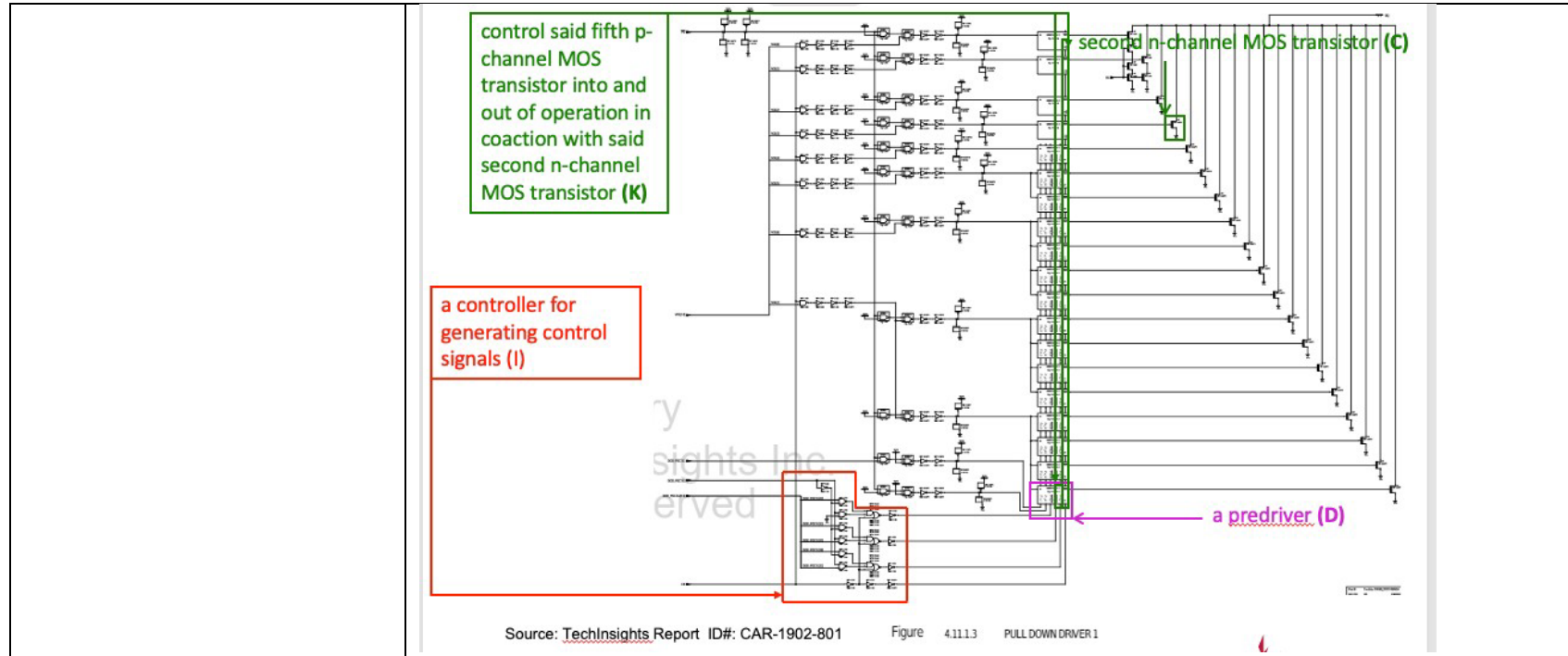
Figure 4.11.1.1 PULL UP DRIVER 1



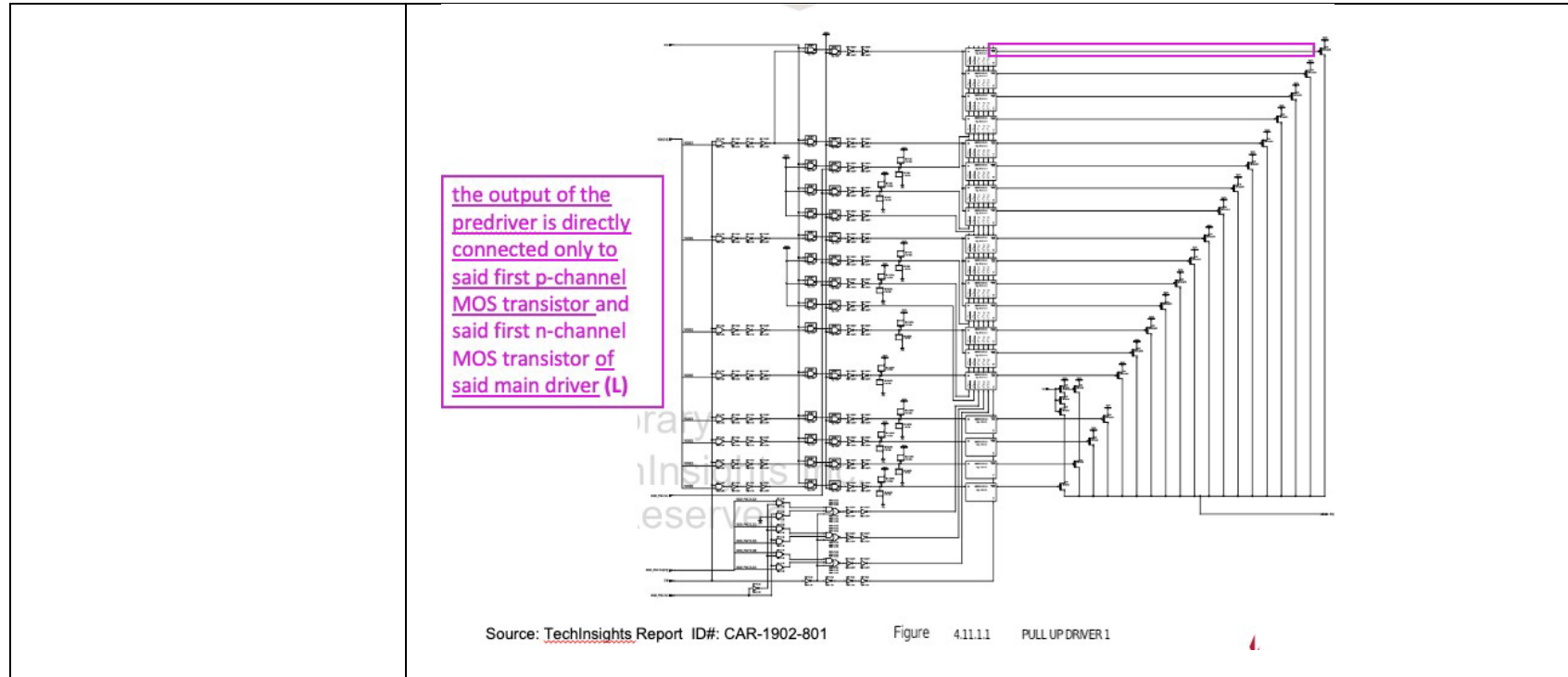


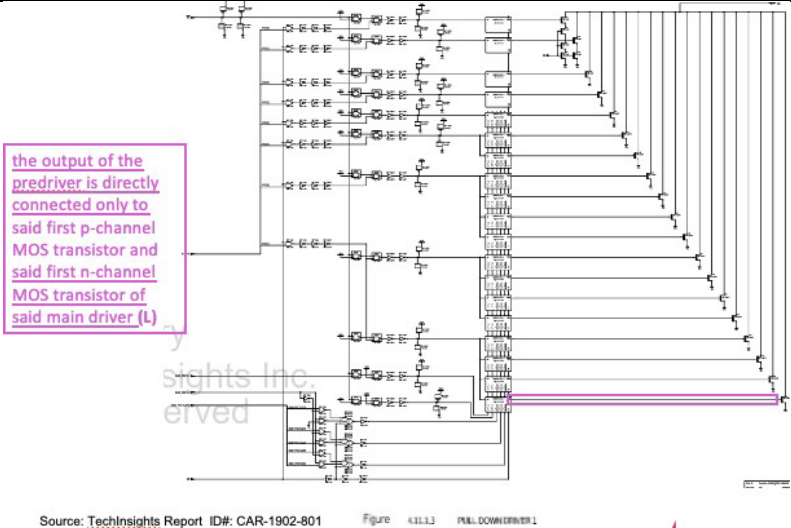




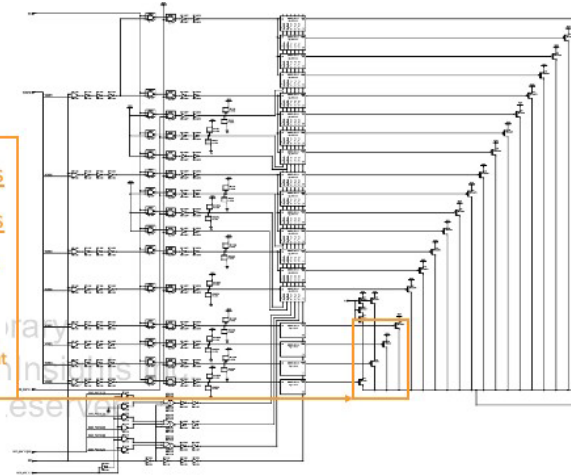


	at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor (H) control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor (K) a fourth p-channel MOS transistor (F) Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3.1 DRIVER CELL 2
1[d] wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver	The Western Digital PC SN530 NVMe SSD further includes a controller wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver:



	 the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver (L) Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PML DOWN DRIVER 1
3. The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors and said second n-channel MOS transistors and the number of said fifth n-channel MOS transistors and said fifth p-channel MOS transistors are different from each other.	The Western Digital PC SN530 NVMe SSD further includes the output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors and said second n-channel MOS transistors and the number of said fifth n-channel MOS transistors and said fifth p-channel MOS transistors are different from each other:

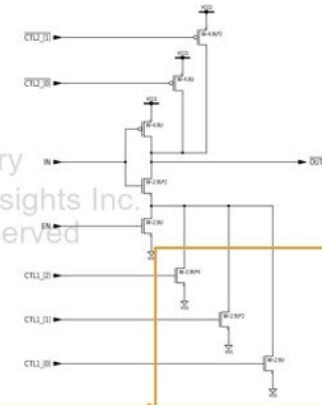
the number of said second p-channel MOS transistors and said second n-channel MOS transistors and the number of said fifth n-channel MOS transistors and said fifth p-channel MOS transistors are different from each other (M)



Source: Technisights Report ID#: CAR-1902-801

Figure 4.11.1.1 FULL UP DRIVER 1

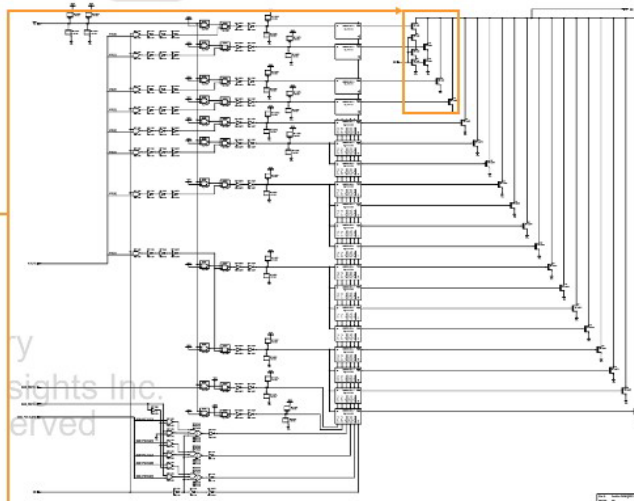
the number of said second p-channel MOS transistors and said second n-channel MOS transistors and the number of said fifth n-channel MOS transistors and said fifth p-channel MOS transistors are different from each other (M)



Source: Technisights Report ID#: CAR-1902-801

Figure 4.11.1.1 DRIVER CELL 1

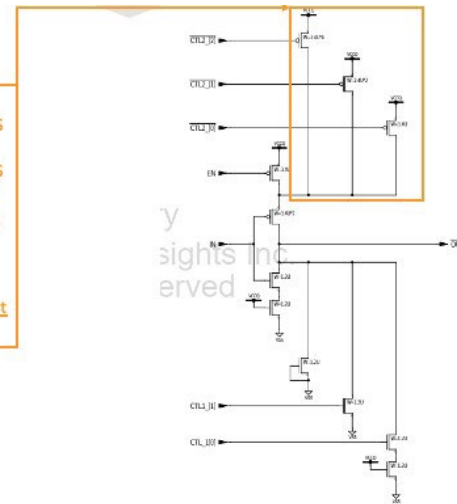
the number of said second p-channel MOS transistors and said second n-channel MOS transistors and the number of said fifth n-channel MOS transistors and said fifth p-channel MOS transistors are different from each other (M)



Source: TechInsights Report ID#: CAR-1902-801

Figure 411.13 P-channel MOSFET DRIVER

the number of said second p-channel MOS transistors and said second n-channel MOS transistors and the number of said fifth n-channel MOS transistors and said fifth p-channel MOS transistors are different from each other (M)



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Figure 411.13.1 DRIVER CELL 2

4. The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor, and have a small effect on rise and fall times of pulses output from said main driver.

The Western Digital PC SN530 NVMe SSD further includes the output buffer circuit according to claim 1, wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor, and have a small effect on rise and fall times of pulses output from said main driver:

