

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

Case IPR2023-01286
U.S. Patent No. RE43,539

PATENT OWNER'S RESPONSE TO THE PETITION

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TABLE OF AUTHORITIES

Cases

<i>Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.</i> , 289 F.3d 801 (Fed. Cir. 2002)	10, 13
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PATENT OWNER'S EXHIBIT LIST

No.	Description
2001	Listing of possible size values for device size and gate width for each of four transistors P1, N1, P2, and N2
2002	January 10, 2024 Disclaimer of Claims 1-3 and 5-12 of U.S. Patent No. RE43,539
2003	Declaration of Brian D. Ledahl in Support of Motion for <i>Pro Hac Vice</i> Admission
2004	Declaration of Paul A. Kroeger in Support of Motion for <i>Pro Hac Vice</i> Admission
2005	Declaration of Dr. Bruce Jacob in Support of Patent Owner's Response
2006	May 15, 2024 Deposition Transcript of Scott E. Thompson, Ph.D.

I. Introduction

As set forth in Ex. 2002, Patent Owner has disclaimed all challenged claims other than claim 4 of the '539 Patent.

The Petition's sole challenges to claim 4 rely on a combination of two embodiments with Itoh. However, claim 4 requires (due to its dependency on claim 1) an "output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance." This preamble is limiting, at least because it provides antecedent basis to other claim limitations (e.g., "said data" as recited in claim 1).

Despite the limiting nature of the preamble, the Petition identifies no "predetermined output impedance" at which "data in the form of an input pulse train" is output. Instead, Petitioner's expert acknowledges that the pulse train that is output by the combination the Petition relies on to satisfy claim 4 is output at two *different* output impedances, contrary to the plain meaning of the claim language which requires the pulse train to be output at a *predetermined* output impedance. Accordingly, claim 4 of the '539 Patent should be found not unpatentable.

II. Background

A. Western Digital's Petition

Petitioner Western Digital Technologies, Inc. (“Petitioner” or “Western Digital”) challenges claims 1-12 of the '539 Patent. The Petition's six asserted grounds for unpatentability are structured as follows:

- Ground 1: Obviousness of claims 1-3 and 5-7 over Itoh and Skorup.
- Ground 2: Obviousness of claims 1-8 over Itoh.
- Ground 3: Obviousness of claims 1-8 over Itoh in view of Muljono.
- Ground 4: Obviousness of claims 9-12 over Itoh in view of Skorup and Borkar.
- Ground 5: Obviousness of claims 9-12 over Itoh in view Borkar.
- Ground 6: Obviousness of claims 9-12 over Itoh in view of Muljono and Borkar.

Only Grounds 2 and 3 challenge claim 4 of the '539 Patent. Because Patent Owner has disclaimed all challenged claims of the '539 Patent other than claim 4, those Grounds 2 and 3 of the Petition are the only remaining grounds the Board need decide in this proceeding.

However, neither of Grounds 2 or 3 provide any theory under which the output pulses output from the claimed “output buffer circuit” would be provided at a “predetermined output and slew rate” as required by claim 4 of the '539 Patent. Instead, as Petitioner's expert admitted, in the Petition's combination that forms the basis for both Grounds 2 and 3, “the output impedance change[s]” during operation,

such that the output pulses are provided at a ***variable*** output impedance, not a ***predetermined*** output impedance as the claim requires.

B. Overview of the '539 Patent

The '539 Patent is directed generally to an output buffer circuit for outputting a train of pulses at a predetermined slew rate and output impedance. *See* Ex. 1001 at Claim 1, preamble (reciting an “output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate”). A POSITA would understand that, in the context of the '539 Patent, the output impedance and slew rate are “predetermined” with respect to a given “pulse train” that is output from the output buffer circuit. *See* Ex. 2005 at ¶107.

The specification teaches that in the prior art, there was “an arrangement for adjusting ***either*** one of the output impedance and the slew rate” (Ex. 1001 at 2:18-20)¹, and solves the problems resulting from this approach by providing a system which can “***simultaneously*** adjust... the slew rate as well as the output impedance with the ***same*** control signals.” *Id.* at 3:14-19 (“With the above arrangement, the number of transistors of the main driver of the main driver... and the number of transistors of the predriver are automatically changed to ***simultaneously adjust... the slew rate as well as the output impedance with the same control signals.***”). The

¹ Emphases herein have been added unless otherwise specified.

'539 Patent discloses an important benefit to controlling both the output impedance and slew rate simultaneously with the same control signals:

Since the output impedance and the rise and fall times of output pulses are simultaneously controlled, the number of control signals and the steps of a testing process are made smaller than if the output impedance and the rise and fall times of output pulses were controlled independently of each other. Thus, the manufacturing cost of the output buffer circuit is prevented from increasing.

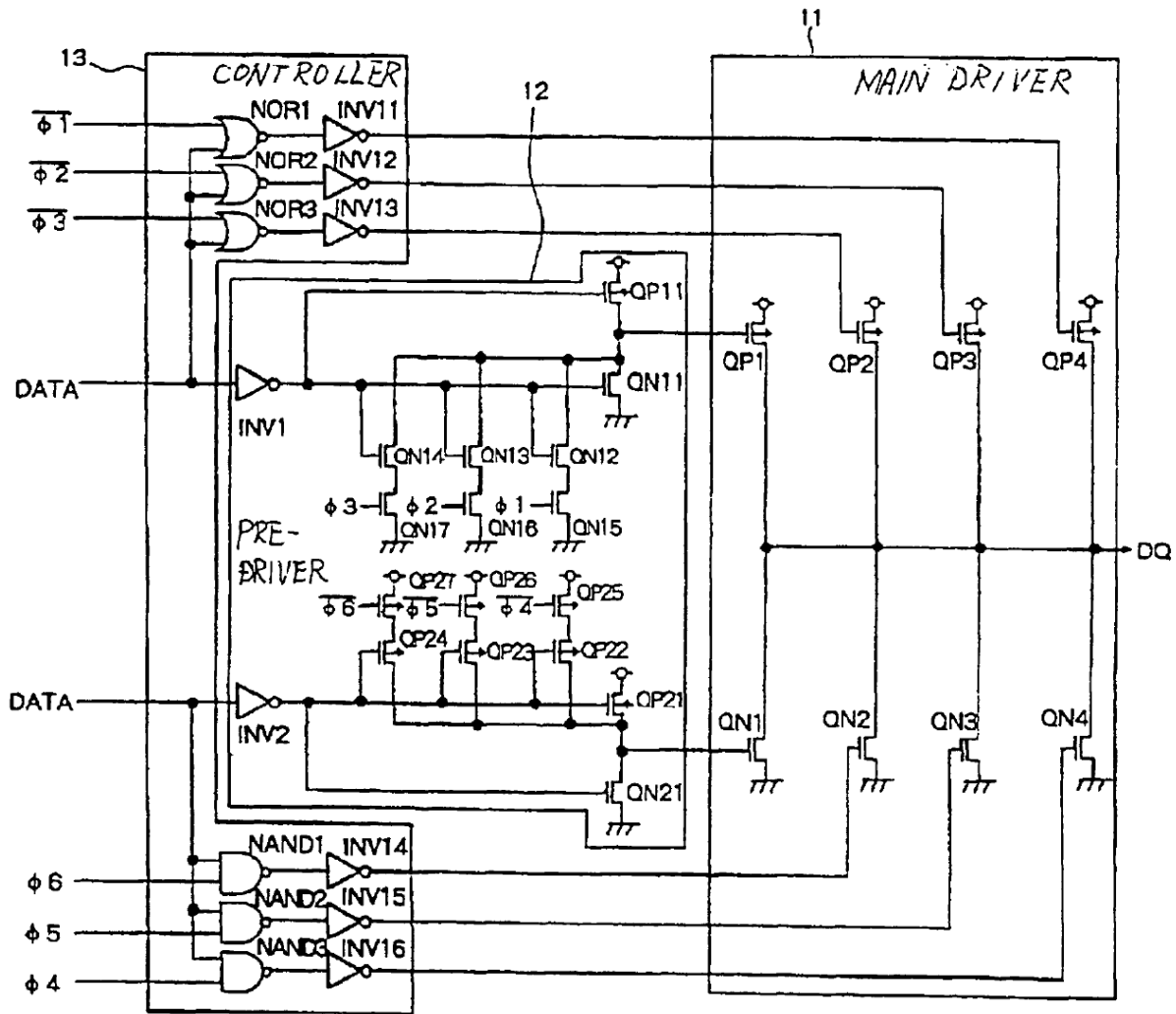
Ex. 1001 at 3:24-30.

The '539 Patent teaches that this simultaneous control of slew rate and output impedance is accomplished by enabling or disabling transistors such as the second p-channel and n-channel MOS transistors QP2 and QN2 to arrive at the predetermined slew rate and output impedance values:

pMOS transistors QP2 through QP4 as well as pMOS transistor QP1 drive the load connected to DQ terminal to adjust the output impedance when high-level data is output from main driver 11. nMOS transistors QN2 through QN4 as well as nMOS transistor NP1 drive the load connected to DQ terminal to adjust the output impedance when low-level data is output from main driver 11.

pMOS transistors QP2 through QP4 and nMOS transistors QN2 through QN4 comprise transistors having a small device size (a narrow gate width) whose effect on the [slew rate] of output pulses is smaller than pMOS transistor QP1 and nMOS transistor QN1.

Ex. 1001 at 6:28-40. A POSITA would understand that transistor pairs (such as QP2 and QN2) can be enabled or disabled depending on what output impedance and slew rate are desired, and that that selection of which transistor pairs to enable is based on control signals ϕ_1 through ϕ_N . *See* Ex. 1001 at 5:51-54 (“The circuit for monitoring the delay in output buffer circuit 8 has its output impedance and slew rate controlled... by control signals ϕ_1 through ϕ_N , $/\phi_1$ through $/\phi_N$”); *id.* at 5:65-6:1 (discussing “a controller 13 for generating signals to change the output impedance of main driver 11 and the [slew rate] of output pulses according to control signals ϕ_1 through ϕ_6 from a control circuit, etc.”); *id.* at FIG. 3 (depicting transistor pairs QP2/QN2 being enabled or disabled based on control signals ϕ_3 and ϕ_6 , which a POSITA would have understood would have the same value and thus would have enabled or disabled both QP2 and QN2 as a pair).



Ex. 1001 at FIG. 3.

The '539 Patent further shows that transistors QP2 and QN2 affect the slew rate of the output signal due to their device size (which the Board construed to be synonymous with “gate width”—see Paper No. 9 at 26). Specifically, as Petitioner’s expert testified, “impedance and resistance are... proportional to gate width.” Ex. 2006 at 23:7-13; *id.* at 24:14-16 (“[W]idth is the key knob that a circuit designer users to control how much current a transistor has, which translates into its

impedance.”). The formulas for output impedance are known, and the end result is that when QP2 or QN2 is turned on “[o]utput impedance is reduced” (*id.* at 24:17-25:21) compared to when they are off, but their effect on the overall output impedance would be less than QP1 or QN1’s effect on output impedance. *See* 2005 at ¶¶60-69.

Similarly, a POSITA would understand that a smaller device size (and higher impedance value) of transistors QP2 and QN2 would have a relatively small impact on slew rate, relative to QP1 and QN1. *Ex.* 2005 at ¶¶70-71; *Ex.* 1001 at 6:36-40 (“pMOS transistors QP2 through QP4 and nMOS transistors QN2 through QN4 comprise transistors having a small device size (a narrow gate width) whose effect on the [slew rate]² of output pulses is smaller than pMOS transistor QP1 and nMOS transistor QN1.”).

² Both parties agree that slew rate means “the rate of change of the output voltage versus time.” *Ex.* 2006 at 14:8-16 (Dr. Thompson stating that “[t]he slew rate is the rate of change of the output voltage versus time”); *Ex.* 2005 at 61 n.3. This is also consistent with the disclosure of the ’539 Patent. *See* *Ex.* 1001 at FIG. 6 (depicting slew rate in terms of units of voltage over time (e.g., “1.46v/ns”). The ’539 Patent additionally refers to the “ratio tr/tf... of output pulses” as referring to slew rate. *See, e.g.,* *Ex.* 1001 at 7:59 (referring to “the ratio tr/tf (slew rate) of output pulses”). However, a POSITA would understand that slew rate maintains its plain meaning of the change in output voltage over time, and that the “ratio tr/tf of output pulses” as used in the ’539 Patent is simply a reference to that ordinary meaning of “slew rate.” *Ex.* 2005 at 61 n.3.

These teachings convey to a POSITA that as the need arises, a predetermined slew rate and output impedance can be selected by enabling or disabling transistor pairs such as QP2/QN2 such that the slew rate and output impedance are modified according to a predetermined need. Ex. 2005 at ¶¶60-71. This configuration, where transistors QP2 and QN2 would be set to arrive at both a predetermined output impedance and a predetermined slew rate for pulses output from the claimed output buffer circuit is recited in claims 1 and 4, which are reproduced below:

1. *An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:*

a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor;

a predriver with outputs for driving only said first [n]-channel MOS transistor and only said first p-channel MOS transistor having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor

in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor; and

a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor,

wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.

4. The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a ***smaller device size with a smaller gate width*** than said first p-channel MOS transistor and said first n-channel MOS transistor, and have a ***small effect on rise and fall times of pulses output from said main driver.***

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '539 Patent "would have a bachelor's or the equivalent degree in electrical or computer engineering or a related field, and 2-3 years of professional experience relating to integrated circuit design." Pet. 3. For purposes of this Response, Patent Owner does not challenge that definition.

IV. Claim Construction

A. The preamble to claim 1 is limiting.

The Petition states that “for purposes of this proceeding and the analysis presented herein, no claim term requires express construction.” Pet. 4. The Petition further takes no position as to whether the preamble to claim 1 is limiting (and thus does not contend that it is *not* limiting). *See, e.g.*, Pet. at 13 (alleging that “Itoh teaches the preamble to the extent that it’s limiting”).

The preamble to claim 1 recites “An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate.”

A preamble is limiting when it “is essential to understand limitations or terms in the claim body.” *MEMS Tech. Berhad v. Int'l Trade Comm'n*, 447 F. App'x 142, 154 (Fed. Cir. 2011) (quoting *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002)). A preamble is also limiting where it reflects “the essence or a fundamental characteristic of the claimed invention.” *In re Jasinski*, 508 F. App'x 950, 952 (Fed. Cir. 2013) (quoting *Vizio, Inc. v. Int'l Trade Comm'n*, 605 F.3d 1330, 1341 (Fed. Cir. 2010)). Here, the preamble to claim 1 is limiting for both reasons.

1. The preamble is essential to understand limitations in the claim body.

Claim 1 and claim 4, taken together, recite:

1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor *for driving a load according to **said data***, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load....

4. ... wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor, and *have small effect on rise and fall times of **pulses output*** from said main driver.

Ex. 1001 at Claims 1, 4. As explained further below, the preamble is limiting because it is essential to understand several limitations in the claim body.

As an initial matter, the preamble provides antecedent basis for the very first limitation: “a main driver having at least a pair of first p-channel MOS transistor and a first n-channel MOS transistor *for driving a load **according to said data***.” Without the preamble’s recitation of “[a]n output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate,” “said data” would have no antecedent basis. Ex. 2005 at ¶83. Accordingly, the preamble must be limiting. *See In re Fought*, 941 F.3d 1175, 1178 (Fed. Cir. 2019) (“We have

repeatedly held a preamble limiting when it serves as antecedent basis for a term appearing in the body of a claim.”).

Furthermore, the preamble is *also* necessary to understand the final limitation of dependent claim 4, which recites that the second transistor pair has a “small effect on rise and fall times of *pulses output* from said main driver.” Ex. 1001 at Claim 4. Of course, claims 1 and 4 are *apparatus* claims, and do not (and cannot) recite any *method* step of “outputting pulses” from the main driver. However, the preamble makes clear that the apparatus of the claim is “for *outputting data in the form of an input pulse train* at a predetermined output impedance and slew rate,” and the first limitation of claim 1 further makes clear that the main driver is “for driving a load *according to said data*.” Thus, the preamble and the first limitation make clear that pulses are output “in the form of an input pulse train at a predetermined output impedance and slew rate.”

As explained by Patent Owner's expert Dr. Jacob, without the preamble, there would also be no context for understanding claim 4's recitation of “pulses output from said main driver,” because there would be no indication of *any* pulses to be output from the overall output buffer circuit generally or the main driver more specifically. Ex. 2005 at ¶¶83-84. Accordingly, the preamble provides necessary context to understanding the claim term “pulses output from said main driver” as recited by claim 4, and as a result must be limiting. *MEMS Tech. Berhad v. Int'l*

Trade Comm'n, 447 F. App'x 142, 154 (Fed. Cir. 2011) (quoting *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002)).

2. The preamble also reflects a fundamental aspect of the invention.

The preamble is limiting for an additional reason: the specification makes clear that a fundamental aspect of the invention is to provide an output in the form of a pulse train according to predetermined impedance and slew rate characteristics. For example, the Summary of the Invention states:

It is therefore an object of the present invention to provide an output buffer circuit which is capable of sufficiently *compensating for variations in the cross-point between rising and falling waveforms of output pulses and variations in the slew rate against variations in the power supply voltage and the ambient temperature even when the output buffer circuit is incorporated in a system.*

...

With the [inventive] arrangement, the number of transistors of the main driver for driving the load according to control signals and the number of transistors of the predriver are *changed to simultaneously adjust the cross-point of output pulses and the slew rate as well as the output impedance with the same control signals*. Consequently, the data receiving side connected to the output buffer circuit is prevented from malfunctioning, making it possible to achieve a system which operates normally even when the power supply voltage and the ambient temperature vary.

Since *the output impedance and the rise and fall times of output pulses are simultaneously controlled*, the number of control signals and the steps of a testing process are made smaller than if the output impedance and the rise and fall times of output pulses were controlled independently of each other. Thus, the manufacturing cost of the output buffer circuit is prevented from increasing.

The system incorporating the output buffer circuit has its performance capability increased because *the slew rate is automatically improved by monitoring and adjusting only the output impedance of the output buffer circuit*.

...

With the above arrangements, since *the delay monitor circuit reflects the adjusted values of the output impedance of the output buffer circuit and the [slew rate] of output pulses*, a system clock signal and the data output from the output buffer circuit can be synchronized more accurately with each other.

Ex. 1001 at 2:54-60, 3:14-3:34, 4:18-22. Furthermore, as explained by Dr. Jacob, each embodiment of the '539 Patent is consistent with the goal of providing data in the form of a pulse train at a predetermined slew rate and output impedance. Ex. 2005 at ¶¶ 72-78, 85-87, 105-107.

Accordingly, the goal of outputting data in the form of pulses (and doing so at a predetermined output impedance and slew rate that are controlled together) is a fundamental aspect of the invention, and is entitled to patentable weight. *See Vizio*,

Inc. v. Int'l Trade Comm'n, 605 F.3d 1330, 1341 (Fed. Cir. 2010) (“[T]he ‘for decoding’ language . . . is properly construed as a limitation, and not merely a statement of purpose or intended use for the invention, because ‘decoding’ is the essence or a fundamental characteristic of the claimed invention.”).

B. Claim 4 requires two comparisons: a comparison between the p-channel transistors and the n-channel transistors.

Claim 4 recites:

4. The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor, and have a small effect on rise and fall times of pulses output from said main driver.

Ex. 1001 at Claim 4. For purposes of this discussion, “P1” and “P2” refer respectively to the first p-channel and second p-channel MOS transistors, and “N1” and “N2” refer respectively to the first n-channel and second n-channel MOS transistors.

The Board’s Institution Decision states that “P2 and N2 operate as a pair of transistors and P1 and N2 operate as a pair, logically P2 and N2 would be sized as a pair to be smaller, larger, or the same size as the P1, N1 pair.” Paper No. 9 at 26-27. In view of the Board’s reasoning and the knowledge of a POSITA, Patent Owner

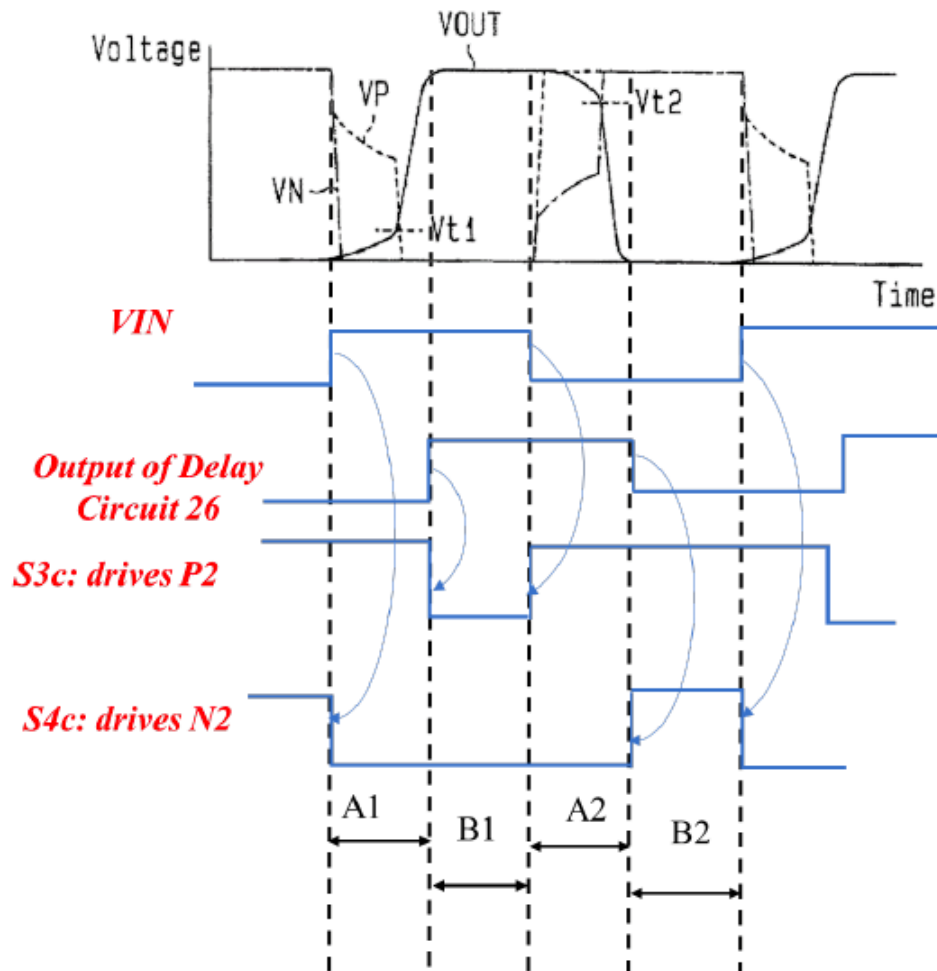
acknowledges the understanding set forth in the Board's Institution Decision, and accepts that the proper comparison is between the combined device size of the P2, N2 pair with the device size of the combined device size of the P1, N1 pair. In other words, if the device size of P2 is less than the device size of P1, and the device size of N2 is less than the device size of N1, then the size requirements of claim 4 are satisfied. *See* Ex. 2005 at ¶80 & n.5.

V. The Petition's challenge of claim 4 fails.

As noted above, the claim requires an “output buffer circuit for outputting data *in the form of an input pulse train at a predetermined output impedance* and slew rate.” Both of the Petition's challenges to claim 4 rely on a combination of Itoh's “Category 1” and “Category 2” embodiments (such as a combination of Itoh's embodiments 2 and 4). *See* Pet. 43-46 (proposing a combination of Itoh's embodiments 2-4 for Ground 2); *id.* at 82 (relying solely on the Petition's Ground 2 analysis for the preamble of claim 1).

However, in the combined Itoh system, there is no “output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance” as the claim requires. Instead, in the Petition's proposed combination of Itoh's embodiments, the combined system would constantly adjust output impedance *within* a given pulse train output by the system, such that data would not be output “in the form of an input pulse train at a predetermined output impedance.”

More specifically, the Petition's proposed combination involves the following timing diagram, where pulses output by the system correspond to the below timing diagram:



Waveforms of Example 2.1

Pet. at 50. In the combination, the transistors P2 and N2 are turned off entirely during periods A1 and A2. During these periods, P2 and N2 do not provide output impedance control. Only during periods B1 and B2 are P2 and N2 “turned on for output impedance control.” See Pet. 49-50 (“P2 and N2 are turned off during periods

A2 and A1.... During B1 and B2 when VOUT is substantially stable, P2 and N2 are turned on for output impedance control.”).

Accordingly, as explained by Patent Owner's expert Dr. Jacob, Itoh's system constantly changes the output impedance over the course of every pulse transition, and thus is not designed to output data in the form of an input pulse train at “a predetermined output impedance” as claim 1 requires. Ex. 2005 at ¶107 (“Itoh outputs each and every data pulse at two different output impedance values.”).

Indeed, Petitioner's expert Dr. Thompson admitted at his deposition that the output impedance of the system changes rapidly over the course of a single pulse. Specifically, he stated that between A1 and B1, “the output impedance of the system change[s]”:

8 Q Okay. Does the output impedance of the
9 system change between A1 and B1?
10 **A Yes.**
11 Q Why does the output impedance change
12 between A1 and B1?
13 **A For the same reason I discussed earlier.**
14 **S3c is changing from A1 to B1. When S3c is low,**
15 **Transistor P2 now becomes low resistance.**
16 **In the time of A1, S3c is high. And in**
17 **that case, the transistor is off, so it has high**
18 **resistance. So a transistor in this application is**
19 **a voltage-controlled resistor, and that's why the**
20 **impedance is changing.**

Ex. 2006 at 16:8-20. He further explained that the system changes provide different output impedances during time periods B1 and B2 than during time periods A1 and A2, because the system “alters the impedance during B1 and B2” but has “no effect during A1 and A2.” *Id.* at 27:13-18.

Accordingly, as explained by Patent Owner's expert Dr. Jacob, a POSITA would have understood that the Petition's combination would have changed output impedance during *each* pulse, during every transition from an “A” period to a “B” period and again from every transition from a “B” period to an “A” period. Ex. 2005 at ¶¶107-109. Accordingly, as explained by Dr. Jacob, the proposed combination of Itoh's embodiments would “not drive its output pulse train ‘at a predetermined output impedance’” as claims 1 and 4 require, but would “instead driv[e] *each bit* of its pulse train at *two different* output impedance values.” Ex. 2005 at ¶110 (emphasis in original).

Of course, an output buffer circuit designed to output a pulse train at two different impedance values (which impedances are toggled during every output pulse transition) does not meet the plain meaning of an output buffer circuit “for *outputting data in the form of an input pulse train at a predetermined output impedance.*” Ex. 2005 at ¶¶110-111.

Nor does the Petition provide any rationale as to how this limitation would be met—the Petition at most alleges that Itoh's drive circuit “performs output

impedance control,” but does not provide any explanation of how Itoh’s output buffer circuit would “output[] data in the form of an input *pulse train at a predetermined output impedance*.” See Pet. 13 (failing to identify any single “predetermined output impedance”). As explained by Dr. Jacob, a POSITA would understand that the preamble of claim 1 could only be satisfied by a pulse train being output at a single predetermined output impedance, rather than the pulse train being output by rapidly switching between two *different* output impedances as Dr. Thompson acknowledges the Petition’s combination entails. See Ex. 2005 at ¶105 (“[I]t would have been clear to a person of ordinary skill that Takahashi’s output buffer was intended to have the same output impedance over an entire output pulse train.”).

Because the Petition does not even allege a single “predetermined output impedance” that “data in the form of an input pulse train” would be output at for the Petition’s theories regarding Grounds 2 and 3, the Petition’s Ground 2 and 3 theories (the only two Grounds challenging claim 4 of the ’539 Patent) cannot succeed.

If you put the first stage of secondary drive transistors into operation, then you of necessity put the first stage of slew rate transistors into operation.

VI. Conclusion

Because the Petition fails to establish invalidity of the sole remaining challenged claim 4 of the ’539 Patent, claim 4 should be found not unpatentable.

Date: June 19, 2024

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 4,312 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

Date: June 19, 2024

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on June 19, 2024, by filing this document through the Patent Trial and Appeal Board Cast Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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