

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re *Inter Partes* Review of:

Inventor: Takahashi

U.S. Patent No. RE43,539

Reissued: July 24, 2012

For: Output Buffer Circuit and  
Integrated Semiconductor  
Circuit Device with Such  
Output Buffer Circuit

IPR2023-01286

**DECLARATION OF DR. BRUCE JACOB  
IN SUPPORT OF PATENT OWNER'S RESPONSE  
RE: *INTER PARTES* REVIEW OF U.S. PATENT NO. RE43,539**

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## **I. OVERVIEW**

### **A. Introduction**

(1) I have been asked by counsel for plaintiff Longitude Licensing Limited (“Longitude”) to provide my opinions concerning the petition for *Inter Partes* Review of U.S. Patent No. RE43,539 (“the ’539 Patent”).

(2) I am being compensated at my standard hourly rate of \$690/hr plus any out-of-pocket expenses. My compensation does not depend in any way on the particular testimony or opinions that I express in this disclosure, or on the outcome of this litigation.

(3) For this document, I have been asked to prepare a disclosure of my opinions regarding the ’539 patent and associated documents.

(4) I reserve the right to respond to any disclosed opinions, declarations, or arguments made by Defendant or its experts during claim construction. I have prepared this disclosure having reviewed the patent-in-suit and the IPR filed regarding the patent-in-suit. I have also reviewed the material specifically cited within this Declaration.

**B. Legal Principles**

(5) In rendering my opinion herein and considering the subject matter of the patent, I am relying on legal principles related to validity that counsel for Patent Owner has explained to me. These principles are summarized below.

(6) I understand that a patent may be rendered “obvious” based on an alleged prior art reference or a combination of such references plus what a person of ordinary skill in the art would understand based on his or her knowledge and the references. I understand that a patent cannot be properly granted for subject matter that would have been obvious to a person of ordinary skill in the art at the time of the alleged invention, and that a patent claim directed to such obvious subject matter is invalid under 35 U.S.C. § 103. It is also my current understanding that in assessing the obviousness of claimed subject matter one should evaluate obviousness over the prior art from the perspective of one of ordinary skill in the art at the time the invention was made (and not from the perspective of either a layman or a genius in that art).

(7) I understand that obviousness is a question of law premised on underlying facts including: (a) the scope and content of the prior art, (b) the differences between the prior art and the claims, and (c) the level of ordinary skill in the pertinent art. I understand that the question is not whether the differences

themselves would have been obvious, but whether the claimed invention as a whole would have been obvious.

(8) In arriving at an obviousness determination, I understand that one must sufficiently explain and support the conclusions that the prior art references disclose all the elements recited in the Challenged Claims, and that a POSITA not only could have, but would have been motivated to combine all the prior art references in the way the patent claims, and would have had an expectation of success in doing so. That is, even if all the claim elements are found across a number of references, an obviousness determination must consider whether a person of ordinary skill in the art would have the motivation to combine those references. I understand that this combinability determination, as supported by an articulated motivation to combine, requires a plausible rationale for why those prior art references would have worked together. I understand that absent some articulated rationale, a “common sense” finding is no different than the conclusory statement “would have been obvious.” I understand that it is also important that knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references.

(9) I understand that even if all the claim elements are found across a number of combinable references with sufficient motivation to combine those references, a

POSITA would still need a “reasonable expectation of success” in making the claimed invention as a whole, in order for the invention to be found obvious. I understand that in order to possess the requisite “reasonable expectation of success” in combining all the references to make the claimed invention as a whole, the POSITA must be motivated to do more than merely vary all parameters with no indication of critical parameters or try all of a number of possible choices with no direction until successful. I understand that the prior art must provide more than a mere “general guidance” that seems to be a “promising field of experimentation.”

(10) I understand that the obviousness inquiry must exclude hindsight and avoid reading into the prior art the patent's teachings. I understand that imbuing a POSITA with knowledge of the invention when no prior art reference or references of record convey or suggest that knowledge, is such example of improper hindsight bias. I understand that invoking design choice to add many distinct components to a system evidences impermissible hindsight, not obviousness.

**C. Qualifications**

(11) In 1988, I earned the *Ars Baccalaureate* degree in mathematics from Harvard University in Cambridge, Massachusetts. In 1995 and 1997, respectively, I earned M.S. and Ph.D. degrees, both in Computer Science & Engineering, from the

University of Michigan in Ann Arbor, Michigan. In 2020, I was named a Fellow of the IEEE (Institute of Electrical and Electronics Engineers) “for contributions to computer memory design and analysis.”

(12) From 1997 to 2003, I was an Assistant Professor in the Department of Electrical & Computer Engineering at the University of Maryland at College Park, Maryland. I was promoted to Associate Professor and was granted tenure in 2003. In 2007, I was promoted to Director of Computer Engineering, a position I held until my sabbatical beginning Fall 2010. In the Spring of 2011, I was promoted to full Professor. In 2022, I joined the United States Naval Academy in Annapolis Maryland, where I am a Professor of Cyber Science and study the security of memories and computer hardware systems.

(13) For the past twenty-five years I have designed high-performance semiconductor memory systems and computer-systems architectures for both industry and government. For example, I helped Micron design their Hybrid Memory Cube architecture, redesigned Cray's memory controller for their Black Widow memory system, helped Northrop Grumman design a memory-system interconnect for their experimental ultra-low-power datacenter, designed a high-performance memory system for the 1024-core Teraflux chip funded by the European Commission, and have collaborated with the Departments of Energy

and Defense on the design of their next-generation supercomputers. My group also fabricated semiconductor memory chips and a CPU chip as part of an early DOD research program on die stacking using through-silicon vias.

(14) I received the National Science Foundation CAREER Award in 1999 for my work in semiconductor memory devices and memory systems. At Maryland, I was decorated seven times as a Clark School “Rainmaker” (renamed “Research Leader” in 2006) for my research program, being one of the top 100 researchers and fundraisers in the University.

(15) I have published two books on computer memory systems: Memory Systems: Cache, DRAM, Disk (Morgan Kaufmann) 2007; and The Memory System (You Can't Avoid It; You Can't Ignore It; You Can't Fake It) (Morgan & Claypool) 2009. My MS thesis at Michigan was on the design of multi-level cache hierarchies; my Ph.D. thesis at Michigan was on the topic of virtual memory system architectures. I have written over eighty refereed articles on memory systems, cache systems, computer design, embedded systems, operating systems design, astrophysics, and algorithmic composition. These can be found listed in my *curriculum vitae*. As of Summer 2023, my body of research has been cited over 8000 times, with over 80 cites per work on average. I hold three patents in the area of circuit design and another two in the area of memory-systems design.

(16) I founded the annual *International Symposium on Memory Systems* and am frequently invited to give keynote speeches and high-level briefings on the topic of memory systems around the world. I have been the keynote speaker at meetings including EMS, MCHPC, MODSIM, SAMOS, and Computing Frontiers. I was asked to speak before a National Academies panel on the topic of memory systems and to participate in a roundtable discussion with the Department of Energy (DOE) to create a roadmap for computer science and applied mathematics research at DOE in the coming decades.

(17) Topics my research group has researched extensively include *DRAM and main memory technologies* (e.g., controllers, devices, bus organizations, system architectures, and memory-system power), *non-volatile memories* (e.g., flash memories, numerous resistive RAM variants, and controller & system designs for both main memory and storage), and *embedded systems*. The last area includes investigation of topics in design verification for heterogeneous systems (e.g., the detailed, hardware-verified simulation of heterogeneous systems, for the design and verification of embedded systems that control various hardware devices in real time), highly integrated, heterogeneous systems-on-a-chip (e.g., design and implementation of a monolithic *micro electro mechanical systems* [MEMS]-based gas sensor component, integrated on silicon with a digital microcontroller), and the hardware/software co-design of embedded microcontrollers and real-time operating systems.

(18) In summary, I have extensive technical experience and expertise relating to aspects of designing and implementing computer memories and memory systems, including the fabrication of semiconductor devices and chips, all of which are the topics of concern in this matter.

(19) My *curriculum vitae* is attached as Exhibit 1.

(20) The following is a brief overview of my opinions.

## **II. LEVEL OF SKILL IN THE ART**

(21) I understand Dr. Thompson proposes that a person of ordinary skill in the art “would have a bachelor’s or the equivalent degree in electrical or computer engineering or a related field, and 2–3 years of professional experience relating to integrated circuit design.” For purposes of this declaration, I adopt his proposed level of skill in the art.

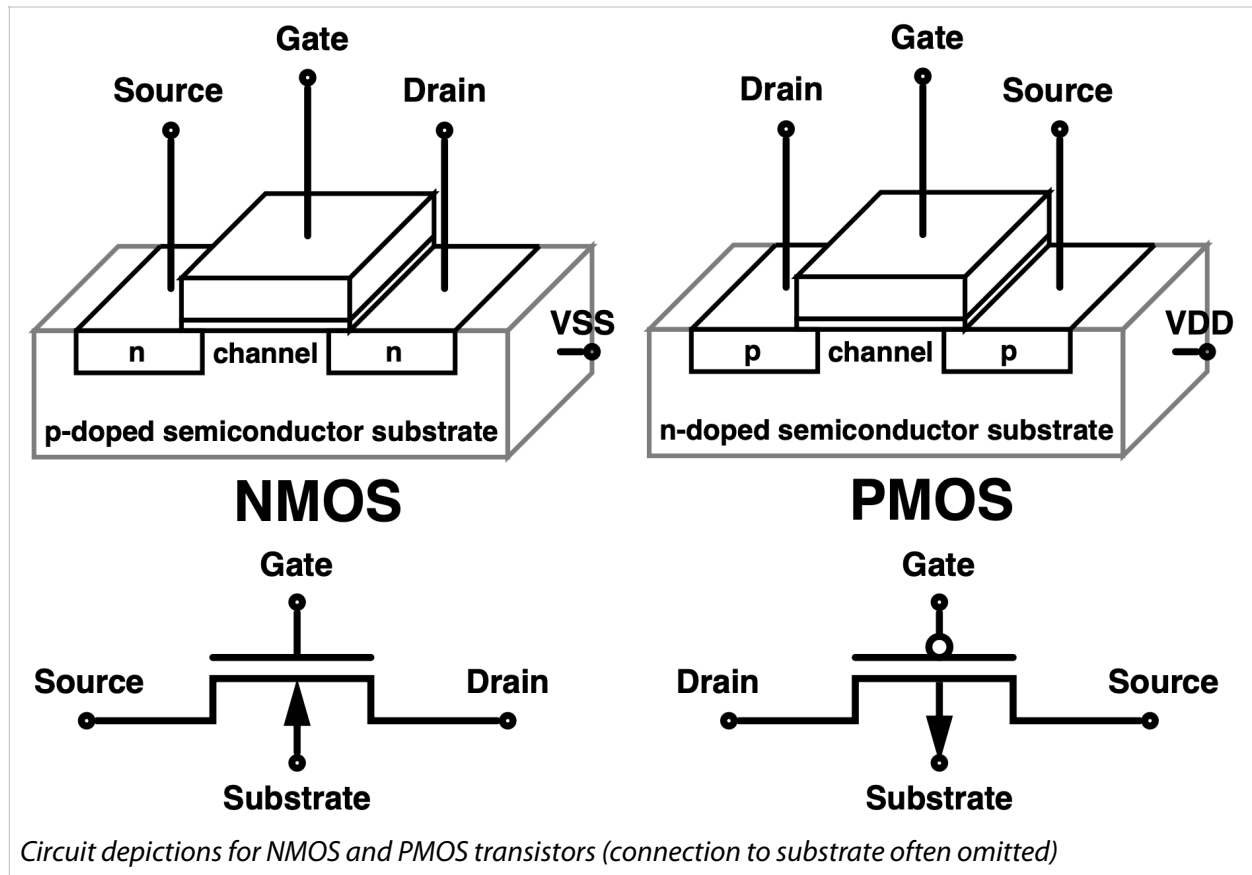
### **III. TECHNICAL BACKGROUND**

(22) The '539 patent is concerned with transistors, their timing, and the effects of slew rate and impedance. The following discusses some charge-pump fundamentals.

#### **A. Fundamentals of Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs)**

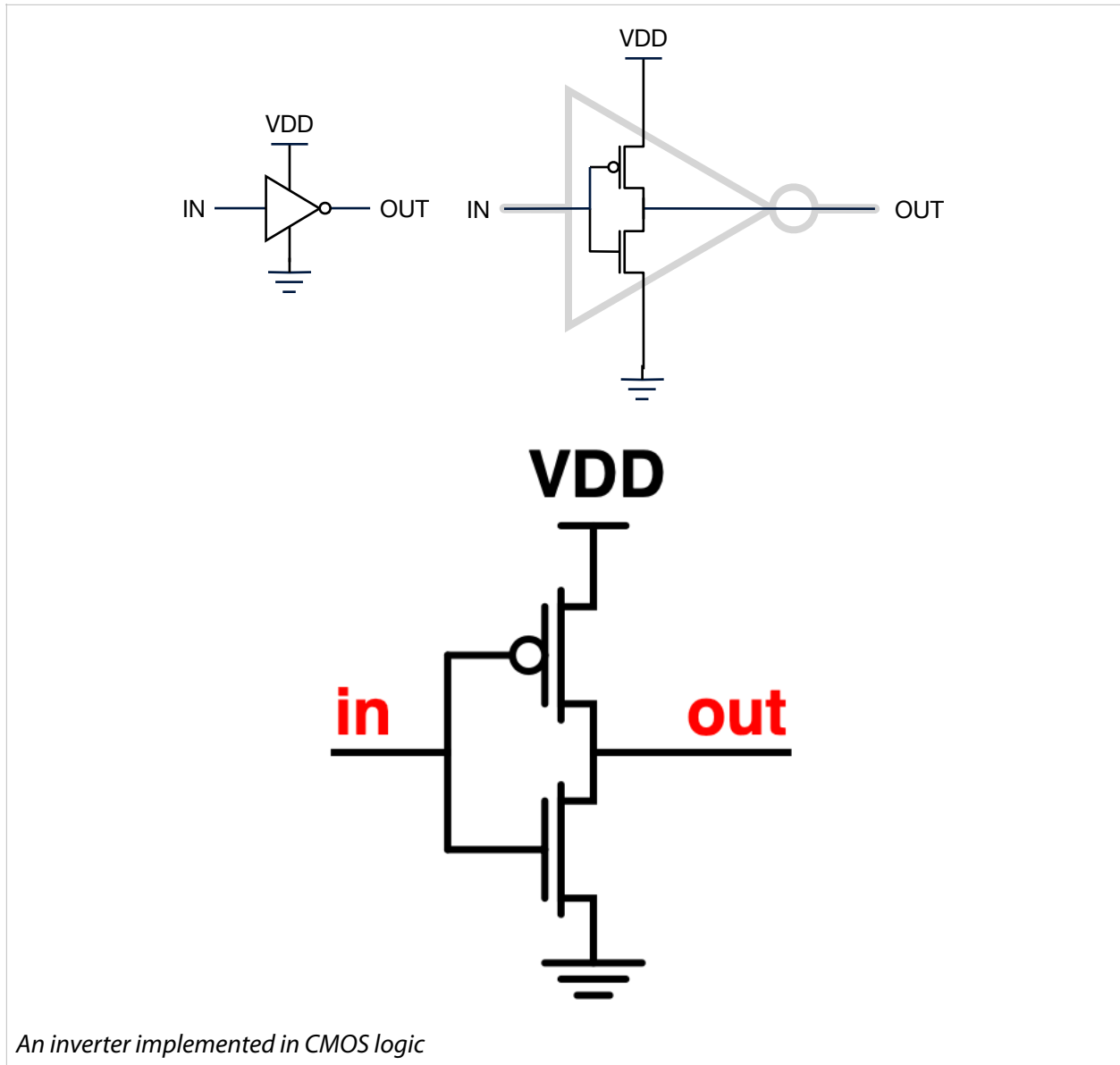
(23) Modern digital systems are built of *MOS (metal-oxide semiconductor) FETs (field-effect transistors)*, herein just *transistors*. They are typically arranged in a “complementary” circuit design — thus the term *CMOS (complementary metal-oxide semiconductor)*. The individual devices are *n-type* and *p-type* transistors, called *NMOS* and *PMOS* devices, respectively. They are electrically controlled switches. When the correct voltage is presented at their *gate* input, they become electrically conductive between *source* and *drain* contacts; when a different voltage is presented at their gate input, they become nonconductive.

(24) The following are the 3D structures and circuit symbols for these transistors:



(25) A PMOS device is conductive when *ground* (logic 0) is presented to its gate; an NMOS device is conductive when *VDD* (logic 1) is presented to its gate.

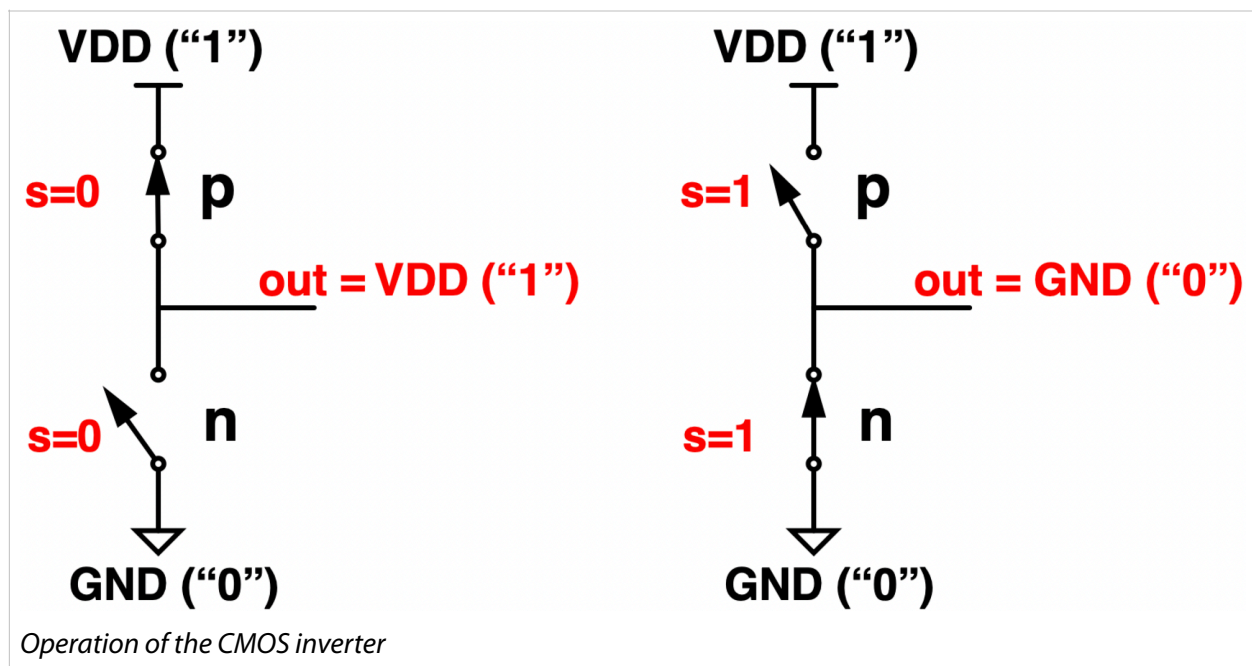
(26) The following show how these transistors are arranged to form an inverter, the most fundamental CMOS logic gate:



(27) As mentioned, a PMOS device is conductive when ground (logic 0) is presented to its gate; an NMOS device is conductive when VDD (logic 1) is presented to its gate. Thus, if ground (logic 0) is presented to the inverter at its

input, the PMOS device will become conductive, and the NMOS device will remain nonconductive. If VDD (logic 1) is presented to the inverter at its input, the NMOS device will become conductive, and the PMOS device will remain nonconductive.

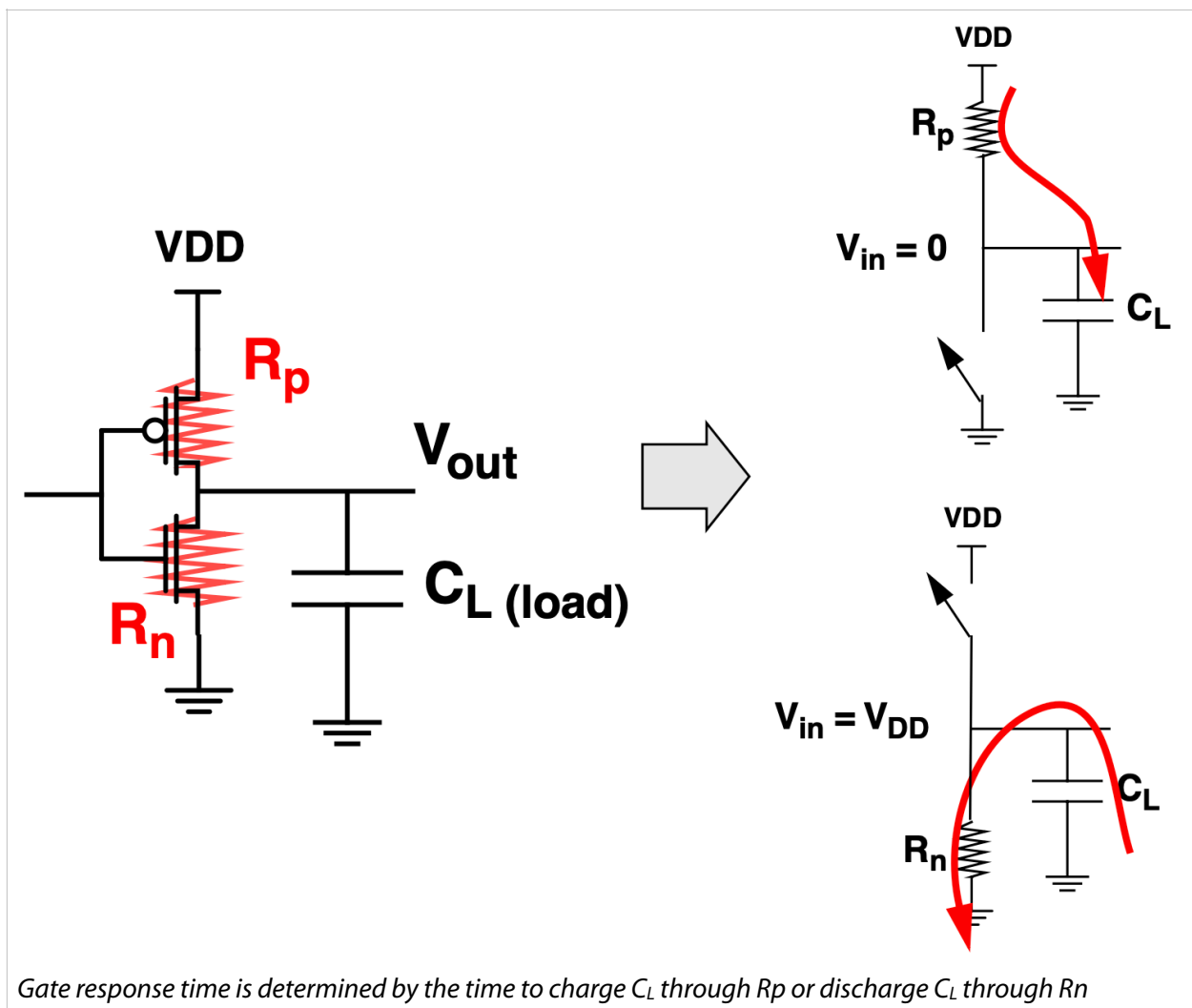
(28) This switch-level operation is illustrated in the figure below:



(29) A logic 0 input results in the PMOS device conductive and the NMOS device nonconductive; the output is thus connected directly to VDD, a logic 1 output. A logic 1 input results in the NMOS device conductive and the PMOS device nonconductive; the output is thus connected directly to ground, a logic 0 output. Both scenarios represent a logical inversion of the input.

## B. Transistor Performance — Propagation Delay

(30) The performance of a gate, i.e. the propagation delay through the gate, can be understood intuitively through the following illustration, which suggests that in the real world transistors have non-zero resistance, and when used in logic gates they drive outputs that have non-zero capacitance.

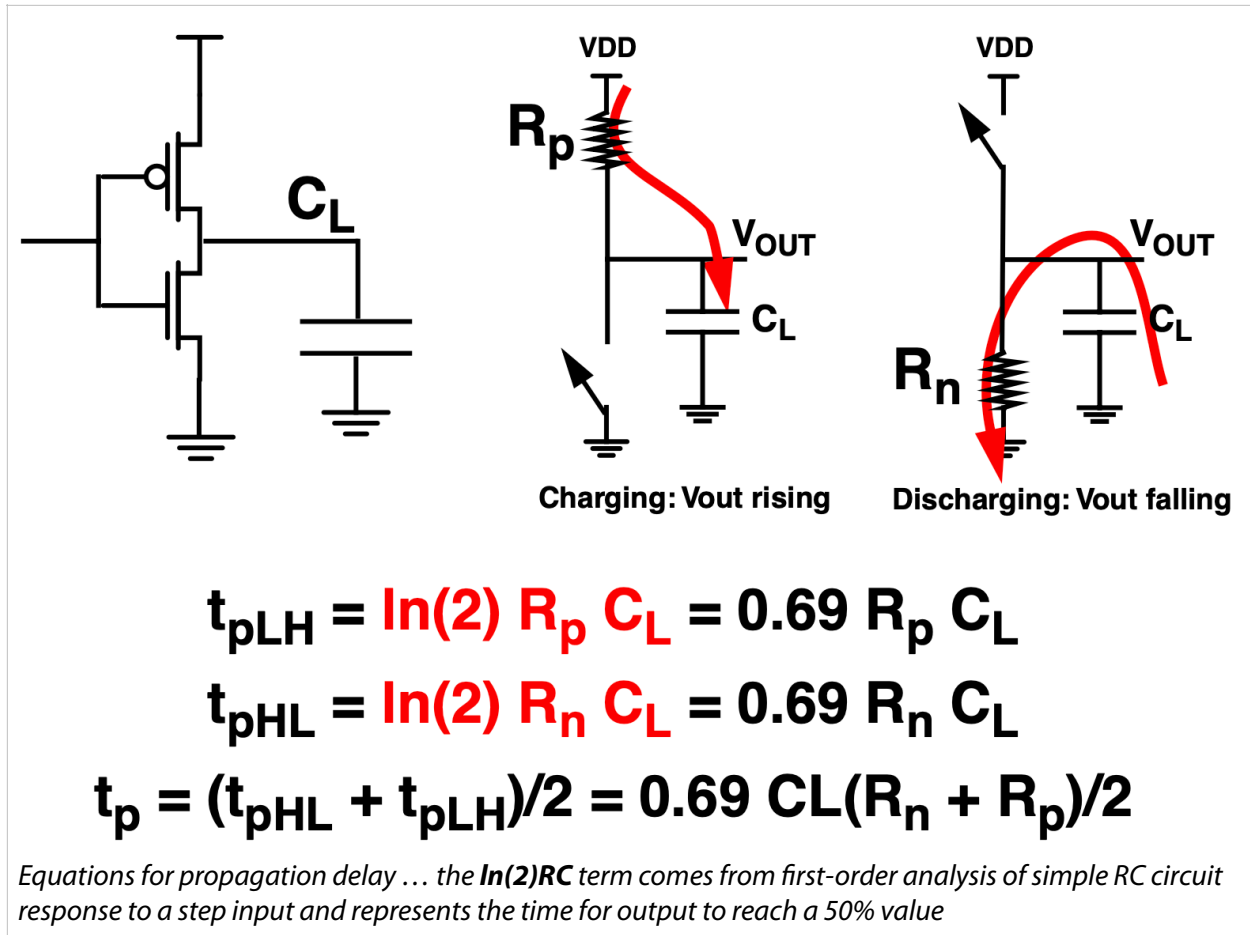


(31) The PMOS device has effective resistance  $R_p$ ; the NMOS device has effective resistance  $R_n$ ; and the output load has a capacitance of  $C_L$ . Inverting an input of 0 to an output of 1 (top right) means connecting the output to VDD and therefore charging up the load capacitance to VDD through the PMOS resistor. Inverting an input of 1 to an output of 0 (bottom right) means connecting the output to ground and therefore discharging the load capacitance to ground through the NMOS resistor.

(32) What are logical results (the production of VDD and ground voltages that represent logic 1 and 0, respectively) are accomplished through physical processes that take non-zero time. These processes are governed by what is called the *RC time delay*, meaning that the time it takes to charge or discharge a capacitance  $C$  through a resistance  $R$  takes a time  $\tau$  that is proportional to the product of the resistance and capacitance:

$$\tau \propto RC$$

(33) The equations are given in the figure below for the time that these processes take in an *inverter*, the most fundamental of gates.



(34) The propagation time when pulling the output from low to high (to charge the load capacitance from ground to VDD through the PMOS device) is called  $t_{pLH}$  and is given by the following equation:

$$t_{pLH} = 0.7 R_p C_L$$

(35) The propagation time when pulling the output from high to low (to discharge the load capacitance from VDD to ground through the NMOS device) is called  $t_{pHL}$  and is given by the following equation:

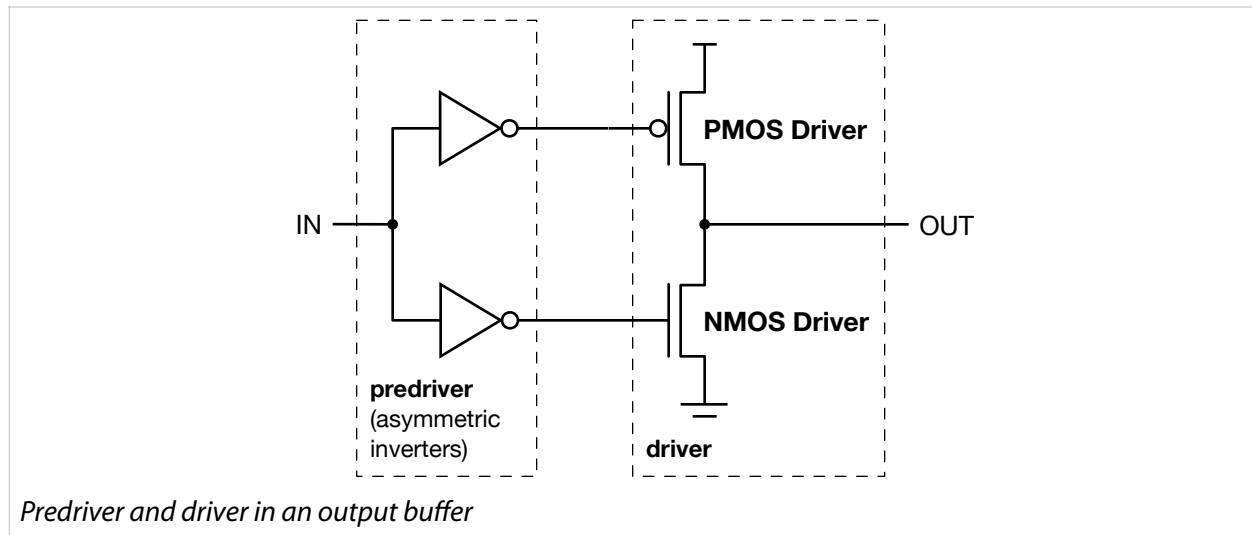
$$t_{pHL} = 0.7 R_n C_L$$

(36) What is called the gate's overall *propagation delay*,  $t_p$ , is given by the average of  $t_{pLH}$  and  $t_{pHL}$  ... it is a common way to express gate performance and/or transistor performance.

### **C. Output Buffers (Output Drivers)**

(37) An output buffer, or driver, is a circuit intended for driving communications between chips; it therefore uses larger transistors than the normal on-chip circuits, because it is expected to drive a larger load, that load being the output pins on the transmitting size, the receiving pins on the input side, the circuit-board traces, and so forth. While output buffers in integrated circuits can be little more than oversized inverters, they are often a combination of a *predriver* and a *driver*, where the predriver generates the logical signal and some degree of control, and the driver is a pair of independently controlled oversized MOSFETs.

(38) The predriver/driver arrangement looks something like the following:



(39) The predriver uses *asymmetric* inverters, such that each inverter turns its corresponding driver MOSFET *on slowly* and *off rapidly*. In the circuit above, one would have the following:

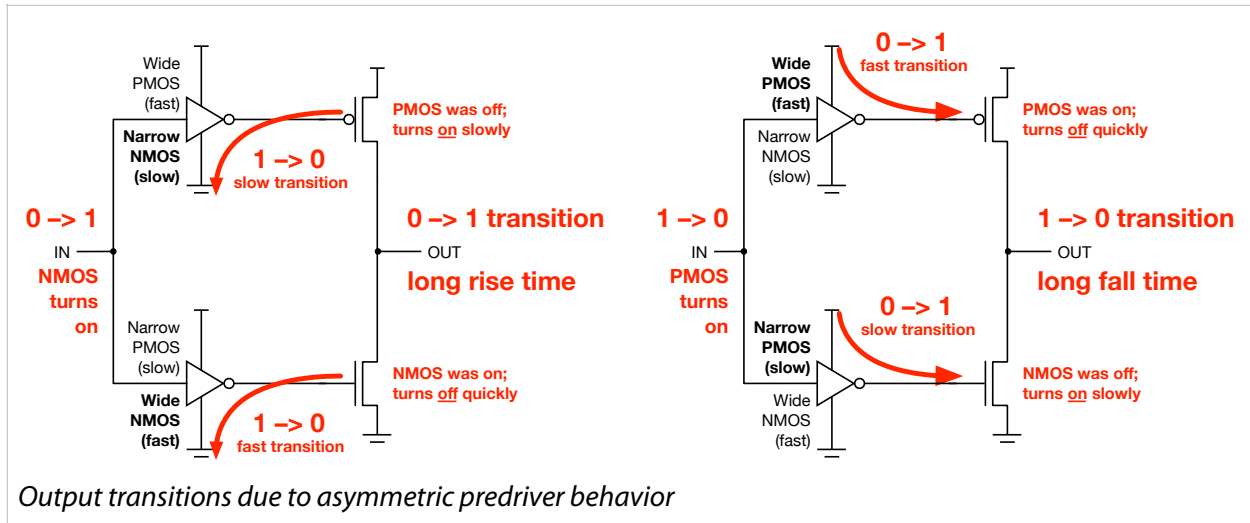
**top inverter** — drives the PMOS driver; want  $t_{pHL} > t_{pLH}$   
(need fast PMOS inside inverter => e.g., wide transistor  
need slow NMOS inside inverter => e.g., narrow and/or stacked)

**bottom inverter** — drives the NMOS driver; want  $t_{pHL} < t_{pLH}$   
(need slow PMOS inside inverter => e.g., narrow and/or stacked  
need fast NMOS inside inverter => e.g., wide transistor)

(40) The design uses asymmetry to reduce the short-circuit current in the output driver. MOSFETs do not turn immediately on or off, and so there can be times

when both of the driver MOSFETs are partially on, while one is turning on and the other is turning off. The desire for gentle rise and fall times on the output (larger *slew rates*), which leads to better signal integrity in chip-to-chip communications, exacerbates this problem: a long, gentle rise or fall time means that the output MOSFETs are in partial on/off states for longer periods of time than they would be with a short rise/fall time. This would lead to long times when both transistors are both on, and this generates large short-circuit currents, which is highly problematic in output drivers: even in normal operation, they drive significant current, so their short-circuit current would be very high.

(41) The asymmetric control structure of the predriver addresses this potential problem by shutting down one driver transistor quickly while turning on the other driver transistor slowly. This allows for both a gentle transition from one output state to another (from low to high or high to low), and a minimal period of time during which both output driver transistors are partially on. One way to achieve asymmetry is to make some of the transistors much wider (or “larger”) than the others; doing this gives a wider transistor a lower resistance than otherwise equivalent transistors with narrower channels. The wider transistors, with lower resistance, will drive their output faster than the others. The resulting effect is shown in the figure below.

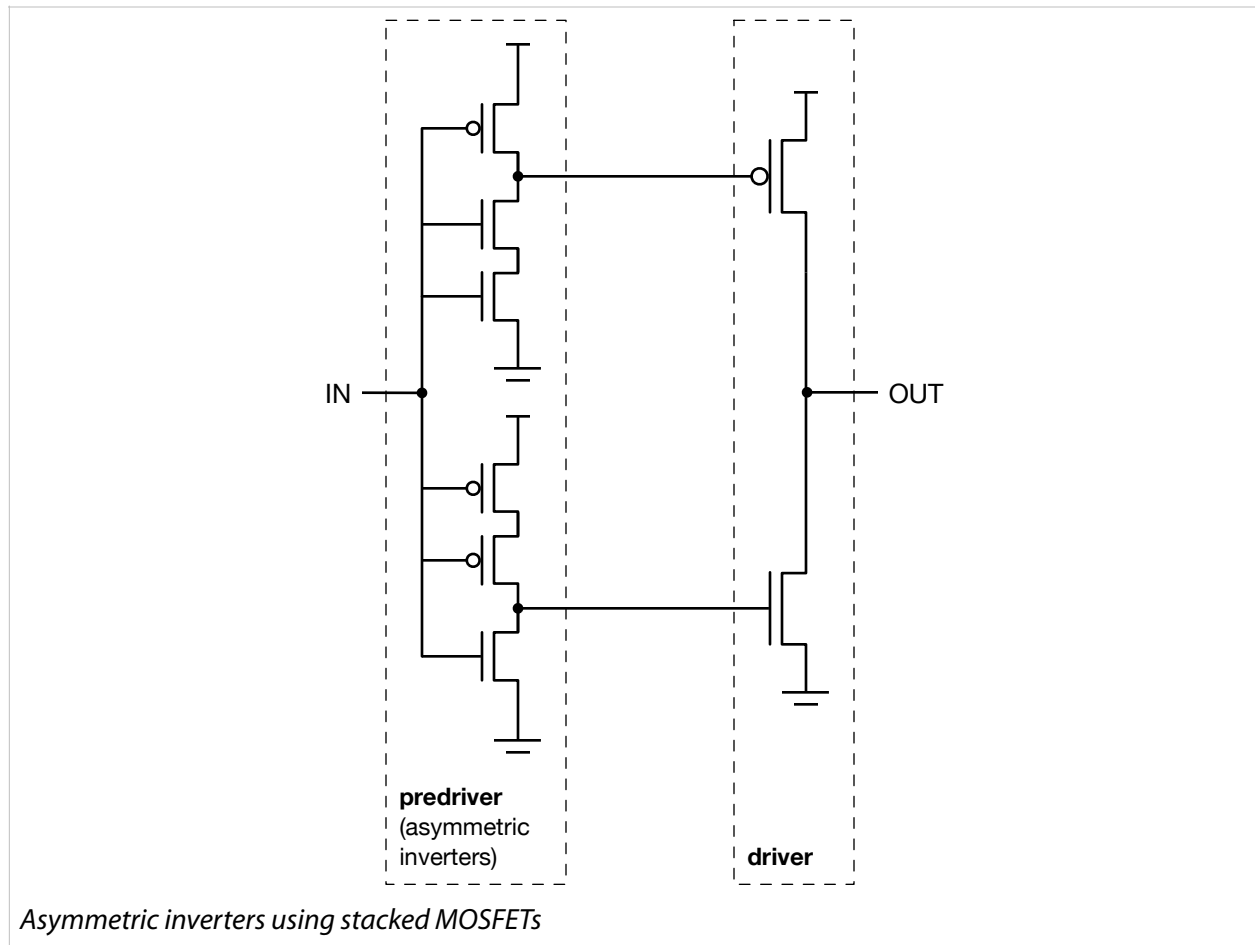


(42) In the 0 → 1 transition, the NMOS devices in the inverters turn on; they are the focus of attention. When the top inverter of the predriver turns on, the inverter's output goes to ground, which turns on the top transistor in the output driver — the PMOS driver. The top inverter of the predriver uses a narrow and therefore slow NMOS device; the output of the inverter will go to ground much more slowly than if using a wide transistor — the resistance is higher, and therefore the RC time delay is higher. This causes the PMOS output driver to turn on slowly. Meanwhile, as the PMOS output driver is slowly turning on, the NMOS output driver (the bottom MOSFET in the driver) is controlled by the bottom inverter in the predriver, which has a wide NMOS device, and so that inverter's output goes to ground quickly. This means that the NMOS driver turns off quickly. Thus, because of this arrangement, the top PMOS driver transistor turns on very slowly during a

0 → 1 output transition, while at the same time, the bottom NMOS driver transistor turns off very quickly.

(43) In the 1 → 0 transition, the PMOS devices in the inverters turn on; they are the focus of attention. When the bottom inverter of the predriver turns on, the inverter's output goes to VDD, which turns on the bottom transistor in the output driver — the NMOS driver. The bottom inverter of the predriver uses a narrow and therefore slow PMOS device; the output of the inverter will go to VDD much more slowly than if using a wide transistor — the resistance is higher, and therefore the RC time delay is higher. This causes the NMOS output driver to turn on slowly. Meanwhile, as the NMOS output driver is slowly turning on, the PMOS output driver (the top MOSFET in the driver) is controlled by the top inverter in the predriver, which has a wide PMOS device, and so that inverter's output goes to VDD quickly. This means that the PMOS driver turns off quickly. Thus, because of this arrangement, the bottom NMOS driver transistor turns on very slowly during a 1 → 0 output transition, while at the same time, the top PMOS driver transistor turns off very quickly.

(44) The following is a depiction of another way to achieve asymmetric inverters:



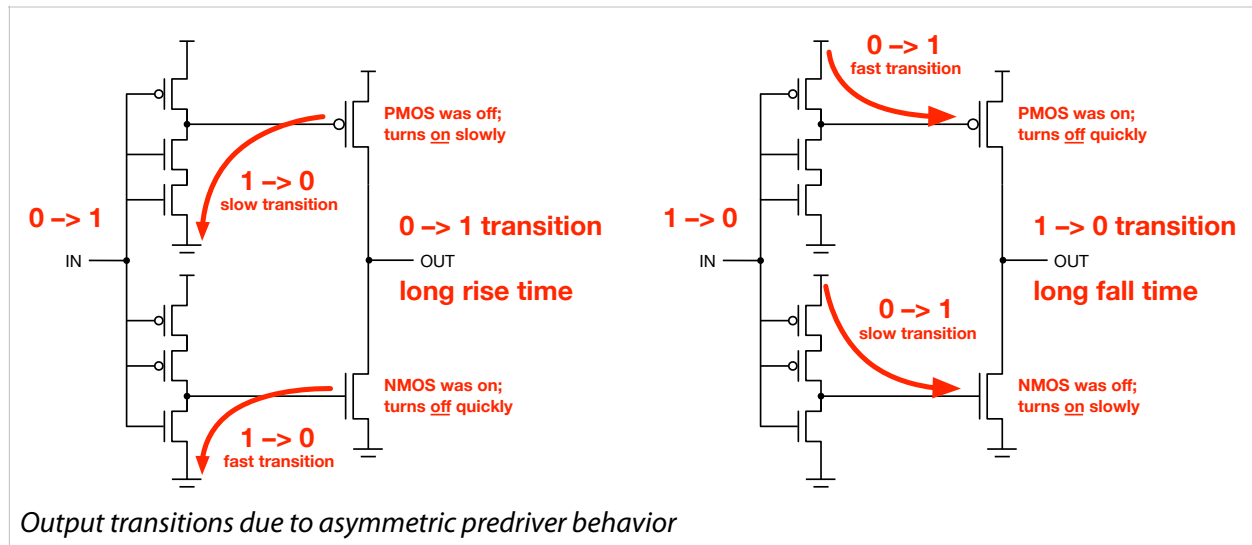
(45) The top inverter of the predriver uses a pair of stacked NMOS devices; when they turn on, the inverter's output goes to ground, which turns on the top transistor in the output driver — the PMOS driver. Because the two NMOS devices in the predriver are wired in series, the output of the circuit will go to ground much more slowly than if there were only one transistor — the effective resistance is twice as large, and therefore the RC time delay is twice as large. Meanwhile, as the PMOS output driver is slowly turning on, the NMOS output

driver (the bottom MOSFET in the driver) is controlled by the bottom inverter in the predriver, which has a single NMOS device instead of two NMOS devices in series, and so that inverter's output goes to ground quickly. This means that the bottom NMOS driver turns off quickly. Thus, because of this arrangement, the top PMOS driver transistor turns on very slowly during a 0  $\rightarrow$  1 output transition, while at the same time, the bottom NMOS driver transistor turns off very quickly.

(46) Similarly, the bottom inverter of the predriver uses a pair of stacked PMOS devices; when they turn on, the inverter's output goes to VDD, which turns on the bottom transistor in the output driver — the NMOS driver. Because the two PMOS devices in the predriver are wired in series, the output of the circuit will go to VDD much more slowly than if there were only one transistor — the effective resistance is twice as large, and therefore the RC time delay is twice as large.

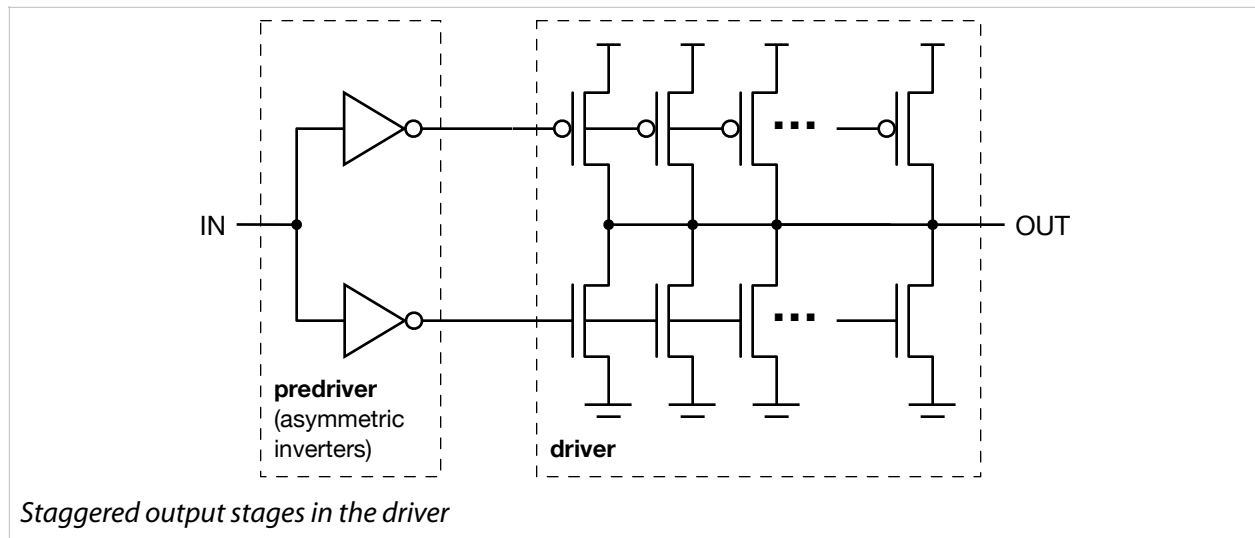
Meanwhile, as the NMOS output driver is slowly turning on, the NMOS output driver (the bottom MOSFET in the driver) is controlled by the bottom inverter in the predriver, which has a single PMOS device instead of two PMOS devices in series, and so that inverter's output goes to VDD quickly. This means that the top PMOS driver turns off quickly. Thus, because of this arrangement, the bottom NMOS driver transistor turns on very slowly during a 1  $\rightarrow$  0 output transition, while at the same time, the top PMOS driver transistor turns off very quickly.

(47) These transitions are illustrated in the figure below:



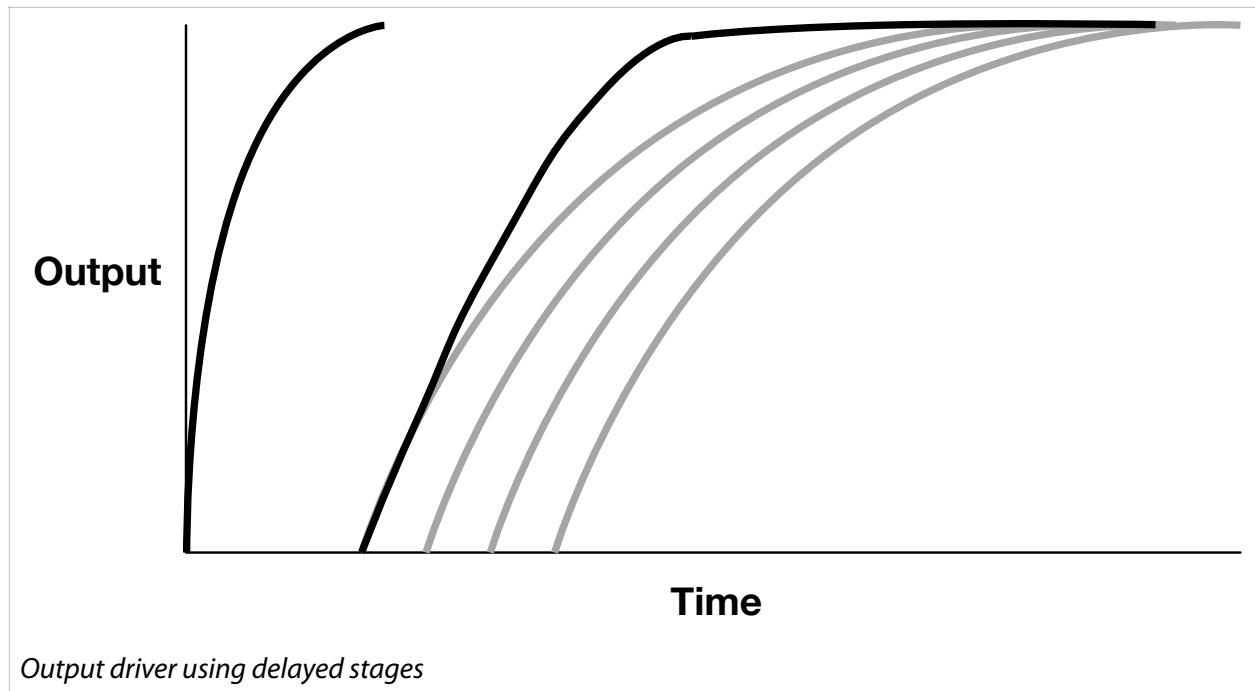
(48) If one wants sharper rise/fall times, one would reduce the resistance in the predriver inverters, making the slow transitions less slow.

(49) Another mechanism used in output buffers to achieve longer slew rates is to divide the output driver into multiple stages and stagger the output of those stages. A simple form of this arrangement is shown below.



(50) Each transistor in the output driver portion receives its control signal slightly later than the one before it in the sequence, and therefore each stage begins its output behavior slightly after the one before it in the sequence. The effect is a more gradual rise or fall in the output signal than if there were only one stage of driver transistors.

(51) The following illustration gives an example of this behavior.



(52) The graph shows the output buffer's output (voltage) as a function of time. On the left-hand side is the output of a single wide output driver, giving a relatively fast rise time. On the right-hand side is shown the results of having four staggered output drivers with transistor widths a factor of four narrower than the driver on the left-hand side of the graph. Each of these has a rise time roughly a factor of four longer, illustrated with light grey curves. When their output is staggered and summed, the result is a waveform that has a more gradual rise than the output on the left, yet the driver has the same overall transistor width and thus the same overall drive strength or drive capability as the driver whose output is shown on the far left.

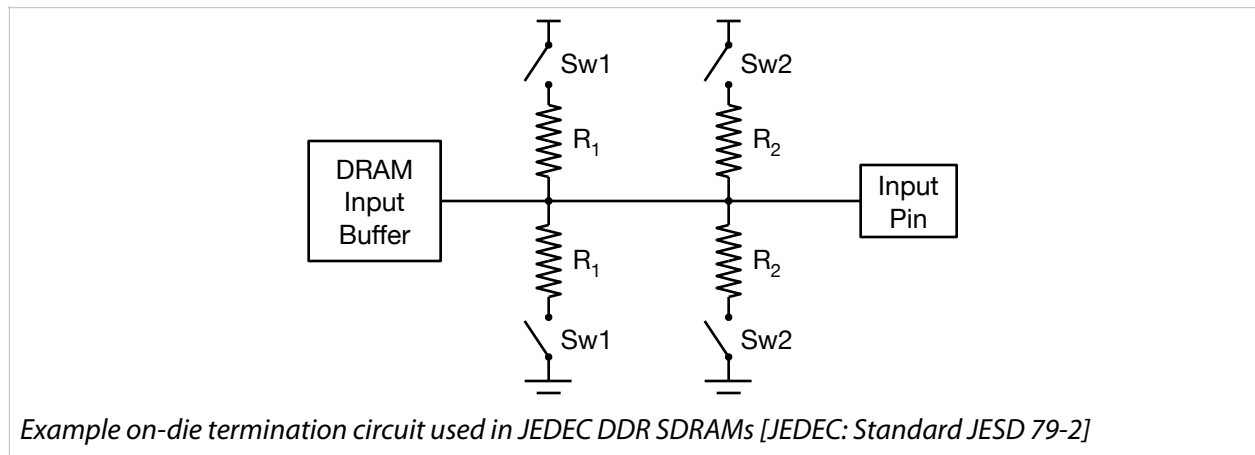
(53) If the different stages of the output driver are separately controlled (as opposed to the circuit in the figure above, in which the multiple stages are all controlled by the same signals), then the arrangement provides a finer degree of control regarding a designer's ability to change the slew rate of the signal, and it can also be used to increase or decrease the amount of current being driven to the output. For instance, turning on more stages of the output buffer would allow one to drive more current to the buffer's output pin. This is often called creating a *low impedance* output buffer. Lower impedance is generally more desirable, because as mentioned previously, drivers tend to use significant current, as they drive large loads.

#### **D. On-Die Termination (ODT)**

(54) Another aspect of impedance characteristics is that of impedance matching. Many memory devices have configurable *on-die termination (ODT)*, a mechanism that allows one to modify at run time the impedance characteristics of an input/output line by changing the resistance/s electrically attached to that line. Matching the impedances of output drivers, transmission lines, and input receivers is important because impedance is a significant factor of signal integrity. Mismatched impedance levels cause signal reflections at every boundary, much like one can see waves cresting in the ocean wherever there are abrupt changes in the water depth.

Elimination of these reflections makes the resulting signal smoother and easier to read correctly, which enables faster communications.

(55) The following diagram shows an example ODT circuit used in many modern DRAM devices<sup>1</sup>:



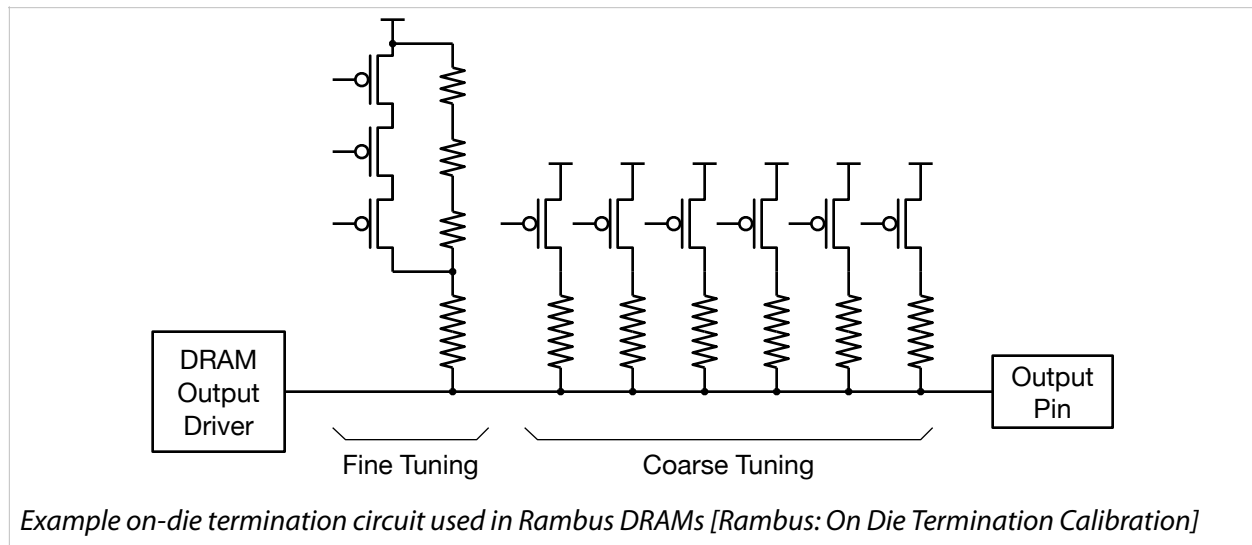
(56) Turning the various switches on and off couples and decouples the various resistances to the input lines, and this changes the effective resistance of the input line; changing the resistance of the line changes the impedance of the line accordingly (resistance is effectively a subset of impedance). Changing the on/off states of the switches in the circuit above therefore changes the impedance characteristics of the DRAM's input receiver.

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<sup>1</sup> JEDEC Solid-State Technology Association. *JEDEC Standard JESD 79-2 — DDR2 SDRAM Specification*. September 2003.

(57) On-die termination circuits come in different forms and can be used to change the characteristics of input receivers, output drivers, or both.

(58) The following diagram shows an example ODT circuit used in Rambus DRAM devices on the output driver side<sup>2</sup>:



(59) Each of the transistors in the circuit is independently controllable, providing a fair degree of flexibility in setting the impedance of the output driver. As with the JEDEC ODT mechanism, one can change the effective resistance by turning on and off different combinations of switches, and the switches that are shown wired in series on the left are, as Rambus describes, used for fine-tuning the effective resistance value. Changing the effective resistance changes the circuit's impedance.

<sup>2</sup> Rambus. *On Die Termination Calibration*. Downloaded from <https://www.rambus.com/on-die-termination-calibration/> on May 26, 2024.

#### **IV. OVERVIEW OF U.S. PATENT RE43,539 ('TAKAHASHI')**

##### **A. Specification**

(60) The '539 patent ('Takahashi') is concerned with the development of output buffers that are configurable in two ways: output slew rate (rate of change of the output voltage over time) and the output drive strength or drive capability (amount of current that the driver can deliver). As Takahashi describes, this is what is required to maintain reliable communications in view of what are known as *PVT variations*, meaning timing variations resulting from manufacturing differences due to *process* effects, timing variations at runtime due to fluctuations in the *voltage* level coming from the power supply, and timing variations at runtime due to *temperature* changes in the ambient environment:

It is important for systems operating at higher speeds and under low voltages to suppress variations in the driving capability and slew rate of the output buffer circuit of the integrated semiconductor circuit device in view of fluctuations in the power supply voltage and the ambient temperature and different device performance capabilities.

For example, Japanese patent applications laid-open Nos. 05-175444 and 2-092019 propose arrangements for adjusting the driving capability of an output buffer circuit by changing the output impedance thereof. Proposals disclosed in Japanese patent applications laid-open Nos. 2001-68986 and 2000-332593 adjust the slew rate of

an output buffer circuit by changing the ratio of  $t_r$ (rise time)/ $t_f$ (fall time) [slew rate] of an output pulse waveform. [Takahashi, 1:30–43]

(61) Designers usually compensate for PVT variations through adjustments made at initialization, or (as in the case of temperature fluctuations) occasionally throughout the day. Takahashi confirms this understanding:

Generally, as the output impedance of an output buffer circuit increases due to variations in the power supply voltage and the ambient temperature, the ratio  $t_r/t_f^3$  [slew rate] of output pulses tends

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<sup>3</sup> In the field of semiconductor device communications, the term “slew rate” is often used interchangeably with the terms “rise time” and/or “fall time.” Note that Takahashi makes a number of references to “the ratio  $t_r/t_f$ ” to indicate slew rate. This seems to be a mistranslation, as in English slew rate is often written as “rise/fall time” or “rise time/fall time” meaning *either* rise time *or* fall time (under normal circumstances, the two are engineered to be as close to one another as possible) and not a mathematical combination of the two. This understanding is confirmed by a number of passages within Takahashi, including the following:

Proposals disclosed in Japanese patent applications laid-open Nos. 2001-68986 and 2000-332593 adjust the slew rate of an output buffer circuit by changing the ratio of  $t_r$ (rise time)/ $t_f$ (fall time) of an output pulse waveform. [1:39–43]

FIG. 6 shows the results of a simulation which indicate that when the ratio  $t_r/t_f$  is controlled, the range of variations of the slew rate is reduced to about  $\frac{1}{3}$  of the range of variations of the slew rate when the ratio  $t_r/t_f$  is not controlled. FIG. 6 illustrates waveforms (a: Device worst) when the ratio  $t_r/t_f$  is not controlled, the power supply voltage is minimum, and the device is at a high temperature at which the slew rate is lowest, waveforms (b: Device best) when the ratio  $t_r/t_f$  is not controlled, the power supply voltage is maximum, and the device is at a low temperature at which the slew rate is highest, and waveforms (c: Device best) when the ratio  $t_r/t_f$  is controlled, the power supply voltage is maximum, and the device is at a low temperature at which the slew rate is highest. In the results of the simulation shown in FIG. 6, the output impedance is controlled both when the ratio  $t_r/t_f$  is controlled and when the ratio  $t_r/t_f$  is not controlled. [9:6–21]

In these passages, Takahashi appears to be using “slew rate” and “the ratio  $t_r/t_f$ ” interchangeably.

to be greater (longer). Therefore, if the relationship between changes in the output impedance of the output buffer circuit and changes in the ratio  $t_r/t_f$  [slew rate] is determined in advance, then, since a corrective quantity for the ratio  $t_r/t_f$  [slew rate] of output pulses is known for a corrective quantity for the output impedance, the output impedance and the ratio  $t_r/t_f$  [slew rate] can simultaneously be corrected by one control signal. Consequently, the data receiving side is prevented from malfunctioning, making it possible to achieve a system which operates normally even when the power supply voltage and the ambient temperature vary. [Takahashi, 8:45–58]

(62) Takahashi's mechanism for adjusting output impedance can control the output buffer's drive strength:

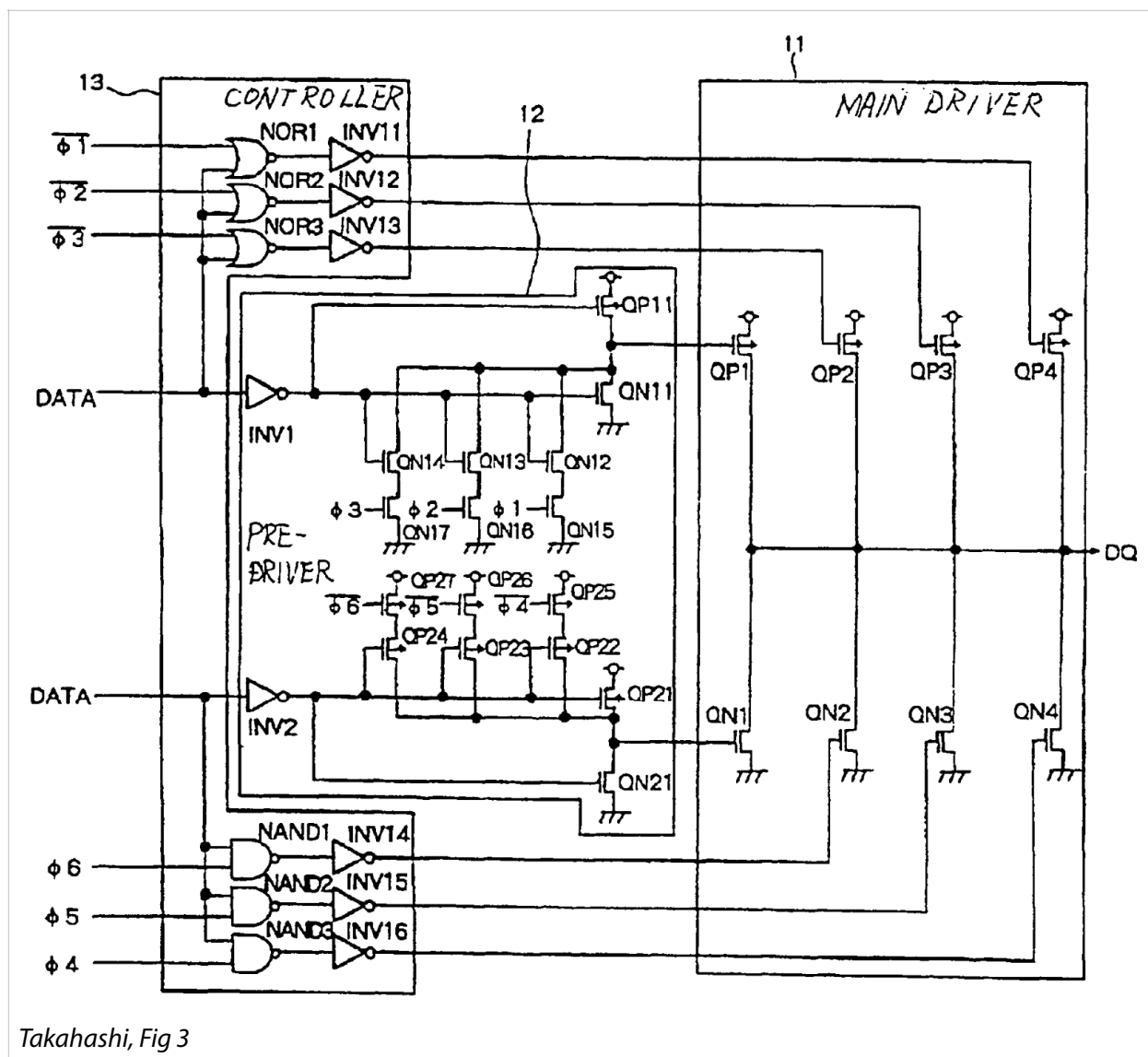
In the first embodiment, of pMOS transistor QP11 and nMOS transistor QN11 which are provided to drive pMOS transistor QP1 of the main driver, only nMOS transistor QN11 has its driving capability increased, and of pMOS transistor QP21 and nMOS transistor QN21 which are provided to drive nMOS transistor QN1 of the main driver, only pMOS transistor QP11 has its driving capability increased.

With such an arrangement, when pMOS transistor QP11 switches from the ON state to the OFF state and the nMOS transistor QN11 switches from the OFF state to the ON state, as shown in FIG. 8(a), if the speed of switching from the OFF state to the ON state increases because of the large driving capability of nMOS transistor QN11, then there occur periods of time in which pMOS transistor QP11 and nMOS transistor QN11 are turned on, allowing a through current to flow from the power supply to the ground potential. The through

current serves as a noise source, and tends to increase the current consumption of the output buffer circuit.

In the present embodiment, pMOS transistors QP31 through QP36 are added to the arrangement shown in FIG. 3 to increase the driving capabilities of both pMOS transistor QP11 and nMOS transistor QN11 as shown in FIG. 8(b). The arrangement according to the second embodiment offers the advantages of the output buffer circuit according to the first embodiment, and is additionally effective to prevent noise from being produced and the current consumption from being increased by the through current. Similarly, nMOS transistors QN31 through QN36 are added to the arrangement shown in FIG. 3 to increase the driving capabilities of both pMOS transistor QP21 and nMOS transistor QN21 prevent noise from being produced and the current consumption from being increased by the through current. [Takahashi, 9:66–10:30]

(63) Takahashi's circuit design incorporates a predriver, a main driver, and a controller that enables the various stages of the main driver (which adjusts the output drive strength of the main driver transistors) at the same time enables the various transistors of the set of stacked sets (which adjusts the slew rate of the main driver transistors). One of the embodiments is shown below:



Takahashi, Fig 3

(64) Takahashi explains that the adjustments are made simultaneously to both the slew rate and the output impedance (drive strength):

In the present embodiment, the output impedance is adjusted and the ratio  $t_r/t_f$  [slew rate] are adjusted simultaneously. For example, when control signal  $\phi 1$  is rendered low and control signal  $\phi 4$  is rendered high in order to lower the output impedance by one stage, control

signal  $\phi 1$  which is an inversion of control signal  $\phi 1$  goes high, turning on nMOS transistors QN12, QN15, and control signal  $\phi 4$  which is an inversion of control signal  $\phi 4$  goes low, turning on pMOS transistors QP22, QP25. Therefore, the ratio  $t_r/t_f$  [slew rate] is reduced by one stage. Similarly, when the output impedance is lowered by two stages, the ratio  $t_r/t_f$  [slew rate] is reduced by two stages, and when the output impedance is lowered by three stages, the ratio  $t_r/t_f$  [slew rate] is reduced by three stages. The output impedance and the rise time  $t_r$  at the time the high-level data is output and the output impedance and the rise time  $t_f$  at the time the low-level data is output can be adjusted independently of each other. [Takahashi, 8:4–19]

(65) These adjustments are intended to be performed at initialization time, or occasionally when temperature changes are high enough to warrant recalibration, as one would not try to adjust slew rate in the middle of a transmission. As Takahashi explains, “it is difficult to detect fluctuations of the slew rate of the output buffer circuit because *the slew rate cannot easily be monitored*.” [Takahashi, 2:14–17, emphasis added]

(66) A person of ordinary skill would understand that transistor pairs that make up the secondary drivers (such as QP2 and QN2, QP3 and QN3, etc.) can be enabled or disabled depending on what output impedance and slew rate are desired, and that that selection of which transistor pairs to enable is based on

control signals  $\phi 1$  through  $\phi N$ . The passage above describes this, as does other passages:

Output buffer circuit 8 outputs data in synchronism with compensating clock signal CLKOE supplied from phase synchronizing circuit 9. *The circuit for monitoring the delay in output buffer circuit 8 has its output impedance and slew rate controlled, as with output buffer circuit 8, by control signals  $\phi 1$  through  $\phi N$ ,  $\neg \phi 1$  through  $\neg \phi N$  to be described later on.* [Takahashi, 5:49–54, emphasis added]

As shown in FIG. 3, the output buffer circuit according to the first embodiment has main driver 11 for driving a load connected to DQ terminal, main driver 11 having an output impedance which can be changed, a predriver 12 for driving main driver 11 according to data (DATA) read from a sense amplifier and changing the ratio  $t_r/t_f$  [slew rate] of output pulses of main driver 11, and *a controller 13 for generating signals to change the output impedance of main driver 11 and the ratio  $t_r/t_f$  [slew rate] of output pulses according to control signals  $\phi 1$  through  $\phi 6$  from a control circuit, etc. Control signals  $\neg \phi 1$  through  $\neg \phi 6$  shown in FIG. 3 are inversions of signals  $\phi 1$  through  $\phi 6$ .* Inverters for inverting signals  $\phi 1$  through  $\phi 6$  are omitted from the illustration in FIG. 3. [Takahashi, 5:59–6:4, emphasis added]

(67) Figure 3 shows the transistor pairs that make up the secondary drivers being enabled or disabled based on control signals  $\phi 1$  through  $\phi 6$ . For example, transistor pair QP2/QN2 is controlled by control signals  $\phi 3$  and  $\phi 6$ , and a person

of ordinary skill would have understood these signals to have the same value and thus would have enabled or disabled both QP2 and QN2 as a pair, as Takahashi provides no description of how one should enable/disable the drive transistors of a given stage separately.

(68) Regarding the drive transistors of the secondary drivers, for instance transistors QP2 and QN2, Takahashi shows that, and a person of ordinary skill would have understood that, while they affect the output impedance of the output buffer, their effect on the overall output impedance would be less than the effect on output impedance of the main drive transistors QP1 and QN1. The drive transistors affect output impedance due to their device size, and in the institution decision<sup>4</sup> the Patent Board construed device size and gate width to be synonymous (“we construe ‘smaller device size’ and ‘smaller gate width’ to be synonymous” [p. 26]). The end result is that when a secondary drive transistor such as QP2 or QN2 is enabled and then turned on for driving output, this places an additional resistor in parallel with the main drive transistor QP1 or QN1. This reduces the resistance and thus impedance of the output as compared to that of QP1 or QN1 by itself. Because these secondary drive transistors are described by Takahashi as being smaller than the primary drive transistors, their effect on the overall output impedance would be less than that of the primary drive transistors. As Takahashi

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<sup>4</sup> IPR2023-01286 — *DECISION Granting Institution of Inter Partes Review* 35 U.S.C. § 314.

states, the secondary drive transistors QP2–QP4 and QN2–QN4 are smaller than the primary drive transistors QP1 and QN1:

pMOS transistors QP2 through QP4 as well as pMOS transistor QP1 drive the load connected to DQ terminal to adjust the output impedance when high-level data is output from main driver 11. nMOS transistors QN2 through QN4 as well as nMOS transistor QN1 drive the load connected to DQ terminal to adjust the output impedance when low-level data is output from main driver 11.

*pMOS transistors QP2 through QP4 and nMOS transistors QN2 through QN4 comprise transistors having a small device size (a narrow gate width) whose effect on the ratio  $t_r/t_f$  [slew rate] of output pulses is smaller than pMOS transistor QP1 and nMOS transistor QN1.* The number of pMOS transistors connected parallel to pMOS transistor QP1 and the number of nMOS transistors connected parallel to nMOS transistor QN1 are not limited to three, but at least one pMOS transistor may be connected parallel to pMOS transistor QP1 and at least one nMOS transistor may be connected parallel to nMOS transistor QN1. [Takahashi, 6:29–46, emphasis added]

(69) Takahashi also states that enabling these secondary drive transistors reduces the output impedance of the output buffer:

For adjusting the output impedance of the output buffer circuit shown in FIG. 3, the level of control signals  $\phi 1$  through  $\phi 3$  is rendered low *to turn on corresponding pMOS transistors QP2 through QP4 to lower the output impedance at the high-level data is output. At this time, the greater the number of*

*pMOS transistors that are turned on, the smaller the output impedance. Similarly, the level of control signals  $\phi_4$  through  $\phi_6$  is rendered high to turn on corresponding nMOS transistors QN2 through QN4 to lower the output impedance at the low-level data is output. At this time, the greater the number of nMOS transistors that are turned on, the smaller the output impedance.* [Takahashi, 7:47–58, emphasis added]

(70) Takahashi states explicitly in the first passage above that, being smaller than the primary drive transistors, the secondary drive transistors QP2–QP4 and QN2–QN4 would have an effect on the output buffer's slew rate that is less than that of the primary drive transistors QP1 and QN1. Takahashi states this elsewhere as well, for example:

*As described above, pMOS transistors QP2 through QP4 and nMOS transistors QN2 through QN4 comprise transistors having a small device size whose effect on the ratio  $t_r/t_f$  [slew rate] is smaller than pMOS transistor QP1 and nMOS transistor QN1. In FIG. 3, the ratio  $t_r/t_f$  [slew rate] is adjusted using only pMOS transistor QP1 and nMOS transistor QN1.* [Takahashi, 8:20–25, emphasis added]

(71) Takahashi thus conveys to a person of ordinary skill how to adjust an output buffer such that a predetermined slew rate and output impedance can be selected, by enabling or disabling secondary drive-transistor pairs such as QP2/QN2, thereby configuring the slew rate and output impedance according to a predetermined need.

(72) Takahashi says that the simplicity of the system allows for reduced testing steps and thus manufacturing costs:

Since the output impedance and the rise and fall times of output pulses are simultaneously controlled, *the number of control signals and the steps of a testing process are made smaller* than if the output impedance and the rise and fall times of output pulses were controlled independently of each other. *Thus, the manufacturing cost of the output buffer circuit is prevented from increasing.* [Takahashi, 3:24–30, emphasis added]

(73) This would not be the case if one needed to reconfigure the system in the middle of a pulse train, as doing so would require many more testing steps (one would need to test all possible combinations of mid-plus reconfigurations).

(74) In a similar vein, at the end of the excerpt above from 8:4–19, Takahashi says, “The output impedance and the rise time  $t_r$  at the time the high-level data is output and the output impedance and the rise time  $t_f$  at the time the low-level data is output can be adjusted independently of each other.” While this may be technically possible, I note that Takahashi’s primary embodiments teach that these settings would be adjusted at the same level for both high and low voltages, and all of the examples in the specification conform to this understanding. Further, adjusting the output buffer’s voltage-high and voltage-low output scenarios independently of each other would increase the number of testing steps and

therefore negate any savings in testing costs (one would need to test all possible combinations of unbalanced drive transistor sizes).

(75) Takahashi explains that the reconfiguration signals that adjust the output impedance and slew rate come from an external semiconductor device:

For example, *control signals  $\phi 1$  through  $\phi 6$  are generated from a control circuit 6 **according to commands supplied from an external integrated semiconductor circuit** that contains an output buffer circuit shown in FIG. 3. The data receiving the output buffer circuit shown in FIG. 3 is a signal which is synchronous with compensating clock signal CLKOE supplied from phase synchronizing circuit 9 shown in FIG. 2. [Takahashi, 6:5–13, emphasis added]*

(76) This could represent, for instance, a memory controller reconfiguring a memory device. The passage above is further evidence that the reconfiguration is infrequent and not performed on an access-by-access basis (it is generated by “commands” that come from the external device).

(77) Lastly, Takahashi explains that the purpose of the configuration changes is to account for variations in the power supply and ambient temperature, indicating that any reconfigurations occur on timescales relevant to these processes, and not timescales on the order of individual transactions.

Generally, *as the output impedance of an output buffer circuit increases **due to variations in the power supply voltage and the ambient temperature**, the ratio  $tr/tf$  of output pulses tends to be greater (longer).*

Therefore, if the relationship between changes in the output impedance of the output buffer circuit and changes in the ratio  $tr/tf$  is determined in advance, then, since a corrective quantity for the ratio  $tr/tf$  of output pulses is known for a corrective quantity for the output impedance, *the output impedance and the ratio  $tr/tf$  can simultaneously be corrected by one control signal. Consequently, the data receiving side is prevented from malfunctioning, making it **possible to achieve a system which operates normally even when the power supply voltage and the ambient temperature vary**.* [Takahashi, 8:45–58, emphasis added]

(78) Thus, it would have been clear to a person of ordinary skill that Takahashi's reconfigurable output buffer was intended to be reconfigured at initialization time, or occasionally when temperature changes are high enough to warrant recalibration. Further, it would therefore have been clear to a person of ordinary skill that the output impedance of Takahashi's output buffer would have remained the same over a given pulse train.

## **B. Claim 4**

(79) Takahashi's Claim 4 is dependent on Claim 1 ... the two are reproduced below, with the components identified in Claim 4 highlighted in Claim 1:

1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor;

a predriver with outputs for driving only said first [n-channel] MOS transistor and only said first p-channel MOS transistor having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor; and

a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor,

wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.

4. The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor, and have a small effect on rise and fall times of pulses output from said main driver.

(80) Regarding the limitation expressed in Claim 4, the institution decision<sup>4</sup> states that “because P2 and N2 operate as a pair of transistors and P1 and N1 operate as a pair, logically P2 and N2 would be sized as a pair to be smaller, larger, or the same size as the P1, N1 pair.” [pp. 26–27] Given this understanding, and given the engineering tendency to compare apples to apples, a person of ordinary skill would have viewed the claim language as calling for a size comparison between P1 and P2, and between N1 and N2 (i.e., between the second p-channel transistor and the first p-channel MOS transistor, and between the second n-channel transistor and the first n-channel MOS transistor), and that is the understanding of the claim language that I applied in my analysis<sup>5</sup>.

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<sup>5</sup> I also note that if the second p-channel transistor is smaller than the first p-channel transistor, and if the second n-channel transistor is smaller than the first n-channel transistor, then the “said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor,” as claimed.

**C. Claim 1 Preamble**

(81) The preamble for Claim 1 reads as follows:

1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

(82) I understand from counsel that whether a preamble is limiting depends in part on whether the preamble is essential to understanding limitations in the claim body, and whether it reflects a fundamental aspect of the invention.

(83) In my opinion, the preamble of Claim 1 is essential to understanding limitations in the claim body, because Claim 1's preamble is the only part of the claim that instructs the person of ordinary skill, an engineer, what the claimed invention is intended to *do*. An engineer needs to have a clear picture of the end goal while building something, to ensure that the final creation satisfies the desired intent. In particular, the preamble provides the antecedent for the "said data" limitations; the "said data" is supposed to be output in a very specific fashion by the claimed output buffer: Claim 1 requires, for instance, "driving a load **according to said data**" ... the claim requires a certain function of the main drive transistors, that they behave in a manner "according to said data," and yet, without the preamble, an engineer, a person of ordinary skill, can do nothing with this. The

preamble is the only place that provides the details on how the data should be output: that it is to be output “at a predetermined output impedance and slew rate.” This is a critical piece of information that, if removed from the claim, would render the claim ambiguous to a person of ordinary skill.

(84) The preamble introduces the data as a “pulse train,” to which Claim 4 refers in its “pulses output from said main driver.” Without the preamble, Claim 4’s requirement of output needs further clarification. For example, Claim 4 requires that certain drive transistors “have a small effect on rise and fall times” of those pulses, and to understand this, a person of ordinary skill would require Claim 1’s preamble and its description of a “predetermined ... slew rate” for explanation.

(85) It is also my opinion that the preamble of Claim 1 reflects a fundamental aspect of the invention. The notion of “a predetermined output impedance and slew rate” is fundamental to the claimed invention. These two aspects, output impedance and slew rate, are always treated as a unit — they are “simultaneously controlled,” which is the primary inventive aspect according to Takahashi and the reason for the received benefits:

With the [inventive] arrangement, *the number of transistors of the main driver for driving the load according to control signals and the number of transistors of the predriver are changed **to simultaneously adjust** the cross-point of output pulses and the slew rate as well as the output impedance with the same*

*control signals*. Consequently, the data receiving side connected to the output buffer circuit is prevented from malfunctioning, making it possible to achieve a system which operates normally even when the power supply voltage and the ambient temperature vary. [Takahashi, 3:14–23, emphasis added]

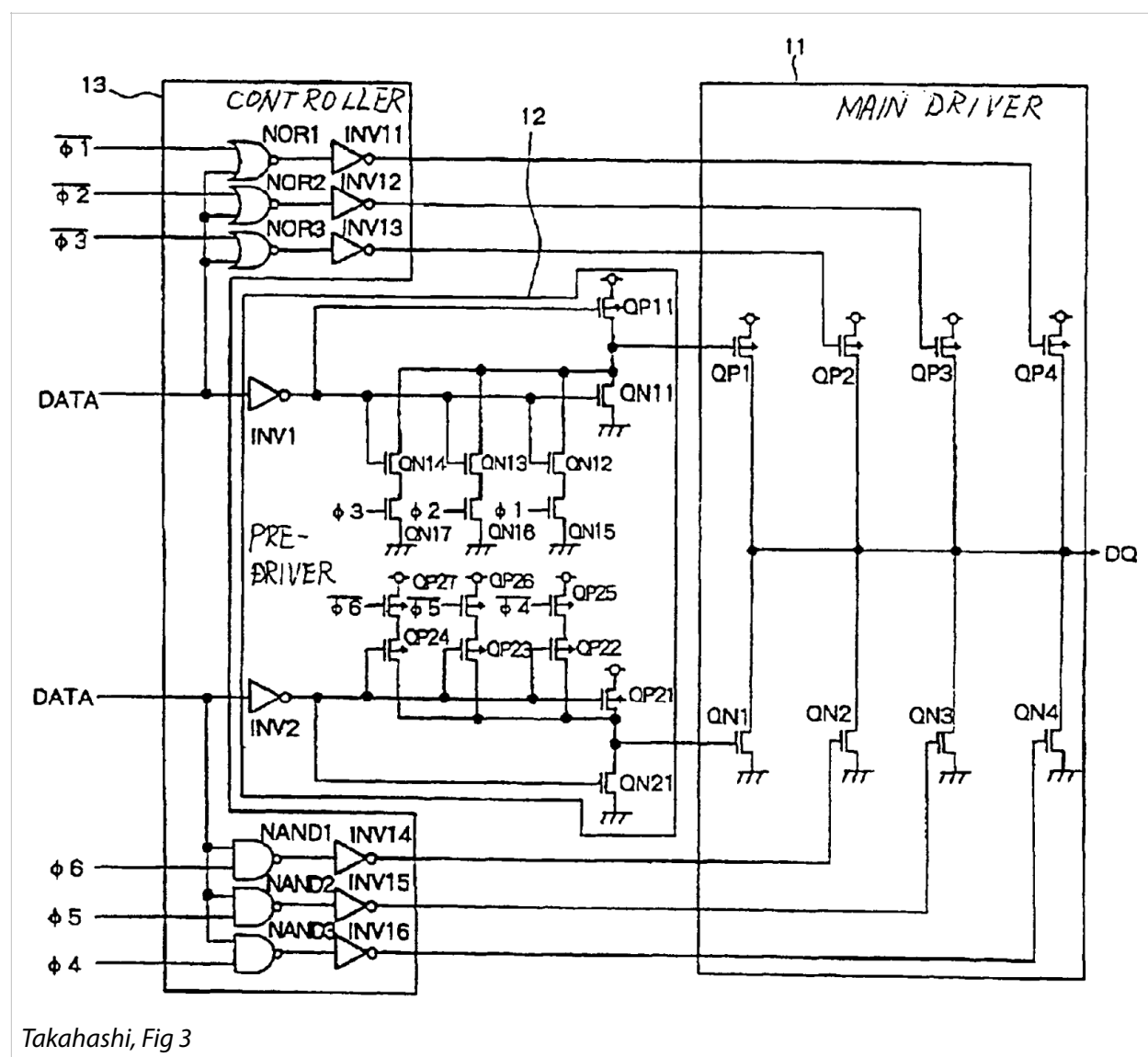
***Since the output impedance and the rise and fall times of output pulses are simultaneously controlled***, the number of control signals and the steps of a testing process are made smaller than if the output impedance and the rise and fall times of output pulses were controlled independently of each other. Thus, *the manufacturing cost of the output buffer circuit is prevented from increasing*. [Takahashi, 3:24–30, emphasis added]

The system incorporating the output buffer circuit has its *performance capability increased because the slew rate is automatically improved by monitoring and adjusting only the output impedance of the output buffer circuit*. [Takahashi, 3:31–34, emphasis added]

(86) This understanding is consistent with the specification's embodiments, each of which shows an output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate. As described previously, Takahashi explains that adjustments are made simultaneously to both the slew rate and the output impedance (drive strength), which configures the output buffer circuit for outputting data at a predetermined output impedance and

slew rate. In the following example, Takahashi explains how this is done, regarding

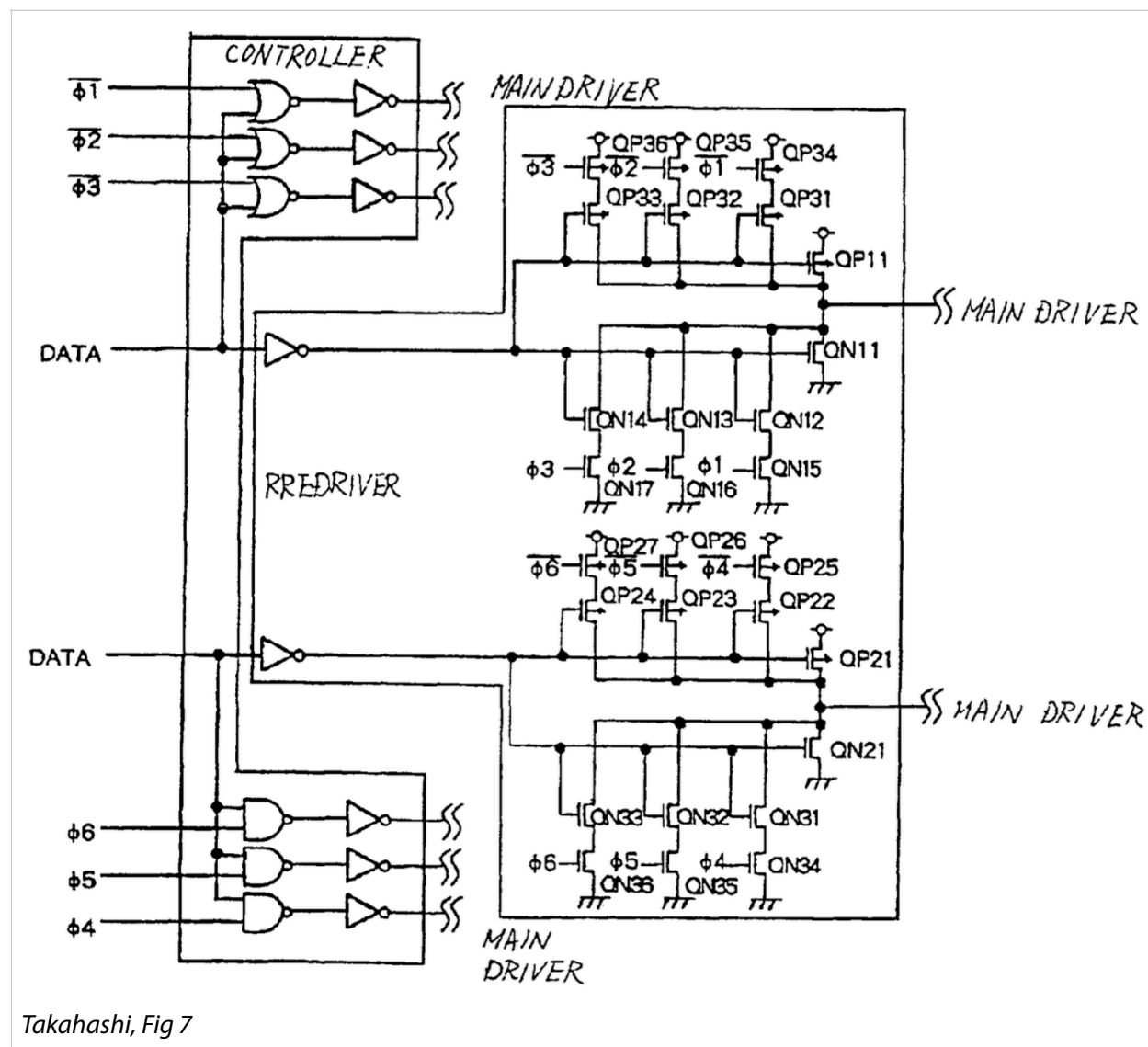
Figure 3:



In the present embodiment, the output impedance is adjusted and the ratio  $tr/tf$  [slew rate] are adjusted simultaneously. For example, when control signal  $\phi 1$  is rendered low and control signal  $\phi 4$  is rendered high in order to lower the output impedance by one stage, control signal  $\phi 1$

which is an inversion of control signal  $\phi 1$  goes high, turning on nMOS transistors QN12, QN15, and control signal  $\phi 4$  which is an inversion of control signal  $\phi 4$  goes low, turning on pMOS transistors QP22, QP25. Therefore, the ratio  $t_r/t_f$  [slew rate] is reduced by one stage. Similarly, when the output impedance is lowered by two stages, the ratio  $t_r/t_f$  [slew rate] is reduced by two stages, and when the output impedance is lowered by three stages, the ratio  $t_r/t_f$  [slew rate] is reduced by three stages. The output impedance and the rise time  $t_r$  at the time the high-level data is output and the output impedance and the rise time  $t_f$  at the time the low-level data is output can be adjusted independently of each other. [Takahashi, 8:4–19, emphasis added]

(87) Takahashi's second embodiment, illustrated in Figure 7, is similar in this regard to the first. The figure and its related description are given below.



Takahashi, Fig 7

An output buffer circuit according to a second embodiment of the present invention will be described below with reference to the drawings.

As shown in FIG. 7, the output buffer circuit according to the second embodiment includes, in addition to the components of the predriver of the output buffer circuit according to the first embodiment shown in FIG. 3, pMOS transistors QP31 through QP33 for increasing the driving capability of the pMOS transistor QP11 for

driving the pMOS transistor QP1, pMOS transistors QP34 through QP36 for turning on and off pMOS transistors QP31 through QP33, nMOS transistors QN31 through QN33 for increasing the driving capability of the nMOS transistor QN21 for driving the nMOS transistor QN1, and nMOS transistors QN34 through QN36 for turning on and off nMOS transistors QN31 through QN33.

*pMOS transistors QP34 through QP36 are controlled by respective control signals  $\phi 1$  through  $\phi 3$ , and nMOS transistors QN34 through QN36 are controlled by respective control signals  $\phi 4$  through  $\phi 6$ . Therefore, the ON/OFF states of pMOS transistors QP31 through QP33 are controlled at the same timing as nMOS transistors QN12 through QN14 shown in FIG. 3, and the ON/OFF states of nMOS transistors QN31 through QN33 are controlled at the same timing as pMOS transistors QP22 through QP24 shown in FIG. 3. Other structural and operational details of the output buffer circuit according to the second embodiment are identical to those of the output buffer circuit according to the first embodiment, and will not be described below. [Takahashi, 9:37–65, emphasis added]*

## **V. RESPONSE TO CLAIMS ANALYSIS IN '539 PETITION**

(88) In this section, I respond to the technical-expert analysis presented in the report titled “Declaration of Dr. Scott E. Thompson under 37 C.F.R. §1.68 in Support of Petition for *Inter Partes* Review” (“Thompson Report”). The Thompson Report and '539 Petition present effectively the same analysis.

### **A. Overview of the Prior Art Used for Grounds 2 and 3: United States Patent No. 6,924,66 ('Itoh')**

(89) The following section describes Itoh, the primary prior-art document used in Dr. Thompson's analysis for Grounds 2 and 3.

(90) Itoh presents a buffer circuit that allows one to adjust the slew rate of the output signal as well as the impedance with respect to the buffer's output terminal.

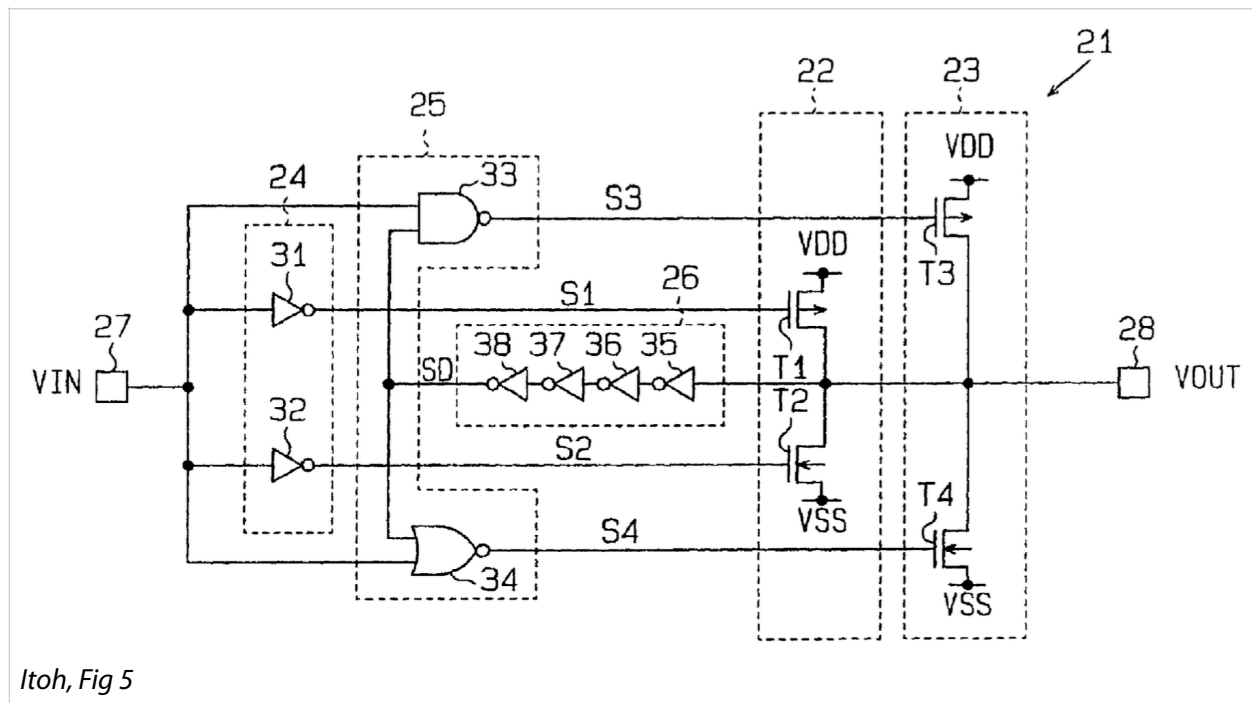
Itoh describes the system:

The present invention relates to an output buffer circuit, and, more particularly, to an output buffer circuit that outputs an output signal having gentle rising and falling edges and a slew-rate control type output buffer circuit.

For example, an interface, such as USB (Universal Serial Bus), which is used to connect a computer to a keyboard and achieves slow data transfer, is equipped with an output buffer circuit which has long signal rising and falling times. The use of a signal which has long

rising and falling times makes it unnecessary to provide a bus cable with a shield for preventing undesirable radiation. [Itoh, 1:6–15]

(91) An example of the output buffer is shown below:



(92) Itoh describes the operation of this buffer as follows:

FIG. 5 is a schematic circuit diagram of an output buffer circuit 21 according to the first embodiment of the present invention. The output buffer circuit 21 has first and second drive circuits 22 and 23, first and second control circuits 24 and 25, and a delay circuit 26. The output buffer circuit 21 receives an external input signal VIN from an input terminal 27 and generates an external output signal VOUT which has gentle rising and falling edges corresponding to a predetermined specification. The output buffer circuit 21 outputs the

external output signal VOUT from an output terminal 28. The output buffer circuit 21 has a low impedance characteristic with respect to the output terminal 28.

The first drive circuit 22 generates the external output signal VOUT that has gentle rising and falling edges corresponding to a predetermined specification, and the second drive circuit 23 is provided for the low impedance characteristic.

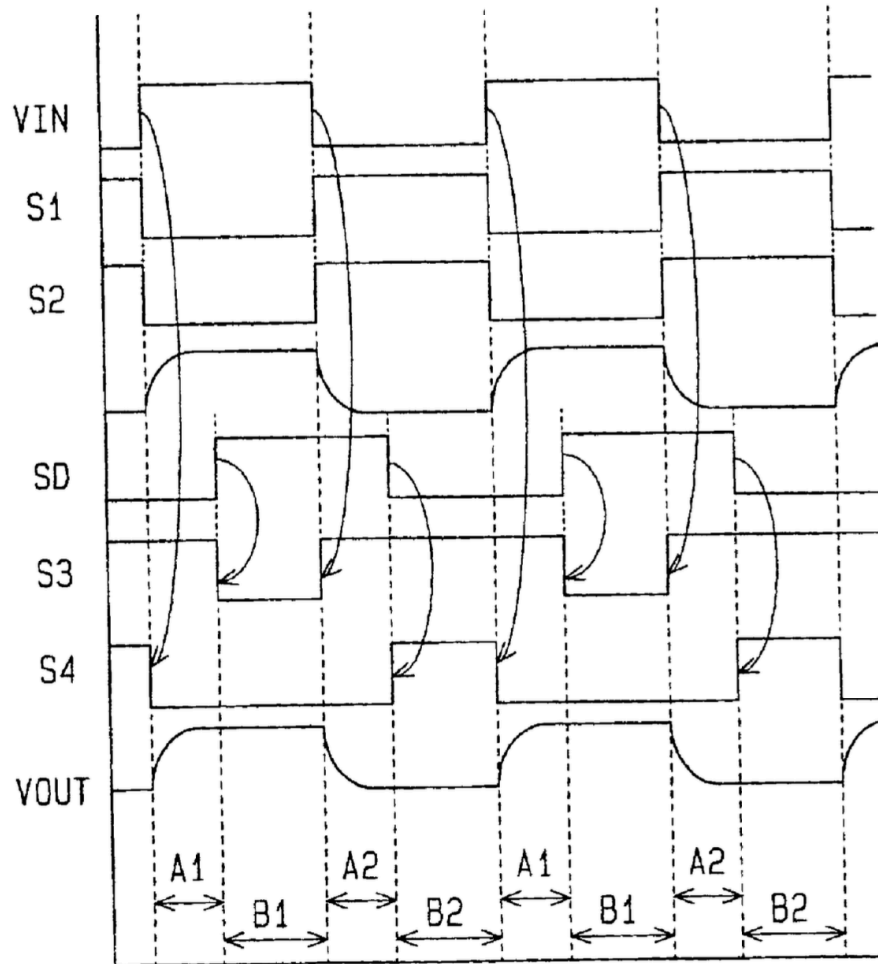
The first drive circuit 22 includes a PMOS transistor (first output transistor) T1 and an NMOS transistor (second output transistor) T2, connected in series between a high-potential power supply VDD and a low-potential power supply VSS. The output transistors T1 and T2 have transistor sizes (gate widths) set such that the external output signal VOUT gently rises and falls in response to a sudden change in the input signal VIN. That is, the output transistors T1 and T2 have the transistor sizes so set as to have a high impedance characteristic. A first control signal S1 from the first control circuit 24 is applied to the gate of the first output transistor T1, and a second control signal S2 from the first control circuit 24 is applied to the gate of the second output transistor T2.

The second drive circuit 23 includes a PMOS transistor (third output transistor) T3 and an NMOS transistor (fourth output transistor) T4, connected in series between the high-potential power supply VDD and the low-potential power supply VSS. ***The output transistors T3 and T4 have transistor sizes (gate widths) so set as to have a low impedance characteristic when the external output signal VOUT is in a static state.*** A third control signal S3 from the second control circuit 25 is applied to the gate of the third output transistor T3, and a fourth control signal S4 from the

second control circuit 25 is applied to the gate of the fourth output transistor T4. [Itoh, 6:59–7:34, emphasis added]

(93) An important aspect of Itoh is that the relevant drive transistors in the secondary drive circuit 23 (the second stage of the driver, comprising drive transistors T3 and T4) are not activated until “the external output signal VOUT is in a static state.” This is highlighted in the extract above.

(94) Itoh confirms this understanding by presenting the control-signal waveforms in figure 6 with an accompanying description:



Itoh, Fig 6

(95) Itoh describes this as follows:

First, a description will be given of the case where the external input signal VIN rises to the H level (the level of the high-potential power supply VDD) from the L level (the level of the low-potential power supply VSS). ***In this case, the period from the point of a***

***change in the external output signal VOUT to the point of a change in delay signal SD is set as a first period (period A1 in FIG. 6), and a period after the delay signal SD changes is set as a second period (period B1 in FIG. 6).***

**[First Period]**

In response to the rising of the input signal VIN, the first control circuit 24 causes the first and second control signals S1 and S2 to fall, thus turning on the first output transistor T1 and turning off the second output transistor T2.

The second control circuit 25 outputs the H-level third control signal S3 and causes the fourth control signal S4 to fall in response to the rising of the input signal VIN. This keeps the third output transistor T3 turned off and turns off the fourth output transistor T4. As a result, the first output transistor T1 having a high impedance characteristic causes the external output signal VOUT to slowly rise to the H level from the L level.

In the first period, the first and second output transistors T1 and T2 may be turned on simultaneously. As the output transistors T1 and T2 have a high impedance characteristic, however, the amounts of currents flowing in the output transistors T1 and T2 are smaller than the amounts of currents flowing in the conventional output transistors TP1 and TN1 that have a low impedance characteristic.

**[Second Period]**

In response to the rising of the delay signal SD, the second control circuit 25 causes the third control signal S3 to fall, thus turning on the third output transistor T3. The ON action of the third output transistor T3 causes the output buffer circuit 21 to have a low-output impedance characteristic. As apparent from the above, the fourth output transistor T4 is turned off first and then the third output

transistor T3 is turned on after a predetermined time elapses.

Therefore, the output transistors T3 and T4 are not turned on simultaneously, so that the through currents that flow in the output transistors T3 and T4 are almost zero. [Itoh, 8:8–49, emphasis added]

(96) Again, as both the figure and the passage demonstrate, the relevant transistor in the secondary driver circuit, drive transistor T3, which responds to control signal SD, does not turn on until after the output stabilizes — this is during the B1 range of time, during which VOUT has stabilized at a ‘1’ voltage state. Therefore, because it happens after the output has stabilized, the turning on of drive transistor T3 in response to the SD control signal does not affect the output in either voltage level or slew rate. An analogous region of time, B2, corresponds to the time during which VOUT has stabilized at the ‘0’ voltage state, and drive transistor T4 is turned on.

(97) Itoh explains that the point of activating the secondary driver after the output has stabilized is “so that a variation in the transition time of the output signal VOUT becomes smaller due to the low impedance characteristic of the second drive circuit 23 in the static state of the output signal VOUT.” This is highlighted in the passage below:

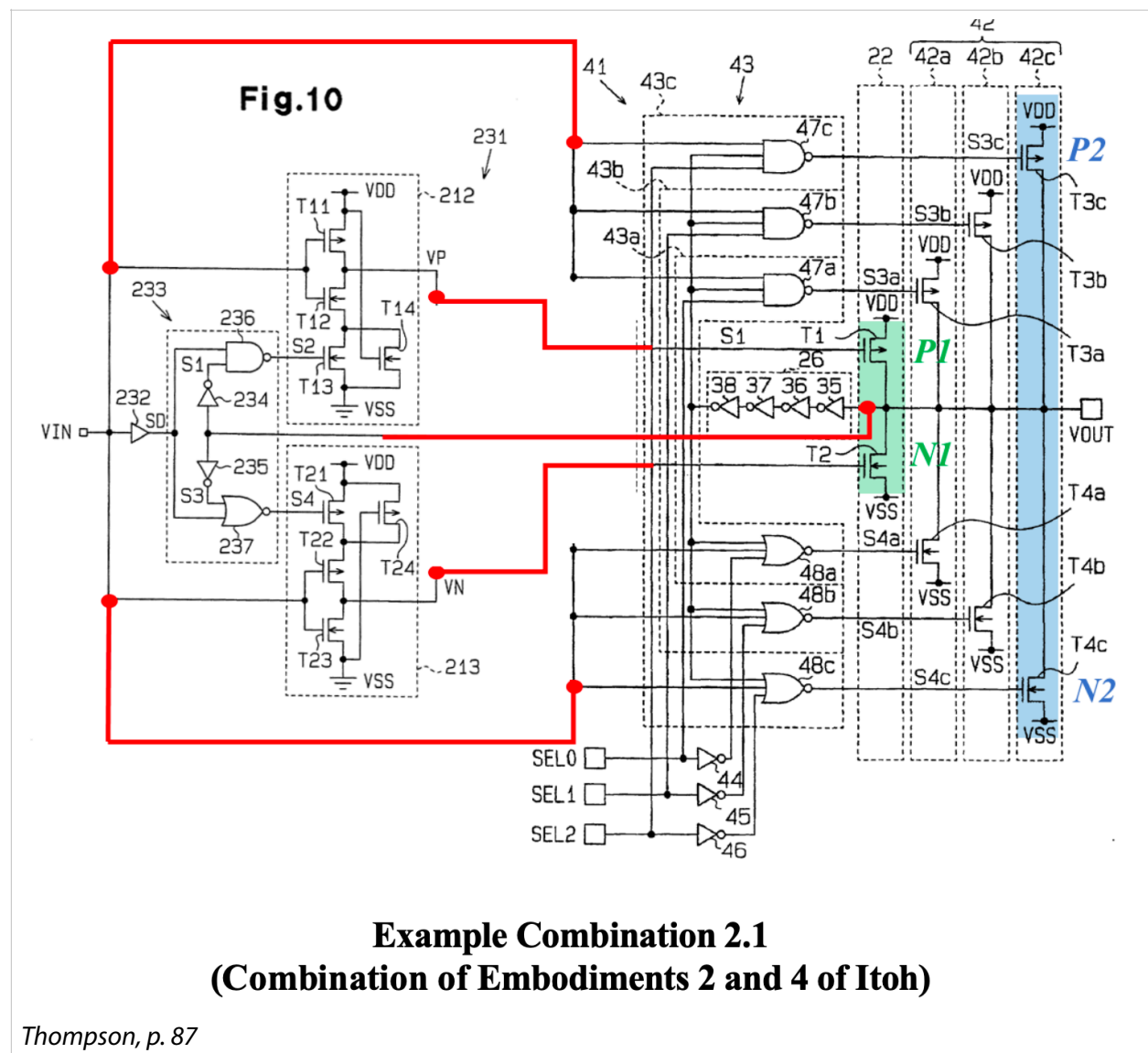
(1) The first drive circuit 22 generates the signal VOUT having a gentle waveform in response to the input signal VIN having a sharp

waveform, and ***the second drive circuit 23 has a lower output impedance than the first drive circuit 22. The first and second control circuits 24 and 25 drive the second drive circuit 23 after the output signal VOUT is sufficiently changed by the first drive circuit 22*** in response to the input signal VIN and the delay signal SD from the delay circuit 26. The control signals S1 and S2 that are applied to the gates of the respective output transistors T1 and T2 of the first drive circuit 22 are unlikely to be affected by production variations. Consequently, the first drive circuit 22 generates the output signal VOUT having a gentle waveform ***so that a variation in the transition time of the output signal VOUT becomes smaller due to the low impedance characteristic of the second drive circuit 23 in the static state of the output signal VOUT.*** [Itoh, 9:41–58, emphasis added]

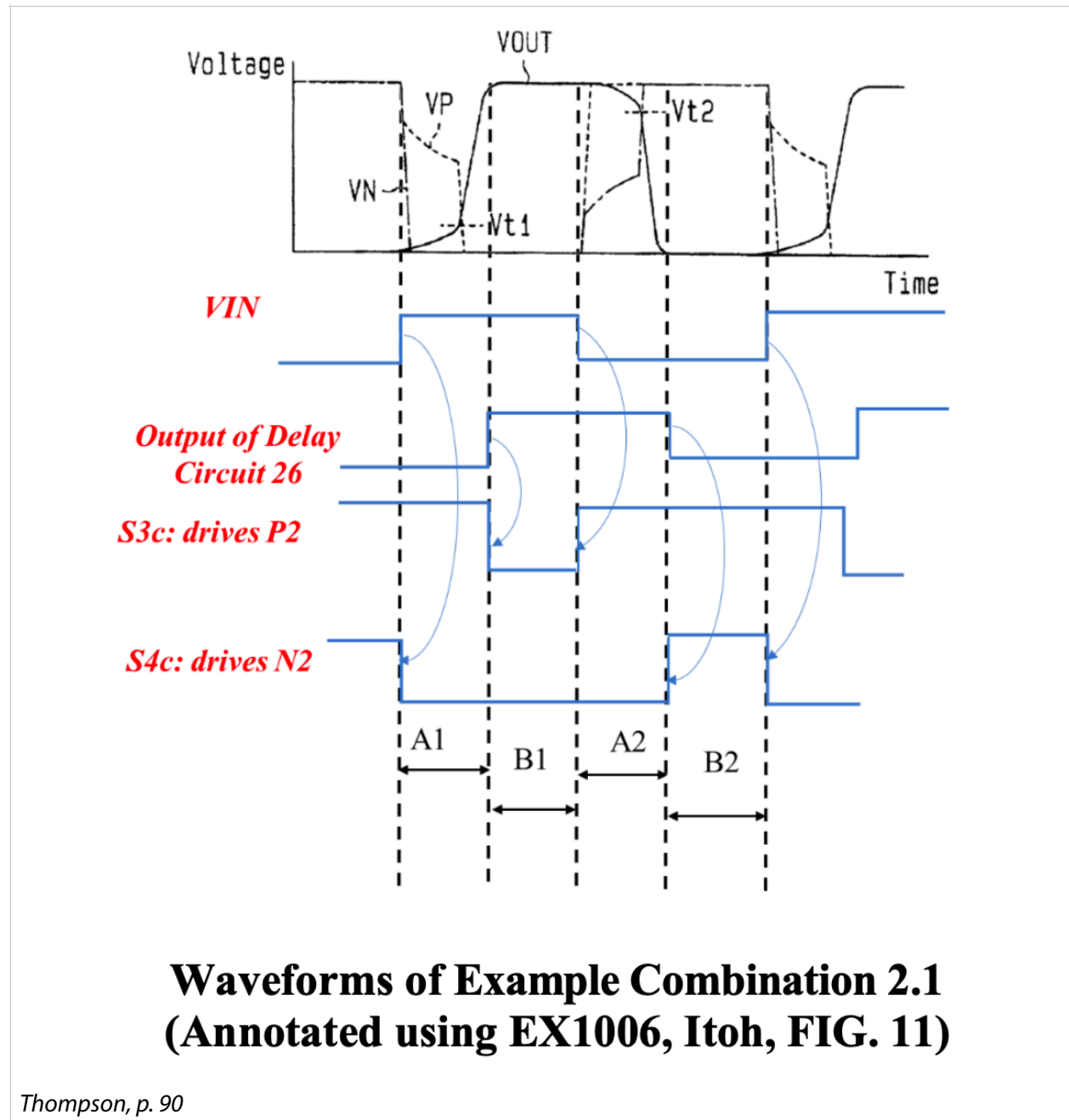
(98) Again, Itoh says that the point of the secondary driver is to reduce further variations in the output *after* the output buffer has transitioned its output to a steady-state value (either a ‘1’ value or a ‘0’ value, a high voltage or a low voltage). Its activation ensures that the signal transition has finished. This is an important aspect of Itoh: the secondary output driver comprising the output transistors T3 and T4 is not turned on until the B1 and B2 time periods, representing a time period after the output transition (VOUT transitioning from low to high or high to low) and during which the output VOUT is stable. As will be seen in the next section, Dr. Thompson confirms this understanding.

**B. The Proposed Combinations of Itoh With Itself (Ground 2) and Itoh With Muljono (Ground 3)**

(99) Dr. Thompson proposes a combination of Itoh with itself in the Ground-2 analysis. His proposed circuit is shown below:



(100) Dr. Thompson explains the behavior of his circuit using the following waveform:



(101) Dr. Thompson explained that the figure was created by combining Itoh's figures 6 and 11. From Dr. Thompson's deposition:

Q Can you turn to Page 90 of your declaration. And there's a figure just above Paragraph 188 there.

A Yes.

Q So this is an annotation of Itoh's Figure 11; is that correct?

A That is correct. This comes from Itoh Figure 11, correct.  
[Thompson depo, pp. 13–14]

(102) Dr. Thompson confirms that the relevant output drive transistors P2 and N2 are not turned on during the transition periods A1 and A2 and are only turned on during the periods B1 and B2 when the output VOUT is stable:

187. The waveforms of Example Combination 2.19 below illustrate the details of how the pair of P2 and N2 (driven by signals S3c and S4c) drives the load in coaction with the pair of P1 and N1. Specifically, ***P2 and N2 are turned off during periods A1 and A2***, during which period P1 and N1 are controlled by VP and VN (generated based on VOUT) for slew rate control. ***During B1 and B2 when VOUT is substantially stable, P2 and N2 are turned on for output impedance control.*** Each of VP, VN, S3c, and S4c for

controlling P1, N1, P2, N2 are generated based on both VIN and VOUT. [Thompson, p. 89, emphasis added]

**C. Rebuttal: Takahashi Did Not Intend for the Secondary Driver Stages To Be Turned Off During Buffer Operation and Then Turned Back on Immediately Afterward**

(103) Dr. Thompson uses a mechanism (the output buffer of Itoh) that adjusts output impedance on every single transition (every time a bit is output by the driver), at the end of the transition, to hold the output constant. Takahashi on the other hand, adjusts output impedance only once per recalibration (e.g., once at system startup) and does so to set the drive strength of the output buffer. Itoh's output buffer works very differently than that of Takahashi. They use different circuits, different techniques, different timing of the control signals, and achieve different ends, but because they use the same word ("impedance"), Dr. Thompson is able to fit a square peg into a round hole and make it look like Itoh renders Takahashi obvious. A person of ordinary skill would not have believed that Itoh's invention is the same as Takahashi's — they solve different problems and go about it in different ways.

(104) Claim 4 is therefore valid. The following section discusses this in more detail.

**1. “At a Predetermined Output Impedance” Means What It Says**

(105) As described earlier, it would have been clear to a person of ordinary skill that Takahashi's output buffer was intended to have the same output impedance over an entire output pulse train — a person of ordinary skill would **not** have understood that Takahashi's output buffer was intended to be reconfigured in the middle of an output pulse train. The person of skill would have understood that the reconfiguration of the output impedance of Takahashi's output buffer was intended to be performed either once at system start-up, or periodically on timescales appropriate to changes in ambient temperature and power-supply fluctuations, which are many millions of times longer than an output pulse.

(106) Claim 1, from which Claim 4 depends, includes the language “at a predetermined output impedance” to describe what the circuit is supposed to do and how it is supposed to behave:

1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

(107) The claim requires that the output buffer output its data “at a predetermined output impedance.” Given the preamble, a person of ordinary skill would have understood that the impedance and slew rate would both be *predetermined* with

respect to a given *pulse train* that is output from the output buffer circuit of Claim 1. Itoh does not do this; Itoh outputs each and every data pulse of its pulse trains at two different output impedance values, and Dr. Thompson admits this.

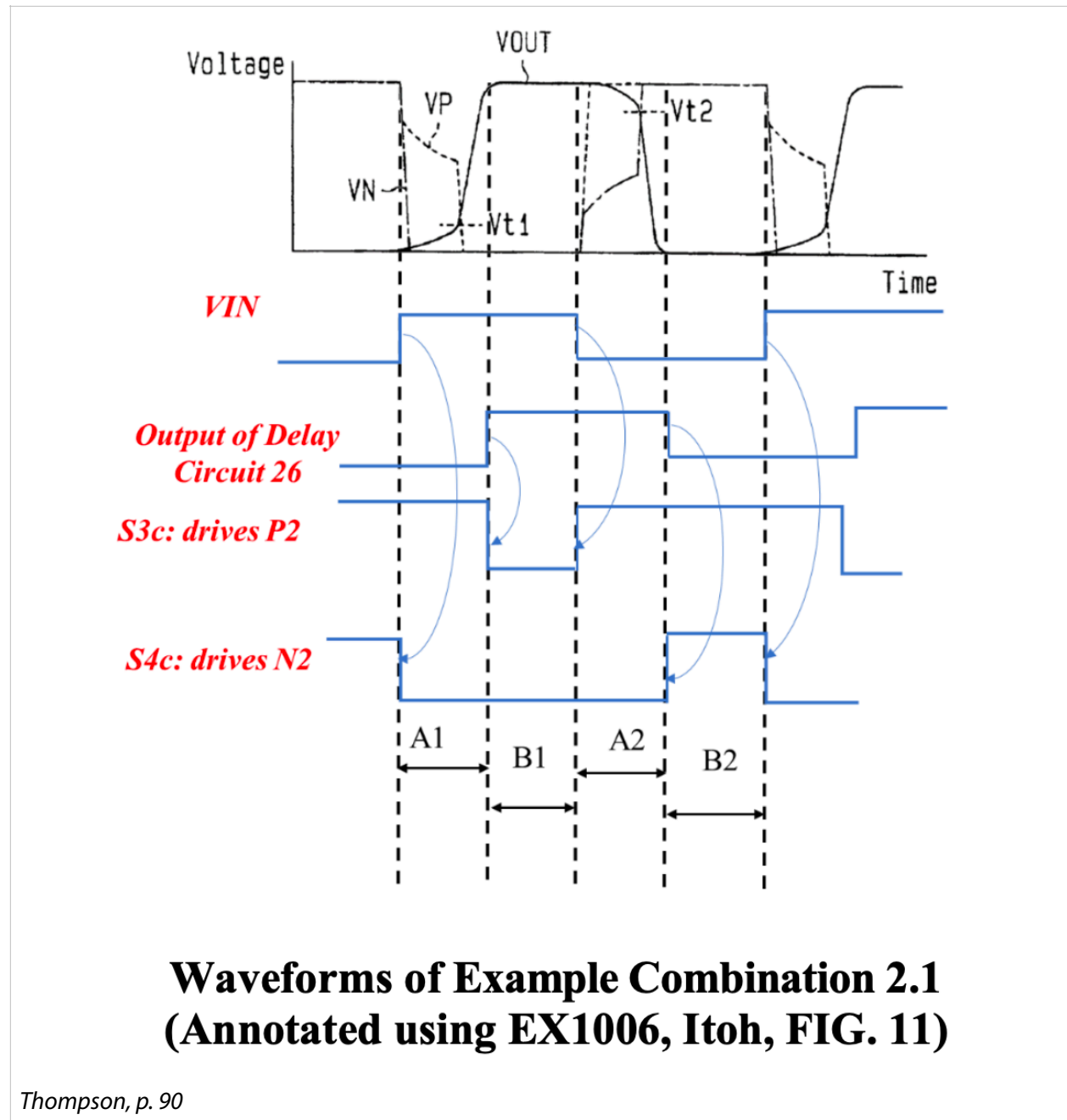
Q Okay. Does the output impedance of the system change between A1 and B1?

A Yes.

Q Why does the output impedance change between A1 and B1?

A For the same reason I discussed earlier. S3C is changing from A1 to B1. When S3C is low, Transistor P2 now becomes low resistance. In the time of A1, S3C is high. And in that case, the transistor is off so it has high resistance. So a transistor in this application is a voltage controlled resistor and that's why the impedance is changing. [Thompson depo, p. 16]

(108) Recall Dr. Thompson's timing diagram from earlier, which is what he is describing in the passage above:



(109) As Dr. Thompson explains, each A/B pair (A1/B1 and A2/B2, etc) is the time during which the output buffer drives the input waveform value from  $V_{IN}$  to the output as  $V_{OUT}$ . So each A/B pair represents a single bit — the A period represents the transition from low to high or high to low, and the B period is the

time during which the signal has finished its transition and is stable ... it is during this stable period that the receiver circuit at the other end can capture the data.

(110) Dr. Thompson fully admits that the impedance of the output buffer changes from high impedance to low impedance during the B period, and then goes back to high impedance during the next A period. Thus, Itoh does not drive its output pulse train “at a predetermined output impedance” but instead drives *each bit* of its pulse train at *two different* output impedance values. Dr. Thompson’s output buffer circuit, for outputting data in the form of an input pulse train, does not output the data at a predetermined output impedance but instead outputs the data at *two different* output impedance values every time it is operated.

(111) This clearly fails to meet the claim language. Claim 4 is therefore valid.

Executed on Wednesday, June 19, 2024 in Annapolis, Maryland



Dr. Bruce Jacob