

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES,	)	
INC.,	)	
	)	
Petitioner,	)	
	)	Case No.
vs.	)	IPR2023-01286
	)	
LONGITUDE LICENSING LTD.,	)	
	)	
Patent Owner.	)	
_____	)	

REMOTE VIDEOTAPED DEPOSITION OF SCOTT E. THOMPSON, Ph.D.
WEDNESDAY, MAY 15, 2024, 9:08 A.M.

STENOGRAPHICALLY REPORTED BY:
Tami L. Le, CSR No. 8716, RPR
Job No. 98690

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I N D E X

WITNESS: SCOTT E. THOMPSON, Ph.D.

EXAMINATION

PAGE

By Mr. Milkey

6

PREVIOUSLY MARKED EXHIBITS:

Exhibit 1001 (Not attached)

19

Exhibit 1003 (Not attached)

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1 WEDNESDAY, MAY 15, 2024, 9:08 A.M.

2 oOo

3 THE VIDEOGRAPHER: Okay. We are on the
4 record. This is the beginning of Media No. 1 in the
5 deposition of Scott Thompson, Ph.D., in the matter
6 of Western Digital versus Longitude Licensing. The
7 case number is IPR2023-01286, being held remotely
8 via Zoom on May 15th, 2024 at 9:08 a.m.

9 The court reporter is Tami Le, and I am
10 Steven Henry, videographer, on behalf of First Legal
11 Depositions located in Los Angeles, California.
12 This deposition is being videotaped at all times
13 unless specified to go off the record.

14 Would all counsel please identify
15 themselves and state whom you represent, beginning
16 with the noticing attorney.

17 MR. MILKEY: This is James Milkey on behalf
18 of patent owner Longitude Licensing with the law
19 firm of Russ August & Kabat.

20 MS. SHI: This is Hong Shi from Haynes and
21 Boone on behalf of Western Digital.

22 MR. O'DELL: This is David O'Dell from
23 Haynes and Boone on behalf of Western Digital.

24 THE VIDEOGRAPHER: Thank you.

25 Will the court reporter please administer

1 the oath.

2 (Witness sworn.)

3 THE VIDEOGRAPHER: You may begin.

4

5 SCOTT E. THOMPSON, Ph.D.,
6 having been first duly sworn, was
7 examined and testified as follows:

8

9 EXAMINATION

10 BY MR. MILKEY:

11 Q Hello, Dr. Thompson. What time zone are
12 you currently in?

13 A Eastern Standard Time.

14 Q Okay. Well, good afternoon, and thank you
15 for accommodating the later start time.

16 Have you been deposed before?

17 A Yes.

18 Q Approximately how many times?

19 A Over -- over ten.

20 Q Okay. Were -- were all of your depositions
21 in patent litigation matters?

22 A No.

23 Q What other types of proceedings have you
24 been deposed in?

25 A The -- one other one was security fraud.

1 It was a civil -- no. What are -- what are those
2 things called? Class action suit, and it was on
3 security fraud.

4 Q Okay.

5 A On related chips.

6 Q Is that the only deposition that you've
7 provided in a case that was not a patent litigation
8 proceeding?

9 A From memory, I believe that's correct.

10 Q Okay. Have you ever given a deposition in
11 which you testified on behalf of the patent owner?

12 A Yes.

13 Q Could you turn to Paragraph 170 of your
14 declaration.

15 MR. MILKEY: And for the record, that is
16 Exhibit 1003.

17 THE DEPONENT: I am there.

18 BY MR. MILKEY:

19 Q All right. And this is the start of your
20 analysis for Ground 2 regarding the obviousness of
21 Claims 1 through 8 over Itoh.

22 Do you see that?

23 A I do.

24 Q Okay. So in -- in this ground, you propose
25 combining two embodiments of Itoh; is that correct?

1 A I combined Figure, I believe, 8 and 10,
2 correct.

3 Q Okay. And how do you propose combining
4 Figures 8 and 10 of Itoh?

5 A If you look at the bottom of Paragraph 174,
6 there's a figure showing the combination. In
7 Figure 8, there's a red box that I've highlighted.
8 Inside that red box are two inverters. That's a
9 very simple circuit. It's labeled 24 in Figure 8.
10 That's a controller.

11 So all I'm doing combining these is taking
12 the controller in Figure 10, which is a more complex
13 controller, giving you more capability, and
14 replacing the controller of 24, which is a very
15 simple controller.

16 Q Okay. So what is the benefit of adding the
17 more complex controller of Figure 10 into the more
18 simple circuit of Figure 8?

19 A It gives you more options to compensate for
20 process, voltage, and temperature.

21 Q And then so Figure 10 standing alone is a
22 separate embodiment from Figure 8; correct?

23 A I mean, Figure 10 is an output buffer just
24 like Figure 8 is an output buffer. They have
25 different control knobs. And Itoh talks about these

1 two independently, but that's just for
2 clarification.

3 At this time I -- I worked for Intel in
4 this time frame. Muljono is one of the other prior
5 arts well before the '539. That's a 1998 patent.
6 It was my business at Intel to work on Apple
7 buffer -- that's a fundamental circuit and all
8 integrated circuits -- and my job at Intel was to
9 provide process files that describe how transistors
10 operate over the range of process variation,
11 temperature variation, and voltage variation that
12 our products would see.

13 And so at a high level, this is the -- a
14 fundamental building block of integrated circuits.

15 (Reporter seeks clarification.)

16 A And in this time frame, because the voltage
17 supply is getting smaller, you need more and more
18 control knobs to get it to perform according to the
19 business conditions and design conditions you need
20 for a commercial product.

21 Q Okay. Understood.

22 So my question is what benefit does -- so
23 we've talked a little bit about the benefit of
24 supplementing the Figure 8 embodiment with
25 Figure 10. My question is what is the benefit of

1 adding the functionality of Figure 8 to Figure 10?

2 A There's many. So I'll give you one
3 example. So what figure -- what the better
4 controller in Figure 10 is doing when you replace it
5 with 24, it's turning on the voltage at T1 and T2
6 slower. It turns on transistors P1 and P2 slower.
7 And as taught earlier by Itoh, if I turn them on
8 slower, I can use a bigger transistor there.

9 And so it allowed me to use a bigger
10 transistor there that had the advantages for lower
11 output impedance. When I use a bigger transistor
12 for P1 and P2, I can now use smaller transistors for
13 the subdrivers that are the -- labeled 42a, b, and
14 c. So there's many advantages of combining these
15 two, and as Muljono tells us, it was commonplace and
16 it was common business practice to do that well
17 before the '539 patent.

18 Q Okay. So what I'm asking specifically is I
19 understand that Figure 10 provides some advantages.
20 But what is -- what is the advantage of -- for
21 example, why wouldn't you simply just use Figure 10?
22 Why do you need to use Figure 8 in your combination?

23 A If I only have Figure 10, I don't have as
24 much control in terms of adjusting output impedance.
25 If you looking at Figure 10, there is no other

1 drivers on the output node other than P1 and N1.
2 When I go to -- when I now combine them with
3 Figure 8, I have three additional drivers that I can
4 use to adjust the impedance.

5 And so, for example, let's assume under
6 process variation I was targeting a device size
7 which is equal to a transistor gate width of ten
8 microns for, let's say, P1. If the process turns
9 out and delivers only nine microns of transistor
10 width, I want to correct it back to ten. And so I
11 could have a one micron width in P2 in circuit 42 to
12 turn that on to now compensate if my device in
13 Figure 10, the output transistor was on the small
14 side.

15 So it gives you far better control of
16 hitting your design parameters, and there's a host
17 of design parameters you have to hit for a
18 commercial circuit. Not only output impedance, not
19 only slew rates, rise and fall time, the ratio of
20 rise and fall time, cross point, all of them have to
21 be targeted on a commercial high-speed chip.

22 Q Okay. So I appreciate the level of detail.
23 Is it fair to say that at a high level, the -- the
24 components of Figure 8 allow additional control over
25 output impedance?

1 MS. SHI: Objection; misstates the
2 testimony.

3 MR. MILKEY: I wasn't stating his
4 testimony. I'm asking a question. Please limit
5 your objections to form.

6 BY MR. MILKEY:

7 Q So I'll just re-ask the question for the
8 record.

9 I appreciate your previous level of detail.
10 Is it fair to say that at a high level, the
11 components of Figure 8 allow additional control over
12 output impedance?

13 A Figure 8 adds additional control. It adds
14 other things more than that, but -- but
15 the -- Driver 42 gives you additional level of
16 control. You have three additional drivers you can
17 turn on if needed, and you can adjust the sizes of
18 them depending on your design criteria.

19 Q Okay. Thank you.

20 So at -- is Driver -- you mentioned
21 Driver 42. Are those the components 42a, 42b, and
22 42c depicted in Itoh's Figure 8?

23 A Right. In Figure 8, on the output node,
24 which is labeled "VOUT," there's Drivers 22 and 42,
25 and 42 is made up in this embodiment of three

1 subdrivers: 42a, 42b, 42c.

2 Q Okay. And in your proposed combination, at
3 what moments in time is Driver 42 active?

4 A The teaching of Itoh activates 42 on a
5 delay. You see the output -- the output node is
6 routed back through three inverters, 35, 36, 37, 38,
7 up to AND gates to control PMOS's and down -- run it
8 down to NOR gates to control NMOS's. So the drivers
9 42a, b, and c are designed to turn on after the rise
10 or fall of the outputs.

11 Q Okay. In your proposed combination of
12 Figure 8 with Figure 10 of Itoh, how is the slew
13 rate controlled?

14 A It's controlled in a few different ways.
15 The -- the Figure 10 controller affects the turn on
16 of P1 and N1. And so that -- they turn on slowly so
17 you get a slow skew -- slow slew rate.

18 But as I said earlier, it's more
19 complicated than that. The size that you pick for
20 P1 and N1 are also going to affect the slew rate.
21 And this combination allows me to choose a bigger
22 transistor for P1 and N1. Because I turn them on
23 slowly, I can still have a slow skew -- a slow
24 slew -- slew rate.

25 Q Can you turn to Page 90 of your

1 declaration. And there's a figure just above
2 Paragraph 188 there.

3 **A Yes.**

4 **Q** So this is an annotation of Itoh's
5 Figure 11; is that correct?

6 **A That is correct. This comes from Itoh**
7 **Figure 11, correct.**

8 **Q** Okay. So where is the slew rate depicted
9 in this figure?

10 **A The slew rate is the rate of change of the**
11 **output voltage versus time. The units for that are**
12 **generally, you know, volts over nanosecond or volts**
13 **over microsecond. And so the slew is the slope of**
14 **the out. So if you look at the time period of A1,**
15 **VOUT is changing, and so the slope of that is your**
16 **slew rate during A1.**

17 **Q** So it looks like the slope is changing
18 during A1 and A2 and is relatively constant at B1
19 and B2; is that fair?

20 **A Yes. By design the rise and fall is over**
21 **when you transition from A1 to B1. There's a**
22 **circuit element, a delay element that denotes that,**
23 **and when you -- when the transition is over, the**
24 **circuit is designed then to switch on P2.**

25 **Q** Okay. And then at what moment in time do

1 the -- does the Driver 42 get turned on in this
2 figure?

3 A So if you look at the figure we started
4 with in Paragraph 183, Driver 42, I'm focused on P2
5 and N2 in 42c. And so what turns on P2 is a signal
6 called S3c. That goes to the gate. That driver
7 turns on when S3c is low.

8 If we now go back to the figure we were
9 looking at on Page 90, you see S32 [sic] labeled in
10 red. It says "drives P2."

11 (Reporter seeks clarification.)

12 A "Drives P2." And that transitions from
13 high to low at the start of B1.

14 Q And is the Driver 42 active during B2?

15 A When you say "Driver 42 active," I'm going
16 to restrict it to 42c on -- on P2. And so that
17 driver is active -- it's an act- -- P2 -- P2 is
18 active low. So any time S3c is equal to zero volts,
19 logic zero, that driver is -- is -- P2 is on. On is
20 generally what you mean by "active."

21 And so going back to the diagram on Page 90
22 again, you see S3c is low the entire time of B1. So
23 P2 is on the entire time of B1.

24 Q Okay. And so the Driver 42c is -- at least
25 in this diagram above Paragraph 188 of your

1 declaration, Driver 42c is off at every moment in
2 time other than the duration of B1; is that correct?

3 A That is not correct.

4 Q Okay.

5 A So it's not correct because the driver is
6 P2. S3c is the control signal that goes to the
7 driver.

8 Q Okay. Does the output impedance of the
9 system change between A1 and B1?

10 A Yes.

11 Q Why does the output impedance change
12 between A1 and B1?

13 A For the same reason I discussed earlier.
14 S3c is changing from A1 to B1. When S3c is low,
15 Transistor P2 now becomes low resistance.

16 In the time of A1, S3c is high. And in
17 that case, the transistor is off, so it has high
18 resistance. So a transistor in this application is
19 a voltage-controlled resistor, and that's why the
20 impedance is changing.

21 (Pause in proceedings.)

22 Q Okay. So in the annotated Figure 11 of
23 Itoh, how did you arrive at the timing diagrams for
24 S3c and S4c?

25 A Itoh provides them based on the delay

1 circuit -- these are a -- it's a self-timed circuit
2 going through Inverters 35, 36, 37, and 38. It's
3 designed to work such that P2 only turns on after
4 the -- the rise.

5 I just -- that's a pretty common trick to
6 use a self-timed circuit to control another circuit.
7 So the output node is actually telling you when S3c
8 should turn on. With a programmable delay, you can
9 make that longer or shorter based on the number of
10 inverters you have on the output node and also the
11 size of the inverters.

12 Q Okay. Okay. If you could go to
13 Paragraph 216 of your declaration on Page 106.

14 A I am here.

15 Q Okay. And this is the beginning of your
16 analysis for Claim 4.

17 Do you see that?

18 A I do, yes. Claim 4 for Ground 2.

19 Q Yeah.

20 Do you see that the last clause of Claim 4
21 reproduced just above Paragraph 216 refers to,
22 quote:

23 "...a small effect on rise and fall
24 times of pulses output from said main
25 driver"?

1 A I see that, yes.

2 Q Okay. What is your understanding of that
3 clause?

4 A It's not clear what is meant by a small
5 effect. Is that changing it by 1 percent?
6 5 percent? 10 percent? 20 percent? 40 percent?
7 There's nothing in the spec that helps me understand
8 what "small effect" means.

9 Q Okay. How did you apply "small effect" in
10 your analysis in this IPR?

11 A Itoh was a interesting case where P2 has a
12 negligible, zero, minuscule effect. And so I don't
13 need to define the boundary whether "small" is
14 1 percent, 2 percent, 3 percent. During the rise
15 and fall, P2 and N2 are often Itoh. So in all
16 transistor, all you have is leakage current there.
17 Leakage current is minuscule. The on current to off
18 current for these transistors, which I designed at
19 Intel in this time frame, we had to hit a spec of
20 1 million between on current and off current.

21 And so Itoh P2 and N2 have no effect on the
22 rise and fall because it's a transistor that's off
23 connected to that node. Now, it's not absolutely
24 zero, but it's .0000, more zeros, 1. That's how
25 small it is.

1 So we say it has no effect. In reality,
2 it's a minuscule effect. But for this example,
3 then, I can find -- I can find -- Itoh has a small
4 effect because no effect is a small effect.

5 Q Okay. And you've reviewed the
6 specification of the '539 patent; correct?

7 A I have.

8 Q Were there any -- were there any teachings
9 in the specification of the '539 patent that helped
10 you understand what the term "small effect" meant?

11 A Not for small effect on the rise and fall
12 times of the pulses.

13 Q And do you have a copy of the '539 patent?

14 A I do.

15 Q Okay. Could you open that? Again, this is
16 Exhibit 1001.

17 A I have it open.

18 Q And if you could go to Column 8, the
19 paragraph starting at Line 20.

20 A Yes, I'm here.

21 Q Okay. And do you see there it refers to
22 transistors -- I'm not going to quote the whole
23 thing, but generally it refers to transistors:

24 (As read) "...whose effect on the
25 ratio t_r over t_f is smaller than pMOS

1 transistor QP1 and nMOS transistor
2 QN1."

3 Do you see that?

4 A I see that.

5 Q Okay. Does this provide any guidance as to
6 what is meant by "small effect"?

7 A It does not. Remember the small effect
8 that's claimed is on the rise and fall time. This
9 is referring to a ratio of T rise over T fall, and
10 it's also using the word "smaller." I understand
11 the word "smaller." I don't understand what they
12 mean by "small."

13 Q Are there any disclosures in the '539
14 patent that provide specification support for a
15 transistor having a small effect on rise and fall
16 times of pulses output from the main driver?

17 A I could find nothing -- no support for what
18 is meant by "small effect" on the rises and fall
19 time of the output driver.

20 Q Okay. So also in Claim 4, there is a
21 reference to both a smaller device size and a
22 smaller gate width.

23 Do you see that?

24 A Let me just go to the claim here.

25 So I have the -- I have -- the patent open

1 again. Having a -- having --

2 (As read) "...transistors have a
3 smaller device size with a smaller gate
4 width..."

5 I see that, yes.

6 Q Okay. Is it -- is it your understanding
7 that "device size" and "gate width" have the same
8 meaning?

9 A In circuit design, it's the rule that
10 device size equals gate width. That's an understood
11 rule in circuit design. We can go into the reasons
12 why that would be, but, you know, in this time frame
13 I worked at Intel, that was our rule. I also worked
14 with Cypress after this time frame. That was the
15 rule at Cypress. I also worked with Fujitsu.
16 Fujitsu is the owner of the Itoh patent. I worked
17 with Fujitsu for six years. They are like
18 everywhere and I teach in my classes device size in
19 circuit design equals gate width, correct.

20 Q So it's your opinion that even though
21 "device size" and "gate width" are different terms,
22 they mean the same thing?

23 A No. I'm saying if you -- if you read
24 Claim 4, it says:

25 "...a smaller device size with a

1 smaller gate width..."

2 I'm saying a POSITA would understand that

3 as --

4 (Reporter seeks clarification.)

5 A A POSITA, a person of ordinary skill, would
6 understand that there's only one constraint there,
7 and that basically is smaller gate width.

8 Q And just for the record, when you're
9 referring to "POSITA," that's P-O-S-I-T-A?

10 A Yes.

11 If you'd like, I can give you background
12 why in circuit design device size equals gate width
13 if you'd like.

14 Q No. That's fine. I -- I think that you've
15 provided some helpful context there already.

16 My question is just specifically in the
17 context of this -- of this art and in the context of
18 this claim, it's your opinion that "device size"
19 means the same thing as "gate width"?

20 A Yes, because in a circuit that we're seeing
21 in the circuit pattern -- we're seeing
22 circuits -- there's no physical implementation of
23 those circuits. The only thing that's being modeled
24 there is an electrical model and the gate width of
25 the device to give you -- give you current.

1 The physical dimension of the device in
2 terms of XY area is not included in a circuit
3 configuration. That's assigned later in the design
4 flow with physical layouts when you include how you
5 do the body contact. So in the circuit design,
6 device size equals gate width.

7 Q And how are device size and gate width
8 related to output impedance?

9 A Gate width -- so the current equation of a
10 MOSFET for all modes, linear, saturation, off, the
11 current is proportional to gate width. So that
12 means the impedance and resistance are also
13 proportional to gate width.

14 So if I want to cut my impedance in half, I
15 double my width, my gate width. That's the
16 adjustable parameter that designers can use to
17 change the impedance. They adjust gate width.

18 Gate length, which is another process
19 parameter, is set by the process people --

20 (Reporter seeks clarification.)

21 A So circuit designers can only control
22 certain parameters. The technologists who design
23 the device control the gate length.

24 And so, for example, if you're doing a
25 quarter micron technology, at Intel I was the one in

1 my group who set the exact size of the transistor,
2 the gate length, and then we would take that and
3 tell the designers, "This is the length you have to
4 use for the nominal gate length."

5 And if a company like Apple wanted to
6 change the length below the nominal value, we would
7 never support that because our design data, our
8 qualification data, reliability data, short shock
9 effects data, linkage data would all be -- have been
10 developed for a given transistor length, nominal
11 length.

12 But designers are free to adjust the width
13 when they want to tune the circuit current or
14 impedance. So width is the key knob that a circuit
15 designer uses to control how much current a
16 transistor has, which translates into its impedance.

17 Q Okay. So if the transistors in -- turning
18 back to your combination of Figure 8 and Figure 10
19 in Itoh, if the transistors in 42c have a smaller
20 device size and gate width than the device size and
21 gate width of P1 and N1, how does that impact their
22 output impedance relative to P1 and N1?

23 A So we're -- we're looking at the figure in
24 Paragraph 183. And so I'm defining P1 as the first
25 driver in Block 22 and P2 in the -- the Subdriver 42

1 but particularly 42c. So that's my definition of
2 where -- what P1 and P2 are.

3 Now, in terms of output impedance, it
4 depends on the mode in terms of how much the output
5 impedance is going to affect P1. So how much does
6 P2 affect P1, it's going to depend on the mode of
7 operation. So when P2 is off and P1 is on, then the
8 output impedance is dominated by P1. And if I
9 change the size of P2, it's not going to have much
10 effect.

11 If they're both on and then I make P2
12 bigger, that node is going to reduce its impedance.

13 There's formulas of how you would add them
14 in -- in -- they would be in parallels. There's
15 ways to add them in parallel. So you can even
16 quantify how that -- how that would change the
17 impedance based on well-known circuit rules.

18 Q Okay. So when P2 is on, the output
19 impedance of the system will be reduced?

20 A Compared to when P2 is off, that's correct.
21 Output impedance is reduced.

22 Q So I understand that in your proposed
23 combination you propose that P2 and N2 would have a
24 smaller device size and gate width than P1 and N1.

25 Is it correct, though, that regardless of

1 what the size of P2 and N2 is in your proposed
2 combination, those transistors would have a small
3 effect on the rise and fall times of the output
4 pulses?

5 A P2 and N2 have a minuscule effect on the
6 rise and fall of the output pulses. As I explained
7 earlier, the control signal S3c does not turn on
8 either of those -- P2 -- or S4c does not turn on N2
9 until after the rise and fall is over.

10 Q And in Itoh's Figure 8, that would be true
11 regardless of whether the P2 and N2 transistors had
12 a smaller device size than the P1 and N1
13 transistors; correct?

14 A The turn on of P2 and N2, when they turn
15 on, it is independent of the size. The turn on of
16 that is controlled by S3c for P2 and S4c for N2.
17 And so transistors turn on based on that voltage,
18 not the size of the transistor.

19 Q If you could go to Paragraph 197 of your
20 declaration on Page 94.

21 A Okay.

22 Q And do you see that the claim language
23 reproduced here in Limitation 1.2.3 refers to:

24 (As read) "...one fifth n-channel
25 MOS transistor for driving said first

1 p-channel MOS transistor in coaction
2 with other transistors"?
3 What is your understanding of what is meant
4 by "coaction"?

5 **A Let me just read that for a second.**

6 **"Coaction" just means joint action.**

7 (Pause in proceedings.)

8 Q Okay. And just turning back to the figure
9 on Page 90 of your declaration, which is the
10 annotation of Itoh's Figure 11.

11 Let me know when you're there.

12 **A I'm here.**

13 Q Okay. At Time Periods A1, A2, and B2, does
14 the driver 42c in your proposed combination have any
15 impact on the output impedance of the system?

16 **A Driver 42c alters the impedance during B1**
17 **and B2, and it has a negligible effect, no effect**
18 **during A1 and A2.**

19 MR. MILKEY: All right. I have no further
20 questions.

21 MS. SHI: Okay. Can -- can we take a break
22 and maybe -- ten-minute break?

23 MR. MILKEY: Okay.

24 MS. SHI: Okay. So we will come back in
25 ten minutes.

1 THE VIDEOGRAPHER: Okay. We're going off
2 the record. The time is 10:03 a.m.

3 (Recess taken.)

4 THE VIDEOGRAPHER: Okay. We are back on
5 the record. The time is 10:10 a.m.

6 MS. SHI: I don't have any questions.
7 Thank you, everyone.

8 MR. MILKEY: Great. Thank you.

9 MS. SHI: We can go off record.

10 THE VIDEOGRAPHER: All righty. A
11 quick -- Mr. Milkey, would you like to order the
12 transcript for this?

13 MR. MILKEY: Yeah, if we could get a
14 five-business-day expedite, that would be great.

15 THE VIDEOGRAPHER: Okay. And for the
16 video?

17 MR. MILKEY: Oh, we don't need the video.

18 THE VIDEOGRAPHER: You don't need the
19 video. Okay. Then that concludes the deposition of
20 Scott Thompson, Ph.D. We are off the record at
21 10:11 a.m.

22 (The deposition concluded at 10:11 a.m.)

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-oOo-

I have read the foregoing deposition
transcript and by signing hereafter, approve same.

Dated _____ .

(Signature of Deponent)

1 CORRECTION SHEET/ERRATA SHEET

2

3 I, SCOTT E. THOMPSON, Ph.D., do hereby
4 certify that I have read the foregoing statement and
5 that, to the best of my knowledge, said statement is
6 true and accurate (with the exception of the
7 following changes listed below):

8

9 PAGE LINE CHANGE TESTIMONY TO READ AS FOLLOWS:

10 _____

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SCOTT E. THOMPSON, Ph.D.

1 DEPOSITION OFFICER'S CERTIFICATE

2

3 STATE OF CALIFORNIA)
4 COUNTY OF ORANGE) ss.

5

6

7 I, TAMI L. LE, hereby certify:

8 I am a duly qualified Certified Shorthand
9 Reporter in the State of California, holder of
10 Certificate Number CSR 8716 issued by the Court
11 Reporters Board of California and which is in full
12 force and effect. (Fed. R. Civ. P. 28(a)).

13 I am authorized to administer oaths or
14 affirmations pursuant to California Code of Civil
15 Procedure, Section 2093(b), and prior to being
16 examined, the deponent was first duly sworn by me.
17 (Fed. R. Civ. P. 28(a), 30(f)(1)).

18 I am not a relative or employee or attorney
19 counsel of any of the parties, nor am I a relative or
20 employee of such attorney or counsel, nor am I
21 financially interested in this action. (Fed. R. Civ.
22 28).

23 I am the deposition officer that
24 stenographically recorded the testimony in the
25 foregoing deposition and the foregoing transcript is

1 a true record of the testimony given by the witness.
2 (Fed. R. Civ. P. 30(f)(1)).

3 Before completion of the deposition, a review
4 of the transcript [] was [X] was not requested. If
5 requested, any changes made by the deponent (and
6 provided to the reporter) during the period allowed,
7 are appended hereto. (Fed. R. Civ. P. 30(e)).

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9 Dated: May 21, 2024.

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TAMMY L. LEE
Certified Shorthand Reporter No. 8716, RPR

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