

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
PETITIONER

v.

LONGITUDE LICENSING LTD.,
PATENT OWNER

IPR2023-01286

U.S. Patent No. RE43,539

PETITIONER'S REPLY

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PETITIONER'S EXHIBIT LIST

Updated: September 4, 2024

EX1001	U.S. Patent No. RE43,539 to Takahashi ("539 patent")
EX1002	Reissue Application File History of the '539 patent ("773 Reissue App")
EX1003	Declaration of Dr. Scott E. Thompson
EX1004	CV of Dr. Scott E. Thompson
EX1005	Prosecution File History of the Original Patent of '539 patent ("059 App")
EX1006	U.S. Patent No. 6,924,669 to Itoh et al. ("Itoh")
EX1007	U.S. Patent No. 3,943,551 to Skorup ("Skorup")
EX1008	U.S. Patent No. 4,975,598 to Borkar ("Borkar")
EX1009	U.S. Patent No. 3,356,858 to Wanlass ("Wanlass")
EX1010	U.S. Patent No. 6,288,563 to Muljono et al. ("Muljono")
EX1011	Order Granting Motion to Stay (Lenovo) (05-16-23)
EX1012	Order Granting Western Digital's Motion to Intervene (Amazon) (05-16-23)
EX1013	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
EX1014	U.S. Patent No. 5,194,765 to Dunlop et. al ("Dunlop")
EX1015	U.S. Patent No. 4,612,466 to Stewart ("Stewart")
EX1016	Dabral et al., Basic ESD and IO Design (1998) ("Dabral")
EX1017	Longitude Preliminary Infringement Contentions, Exhibit B - 539 Patent, CDCA-8:23-cv-00039-JWH-DFM
EX1018 (New)	Texas Instruments, Technical Reference Manual - Power MOSFET Gate Driver Bias Optimization, April 2020
EX1019 (New)	U.S. Patent No. 6,198,307 to Garlepp et. al ("Garlepp")

EX1020 (New)	Bruce Jacob deposition transcript, August 20, 2024 ("Jacob Deposition")
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I. Introduction

Longitude (“Patent Owner” or “PO”) has disclaimed all challenged claims other than Claim 4 of the ’539 Patent. In its Patent Owner’s Response (“POR”), PO cannot dispute that the claim limitations of Claim 4 are rendered obvious by the prior art. So, to avoid a clear finding of unpatentability, PO attempts to argue that the preamble of Claim 1 (which has been disclaimed by PO), from which Claim 4 depends, is limiting and not disclosed by prior art. PO’s arguments fail because they are contrary to the claims, specification, and prosecution history of the ’539 Patent, contrary to a POSITA’s knowledge, and contrary to the law. Furthermore, even if the preamble of Claim 1 were limiting, Claim 4 is rendered obvious under each of Petitioner’s Grounds 2 and 3 as presented in the Petition, because each of Petitioner’s Grounds 2 and 3 discloses the preamble. Accordingly, the Board should disregard PO’s arguments and find Claim 4, the single remaining challenged claim, unpatentable.

II. Claim Construction

A. “a smaller device size with a smaller gate width” (Claim 4)

In its decision granting institution, the Board construed “smaller device size” and “smaller gate width” to be synonymous rather than two separate requirements. Institution Decision, Paper 9, 11-13. PO did not dispute this construction nor did it make any related arguments in its POR.

B. Preamble phrase “at a predetermined output impedance” of Claim 1 is not limiting.

When a preamble “recites essential structure or steps, or if it is ‘necessary to give life, meaning, and vitality’ to the claim,” the preamble limits the claim.

TomTom, Inc. v. Adolph, 790 F.3d 1315, 1323 (Fed. Cir. 2015) (internal citation omitted). “Conversely, a preamble is not limiting ‘where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.’” *Id.* (citations omitted). The “facts of each case in light of the claim as a whole and the invention described in the patent” govern this claim construction issue. *Id.* (citing *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 952 (Fed. Cir. 2006) (quoting *Storage Tech. Corp. v. Cisco Sys., Inc.*, 329 F.3d 823, 831 (Fed. Cir. 2003))).

The preamble of Claim 1 recites, “An output buffer circuit for outputting data in the form of an input pulse train ***at a predetermined output impedance*** and slew rate.” The only phrase necessary to resolve the disputes here is “at a predetermined output impedance,” because the only remaining dispute is whether the prior art discloses this phrase if it is limiting. *See generally* POR, 1 (PO stating that Claim 4 is the only remaining challenged claim, and arguing that Petition’s prior art combinations do not disclose “a predetermined output impedance.”), 16-20 (PO asserting that “a POSITA would understand that the preamble of claim 1

could *only* be satisfied by a pulse train being output *at a single predetermined output impedance*").

Contrary to PO's arguments, the claims, specification, and prosecution history of the '539 Patent demonstrate that the preamble phrase "at a predetermined output impedance" is not a limitation of Claims 1 and 4. Claim 4 is invalid for that reason alone.

The positions of Petitioner and PO are summarized below. It is noted that while the discussion below focuses on the disputed phrase "at a predetermined output impedance," the entire preamble of Claim 1 including other phrases are not limiting for the same reasons.

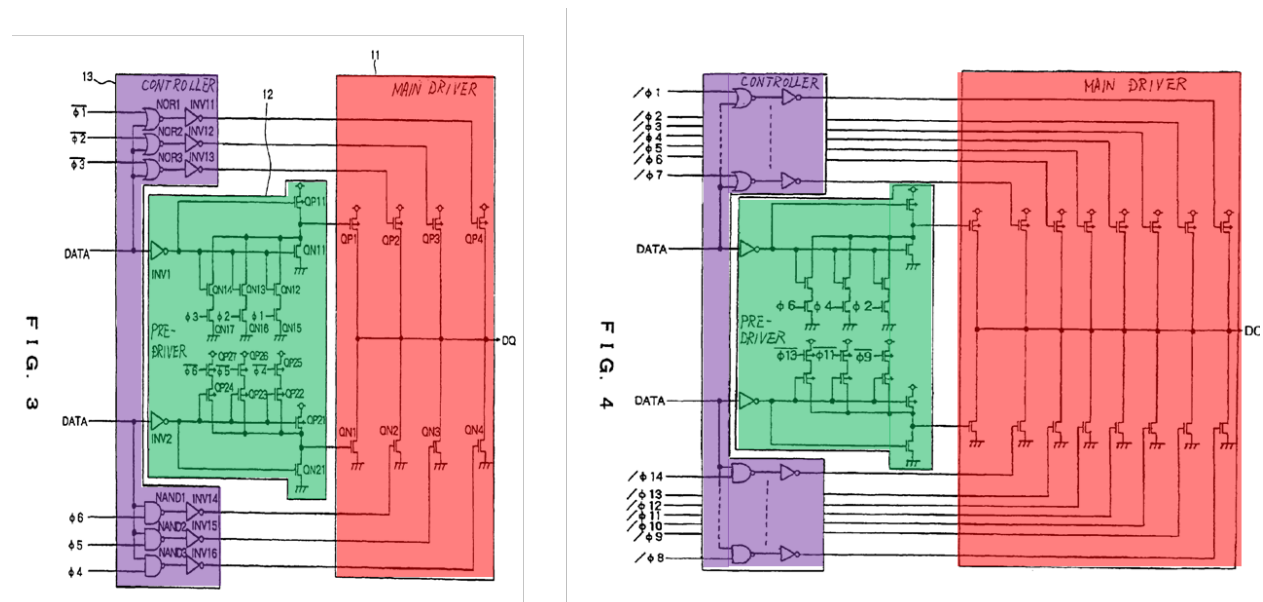
Preamble Phrase	Petitioner's Position	PO's Position
"at a predetermined output impedance"	Not limiting.	Limiting.

a. The disputed preamble phrase is not limiting, because the claim body describes a structurally complete invention and this phrase is only used as a purpose or intended use.

The preamble, including the disputed phrase "at a predetermined output impedance," is not limiting, because the claim body describes a structurally complete invention, and the preamble refers to "at a predetermined output impedance" only as a purpose or intended use. *See TomTom*, 790 F.3d at 1324 ("A preamble is not regarded as limiting...when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the

structure or steps of the claimed invention.”). Like *TomTom*, here the claim body describes a structurally complete invention, and deletion of the disputed preamble phrase does not affect the structure or steps of the claimed invention.

As detailed below, Claims 1 and 4 of the '539 Patent defines a structurally complete invention in the their detailed claim body (reciting a main driver, a predriver, a controller, and their relationships), and use the preamble only to state a purpose or intended use. As shown in annotated FIGS. 3 and 4 of the '539 Patent, the claim body defines a structurally complete invention, as supported by the '539 Patent.



'539 Patent, FIGS. 3 and 4 (annotated)

As an example, FIGS. 3 and 4 of the '539 Patent each illustrate an embodiment of the alleged invention including a main driver (annotated in red), a predriver (annotated in green), and a controller (annotated in purple), and the

complete structure of the alleged invention illustrated therein are defined by the claim body of Claim 1. *See also* '539 Patent, 4:35-38 ("FIG. 3 is a circuit diagram of an output buffer circuit according to a first embodiment of the present invention; FIG. 4 is a circuit diagram of a modification of the output buffer circuit according to the first embodiment"); POR, 14 (PO admitting that "***each embodiment*** of the '539 Patent is consistent with the goal of providing data in the form of a pulse train at a predetermined slew rate and output impedance"). The ***intended use*** of the claimed output buffer circuit with a main driver, a predriver, and a controller is to output data, and to do so at a predetermined impedance and slew rate.

The fact that the preamble language is unnecessary to the life, meaning, and vitality of claim is supported by the '539 Patent and the prosecution history. The specification of the '539 Patent does not mention or describe how to achieve "a pulse train being output at a ***single*** predetermined output impedance" as asserted by PO (POR, 20), much less describing it as necessary to the life, meaning, and vitality of the claim, in addition to the structurally complete invention recited in the claim body of Claim 1. Also, and as a reminder, the claims do not recite a "***single***" predetermined output impedance.

Similarly, during prosecution, PO did not rely on the preamble to distinguish its invention over the prior art. *See* EX1005, '059 App, 23-44 (after multiple anticipation rejections, the amendment "a predriver with outputs for driving only

said first n-channel MOS transistor and only said first p-channel MOS transistor” resulted in allowance). Indeed, PO could not rely on the preamble to distinguish its invention over prior art, because “it was basic knowledge to design output buffers with output impedance and slew rate control well before the ‘539 and found in textbooks.” EX1003, Thompson Decl., ¶¶32-37 (explaining that “two important inherent properties of an output buffer are output impedance (opposition to current flow) and slew rate (rate of change of the output voltage with time)”)(citing EX1016, Dabral, 122); EX1010, Muljono, 2:23-27 (it was well-known in the art to provide output buffers “that operate with an approximately uniform output impedance and slew rate”); EX1020, Jacob Tr., 47:1-53:14 (PO’s expert Dr. Jacob describing that for output buffer design in memory applications, typically the well-known JEDEC standards provide specific design parameters including slew rate and output impedance).

Also, PO does not specify any claim limitation that would be affected by the preamble phrase “a predetermined output impedance,” nor does PO specify any “structure or steps of the claimed invention” would be affected by the deletion of this preamble phrase. *TomTom*, 790 F.3d at 1325. This further emphasizes that this preamble phrase is not a limitation to the claims.

In short, the preamble here merely describes what the claimed output buffer circuit is being used for: “outputting data in the form of an input pulse train at a

predetermined output impedance and slew rate.” It also arguably extols benefits of the claims, but adds nothing to the highly detailed elements of the claims, and thus cannot be considered to give “life, meaning, and vitality” to it. *Catalina Marketing Intern. v. Coolsavings.com*, 289 F. 3d 801, 808-809 (Fed. Cir. 2002) (“preamble language merely extolling benefits or features of the claimed invention does not limit the claim scope without clear reliance on those benefits or features as patentably significant”).

b. PO's unjustified conversion of the preamble into a new *method* claim limitation on an *apparatus* claim should be rejected.

Claim 1 and its dependent Claim 4 are apparatus claims. Even PO itself states, “claims 1 and 4 are apparatus claims, and do not (and cannot) recite any method step of ‘outputting pulses’ from the main driver.” POR, 12. PO's attempt to effectively impose a new method claim limitation on apparatus Claims 1 and 4 should be rejected, because PO failed to provide any proper justification.

1. Preamble phrase “*for outputting data*” does not convert other preamble phrases into a new claim limitation.

PO states that the phrase “for outputting data” in the preamble provides antecedent basis for the very first limitation: ‘a main driver...for driving a load according to said data,’ and as such, “the preamble *must* be limiting.” POR, 11-12 (citing *In re Fought*, 941 F.3d 1175, 1178 (Fed. Cir. 2019)). PO's arguments should be rejected because they are contrary to the law.

As an initial matter, it is undisputed that the prior art discloses the preamble phrase “for outputting data,” and as such, it is not necessary to construe the preamble phrase “for outputting data.” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Furthermore, antecedent basis alone is not dispositive of whether a preamble phrase is limiting. *Catalina Mktg. Int’l*, 289 F.3d at 808 (“[D]ependence on a particular disputed preamble phrase for antecedent basis **may** limit claim scope because it indicates a reliance on both the preamble and claim body to define the claimed invention.”) (emphasis added); *Shoes by Firebug LLC v. Stride Rite Children's Grp.*, LLC, 962 F.3d 1362, 1368 (Fed. Cir. 2020) (“While antecedent basis **alone is not determinative** of whether a preamble is limiting, use of preamble terms to define positive limitations in the body of claims can evince an inventor’s intent that the preamble limit the scope of the claim.”). Here, the preamble phrase “for outputting data” (and similarly the claim term “for driving a load according to said data”) is simply a statement of intended use and does not add any structural limitation to the claims, because it does not place any constraints on the structural characteristics of the invention and does not define physical components for

achieving this intended use. That is, the claim is not directed to “data”, but is rather directed to a “circuit” that is intended to be used *for* outputting data. Accordingly, this phrase has no patentable weight and is not limiting.

Even if the preamble phrase “for outputting data” were limiting, it does *not* convert the entire preamble into a new claim limitation. *TomTom*, 790 F.3d at 1323-24 (finding that “the court erred in determining that it had to construe the entire preamble if it construed a portion of it”). PO’s assertion that the entire preamble “*must* be limiting” based on the undisputed phrase “for outputting data” is contrary to the law.

Like *TomTom*, here the phrase “at a predetermined output impedance” is an independent part of the preamble from “for outputting data,” and does not recite essential structure or steps or give necessary life, meaning, and vitality to the claim. As such, the phrase “at a predetermined output impedance” cannot be converted into a new claim limitation based on an antecedent basis rationale related to another phrase. *TomTom*, 790 F.3d 1315 at 1324 (“The [phrase at issue] does not recite essential structure or steps, or give necessary life, meaning, and vitality to the claim. It was therefore error for the district court to use an antecedent basis rationale to justify converting this independent part of the preamble into a new claim limitation.”); *see also Nearmap US, Inc. v. Eagle View Technologies, Inc.*, IPR2022-01090, Paper 31, 23 (PTAB Jan. 9, 2024) (in the Final Written

Decision, the Board found a preamble phrase not limiting, noting that

“[a]lthough...a different preamble phrase...provides the antecedent basis for later-used terms,...‘that does not necessarily convert the entire preamble [including the disputed preamble phrase] into a limitation.’”) (citing *TomTom*, 790 F.3d at 1323).

PO's reliance on *In re Fought* is misplaced. First, the Court did not hold that a preamble phrase “***must*** be limiting” ***only*** because it provides antecedent basis for a claim limitation. The Court determined whether a preamble phrase is limiting considering both (1) that the phrase provides antecedent basis; and (2) that the phrase “‘travel trailer’ is a specific type of recreational vehicle and that this term is a structural limitation of the claims.” *In re Fought*, 941 F.3d at 1178-79. Second, the Court provided its analysis for the disputed phrase “travel trailer,” and did ***not*** hold that an ***entire*** preamble “***must*** be limiting” only based on a preamble phrase. *Id.*

2. Preamble of Claim 1 is not necessary to understand the claim body of either of Claims 1 and 4, nor does it refer to the essence of the invention.

PO argues that the preamble phrase “an input pulse train” is necessary to understand the limitation of claim 4, because “without the preamble, there would also be no context for understanding Claim 4’s recitation of ‘pulses output from said main driver’ because there would be no indication of any pulses to be output from the overall output buffer circuit generally or the main driver more

specifically.” POR, 12. This is incorrect. Contrary to PO’s arguments, there is no dispute that the plain and ordinary meaning of “pulses output from said main driver” indicates pulses output from the main driver.

Notably, the body of dependent Claim 4 recites “pulses output from said main driver,” which introduces “pulses” as an element independently from “an input pulse train” recited in the preamble of Claim 1. The preamble of Claim 1 then, cannot be said to provide essential structure or necessary meaning to the claimed invention of Claim 4, because the element “pulses output from said main driver” is independently recited in the body of the claim.

Citing *Vizio, Inc. v. Int’l Trade Comm’n*, 605 F.3d 1330, 1341 (Fed. Cir. 2010), PO also argues that the preamble is limiting because it reflects a fundamental aspect of the invention. POR, 13. PO’s reliance on *Vizio* is inapposite. In *Vizio*, the Court found that the preamble reciting the decoding objective was limiting because the claims “would ‘have little meaning without the intended objective of decoding.’” 605 F.3d at 1341. Unlike *Vizio*, here the meaning of the claim limitations of Claims 1 and 4 is not affected by the disputed phrase “at a predetermined output impedance.” Instead, claim body of Claims 1 and 4 describes a structurally complete invention, and deletion of the preamble phrase does not affect the structure or steps of the claimed invention, and as such, the disputed preamble phrase “at a predetermined output impedance” is not limiting.

It is noted that after receiving the Petition showing invalidity of Claim 1 over grounds presented in the Petition, PO disclaimed Claim 1 in its entirety including its preamble. Now PO attempts to argue that Claim 4 is patentable because the prior art does not teach Claim 1.¹ Regardless, PO's reliance on the preamble of disclaimed Claim 1 contradicts the Office's permitted use of a statutory disclaimer "to streamline the proceedings." Consolidated Trial Practice Guide, 52. Indeed, Claim 1 has been disclaimed, and for a streamlined proceeding, we should be focusing on the remaining claim at issue, Claim 4, and not arguing the patentability of Claim 1.

III. Even if the Preamble Were Limiting, Claim 4 is Obvious.

As discussed above at Section II, the preamble is not limiting. Because no claim limitations are in dispute, Claim 4 is obvious for this reason alone.

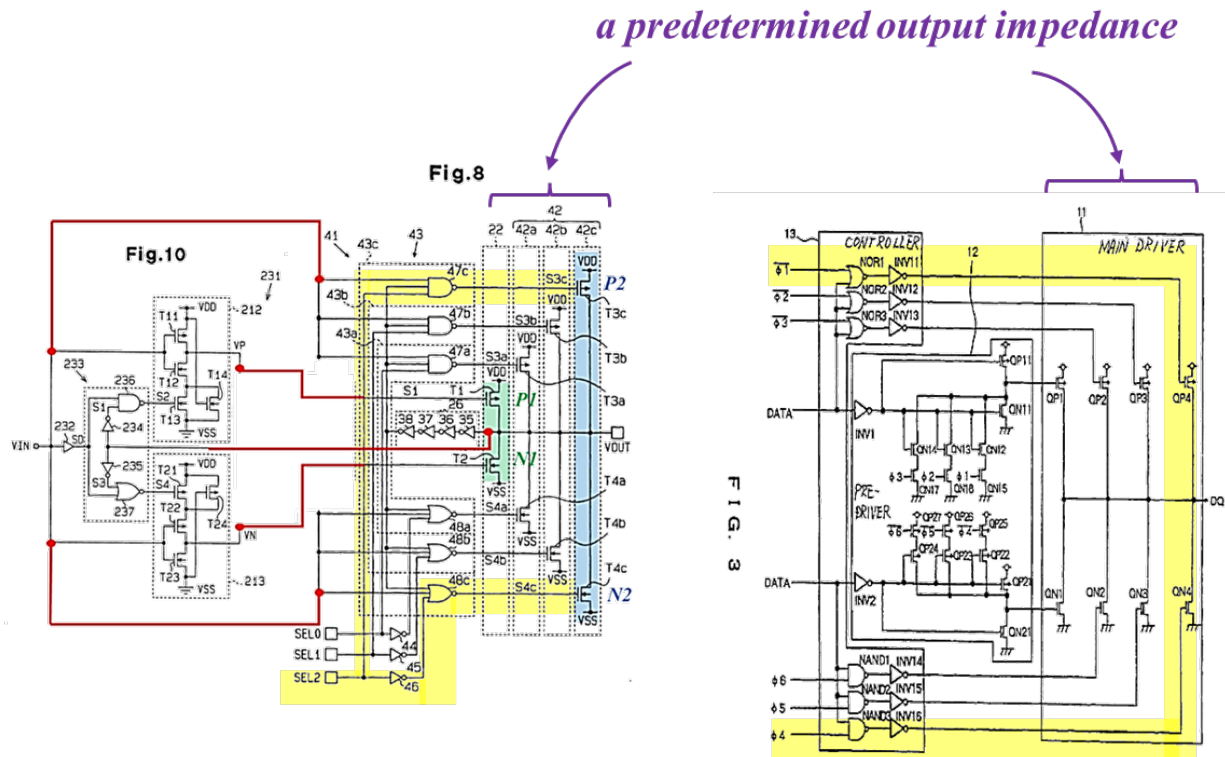
Furthermore, even if the preamble were limiting, Claim 4 is obvious under each of Grounds 2 and 3 presented in the Petition, because the prior art discloses all limitations and the preamble. The discussion below focuses on the preamble phrase "at a predetermined output impedance," because it is the only disputed phrase.

¹ It is unclear if PO is now trying to withdraw its disclaimer and argue Claim 1's patentability.

A. Ground 2: Itoh Combination renders Claim 4 obvious.

As explained in the Petition and as illustrated by the example of Combination of Itoh Embodiments 2 and 4, combination of embodiments of Itoh (“Itoh Combination”) renders Claim 4, including the preamble phrase “at a predetermined output impedance” of claim 1 to the extent that it is limiting, obvious.

As shown by the side-by-side illustration of Example 2.1 of the Itoh Combination and '539 Patent, FIG. 3 below, the Itoh Combination and the '539 Patent use the same technology (using a main driver, a predriver, and a controller to provide output impedance and slew rate control) to achieve the same goal of providing an improved output buffer with output impedance and slew rate control. Pet. 42-46.



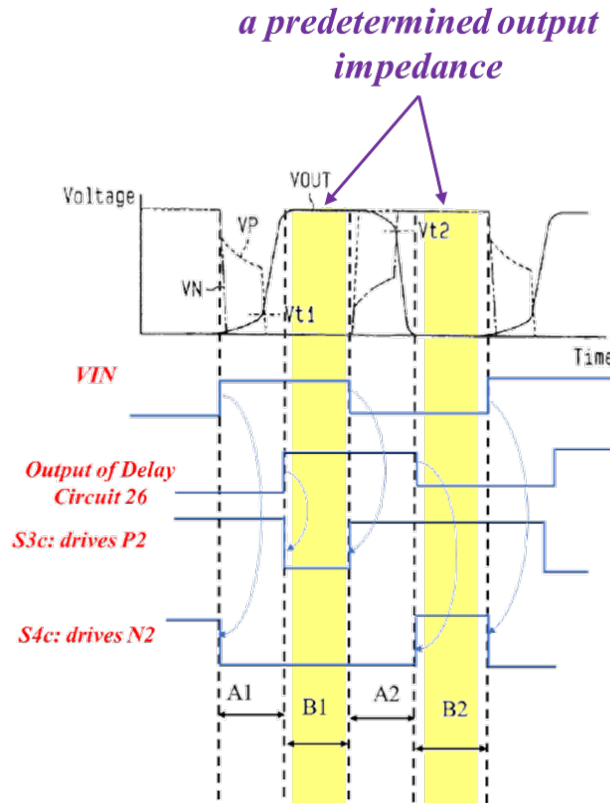
Example 2.1 of Itoh Combination vs. '539 Patent, FIG. 3

As highlighted in yellow and explained in the Petition, the Itoh Combination achieves improved impedance control to provide a predetermined output impedance “by using the additional pair(s) of output transistors for output impedance control.” Pet., 43; EX1006, 10:37-43 (“In accordance with the select signals SEL0 to SEL2, at least one of the sub-drive circuits 42a-42c is enabled to *select the output impedance when the output signal VOUT is in a static state.*”).

The Itoh Combination describes the same technique that the '539 Patent described for adjusting the output impedance of the output buffer, by controlling the pair of transistors in the main driver 11 as shown in FIG. 3 of the '539 Patent.

'539 Patent, 7:47-58 (“For adjusting the output impedance of the output buffer circuit shown in FIG.3, the level of control signals p1 through p3 is rendered low to turn on corresponding pMOS transistors QP2 through QP4 to ***lower the output impedance at the high level data is output.*** At this time, the greater the number of pMOS transistors that are turned on, the smaller the output impedance. Similarly, the level of control signals p4 through p6 is rendered high to turn on corresponding nMOS transistors QN2 through QN4 to ***lower the output impedance at the low-level data is output.*** At this time, the greater the number of nMOS transistors that are turned on, the smaller the output impedance.”).

In its POR, PO refers to the timing diagram of the Petition below and argues that the Itoh Combination provides “two different output impedance values.” POR, 17-18. However, PO does not dispute that when the output signal VOUT is driving data in a static state (periods B1 and B2 highlighted in yellow), the Itoh Combination discloses a single, predetermined output impedance with output impedance control. *See generally* POR, 17-18.



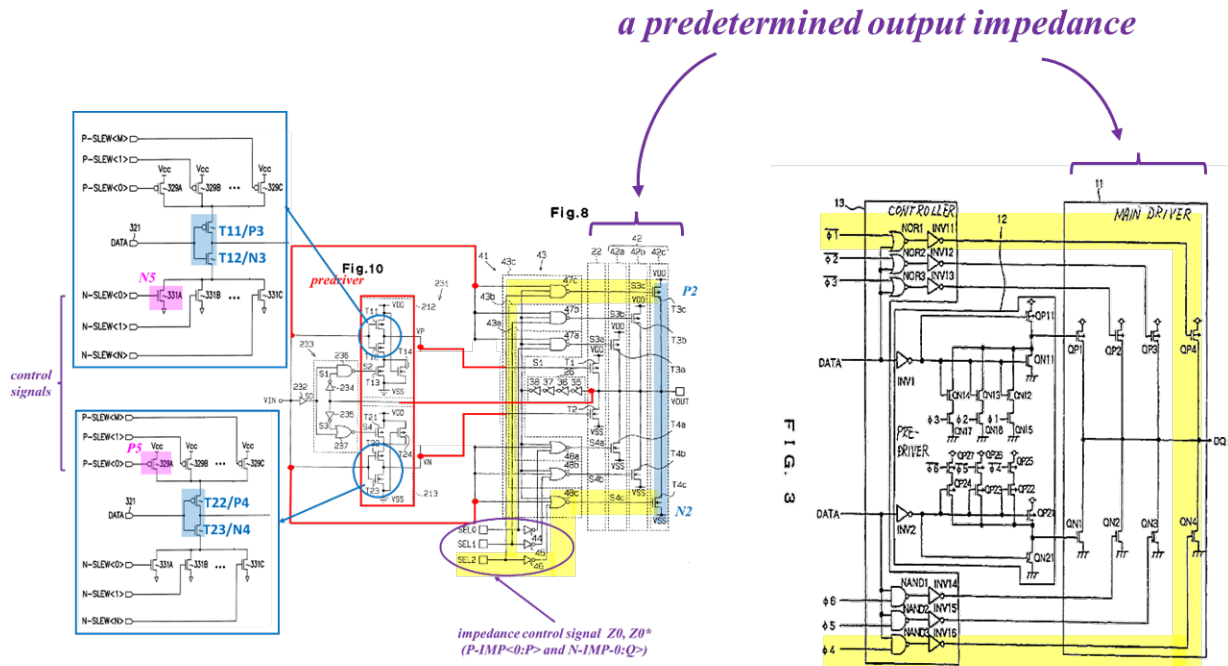
**Waveforms of Example 2.1
(Annotated using EX1006, FIG. 11)**

Indeed, by arguing the Itoh Combination discloses “two different output impedance values,” PO admits that the Itoh Combination discloses *at least one* predetermined output impedance value during the static state periods B1 and B2. POR, 19 (stating that the proposed combination of Itoh’s embodiments drives its pulse train “at two different output impedance values.”). Accordingly, the Itoh Combination discloses the preamble phrase “at a predetermined output impedance,” even if the preamble phrase were limiting.

B. Ground 3: Itoh in view of Muljono renders Claim 4 obvious.

As explained in the Petition and as illustrated by the example of Combination of Itoh and Muljono (Itoh-Muljono), Itoh-Muljono renders Claim 4, including the preamble phrase “at a predetermined output impedance” to the extent that it is limiting, obvious. This is because it is undisputed that Muljono, as applied in Itoh-Muljono, goes into significant detail about how to provide a uniform output impedance and the benefits thereof, as described in the Petition (Pet. 85-88; EX1003, Thompson Decl., ¶¶70-71, 278-283) and further discussed below.

As shown by the side-by-side illustration of Example 3.1 of Itoh-Muljono and '539 Patent, FIG. 3 below, Itoh-Muljono and the '539 Patent use the same technology (using a main driver, a predriver, and a controller to provide output impedance and slew rate control) to achieve the same goal of providing an improved output buffer with output impedance and slew rate control. Pet. 85-88.



Example 3.1 of Itoh-Muljono vs. '539 Patent, FIG. 3

As highlighted in yellow and explained in the Petition, Itoh-Muljono achieves improved impedance control to provide a predetermined output impedance, for at least the same reasons regarding Ground 2. Furthermore, the Petition explicitly explains that Itoh-Muljono discloses a predetermined output impedance, because “it would have been obvious for a POSITA to apply Muljono’s impedance control signals (e.g., EX1010, FIGS. 1, 2) to select signals SEL0-SEL2 of FIG. 8, for selecting the sub-driver circuits for output impedance control.” Pet. 84; *see also* Pet., 81 (“A POSITA would have been motivated to combine Muljono’s teaching of a compensation circuit in Itoh to achieve the obvious, beneficial, and predictable results of an output buffer circuit having ‘an

approximately uniform output impedance and slew rate independent of variations in process skew, supply voltage and temperature” as taught by Muljono.””) (citing EX1010, 2:23-27; EX1003, ¶¶270-275); *see also* EX1010, Muljono, Claim 1 (“An output buffer comprising: *a driver circuit having an impedance* that is controlled by an impedance control signal; and a pre-driver circuit to control *a slew rate of the driver circuit* according to a slew rate control signal that is generated *in response to the impedance control signal*.”), annotated FIG. 1 (Pet. 87).

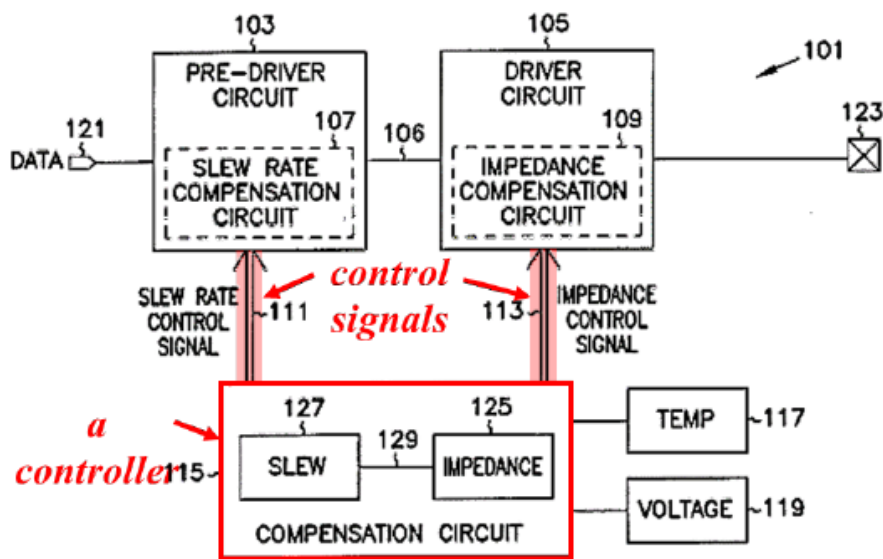


FIG. 1

EX1010, FIG. 1, annotated

In its POR, PO does not dispute any teachings of Muljono or their combination with Itoh. *See* POR, 20 (simply asserting that the Petition’s Ground 3 cannot succeed without any analysis of Muljono and its combination with Itoh).

Because it is undisputed that Itoh-Muljono provides “*an approximately uniform output impedance and slew rate* independent of variations in process skew, supply voltage and temperature” (Pet. 81), Itoh-Muljono discloses the preamble phrase “at a predetermined output impedance,” even if the preamble phrase were limiting.

C. PO’s unsupported requirement of “*only...a single* predetermined output impedance” should be rejected.

The gist of PO’s argument is that the prior art does not disclose the preamble phrase “at a predetermined output impedance,” because it requires “*only...a single* predetermined output impedance.” POR, 20 (“a POSITA would understand that the preamble of claim 1 could *only* be satisfied by a pulse train being output at a *single* predetermined output impedance.”).

As an initial matter, as discussed at II.B, the preamble of Claim 1 is not limiting, and as such, PO’s unsupported requirement of “*only...a single* predetermined output impedance” should be rejected for this reason alone. Furthermore, even if the preamble were limiting, PO’s arguments should be rejected because they are contrary to the law, contrary to the fundamental knowledge in circuit design, and contrary to the operation of embodiments of the ’539 Patent.

a. PO's importation of "*only...a single* predetermined output impedance" into "*a* predetermined output impedance" is contrary to the law.

PO attempts to create, from the preamble "*a* predetermined output impedance," a new claim limitation "*only...a single* predetermined output impedance." *See* POR, 20. PO's attempt should be rejected, because it is contrary to the law.

The Federal Circuit has repeatedly emphasized that an indefinite article "a" or "an" in patent parlance carries the meaning of "one or more" in open-ended claims containing the transitional phrase "comprising." *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1355 (Fed. Cir. 2000). The court has called this the "general rule," adding that an exception "only arises where the language of the claims themselves, the specification, or the prosecution history necessitate a departure from the rule." *ABS Global, Inc. v. Cytonome/St, LLC*, 84 F. 4th 1034, 1040 (Fed. Cir. 2023).

None of the language of the claims themselves, the specification, or the prosecution history necessitate a departure from the rule. The '539 Patent does not require *only a single* output impedance. To the contrary, the '539 Patent recognizes that systems have an "*allowable range of variations*," which includes an allowable range of variations of the output impedance. '539 Patent, 1:67-2:1 (describing a goal to achieve "a compensation within the *allowable range of*

variations of the system,” where “the slew rate depend[s] on *variations of both the output impedance* and the power supply voltage”).²

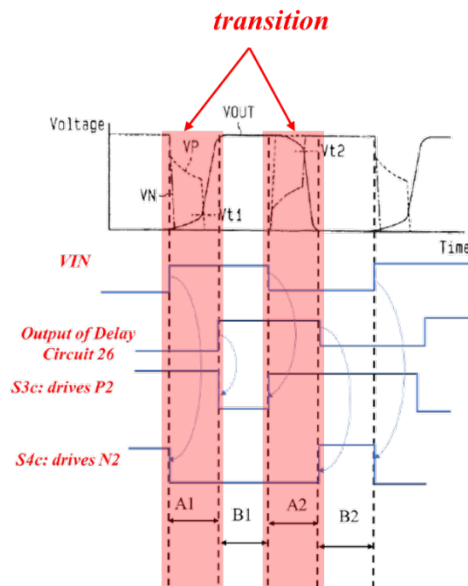
As such, contrary to PO's assertion that providing *only a single* predetermined output impedance is a fundamental aspect of the invention, the asserted fundamental aspect of the invention as described in the '539 Patent is to achieve output buffers with output impedance and slew rate within an “*allowable range of variations*.”

Accordingly, the preamble of Claim 1 does not recite a *single* predetermined output impedance, and instead only recite that there be a predetermined output impedance, which is unquestioned that each of Petition's Grounds 2 and 3 has when it is driving data at a high level or at a low level.

² PO's “only...a single” requirement is also contrary to '539 Patent's description of slew rate having a range of variations, as the preamble recites “*a* predetermined output impedance and *slew rate*.” See, e.g., '539 Patent, 9:6-9:9, FIG. 6 (illustrating the asserted goal for reducing “*the range of variations* of the slew rate,” instead of keeping the slew rate at only a single value).

b. PO's unsupported requirement of “only...a single output impedance” is contrary to well-known knowledge in the art and the operation of embodiments of the '539 Patent.

In its POR, referring to the Petition's timing diagram below, PO argues the preamble phrase “a predetermined output impedance” requires only a single output impedance for an output buffer throughout the entire pulse train, including the transition periods A1 and A2 when VOUT transitions between high and low. POR, 17-18. PO argues that the Itoh Combination does not disclose the preamble phrase because the output impedance changes between A1 (VOUT transitioning between 1 and 0) and B1 (VOUT at a static state). *Id.* (citing Dr. Thompson's testimony EX2006 at 16:8-20).



Waveforms of Example 2.1
(Annotated using EX1006, FIG. 11)

PO's arguments ignore the fundamental well-known knowledge that the main driver of output buffers includes pairs of MOSFETS for output impedance

control, and during the transition time, the resistance between the source and drain of a MOSFET (referred to as $R_{DS(on)}$) transitions between infinite and a relatively stable value. *See* EX1003, Thompspon Decl., ¶35 (“Generally, transistors with a large width or multiple transistors in parallel that are electrically fully ON provided low output impedance. Transistors that are turned OFF have high output impedance. Transistors turned on partially have output resistance between the on and off values.”); EX2005, Jacob Decl., ¶40 (“MOSFETs do not turn immediately on or off, and so there can be times when both of the driver MOSFETs are partially on, while one is turning on and the other is turning off.”); EX1020, Jacob Tr., 22:22-23:9; 25:19-26:6 (PO’s expert agreeing that the change of the resistance of a MOSFET related to the voltage of the gate “is not really very linear” in the cutoff regions and saturation regions).³

The figure below illustrates the typical $R_{DS(on)}$ vs V_{GS} (gate drive voltage) electrical characteristics curve.⁴

³ Jacob Tr. 26:3-4 includes a clerical error as corrected below: “Q. And in the cutoff regions and saturation regions, they become ~~new~~ non-linear; is that fair?”

⁴ The two curves of Figure 1 also illustrate that different curves corresponding to different temperatures, where resistance $R_{DS(on)}$ (impedance) increases when temperature increases.

*MOSFET channel resistance
 $R_{DS(on)}$ Changes during
Transition Period*

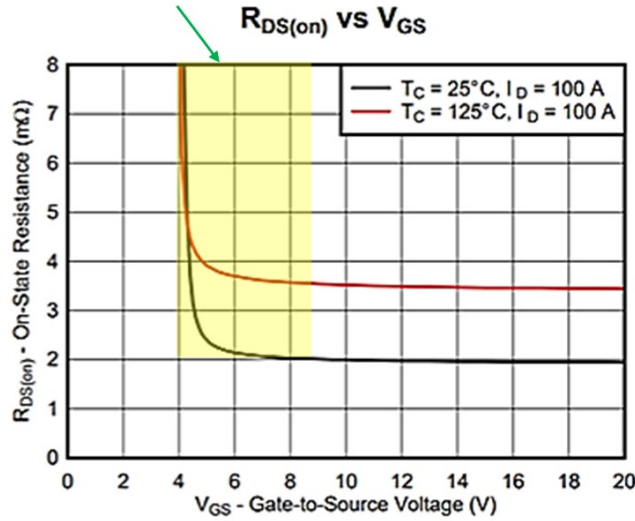


Figure 1. $R_{DS(on)}$ vs Gate Drive Voltage

EX1017, FIG. 1, annotated

Because $R_{DS(on)}$ the MOSFETS changes (nonlinearly) during transition, and because the output buffer's output impedance is affected by the $R_{DS(on)}$ of the MOSFETS in the output buffer, the output impedance of an output buffer changes during the transition. Such output impedance changes during transition are illustrated by the spikes of the output impedance $Z_{out(t)}$ during transition below:

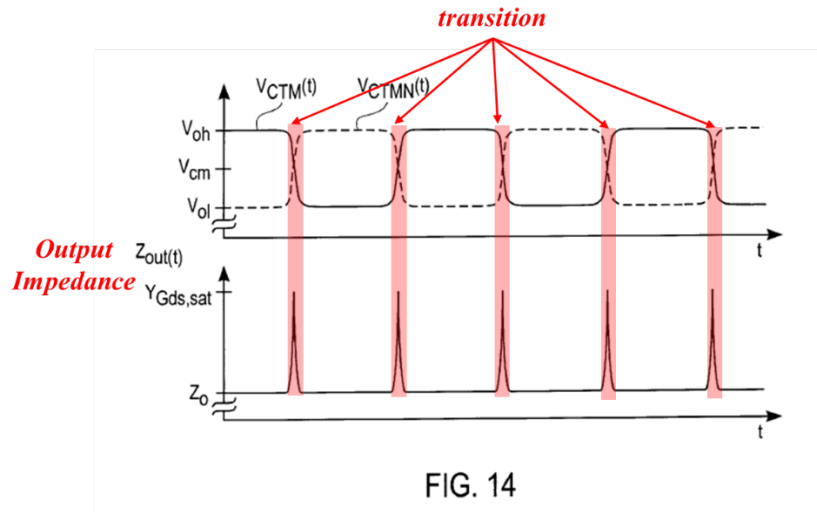


FIG. 14

EX1018, Garlepp, FIG. 14, annotated

While technologies for reducing the spikes in Z_{out} during the transition were well-known, they cannot completely remove the spikes, and some level of impedance variation during the transition periods persists because of the fundamentally inherent nonlinearity and operational characteristics of MOSFETs and other limitations in circuit design. See EX1018, Garlepp, FIG. 17; see also '539 Patent, 1:67-2:1 (describing “*allowable range of variations* of the system”) and discussion below. As such, PO's requirement of “only...a single output impedance” during the entire pulse including transition periods is contrary to the fundamental operational characteristics of MOSFETs and circuit design.

Indeed, PO's requirement of “only...a single output impedance” during the entire pulse including transition periods is contrary to the operation of embodiments of the '539 Patent, which is also subject to the fundamental non-linear operational characteristics of MOSFETs and circuit design. In the example

of FIG. 3 of '539 Patent, the nonlinear resistance transition also applies to QP1, QP2, QP3, QP4, QN1, QN2, QN3, QN4 of the main driver, which causes changes in output impedance of the output driver during transitions between high-level and low-level data.

Specially, the '539 Patent simply describes controlling the output impedance when the output data is *at* a high-level or a low-level at the static state,⁵ without description of controlling the output impedance *during* the transition period (when the data switching between low-level and high-level). '539 Patent, 7:47-58 ("For adjusting the output impedance of the output buffer circuit shown in FIG.3, the level of control signals p1 through p3 is rendered low to turn on corresponding pMOS transistors QP2 through QP4 to lower the output impedance *at the high level data* is output. At this time, the greater the number of pMOS transistors that are turned on, the smaller the output impedance. Similarly, the level of control signals p4 through p6 is rendered high to turn on corresponding nMOS transistors QN2 through QN4 to lower the output impedance *at the low-level data* is output. At this time, the greater the number of nMOS transistors that are turned on, the

⁵ This discussion of the '539 patent's "high level" and "low level" states corresponds to periods B1 and B2 of Itoh's Fig. 11 (*see* annotated Fig. 11 above, at p. 14).

smaller the output impedance.”). Indeed, the '539 Patent does not describe how it keeps the output impedance only at a single value during the transition between high-level and low-level, much less considering of the resistance changes of these transistors during transition.

Accordingly, PO's arguments should be rejected because they are contrary to the fundamental knowledge in circuit design, and contrary to the operation of embodiments of the '539 Patent.

IV. Conclusion

The Board should find all challenged claims unpatentable.

Respectfully submitted,

Dated: September 4, 2024

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V. Certificate of Word Count

Pursuant to 37 C.F.R. § 42.24, the undersigned attorney for the Petitioner declares that the argument section of this Petition (Sections I-IV) has a total of 5,176 words, according to the word count tool in Microsoft Word™.

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that a true and correct copy of the foregoing was served on the Patent Owner as detailed below:

Date of service September 4, 2024

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Documents served PETITIONER'S REPLY;
Petitioner's Updated Exhibit List; and
Exhibits 1001-1020

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