

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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WESTERN DIGITAL TECHNOLOGIES, INC.,  
Petitioner,

v.

LONGITUDE LICENSING LTD.,  
Patent Owner.

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Case IPR2023-01286  
U.S. Patent No. RE43,539

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**PATENT OWNER'S SUR-REPLY**

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## I. Introduction

Patent Owner's Response was supported by expert opinion explaining that claim 1's preamble—which recites in part “data in the form of an input pulse train at a predetermined output impedance and slew rate”) is limiting. *See* POR 10-16; Ex. 2005, ¶¶81-87. Despite Petitioner having the responsibility to “identify... [h]ow the challenged claim is to be construed” within the Petition itself,<sup>1</sup> the Petition did not identify any portion of the preamble as not being limiting.

Petitioner newly alleged in Reply that the preamble is *not* limiting. Petitioner presents several attorney arguments in this respect, including a surprising allegation that none of the preamble should be limiting even though it is undisputed that the preamble's recitation of “data” is necessary to provide antecedent basis support for “said data” in the body of the claims.<sup>2</sup> But these arguments are flawed for numerous reasons and are tellingly unsupported by *any* expert testimony. Accordingly, there is undisputed expert testimony that a POSITA would have viewed the preamble as limiting.

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<sup>1</sup> 37 C.F.R. §42.104(b)(3).

<sup>2</sup> *See* Reply 3 (“The preamble... is not limiting, because the claim body describe a structurally complete invention....”); Reply 7-8 (not disputing that the preamble is necessary to provide antecedent basis support for the body of the claim).

There is also no real dispute that the Petition's claim 4 theory does *not* satisfy the required "output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate." Indeed, Petitioner's expert admitted his combination is *not* designed to output data in the form of an input pulse train at a predetermined output impedance, because the design *intentionally* changes the output impedance along *every* output pulse transition (A1 and A2, under the Petition's claim 4 theory). See POR 18-19 (quoting Ex. 2006, 16:8-20, 27:13-18). Accordingly, as Patent Owner's expert explained, the Petition's theory is not designed to "drive its output pulse train 'at a predetermined output impedance' as claims 1 and 4 require, but would 'instead driv[e] *each bit* of its pulse train at *two different* output impedance values.'" Ex. 2005 ¶110 (emphasis in original) (quoted by POR 19).

Again, Petitioner provides only attorney argument in response, primarily alleging that systems such as those disclosed in the '539 patent will necessarily have *some* level of variation in output impedance such that the claims cannot require a completely and strictly unvarying output impedance. See Reply at 21-28 (discussing variation in output impedance); *id.* at 26 (alleging that "*some* level of impedance

variation during the transition periods persists”).<sup>3</sup> Patent Owner acknowledges that output impedances can undergo natural fluctuations in *any* physical system, but this does not undermine the claim’s limiting purpose of providing data in the form of an input pulse train at a predetermined impedance, in contrast to Petitioner’s claim 3 theory in which the system is *intentionally* designed to *modify* the output impedance across every pulse transition.

In sum, there is unrebutted expert testimony that the preamble is limiting and that the Petition’s sole claim 4 theory does not include the claimed “output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate.” Accordingly, challenged claim 4 should be found not unpatentable.

## **II. The entire preamble is limiting.**

The preamble of claim 1 recites, in its entirety, “[a]n output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate.” Ex. 1001, 12:54-56.

As explained in Patent Owner’s response and by Patent Owner’s expert Dr. Jacob, the preamble is limiting for several reasons. First, it provides the necessary

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<sup>3</sup> All emphases herein are added unless otherwise specified.

antecedent basis for “said data,” which occurs several times in the body of the claim. POR 11-12; Ex. 2005 ¶83. Second, if the preamble were *not* limiting, claim 4 would require “pulses output from said main driver”—in other words, it would require that the apparatus actually be *used* to output pulses, rather than be “*for* outputting data in the form of input pulses” with the specified characteristics as the preamble recites. POR 12-13 (explaining that apparatus claims cannot include method steps); Ex. 2005 ¶84 (“Without the preamble, Claim 4’s requirement of output needs further clarification.”). Third, the preamble provides a fundamental aspect of the invention—the capability of providing an input pulse train according to a predetermined output impedance and slew rate. *See* POR 13-15; Ex. 2005 ¶¶85-87.

Furthermore, contrary to Petitioner’s Reply arguments, the preamble *does* recite “essential structure” (Reply 9), because the “input pulse train at a predetermined output impedance and slew rate” is provides important structural definition for the form of the “data” that the system is configured to output. Each of these reasons is discussed in turn.

**A. There is no dispute that the preamble provides necessary antecedent basis for the body of the claims.**

The POR explained that the preamble provides the necessary antecedent basis for “said data,” which occurs three times within the body of claim 1. *See* POR 11-

12; Ex. 1001, 12:59, 13:2, 13:5 (instances of claim 1 reciting “said data” which can only refer back to the preamble); Ex. 2005, ¶83.

Petitioner cannot dispute this basic fact; accordingly, the preamble is limiting. *In re Fought*, 941 F.3d 1175, 1178 (Fed. Cir. 2019) (“We have repeatedly held a preamble limiting when it serves as antecedent basis for a term appearing in the body of a claim.”) (collecting cases); *see also C.W. Zumbiel Co. v. Kappos*, 702 F.3d 1371, 1385 (Fed. Cir. 2012) (“In *Catalina Marketing International, Inc. v. Coolsavings.com, Inc.*, we stated that ***the preamble constitutes a limitation when the claim(s) depend on it for antecedent basis....***”).

In the face of extensive Federal Circuit authority cited by *Fought* that a preamble is limiting when it provides antecedent basis, Petitioner asserts that the preamble should be found not limiting ***despite*** providing necessary antecedent basis to the body of the claim. Reply 3 (arguing that the entirety of the preamble is not limiting); Reply 8 (contending that “the preamble phrase ‘for outputting data’... is simply a statement of intended use” nonlimiting despite providing antecedent basis for claim terms in the body of the claim).

In support of this assertion, Petitioner’s Reply alleges that there might be at least ***some*** instances where reliance on a preamble for antecedent basis might not render it limiting. Reply at 8-9. But Petitioner cannot identify (and Patent Owner is

not aware of) **any** case holding a preamble non-limiting despite providing antecedent basis for terms in the body of the claim.

Indeed, even the seminal *Catalina Marketing* case on which Petitioner relies makes clear that a claim's reliance on the preamble for antecedent basis necessarily renders the preamble limiting. There, the Federal Circuit stated that "a preamble limits the invention... if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (quoting *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999)). And the *Pitney Bowes* case *Catalina Marketing* quoted makes clear that when the body of a claim derives necessary antecedent basis from a preamble, "the term ***can only be understood in the context of the preamble.***" *Pitney Bowes*, 182 F.3d at 1306.

Indeed, Petitioner *acknowledges* that ignoring the preamble would substantively alter the rest of the claim. Specifically, Petitioner alleges that the term "for driving a load according to said data" ***in the body*** of claim 1 "is simply a statement of intended use" and "has no patentable weight and is not limiting." Reply at 8-9. Petitioner thus concedes that without the preamble, at least three limitations in the body of claim 1 would be effectively excised from the claim. *See* Ex. 1001, 12:59, 13:2, 13:5 (instances of claim 1 reciting "said data"). Petitioner provides ***no***

**support** for ignoring these limitations in the body of the claims, presumably because there is none.<sup>4</sup>

Furthermore, the intended use of the claimed system has **already** been put at issue by Petitioner’s theory for claim 4, in which the prior art would be intended to be used such that “P2 and N2 are turned off (by control signals S3c and S4c), and as such, have small effect on rise and fall times of VOUT.” Pet. 61. Petitioner does not contend that the **structure** of transistors P2 and N2 would “have a small effect on rise and fall times of pulses output from said main driver” as claim 4 requires (Ex. 1001, 13:30-36); instead, Petitioner alleges that its proposed system would be *intended to be used* in a way that the “small effect” limitation would be satisfied. Pet. 61. Accordingly, if Petitioner’s allegation that only the specific *structure* of the system should be considered, and the manner in which it is configured or intended to operate should be ignored, then Petitioner’s claim 4 theory would fail for the sole

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<sup>4</sup> To the extent that Petitioner contends that any claim term that recites structure “for” accomplishing a certain result should be ignored, that is obviously contrary to law. *See* 35 U.S.C. §112 ¶6 (pre-AIA). And such a rule would have uncertain and wide-ranging implications for claim 1 of the ’539 patent, which uses “for” language on eight different occasions. Ex. 1001 12:58, 12:61, 12:64, 13:1, 13:4, 13:6, 13:9, 13:11.

reason that Petitioner has alleged a “small effect” on rise and fall times would occur *solely* because of the *intended use* the Petition’s combination.

In sum, because the preamble indisputably provides antecedent basis support for the body of the claims, it is limiting.

**B. The preamble also is essential to understanding the “small effect on pulses output from said main driver” limitation of claim 4.**

Petitioner further argues that even if some of the preamble is limiting, *only* the words “for outputting data” should be limiting, because “an input pulse train at a predetermined output impedance and slew rate” is allegedly not necessary to understand claim 4’s “small effect on rise and fall times of pulses output from said main driver” limitation.

However, as explained in the POR (and Petitioner does not dispute), “claims 1 and 4 are *apparatus* claims, and cannot recite any *method* step of ‘outputting pulses’ from the main driver.” POR 12; *see also* Reply 7 (acknowledging that claims 1 and 4 cannot recite a method step of outputting pulses). Accordingly, claim 4 cannot literally mean that there must be “pulses output from said main driver,” because requiring the outputting of pulses would improperly introduce a method step in an apparatus claim. POR 12.

Resolution of the interpretation of claim 4 can thus *only* be determined by reference to the preamble, which makes clear that the “output buffer circuit” must

be “*for* outputting data in the form of an input pulse train at a predetermined output impedance and slew rate.” Ex. 2005 ¶83-84. In other words, the “pulses output from said main driver” referenced in claim 4 are pulses of the “input pulse train at a predetermined output impedance and slew rate” that the output buffer circuit is designed to output (but need not *actually* output because the claim is an apparatus claim rather than a method claim). POR 12-13.

Indeed, Petitioner does not dispute that if the preamble were not limiting, claim 4 would require that the system be *used* to output pulses from the main driver. See Reply 10-11. This would improperly import a method step into an apparatus claim, which is particularly unnecessary when the preamble clarifies that “pulses” refers to pulses the system is *designed to* output. Cf. *IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005) (noting that a claim cannot be properly understood if it is “unclear whether infringement... occurs when one creates a system that allows” a method to be performed, “or whether infringement occurs when” the method step is actually performed).

Like in *IPXL*, under Petitioner’s proposed interpretation without respect to the preamble, it is not clear whether infringement would occur when the system is created, or when the system actually creates “pulses output from the main driver.” As explained by Patent Owner’s expert, this term “needs further clarification” that is provided by the preamble itself. Ex. 2005 ¶84.

Petitioner has no evidence that a POSITA would *not* need the preamble to properly understand this aspect of claim 4, and even Petitioner’s attorney argument does not describe how its interpretation of claim 4 *without* reference to the preamble would not improperly require pulses to *actually* be output from the driver.<sup>5</sup>

Because Petitioner does not provide any plausible, coherent meaning for the “pulses output from the main driver” *without* reference to the preamble, that further confirms the limiting nature of the preamble.

**C. The preamble as a whole provides a fundamental aspect of the invention—providing data in the form of an input pulse train at a predetermined output impedance and slew rate.**

As explained in Patent Owner’s Response, the ’539 patent teaches the importance of outputting an input pulse train at a predetermined output impedance and slew rate. POR at 13-15. And as explained by Patent Owner’s expert, a POSITA would have understood from the teachings of the ’539 patent that impedance characteristics and slew rate characteristics would be controlled on far longer timescales than on a pulse-by-pulse basis. Ex. 2005 ¶105 (opining that “the

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<sup>5</sup> Notably, Petitioner did not allege that “pulses output from the main driver” was indefinite during claim construction at the district court, thus acknowledging that claim 4 does *not* require pulses to actually be output from the main driver.

configuration of the output impedance of [the '539 patent's] output buffer was intended to be performed either once at system start-up, or periodically on timescales... many millions of times longer than an output pulse"). In other words, the system is designed to provide at least one train of multiple input pulses (i.e., an "input pulse train"), wherein that input pulse train is provided at a predetermined impedance and slew rate. A POSITA would have recognized that this is an important aspect for performance of the claimed output buffer circuit, because of the concept of "impedance matching":

Matching the impedances of output drivers, transmission lines, and input receivers is important because impedance is a significant factor of signal integrity. Mismatched impedance levels cause signal reflections at every boundary, much like one can see waves cresting in the ocean wherever there are abrupt changes in the water depth. Elimination of these reflections makes the resulting signal smoother and easier to read correctly, which enables faster communications.

Ex. 2005 ¶54. Of course, if an impedance needs to be matched to a particular value (which is typically the case in output buffer circuits), significant variations in output impedance within a train of pulses would lead to "[m]ismatched impedance levels," thus decreasing the integrity of the resulting pulse train. *See id.*

Accordingly, Dr. Jacob opined that it would “have been clear to a person of ordinary skill that the output impedance of [the ’539 patent’s] output buffer would have remained the same over a given pulse train.” Ex. 2005 ¶78.

In Reply, Petitioner does not seriously dispute that the output buffer circuit of the ’539 patent is an “output buffer circuit *for* outputting data in the form of an input pulse train at a predetermined output impedance and slew rate.” Indeed, Petitioner acknowledges that the “intended use” of the disclosed invention “is to output data, and to do so at a predetermined impedance and slew rate.” Reply 4-5.

Petitioner’s criticism is instead that in physical operation of the ’539 patent’s output buffer circuit, there may be slight “variations” in output impedance or slew rate. Pet. 21-22 (discussing an “allowable range of variations” that may occur).

That there may be undesired variations in output impedance and slew rate, however, is precisely the reason for the invention of the ’539 patent: the goal of the invention is to “*suppress* variations in the driving capability [i.e., output impedance] and slew rate of the output buffer circuit... in view of fluctuations in the power supply voltage and the ambient temperature.” Ex. 1001, 1:30-35. In other words, the purpose of the inventive system is to maintain the output impedance and slew rate according to predetermined values by *suppressing undesired* variations.

Notably, the ’539 patent’s invention is in stark contrast to the proposal set forth by the Petition, in which output impedance is *intentionally* varied on every

pulse transition, such that the Petition's combination would *not* be designed to provide an "input pulse train" (i.e., a train of a plurality of pulses) that maintains a constant output impedance.

The fact that the inventor regarded this aspect of the '539 patent to be part of the ***invention*** (and not *merely* as an intended purpose as Petitioner contends) is further shown by other claims of the patent, in which the exact phrase at issue ("for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate") is recited ***outside*** of the preamble. *See* Ex. 1001, 15:1-42 (claim 13), 15:46-16:44 (claim 15).

It would be particularly odd for these exact same phrases in claim 1 and claims 13 and 15 to have different meanings, given the "strong" presumption that "the same phrase in different claims of the same patent should have the same meaning," which can be "overcome only if 'it is clear' that the same phrase has different meanings in different claims." *See In re Varma*, 816 F.3d 1352, 1363 (Fed. Cir. 2016) (quoting *Fin Control Sys. Pty, Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001)). Here, given the evidence (including unrebutted expert testimony) that the preamble as a whole is important to understanding the claims at issue, it is anything but "clear" that the preamble of claim 1 should be interpreted differently than the non-preamble language of claims 13 and 15. *See id.*

**D. Contrary to Petitioner’s allegation, the preamble provides structural detail regarding the “data” the system is designed to output.**

Petitioner argues extensively that “deletion of the disputed preamble phrase does not affect the structure or steps of the claimed invention.” Reply at 3-4. This is incorrect; as noted above in Section II.A, there *should* be no real dispute that at least “for outputting data” is limiting, as it provides antecedent basis for several claim limitations and there is no authority for finding a preamble non-limiting under such circumstances. Accordingly, the claimed system must be “for outputting data.”

Additionally, “data” standing alone is not structurally well-defined. This is important because the body of claim 1 refers back to “said data” several times, so a POSITA would want to know the structural nature of the “data” being referenced. Ex. 2005, ¶83. The entirety of the preamble answers this question—the data to be output is in the structural “form of an input pulse train at a predetermined output impedance and slew rate.” Ex. 1001, 12:54-56. This provides structural guidelines regarding the data the system is designed to output, which a POSITA would be able to visualize and understand the actual structural characteristics of (as opposed to just “data” in the abstract, which can take any number of forms). See Ex. 2005, ¶83 (“The preamble is the only place that provides the structural details of how the data is intended to be “output”: “in the form of an input pulse train at a predetermined output

impedance and slew rate.” Accordingly, the entire preamble phrase is important to understanding the structure of the data that the system is designed to output.

### **III. The Petition’s Ground 2, claim 4 theory fails.**

#### **A. Unlike claim 4, the Petition’s combination is specifically designed to vary output impedance.**

As noted above, the apparatus of claim 1 (and thus claim 4) of the ’539 patent is designed to output data in the form of an input pulse train at a predetermined output impedance. As explained, e.g., in Section II.C above, this does not require that, in operational practice, the output impedance remains *entirely* constant; it simply requires that the system be designed to output data in the form of an input pulse train at a predetermined output impedance. Instead, the claim requirement can be satisfied, for example, by a system that is designed to suppress variations in a predetermined output impedance throughout the entirety of a given input pulse train. *See* Ex. 1001, 1:30-35 (“It is important for systems operating at higher speeds and under low voltages to suppress variations in the driving capability and slew rate of the output buffer circuit... in view of fluctuations in the power supply voltage and the ambient temperature and different device performance capabilities.”).

Unlike the ’539 patent’s teaching of *suppressing* variations in a predetermined output impedance, Petitioner’s claim 4 theory involves *intentionally changing* the output impedance along *every* pulse transition such that particular

transistors would have effectively no impact on rise and fall times of the pulses that are output from the main driver. *See* Pet. 60-62; POR 18-19 (quoting Ex. 2006, 16:8-20 and 27:13-18, where Petitioner’s expert acknowledged his claim 4 theory modifies the output impedance during transitional periods by disabling both the P2 and N2 transistors). As explained further in Section III.C below, such an interpretation of the claim scope is contrary to the plain meaning of the claim language to a POSITA.

In summary, the Petition’s claim 4 theory fails because the intended use of the Petition’s prior art combination (in order to arrive at the “small effect” requirement of claim 4) is to significantly vary the output impedance along every input pulse transition, such that the preamble to claim 1 is not satisfied. *See* Ex. 2005 ¶¶105-111.

**B. Petitioner’s reliance on structural similarities between the proposed combination and the ’539 patent are irrelevant to the claim 4 analysis.**

Unlike the Petition’s claim 4 theory, which is intended to vary output impedance over a given input pulse, Patent Owner presented undisputed expert testimony that the ’539 patent embodiments “adjust output impedance only once per recalibration (e.g., once at system startup) and does so to set the drive strength of the output buffer” such that the ’539 patent’s circuit buffer is “for outputting data in the

form of an input pulse train at a predetermined output impedance.” Ex. 2005 ¶ 103; *id.* ¶¶81-87 (explaining how the specification teaches this claim requirement).

Petitioner does not dispute that the embodiments of the ’539 Patent do *not* intentionally vary the predetermined output impedance along every pulse transition. Indeed, Petitioner does not dispute that the ’539 patent’s embodiments *are* intended to “keep the output impedance only at a single value during the transition,” but alleges only that the ’539 patent “does not describe *how*” it does so. Reply 28.<sup>6</sup> And Petitioner does not dispute that this is a significant difference from the way in which Petitioner’s claim 4 combination is designed to operate.

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<sup>6</sup> Petitioner’s allegation ignores Dr. Jacob’s testimony that the “predetermined output impedance” requirement is satisfied by the ’539 Patent’s simultaneous control of both slew rate and output impedance using the same control signals (a feature Petitioner does not allege to be present in the Ground 2 or Ground 3 combinations). *See* Ex. 2005 ¶¶85-87. Petitioner also recognizes that “technologies for reducing the [impedance variation] during the transition were well-known.” Reply 26; *see also* Ex. 2005 ¶¶37-59 (discussing various means for reducing impedance variations while also avoiding “highly problematic” “short-circuit currents”).

Accordingly, it is undisputed that there are significant differences between how the '539 patent's embodiments are designed to operate, and how the Petition's claim 4 combination is alleged to have been designed to operate.<sup>7</sup>

Glossing over these differences in intended usage of these two systems, Petitioner points to structural similarities in the physical transistor arrangement between its Itoh combination and FIG. 3 of the '539 Patent. *See, e.g.*, Reply 13-14 (providing a side-by-side comparison of two figures); *id.* 17-19 (same). But this ignores the fact that for the Petition's claim 4 theory, Petitioner *relies on* the intended use of the Itoh combination (i.e., to disable P2 and N2 during time periods "A1 and A2 where the slew rate is controlled," such that they would "have [a] small effect on rise and fall times of VOUT"). Pet. 61-62.

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<sup>7</sup> Petitioner provides a cursory citation to teachings of the '539 patent that pMOS transistors "lower the output impedance [when] the high level data is output," and that nMOS transistors "lower the output impedance [when] the high level data is output." Reply 14-15 (quoting Ex. 1001, 7:47-58). Notably, however, the Petition does *not* allege that the design of the system would intentionally change the output impedance during pulse transitions, and does not dispute that the '539 teaches suppressing variations in output impedance. *See* Ex. 1001, 1:30-35 (recognizing that "[i]t is important... to suppress variations in the driving capability and slew rate of the output buffer circuit").

This intended usage of the system was necessary for Petitioner's expert Dr. Thompson to agree to testify that the "small effect" limitation was satisfied. *See* Ex. 2006, 17:20-19:12 (Dr. Thompson testifying that could not identify the bounds of "small effect," but that the limitation was nevertheless satisfied because "[d]uring the rise and fall, P2 and N2 are [off in] Itoh," such that they have "a negligible, zero, miniscule effect").

And fatal to the Petition's theory, Dr. Thompson acknowledged that when P2 and N2 are turned off in Itoh (as is necessary for his claim 4 theory), "[d]river 42c" has "no effect" on output impedance "during A1 and A2," in contrast to B1 and B2 in which "[d]river 42c alters the impedance." Ex. 2006 27:13-18; *id.* 16:8-20 (explaining that the "impedance is changing" between time periods A1 and B1 because the P2 and N2 transistors are both turned off during A1, but not during B1).

Thus, because the Petition relies in the *intended use / configuration* of the proposed combination to arrive at the "small effect" limitation, Petitioner cannot ignore differences between how the claimed invention and the proposed prior art combination are intended to be operated.

In short, Petitioner cannot have it both ways. Either the claim requires that the system be designed to output data in the form of an input pulse train at a predetermined output impedance (and Petitioner cannot show the preamble to be satisfied under its claim 4 theory), or the actual intended use of the system is

irrelevant to claim scope (and Petitioner cannot show the additional limitations of claim 4 to be satisfied).

**C. The claims do require a system designed to output data in the form of an input pulse train at a (single) predetermined output impedance.**

Petitioner argues in Reply that an input pulse train can be provided “at a predetermined output impedance” by *any number* of output impedances, so long as there is “*at least one* predetermined output impedance.” See Reply 16. This is contrary to the plain meaning of “outputting data in the form of an input pulse train at a predetermined output impedance,” which as Patent Owner’s expert explained, means that the output impedance was *not* “intended to be reconfigured in the middle of an output pulse train.” Ex. 2005 ¶105.

Petitioner provides no rebuttal expert testimony, and instead provides only conclusory attorney argument that this expert opinion is incorrect.

Under Petitioner’s theory, under which there only need be “at least one” predetermined output impedance for a given input pulse train, the system could be designed to, for example, provide twenty pulses within a twenty-pulse train, *each pulse* at a different intended impedance. Petitioner’s interpretation would mean that if *at least one* of those output impedances is “predetermined,” intentionally providing the pulse train at twenty *different* output impedances would constitute a

system designed to “output data in the form of an input pulse train at a predetermined output impedance.” That is contrary to common sense, and also contrary to the un rebutted expert testimony of Dr. Jacob. Ex. 2005 ¶105 (opining that reconfiguring impedance on the timeframe of a single pulse does not meet the claim requirement).

Notably, the requirement that the system be designed to provide “data in the form of an input pulse train at a predetermined output impedance” is not a particularly difficult requirement to satisfy. A “pulse train” is simply a train of multiple pulses, so a system designed to output (for example) data in the form of three consecutive pulses at a predetermined output impedance could satisfy the claim requirement, even if a different predetermined output impedance were used for a subsequent pulse train. But under Petitioner’s claim 4 theory, the output impedance is intentionally varied along *every* pulse transition, such that there is not even *one* complete pulse (much less a complete “pulse train”) intended to be provided at “a predetermined output impedance.”

Accordingly, the claim should be interpreted such that the output buffer circuit must be “for outputting data in the form of an input pulse train at a predetermined output impedance,” which requires a design intended to output at least one full “pulse train” at a given output impedance (rather than intentionally varying the output impedance of the pulse train before as the Petition’s claim 4 theory requires).

**IV. The Petition’s Ground 3 theory for claim 4 suffers exactly the same deficiencies.**

The Petition’s Ground 3 theory for both the preamble of claim 1 *and* for the entirety of claim 4 is *exactly* the same as the Petition’s Ground 2 theory. *See* Pet. 82, 91. The *entirety* of the Petition’s Ground 3 analysis of these limitations is reproduced below in the below images.

[1.0]-[1.2.2]

Itoh teaches this element for the reasons discussed at Ground 2:[1.0]-[1.2.2].

EX1003, ¶276.

Pet. 82.

**5. Claim 4**

Itoh teaches this element for the reasons discussed at Ground 2:[4.0].

EX1003, ¶290.

Pet. 91.

Petitioner in Reply contends that “PO does not dispute any teachings of Muljono or their combination with Itoh” with respect to Ground 3. Reply 19. But Patent Owner *did* dispute Petitioner’s theory with respect to Ground 3 as to the preamble and claim 4, because that theory is *identical* to the Petition’s Ground 2 theory in relevant respect.

Tellingly, even in Reply Petitioner does not dispute that in Petitioner’s Ground 3 claim 4 theory, the output impedance would be designed to vary across

every input pulse transition (consistent with Petitioner’s Ground 2 claim 4 theory). Nor *could* Petitioner dispute as much in good faith, because the Petition’s Ground 3 claim 4 theory does nothing more than incorporate the Ground 2 claim 4 theory by reference. There is thus no dispute that the Petition’s Ground 2 claim 4 theory involves a system designed to intentionally varying the output impedance between steady-state and transition periods. *See* Section III.A, above.

Petitioner’s sparse attorney argument that the Ground 3 claim 4 theory (which—again—is merely the Petition’s Ground 2 claim 4 theory incorporated by reference) could render claim 4 obvious even if the Petition’s Ground 2 claim 4 theory fails is contrary to common sense and unsupported by any evidence of record. The Reply’s argument relies entirely on a single quote from Muljono, cited only in the Petition’s “Reasons to Combine Itoh and Muljono” section. *See* Reply 19-20 (quoting Pet. 81); Pet. 81 (quoting Ex. 1010, 2:23-27). But Petitioner does not allege that Muljono’s discussion of an “approximately uniform output impedance” would be “approximately uniform” *across an input pulse train*, or explain how Muljono *combined with Itoh* would accomplish as much. And an “approximately uniform” impedance across a pulse train would be directly inconsistent with Petitioner’s *claim*

4 theory in which the “small effect” limitation is accomplished only due to an intentional variation in impedance within the pulse train. *See* Section III.A, *supra*.<sup>8</sup>

Accordingly, the Petition’s Ground 3, claim 4 theory fails for exactly the same reasons as the Petition’s Ground 2, claim 4 theory.

**V. Patent Owner’s arguments address the patentability of claim 4, not claim 1 as Petitioner confusingly suggests.**

Patent Owner briefly responds to Petitioner’s odd suggestion that “[n]ow PO attempts to argue that Claim 4 is patentable because the prior art does not teach Claim 1.” *See* Reply 12. Although “Patent Owner does not concede the merits of any of the grounds identified by Petitioner as to any of the claims” (POPR 1 n.1), Patent Owner focuses *exclusively* on the validity of claim 4 in this proceeding.

Petitioner asserts that focusing on whether the Petition’s claim 4 theory meets each and every requirement of claim 1 is somehow improper. *See* Reply 12 (asserting that it is improper to “rel[y] on the preamble of disclaimed Claim 1”). Petitioner

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<sup>8</sup> Any implication that there are differences between the operation of the Petition’s Ground 2 and Ground 3 combinations with respect to the limitations at issue is undermined by the Reply’s contention that both the Ground 2 and Ground 3 combinations “use the same technology... to achieve the same goal.” *Compare* Reply 13 *with* Reply 17.

presents no authority for that allegation, nor could it, because dependent claim 4 *includes* all limitations of claim 1. *See* 35 U.S.C. §112 ¶4 (pre-AIA) (“A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.”).

As discussed herein and in the POR, Petitioner’s claim 4 theory (in which the prior art is designed to intentionally vary the output impedance on every pulse transition) is inconsistent with the claim 1 requirement that the claimed output buffer circuit be “for outputting data in the form of an input pulse train at a predetermined output impedance.” Accordingly, Petitioner’s claim 4 theory cannot succeed.

## **VI. Conclusion**

Petitioner’s Reply responds to Patent Owner’s reasoned expert testimony with flawed attorney argument. For the reasons expressed herein and in Patent Owner’s Response, all challenged claims should be found not unpatentable.

Date: October 7, 2024

Respectfully submitted,

/James A. Milkey/  
James A. Milkey, Reg. No. 79,503  
Russ, August & Kabat  
12424 Wilshire Blvd., 12th Floor  
Los Angeles, CA 90025

*Counsel for Patent Owner*

**CERTIFICATION REGARDING WORD COUNT**

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 5,599 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

Date: October 7, 2024

Respectfully submitted,  
/James A. Milkey/  
James A. Milkey, Reg. No. 79,503  
Russ, August & Kabat  
12424 Wilshire Blvd., 12th Floor  
Los Angeles, CA 90025

*Attorney for Patent Owner*

**CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))**

The undersigned hereby certifies that the above document was served on October 7, 2024, by filing this document through the Patent Trial and Appeal Board Cast Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

David O'Dell  
Hong Shi  
david.odell.ipr@haynesboone.com  
hong.shi.ipr@haynesboone.com  
HAYNES AND BOONE, LLP

Date: October 7, 2024

/James A. Milkey/

RUSS AUGUST & KABAT  
12424 Wilshire Blvd., 12<sup>th</sup> Fl.  
Los Angeles, CA 90025  
(310) 826-7474

James A. Milkey  
Reg. No. 79,503  
Attorney for Patent Owner