

Inter Partes Review U.S. Patent No. RE43,539

Western Digital Technologies, Inc. v. Longitude Licensing LTD, IPR2023-01286

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IPR2023-01286

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claim 1 of '539 Patent

The inventive concept of the '539 Patent is the predriver with outputs for driving only the first n-channel MOS transistor and only the first p-channel MOS transistor of said main driver.

An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor;

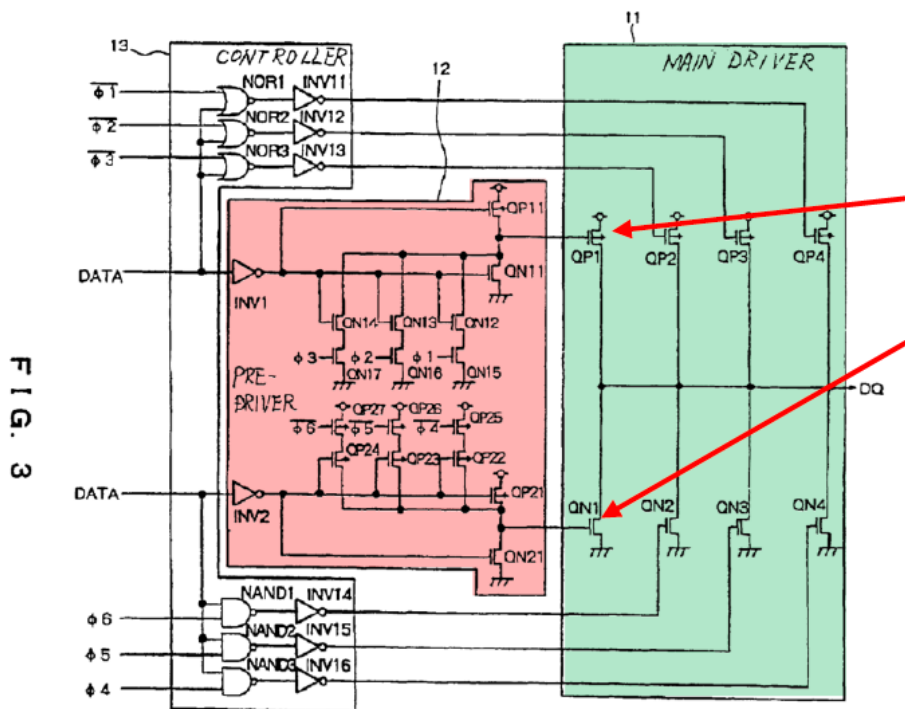
a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor; and

a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor,

wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.

Claim 1 of '539 Patent

The inventive concept of the '539 Patent is the predriver with outputs for driving only first n-channel MOS transistor and only said first p-channel MOS transistor of said main driver.



The predriver 12 (shaded red) drives only QP1 (first p-channel MOS transistor) and only QN1 (first n-channel MOS transistor) of the main driver 11 (shaded green)

Instituted Grounds

Claim Challenged ²	35 U.S.C. §	References
4	103(a) ³	Itoh
4	103(a)	Itoh, Muljono

Inst. Dec. 10, 37.

- After institution, PO presents a new argument that the preamble phrase “at a predetermined output impedance” of disclaimed claim 1 is limiting, and that it is not taught by the prior art. POR, 10.
 - Claim 1: “An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:”

The Petition

The Petition states that “to the extent [the preamble] is limiting”, Itoh “secures the low-output impedance characteristics” of the output buffer, and as such, teaches outputting data “at a predetermined output impedance.”

Itoh teaches the preamble to the extent that it’s limiting. EX1003, ¶¶79-82.

First, Itoh describes an output buffer circuit that receives data (VIN) in the form of an input pulse train and then drives a corresponding output signal VOUT. EX1006, FIGS. 3 and 6 (illustrating generally VIN and VOUT); 3:15-17.

Second, Itoh describes outputting data at a predetermined output impedance and slew rate. For example, referring to FIG. 5, Itoh describes that “the first drive circuit 22 causes the external output signal VOUT to gently rise and fall, and the second drive circuit 23 secures the low-output impedance characteristics.” EX1006, 8:2-5, FIG. 6. Furthermore, a POSITA would have understood by securing the low-output impedance characteristics, the second drive circuit of FIG. 5 performs output impedance control to provide an output having a relatively low impedance.

First, as discussed at Ground 1:[1.0], embodiments of Itoh teach the preamble.

Second, as discussed in detail below, combinations of embodiments of Itoh, e.g., Exmple Embodiment 2.1 (Embodiments 2 and 4 combined), similarly provide an output buffer circuit that outputting data (VIN) in the form of an input pulse train, with output impedance control and slew rate control.

Pet. 47; and Pet. discussion of Ground 2: [1.1]-[1.4];
Thompson Decl. ¶¶ 178-209.

Pet. 13, Ex1006, Itoh, 8:2-5, FIG. 6; Ex1003, Thompson Decl. ¶¶79-82. *See also*, technical description at Pet. 62, and description of Itoh-Muljono at Pet. 81-82; *see also* Pet. discussion of Ground 2:[1.2.3]-[1.3]; Ex1003, Thompson Decl. ¶¶270-283.

The Institution Decision

Patent Owner does not yet contest these allegations, and we find Petitioner's arguments and evidence as to these claim limitations sufficient at this stage of the proceeding.

Inst. Dec. 20-23.

⁶ We do not decide, at this stage of the proceeding, whether the preamble of claim 1 is limiting.

Inst. Dec. 20n6.

Claims 1 and 4

An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor;

a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor; and

a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor,

wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.

An output buffer circuit for outputting data in the form of an input pulse train at **a predetermined output impedance** and slew rate, comprising:

EX1001, claim 1.

4. The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor, and have a small effect on rise and fall times of pulses output from said main driver.

EX1001, claim 4.

PO's Improper Attempt to Add Limitations to Claim 4 Fails.

Claim 1: An output buffer circuit for outputting data in the form of an input pulse train at **a predetermined output impedance** and slew rate, comprising:

The only remaining dispute is the single preamble phrase “at a predetermined output impedance”.

1. PO has already disclaimed claim 1 including its preamble, together with claims 2-3 and 5-12. ID. at 2.
2. Claim 1's preamble phrase “at a predetermined output impedance” is not limiting. Reply, 2-11.
3. Even if it were limiting, PO's construction of this preamble phrase is incorrect. Reply, 20-29.
4. Even if it were limiting, Itoh and Itoh-Muljono each teach this preamble phrase. Reply, 13-20.

2. Preamble Phrase “at a Predetermined Output Impedance” is not Limiting

Claim 1: An output buffer circuit for outputting data in the form of an input pulse train at **a predetermined output impedance** and slew rate, comprising:

Everything in the preamble after “output buffer circuit for ...” is describing the purpose or intended use of the circuit. Reply, 8.

PO incorrectly argues that the entire preamble is limiting because the word “data” is used in the body of the claim.

- In addition to this being part of the intended use of the circuit, the word “data” does not make the preamble phrase “at a predetermined output impedance” limiting. Reply, 8-9, citing *TomTom* and *Nearmap*.

Antecedent Basis of One Term in the Preamble does not Render the Entire Preamble as Limiting

Claim 1: An output buffer circuit for outputting **data** in the form of an input pulse train at **a predetermined output impedance** and slew rate, comprising:

- **PO improperly relies on the antecedent basis of “data” to require that another, independent part of the preamble, “a predetermined output impedance,” be a limitation.** Reply, 7.
 - *TomTom, Inc. v. Adolph*, 790 F.3d 1315, 1324 (Fed. Cir. 2015) “It was therefore error for the district court to use an antecedent basis rationale to justify converting this independent part of the preamble into a new claim limitation.”

A discussion showing the similarity of the preamble of the '539 patent with the preamble in *TomTom* is provided in the Reply at 9, and further at slide 30 of this presentation.

3. Even if the Disputed Preamble Phrase were Limiting, PO's Implicit Construction is Incorrect.

Claim 1: An output buffer circuit for outputting data in the form of an input pulse train at **a predetermined output impedance** and slew rate, comprising:

- PO's implicit construction that the output impedance must be a single value during both static data periods and transition periods is incorrect. Reply, 20-29.
 - It contradicts '539 Patent's disclosure. Reply, 26-28.
- PO's improper requirement that "**a predetermined output impedance**" be "**only...a single**" is contrary to the law. Pet, 21.

'539 Patent Description of Output Impedance

'539 Patent describes output impedance “when” output data is at high-level or low-level.

“pMOS transistors QP2 through QP4 as well as pMOS transistor QP1 drive the load connected to DQ terminal to **adjust** the **output impedance when high-level data is output** from main driver 11. nMOS transistors QN2 through QN4 as well as nMOS transistor NP1 drive the load connected to DQ terminal to **adjust** the **output impedance when low-level data is output** from main driver 11.”

'539 Patent, 6:28-31; also discussed at ID. 4-5.

'539 Patent Describes Output Impedance When Output Data is High-Level or Low-Level

'539 Patent:

“For **adjusting** the output impedance of the output buffer circuit shown in FIG.3, the level of **control signals** $\phi 1$ through $\phi 3$ is rendered low to turn on corresponding pMOS transistors QP2 through QP4 to **lower the output impedance at the high level data is output**. At this time, the greater the number of pMOS transistors that are turned on, the smaller the output impedance. Similarly, the level of **control signals** $\phi 4$ through $\phi 6$ is rendered high to turn on corresponding nMOS transistors QN2 through QN4 to **lower the output impedance at the low-level data is output**.”

'539 Patent, 7:47-58; cited and discussed in Reply, 15.

Itoh teaches the same technique:

“The output buffer circuit 41 has the second drive circuit 42 that includes three sub-drive circuits 42a-42c having different impedances. In accordance with the **select signals** SEL0 to SEL2, at least one of the sub-drive circuits 42a-42c is enabled to select the **output impedance when the output signal VOUT is in a static state**.”

EX1006, Itoh, 10:36-42; Pet. 9; Pet. 47-50 (citing EX1003, Thompson Decl. ¶¶61-63, 186-188); Pet. 62-63, 73-75.

PO's Improper “Only...a Single” Requirement is Contrary to The Law.

Claim 1: An output buffer circuit for outputting data in the form of an input pulse train at **a predetermined output impedance** and slew rate, comprising:

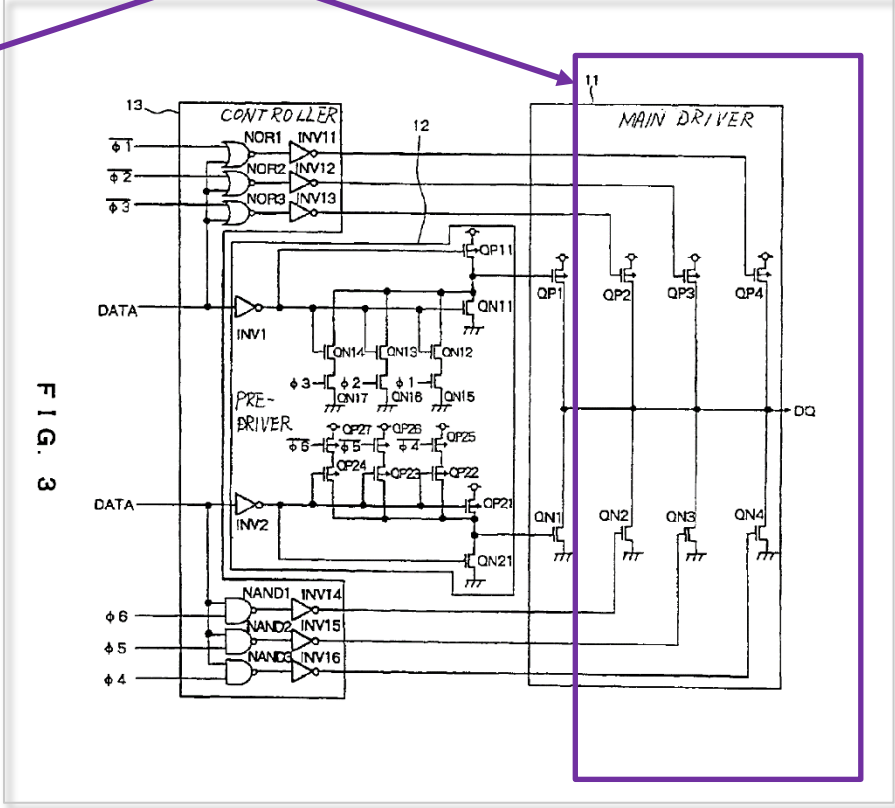
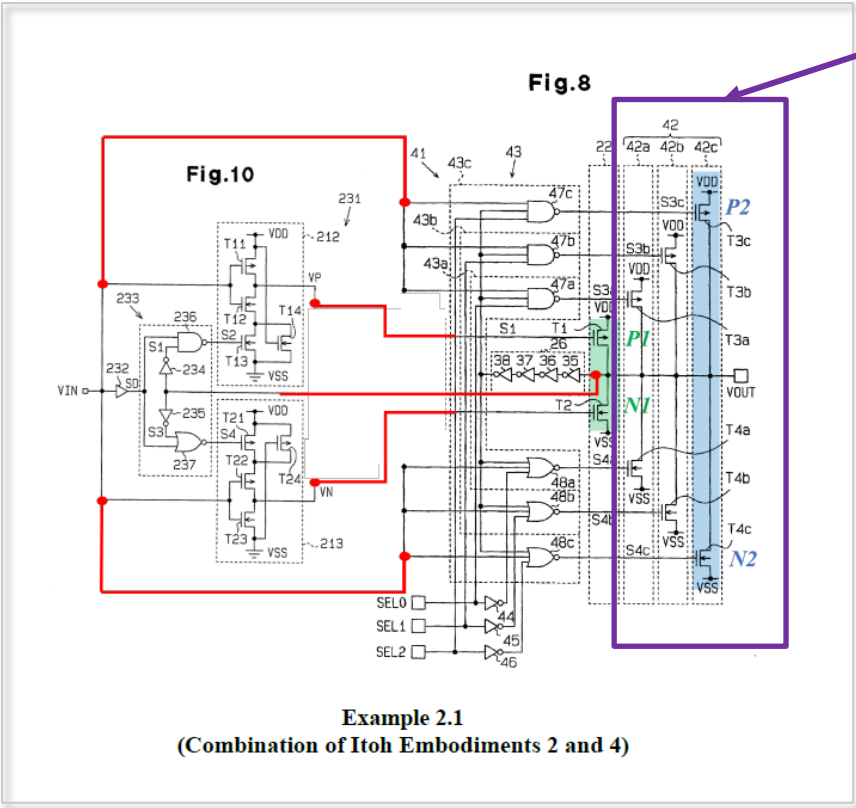
- PO's importation of “*only...a single* predetermined output impedance” into “*a* predetermined output impedance” is contrary to the law. Reply, 21.
 - *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1355-56 (Fed. Cir. 2000) “This court has repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’”

4. Petitioner's Grounds 2 and 3 Each Render the Disputed Preamble Phrase Obvious.

- **Itoh Combination describes the same technique that the '539 Patent described for adjusting the output impedance.**
 - It is undisputed that in Itoh, the output driver outputs data at a predetermined output impedance. Pet, 9, 44, 47, throughout 42-80.
- **Itoh-Muljono further describes using control signals to achieve “an approximately uniform output impedance and slew rate.”** Pet, 81, and throughout 81-99.

Itoh Outputs Data at a Predetermined Output Impedance, Just Like the '539 Patent

Output Impedance Control



Itoh combination from Petition

FIG. 3 of '539 Patent

Pet., 48.

'539 Patent Controls Output Impedance When Output Data is at High or Low Level

'539 Patent:

“For adjusting the output impedance of the output buffer circuit shown in FIG.3, the level of **control signals $\phi 1$ through $\phi 3$** is rendered low to turn on corresponding pMOS transistors **QP2 through QP4** to lower the output impedance at the high level data is output. At this time, the greater the number of pMOS transistors that are turned on, the smaller the output impedance. Similarly, the level of **control signals $\phi 4$ through $\phi 6$** is rendered high to turn on corresponding nMOS transistors **QN2 through QN4** to lower the output impedance at the low-level data is output.”

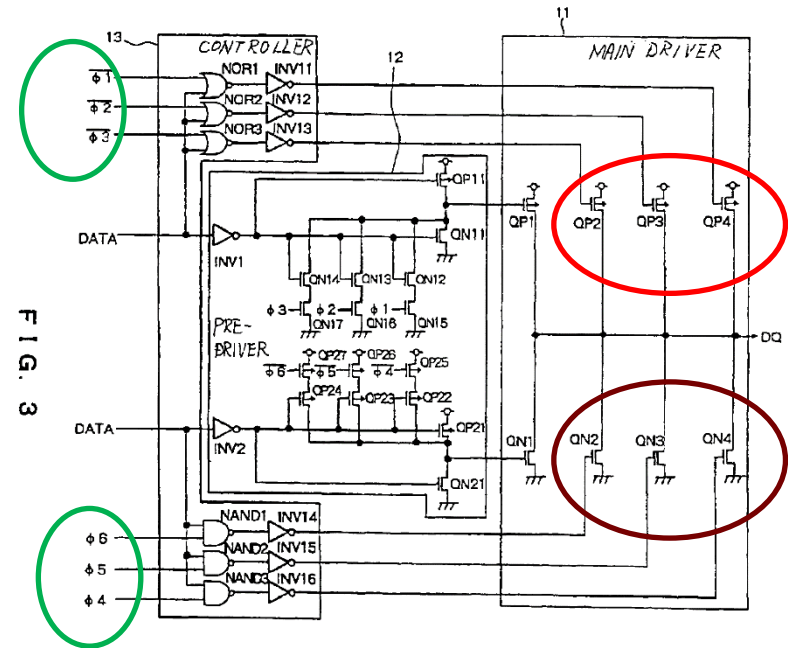


FIG. 3 of '539 Patent

'539 Patent, 7:47-58; cited and discussed at Reply, 15.

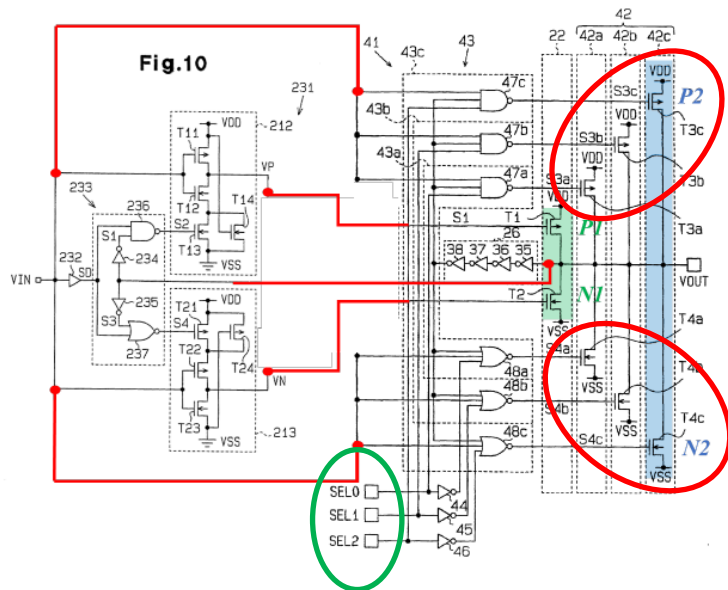
Itoh Uses the Same Technique to Control Output Impedance

Itoh teaches the same technique:

“The output buffer circuit 41 has the second drive circuit 42 that includes three sub-drive circuits 42a-42c having different impedances. In accordance with the **select signals SEL0 to SEL2**, at least one of the **sub-drive circuits 42a-42c** is enabled to select the output impedance when the output signal VOUT is in a static state.”

EX1006, Itoh, 10:36-42; Pet. 9; Pet. 47-50 (citing EX1003, Thompson Decl. ¶¶61-63, 186-188); Pet. 62-63, 73-75.

Fig.8



Example 2.1

(Combination of Itoh Embodiments 2 and 4)

Itoh combination from Petition

Pet., 48.

Itoh-Muljono Outputs Data at a Predetermined Output Impedance.

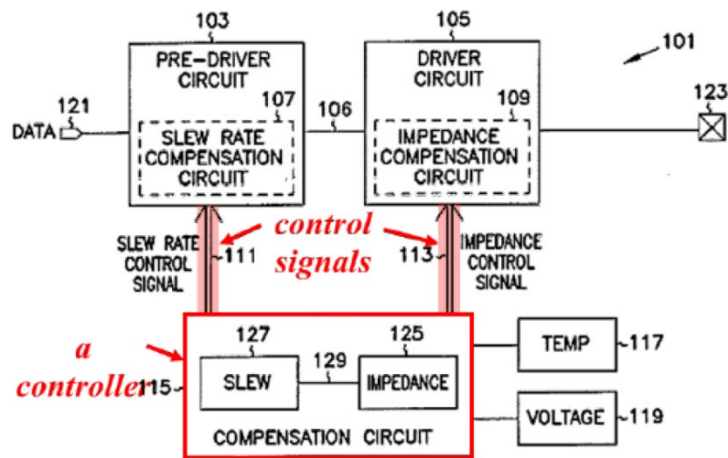


FIG. 1

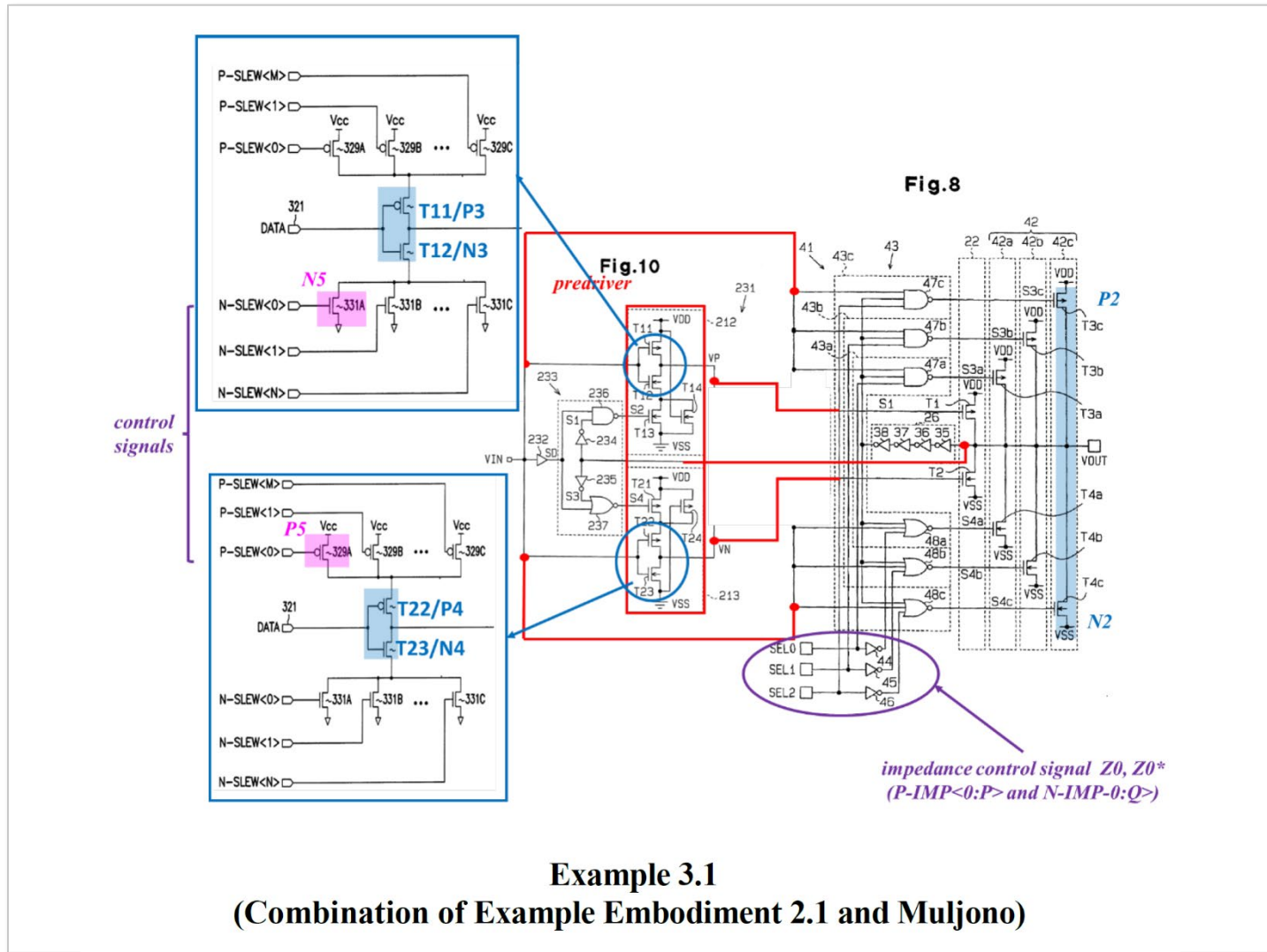
EX1010, FIG. 1, annotated

There remains a need for output buffers in high speed bus structures that operate with an approximately uniform output impedance and slew rate independent of variations in process skew, supply voltage, and temperature. For these and other reasons there is a need for the present invention.

EX1010, Muljono, 2:23-27; Pet. 81.

EX1010, Muljono, FIG. 1; Pet. 87.

Itoh-Muljono



EX1010, Muljono, FIG. 3; EX1006, Itoh, FIGS. 8, 10; Pet. 88.

Inter Partes Review

U.S. Patent No. RE43,539

Western Digital Technologies, Inc. v. Longitude Licensing LTD, IPR2023-01286

David O'Dell,
Hong Shi,
Haynes Boone, LLP
Representing Petitioner Western Digital



Background

34. Output impedance measured the opposition or resistance to current flow. Output impedance for an output buffer refers to the impedance as it appears on the external signal line or bus. The impedance of the output buffer is set by the transistors connected to the output node, and the gate voltage applied to the gate of each transistor since the gate controls the channel charge which sets the resistance of the switch (transistor).

EX1003, Decl. Thompson, ¶134; Pet. 1; Reply, 24.

Background

Generally, transistors with a large width or multiple transistors in parallel that are electrically fully ON provided low output impedance. Transistors that are turned OFF have high output impedance. Transistors **turned on partially** have output resistance between the on and off values.

EX1003, Decl. Thompson, ¶135; Pet. 1; Reply, 24.

MOSFETs do not turn immediately on or off, and so there can be times when both of the driver MOSFETs are **partially on**, while one is turning on and the other is turning off.

EX2005, Decl. Jacob, ¶140; Reply, 24.

Background

Q. Okay. So I can try to restate, and please tell me if I get it right this time.

So when the gate voltage is changed such that it's turning the transistor from on to off, the resistance --

A. Okay.

Q. -- changes from very low to infinite; is that correct?

A. Yes. It changes from low to high. You -- you shut it off, and it's no longer conducting current.

EX1020, Jacob Depo.
Tr., 23:16-25; Reply, 6.

Q. Okay. So I asked is the change of the resistance from very low to infinite a linear change.

Is it a linear change?

A. And I said it depends on how you're measuring it. Are you measuring it, for instance, in time? And the answer would be, you know, no.

EX1020, Jacob Depo.
Tr., 24:11-16; Reply, 6.

Background

*MOSFET channel resistance
 $R_{DS(on)}$ Changes during
Transition Period*

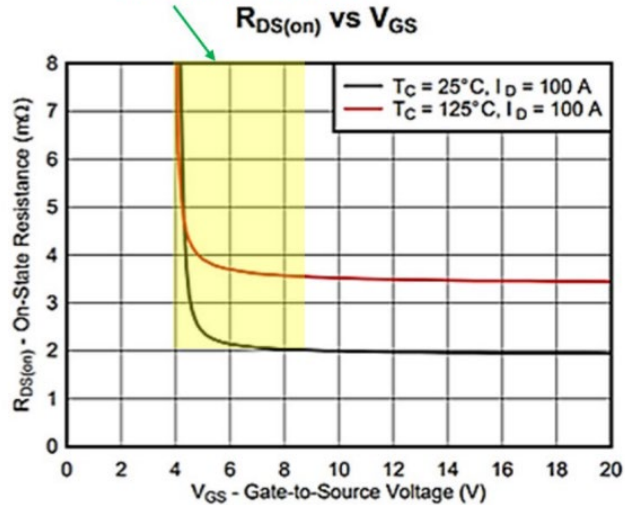


Figure 1. $R_{DS(on)}$ vs Gate Drive Voltage

EX1018, TI Manual, FIG. 1, Reply, 25.

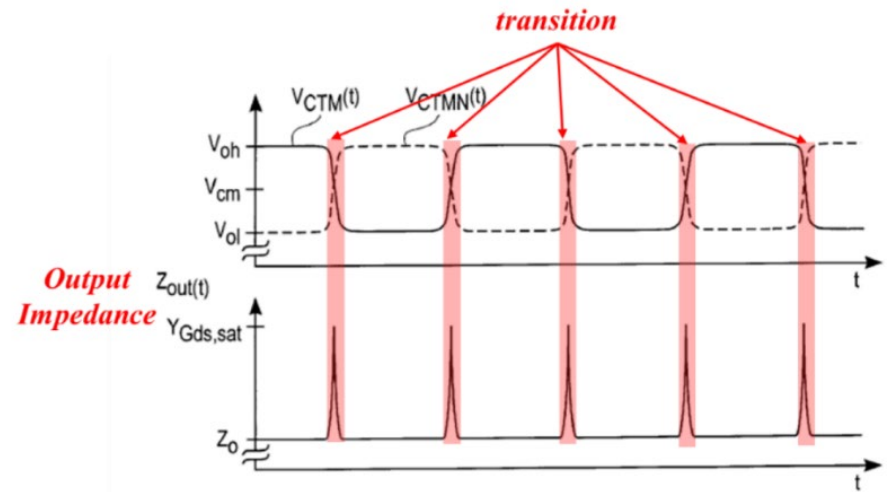


FIG. 14

EX1019, Garlepp, FIG. 14; Reply, 26.

'539 Patent, Claim 1

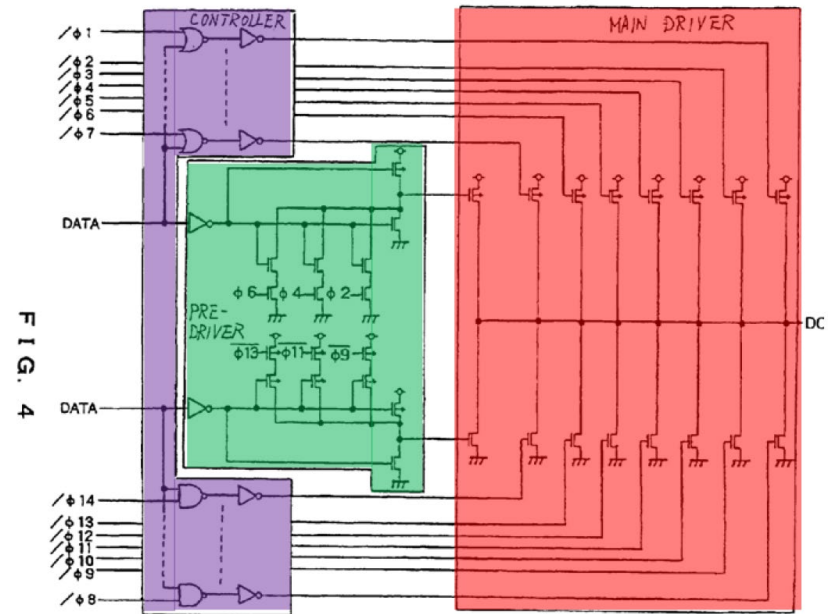
Claim 1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

a main driver ...;

a predriver ...; and

a controller

'539 Patent, claim 1.



'539 Patent, FIG. 4; Reply, 4.

'539 Patent, Claim 4

Claim 4. The output buffer circuit according to claim 1, wherein **said second p-channel MOS transistor and said second n-channel MOS transistor** have a smaller device size with a smaller gate width than **said first p-channel MOS transistor and said first n-channel MOS transistor**, and have a small effect on rise and fall times of pulses output from **said main driver**.

Reply, 4, 11.

'539 Patent

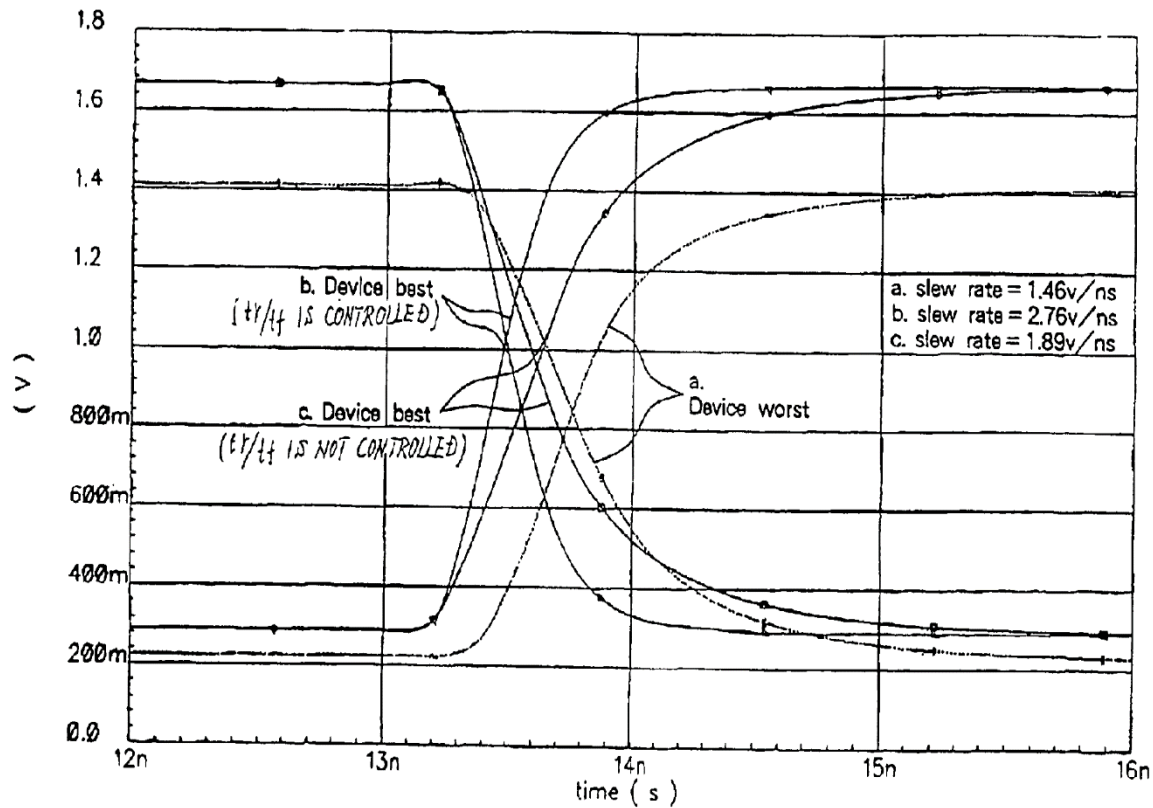


FIG. 6

'539 Patent, Fig. 6; Reply, 22n2.

'539 Patent Prosecution History

- During prosecution, PO did not rely on the preamble to distinguish its invention over the prior art. See EX1005, '059 App, 23-44; Pet. 2-3; Reply 5-6.
- The amendment “a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor” to claim 1 resulted in allowance. EX1005, '059 App, 23-44; Pet. 3.

STATEMENT OF REASONS FOR ALLOWANCE

In the above Examiner's Amendment, all indefiniteness and informalities have been overcome. Further, claims 1 and 4 were amended to be consistent with Applicant's remarks. The applied reference to Atsushi discloses that outputs the “predriver” controls plural output stages, whereas the claims now recite that the outputs of the “predriver” drive only the “first n-channel transistor” and only the “first p-channel transistor”. Since the cited prior art references do not disclose the circuit recited in the pleasant claims, the case is in condition for allowance.

EX1005, '059 App, 23;Pet. 3.

TomTom, Inc. v. Adolph, 790 F.3d 1315 (Fed. Cir. 2015)

- “The preamble of claim 1 of the `836 patent recites “[a] method for **generating and updating data for use in [("the generating language")] a destination tracking system of at least one mobile unit** comprising.”” *TomTom*, 790 F.3d at 1322.
- “That the phrase in the preamble ‘**destination tracking system of at least one mobile unit**’ provides a necessary structure for claim 1 **does not** necessarily convert the entire preamble into a limitation, particularly one that only states the intended use of the invention.” *Id.* at 1323.
- “**the generating language** is not limiting and does not provide an antecedent basis for any of the claims.” *Id.* at 1324.
- “Additionally, the invention claimed in the `836 patent is structurally complete without **the generating language**.” *Id.*

See Reply, 9; Sur-Reply, 5-6.

Nearmap US, Inc. v. Eagle View Technologies, Inc., IPR2022-01090, Paper 31, 22-23 (PTAB Jan. 9, 2024)

- “36. **A non-transitory computer-readable storage medium** whose contents enable a computing system to generate a roof estimate report for **a building having a roof**, by performing a method comprising:” USP 8,078,436 claim 36, cited by *Nearmap* at 22.
- “Independent claim 36’s preamble requires “[a] **non-transitory computer-readable storage medium**.” *Id.* at 22.
- “Although, as Patent Owner notes, a different preamble term (“**a building having a roof**”) provides the antecedent basis for later-used terms, see PO Resp. 59, that “does not necessarily convert the entire preamble into a limitation.” *TomTom, Inc. v. Adolph*, 790 F.3d 1315, 1323 (Fed. Cir. 2015).” *Id.* at 23.
- “Here, claim 36 does not recite any step related to the preamble’s **memory**.” *Id.*
- “Because claim 36 describes a structurally complete invention without the preamble’s **non-transient computer memory**, we find that phrase is not limiting.” *Id.*

See Reply, 9-10; Sur-Reply, 5-6.

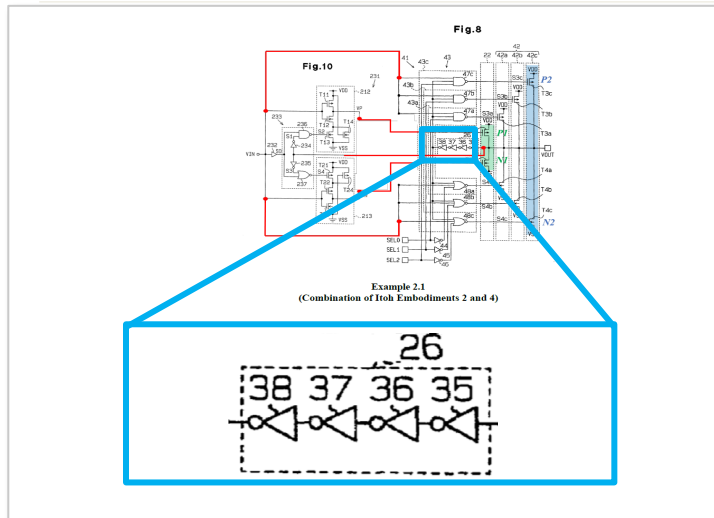
Other Preamble Phrases Do Not Convert “At A Predetermined Output Impedance” Into A New Claim Limitation.

- It is undisputed that the prior art discloses other preamble phrases including “for outputting data” and “input pulse train.” Reply, 8.
- “for outputting data,” while providing antecedent basis to claim 1, does not convert other independent preamble phrases into a new claim limitation. Reply, 8.
- “input pulse train” does not even provide antecedent basis. Reply, 8.

Notably, the body of dependent Claim 4 recites “pulses output from said main driver,” which introduces “pulses” as an element independently from “an input pulse train” recited in the preamble of Claim 1. The preamble of Claim 1 then, cannot be said to provide essential structure or necessary meaning to the claimed invention of Claim 4, because the element “pulses output from said main driver” is independently recited in the body of the claim.

Reply, 11.

Itoh Uses Delay Circuit (Well-Known “Self-Timed Control Signal”) to Output Data at a Predetermined Output Impedance and Slew Rate

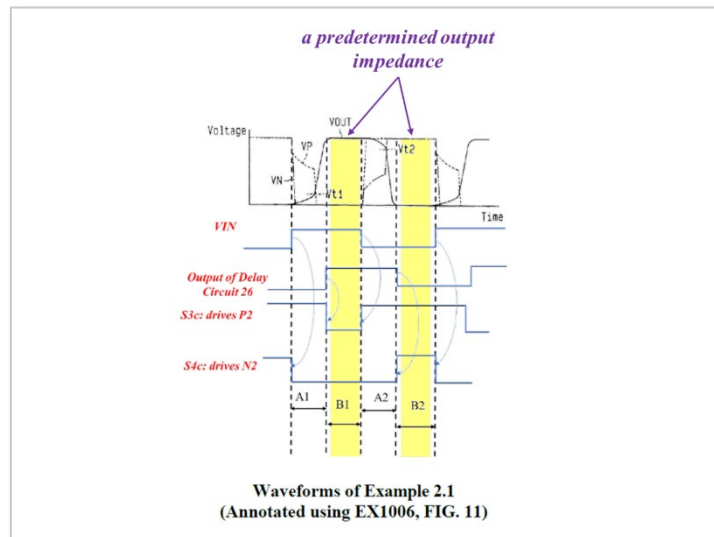


Pet., 48.

Itoh:

“After the external output signal VOUT rises or falls sufficiently, the second drive circuit 23 is driven. The second drive circuit 23 has a low impedance characteristic. Therefore, the first drive circuit 22 causes the external output signal VOUT to gently rise and fall, and the second drive circuit 23 secures the low-output impedance characteristic.”

EX1006, Itoh, 7:66-8:5; Pet. 36.



Pet., 50.

Petition Discussing Itoh Combination:

Any modification required for the combination would have been within the skills of a POSITA. For example, it would have obvious to include various connections, **adjust the delay time of delay circuit 26**, and/or adjust the sizes of the transistors based on the design needs (e.g., required output impedance and slew rate).

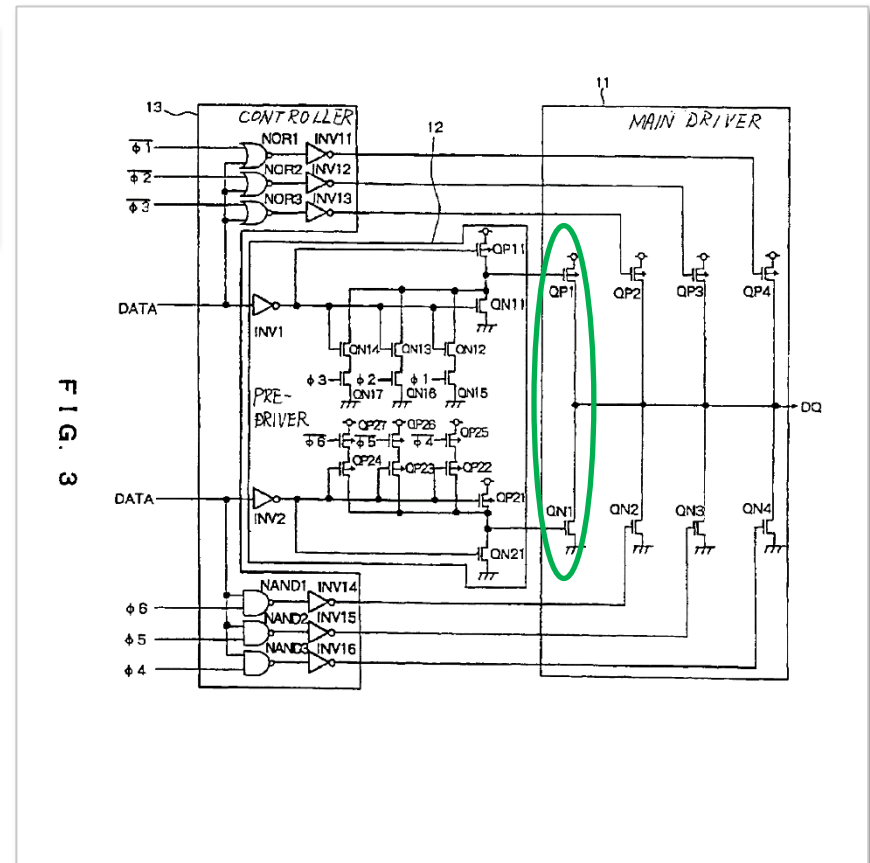
Pet., 46; EX1003, Thompson Decl. ¶177
(Discussing Itoh Combination).

'539 Patent Controls Slew Rate Using *Only* QP1 and QN1.

'539 Patent:

In FIG.3, the ratio t_r/t_f is adjusted using **only pMOS transistor QP1 and nMOS transistor QN1.**

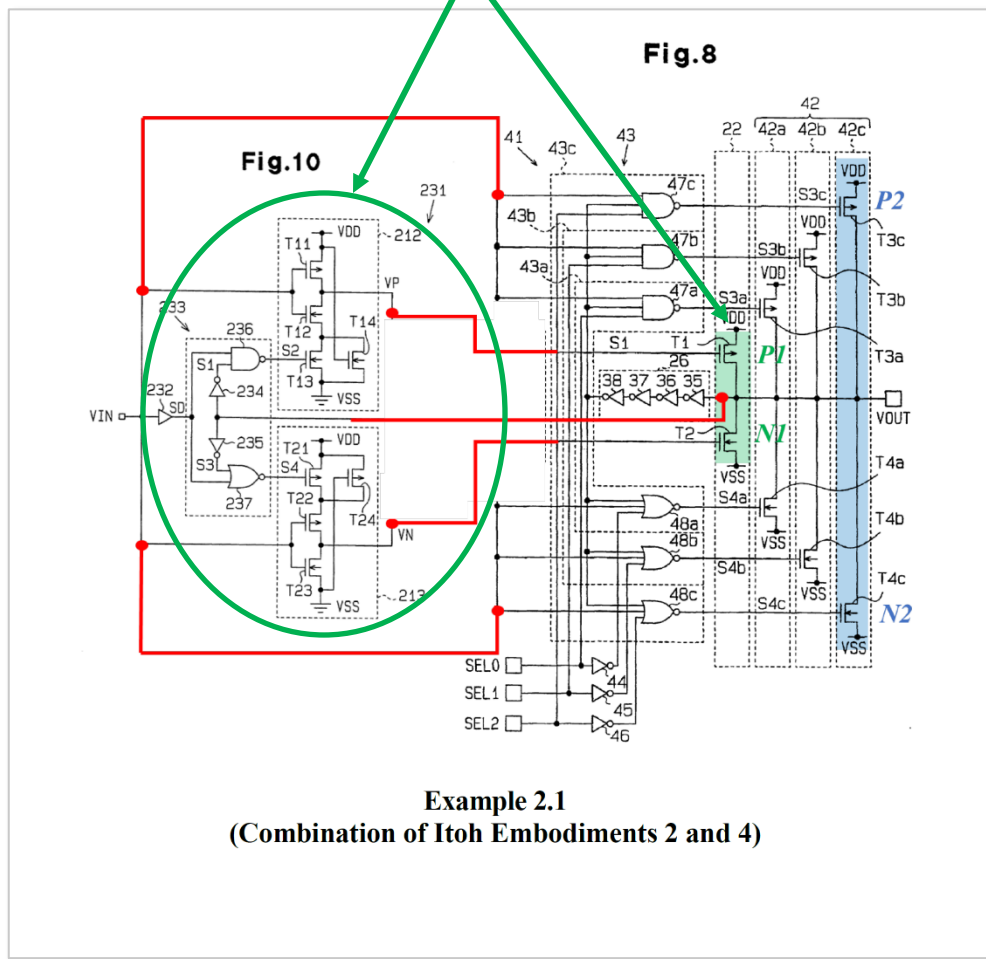
'539 Patent, 8:24-25, further discussed at '539 Patent, 8:25-34, also further discussed at ID., 6.



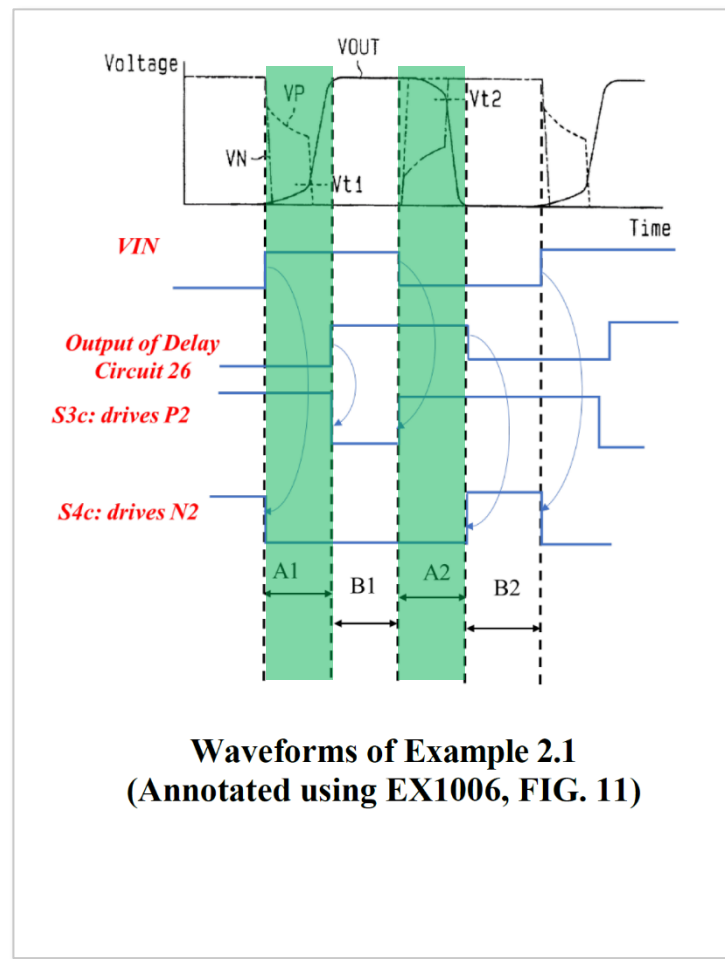
'539 Patent, 8:24-25.

Itoh Uses the Same Claimed Technique.

Slew Rate Control



Pet., 48.



Pet., 62.

Itoh-Muljono Outputs Data at a Predetermined Output Impedance and Slew Rate.

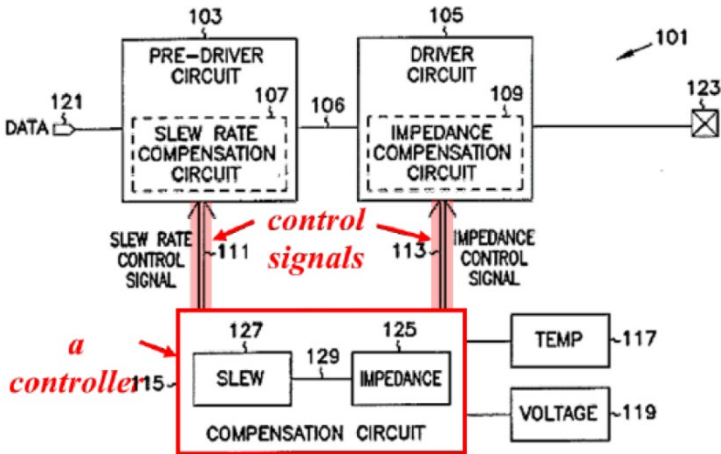


FIG. 1

EX1010, FIG. 1, annotated

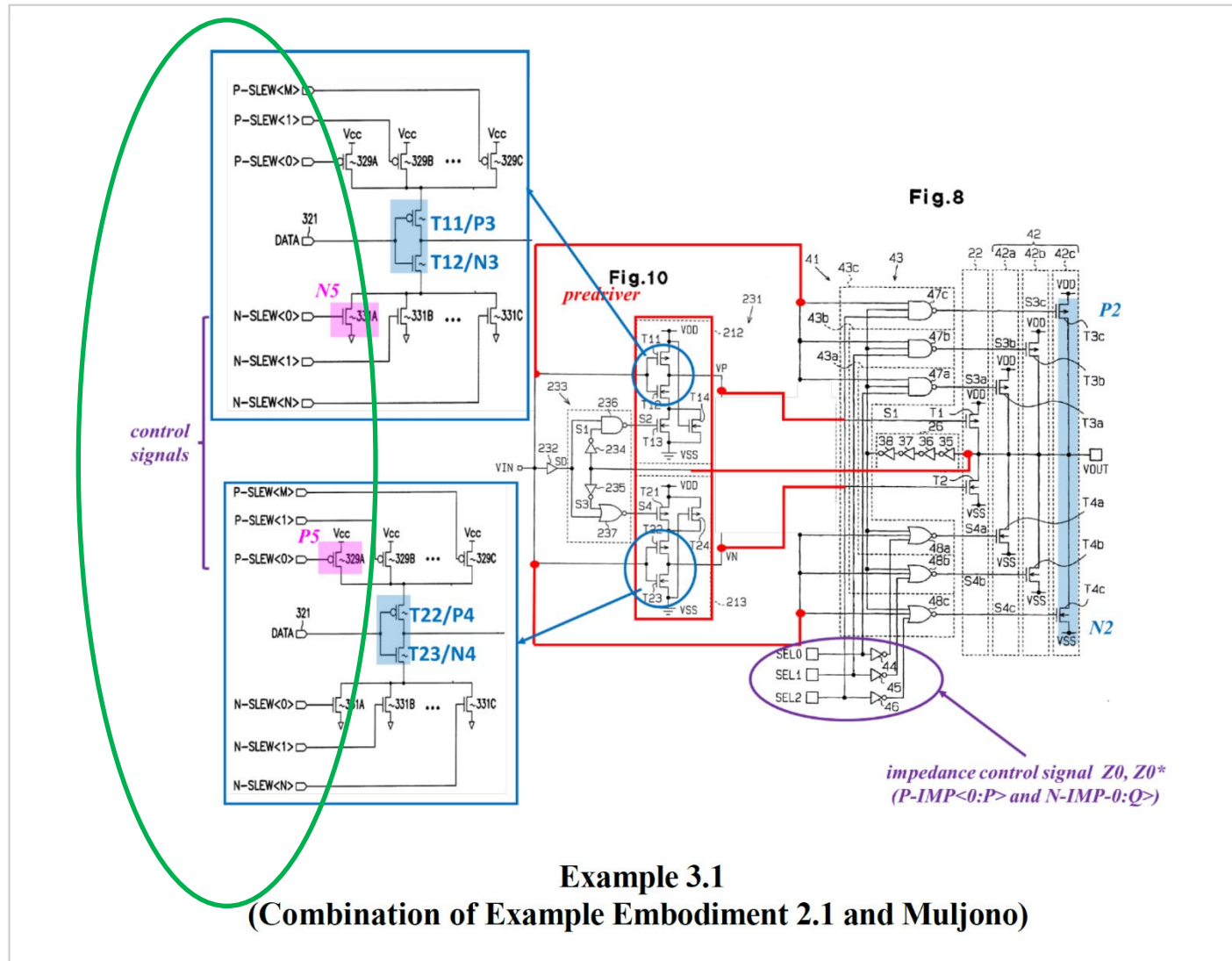
There remains a need for output buffers in high speed bus structures that operate with an approximately uniform output impedance and slew rate independent of variations in process skew, supply voltage, and temperature. For these and other reasons there is a need for the present invention.

EX1010, Muljono, 2:23-27; Pet. 81.

As discussed above, C_{LOAD} changes according to the number of transistors in the driver circuit **105** or **205** that are switched on or off. The signals **Z0**, **Z0*** are generated by the impedance control signal generator **125** to control the transistors in the driver circuit **105** to maintain the output impedance of the output buffer **101** at a desired level as the temperature and V_{cc} change. The signals **P-SLEW <0:M>** and **NSLEW <0:N>** are generated by the slew rate control signal generator **127** in response to the signals **Z0**, **Z0*** to compensate R and maintain the product of R and C_{LOAD} to be approximately uniform as C_{LOAD} changes. The slew rate of the output buffer **101** is thereby controlled to be approximately uniform during changes in the temperature, V_{cc} , and the output impedance, and the slew rate is compensated for the process skew of the chip to support rapid communication on the bus coupled to the pin **123** of the output buffer **101**.

EX1010, Muljono, 6:36-45; Pet. 88.

Itoh-Muljono Uses the Same Claimed Technique.



Pet. 88.