

Western Digital Technologies, Inc..

v.

Longitude Licensing Ltd.

U.S. Patent No. RE43,539

IPR2023-01286

Longitude's Hearing Demonstratives

November 21, 2024

IPR2023-01286
Longitude Ex. 2007

Argument Roadmap

- Challenged claim 4 requires a system that is “for outputting data in the form of an input pulse train at a predetermined... output impedance.”
 - Claim 1’s preamble is necessary to understand claim terms in the body.
 - The inventor understood the preamble to be part of the invention.
- The Petition’s proposed combinations are intended to output an input pulse train at an intentionally varying output impedance.

Patent Owner's expert Dr. Jacob: POSITA would have understood entire preamble to be limiting

- “In my opinion, the preamble of Claim 1 is essential to understanding limitations in the claim body....” Ex. 2005, ¶83.
- “The [preamble’s] notion of ‘a predetermined output impedance and slew rate’ is fundamental to the claimed invention.” Ex. 2005, ¶85.

POR 11-14; Sur-Reply 3-5.

Petitioner's expert testimony

- Petitioner did not provide any expert testimony on the meaning of the preamble

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Preamble provides antecedent basis

[1.0] An output buffer circuit **for outputting data in the form of an input pulse train** at a predetermined output impedance and slew rate, comprising:

[1.1] a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load **according to said data**...

[1.2] ... “at least a pair of... transistor[s] for driving said first p-channel MOS transistor **according to said data**, [and] at least a pair of... transistor[s] for driving said first n-channel MOS transistor **according to said data**....”

POR 11-13; Sur-Reply 4-6.

Petitioner must justify starting point of an obviousness combination

We have repeatedly held a preamble limiting when it serves as antecedent basis for a term appearing in the body of a claim.

In re Fought, 941 F.3d 1175, 1178 (Fed. Cir. 2019).

“In *Catalina Marketing International, Inc. v. Coolsavings.com, Inc.*, we stated that the preamble constitutes a limitation when the claim(s) depend on it for antecedent basis, or when it ‘is essential to understand limitations or terms in the claim body.’”

C.W. Zumbiel Co. v. Kappos, 702 F.3d 1371, 1385 (Fed. Cir. 2012).

Preamble necessary to understand claim 4

- Both parties agree – claim 4 cannot require the system to practice a method of outputting pulses. Thus, the system must be ***designed*** to output these pulses.

[1.0] An output buffer circuit **for outputting data in the form of an input pulse train** at a predetermined output impedance and slew rate, comprising:

[4.0] wherein said second p-channel MOS transistor and said second n-channel MOS transistor... have a small effect on rise and fall times of **pulses output from said main driver**.

POR 12-13; Reply 7; Sur-Reply 8-9.

Preamble necessary to understand claim 4

Undisputed that Petitioner's interpretation, **system** claim 4 would require "pulses output from said main driver" instead of the system being **intended to** output data in the form of pulses from said main driver.

[1.0] An output buffer circuit **for outputting data in the form of an input pulse train** at a predetermined output impedance and slew rate, comprising:

[4.0] wherein said second p-channel MOS transistor and said second n-channel MOS transistor... have a small effect on rise and fall times of **pulses output from said main driver**.

POR 12-13; Sur-Reply 8-10.

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The purpose of outputting an input pulse train according to a single predetermined output impedance is important to the invention

13. An integrated semiconductor circuit device **comprising:**

an output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate....

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Sur-Reply 13

The purpose of outputting an input pulse train according to a single predetermined output impedance is important to the invention

Dr. Jacob:

Matching the impedances of output drivers, transmission lines, and input receivers is important because impedance is a significant factor of signal integrity. Mismatched impedance levels cause signal reflections at every boundary, much like one can see waves cresting in the ocean wherever there are abrupt changes in the water depth. Elimination of these reflections makes the resulting signal smoother and easier to read correctly, which enables faster communications.

Ex. 2005, ¶54.

Sur-Reply 10-12

The purpose of outputting an input pulse train according to a single predetermined output impedance is important to the invention

Dr. Jacob:

Further, it would therefore have been clear to a person of ordinary skill that the output impedance of Takahashi's output buffer would have remained the same over a given pulse train.

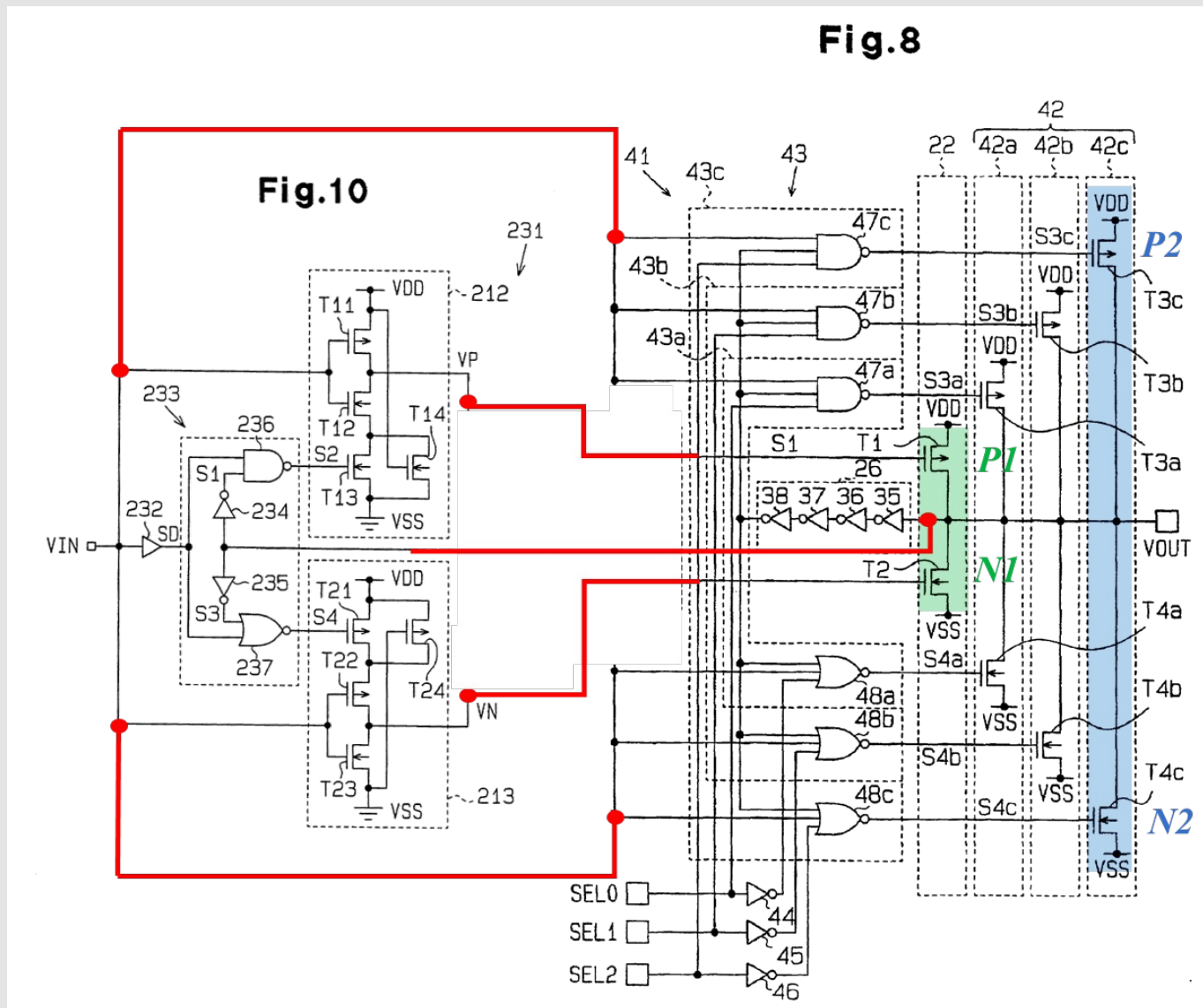
Ex. 2005, ¶78.

POR 14; Sur-Reply 10-12

Argument Roadmap

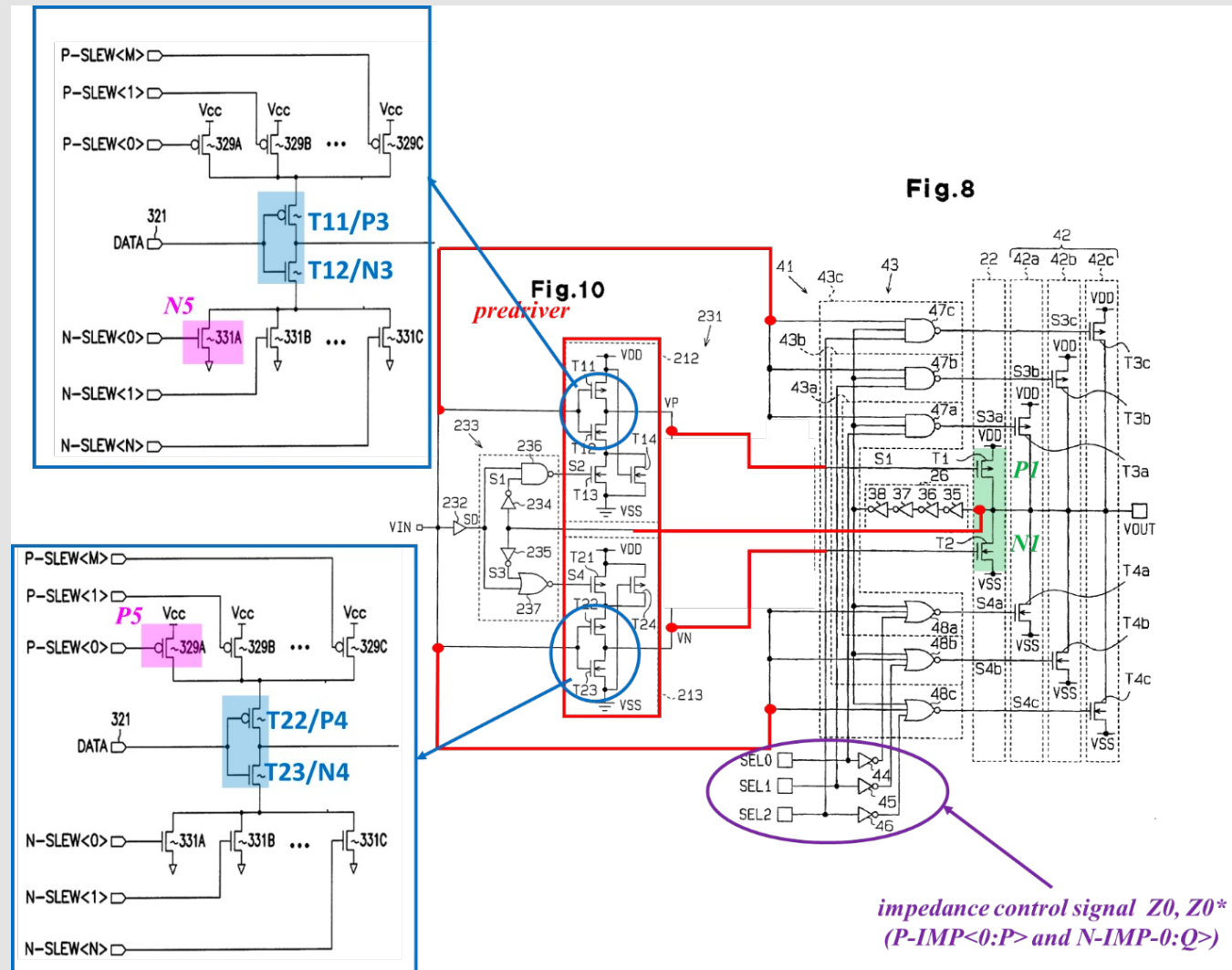
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Petition's Proposed combination

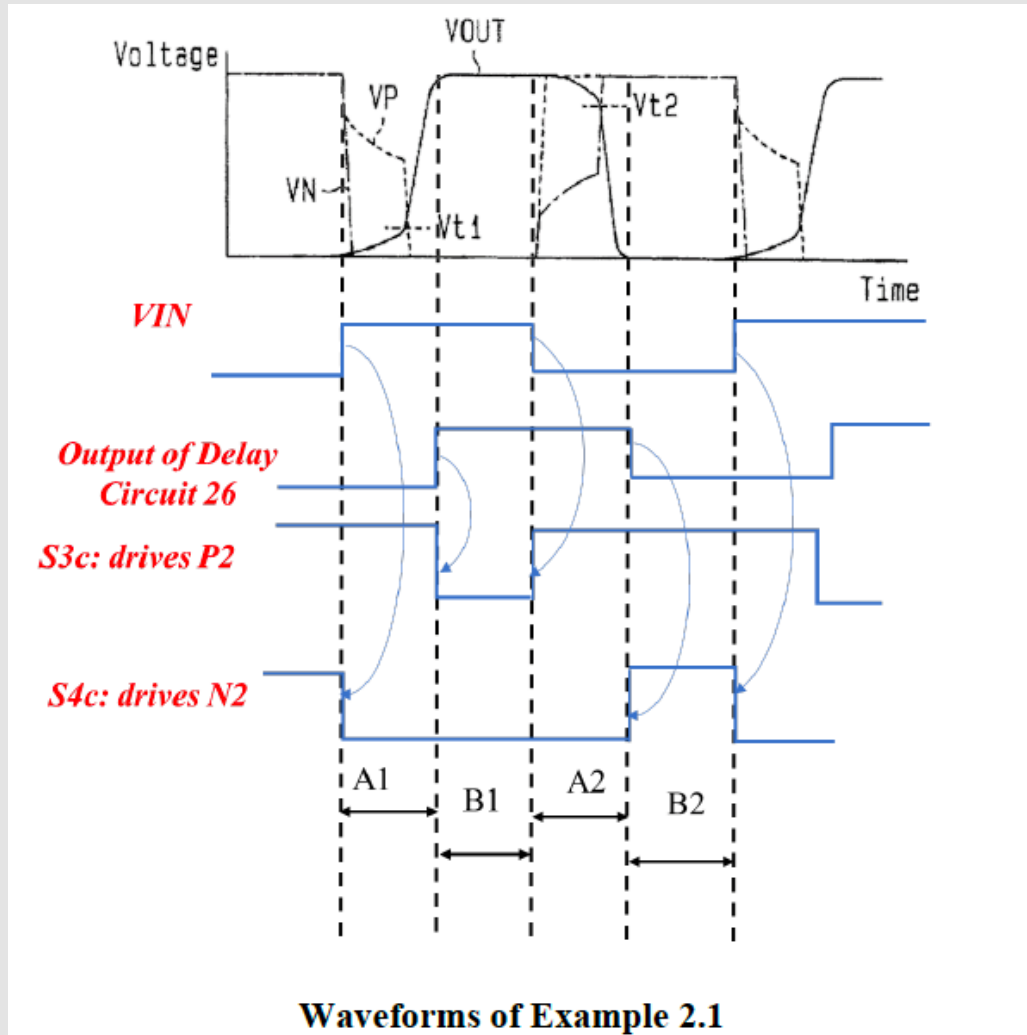


Pet. 61

Petition's Proposed combination

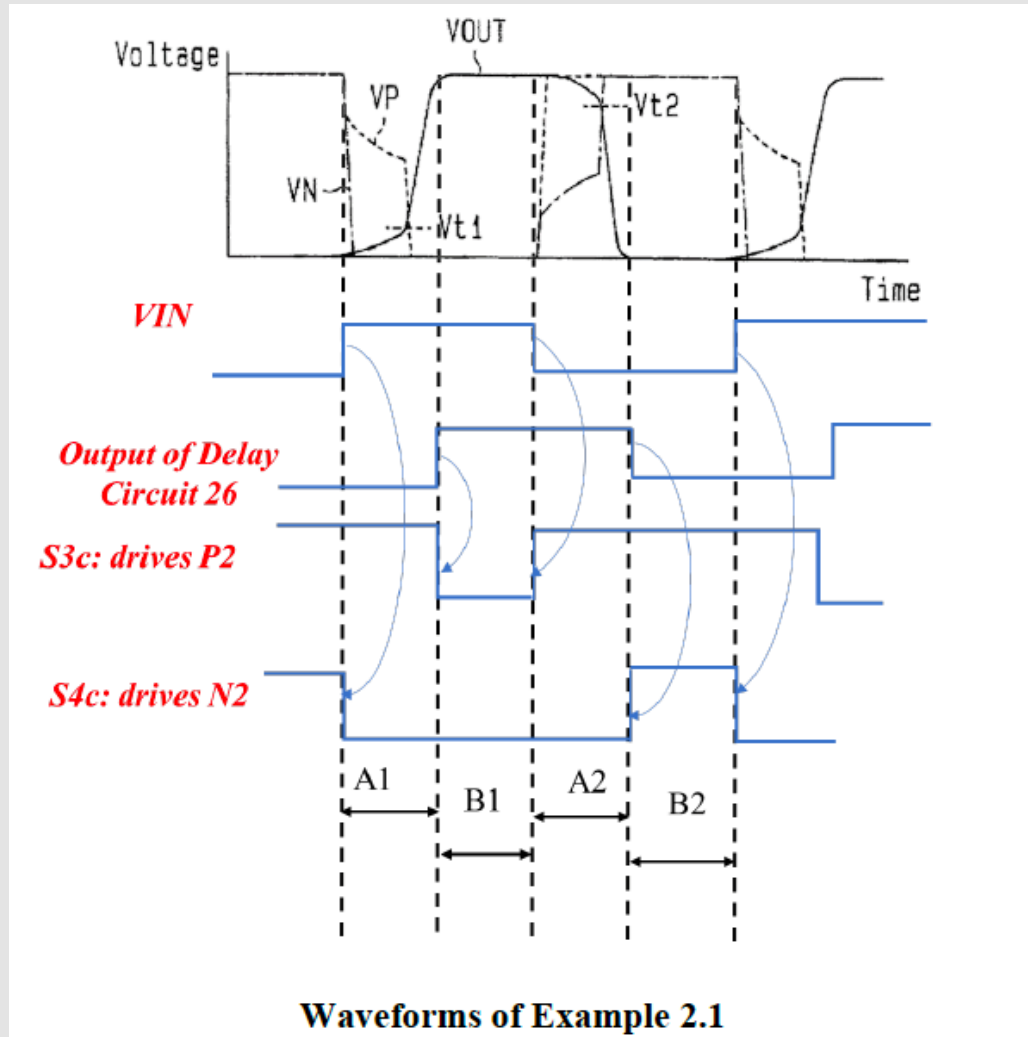


Petition's proposed combination only controls output impedance during A1 and A2



“P2 and N2 are turned off during periods A2 and A1 During B1 and B2 when V_{OUT} is substantially stable, P2 and N2 are turned on for output impedance control.”

Petition's proposed combination only controls output impedance during A1 and A2



8 Q Okay. Does the output impedance of the
9 system change between A1 and B1?

10 A Yes.

11 Q Why does the output impedance change
12 between A1 and B1?

13 A For the same reason I discussed earlier.
14 $S3c$ is changing from A1 to B1. When $S3c$ is low,
15 Transistor $P2$ now becomes low resistance.

16 In the time of A1, $S3c$ is high. And in
17 that case, the transistor is off, so it has high
18 resistance. So a transistor in this application is
19 a voltage-controlled resistor, and that's why the
20 impedance is changing.

Ex. 2006 16:8-20

Undisputed that in the '539 patent, impedance is not intentionally varied within a single input pulse train

Dr. Jacob:

Dr. Thompson uses a mechanism (the output buffer of Itoh) that adjusts output impedance on every single transition (every time a bit is output by the driver), at the end of the transition, to hold the output constant. Takahashi on the other hand, adjusts output impedance only once per recalibration (e.g., once at system startup) and does so to set the drive strength of the output buffer. Itoh's output buffer works very differently than that of Takahashi.

Ex. 2005, ¶103; Sur-Reply 16-17

Undisputed that the operation of Petitioner's combinations is different than operation of the '539 patent

Dr. Jacob:

Dr. Thompson uses a mechanism (the output buffer of Itoh) that adjusts output impedance on every single transition (every time a bit is output by the driver), at the end of the transition, to hold the output constant. Takahashi on the other hand, adjusts output impedance only once per recalibration (e.g., once at system startup) and does so to set the drive strength of the output buffer. **Itoh's output buffer works very differently than that of Takahashi.**

Ex. 2005, ¶103; Sur-Reply 16-17

Unlike the Petition's theory, the '539 patent simultaneously controls slew rate and impedance

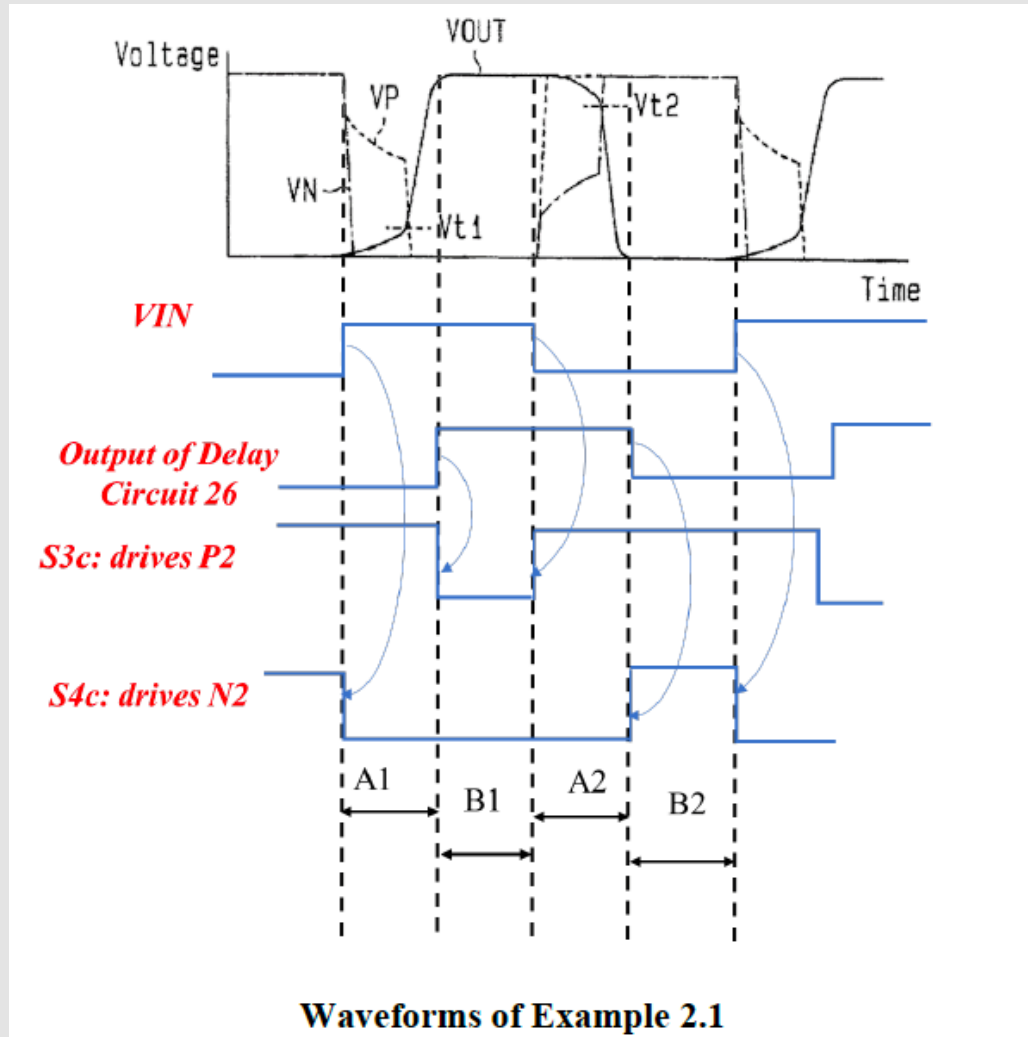
Dr. Jacob:

It is also my opinion that the preamble of Claim 1 reflects a fundamental aspect of the invention. The notion of “a predetermined output impedance and slew rate” is fundamental to the claimed invention. These two aspects, output impedance and slew rate, are always treated as a unit — they are “simultaneously controlled,” which is the primary inventive aspect according to Takahashi and the reason for the received benefits

Ex. 2005, ¶85.

Ex. 2005, ¶185; Sur-Reply 16-17

Petitioner relies on this different operation to allege that the “small effect” limitation is satisfied



As shown in the waveforms of Example 2.1 below, during A1 and A2 where the slew rate is controlled, P2 and N2 are turned off (by control signals S3c and S4c), and as such, have small effect on rise and fall times of V_{OUT} .

Sur-Reply 18-19; Ex. 2006, 17:20-19:12