

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING, LTD
Patent Owner

IPR2023-01286
Patent RE43,539 E

Record of Oral Hearing
Held: November 21, 2024

Before RICHARD M. LEBOVITZ, DAVID C. McKONE, and KEVIN C.
TROCK, *Administrative Patent Judges*.

APPEARANCES:

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The above-entitled matter came on for hearing on November 21, 2024, commencing at 1:00 p.m., via video teleconference.

P R O C E E D I N G S

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JUDGE MCKONE: Hey, good afternoon and welcome. We are here for a final hearing in the inter parties review, IPR2023-01286, captioned *Western Digital v. Longitude Licensing*. Let me introduce the panel. I am Judge McKone. With me are Judges Trock and Lebovitz. Also on the line is Ann Hoang, a patent attorney with PTAB, who is working on the case with us. Let's get the parties' appearances. Who do we have appearing on behalf of Petitioner?

MR. O'DELL: Hello, Your Honors. My name is David O'Dell, and with me is Hong Shi. And I would like to say that in the past 30 minutes, we've been struggling a little bit with Ms. Shi's bandwidth. She is in her office building, and if it needs to be, she's here on the LEAP program, I am ready and able to do this entire presentation if that's the worst case, and she can call in. But I just wanted to give you a warning in case she drops off.

JUDGE MCKONE: Okay. Is she going to be beginning the argument?

MR. O'DELL: I will begin, and then she will be -- we plan for her to do the bulk of the discussion. But if that doesn't happen, then we can work around it.

JUDGE MCKONE: Okay, sounds good. And let us know if there's technical issues, and we'll do our best to help. Who do we have appearing on behalf of Patent Owner?

MR. MILKEY: Yes, Your Honors. This is James Milkey on

1 behalf of Patent Owner Longitude Licensing with the law firm of Russ,
2 August and Kabat.

3 JUDGE MCKONE: Okay. We set forth a procedure today for our
4 hearing today in our oral argument order. According to the order, each party
5 will have 45 minutes of total time to present its arguments. However, I also,
6 as was just mentioned, Petitioner has a LEAP practitioner that will present
7 part or all the argument, and thus will receive an additional 15 minutes.
8 Therefore, Petitioner will have one hour and Patent Owner will have 45
9 minutes. Petitioner has the burden of proof and will go first. Patent Owner
10 will then present opposition arguments. Then, to the extent Petitioner has
11 reserved time, Petitioner will present arguments in rebuttal. Thereafter, to
12 the extent Patent Owner has reserved sur-rebuttal time, Patent Owner may
13 present its sur-rebuttal.

14 As we noted in the hearing order, although we are not appearing
15 remotely and there is no physical courtroom, members of the public have the
16 option to attend remotely via a public line. For example, a journalist might
17 attend that way. In the oral hearing order, we requested that if there were
18 any concerns about the disclosure of confidential information at the hearing,
19 you were to contact the Board. To my knowledge, neither party indicated
20 that they intend to present confidential information. Petitioner, can you
21 confirm that?

22 MR. O'DELL: I confirm. We do not plan to present any
23 confidential information.

24 JUDGE MCKONE: And Patent Owner?

25 MR. MILKEY: Yes, Your Honor, confirmed. We do not plan to
26 present confidential information.

1 JUDGE MCKONE: Thank you. For clarity in the transcript, and
2 since all of the Judges and counsel are appearing remotely, when you refer
3 to an exhibit on the screen, please identify the exhibit number and page
4 number. And when you refer to the demonstrative slides, please identify the
5 slide number. Counsel should unmute only when speaking. If at any time
6 during the hearing you encounter technical or other difficulties, please let the
7 panel know immediately if you can, so that we can make adjustments. There
8 is also technical support listening in, and they will also try to keep their eyes
9 out for technical problems as well. Are there any questions on behalf of
10 Patent Owner at this time?

11 MR. MILKEY: No, Your Honor.

12 JUDGE MCKONE: Are there any questions on behalf of
13 Petitioner at this time?

14 MR. O'DELL: No, Your Honor.

15 JUDGE MCKONE: Petitioner, would you like to reserve a certain
16 amount of time for rebuttal?

17 MR. O'DELL: Yes, 30 minutes for rebuttal.

18 JUDGE MCKONE: All right. Petitioner, are you ready to begin?

19 MR. O'DELL: Yes.

20 JUDGE MCKONE: You can begin whenever you are ready.

21 MR. O'DELL: All right. We're going to share our screen. Does
22 everybody see the title presentation of the slide 1 of the presentation?

23 JUDGE MCKONE: Yes.

24 MR. O'DELL: Okay. Great. May it please the Board. My name
25 is David O'Dell. With me is Hong Shi. Together, we are going to be talking
26 about the IPR of RE '539. Next slide, please. On slide 2, we have a copy of

1 the claim, and I would like to give a very brief and very focused background
2 if I may, that I think will help to clarify some of the issues that are before the
3 Board. And then Ms. Shi is going to describe the substantive discussion of
4 the issues that are before the Board.

5 So, starting very briefly with Claim 1, Claim 1 is directed to an
6 output buffer circuit. The output buffer circuit has the components
7 identified in the body, a main driver, a pre-driver, and a controller. The
8 purpose of the output buffer circuit is for outputting data, data that comes
9 into the circuit in the form of a pulse train, and it outputs that data at a
10 predetermined output impedance and slew rate. On slide 3, here is a picture
11 of the output buffer circuit from Figure 3 of the '539 patent. And the three
12 components there, the controller, the predriver shaded red, and the main
13 driver in green. And I would like to point out, I know everyone's read the
14 patent, so I'm not going to talk about the functionality of this circuit, only to
15 say that there is data coming in on the left of the screen. That data would be
16 in the form of an input pulse train. And then the output, the buffer circuit,
17 and as a whole, outputs data on the right of the screen. And the purpose of
18 the output buffer circuit is to output this data at a predetermined output
19 impedance and slew rate.

20 I would like to discuss very briefly here the terms output
21 impedance and slew rate. If I could slide 28 of the presentation please.
22 Slide 28 of the presentation is simply a photocopy of Figure 6 from the '539
23 patent. And this is a waveform diagram of an output buffer circuit in the
24 embodiments of the specification. And in this, there's a vertical axis, y-axis,
25 that shows voltage of the output. And then there's time on the horizontal
26 axis, measured in nanoseconds. If you look at the first period, 12 to 13

1 nanoseconds, you can see that the voltage is static or steady. And that is, it's
2 the output buffer circuit is either at a V-high or V-low state. If you look at
3 the next period, 13 to 14 nanoseconds, within that period is something we
4 call the transition state. And that is what defines the slew rate. So, on the
5 right side of the figure, there is three example slew rates from this figure.
6 For example, 1.46 volts per nanosecond.

7 I want to make sure it's clear with the Board that the slew rate,
8 although the patent requires or recites a predetermined slew rate, the slew
9 rate is really only the transition period. The period from 12 to 13
10 nanoseconds where the output voltage is static, there is no slew rate or said
11 differently, there's zero. So, slew rate would be zero change in voltage over
12 time. So, when the patent describes a predetermined slew rate, it's really just
13 referring to the transition time and not the static times of the output. And
14 this is, I bring this up because the issue that's before the Board today -- well,
15 there's two issues. One is whether the preamble is limiting. And the other
16 issue is whether the output impedance must be over this entire picture that
17 we have here, or that the output impedance is measured or determined at the
18 static state. That is, not during the transition time. Petitioner -- our position
19 is that output impedance is only here in this example would be from 12 to 13
20 nanoseconds and from about 14 to 16 nanoseconds when the data is at a high
21 or low level.

22 And Ms. Shi is going to discuss that in detail and is going to
23 discuss how the '539 patent specification actually says that exactly. And not
24 only does the patent specification say it, but the prior art references both Itoh
25 and Muljono describe this same thing.

26 All right, back to the sequence of our presentation. Turning to

1 slide 4, this patent has gone through a little bit of a circuitous route. It had
2 two -- it went through original prosecution and then a reissue prosecution,
3 and it's also been before this Board at the institution decision. At no time
4 did the Patent Owner mention that they argue that the preamble was limiting.

5 JUDGE MCKONE: The Patent Owner, of course, doesn't have an
6 obligation to file a preliminary response in the first place. So, the Patent
7 Owner response really is the first required presentation of arguments from
8 Patent Owner. Isn't that right?

9 MR. O'DELL: That is fine. Yes, I agree. I just point that out.
10 And then second, the Patent Owner has disclaimed Claim 1. Claim 4, which
11 is the remaining claim, is a dependent claim, which depends on Claim 1.
12 But they have disclaimed it during the initial proceedings prior to institution
13 so that only Claim 4 is before the Board. Now, Claim 4, of course, depends
14 on Claim 1, so it includes Claim 1. But I do think it's relevant that Claim 1
15 has effectively been donated to the public. And it's now this preamble of
16 Claim 1, which the Patent Owner is arguing as their point of novelty.

17 Okay. I believe we have slides 5 and 6 talk about the petition and
18 the institution decision. All I want to say here is maybe it's slide 6, I want to
19 point out that the Board did not address whether the preamble is limiting at
20 the time of the institution decision. So, that's just a refresher on that.

21 Slide 7. Here we have a copy of the claims at issue in case we
22 need to refer to them. But again, the claim term at issue is this phrase out of
23 the preamble, a predetermined output impedance of Claim 1. And that is the
24 argument that the Patent Owner is making for Claim 4.

25 Okay. All right.

26 JUDGE MCKONE: I think we're all up to speed on that

1 background.

2 MR. O'DELL: All right. And that's all I had too. So, turning to
3 slide 8, here is our agenda for the call today. And the first two points are
4 going to be very brief. Actually, we don't have any slides to the first point
5 other than to say Claim 1 has already been disclaimed. Claim 2 we're going
6 to -- the point two is we're going to show that the preamble phrase at a
7 predetermined output impedance is not limiting. But the bulk of our
8 discussion today is going to be on points three and four about even if it were
9 limiting, we don't believe it is, and we think our reply brief is very strong on
10 this point, so we don't need to belabor it.

11 What I do believe has been -- would benefit from our discussion
12 today is points three and four that the Patent Owner not only is arguing that
13 it's limiting, but they're arguing construction of this preamble phrase that is
14 incorrect and inconsistent with the '539 patent. And with that, I would like
15 for Ms. Shi to take over the discussion.

16 MS. SHI: Good afternoon. My name is Hong Shi and I represent
17 Petitioner. So turning to slide 9, I will first explain why this disputed
18 preamble phrase is not limiting and how both Federal Circuit and PTAB
19 cases support this. So, first is that everything in the preamble after an output
20 buffer circuit is actually simply a statement of intended use. You can see
21 how it does not add any structural limitation to the claim body at all. It
22 doesn't limit the main driver, the pre-driver, or the controller. So, now the
23 Patent Owner actually the only phrase that it relies upon is the word data.
24 So, their argument is that because the word data provided antecedent basis to
25 the claim body that the entire preamble has to be limiting and which includes
26 the disputed preamble phrase at a predetermined output impedance.

1 So, I want first to make it clear that we do not -- there is no dispute
2 that the preamble term data provides antecedent basis to the claim body of
3 Claim 1. However, we do want to make it very clear is that this preamble
4 term data by providing antecedent basis to a claim body does not convert the
5 entire preamble into a new claim limitation.

6 JUDGE MCKONE: Let me ask a question, please. This is Judge
7 McKone. So, do you agree that at least part of the preamble is limiting the
8 data in the form of an input pulse train? Is that much of the preamble
9 limiting?

10 MS. SHI: So first, you don't need to decide whether outputting
11 data or in the form of an input pulse train is limiting because they are not in
12 dispute. Patent Owner does not dispute that the prior art teach these terms.

13 JUDGE MCKONE: Well, I want your position on this. If we're
14 going to evaluate whether the preamble is limiting, you're asking us to find
15 part of the preamble not limiting. I'm just wondering if you have a position
16 on whether data in the form of an input pulse train is limiting by virtue of
17 antecedent basis for terms that appear in the body.

18 MS. SHI: We do not. So, as we explained as the first issue,
19 everything in the preamble after output buffer for is describing the purpose
20 or intended use of the circuit. So as such, they are not limiting. So, our
21 argument --

22 JUDGE MCKONE: Is it your position that -- your position that
23 the recitations of said data in the body of the claim are lacking an antecedent
24 basis?

25 MS. SHI: Our position is it is for intended use of the circuit as we
26 explained in the reply. And even in the body it is also describing the

1 purpose, and as such they do not carry any patentable weight. We do -- our
2 argument is that even to the extent that the word data is limiting, it does not
3 convert either in the form of an input pulse train or a predetermined output
4 impedance, which is a term here in dispute that the Board needs to determine
5 whether it's limiting. So, our argument basically doesn't --

6 MR. O'DELL: If I may add, and I'm hoping to answer the
7 question. We agree that data is in the body of the claim and therefore a
8 limitation.

9 JUDGE MCKONE: Okay. But how about the form of that data,
10 data in the form of an input pulse train? Is that much of the preamble
11 limiting?

12 MR. O'DELL: I don't have a problem within the form of an input
13 pulse train, but a pulse train is, pulses are mentioned elsewhere as being
14 output, not -- I want to make sure we're clear that input and output are
15 different. The data that is output comes into the circuit in the form of a pulse
16 train, but the circuit manipulates the data or the voltage showing the data
17 when it outputs it. The output of the output buffer circuit, we do not agree
18 provides antecedent basis.

19 JUDGE MCKONE: And this is Judge McKone. I will ask you,
20 Mr. O'Dell, when you interject, please let us know who you are. The court
21 reporters are usually pretty good at catching that, but just in case for the
22 record.

23 MR. O'DELL: Thank you for that. Yes. Ms. Shi, you can
24 continue.

25 MS. SHI: Okay. So, I would like to add to what Mr. O'Dell just
26 discussed. Here, this is the overview of Claim 1 and 4. So, our

1 understanding is Patent Owner is trying to say the pulse here in the preamble
2 of Claim 1 is the pulses output from said main driver, and that is incorrect.

3 So, let's go back to slide 3. Here we have data input provided to
4 the input of the output buffer. So, data is in the value of, for example, 0 and
5 1. So, what really is provided to the input is the pulses, which is the input
6 pulse train. And then the output DQ, when we talk about output data, again,
7 it's output pulses. So, the input pulses are different from output pulses
8 because that is the purpose of this output buffer. That brings -- introduces
9 changes to the input pulses such that the output pulses have a different
10 waveform, have a different high level voltage, low level voltage, have a
11 different slew rate. And that's why we have an output buffer. That is to
12 introduce different -- introduce changes of the input pulses such that we can
13 provide output pulses that can be properly communicated onto the bus. So,
14 this is important. I want to make it clear that the preamble phrase input
15 pulse train is very clearly about input and the Claim 4's output buffer, output
16 from said main driver is talking about a different set of pulses that is from
17 the output that has different waveforms, different slew rate, different
18 voltages. So --

19 JUDGE LEBOVITZ: This is Judge Lebovitz. I have a question.

20 MS. SHI: Sure.

21 JUDGE LEBOVITZ: What part of the circuit -- your argument is
22 that it's intended use, but the circuit has to be capable, it has to have a
23 structure that can carry out that intended use. So, what part of the circuit
24 creates the -- where is the impedance in the circuit derived from?

25 MS. SHI: Sure. So, we're at slide 3, Figure 3 of the '539 patent.
26 So, the main driver includes four pairs of transistors, PMOS transistors, and

1 includes four pairs of NMOS transistors. When the data is, for example, the
2 input data is 1, what happens is, we call this pull-up transistors. It will pull
3 this output voltage to high voltage. So basically, this becomes here -- this
4 becomes conductive, and this point is now pulled up to the high voltage so
5 that it becomes the data 1. And when these transistors are fully turned on, so
6 they will be -- when transitioning from 0 to 1, there will be a transition
7 period to turn it from off to on. When it is fully turned on, all these
8 transistors will have a resistance value. And that combined resistance value
9 determines the output impedance. So, more -- if more transistors are turned
10 on then it will lower the resistance, combine the resistance, lower the output
11 impedance.

12 JUDGE MCKONE: Oh, and then the -- I'm assuming this is we're
13 looking at the preferred embodiment and the specification of the
14 (CROSSTALK) --

15 MS. SHI: Correct. Figure 3, yes.

16 JUDGE MCKONE: Okay. Is it your position that the output
17 impedance I guess we could say toggles back and forth between whatever
18 impedance it is at 1 and whatever impedance it is during the transition. So,
19 it behaves like Patent Owner argues that Itoh behaves and that it's the output
20 impedance goes back and forth during the pulse train?

21 MS. SHI: So, yes, this is what Figure 3 of the '539 patent. I
22 understand your question is about how Patent Owner is describing Itoh, but
23 that actually is --

24 JUDGE MCKONE: No. My question is how does Figure 3 here
25 behave?

26 MS. SHI: Right. Thank you for the question, and that's exactly

1 what we covered in our next slide. So, I will give a preview here and then I
2 will dive into the detailed description here. So, this here in '539, yes, it is
3 just like the Itoh reference. When it's switching between 0 and 1 these
4 transistors will be switched from off, from off to on which will change the
5 output impedance, actually, such that it will once it's -- once they're fully
6 turned on, it will reach a predetermined output impedance, when the data --
7 when the output voltage is at the high level.

8 JUDGE MCKONE: Now, when you get to the next slide are you
9 going to tell us, hopefully where your expert has explained this? You know,
10 it's been a little while since I've had my circuits class in college, so having an
11 expert go through this would be helpful.

12 MS. SHI: So, first I would like to go to the '539 patent's own
13 description, which actually explains how it works. This is at slide 12. And
14 what's reproduced here is '539 patent column 6, line 28 through 31. This
15 actually is the paragraph that the Board already considered by itself in its
16 institution decision. So, here the '539 patent describes that the transistors as
17 we just described, the transistors QP2 through QP4 which are the
18 highlighted transistors in yellow in Figure 3 in the main driver, they are used
19 to adjust the output impedance. So, we highlighted the word adjust in green
20 because it says adjust which means changes. It doesn't say maintain or keep
21 a single fixed output impedance as Patent Owner asserted. Again, the '539
22 patent says adjust when the -- adjust the output impedance.

23 And then the next word I would like to emphasize is the word
24 when and this is consistent with what we just described as the background
25 information. This is -- it is talking about the output impedance during the
26 static data period, when the output is either high-level data or low-level data.

1 Because during the transition the output voltage actually is switching,
2 transitioning between high-level and low-level. So, for that it is not 0 or 1.
3 Only when the output voltage exceeds certain level, reach the high level, it is
4 high-level data, only when it goes down to low level, it becomes low-level
5 data. So, here the '539 patent, as recognized by the Board in the institution
6 decision, describes first adjusting the output impedance, and second, this
7 output impedance is describing the impedance when the output data is in a
8 static data state. It is not describing the transition period.

9 MR. O'DELL: Hello, this is David O'Dell. If I can interject to
10 hopefully further answer the question. Our expert explained this in his
11 deposition, which the Patent Owner has highlighted for us in slide 18. But
12 before I go there, I'd like to go to slide 25 of our present -- our
13 demonstrative. So, we have both our expert and we have contemporaneous
14 descriptive documents that describe this phenomenon, this very thing that
15 you're asking about, Your Honor. And the chart on the left is from a TI data
16 book for an output driver circuit or for a transistor, actually, and it shows
17 resistance on the left and that would correspond to impedance and versus
18 voltage, whether the transistor voltage of the gate source, which is
19 determining whether the transistor is on and off. And you can see that the
20 resistance changes dramatically and quickly. So, you've got the pull up
21 transistors going one direction and the opposite transistors going the
22 opposite direction. So, what is shown in Figure 14 from another
23 contemporaneous reference, the Garlepp patent, which we referenced in the
24 reply brief, here we have an output buffer circuit switching between V
25 output high and V output low. And you can see at the transition time that
26 the output impedance changes. It actually increases for that brief period of

1 time, but then it goes back to the normal level.

2 And so, this was also discussed by our expert during his
3 deposition, that testimony, which is Exhibit 2006, page 16, lines 8 through
4 20, where he talks about when the transistor is off it's high resistance. And
5 when it's on, it's low resistance. But that it will -- but when you're
6 transitioning from one to the other, the impedance will change at that
7 moment. So, we have both expert testimony and corroborating
8 contemporaneous evidence that shows that, yes, during transition time the
9 output impedance will change.

10 JUDGE MCKONE: And then do we have any confidence in the
11 record that Garlepp and the other reference you're talking about are
12 representative of what would happen in the circuit of the preferred
13 embodiment?

14 MR. O'DELL: No. For that, we rely on our expert testimony
15 where he is describing the circuit of Itoh. But that's at Exhibit 2006, 16, 8
16 through 20. According to our expert, the '539 patent behaves the same way
17 in that the impedance will change. And that is the point that the Patent
18 Owner is trying to rely on. And we're not disagreeing with that point. What
19 we're saying is the patent, when it describes output impedance, is referring to
20 when the output impedance -- when the data is at the high level or when the
21 data is at the low level. And it says this multiple times. This is one
22 example. And this is it. We show this because this is what the Board
23 focused on in the institution decision, and we're in agreement there. And
24 also the '539 patent, as Ms. Shi said, it adjusts the output impedance. So, the
25 output impedance is changing.

26 JUDGE MCKONE: I think we understand your argument on this

1 point.

2 MR. O'DELL: Okay.

3 JUDGE MCKONE: But I just wanted to confirm that we don't
4 have any direct testimony on the behavior of the circuit of Figure 3. Rather,
5 we have testimony on Itoh and an opinion that Figure 3 behaves the same as
6 Itoh. Am I correct?

7 MR. O'DELL: Yes. Yes.

8 JUDGE MCKONE: Okay.

9 MR. O'DELL: And with that --

10 JUDGE MCKONE: You're about 30 seconds away from your
11 rebuttal.

12 MR. O'DELL: Oh, my goodness. Okay.

13 JUDGE MCKONE: But I think you have other things to cover.

14 MR. O'DELL: Slide 13 now. I'll let Ms. Shi finish with slide 13.

15 MS. SHI: Okay. So, before we jump to 13, I would like to quickly
16 cover a couple of basic points that are not in dispute. So, this is on slide 23.
17 This is both from Petitioner's expert and Patent Owner's expert. Both sides
18 that there is no dispute that the fundamental behavior of MOSFETs is that
19 they are on or off. And there is a third state, which is turned on partially.
20 And during this period, the resistance or which will affect the output
21 impedance will change. And this is from Dr. Jacob's deposition transcript
22 which again states that the resistance of the transistors will switch between
23 low and infinite when it's turned between on and off. And nobody is
24 disputing that Itoh or the '539 patent are not using these fundamental
25 MOSFET transistors.

26 So, we have expert testimonies from both our expert and Patent

1 Owner's experts testifying to the behavior of the MOSFET behavior of the
2 '539 patent.

3 JUDGE MCKONE: Since we're running into the rebuttal, I do
4 have a question though for the Muljono reference, the combination with
5 Muljono. Does that change the form of the output impedance? Or is that the
6 same where the output impedance is going to change during these transition
7 periods and settle according to what you say is just the general behavior of
8 transistors? In other words, is there anything different about adding
9 Muljono that we need to account for? Or is it going to stand or fall with our
10 decision on Itoh?

11 MS. SHI: So, Muljono, what is different from Muljono, the
12 combination of Itoh, Muljono, and Itoh. First, I would like to clarify. I
13 think we have altogether 60 minutes. So, have we used close to 30 minutes
14 already, or?

15 JUDGE MCKONE: You've used about 33 minutes almost.

16 MS. SHI: Okay. So, I would like to finish answering this question
17 first. So, the difference between Itoh and the combination of the Itoh-
18 Muljono is that in Itoh combination, we don't directly specifically show that
19 the same control signals control the output impedance and the output
20 impedance here and the slew rate here. So, Itoh does not show that the
21 control signals -- the output impedance signal and the slew rate control
22 signals are generated together by the controller. That's the difference. And
23 that is how Muljono teaches that it achieves an approximately uniform
24 output impedance and slew rate.

25 So, to the extent --

26 JUDGE MCKONE: But here, and this is Judge McKone. But here

1 by the uniform output impedance, you mean when the data has settled to a 0
2 or 1, not during the transition period, right? In other words, the output
3 impedance is going to change in the same manner as it would under Itoh
4 alone, correct?

5 MS. SHI: So, at least, we will say at least Itoh-Muljono
6 combination teaches the uniform output impedance when in the data state.
7 However, to the extent that Patent Owner argues whatever their technique,
8 for example, control signals, because are used to --

9 JUDGE MCKONE: I just want to know if as far as this uniform or
10 predetermined output impedance, is Muljono, the addition of Muljono any
11 different, or is it still going to -- the output impedance is still going to
12 transition from when you have a steady 0 output data to a steady 1 output
13 data there's a transition period. Is this going to be behave the same way with
14 the additional of Muljono as it was to Itoh alone. That's all I want to know.

15 MS. SHI: Yes. So, to the extent that Patent Owner argues any
16 control signal needs to control it to achieve uniform output impedance, here
17 Muljono teaches that you can have this control signals to control. A
18 POSITA will know how to use the control signals to control the slew rate,
19 and the output impedance to achieve.

20 JUDGE MCKONE: I honestly have no idea whether I got a no or
21 yes to my question.

22 MS. SHI: So, it does change. I guess my answer is, it does change
23 the behavior of the output circuit, output buffer. Yes.

24 JUDGE MCKONE: In a manner that's meaningful with the claim
25 construction dispute that we have.

26 MR. O'DELL: This is David Odell speaking. I think we're just

1 going to rely on the fact that Muljono has control signals that produce a
2 uniform output impedance, and that is the same. That's the same level of
3 detail that the Patent Owner is relying on.

4 JUDGE MCKONE: But what I, what I want to understand is what
5 are you meaning by uniform output impedance here? Is this the same
6 uniform output impedance that we have in Figure 3 of the patent and in the
7 combination of Itoh, or is this a different uniform output impedance?

8 MR. O'DELL: It's the same uniform output impedance we have in
9 Figure 3 of the patent.

10 JUDGE MCKONE: Okay. Under your view of the patent,
11 correct?

12 MR. O'DELL: Yes.

13 JUDGE MCKONE: Okay, thank you. That's all I needed to know.

14 MS. SHI: I would like to use a few more minutes to actually go to
15 slide 13. This is Hong Shi speaking. This will help further confirm and
16 clarify how '539 patent describes its output impedance. So, I will be a little
17 bit repetitive here because the '539 patent here itself is repetitive and
18 consistent with our interpretation of Figure 3. So, consistent with the
19 paragraph on slide 12, if you recall, we emphasize the word adjust and we
20 emphasize the word high-level data and low-level data. So, consistently the
21 '539 patent again describes that the control signal is used to adjust the output
22 impedance by turning on the QP2 through QP4. And here, again, it says
23 low -- when the output impedance is at low-level data or at the high-level
24 data. So, what it added additional clarification is it used the word lower. So,
25 it confirms the meaning of adjusting is not merely changing, it is about
26 lowering the output impedance when the output is either high-level data or

1 low-level data.

2 So, as we explained, when you're turning the transistors from off to
3 on, it will need to transition between very high to lower resistance. And
4 that's how it is used to lower. These transistors are turned on, QP2 through
5 QP4 are turned on by the control signals to lower the output impedance at
6 the high-level data.

7 And it's the same thing for the low-level data. You turn on the
8 nMOS transistors QN2 through QN4 to lower the output impedance when
9 the output is low-level data. So, this is how the '539 patent describes the
10 output impedance. It describes the output impedance in the context when
11 the output-level data is high-level or a low level. And it describes turning on
12 these transistors to lower the output impedance during the transition. And
13 that directly contradicts with Patent Owner's assertion that a predetermined
14 output impedance needs to be a single fixed value of the entire pulses. I will
15 pause here if you have any questions or Mr. O'Dell has any clarification.

16 JUDGE MCKONE: I have nothing further. Would you like to
17 wrap up and begin your rebuttal, or I guess save the rest of your time for
18 rebuttal?

19 MR. O'DELL: Yes. Sorry, this is David O'Dell. Yes, please save
20 the rest of the time for rebuttal.

21 JUDGE MCKONE: Okay. You will have about 19 minutes and
22 45 seconds for rebuttal.

23 MR. O'DELL: Very well. Thank you.

24 MS. SHI: Thank you.

25 JUDGE MCKONE: Patent Owner, would you like to save any
26 time for rebuttal?

1 MR. MILKEY: Yes, Your Honor, 10 minutes.

2 JUDGE MCKONE: And are you ready to start?

3 MR. MILKEY: Yes. Can you see my screen?

4 JUDGE MCKONE: Yes.

5 MR. MILKEY: Okay. Thank you. So, I'll get started into
6 rebutting the specific -- some of the specific points that were raised many of
7 which were new arguments that I'm sort of hearing for the first time in this
8 hearing. But at a high level, Your Honors, there are lots of factual disputes
9 here about how these systems work, about how Itoh operates, about how the
10 '539 patent operates.

11 What I think is really exceptional about this case is despite this
12 case rising and falling largely on factual disputes on many issues, all of the
13 actual relevant issues in this case that the Patent Owner is focusing on don't
14 have any relevant expert testimony from Petitioner on these issues, and they
15 have the burden of proof. If in these proceedings if there's a factual dispute
16 that Petitioner believes that they're right on, there's a pretty simple way for
17 them to meet their burden in that way, and it's to submit an expert
18 declaration where the expert actually addresses these issues, and the expert
19 is then that, you know, the trade-off there is that the expert is subject to
20 cross-examination. You know, in this case, Petitioner decided not to do that
21 and we were unable to cross-examine their attorney argument on these
22 issues. But, you know, these are highly technical issues that I really do think
23 need to be addressed by expert testimony and I certainly would expect that
24 the Federal Circuit would expect in order to meet the substantial evidence
25 burden that, you know, this would have been addressed by expert testimony.

26 Getting into the specific issues, I first want to address a couple of

1 new arguments raised by Petitioner. The first is with regard to, I believe
2 they addressed this on Petitioner's demonstrative. Well, so on our
3 demonstrative slide 8, they made this new argument that the input pulse train
4 is not what's actually output by the system. So, I'm looking at Patent
5 Owner's demonstratives slide 8, and the claim, the preamble clearly says an
6 output buffer circuit for outputting data in the form of an input pulse train at
7 a predetermined output impedance and slew rate. This argument that the
8 input pulse train is not how that data is output is contrary to the claim
9 language.

10 JUDGE MCKONE: Well, what does this mean? They're
11 outputting data in the form of an input pulse train. All that looks like to me
12 is the data output is going to have the same 1s and 0s as what was input,
13 which would make sense, right? I mean, if you have data that's coming in
14 and all this is is a buffer, then if you have a one that comes in, you better
15 output a one. And if you have a 0 that comes in, you better output a 0. Isn't
16 that what this is saying?

17 MR. MILKEY: Yes, Your Honor. So, I think that one, I think that
18 the data that's coming into the system is consistent with the data that's going
19 out of the system. The issue with the input pulse train is that the data is
20 output, it says for outputting data in the form of an input pulse train. One
21 issue with circuits is that the reason you output anything is so it can be an
22 input to something else. So, in this case, the data is output and it's in the
23 form of an input pulse train for something else. And that the data that's
24 output in the form of an input pulse train is at a predetermined output
25 impedance and slew rate. So, you know, this -- I think what's clear from this
26 preamble is that we're talking about the outputs. The data is talking about

1 the outputs and the use of the term input pulse train is just a reference to the
2 fact that the purpose of this data is so that it'll be an input to something else.
3 So, I just wanted to briefly clarify that.

4 And then with regard to Petitioner's slide 28, they made this new
5 argument that the slew rate is 0 during the steady state periods. That's one,
6 again, this is the first time that we've heard this argument, but I don't believe
7 that's how a person of ordinary skill will understand this. I think a slew rate
8 is how fast a pulse transition occurs. It's not correct to say that the slew rate
9 is 0 or infinite or anything like that when a pulse transition is not occurring.
10 The slew rate, by definition, is sort of confined to a pulse transition, and
11 that's what we're talking about. So, you know, to say that the slew rate
12 changes over time within the system, that's not correct. The slew rate is
13 constant because it's the same -- the pulse transitions happen at the same rate
14 throughout the system. So --

15 JUDGE TROCK: Counsel, this is Judge Trock. When the voltage
16 is constant, what is the slew rate?

17 MR. MILKEY: The slew rate is -- there hasn't been expert
18 testimony on this. So --

19 JUDGE TROCK: I didn't ask you that. I asked you.

20 MR. MILKEY: Right. I understand. So, my understanding is --

21 JUDGE TROCK: If the voltage is constant, what is the slew rate?

22 MR. MILKEY: The slew rate, I would say, is not applicable at
23 that point.

24 JUDGE TROCK: But that's not what I asked. What is the
25 measure of the slew rate when the voltage is constant? I didn't ask whether
26 it was relevant or not. What I asked is what is it? If there's no change in

1 voltage, what's the slew rate?

2 MR. MILKEY: I honestly don't know, Your Honor. I think that
3 the slew rate is how quickly something changes on a pulse transition. So, I
4 don't think that -- I think that outside of a pulse transition, there is no
5 applicable slew rate. I just don't -- I'm not sure I know how to answer that.

6 JUDGE TROCK: So, are you saying you can't measure a slew rate
7 if there's no change in voltage? I don't know is an answer. That's fine.

8 MR. MILKEY: Yeah, I don't know that you can.

9 JUDGE TROCK: Okay, thank you.

10 MR. MILKEY: So, I just wanted to get those issues out of the
11 way. Turning back to Patent Owner's demonstratives at slide 2. The claim
12 requires a system that's for outputting data in the form of an input pulse train
13 at a predetermined output impedance. We have -- turning to slide 3 of our
14 demonstratives, we have undisputed expert testimony that the preamble of
15 Claim 1 is essential to understanding limitations in the claim body, and that
16 even just the predetermined output impedance and slew rate is fundamental
17 to the claimed invention.

18 Turning to slide 4. The Petitioner did not submit any expert
19 testimony on this issue. So, turning to slide 5, the Claim 1 preamble is
20 necessary to understand claim terms in the body. On slide 6, we can see that
21 the preamble recites, it's for outputting data in the form of an input pulse
22 train at a predetermined output impedance and slew rate. The body
23 limitations, talk about driving a load, according to said data. And --

24 JUDGE MCKONE: I'd like to ask you about that actually. So, we
25 want to bring in something from the preamble about outputting data. For
26 claim limitation 1.1, okay, they're talking about driving a load according to

1 said data. That looks like it might be on the output side of things. However,
2 1.2, where this is driving the MOS transistors according to said data. That's
3 the, as I understand it, the input side of the driver circuit. So, why would the
4 characteristics of the preamble, predetermined output impedance and slew
5 rate, have anything to do with said data at the input for the driver transistors?

6 MR. MILKEY: So, I think that the language here is referring to
7 the transistor when it's being driven according to said data. It's providing
8 that data so that driving the transistor according to said data, according to
9 here, is used to mean to achieve that data characteristic of the data output at
10 a predetermined output impedance and slew rate.

11 JUDGE MCKONE: Do you have any evidence to support your
12 reading it that way, as opposed to just the characteristics of the data being
13 input?

14 MR. MILKEY: We have expert testimony that says that this is an
15 antecedent basis for according to said data. I don't think that this issue was
16 raised in the briefing. And I don't think that any side addressed this
17 particular question. But in terms of our expert saying that this is something
18 that provides the antecedent basis in this way, there certainly is expert
19 testimony on that. I do not think that that precise question that Your Honor
20 has raised is addressed by expert testimony.

21 JUDGE MCKONE: All right. Well, whatever you can do to
22 enlighten us because if we're going to -- if it's going to be antecedent basis as
23 the reason to bring in something from the preamble, it ought to provide
24 correct antecedent basis for each time said data is mentioned rather than just
25 the first.

26 MR. MILKEY: Yes, and I think it does because driving transistors

1 according to the data means that you drive it in a way that will achieve that
2 data characteristic. So, I don't think that there's any inconsistency there.

3 JUDGE MCKONE: Also, I don't know if you're going to address
4 this or not, but, for outputting data in the form of an input pulse train at a
5 predetermined output impedance and slew rate, that is arguably not
6 structural. The rest of the claim recites very clear structure, transistors and
7 so forth that are clearly structure. Why are we bringing in something that
8 looks kind of methody into a structural claim?

9 MR. MILKEY: That's a great question, Your Honor. And to
10 answer that I want to turn to our demonstrative at slide 8. I think that it is
11 clear that the claim recites that the intended use of this and the intended
12 configuration of the circuit is to output data in the form of an input pulse
13 train. However, this definitely is a system claim. It's a claim for an output
14 buffer circuit comprising things. And so, you can't actually require -- for
15 example, if I were to design the circuit of the '539 patent and just put it on a
16 desk somewhere and never use it, I would still have infringed the '539 patent
17 because I have designed this circuit that is for outputting data in the form of
18 an input pulse train at a predetermined output impedance and slew rate.
19 However, Claim 4 recites that these transistors have a small effect times of
20 pulses output from said main driver. Without the preamble, Your Honor, the
21 Claim 4 recitation of pulses output from said main driver would imply that
22 pulses actually need to be output from said main driver. And that, of course,
23 is not permissible in a system claim. You can't require that the system claim
24 be used for something consistent with the, you know, that it actually be used
25 for something consistent with certain case law.

26 So the --

1 JUDGE MCKONE: I know you're looking at Claim 4 here to have
2 us determine whether Claim 1's preamble is limiting. Is your position that
3 Claim 1's preamble is limiting for Claim 4, but not necessarily for Claim 1?

4 MR. MILKEY: I think that the fact that Claim 4 exists is an
5 indication that Claim 1's preamble is limiting. I don't think that the scope of
6 Claim 1 changes depending whether you're looking at Claim 1 or Claim 4.
7 Claim 1 has a consistent scope, but the fact that the Patentee added this
8 limitation to Claim 4 is an indication that Claim 1 is intended, you know, the
9 preamble of Claim 4 is limiting as an intended configuration of the system.

10 JUDGE MCKONE: Do you have any case law where the Federal
11 Circuit has used a dependent claim to find the preamble of an independent
12 claim limiting?

13 MR. MILKEY: I think the -- I actually -- this, again, wasn't raised
14 in the briefing. I'm not aware of any specific authority on that. I think that it
15 logically follows, though, simply from the patent statute, which says that
16 each dependent claim includes all of the limitations of the independent
17 claim. So, if we're looking at Claim 4, that's its own claim. It has its own
18 scope. And Claim 4 includes all of the limitations of Claim 1. So, the way
19 to interpret, the way to understand Claim 4 is to basically just add on all of
20 the limitations of Claim 1. You know, you have all the limitations of Claim
21 1, and then you add Claim 4. And so, to make sense of --

22 JUDGE MCKONE: Well, let me ask you this. You need pulses
23 output from said main driver in Claim 4 to make your argument for the
24 preamble of Claim 1. In other words, if we scratched Claim 4 out, would the
25 preamble of Claim 1 still be limiting?

26 MR. MILKEY: Yes, Your Honor, because the data that's recited

1 in Claim 1 does provide antecedent basis even within Claim 1. And there's
2 also undisputed expert testimony that this is a fundamental aspect of the
3 invention because of the impedance matching characteristics of, you know,
4 how you would want to do circuit design. But --

5 JUDGE MCKONE: It's really the antecedent basis in Claim 1
6 that's your argument, not this pulses output from said main driver in Claim
7 4, because that's not necessary, correct?

8 MR. MILKEY: I think that these are all independent reasons why
9 the preamble of Claim 1 is limiting. I don't think that -- I answered your
10 question directly in terms of if we scratched Claim 4, how you would
11 interpret Claim 1, but I want to push back on that a little bit. I certainly don't
12 think it's appropriate to just scratch Claim 4 and interpreting Claim 1.
13 Courts consistently look to dependent claims to understand the scope of
14 independent claims through principles such as claim differentiation. And I
15 don't, you know, if something would impact -- you know, the
16 interrelationship between the claims is important, and I certainly don't think
17 it's appropriate to just ignore what Claim 4 says in interpreting Claim 1.

18 And so, you know, ultimately Claim 4 under Petitioner's
19 interpretation would require this, you know, that pulses actually be output
20 from the system. Their -- Petitioner has admitted that that's not appropriate
21 and they also haven't alleged in the District Court that this is indefinite. So,
22 the only logical conclusion can be that Claim 4 does not require pulses to
23 actually be output from the main driver. And the only way that that would
24 be consistent with the claim language would be if the preamble were
25 limiting.

26 JUDGE MCKONE: You're saying pulses output from said main

1 driver has an antecedent basis problem if we don't look at the preamble of
2 Claim 1?

3 MR. MILKEY: Essentially, yes. I think that pulses output from
4 said main driver, it's not strictly an antecedent basis problem. It's more an
5 *IPXL* problem under Federal Circuit precedent where if the preamble to
6 Claim 1 were not limiting, it would improperly mix system and method
7 claims in a way that both parties have acknowledged is not what's happening
8 here. So, I think that would be improper.

9 JUDGE MCKONE: Oh, that was one concern I had for
10 considering the preamble limiting because then we are injecting potentially a
11 method step in. So, that's why I've been a little bit puzzled by your
12 argument here.

13 MR. MILKEY: So, Your Honor, to be clear, we don't contend that
14 the preamble requires that the circuit actually output data at all. You can
15 create the circuit. The circuit can be configured to operate in a certain way.
16 And I can never turn it on and it will infringe because I've created the circuit
17 for outputting data. That's the configuration of the circuit. That's its
18 intended use. It's capable of operating in this way. But what I think is clear
19 about the preamble is that it requires that the circuit be for outputting data.
20 But under *IPXL* and similar cases, intended purpose of system claims is an
21 appropriate thing. That doesn't run afoul of *IPXL* unless the system actually
22 be required to operate in a certain way. And here we're just saying that the
23 intended purpose of the circuit, the intended use of the circuit has to be to do
24 this. That's the distinction.

25 Additional evidence that the preamble is limiting is in Claims 13
26 and 15. This exact same language occurs outside of the preamble in terms of

1 the structural limitations of the claim. That Claims 13 and 15 both have the
2 same introductory portions, which include an integrated semiconductor
3 circuit device comprising an output buffer circuit for outputting data in the
4 form of an input pulse train at a predetermined output impedance and slew
5 rate. So --

6 JUDGE MCKONE: Now, these claims have been disclaimed,
7 right?

8 MR. MILKEY: Yes, Your Honor. My point was that --

9 JUDGE MCKONE: And we haven't been -- there's no -- been no
10 attempt to construe these claims. Correct?

11 MR. MILKEY: Well, I would submit that the only possible way
12 that you can give meaning to the body of these claims is to say that, you
13 know, they're limiting. But yes, I don't -- the construction of Claims 13 and
14 15 specifically is not at issue in this case.

15 JUDGE MCKONE: Okay.

16 MR. MILKEY: And then, again, we have undisputed expert
17 testimony that the, having a, you know, constant intended output impedance
18 is an important aspect of the invention because of how impedance matching
19 and elimination of reflections which result from mismatched impedances
20 makes the resulting signal smoother and easier to read correctly, which
21 enables faster communications.

22 JUDGE MCKONE: So, is your position that in the preferred
23 embodiment of the patent, I think Figure 3 is what we refer to. In that circuit
24 during a transition from a 1 to 0 or a 0 to 1 in the output data, the output
25 impedance stays the same? There's no transition in output impedance?

26 MR. MILKEY: I don't know that it's possible to have a system

1 where the output impedance stays literally the same through all time periods,
2 but the control that determines the output impedance is not intentionally
3 varied. So, the system is attempting to keep the output impedance the same
4 during that whole time period. In terms of how much change there actually
5 is, if there's some sort of microscopic change or instantaneous deviation
6 during some time period, I think that's something that the other side is
7 alleging, but in terms of -- you know, our expert has testified that it stays the
8 same, and that's, you know, in terms of how big any changes, which
9 obviously there's going to be some change in a physical system.

10 JUDGE MCKONE: Now, are we looking at the sum total of your
11 expert's testimony on this point, on the slide that you're showing?

12 MR. MILKEY: No, there's actually lots of expert testimony on
13 this point. I think --

14 JUDGE MCKONE: Does your expert actually go through the
15 circuit and the preferred embodiment and explain how it works?

16 MR. MILKEY: Yeah, it's -- these are -- I'll say it's Exhibit 2005 at
17 paragraphs 60 through 78, discuss the circuit at length and how it operates.
18 And then paragraphs 81 through 87 of Exhibit 2005, give further context.
19 It's pretty long and -- but there is a lot of expert testimony on this point.

20 JUDGE TROCK: Counsel, this is Judge Truck. So, now you've
21 got me confused. What is your position, what is your argument as to what
22 predetermined output impedance means?

23 MR. MILKEY: A predetermined output impedance means that
24 the, again, we're talking about the intended purpose of the system. So, the
25 intent of the system has to be, you know, the way that the system is
26 configured has to be such that it's trying to provide a constant output

1 impedance throughout any input pulse train. Of course, in a physical
2 system, there, it is literally impossible to have a constant physical anything.
3 Like you can't have a constant output voltage on any system over any given
4 period of time because there are going to be fluctuations. But what the
5 system has to be, you know, intended to do, has to be configured to do is to
6 try to output a constant, you know, an input pulse train at a predetermined
7 output impedance.

8 JUDGE TROCK: Okay. So, predetermined does not mean
9 constant?

10 MR. MILKEY: I think in terms of -- predetermined means -- well,
11 what I'll say is, I do think that predetermined means constant. I think that
12 when you read the whole preamble language together, which is an output
13 buffer circuit for outputting data in the form of an input pulse train at a
14 predetermined output impedance, the system is -- the intended purpose of
15 the system is to output data in the form of an input pulse train at a
16 predetermined output impedance. That's the goal of the system. That's the
17 way the system is configured to be operated. But again, in any physical
18 system, you know, claim limitations talk all the time about outputting data at
19 a certain output voltage at 5 volts. That doesn't mean that you can literally
20 have exactly 5 volts output. It can be 5.001 or something like that. You
21 just, you cannot have a completely constant output impedance across any
22 instant in time. It's always going to be changing. That's just the nature of
23 this, you know, the physical reality that we live in that has quantum
24 uncertainty and things like that. So, but the goal of the system has to be to
25 maintain a constant output impedance.

26 JUDGE TROCK: All right. So, then my next question is how

1 much variation is acceptable or allowable to have a constant output
2 impedance?

3 MR. MILKEY: Well, that specific question is not something that's
4 been raised. I think that the specific issue though with Itoh is that there's an
5 intentional variation. The system is shutting off the output impedance
6 control on every transition period, and that's something that's intentionally
7 baked into that system. So, --

8 JUDGE TROCK: I don't want to interrupt, but are you now saying
9 it's a matter of intent that we have to look at?

10 MR. MILKEY: I don't think it's -- I mean, I think that for
11 outputting, when we're talking about intended purpose, it's not sort of a -- I
12 don't think it's like the designer's intent necessarily, but I think that you look
13 at the way the system operates. And if the system is set up to, you know,
14 change these things in a way that is going to -- that's sort of baked into the
15 way the system operates where they are shutting off the output impedance
16 control during certain periods of time and enabling the output impedance
17 control during other periods in time. Obviously, that's not for maintaining a
18 constant output impedance.

19 JUDGE TROCK: Okay, thank you.

20 JUDGE MCKONE: This is Judge McKone. You keep talking in
21 terms of, you know, the intended use and intended purpose of the invention.
22 Usually, it's my understanding that if we look at a preamble, we're looking at
23 whether it's one of two things, a limitation or merely an intended use or
24 merely an intended purpose, where the limitation is just that, a limitation,
25 and an intended use is not a limitation. I mean, are you using the language
26 that you intended to use here? And if so, please explain to me how an

1 intended purpose or an intended use can become a limitation of a claim.

2 MR. MILKEY: So, I think that the key phrase to pick up there,
3 Your Honor, is merely an intended use. The language here is, the system is
4 for outputting data in the form of an input pulse train at a predetermined
5 output impedance and slew rate. This is not merely an intended use. I think
6 that this is what we're talking about is the configuration of the system is how
7 I would phrase that. But whether you were talking about a configuration of
8 the system or intended use of the system, you know, there's no cases holding
9 that. And in fact, there are cases, I don't have them at the ready, but there
10 are certainly cases holding intended uses to be limiting under situations such
11 as this. But whether you view it as an intended use or how the system needs
12 to be configured to operate, there are -- you certainly can't read outputting
13 data to meet, you know, for outputting data along with the rest of the
14 language to be non-limiting because there's clear antecedent basis support.
15 And there are no cases holding an antecedent basis preamble to be non-
16 limiting.

17 JUDGE LEBOVITZ: This is Judge Lebovitz. Well, I mean, you
18 can -- the intended use does imply or infer structure. The circuit has to be
19 capable of performing the use. But again, as somebody said, it doesn't --
20 you can put it on a table and to infringe the claim, it doesn't have to do
21 anything. It just has to have that structure. But I have a question on this
22 predetermined. I thought that in response to Judge Trock's question, you
23 were saying predetermined is sort of constant. But, and maybe I'm wrong
24 about that, but predetermined to me means something completely different.
25 It means it's determined in advance. So, it's sort of like you decide that the
26 output impedance you want the circuit to run at, and maybe you change that

1 during the course so it doesn't necessarily have to be constant. So, I'm a
2 little confused why that term is even in the claim if you want it to mean
3 something else.

4 MR. MILKEY: Well, Your Honor, I think that predetermined in
5 this context if we read it to say that if you could sort of calculate it out, and
6 you see how the system would operate in practice, and you see that, oh, we
7 can calculate that if this transistor is on at this time that this output
8 impedance is going to be roughly 10 ohms, and at this transitional period it
9 will be roughly 20 ohms, I would submit that that would be a meaningless
10 limitation if the predetermined output impedance could just change at any
11 given point during operation of the system, because any system is going to
12 have something where you could calculate out, you know, this is roughly
13 what the output impedance would be at this moment of operation. That's
14 kind of the way that circuit design works, and there's never going to be a
15 situation where we have no idea what the output impedance is going to be at
16 this moment in time. That's not really a possibility under circuit design.

17 JUDGE TROCK: This is Judge Trock. Not to interrupt, but I just
18 want to follow up on Judge Lebovitz's question on predetermined, and I
19 have a tendency to agree with him that predetermined means knowing in
20 advance. It doesn't mean constant. So, if you've got some argument or
21 position to persuade us or persuade me, perhaps, that predetermined equals
22 constant, then I'd like to hear it. But then my follow-up question would be,
23 well, can't predetermined be a range? Why does this have to be a single
24 fixed number? Why can't it be a range?

25 MR. MILKEY: Well, I think output impedance on its own, you
26 know, a determined -- let's get rid of the word predetermined. Let's just talk

1 about determined output impedance. A determined output impedance is not
2 a range. It's not, you know, we're talking about a single number. But in
3 terms of the change of, you know, if we're talking about a changing
4 determined output impedance or predetermined output impedance, we're
5 talking about outputting data in the form of an input pulse train at a
6 predetermined output impedance. So, it's the input pulse train that has this
7 output impedance. And if the input pulse train just has varying output
8 impedances that you could calculate one way or the other at various times,
9 the input pulse train does not have a predetermined output impedance, right?
10 There's a wildly changing output impedance within the input pulse train, and
11 there is no single input pulse train at a predetermined output impedance
12 which the claim requires.

13 So, you know, I just don't -- there's undisputed expert testimony
14 that a person of ordinary skill in the art would have understood, for example,
15 Itoh's combination to not disclose this. The other side didn't even submit
16 rebuttal testimony. I do strongly believe that that's how a person of ordinary
17 skill in the art would have understood this limitation is that in order to give it
18 any meaning at all, you have to say that there has to be a constant output
19 impedance that spans an input pulse train. And that's not a hard thing to do
20 because an input pulse train, you know, is on the order of a microsecond.
21 It's, you know, two input pulses have to have the same output impedance,
22 but the petition's combination doesn't even do that because on every single
23 pulse transition there's this, you know, baked into the system and intentional
24 variation of the output impedance.

25 JUDGE TROCK: Okay, thank you.

26 JUDGE MCKONE: Well, you're into your rebuttal time, and then

1 I'll let Judge Lebovitz ask a question.

2 JUDGE LEBOVITZ: Yeah, just quickly. Did anything happen in
3 the prosecution? Because that's part of claim interpretation, right? In the
4 way that we do it now. Was predetermined part of the original claim? Was
5 it added during prosecution? Is there anything that would help us
6 understand that word that happened during prosecution?

7 MR. MILKEY: I'm not aware of anything from the prosecution
8 that sheds light on this specific question, Your Honor.

9 And then in terms of the petition's combinations, just very briefly
10 on slides 15, on slide 15 of Patent Owner's demonstratives, this is the Itoh
11 combination. And then slide 16 is the Itoh-Muljono combination and both
12 of them operate the same way. The only difference that Petitioner has
13 alleged is that the control signals in purple on the bottom right in Muljono
14 would be controlled in some slightly different way. But what is clear from
15 the petition's Claim 4 analysis, and this is on our slide 17. In their claim for
16 analysis, they rely specifically on these waveforms and specifically on this
17 analysis where P2 and N2 are turned off during periods A2 and A1. And
18 then P2 and N2 are turned on for output impedance control during B1 and
19 B2. So, regardless of anything they want to allege about the Muljono
20 combination, it's clear that in order for Claim 4 to be satisfied under the
21 Muljono combination, this is the only analysis they have for Claim 4 is that
22 P2 and N2 are turned off during A2 and A1, and P2 and N2 are turned on
23 during B1 and B2. And that's the whole reason that their expert testified that
24 you can meet the small effect on rise and fall times limitation of Claim 4.
25 So, this is an important requirement. Basically either the Muljono-based
26 combination satisfies the preamble, or it satisfies Claim 4, but it can't do

1 both. And when I say satisfies Claim 4, I don't mean Claim 4. I mean, it
2 satisfies the small effect limitation of Claim 4. Either it satisfies the
3 preamble limitation or it satisfies the small effect limitation, but they haven't
4 explained how the Itoh-Muljono combination would do both, which
5 obviously they need to show in order to meet all requirements of Claim 4.

6 And I'm happy to answer any other questions, but otherwise I will
7 reserve the rest of my time for rebuttal.

8 JUDGE MCKONE: All right. I have nothing else. Okay.
9 Petitioner, you have 19 minutes and 45 seconds left and you can begin when
10 you are ready.

11 MS. SHI: Thank you, Your Honor. I would like to share my
12 screen again. So, I would like to start with our expert testimony. Give me
13 one second to bring up Exhibit 2006. So, this is our expert's deposition
14 transcript. Are you able to see it on the screen?

15 JUDGE MCKONE: Yes.

16 MS. SHI: So, our expert explained how the design works.
17 Basically the engineer -- as Patent Owner actually does not disagree. This is
18 how it works. The designer will have a design specification that includes the
19 design parameters, including for example predetermined in that
20 specification, the output impedance, the slew rate, and our expert explains
21 there are other parameters, and they --

22 JUDGE MCKONE: Could you tell us just for the record what
23 page of the transcript this is?

24 MS. SHI: Oh, sorry. This is page 11.

25 JUDGE MCKONE: Thank you.

26 MS. SHI: So, our expert explained during the testimony how Itoh

1 and the combination of Itoh and Muljono that actually helps to satisfy better,
2 give the designer more tools, more control signals, more design tools to
3 satisfy all these predetermined design parameters required by the design
4 specification, which includes the predetermined output impedance and
5 predetermined slew rate. And that is our expert's testimony. And
6 interestingly, and good for us is that the same design principle is explained
7 by Dr. Jacob, Patent Owner's expert regarding what predetermined means.
8 So, give me one second to bring up Dr. Jacob's deposition transcript.

9 So here, let's go to page 47.

10 JUDGE MCKONE: And this is which exhibit?

11 MS. SHI: This is Exhibit 1020.

12 JUDGE MCKONE: Thank you.

13 MS. SHI: So, here to explain what predetermined output
14 impedance and slew rate means, Dr. Jacob actually brought into the
15 discussion the JEDEC standard. And that is one of the examples of those
16 design specifications that you provide predetermined output impedance and
17 a predetermined slew rate. And sometimes it's a range. It is not a constant
18 as Patent Owner asserted. A predetermined, what does predetermined
19 mean? It is predetermined by a design specification. And that is exactly
20 what Itoh explained. So, I just looked it up. Itoh exactly had this word, a
21 predetermined specification.

22 So, the purpose of Itoh is to design an output buffer such that it can
23 satisfy all these design requirements, design parameters as specified in the
24 predetermined specification.

25 MR. O'DELL: This is David O'Dell. Could you give the column
26 and line number that you're citing here?

1 MS. SHI: Sorry. This is Exhibit 1006, column 7, line 6. That
2 exactly says predetermined specification. And if you look through
3 specification, actually Itoh talks about the specification throughout. So, I
4 think sometimes it's called external interface specification. So, this is the
5 same predetermined specification. It's called external interface because
6 that's what an output buffer does. It specifies -- it is for a chip to
7 communicate through this external interface over the bus to another device
8 in the system. And this is the specification that defines predetermined,
9 predetermined output impedance and slew rates such that the system is
10 consistent, such that the devices can talk to each other properly, so such that
11 one device can understand the other device. And that is why we need the
12 predetermined.

13 And indeed, let's go back to our expert's testimony -- initial
14 declaration. Patent Owner repeatedly said our expert, Petitioner's expert
15 didn't explain what this patent, what '539 means, or what the preamble
16 means. That's incorrect. So, actually back in Dr. Thompson's declaration,
17 even in the background, Dr. Thompson has explained -- let me get the page
18 number. This is Exhibit 1003. Explained that the output impedance and
19 slew rate are two fundamental requirements of the design of an output
20 buffer. It cannot be the inventive feature as Patent Owner asserted. Having
21 an output buffer to have a predetermined output impedance and slew rate,
22 that's the fundamental basic requirement of an output buffer. And here is
23 paragraph 32. This is Dr. Thompson's word. Here are two important
24 inherent properties of an output buffer. They are output impedance and slew
25 rate. And it was basic knowledge to design output buffers with output
26 impedance and slew rate control well before '539 patent. And it was found

1 in textbooks. And I believe Dr. Thompson also cited the textbooks and
2 supporting references for that.

3 So, Patent Owner cannot after the long prosecution history, after
4 failing to rebut all the limitations, specific limitations of how the controller
5 controls the very specific arrangement of the transistors and how they
6 interact with each other. Now come back and say, hey, no, our invention is
7 not any of these detailed limitations, how these complicated connections and
8 especially how the pre-driver, which is a limitation, get them into allowance
9 that drives only a single pair of the transistors in the main driver. It's the
10 fundamental basic design principle that Itoh and Muljono all based their
11 invention on. That's our inventive feature. And that is because they
12 introduced this fabricated requirement of a single constant output impedance
13 throughout the entire pulses.

14 They are saying we didn't provide any expert evidence. This is
15 incorrect. We provided our experts' declarations and testimonies twice,
16 which are consistent, were supported by Dr. Jacobs' declarations and
17 evidence, were supported by '539 patent itself, its prosecution history,
18 supported by numerous prior art references. It is Patent Owner's argument,
19 on the other hand, that doesn't have any support other than its conclusory
20 statement from their expert.

21 So, if you will allow me, I will go through some of the details of,
22 for example, what input pulse means and what output pulses mean. So, let's
23 go to, let me get the paragraph number first. So, let's go to paragraph 180 of
24 Exhibit 1003. Let me see if I can find it. So, first, I want to remind the
25 Board that none of these terms, other than predetermined output impedance,
26 is in dispute that the prior art teaches it. So, here, our expert explains that

1 Itoh, the example 2.1, provides an output buffer circuit. Outputting data,
2 VIN, that's where pointing to the input data, in the form of an input pulse
3 train with output impedance control. This is our expert testifying what his
4 understanding of the preamble is and why.

5 JUDGE MCKONE: Can you identify where we're at here? What
6 exhibit?

7 MS. SHI: Yes, it's Exhibit 1003 and paragraph 180. And, also, I
8 would like to note that our expert's discussion of this predetermined output
9 impedance and slew rate, that is not limited to preamble 1.0. Our expert
10 said, as discussed in detail, because this is where we explained in detail how
11 the main driver, as we shaded in green in Figure 3 of the target patent, how
12 the main driver controls the output impedance. We explained in detail here
13 in the detailed limitations. And then we go to the other limitations related to
14 pre-driver, and we explain how a predetermined slew rate is taught by our
15 combinations. And then it also go to the limitations related to the controller
16 of how, as claimed by the target patent, how the controller controls the
17 transistors in the pre-driver and in the main driver in co-action. So, that's --
18 and none of those are in dispute. So, Patent Owner was not able to point to
19 any specific limitation. Actually pinpoint to the ones, that claim term that
20 achieves this single constant output value. They couldn't. They instead go
21 to Claim 4, and as Your Honor already asked, first the pulses there are --
22 they do not even use anything in the preamble for antecedent basis. And
23 second, Claim 4 is really about slew rate. It is about rise time and the fall
24 time.

25 So, now they're saying look it's the Claim 4 limitations related to
26 rise time and fall time that actually requires the term predetermined output

1 impedance to bring life into me. And this is how I --

2 JUDGE MCKONE: Could you pull up Claim 4, please.

3 MS. SHI: Of course. So, here is slide 7 of the slides.

4 JUDGE MCKONE: Okay. We have a small effect on rise and fall
5 times of pulses output from said main driver. Is that?

6 MS. SHI: Slew rate. Yes.

7 JUDGE MCKONE: Is that limiting? That last clause. And have a
8 small effect on rise and fall times of pulses output from said main driver. Is
9 that limiting or is that merely a statement of intended use or how should we
10 evaluate that?

11 MS. SHI: We -- there's no dispute that the prior art doesn't teach
12 it. So, you don't need to determine whether it's limiting, even to the extent
13 that it's limiting --

14 JUDGE MCKONE: Indulge me, what do you think. How is it
15 evaluated?

16 MS. SHI: What do I think whether it's limiting?

17 JUDGE MCKONE: Yes.

18 MS. SHI: In District Court we argued the small effect is indefinite.
19 Here, there's no dispute that the prior art teaches it because --

20 JUDGE MCKONE: Are you willing to take a position on whether
21 that clause is limiting?

22 MS. SHI: The entire clause?

23 JUDGE MCKONE: And have a small effect on rise and fall times
24 of pulses output from said main driver.

25 MR. O'DELL: Your Honor, this is David O'Dell. No, we're not
26 willing. This is a new issue for us that I think answering it on the fly like

1 this --

2 JUDGE LEBOVITZ: This is Judge Lebovitz for one sec. I
3 thought you pointed to declaration evidence that said slew rate and
4 impedance are characteristics of circuit design. If that's true then you are
5 taking the position from what you pointed to that this is a limitation.
6 Because you said that slew rate and impedance are pre-de -- are part of the
7 design of a circuit and that's what you are arguing for the predetermined
8 part.

9 MS. SHI: So, rise and fall --

10 MR. O'DELL: Again, this is David O'Dell. We're not going to be
11 able to answer that question on the fly here. So, we have no response. I
12 would like to point out, though, that it -- Claim 4 does not say said pulses. It
13 just says pulses output from the main driver.

14 JUDGE MCKONE: Sure. We understand that. I just want to
15 make sure that we're reading -- if we're looking at language, it's not very
16 structural and could be interpreted as intended use. We do that in a uniform
17 manner. It sounds like we may not have help from Petitioner on this
18 particular clause, and that's fine. We'll let you continue on with the
19 remainder of your presentation.

20 MS. SHI: And I would like to, I think we didn't get to address the
21 two cases we relied upon to rebut Patent Owner's argument regarding
22 whether the preamble is limiting. So, I would like to quickly touch upon
23 that. So, this is -- Patent Owner relied upon, really, as Your Honor noted,
24 data was the only word used in the body of the claim, and we have two
25 cases, actually, contrary to Patent Owner's assertion where the Court is very
26 clear that the antecedent basis rationale of one term cannot be used to turn

1 the entire preamble into a new claim limitation.

2 And I want -- this is very important, and I want to actually read
3 the quote from Federal Circuit into the record. So, this is from the case
4 *TomTom*, we're at slide 10 of the presentation. The Federal Circuit said it
5 was therefore error for the District Court to use an antecedent basis rationale
6 to justify converting this independent part of the preamble into a new claim
7 limitation.

8 So on slide -- I would refer you to slide 30 and 31, where we
9 actually included the specific preambles and the separate phrases in dispute
10 in those cases, which actually further illustrates how Patent Owner's
11 argument was just those rejected in *TomTom* and *Nearmap*. And I will
12 pause here if you have any questions or --

13 JUDGE MCKONE: I do not. You have about a minute and a half
14 if you want to do any closing remarks.

15 MS. SHI: So, another -- one last issue I would like to address is
16 that I would like to go back to the claim language, is that the said data
17 actually really in Claim 1 is talking about the input data because here the
18 driver needs to -- pre-driver needs to drive the transistors according to the
19 data. If the data is output data, this is not what the pre-driver -- the patent
20 meant.

21 JUDGE MCKONE: Except for the statement and the claim
22 limitation 1.1 that refers to the output of the main driver. Isn't it? We're
23 driving a load according to said data. That would be the output data.

24 MS. SHI: No. So, that's according to input data because the
25 output data is based on the input data.

26 JUDGE MCKONE: Okay. Your time has expired.

1 MS. SHI: Thank you.

2 JUDGE MCKONE: We appreciate your comments. And Patent
3 Owner, you have about six and a half minutes remaining in your time. And
4 you can begin whenever you'd like.

5 MR. MILKEY: Thank you, Your Honor. So, I'm sharing my
6 screen again, and this is Petitioner's slide 7, just picking up where they left
7 off. Again, as we've discussed, the preamble says an output buffer circuit
8 for outputting data. The data that's output is not input data. It's in the form
9 of an input pulse train. Again, any data that's output, it's going to be input to
10 something else, but it's data that's output.

11 Next, going to their slide 30, addressing the *TomTom* case. Here,
12 it's a very different situation than what's at issue here. In *TomTom*, the
13 Federal Circuit held the generating language here, the for generating and
14 updating data for use in, to be merely an intended purpose, but then the
15 structural aspect of a destination tracking system of at least one mobile unit
16 comprising, to be limiting.

17 In our case, we have an output buffer circuit for outputting data,
18 and there really can't be any realistic dispute that for outputting data has to
19 be limiting, because the data provides antecedent basis for said data in the
20 claims. So, what we're talking about is the structural aspect that follows that
21 for outputting data, that the data is in the form of an input pulse train at a
22 predetermined output impedance and slew rate. So, it's kind of the opposite
23 situation of *TomTom* in which *TomTom* held the for generating data aspect
24 of the claim to be non-limiting and the structural aspect to be limiting.

25 Here, there's really no real dispute, realistic dispute, that the for
26 outputting data has to be limiting. And so, the question is whether the more

1 structural aspects of the preamble are limiting. And again, we have
2 testimony and even the other side has acknowledged that output impedance
3 control is sort of a fundamental thing in design, and that's a very important
4 part of these systems.

5 A few other points that they raised in Exhibit 1006 at column 7,
6 lines 4 through 8 here. It talks about Itoh was describing output signal
7 VOUT that has gentle rising and falling edges corresponding to a
8 predetermined specification. This is talking about right rising and falling
9 edges. It's talking about this slew rate because we're talking about pulse
10 transitions here. We don't dispute that Itoh discloses a predetermined slew
11 rate, but it's the output impedance, which isn't disclosed to be predetermined
12 that we're contesting.

13 I also want to talk about their -- Petitioner's arguments that output
14 impedance and slew rate control and outputting an input pulse train at a
15 predetermined output impedance can't be the inventive aspect of the
16 invention. We don't think it's appropriate to just reduce the whole invention
17 to a single aspect or limitation. It's really what we've shown is that
18 Petitioner hasn't proposed any combination of prior art that would arrive at
19 both the preamble limitation, as well as the Claim 4 limitation. They have
20 certain grounds that I think Ground 1 for instance, we don't contest that they
21 satisfy the predetermined output impedance limitation in Ground 1, but by
22 the time they get to Claim 4 in their Ground 2 analysis, for example, they
23 have this aspect where they turn off -- they have to in their combination, and
24 by the way this is this isn't something that Itoh itself discloses. This is
25 something that they've proposed needs to be done in order to meet Claim 4.
26 They've proposed turning off the output impedance control during the signal

1 transitions in order to arrive at Claim 4's recitation of small effect on rise and
2 fall times of the output pulses. So, when they modify the prior art to arrive
3 at Claim 4 as they've proposed, they can no longer meet the predetermined
4 output impedance requirement of the Claim 1 preamble. So, that's really the
5 issue is this interplay between the preamble and Claim 4, and that's where
6 Petitioner fails in this regard.

7 I finally want to go to this Claim 4 issue of whether pulses output
8 from -- the pulses output, let me just get the exact language, have a small
9 effect on rise and fall times of pulses output from said main driver is
10 limiting. They've alleged in District Court that this is, and they said this on
11 the record, that they said that this is indefinite. And by the way, not because
12 of *IPXL*, but because small effect doesn't have a clear meaning. Of course,
13 if this didn't have patentable weight, there would be no invalidity problem
14 based on indefiniteness. So, the fact that they've alleged that the patent is
15 invalid in District Court, because this limitation is indefinite shows that they
16 think that it should be given patentable weight. And so, I don't know how
17 they can sit here and say that we don't have a position on whether this should
18 be given patentable weight when they're arguing that the patent is invalid by
19 virtue of including this limitation.

20 So anyway, in short, I don't think that there can be any real dispute
21 that this have a small effect on rise and fall times with pulses output from
22 said main driver should be considered in evaluating the patentable scope of
23 Claim 4.

24 I think that I responded to all of the, oh, I also just want to --

25 JUDGE MCKONE: Your time has expired.

26 MR. MILKEY: Okay. If there are any questions you happen to

1 have, otherwise, thank you.

2 JUDGE MCKONE: Please be short.

3 MR. MILKEY: Oh, yeah, just quickly responding to their
4 characterization of the deposition testimony. If you actually look at the
5 deposition testimony from Exhibit 2006 and Exhibit 1020, where they
6 alleged that that was talking about predetermined output impedance, none of
7 that testimony was specifically about the meaning of predetermined output
8 impedance or even I don't think predetermined at all, so.

9 But unless Your Honors have questions, I thank you for your time.

10 JUDGE MCKONE: We -- I have nothing further. Anyone else?

11 Nope. Okay. We are -- this has been very helpful. I understand your
12 positions better speaking for myself, and we appreciate your time.

13 We are adjourned right now.

14 (Whereupon the above-entitled matter went off the record at 2:51
15 p.m.)

IPR2023-01286
Patent RE43,539 E

P E T I T I O N E R :

D a v i d O ' D e l l
H o n g S h i
H A Y N E S A N D B O O N E , L L P
d a v i d . o d e l l . i p r @ h a y n e s b o o n e . c o m
h o n g . s h i . i p r @ h a y n e s b o o n e . c o m

P A T E N T O W N E R :

J a m e s M i l k e y
Q i T o n g
R U S S , A U G U S T , & K A B A T
j m i l k e y @ r a k l a w . c o m
p t o n g @ r a k l a w . c o m