

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE LICENSING LTD.,
Patent Owner.

IPR2023-01286
Patent RE43,539 E

Before RICHARD M. LEBOVITZ, DAVID C. McKONE, and
KEVIN C. TROCK, *Administrative Patent Judges*.

McKONE, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Challenged Claim Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–12 of U.S. Patent No. RE43,539 E (Ex. 1001, “the ’539 patent”). Longitude Licensing Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition (Paper 6,) and disclaimed claims 1–3 and 5–12 (Ex. 2002). Pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review of claim 4, the sole remaining challenged claim of the ’539 patent. Paper 9 (“Dec.”).

Patent Owner filed a Patent Owner’s Response to the Petition (Paper 20, “PO Resp.”), Petitioner filed a Reply to the Patent Owner’s Response (Paper 22, “Reply”), and Patent Owner filed a Sur-reply to the Reply (Paper 24, “Sur-reply”). An oral argument was held on November 21, 2024. Paper 31 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. Based on the record before us, we determine that Petitioner has demonstrated by a preponderance of the evidence that claim 4 is unpatentable. We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a).

II. BACKGROUND

A. *Related Proceedings*

The parties identify the following related federal district court cases: (1) *Longitude Licensing Ltd. v. ASUSTeK Computer Inc.*, Civil Action No. 8-23-cv-00033 (C.D. Cal.); (2) *Longitude Licensing Ltd. v. Lenovo Group Ltd.*, Civil Action No. 8-23-cv-0035 (C.D. Cal.); (3) *Longitude Licensing Ltd. v. Acer Inc.*, Civil Action No. 8-23-cv-0036 (C.D. Cal.); (4) *Longitude Licensing Ltd. v. HP Inc.*, Civil Action No. 8-23-cv-0038 (C.D. Cal.); (5) *Longitude Licensing Ltd. v. Amazon.com, Inc.*, Civil Action

No. 8-23-cv-0039 (C.D. Cal.); and (6) *Longitude Licensing Ltd. v. Dell Techs. Inc.*, Civil Action No. 8-22-cv-02312 (C.D. Cal.). Pet. 107–08; Paper 11, 2.

B. The '539 Patent (Ex. 1001)

The '539 patent describes an output buffer circuit for outputting data read from memory in a DRAM (Dynamic Random Access Memory) integrated semiconductor circuit device. Ex. 1001, 1:44–48, 5:12–13. According to the '539 patent, variations in the power supply voltage and ambient temperature cause variations in the cross-point between rising and falling waveforms of output pulses and in the slew rate of the output buffer. *Id.* at 2:54–60. This results in failure to correctly receive transmitted data, as well as output distortion and noise. *Id.* at 1:48–62. The '539 patent aims to compensate for the variations by simultaneously controlling the output impedance and slew rate of the output buffer circuit. *Id.* at 3:14–34, 8:59–63. The slew rate is controlled by changing the ratio of rise time to fall time (tr/tf) of the output pulse waveform. *Id.* at 1:41–43, 7:59.

Figure 3 of the '539 patent is reproduced below.

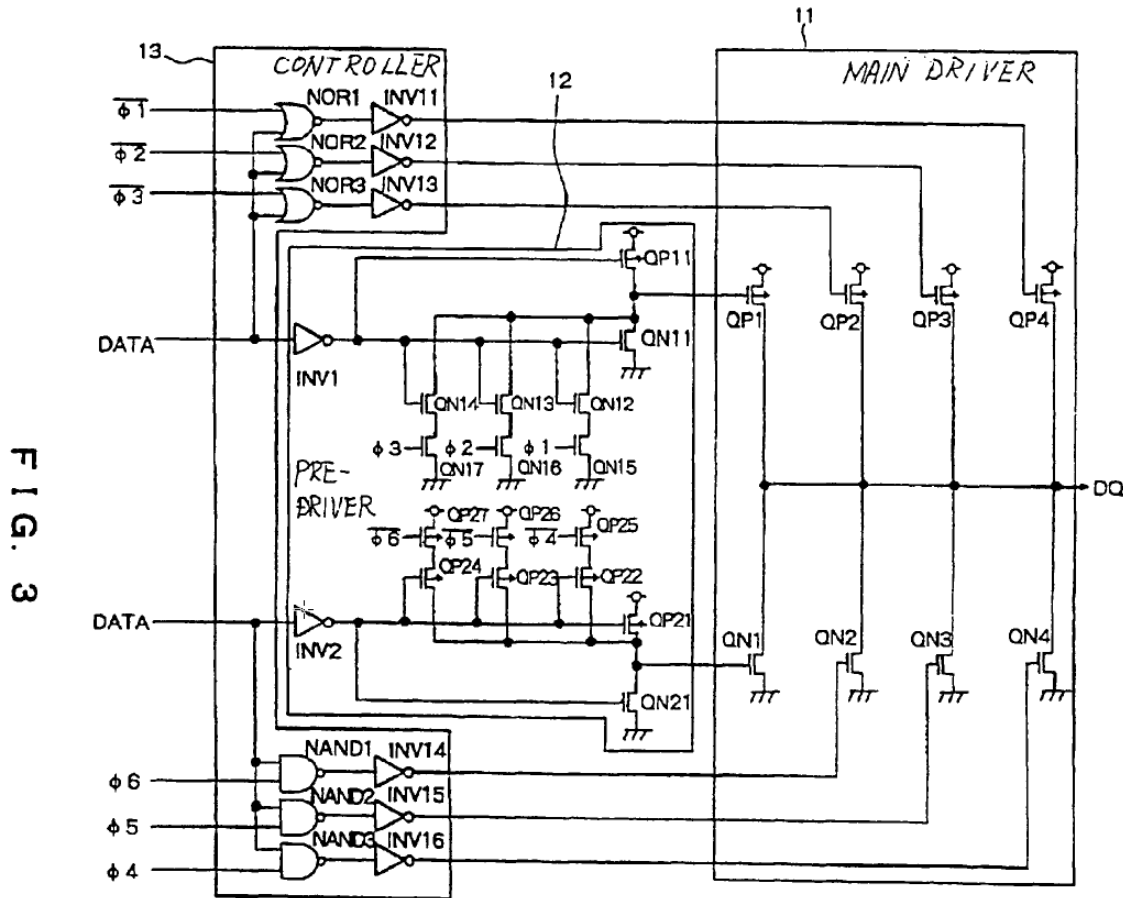


Figure 3 is a circuit diagram of an output buffer circuit disclosed in the '539 patent. *Id.* at 5:59–60. Main driver 11 with an adjustable output impedance drives a load connected to terminal DQ; predriver 12 drives main driver 11 and changes the ratio t_r/t_f of output pulses of main driver 11; and controller 13 generates signals to change the output impedance of main driver 11 and the ratio t_r/t_f of output pulses. *Id.* at 5:60–6:1.

Main driver 11 comprises p-channel MOS (pMOS) transistors QP1–QP4 and n-channel MOS (nMOS) transistors QN1–QN4. *Id.* at 6:13–16. pMOS transistors QP2–QP4, as well as pMOS transistor QP1, drive the load connected to terminal DQ to adjust the output impedance when high-level data is output from main driver 11.

Id. at 6:28–31. Specifically, pMOS transistors QP2–QP4 are turned on to lower the output impedance when high-level data is output. *Id.* at 7:47–51. The greater the number of pMOS transistors turned on, the smaller the output impedance. *Id.* at 7:51–53. nMOS transistors QN2–QN4 as well as nMOS transistor QN1 drive the load connected to terminal DQ to adjust the output impedance when low-level data is output from main driver 11. *Id.* at 6:31–34. Specifically, nMOS transistors QN2–QN4 are turned on to lower the output impedance when low-level data is output. *Id.* at 7:53–56. The greater the number of nMOS transistors turned on, the smaller the output impedance. *Id.* at 7:56–58.

Predriver 12 comprises pMOS transistor QP11 and nMOS transistor QN11 for driving pMOS transistor QP1 of main driver 11, nMOS transistors QN12–QN14 for adjusting the driving capability of nMOS transistor QN11, and nMOS transistors QN15–QN17 for turning on and off nMOS transistors QN12–QN14. *Id.* at 6:47–53. nMOS transistors QN12–QN14, as well as nMOS transistor QN11, drive pMOS transistor QP1 as a load to adjust the time for pMOS transistor QP1 to be turned on from an OFF state, i.e., the rise time t_r of an output pulse of main driver 11. *Id.* at 7:4–8. Specifically, nMOS transistors QN12–QN14 are turned on to shorten the rise time t_r upon switching from the low-level data to the high-level data. *Id.* at 7:59–63. The greater the number of nMOS transistors turned on, the shorter the rise time t_r . *Id.* at 7:63–65. Predriver 12 further comprises pMOS transistor QP21 and nMOS transistor QN21 for driving nMOS transistor QN1 of main driver 11, pMOS transistors QP22–24 for adjusting the driving capability of pMOS transistor QP21, and pMOS transistors QP25–QP27 for turning on and off pMOS transistors QP22–24. *Id.* at 6:53–58. pMOS transistors QP22–QP24 as well as pMOS transistor QP21 drive nMOS transistor QN1

as a load to adjust the time for nMOS transistor QN1 to be turned on from an OFF state, i.e., the fall time t_f of an output pulse of main driver 11.

Id. at 7:8–12. Specifically, pMOS transistors QP22–QP24 are turned on to shorten the fall time t_f upon switching from the high-level data to the low-level data. *Id.* at 7:65–8:1. The greater the number of pMOS transistors turned on, the shorter the fall time t_f . *Id.* at 8:1–3. In this way, the ratio t_r/t_f (slew rate) of output pulses is adjusted. *Id.* at 7:59.

Controller 13 is a logic circuit that generates signals for turning on and off pMOS transistors QP2–QP4 and nMOS transistors QN2–QN4 of main driver 11 and nMOS transistors QN15–QN17 and pMOS transistors QP25–QP27 of predriver 12. *Id.* at 7:19–26.

The '539 patent discloses that pMOS transistors QP2–QP4 and nMOS transistors QN2–QN4 comprise transistors “having a small device size (a narrow gate width) whose effect on the ratio t_r/t_f of output pulses is smaller than pMOS transistor QP1 and nMOS transistor QN1.” *Id.* at 6:36–40. According to the '539 patent, it is preferable to adjust the ratio t_r/t_f using only pMOS transistor QP1 and nMOS transistor QN1. *Id.* at 8:24–34.

Claim 4, and disclaimed independent claim 1 from which it depends (bracketed numbering added to track that used by Petitioner (Pet. 47–58))¹, are reproduced below.

1. [1.0] An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

[1.1] a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS

¹ Matter enclosed in heavy brackets, i.e., [], appears in the original patent but forms no part of the reissue specification, while matter in *italics* are additions to the specification made by the reissue. Ex. 1001, 1:7–10.

transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor;

[1.2.1] a predriver with outputs for driving only said first [in-channel] *in channel* MOS transistor and only said first p-channel MOS transistor [1.2.2] having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and [1.2.3] at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor; and

[1.3] a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor,

[1.4] wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.

4. The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and

said first n-channel MOS transistor, and have a small effect on rise and fall times of pulses output from said main driver.

C. Evidence

In challenging claim 4, Petitioner relies on the references listed below.

Reference		Date	Exhibit No.
Itoh	US 6,924,669 B2	Aug. 2, 2005	1006
Muljono	US 6,288,563 B1	Sept. 11, 2001	1010

Petitioner also relies on the Declaration of Scott E. Thompson, Ph.D. (Ex. 1003).

Patent Owner relies on the Declaration of Bruce Jacob, Ph.D. (Ex. 2005).

D. The Instituted Grounds of Unpatentability

Claim Challenged ²	35 U.S.C. §	References
4	103(a) ³	Itoh
4	103(a)	Itoh, Muljono

² The Petition also challenged claims 1–3 and 5–12 over various grounds involving Itoh, Skorup (US 3,943,551; Ex. 1007), and Borkar (US 4,975,598; Ex. 1008). Pet. 4–5. Because claims 1–3 and 5–12 were disclaimed, we did not institute trial on these additional grounds.

³ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Because the ’539 patent was filed before March 16, 2013, the effective date of the relevant amendment, the pre-AIA version of § 103 applies.

III. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner, relying on the testimony of Dr. Thompson, contends that a person of ordinary skill in the art “would have a bachelor’s or the equivalent degree in electrical or computer engineering or a related field, and 2–3 years of professional experience relating to integrated circuit design.” Pet. 3 (citing Ex. 1003 ¶ 13). Petitioner further contends that “a person with less formal education but more experience, or more formal education but less experience, could have also met the relevant standard for [a person of ordinary skill in the art].” *Id.* Petitioner states that it “does not imply that a person having an extraordinary level of skill should be regarded as [a person of ordinary skill in the art].” *Id.* at 3–4.

Patent Owner does not challenge Petitioner’s contentions or propose a level of ordinary skill in the art. PO Resp. 9.

On the complete record, we adopt Petitioner’s description of the level of ordinary skill in the art, as it is uncontested and is consistent with the technology described in the ’539 patent and the asserted prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. Claim Construction

We construe claims “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b); *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

To distinguish the prior art, Patent Owner seeks to show that “at a predetermined output impedance” from claim 1’s preamble is limiting and that the output impedance is maintained at a single predetermined value for the duration of a pulse train. PO Resp. 19 (“Of course, an output buffer circuit designed to output a pulse train at two different impedance values (which impedances are toggled during every output pulse transition) does not meet the plain meaning of an output buffer circuit ‘for outputting data in the form of an input pulse train at a predetermined output impedance.’”).

1. Whether “at a predetermined output impedance” in the Preamble of Claim 1 is Limiting

The preamble of disclaimed independent claim 1, from which claim 4 depends, recites “[a]n output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate.” Because Patent Owner contends that the asserted prior art fails to teach outputting data “at a predetermined output impedance” as recited in the preamble (PO Resp. 16), we first determine whether the term “at a predetermined output impedance” is limiting. “In general, a preamble limits the invention if it recites essential structure or steps, or if it is ‘necessary to give life, meaning, and vitality’ to the claim.” *Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (citation omitted). “Further, when reciting additional structure or steps underscored as important by the specification, the preamble may operate as a claim limitation.” *Id.* “Conversely, a preamble is not limiting ‘where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.’” *Id.* (citation omitted).

Patent Owner contends that the entire preamble of claim 1 is limiting, including “at a predetermined output impedance.” PO Resp. 10–15; Sur-reply 3–15. First, Patent Owner contends that the preamble must be limiting because the preamble phrase “for outputting data” provides antecedent basis for “said data” recited throughout the body of claim 1. PO Resp. 11–12; Sur-reply 4–6 (citing Ex. 2005 ¶ 83; *In re Fought*, 941 F.3d 1175, 1178 (Fed. Cir. 2019) (“We have repeatedly held a preamble limiting when it serves as antecedent basis for a term appearing in the body of a claim.”)). Petitioner contends that the recitation of “said data” does not convert the *entire* preamble into a limitation, and that “the phrase ‘at a predetermined output impedance’ cannot be converted into a new claim limitation based on an antecedent basis rationale related to another phrase.” Pet. Reply 9 (citing *TomTom, Inc. v. Adolph*, 790 F.3d 1315, 1323–24 (Fed. Cir. 2015)).

The body of claim 1 provides three instances referring to “said data”: “a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to *said data*” in claim limitation [1.1]; and “having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to *said data*, [and] at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to *said data*” in claim limitation [1.2.2]. Patent Owner argues that the preamble “provides structural guidelines regarding the data the system is designed to output.” Sur-reply 14. However, this is not consistent with how “said data” is used in the body of claim 1.

The first instance of “said data” in the body of claim 1, “driving a load according to said data,” does not clearly specify that “said data” refers to the

output of the claimed output buffer circuit. Rather, it can be read as referring to the main driver, “data in the form of an input pulse train,” as recited in the preamble, where the form of the input data (i.e., a train of logical “1s” and “0s”) is used to determine what the output signal looks like (i.e., a train of logical “1s” and “0s” that tracks the input pulse train). The second and third instances of “said data” make clear that this phrase finds antecedent basis in the “data in the form of an input pulse train,” as the first n- and p-channel MOS transistors are driven (their input) according to those data and, accordingly, are not outputting those data.

In *TomTom*, the Federal Circuit held that it was erroneous to construe the entire preamble of a claim as a limitation based on one phrase in the preamble providing antecedent basis for later-recited terms. 790 F.3d at 1323–24 (“It was therefore error for the district court to use an antecedent basis rationale to justify converting this independent part of the preamble into a new claim limitation.”). We agree with Petitioner that, even if the preamble were limiting by virtue of providing antecedent basis for “said data,” the recitation of “said data” in the claim body refers to the form of the input pulse train (“data in the form of an input pulse train”) and does not implicate the portion of the preamble reciting “at a predetermined output impedance.” In other words, “at a predetermined output impedance” is not necessary to understand the instances of “said data” in the body of the claim, which all refer to the form of the data input to the buffer circuit. Thus, simply invoking antecedent basis is not sufficient to show that “at a predetermined output impedance” is limiting.

Patent Owner further contends that claim 1’s preamble is limiting because it “provides necessary context to understanding the claim term ‘pulses output from said main driver’ as recited by claim 4.” PO Resp. 12

(citing Ex. 2005 ¶¶ 83–84). Claim 4 recites that the claimed transistors “have a small effect on rise and fall times of pulses output from said main driver.” Specifically, Patent Owner contends that without context from the preamble, claim 4 improperly introduces a method step of outputting pulses into the apparatus claim. *Id.*; Sur-reply 4, 8–9 (citing *IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005)); Tr. 27:20–23; 30:4–8. Accordingly, Patent Owner argues, “claim 4 cannot literally mean that there must be ‘pulses output from said main driver,’ because requiring the outputting of pulses would improperly introduce a method step in an apparatus claim.” Sur-reply 8. Instead, Patent Owner continues, “the ‘pulses output from said main driver’ referenced in claim 4 are pulses of the ‘input pulse train at a predetermined output impedance and slew rate’ [of claim 1’s preamble] that the output buffer circuit is designed to output (but need not **actually** output because the claim is an apparatus claim rather than a method claim).” *Id.* at 9. Patent Owner’s expert, Dr. Jacob, opines that “[w]ithout the preamble, Claim 4’s requirement of output needs further clarification” and that, in order to understand the “small effect on rise and fall times of pulses output from said main driver” in claim 4, “a person of ordinary skill would require Claim 1’s preamble and its description of a ‘predetermined . . . slew rate’ for explanation.” Ex. 2005 ¶ 84.

Patent Owner’s arguments at the oral hearing illustrate the difficulty of its position. For example, Patent Owner argued

Your Honor, to be clear, we don’t contend that the preamble requires that the circuit actually output data at all. You can create the circuit. The circuit can be configured to operate in a certain way. And I can never turn it on and it will infringe because I’ve created the circuit for outputting data. That’s the configuration of the circuit. That’s its intended use. It’s capable of operating in this way. But what I think is clear about

the preamble is that it requires that the circuit be for outputting data. But under *IPXL* and similar cases, intended purpose of system claims is an appropriate thing. That doesn't run afoul of *IPXL* unless the system actually be required to operate in a certain way. And here we're just saying that the intended purpose of the circuit, the intended use of the circuit has to be to do this. That's the distinction.

Tr. 30:13–24; *see also id.* at 27:10–25 (“I think that it is clear that the claim recites that the intended use of this and the intended configuration of the circuit is to output data in the form of an input pulse train. However, this definitely is a system claim. It's a claim for an output buffer circuit comprising things. . . . However, Claim 4 recites that these transistors have a small effect times of pulses output from said main driver. Without the preamble, Your Honor, the Claim 4 recitation of pulses output from said main driver would imply that pulses actually need to be output from said main driver. And that, of course, is not permissible in a system claim. You can't require that the system claim be used for something consistent with the, you know, that it actually be used for something consistent with certain case law.”).

Patent Owner's arguments are unclear and possibly inconsistent. If, as Patent Owner states, “outputting data in the form of an input pulse train at a predetermined output impedance and slew rate” is a recitation of an “intended use” or “intended purpose” of the output buffer circuit of claim 1, the preamble is not limiting. *See Catalina Mktg.*, 289 F.3d at 808. This part of Patent Owner's argument appears to be an admission that the preamble is not limiting.

However, Patent Owner might have intended to argue that the preamble language somehow modifies or configures the structure recited in the body of claim 1 (and claim 4) such that the structure produces a result

recited in the preamble. *See* Tr. 34:20–35:16 (“I think that this is what we’re talking about is the configuration of the system”). If that is the case, we agree with Petitioner that “the claim body [of claim 1] describes a structurally complete invention, and the preamble refers to ‘at a predetermined output impedance’ only as a purpose or intended use.” Pet. Reply 3 (citing *TomTom*, 790 F.3d at 1324). Specifically, we agree with Petitioner that claim 1 recites in structural detail a main driver, predriver, controller, and their relationships. *Id.* at 4–5. Both claims 1 and 4 recite this structure at the detail of individual transistors. Patent Owner does not explain how the preamble language affects the structure of these system claims. We agree with Petitioner that “at a predetermined output impedance” merely provides that the intended use of the circuit structure in the body of claim 1 (claimed in detail as an arrangement of transistors) is outputting data in the form of an input pulse train at a predetermined output impedance and slew rate. It does not alter or add to the structure of the recited main driver, predriver, and controller.

Similarly, Patent Owner’s argument that the preamble is necessary to understand claim 4’s “pulses output from said main driver” (PO Resp. 12) is not persuasive, as claim 4 does not recite anything that implicates output impedance. Rather, claim 4 recites that certain transistors have a small effect on rise and fall times of pulses output from said main driver. We do not read this language as a method step improperly inserted into a device claim. Rather, like the language in the preamble of claim 1, this functional language in claim 4 specifies an intended use or intended result of the structure, should that structure receive a certain input. Treating the preamble of claim 1 as non-limiting does not somehow transform this language into an impermissible method step.

Patent Owner further contends that the preamble is limiting because “a fundamental aspect of the invention is to provide an output in the form of a pulse train according to predetermined impedance and slew rate characteristics.” PO Resp. 13–14 (citing Ex. 1001, 2:54–60, 3:14–3:34, 4:18–22; Ex. 2005 ¶¶ 72–78, 85–87, 105–107; *Vizio, Inc. v. Int’l Trade Comm’n*, 605 F.3d 1330, 1341 (Fed. Cir. 2010)); Sur-reply 10–11. Patent Owner argues that “each embodiment of the ’539 Patent is consistent with the goal of providing data in the form of a pulse train at a predetermined slew rate and output impedance.” PO Resp. 14 (citing Ex. 2005 ¶¶ 72–78, 85–87, 105–107). Patent Owner’s citations to the specification do not refer to providing output at a predetermined slew rate and output impedance. Rather, output impedance and slew rate are “controlled” and “adjust[ed].” Ex. 1001, 2:54–60, 3:14–3:34, 4:18–22. In any case, Patent Owner points us to no description that purports to limit the claims to outputting data in the form of an input pulse train at a predetermined slew rate and output impedance.

Patent Owner contends that claims 13 and 15 recite the same language as claim 1’s preamble in the body of the claims, and that we should construe the preamble language of claim 1 in the same manner as we would in claims 13 and 15. Sur-reply. 13; *see* Tr. 30:25–31:14. Petitioner, however, has not challenged claims 13 and 15 and neither party has proposed construing that language (“an output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate”) in either claim 13 or 15. For example, Patent Owner has not shown that this language in claims 13 and 15 is more than an intended use. Thus, Patent Owner’s argument is not persuasive.

For the above reasons, we find the phrase “a predetermined output impedance” in the preamble to be non-limiting.

2. Whether “a predetermined output impedance” Means Only a Single Predetermined Output Impedance

Patent Owner contends that a skilled artisan “would understand that the preamble of claim 1 could only be satisfied by a pulse train being output at a single predetermined output impedance, rather than the pulse train being output by rapidly switching between two different output impedances.” PO Resp. 20; *see also* Sur-reply 20–21 (citing Ex. 2005 ¶ 105). Patent Owner further clarifies its position, arguing that “[a] ‘pulse train’ is simply a train of multiple pulses, so a system designed to output (for example) data in the form of three consecutive pulses at a predetermined output impedance could satisfy the claim requirement, even if a different predetermined output impedance were used for a subsequent pulse train.” Sur-reply 21. In support, Dr. Jacob opines that the ’539 patent “adjusts output impedance only once per recalibration (e.g., once at system startup) and does so to set the drive strength of the output buffer” and that “it would have been clear to a person of ordinary skill that [the ’539 patent]’s output buffer was intended to have the same output impedance over an entire output pulse train.” Ex. 2005 ¶¶ 103, 105; *see also id.* ¶ 110 (Dr. Jacob testifying that Itoh “does not output the data at a predetermined output impedance but instead outputs the data at *two different* output impedance values every time it is operated”).

Petitioner contends that “a predetermined output impedance” is not limited to only a single output impedance, but rather covers one or more predetermined output impedances. Pet. Reply 21 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000) (“This court

has repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’”)). “Predetermine” simply means “to determine beforehand.” Predetermine, MERRIAM-WEBSTER DICTIONARY, available at <https://www.merriam-webster.com/dictionary/predetermine>. As Petitioner observes, we typically understand “a” to mean “one or more.” *See KCJ*, 223 F.3d at 1356. Thus, the ordinary meaning of “a predetermined output impedance” is one or more output impedances determined in advance. Patent Owner does not point to any claim language to support its argument that a predetermined output impedance is limited to a single output impedance. As explained in more detail below, the specification does not redefine “a predetermined output impedance” to mean a single output impedance or exclude or disavow multiple output impedances from among those that can be determined in advance.

Patent Owner argues that a skilled artisan “would have understood from the teachings of the ’539 patent that impedance characteristics and slew rate characteristics would be controlled on far longer timescales than on a pulse-by-pulse basis.” Sur-reply 10–11 (citing Ex. 2005 ¶¶ 54, 105). Patent Owner does not cite to the specification, so it is unclear what disclosure of the ’539 patent would support this argument. We have considered Dr. Jacob’s testimony (Ex. 2005 ¶¶ 54, 105), but Dr. Jacob does not identify an objective basis for his testimony (or cite to the ’539 patent), rendering that testimony of little probative value. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”). Patent Owner argues that “Dr. Jacob opined that it would ‘have been clear to a person of ordinary

skill that the output impedance of [the '539 patent's] output buffer would have remained the same over a given pulse train.” Sur-reply 12 (quoting Ex. 2005 ¶ 78 (brackets by Patent Owner)). Once again, Dr. Jacob does not identify an objective basis for his testimony or cite to the '539 patent.

Patent Owner argues that “the claim requirement can be satisfied, for example, by a system that is designed to suppress variations in a predetermined output impedance throughout the entirety of a given input pulse train.” Sur-reply 15 (citing Ex. 1001, 1:30–35). Here, the '539 patent states that it is important to suppress variations in the driving capability and slew rate of the output buffer circuit. Ex. 1001, 1:30–35. However, it does not discuss output impedance or whether output impedance must be maintained at a constant value throughout a pulse train. In providing an overview of the '539 patent, Patent Owner identifies several passages in the specification that describe controlling, adjusting, and changing output impedance values. PO Resp. 3–8 (citing Ex. 1001, 2:18–20, 3:14–19, 3:24–30, 5:51–54, 5:65–6:1, 6:28–40, Fig. 3; Ex. 2005 ¶¶ 60–71). However, the '539 patent's description of controlling, adjusting, and changing an output impedance does not support limiting “predetermined output impedance” to a single constant value maintained for an entire pulse train. Dr. Jacob's supporting testimony (Ex. 2005 ¶¶ 60–71) is entitled to little weight as it does little more than quote the above passages and repeat Patent Owner's arguments.

In Patent Owner's argument that the preamble of claim 1 reflects a fundamental aspect of the invention, Patent Owner cites several passages of the '539 patent and argues that “as explained by Dr. Jacob, each embodiment of the '539 Patent is consistent with the goal of providing data in the form of a pulse train at a predetermined slew rate and output

impedance.” PO Resp. 13–14 (citing Ex. 1001, 2:54–60, 3:14–34, 4:18–22; Ex. 2005 ¶¶ 72–78, 85–87, 105–107). At most, these passages describe monitoring, controlling, and adjusting the output impedance, and do not describe a single output impedance for a pulse train. To the extent that these passages bear on the meaning of “a predetermined output impedance” (a phrase the passages do not use), they do not support limiting “a predetermined output impedance” to a single constant value maintained for a pulse train.

Petitioner contends that the specification counsels against limiting “predetermined output impedance” to a single output impedance. Reply 21–22. According to Petitioner, “[t]he specification of the ’539 Patent does not mention or describe how to achieve ‘a pulse train being output at a *single* predetermined output impedance.’” *Id.* at 5. Petitioner contends that the ’539 patent’s goal of achieving a cross-point CP and slew rate “compensation within an allowable range of variations of the system,” where “the slew rate depend[s] on variations of both the output impedance and the power supply voltage,” indicates an allowable range of variations of the output impedance. Ex. 1001, 1:63–2:5 (quoted at Pet. Reply 21–22).

Petitioner additionally points out that

[Patent Owner’s] “only . . . a single” requirement is also contrary to ’539 Patent’s description of slew rate having a range of variations, as the preamble recites “*a* predetermined output impedance and *slew rate*.” *See, e.g.,* ’539 Patent, 9:6–9:9, FIG. 6 (illustrating the asserted goal for reducing “*the range of variations* of the slew rate,” instead of keeping the slew rate at only a single value).

Pet. Reply 22 n.2.

Acknowledging that “there may be undesired variations in output impedance” (Sur-reply 12; *see* Pet. Reply 23–28 (discussing inevitable

variations in output impedance during MOSFET transition periods)), Patent Owner contends that claim 4 should be interpreted to “require[] a design *intended* to output at least one full ‘pulse train’ at a given output impedance (rather than intentionally varying the output impedance of the pulse train . . .).” Sur-reply 21 (emphasis added); *see* Tr. 31:26–33:25. According to Patent Owner, “the claim requirement can be satisfied, for example, by a system that is designed to suppress variations in a predetermined output impedance throughout the entirety of a given input pulse train.” Sur-reply 15 (citing Ex. 1001, 1:30–35).

As explained above, the ordinary meaning of “a predetermined output impedance” is one or more output impedances determined in advance. We have considered the intrinsic evidence cited by the parties and the extrinsic evidence in the form of expert testimony opining on the intrinsic evidence. We find no support in the way of lexicography or exclusion in Patent Owner’s citations to the ’539 patent’s description of controlling, adjusting, and changing output impedances. That description is equally consistent with controlling, adjusting, and changing an output impedance to be one or more output impedance values determined in advance. Petitioner’s citations to the specification further support the notion that the invention contemplates an output impedance that can vary, albeit in a manner determined in advance by the output buffer’s configuration.

Accordingly, on the complete record, we conclude that “a predetermined output impedance” in the preamble phrase “outputting data in the form of an input pulse train at a predetermined output impedance” is not limited to a single predetermined output impedance, but rather “a

predetermined output impedance” can be one or more output impedances determined in advance.

3. *“a smaller device size with a smaller gate width”*⁴

Claim 4 recites that “said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor.” In the Institution Decision, we preliminarily construed “smaller device size” and “smaller gate width” to be synonymous, rather than two separate requirements. Dec. 11–13.

Patent Owner

acknowledges the understanding set forth in the Board’s Institution Decision, and accepts that the proper comparison is between the combined device size of the P2, N2 pair with the device size of the combined device size of the P1, N1 pair. In other words, if the device size of P2 is less than the device size of P1, and the device size of N2 is less than the device size of N1, then the size requirements of claim 4 are satisfied.

PO Resp. 16. Thus, it appears that Patent Owner does not contest our construction or propose an alternative.

On the complete record, and for the reasons set forth in our Institution Decision, we maintain our construction of “smaller device size” and “smaller gate width” as synonymous.

⁴ Patent Owner presented arguments as to this claim construction in the Preliminary Response (at 9–11), which we found unpersuasive in the Decision to Institute (at 12–13). Patent Owner does not advance those arguments in the Patent Owner Response. Accordingly, those arguments are waived. Paper 10 (Scheduling Order), 9 (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.”).

4. *Remaining Claim Terms*

Based on the record before us, we do not find it necessary to provide express claim constructions of any other terms. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

C. *Obviousness Over Itoh*

Petitioner contends that claim 4 would have been obvious over Itoh. Pet. 42–58, 60–63. For the reasons explained below, Petitioner has made a sufficient showing.

A claim is unpatentable under 35 U.S.C. § 103 “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” We resolve the question of obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.⁵ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

⁵ The complete record does not include allegations or evidence of objective indicia of nonobviousness.

1. Overview of Itoh (Ex. 1006)

Itoh relates to “an output buffer circuit that outputs an output signal having gentle rising and falling edges and a slew-rate control type output buffer circuit.” Ex. 1006, 1:6–9. Itoh discloses several embodiments of an output buffer circuit (*see id.* at 6:25–52), the second of which is shown in Figure 8, reproduced below.

Fig.8

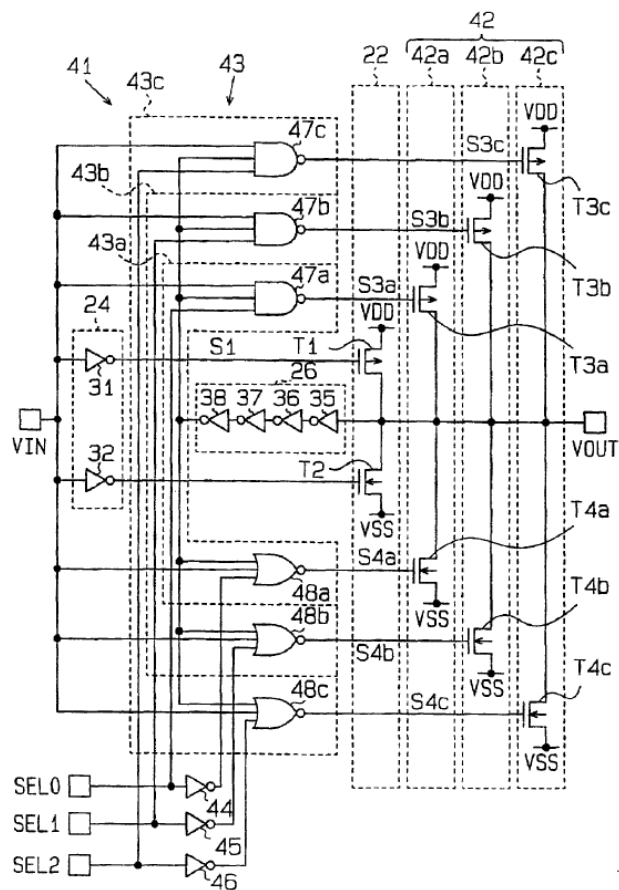


Figure 8 of Itoh is a circuit diagram of output buffer circuit 41 having an adjustable output impedance. *Id.* at 10:1–4. Output buffer circuit 41 includes first drive circuit 22; second drive circuit 42; control circuits 24, 43; delay circuit 26; and inverter circuits 44–46. *Id.* at 10:4–7. Referring to the description of the drive circuit 22 corresponding to Figure 5 (not shown),

first drive circuit 22 generates external output signal VOUT that has gentle rising and falling edges corresponding to a predetermined specification.

Id. at 7:4–6. Returning to Figure 8, second drive circuit 42 includes a plurality of sub-drive circuits 42a–42c, which have different impedances.

Id. at 10:38–40. The output impedance of output buffer circuit 41 is determined by enabling at least one sub-drive circuit 42a–42c via control circuit 43, in accordance with select signals SEL0–SEL2. *Id.* at 10:16–43.

Itoh's fourth embodiment is shown in Figure 10, reproduced below.

Fig.10

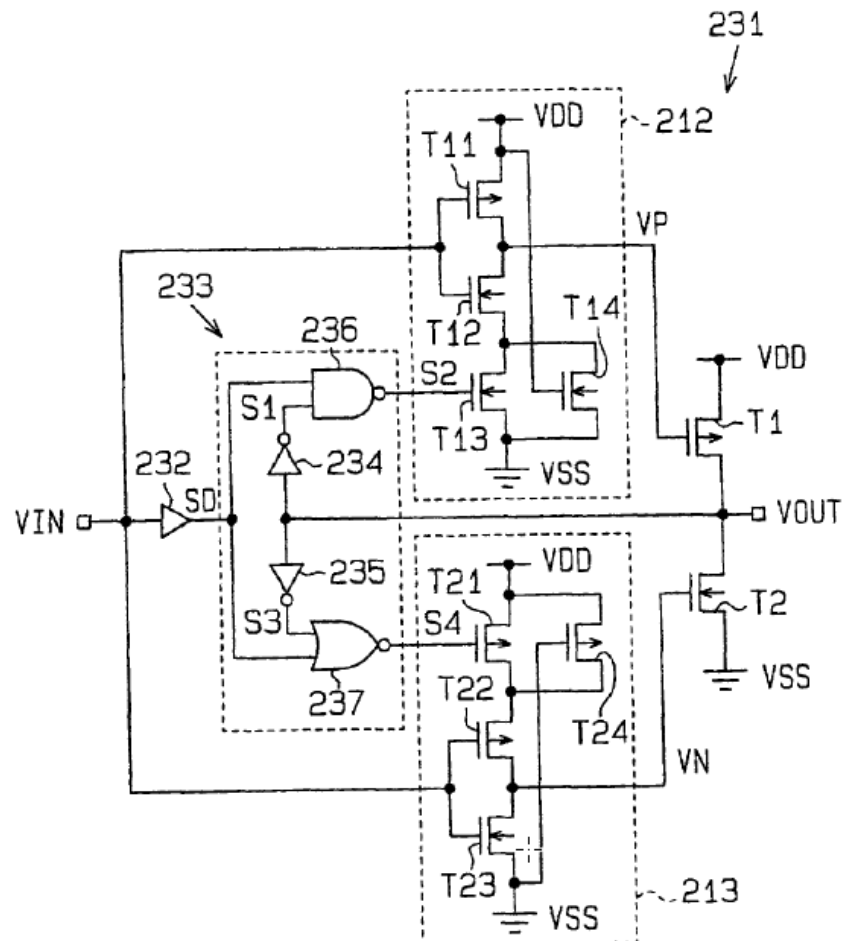


Figure 10 of Itoh is a circuit diagram of slew-rate control type output buffer circuit 231. *Id.* at 11:11–12. Output buffer circuit 231 includes output

transistors T1, T2; slew-rate control circuits 212, 213; delay circuit 232; and signal generator 233. *Id.* at 11:13–20. The ON/OFF of nMOS transistor T13 in slew-rate control circuit 212 determines the falling waveform of control signal VP driving output transistor T1, i.e., the rising waveform of external output signal VOUT. *Id.* at 11:58–60. The ON/OFF of pMOS transistor T21 determines the rising waveform of control signal VN driving output transistor T2, i.e., the falling waveform of external output signal VOUT. *Id.* at 12:34–36.

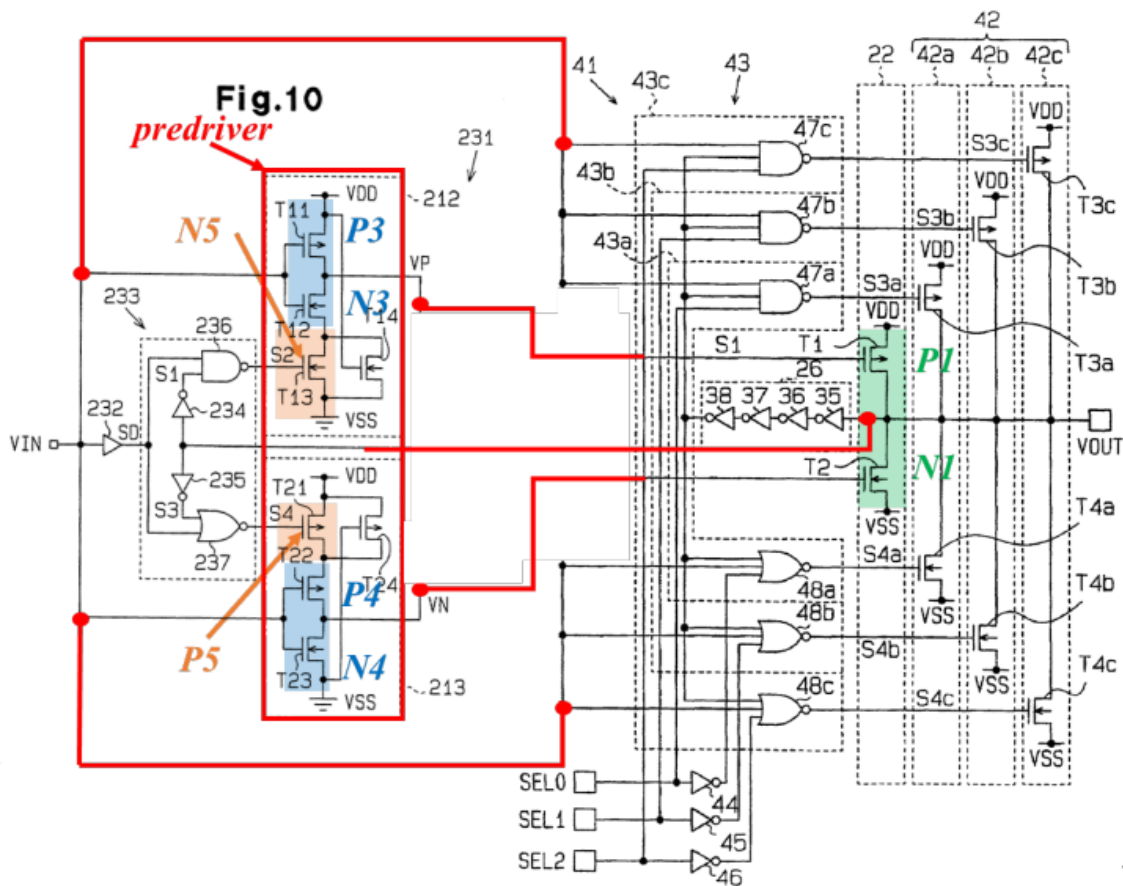
2. Petitioner’s Combination of Itoh Embodiments

According to Petitioner, Figure 8 of Itoh falls under a first group of embodiments (dubbed “Category 1” by Petitioner) relating to a “first method of slew rate control and additional pair(s) of output transistors for output impedance control,” and Figure 10 of Itoh falls under a second group of embodiments (“Category 2”) relating to a “second method of slew rate control and no additional pair(s) of output transistors for output impedance control.” Pet. 8–9 (bolding and italics omitted). Petitioner contends

A [person of ordinary skill in the art] would have been motivated to combine an embodiment from [Category] 1 and another from Category 2 to achieve the obvious, beneficial, and predictable results of an output buffer circuit having improved slew rate control (e.g., by using the slew-rate control type circuit taught by Category 2) and improved impedance control (e.g., by using the additional pair(s) of output transistors for output impedance control taught by Category 1).

Id. at 43 (citing Ex. 1003 ¶¶ 170–177). Specifically, Petitioner combines Figures 8 and 10 of Itoh to produce the figure below.

Fig.8



Example 2.1

The figure above is an annotated circuit diagram provided by Petitioner to illustrate Petitioner's combination of the circuit diagrams of Figures 8 and 10 of Itoh (dubbed "Example 2.1" by Petitioner). *Id.* at 53; *see also id.* at 43–46 (explaining how Figures 8 and 10 are merged); Ex. 1003 ¶¶ 170–177. Specifically, Petitioner proposes using the slew-rate control circuitry shown in Figure 10, rather than control circuit 24, to drive the pair of output transistors T1 and T2 of Figure 8, and also using the control 43 and output impedance 42 circuitry of Figure 8. Pet. 44–45. Petitioner contends:

It would have been obvious to apply FIG. 10's slew-rate control type circuit for driving the pair of output transistors T1

and T2 . . . to drive the same pair of output transistors T1 and T2 (also annotated as P1 and N1) in FIG. 8. Example 2.1 achieves improved output impedance control (provided by circuit 42 of FIG. 8 with the selectable pairs of output transistors) and improved slew rate control (provided by the slew-rate control type circuit of FIG. 10), with various advantages of FIG. 10 including reduced current consumption, a wide frequency band, and reduced noise. EX1006, 14:19–62.

. . . [C]ombining Embodiments of Itoh would have been no more than the combination of known elements (well-known components of an output driver) according to known methods (performing basic [integrated circuit (IC)] design).

Id. at 44–45.

Petitioner supports its proposed combination with the testimony of Dr. Thompson. Ex. 1003 ¶¶ 170–177. On the complete record, we credit this testimony.

Patent Owner does not contest Petitioner’s argument that a skilled artisan would have had reasons to combine the features of the Figure 8 and Figure 10 embodiments of Itoh. On the complete record, we find that Petitioner’s reasons to combine the features of Figures 8 and 10 have rational underpinning.

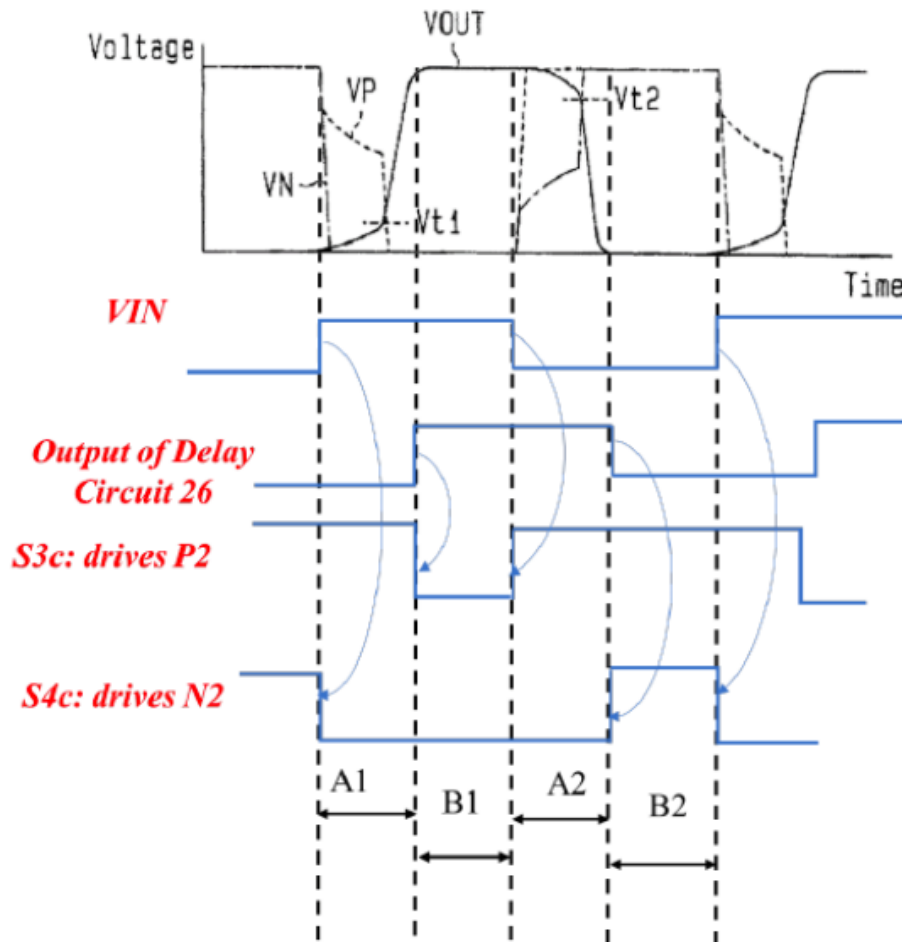
3. Preamble of Claim 1

The parties’ disputes as to claim 4 are focused on the preamble of independent claim 1 (limitation [1.0]), from which challenged claim 4 depends. The preamble of claim 1 recites “[a]n output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate.”

Petitioner contends that its modified version of Itoh (Example 2.1, “modified Itoh”) teaches the preamble to the extent that it is limiting.

Pet. 47 (citing Ex. 1003 ¶¶ 178–181); *see also id.* at 13 (citing Ex. 1003 ¶¶ 79–82). As noted above, Petitioner did not assert a combination of Itoh and Skorup as to claim 4, the only claim remaining in the ’539 patent. Nevertheless, Petitioner’s citations to Itoh in that ground based on the combination of Itoh and Skorup refer to Itoh alone and are relevant to Petitioner’s allegations as to underlying claim 1 in its challenge based on Itoh alone, and we refer to those citations here. Specifically, Petitioner contends that modified Itoh teaches “an output buffer circuit that receives data (VIN) in the form of an input pulse train and then drives a corresponding output signal VOUT,” with output impedance control and slew rate control. *Id.* at 13 (citing Ex. 1006, 3:15–17, 8:2–5, Figs. 3, 6); *see also id.* at 47.

Patent Owner contends that modified Itoh fails to teach that the data are output from the buffer circuit “at a predetermined output impedance.” PO Resp. 16. Specifically, Patent Owner contends that modified Itoh “would constantly adjust output impedance *within* a given pulse train output by the system” (*id.* at 16) rather than outputting the pulse train “at a *single* predetermined output impedance” (*id.* at 20) (emphasis added). Patent Owner (PO Resp. 17) refers to Petitioner’s annotated waveform diagram (Pet. 50) reproduced below:



Waveforms of Example 2.1

The above figure is a waveform diagram created by Petitioner that illustrates how modified Itoh's second pMOS/nMOS transistor pair T3c, T4c (annotated by Petitioner as P2, N2 in the figure above) drives the load at output VOUT in coaction with the first pMOS/nMOS transistor pair T1, T2 (annotated by Petitioner as P1, N1 in the "Example 2.1" figure further above).⁶ Pet. 49. Patent Owner contends:

⁶ We address these transistor pairs in more detail in our discussion of the claim body limitations below.

In [modified Itoh], the transistors P2 and N2 are turned off entirely during periods A1 and A2. During these periods, P2 and N2 do not provide output impedance control. Only during periods B1 and B2 are P2 and N2 “turned on for output impedance control.” *See* Pet. 49–50 (“P2 and N2 are turned off during periods A2 and A1 During B1 and B2 when VOUT is substantially stable, P2 and N2 are turned on for output impedance control.”).

PO Resp. 17–18. According to Patent Owner, both Patent Owner’s expert, Dr. Jacob, and Petitioner’s expert, Dr. Thompson, indicate that modified Itoh intentionally changes the output impedance over the course of each pulse transition. *Id.* at 18–19 (citing Ex. 2005 at ¶¶ 107–110 (Dr. Jacob testifying that “Itoh outputs each and every data pulse at two different output impedance values”); Ex. 2006, 16:8–20, 27:13–18 (Dr. Thompson testifying that the system “alters the impedance during B1 and B2, and it has a negligible effect, no effect during A1 and A2”)). Patent Owner contends that this is to be contrasted with the ’539 patent’s “design[] to provide an ‘input pulse train’ (i.e., a train of a plurality of pulses) that maintains a constant output impedance.” Sur-reply 12–13; *see also id.* at 15–16.

As discussed in the Claim Construction section above, the phrase “at a predetermined output impedance” in the preamble is non-limiting. For that reason alone, Patent Owner’s contention that modified Itoh does not teach “at a predetermined output impedance” is not persuasive.

Even if “at a predetermined output impedance” is limiting, however, we agree with Petitioner that modified Itoh teaches it. As discussed in the Claim Construction section above, we construe “a predetermined output impedance” to mean one or more output impedances determined in advance. In the above waveform diagram, modified Itoh’s output buffer controls the output impedance, in a manner determined in advance by the configuration

of the output buffer, during periods B1 and B2, when VOUT is at a high level or at a low level. *See* Ex. 1006, 10:37–43 (“In accordance with the select signals SEL0 to SEL2, at least one of the sub-drive circuits 42a–42c is enabled to *select the output impedance* when the output signal VOUT is in a static state.”)(emphasis added). The parties do not dispute this. *See* PO Resp. 17–18; Pet. 49–50; Pet. Reply 15. Thus, we find that modified Itoh teaches outputting data “at a predetermined output impedance.”

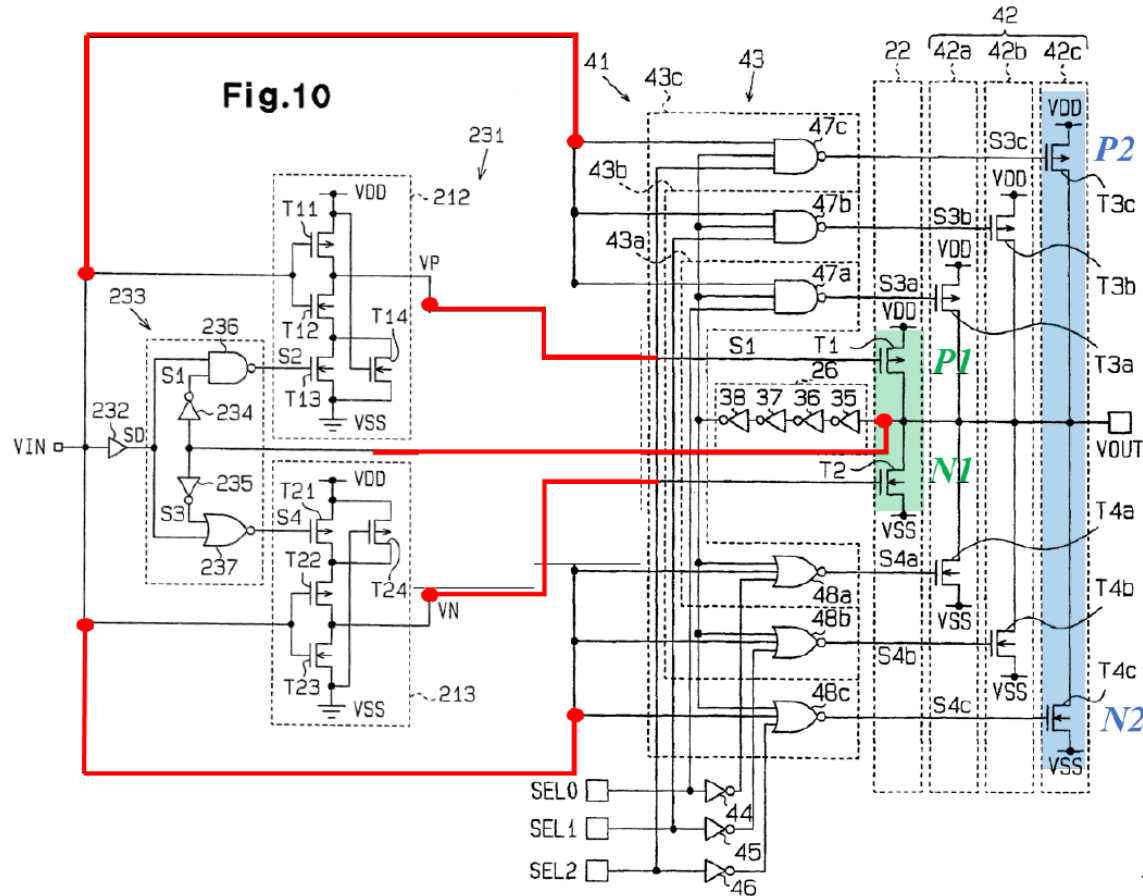
Patent Owner does not contest Petitioner’s allegations that modified Itoh teaches the other elements of the preamble. To the extent that any elements of claim 1’s preamble are limiting, we find, on the basis of Petitioner’s evidence, including the disclosure of Itoh and the credible testimony of Dr. Thompson, that modified Itoh teaches the preamble (limitation [1.0]).

4. Uncontested Limitations of Claim 1

Petitioner maps the remaining limitations of claim 1 to the combination of Figures 8 and 10 of modified Itoh (*see* “Example 2.1” figure above), and argues that modified Itoh teaches all the limitations in the body of claim 1. Pet. 47–58.

For the “main driver” limitation (limitation [1.1]), Petitioner identifies Itoh’s circuits 22, 42 including first pMOS/nMOS transistor pair T1, T2 (annotated by Petitioner as P1, N1 in the figure reproduced below) and second pMOS/nMOS transistor pair T3c, T4c (annotated as P2, N2 in the figure reproduced below). Pet. 47–50 (citing Ex. 1006, 10:1–15, 10:37–42, 12:48–13:62; Ex. 1003 ¶¶ 182–188). A version of the figure depicting Petitioner’s Example 2.1 is reproduced below, with annotations by Petitioner.

Fig.8

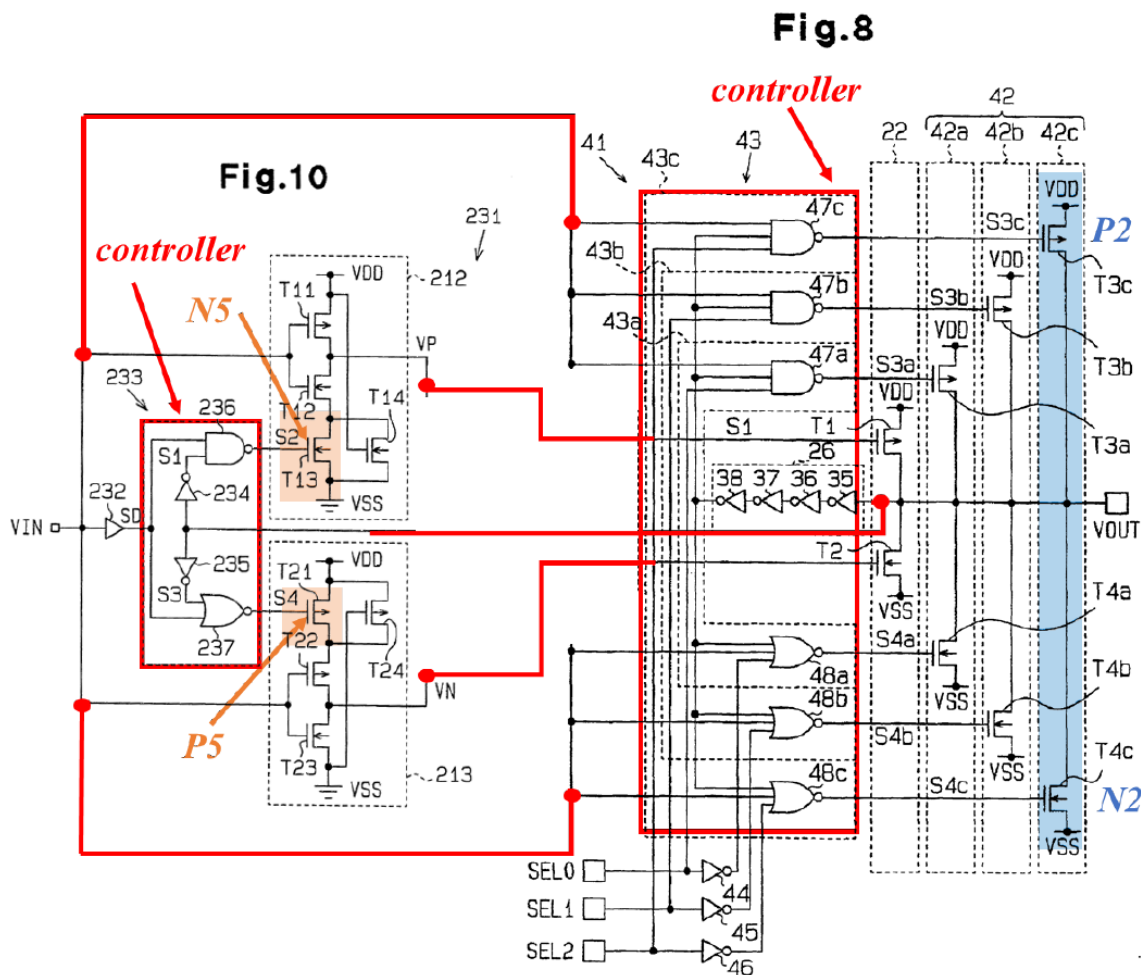


The figure above is an annotated circuit diagram provided by Petitioner to illustrate Petitioner's combination of the circuit diagrams of Figures 8 and 10 of Itoh, with annotations in green for transistors P1 and N1 and blue for transistors P2 and N2. Pet. 48. We agree with Petitioner and find that Itoh teaches claim limitation [1.1].

For the “predriver” limitation (limitations [1.2.1]–[1.2.3]), Petitioner identifies Itoh’s circuits 212, 213 including third pMOS/nMOS transistor pair T11, T12 (annotated as P3, N3 in the “Example 2.1” figure above); fourth pMOS/nMOS transistor pair T22, T23 (annotated as P4, N4); fifth nMOS transistor T13 (annotated as N5); and fifth pMOS transistor T21 (annotated as P5). Pet. 50–55 (citing Ex. 1006, 11:11–20, 11:51–12:4,

12:28–47, 12:50–56, 13:24–30; Ex. 1003 ¶¶ 189–197). We agree with Petitioner and find that Itoh teaches claim limitations [1.2.1]–[1.2.3].

For the “controller” limitation (limitation [1.3]), Petitioner identifies Itoh’s delay circuit 26, control circuit 43, and signal generator 233. Pet. 55–57 (citing Ex. 1003 ¶¶ 202–205); *see also* Ex. 1006, 10:4–7, 10:16–28, 11:13–20, 11:26–57. A version of the figure depicting Petitioner’s Example 2.1 is reproduced below, with annotations by Petitioner:



Pet. 56. According to Petitioner, signal generator 233 receives signals VOUT and Vin and generates signals S2 and S4 to control transistors N5 and P5 in coaction with transistors P2 and N2. *Id.* at 55–57. We agree with Petitioner and find that Itoh teaches claim limitation [1.3].

For the final clause of claim 1 (limitation [1.4]), Petitioner contends that Itoh’s predriver output VP, VN is directly connected only to first pMOS/nMOS transistors T1, T2 (annotated as P1, N1) of main driver 22, 42. Pet. 58 (citing Ex. 1003 ¶¶ 207–209). We agree with Petitioner and find that Itoh teaches claim limitation [1.4].

Patent Owner does not contest Petitioner’s allegations as to limitations [1.1]–[1.4] in the Patent Owner Response or Sur-reply. We find, on the basis of Petitioner’s evidence, including the disclosure of Itoh and the credible testimony of Dr. Thompson, that modified Itoh teaches limitations [1.1]–[1.4].

5. Uncontested Limitations of Claim 4

Claim 4 recites

said second p-channel MOS transistor and said second n-channel MOS transistor have a smaller device size with a smaller gate width than said first p-channel MOS transistor and said first n-channel MOS transistor, and have a small effect on rise and fall times of pulses output from said main driver.

As indicated above, we construe “smaller device size” and “smaller gate width” to be synonymous, rather than two separate requirements of the transistor.

Petitioner contends that during times when the slew rate is controlled, Itoh’s second pMOS/nMOS transistors T3c, T4c (annotated above as P2, N2) are turned off and thus have a small effect on rise and fall times of

output signal VOUT. Pet. 60–61 (citing Ex. 1003 ¶¶ 216–219). Patent Owner does not contest Petitioner’s allegations in the Patent Owner Response or Sur-reply. We find, on the basis of Petitioner’s evidence, including the disclosure of Itoh and the credible testimony of Dr. Thompson, that modified Itoh teaches “said second p-channel MOS transistor and said second n-channel MOS transistor . . . have a small effect on rise and fall times of pulses output from said main driver.”

Petitioner further contends:

For each pair of P2 and N2 of the second-drive circuit 42, selecting a smaller device size with a smaller gate width than P1 and N1 is one of the two well-known design choices (the other is having a greater size), and a [person of ordinary skill in the art] would have used this design option based on corresponding design needs (e.g., specific contribution by this particular pair of P2 and N2 to the overall output impedance).

Id. at 62 (citing Ex. 1003 ¶¶ 220–222; Ex. 1008, 5:8–9); *see also id.* at 46 (contending that it would have been obvious to “adjust the sizes of the transistors based on the design needs (e.g., required output impedance and slew rate)”); Ex. 1003 ¶ 177. Patent Owner does not contest Petitioner’s allegations as to “selecting a smaller device size with a smaller gate width than P1 and N1” in the Patent Owner Response or Sur-reply.⁷

According to the Supreme Court:

When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable

⁷ Patent Owner presented arguments as to this claim limitation in the Preliminary Response (at 9–17), which we found unpersuasive in the Decision to Institute (at 25–29). Patent Owner does not advance those arguments in the Patent Owner Response. Accordingly, those arguments are waived. Paper 10 (Scheduling Order), 9 (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.”).

solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under § 103.

KSR Int’l Co. v. Teleflex Inc., 550 U.S. 398, 421 (2007); *cf. Uber Techs., Inc. v. X One, Inc.* 957 F.3d 1334, 1340 (Fed. Cir. 2020) (“[B]ecause Okubo’s terminal-side plotting and Konishi’s server-side plotting were both well known in the art, and were the only two identified, predictable solutions for transmitting a map and plotting locations, it would have been obvious to substitute server-side plotting for terminal-side plotting in a combination of Okubo and Konishi.”); *CRFD Rsch., Inc. v. Matal*, 876 F.3d 1330, 1347 (Fed. Cir. 2017) (“Based on the Board’s findings and credibility determinations, we conclude that a person of ordinary skill would have two predictable choices for when the Bates system would transmit browser information, providing a person of ordinary skill with a simple design choice as to whether to specify transmission after discontinuation to meet Bates’s goal to preserve the entire session history.”).

In describing Figure 8, Itoh states that “second drive circuit 42 includes a plurality of (three in this case) sub-drive circuits 42*a*, 42*b* and 42*c*.” Ex. 1006, 10:6–8. “The sub-drive circuits 42*a*, 42*b* and 42*c* respectively include PMOS transistors (output transistors) T3*a* to T3*c* and NMOS transistors (output transistors) T4*a* to T4*c*. At least one of the PMOS transistors T3*a*–T3*c* has a different impedance from those of the other.” *Id.* at 10:11–15. According to Itoh, “[t]he output impedance of the output buffer circuit 41 is determined by at least one sub-drive circuit 42*a*–42*c* that has been enabled.” *Id.* at 10:33–35. “In accordance with the select signals

SEL0 to SEL2, at least one of the sub-drive circuits 42a–42c is enabled to select the output impedance when the output signal VOUT is in a static state.” *Id.* at 10:40–43. Thus, Itoh describes enabling one or more of sub-drive circuits 42a–42c to select an appropriate output impedance for the circuit. Although Itoh does not describe the specific sizes of sub-drive circuits 42a–42c relative to each other or to transistors T1 and T2, Dr. Thompson testifies that a skilled artisan would have chosen larger or smaller transistors P2 and N2 to achieve a specific contribution by those transistors to the overall output impedance based on the design needs for the circuit. Ex. 1003 ¶ 220.

We credit Dr. Thompson’s testimony and find Petitioner’s explanation and evidence as to motivation for choosing P2, N2 transistor sizes, i.e., to achieve the desired output impedance, to be persuasive. While Petitioner has not addressed the possibility that P2 and N2 could also be equal in size to P1 and N1, we still find that three possibilities (smaller, larger, and equal) constitute “a finite number of identified, predictable solutions.” *KSR*, 550 U.S. at 421. Furthermore, because P2 and N2 operate as a pair of transistors and transistors P1 and N1 operate as a pair, logically P2 and N2 would be sized as a pair to be smaller, larger, or the same size as the P1, N1 pair.⁸ *See, e.g.*, Ex. 1006, 1:49–52, 7:9–30 (discussing transistor size/gate width of pMOS/nMOS pairs). Thus, we find that a skilled artisan would have considered only these three possibilities in sizing P2, N2 relative to P1, N1.

In sum, we find that Itoh teaches or suggests each limitation of claim 4. Petitioner has introduced persuasive evidence that a skilled artisan would have had reasons to modify Itoh with a reasonable expectation of

⁸ Patent Owner accepts this finding. PO Resp. 15–16.

success. Patent Owner does not argue or introduce evidence of objective indicia of nonobviousness. Upon consideration of all the evidence, we conclude that Petitioner has proved by a preponderance of the evidence that claim 4 would have been obvious over Itoh.

D. Obviousness over Itoh and Muljono

Petitioner contends that claim 4 would have been obvious over Itoh and Muljono. Pet. 81–89, 91. For the reasons explained below, Petitioner has made a sufficient showing.

1. Overview of Muljono (Ex. 1010)

Muljono discloses an output buffer having a driver circuit including an impedance compensation circuit and a pre-driver circuit including a slew rate compensation circuit, to compensate for variations in process skew, supply voltage, and temperature (PVT). Ex. 1010, 2:23–26, 3:31–52, Fig. 1; *see* Pet. 10.

Figure 2 of Muljono is reproduced below.

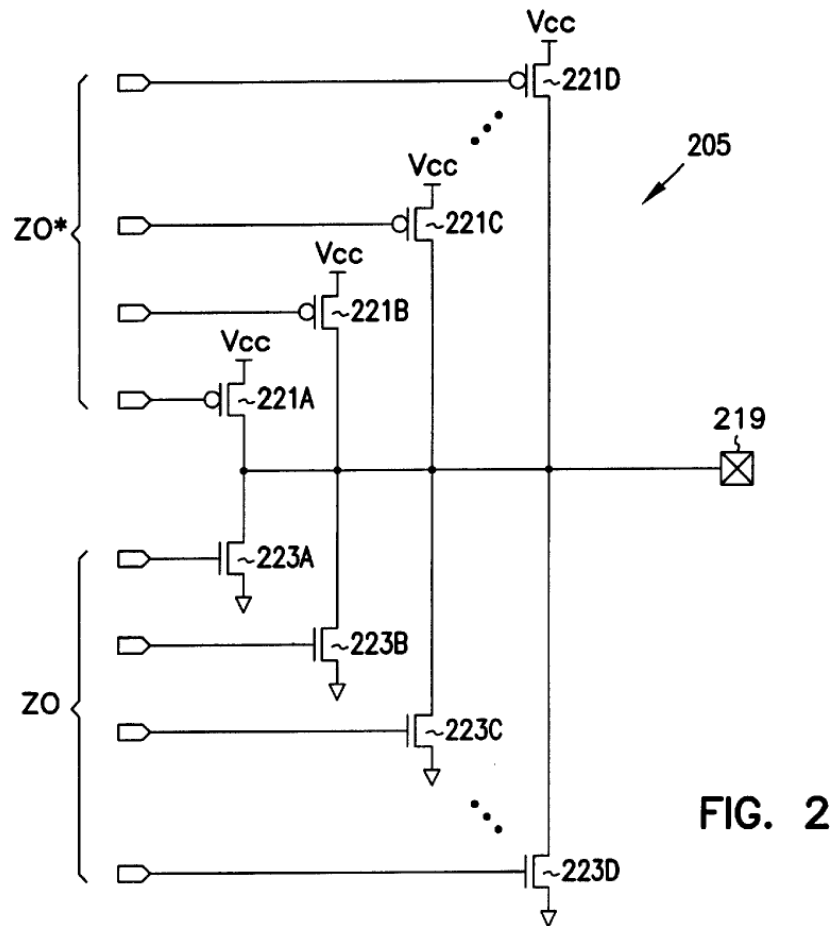


FIG. 2

Figure 2 of Muljono is a circuit diagram of driver circuit 205 including a plurality of p-channel transistors 221A–D coupled in parallel between pin 219 and a bus line (not shown) and supply voltage V_{cc} , and a plurality of n-channel transistors 223A–D similarly coupled in parallel between pin 219 and ground. Ex. 1010, 4:35–40. Transistors 221A–D, 223A–D are controlled by impedance control signals $Z0^*$, $Z0$. *Id.* at 4:41–47. When driver circuit 205 drives a high signal through pin 219, the output impedance is determined by the number of p-channel transistors 221A–D switched on; switching on more p-channel transistors 221A–D decreases the output impedance and vice versa. *Id.* at 4:60–5:4. When driver circuit 205 drives a low signal through pin 219, the output impedance is determined by the number of n-channel transistors 223A–D switched on; switching on more n-

channel transistors 223A–D decreases the output impedance and vice versa.
Id. at 5:5–5:15.

Figure 3 of Muljono is reproduced below.

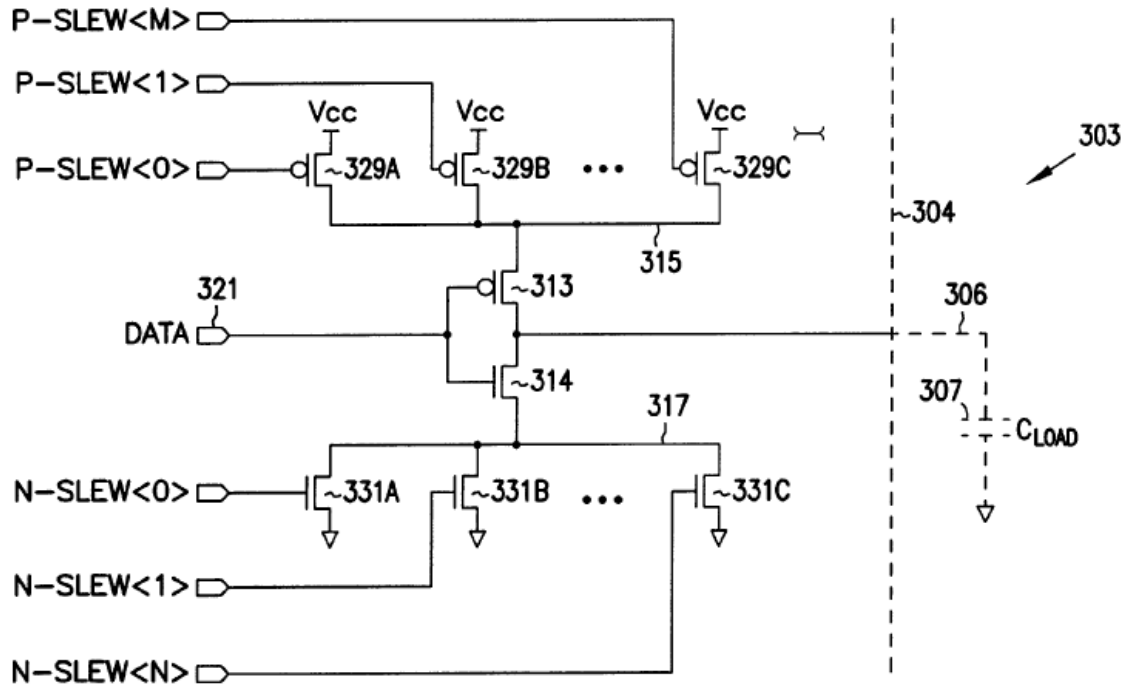


FIG. 3

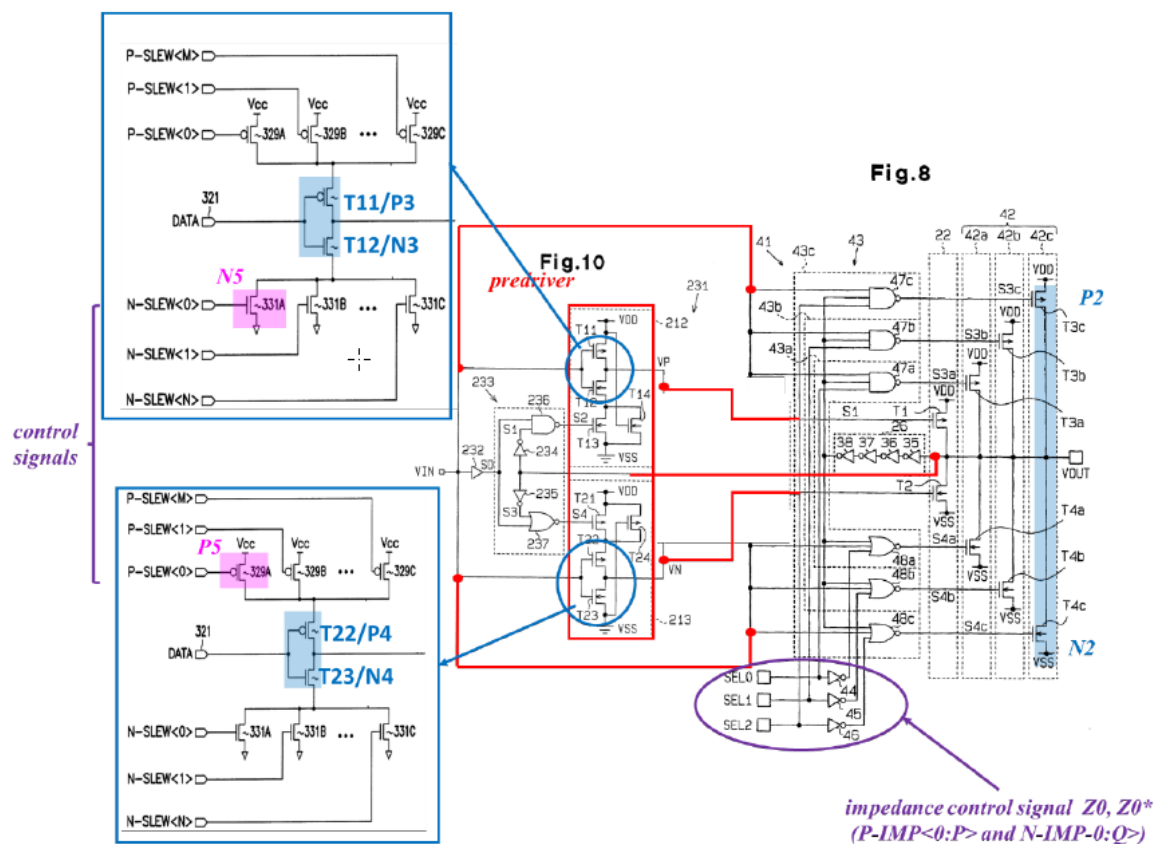
Figure 3 of Muljono is a circuit diagram of pre-driver circuit 303 including an inverter comprising p-channel transistor 313 and n-channel transistor 314. *Id.* at 5:58–60. Pre-driver circuit 303 further includes slew rate compensation circuitry including p-channel transistors 329A–C and n-channel transistors 331A–C, which are driven by slew rate control signals P-SLEW <0:M> and N-SLEW <0:N>, respectively. *Id.* at 5:66–6:20.

2. Petitioner's Combination of Itoh and Muljono

Petitioner starts with its proposed modification of Itoh to combine the teachings of Figures 8 and 10 (Example 2.1) and further adds two aspects

from Muljono. First, Petitioner contends that a skilled artisan “would have been motivated to, for slew rate control, apply Muljono’s slew rate compensation circuit (e.g., EX1010, FIGS. 1, 3) for the inverter pairs with the pairs T11/T12 (P3/N3) and T22/T23 (P4/N4) in FIG. 10 of Itoh.”

Pet. 84. Next, Petitioner argues that “for output impedance control, it would have been obvious for a [person of ordinary skill in the art] to apply Muljono’s impedance control signals (e.g., EX1010, FIGS. 1, 2) to select signals SEL0-SEL2 of FIG. 8, for selecting the sub-driver circuits for output impedance control.” *Id.* Petitioner’s combination of Itoh and Muljono is illustrated in Petitioner’s composite annotated figure below.



Example 3.1
(Combination of Example Embodiment 2.1 and Muljono)

The figure above is an annotated circuit diagram provided by Petitioner to illustrate Petitioner's combination of Itoh and Muljono (dubbed "Example 3.1" by Petitioner). Pet. 88; *see also id.* at 82, 85 (same figure annotated differently); Ex. 1003 ¶¶ 270–276.

Petitioner contends that it would have been obvious to combine Muljono's compensation circuit with modified Itoh (Example 2.1) "to achieve the obvious, beneficial, and predictable results of an output buffer circuit having 'an approximately uniform output impedance and slew rate independent of variations in process skew, supply voltage and temperature' as taught by Muljono." Pet. 81 (quoting Ex. 1010, 2:23–27; citing Ex. 1003 ¶¶ 270–275); *id.* at 83–84 (contending that it would have been obvious to apply Muljono's slew rate compensation circuit and impedance control signals to modified Itoh). According to Petitioner,

applying Muljono's teachings in embodiments of Itoh would have been no more than the combination of known elements according to known methods (e.g., incorporating compensation[] circuits and control signals to the predriver circuit and main driver circuit in an output buffer circuit according to the known IC design steps) obvious to a [person of ordinary skill in the art]."

Id. at 81.

Petitioner supports its proposed combination with the uncontroverted testimony of Dr. Thompson, which we find credible. Ex. 1003 ¶¶ 270–276.

Patent Owner does not contest Petitioner's argument that a skilled artisan would have had reasons to combine Itoh and Muljono. On the complete record, we find that Petitioner's reasons to combine Itoh and Muljono have rational underpinning.

3. *Preamble of Claim 1*

For the preamble of claim 1 (limitation [1.0]), Petitioner and Patent Owner make the same contentions as in the ground alleging obviousness over Itoh, discussed above. Pet. 82 (citing Ex. 1003 ¶ 276); PO Resp. 16, 20; Pet. Reply 18; Sur-reply 22–23. Petitioner adds

Itoh-Muljono renders Claim 4, including the preamble phrase “at a predetermined output impedance” to the extent that it is limiting, obvious. This is because it is undisputed that Muljono, as applied in Itoh-Muljono, goes into significant detail about how to provide a uniform output impedance and the benefits thereof, as described in the Petition

Pet. Reply 17 (citing Pet. 85–88; Ex. 1003 ¶¶ 70–71, 278–283); *see id.* at 19 (citing Ex. 1010, 2:23–27; Ex. 1003 ¶¶ 270–275). As far as the disputed claim language “a predetermined output impedance” is concerned, Petitioner clarified at the oral argument that the addition of Muljono does not change the form of the output compared to modified Itoh. Tr. 18:3–20:12. In other words, the output impedance of the circuit of Itoh-Muljono varies in the same manner as it does in the circuit of modified Itoh.

We apply the same analysis as in the ground alleging obviousness over Itoh discussed above and find the phrase “a predetermined output impedance” in the preamble to be non-limiting. For that reason alone, Patent Owner’s contention that the Itoh-Muljono combination does not teach outputting data “at a predetermined output impedance” is not persuasive.

To the extent that “a predetermined output impedance” is limiting, we find that the Itoh-Muljono combination teaches it for reasons similar to those discussed above. We construe “a predetermined output impedance” to mean one or more output impedances determined in advance. We find that the output buffer of the Itoh-Muljono combination outputs data in the form of an

input pulse train at one or more predetermined output impedances, in the same manner as the circuit of modified Itoh. Although Muljono provides modified control circuitry, we find that the configuration of this control circuitry does not materially change the way the circuit of modified Itoh determines in advance the output impedance during periods when VOUT is at a high level or at a low level. *See* Ex. 1003 ¶¶ 187, 283.

Patent Owner does not contest Petitioner’s allegations that Itoh and Muljono teach the other elements of the preamble. To the extent that any elements of claim 1’s preamble are limiting, we find, on the basis of Petitioner’s evidence, including the disclosures of Itoh and Muljono and the credible testimony of Dr. Thompson, that Itoh and Muljono teach the preamble (limitation [1.0]).

4. Uncontested Limitations of Claim 1

Petitioner maps the remaining limitations of claim 1 to the combination of Itoh and Muljono (*see* “Example 3.1” figure above), and argues that the combination teaches all the limitations in the body of claim 1. Pet. 82–89.

For the “main driver” limitation (limitation [1.1]), Petitioner’s contentions are the same as in the ground alleging obviousness over Itoh, discussed above. Pet. 82 (citing Ex. 1003 ¶ 276). We find that Itoh and Muljono teach claim limitation [1.1] for the same reasons as given above for modified Itoh.

For the “predriver” limitation, with respect to the third pMOS/nMOS transistor pair P3, N3 and fourth pMOS/nMOS transistor pair P4, N4 (limitations [1.2.1–1.2.2]), Petitioner’s contentions are the same as in the ground alleging obviousness over Itoh, discussed above. Pet. 82 (citing

Ex. 1003 ¶ 276). We find that Itoh and Muljono teach claim limitations [1.2.1] and [1.2.2] for the same reasons as given above for modified Itoh.

As to limitation [1.2.3], Petitioner contends that a skilled artisan would have substituted the circuitry of Muljono's Figure 3 for what it previously identified as P3/N3 and P4/N4 in Itoh (circuitry shown in Itoh's Figure 10, and annotated in combined figures above). *Id.* at 83–84. For the fifth nMOS transistor N5, Petitioner identifies Muljono's n-channel transistor 331A. *Id.* at 85 (citing Ex. 1010, 5:67–6:21; Ex. 1003 ¶¶ 278–280). For the fifth pMOS transistor P5, Petitioner identifies Muljono's p-channel transistor 329A. *Id.* at 86. Petitioner contends that a skilled artisan also would have used Muljono's impedance control signals to drive Itoh's sub-driver circuits. *Id.* at 84–85. We agree with Petitioner and find that Itoh and Muljono teach claim limitation [1.2.3].

For the “controller” limitation (limitation [1.3]), Petitioner makes the same contentions as in the ground alleging obviousness over Itoh, discussed above. Pet. 86. Petitioner further identifies Muljono's compensation circuit 115 generating slew rate control signals N-SLEW, P-SLEW and impedance control signals Z0, Z0*. *Id.* at 86–89 (citing Ex. 1010, Fig. 1). Compensation circuit 115, shown in Muljono's Figure 1, supplies slew rate control signals to pre-driver circuit 103, for which the pre-driver circuit of Figure 3 may be substituted. Ex. 1010, 3:44–47, 5:49–52. Compensation circuit 115 further supplies impedance control signals to a driver circuit. *Id.* at 3:44–47. Petitioner contends that N5 and P5 are controlled “in coaction” with P2 and N2, respectively, because “the slew rate control signals are generated **in response to** the impedance control signals Z0, Z0*.” Pet. 88–89 (citing Ex. 1010, 6:36–45); *see* Ex. 1003 ¶ 283. We agree with Petitioner and find that Itoh and Muljono teach claim limitation [1.3].

For the final clause of claim 1 (limitation [1.4]), which recites that the predriver output is “directly connected only to” P1 and N1, Petitioner’s contentions are the same as in the ground alleging obviousness over Itoh, discussed above. Pet. 89 (citing Ex. 1003 ¶ 284). We find that Itoh and Muljono teach claim limitation [1.4] for the same reasons as given above for modified Itoh.

Patent Owner does not contest Petitioner’s allegations as to limitations [1.1]–[1.4] in the Patent Owner Response or Sur-reply. We find, on the basis of Petitioner’s evidence, including the disclosures of Itoh and Muljono and the credible testimony of Dr. Thompson, that Itoh and Muljono teach limitations [1.1]–[1.4].

5. Uncontested Limitations of Claim 4

Petitioner’s and Patent Owner’s contentions for the limitations recited in claim 4 are the same as in the ground alleging obviousness over Itoh, discussed above. Pet. 91 (citing Ex. 1003 ¶ 290); PO Resp. 16, 20; Pet. Reply 18; Sur-reply 22–23. Thus, we apply the same analysis.

In sum, we find that Itoh and Muljono teach or suggest each limitation of claim 4. Petitioner has introduced persuasive evidence that a skilled artisan would have had reasons to combine the teachings of Itoh and Muljono with a reasonable expectation of success. Patent Owner does not argue or introduce evidence of objective indicia of nonobviousness. Upon consideration of all the evidence, we conclude that Petitioner has proved by a preponderance of the evidence that claim 4 would have been obvious over Itoh and Muljono.

IV. CONCLUSION

Petitioner has shown by a preponderance of the evidence that claim 4 would have been obvious.

In summary:

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
4	103(a)	Itoh	4	
4	103(a)	Itoh, Muljono	4	
Overall Outcome			4	

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED, based on a preponderance of the evidence, that claim 4 is unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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