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Paper 10
Entered: February 13, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-01333
Patent 10,049,080 B2

Before WILLIAM V. SAINDON, THOMAS L. GIANNETTI, and GREGG I. ANDERSON, *Administrative Patent Judges*.

GIANNETTI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314
Dismissing Contingent Motion for Joinder
35 U.S.C. § 315(c); 37 C.F.R. § 42.122

I. INTRODUCTION

A. Background

Mercedes-Benz USA, LLC ("Mercedes-Benz") filed a Petition requesting *inter partes* review of claims 1–24 (the "challenged claims") of U.S. Patent No. 10,049,080 B2 (Ex. 1001, the "'080 patent"). Paper 1 ("Pet."). The Petition was accompanied by a "Contingent Motion for Joinder" seeking joinder with IPR2023-00567 (the "'567 IPR"), a proceeding originally filed by Samsung and Qualcomm, involving a challenge to the same claims of the '080 patent as this proceeding. Paper 2. That proceeding has now been terminated. '567 IPR, Paper 22 (Termination Decision).

Daedalus Prime ("Patent Owner") has waived filing of a preliminary response. Paper 9. For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. *See* 35 U.S.C. § 314(a) (*inter partes* review may not be instituted unless "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.") We therefore institute *inter partes* review as to all of the challenged claims of the '080 patent and all of the asserted grounds of unpatentability. *See SAS Inst. Inc. v Iancu*, 138 S.Ct. 1348, 1356 (2018); 37 C.F.R. § 42.108 (a) ("When instituting inter partes review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.").

B. Related Proceedings

The parties identify the following district court and ITC proceedings involving the '080 patent: (1) *Daedalus Prime LLC v. Arrow Electronics, Inc.*, 1:22-cv-01107 (D. Del.); (2) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01109 (D. Del.); (3) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01108 (D. Del.); (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd.*, 2:22-cv-00352 (E.D. Tex.); (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (USITC); and (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (USITC). Pet. 1–2; Paper 5, 2.

As noted *supra*, the '080 patent was also the subject of the '567 IPR, now terminated.

C. Real Parties-in-Interest

Petitioner identifies the following real parties-in-interest: Mercedes-Benz USA, LLC; Mercedes-Benz Intellectual Property GmbH & Co. KG; Mercedes-Benz Group AG; and Mercedes-Benz AG. Pet. 1. Patent Owner identifies Daedalus Prime LLC as the real party-in-interest. Paper 5, 2

At this stage, neither party challenges those identifications.

D. The '080 Patent

The '080 patent is titled "Asymmetric Performance Multicore Architecture with Same Instruction Set Architecture." Ex. 1001, (54). The '080 patent relates to multi-core processors in computing systems and

methods of managing power in multi-core processors. *Id.* at 1:16–1:20; 2:1–2:42; 3:50–4:19.

According to the '080 patent, typically, power management schemes scale up processing performance as the system's workload increases and scale down processing performance as the system's workload decreases. *Id.* at 2:22–26. Scaling process performance with workload is usually accomplished by enabling or disabling entire cores and raising or lowering core supply voltages and operating frequencies in response to workload. *Id.* at 2:30–33. For example, all cores are enabled under a maximum performance/power consumption state, and only one core is enabled under a minimum performance/power consumption state. *Id.* at 2:33–41; *see also id.* Fig. 2.

The '080 patent explains that some prior art multi-core processor power management schemes have been implemented on processors whose constituent cores are identical, while others have been implemented on processors in which the cores are radically different from each other (i.e., asymmetric). Ex. 1001, 3:34–39. For example, a processor with cores that are different from each other may have a low power core that lacks sizeable "chunks" of logic circuitry responsible for executing the program code instructions compared to the other cores in the processor and supports a reduced instruction set. *Id.* at 3:39–46. However, processors with cores that are different from each other can suffer from drawbacks because it is difficult for system software to adjust switch operation between processor cores having different instruction sets. *Id.* at 3:46–49.

The '080 patent purports to address this issue by disclosing multi-core processors in which at least one of the cores is designed to be lower

performance and therefore consumes less power than other cores in the processor. *Id.* at 3:50–4:9. According to the '080 patent, the lower power cores have the same logic design as the higher power cores and support the same instruction set, but consume less power by having narrower drive transistor widths than the higher power cores or other power consumption-related design features. *Id.* at 3:50–62.

The '080 patent explains that the lower power core allows the multi-processor "to entertain a power management strategy that is the same/similar to already existing power management strategies, yet, still achieve an even lower power consumption in the lower/lowest performance/power states." *Id.* at 4:20–46; *see also id.* Fig. 5. The process begins with a multi-core processor in which multiple high power cores and at least one low power core are operating. *Id.* Fig. 6 (610), 4:54–59. When the demand on the processor drops below a threshold, a high power core is disabled. *Id.* at 4:54–59. This process is repeated with the enabled high power cores each time demand reaches a lower threshold. *Id.* at 4:54–5:6. When all of the high power cores are disabled and the demand on the processor continues to drop, the low power cores are disabled one by one in the same manner until only one low power core is enabled and the lower power state is reached. *Id.* at 5:25–35.

E. Illustrative Claim

The Petition challenges claims 1–24, of which claims 1, 9, and 17 are independent. Claim 1 is illustrative of the claimed subject matter and reproduced below: [1]

> 1. [preamble] A multi-core processor comprising:
>
> [a][i] a first plurality of cores and a second plurality of cores that support a same instruction set,
>
> [a][ii] wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and
>
> [b][i] power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,
>
> [b][ii] wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

Ex. 1001, 7:56–8:3.

Independent claim 9 is directed to a method of operating a multi-core processor. *Id.* at 8:38–53. Independent claim 17 is directed to "[a] non-transitory machine readable medium containing program code" that causes the method of claim 9 to be performed. *Id.* at 9:24–41.

F. References and Other Evidence

The Petition relies on the following references:

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[1] Paragraph labeling in brackets is based on those provided by Petitioner.

Name	Reference	Publication Date	Exhibit(s)
Sutardja '748[2]	US 2008/0288748 A1	Nov. 20, 2008	Ex. 1007
Sutardja '785	US 2007/0083785 A1	Apr. 12, 2007	Ex. 1008
Carmack	US 2009/0309243 A1	Dec. 17, 2009	Ex. 1006
Rychlik	US 2011/0145615 A1	Jun. 16, 2011	Ex. 1009
Mathieson[3]	US 2011/0213950 A1	Sep. 1, 2011	Ex. 1005

In addition, Petitioner submits the Declaration of Dr. Robert Horst. Ex. 1034 ("Horst Decl."). In his declaration, Dr. Horst adopts the positions of Dr. Trevor Mudge, who served as petitioners' expert in the '567 IPR. Horst Decl. ¶ 3.

G. Asserted Grounds of Unpatentability

Petitioner asserts the challenged claims are unpatentable on the following grounds:

[2] Sutardja '748 incorporates by reference the disclosure of Sutardja '785 (Ex. 1008) in its entirety. *See* Ex. 1007, 1:8–12.

[3] Petitioner represents that Mathieson incorporates by reference the disclosure of Carmack in its entirety. Pet. 5 n.5; *see also id.* at 18.

Claims Challenged	35 U.S.C. §[4]	References
1–4, 7–12, 15–20, 23, 24	103	Sutardja[5]
5, 6, 13, 14, 21, 22	103	Sutardja, Rychlik
7, 15, 23	103	Sutardja, Carmack
1–4, 7–12, 15–20, 23, 24	103	Mathieson,[6] Sutardja
5, 6, 13, 14, 21, 22	103	Mathieson, Sutardja, Rychlik

See Pet. 5–6.

H. Overview of the Prior Art

1. Sutardja '748 (Ex. 1007)

Sutardja '748 is titled "Dynamic Core Switching." Ex. 1007, (54). Sutardja '748 relates to dynamically switching cores of multi-core processing systems of mobile computing devices. *Id.* ¶ 2. Sutardja '748 explains that processor systems in such computing devices may be asymmetric, with the processors or cores having different instruction set

[4] Because the earliest application from which the '080 patent claims priority was filed before March 16, 2013, the pre-AIA ("America Invents Act") version of § 103 applies. Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011).

[5] Petitioner states that it relies on Sutardja '748 and Sutardja '785, combined, "as a single reference obviousness ground." Pet. 4 n.2. Petitioner therefore refers to the combined references as "combined Sutardja" or just "Sutardja." *See id.*; Horst Decl. ¶ 36 n.2.

[6] References to Mathieson in this ground refer to Mathieson and Carmack (incorporated by reference into Mathieson). Pet. 14 n.3.

architectures, or symmetric, with the processors or cores having identical instruction set architectures. *Id.* ¶¶ 7–8, Figs. 1A, 1B.

Sutardja '748 discloses obtaining increased power savings by using a multi-core processing system with a low-speed, low-power (LP) core and a high-speed, high-power (HP) core. *Id.* ¶ 212. The instruction set architecture (ISA) of the LP core may differ from the ISA of the HP core, or alternatively, both may use the same ISAs. *Id.* ¶ 213.

Sutardja '748 discloses using "core morphing" to optimize power consumption and improve performance. *Id.* ¶ 216. In core morphing, cores are dynamically enabled (i.e., activated) or disabled (i.e., deactivated) based on the system load. *Id.* ¶ 218. When one core is active, other cores may be disabled (i.e., deactivated) to save power. *Id.* For example, the other cores may be put in a standby mode wherein the clock frequency and/or the supply voltage of the other cores may be decreased to values that are lower than when the cores are active. *Id.* Alternatively, the other cores may be completely shut down by disconnecting the power supply to the cores. *Id*.

Sutardja '748 discloses that "[c]ore morphing may be used in multi-core systems comprising one LP core and one HP core. When applications demand still higher performance than that provided by one HP core, multiple HP cores may be used." *Id.* ¶ 219. In the HP mode, the HP core is in the active state and processes threads. *Id.* ¶ 223. The LP core may also operate during the HP mode. In other words, the LP core may be in the active state during all or part of the HP mode. *Id.* Sutardja '748 discloses that core morphing is useful for optimizing battery life and performance of mobile devices. *Id.* ¶¶ 217, 222.

2. Sutardja '785 (Ex. 1008)

Sutardja '785 is titled "System with High Power and Low Power Processors and Thread Transfer." Ex. 1008, (54). Sutardja '785 and Sutardja '748 are related, in that the application for Sutardja '785, U.S. Patent Application No. 11/523,996 (the "'996 application"), is the grandparent (through a continuation and continuation in part) of the application for Sutardja '748. *Id.* (21).[7] As previously noted, the entirety of the Sutardja '785 disclosure is incorporated by reference in Sutardja '748. *See supra*, Section I.F.

Sutardja '785 relates to low power data storage systems. Ex. 1008 ¶ 3. Sutardja '785 discloses a computing device with a system on chip ("SOC") that includes first and second processors. *Id.* ¶ 9. The first processor implemented by the SOC has active and inactive states and processes first and second sets of threads during the active state. *Id.* The second processor implemented by the SOC also has active and inactive states. *Id.* Sutardja '785 explains that the second processor consumes less power in its active state than the first processor when it is in its active state. *Id.*

A control module implemented by the SOC communicates with the first and second processors and selectively transfers the second set of threads from the first processor to the second processor and selects the inactive state of the first processor. *Id.*

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[7] Sutardja '748 is a publication of U.S. Patent Application No. 12/215,760, which is a continuation of U.S. Patent Application No. 12/145,660, which is a continuation-in-part of the '996 application. Ex. 1007, (21), (63).

3. Rychlik (Ex. 1009)

Rychlik is titled "System and Method for Controlling Central Processing Unit Power Based on Inferred Workload Parallelism." Ex. 1009, (54). Rychlik discloses portable computing devices with multiple cores and methods of controlling power in such devices. *Id.* ¶¶ 3–4, 26–30. Rychlik discloses that a computing device includes an operating system with a scheduler that schedules tasks, threads, or a combination of the two for execution within the cores, a parallelism monitor that tracks the workload on the cores, and a controller that controls the power to the cores (i.e., powers them on or off). *Id.* ¶¶ 35–38. When the workload on the cores meets or exceeds a threshold value, the controller may wake up another core, and when the workload on the cores falls below a threshold value, the controller may power off or put a core into standby mode. *Id.* ¶¶ 39–40, 88, 95–96. According to Rychlik, this process may reduce power consumption. *Id.* ¶¶ 4, 95, 97.

4. Carmack (Ex. 1006)

Carmack is titled "Multi-core Integrated Circuits Having Asymmetric Performance Between Cores." Ex. 1006, (54). Carmack discloses a multi-core integrated circuit with asymmetric cores that are each capable of implementing substantially all the functionality of the integrated circuit. *Id.* Abstract, ¶ 3. Carmack specifies that the cores may have the same hardware design, but different component device designs such that the first core may be implemented using a high threshold voltage transistor with a lower leakage current, and the second core may be implemented using a low

threshold voltage transistor with a lower switching delay and lower supply voltage. *Id.* ¶ 15.

Carmack also describes methods of controlling cores based on performance parameters such as workload, operating frequency, power consumption, quality of service, or operating temperature. *Id.* Abstract, ¶¶ 13, 21. Carmack explains that a core control circuit determines which one or more of the cores to use based on the performance parameters and then utilizes a first core and idles a second core if a performance parameter is within a first range, and utilizes a second core and idles a first core if a performance parameter is within a second range. *Id.* Abstract, ¶¶ 3–5, 23–25. A particular core may be idled by turning off its power rail, internally gating its power rail, back biasing its substrate, or gating its clock. *Id.* ¶ 16.

5. Mathieson (Ex. 1005)

Mathieson is titled "System and Method for Power Optimization." Ex. 1005, (54). Mathieson is a continuation-in-part of U.S. Patent Application No. 12/137,053 ("the '053 application") and incorporates its disclosures. *Id.* (63), ¶ 1. Carmack issued from the '053 application. Ex. 1006, (21).

Mathieson discloses a system and method for power optimization. Ex. 1005 ¶ 3. Mathieson discloses a method for optimizing power in a multi-core processing complex that includes a first set of cores comprising one or more fast cores, a second set of cores comprising one or more slow cores, and a controller that determines which mode of operation is more power efficient and causes processing operations to be executed by the first

set of cores or the second set of cores to achieve the lowest total power consumption. Ex. 1005, Abstract, ¶¶ 20, 28, 38.

Mathieson explains that a controller within the CPU switches between a first mode of operation and a second mode of operation based on workload characteristics, performance characteristics of the cores, power characteristics of the cores, and operating conditions of the processing complex. *Id.* Abstract, ¶¶ 8–10, 25, 30, Fig. 2. Mathieson discloses that "[i]n the first mode of operation, the first set of cores is enabled and operable and the second set of cores is disabled" and "[i]n the second mode of operation, the second set of cores is enabled and operable and the first set of cores is disabled." *Id.* ¶ 30 (reference numbers omitted).

The method begins when a processor's controller directs one or more operations to be executed by a first set of cores. *Id.* ¶ 55, Fig. 4A. Next, the controller evaluates a processing parameter associated with processing the operations, such as a processing frequency or instruction throughput, and determines whether the parameter is above a threshold value. *Id.* ¶¶ 55–56. If the parameter exceeds the threshold, the processor continues processing operations using the first set of cores. *Id.* If the parameter is not above the threshold value, the controller directs one or more operations to be executed by a second set of cores. *Id.*

II. DISCRETIONARY DENIAL OF INSTITUTION

The Petition addresses the issue of discretionary denial under 35 U.S.C. §§ 314(a) and 325(d). Pet. 9–14. Petitioner asserts that the Board should not exercise its discretion to deny institution under 35 U.S.C. § 314(b) because the current district court proceedings are stayed and the

proceeding in the ITC is "not a basis to discretionally deny IPR institution." *Id.* at 9 (citing the USPTO Director's June 21, 2022 Guidance Memo "Interim Procedure For Discretionary Denials in AIA Post- Grant Proceedings with Parallel District Court Litigation"). Petitioner asserts that the Board should not exercise its discretion to deny institution under 35 U.S.C. § 325(d)[8] because the analysis under the framework of the Board's precedential decision *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020), "weigh[s] against denial." *Id.* at 9–14.

In this proceeding, Patent Owner has not requested that we exercise our discretion to deny institution under either § 314(a) or § 325(d). Therefore, we do not reach those issues here. In the '567 IPR, Patent Owner argued that the petition there should be denied under § 325(d). '567 IPR, Paper 12 at 10–22. In our Institution Decision in the '567 IPR, we addressed that issue and, after analyzing Patent Owner's arguments, we were not persuaded to exercise our discretion to deny institution under § 325(d). *Id.*, Paper 13 at 13–19.

III. ANALYSIS OF THE CHALLENGED CLAIMS

A. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art of the '080 patent would have possessed "a bachelor's degree in electrical engineering,

[8] "[T]he Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." 35 U.S.C. § 325(d).

computer science, computer engineering, material science, physics, applied physics, or a related field" and would have had "at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa." Pet. 14–15 (citing Horst Decl. ¶ 31).

As noted, Patent Owner has expressly waived filing a preliminary response. Paper 9. At this stage, therefore, Patent Owner does not dispute Petitioner's description of a person of ordinary skill in the art or provide its own description.

We regard Petitioner's description as consistent with the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Thus, for the purpose of our decision, we adopt Petitioner's proposal.

B. Claim Construction

We construe claim terms only as relevant to the parties' contentions and only to the extent necessary to resolve the issues in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Neither party proposes claim constructions for our consideration. Petitioner reports that it "does not believe that any term requires explicit construction." Pet. 15 (citing Horst Decl. ¶¶ 84–85). Patent Owner does not dispute Petitioner's position or address claim construction. Therefore, we determine there are no claim terms that need to be construed at this stage.

C. Obviousness

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called "secondary considerations," including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). At this stage, neither party has presented any evidence on the fourth *Graham* factor.

D. Obviousness of Claims 1–4, 7–12, 15–20, 23, and 24 Based on Sutardja

Petitioner asserts that Sutardja teaches or suggests each limitation of claims 1–4, 7–12, 15–20, 23, and 24 and provides an element-by-element analysis. Pet. 21–45; Horst Decl. ¶¶ 86–160. Patent Owner has not filed a preliminary response and does not dispute these assertions at this stage.

1. Independent Claim 1

a. Preamble: *A multi-core processor comprising*

Petitioner contends Sutardja '748 teaches a multi-core processor. Pet. 22 (citing Ex. 1007 ¶ 221; Fig. 3B); Horst Decl. ¶ 87. Dr. Horst testifies, "Sutardja ['748] teaches a multi-core processor in the form of 'a multi-core

processing system having a LP core and a HP core.'" Horst Decl. ¶ 87 (citing Ex. 1007 ¶ 221).

At this stage, Patent Owner does not dispute this contention. We determine that on this record Petitioner demonstrates sufficiently that the preamble of claim 1 is taught or suggested by Sutardja.[9]

b. Element 1[a][i]: *a first plurality of cores and a second plurality of cores that support a same instruction set,*

Petitioner contends that Sutardja discloses this element. Pet. 22. Petitioner contends that Sutardja '748 discloses a high-speed, high-power (HP) core and a low-speed, low-power (LP) core, both of which support the same instruction set. *Id.* (citing Ex. 1007 ¶ 225). Further, Petitioner contends that "Sutardja ['748] also teaches a plurality of HP cores and a plurality of LP cores." *Id.* (citing Horst Decl. ¶¶ 90–101; Ex. 1007 ¶¶ 219, 248).

At this stage, Patent Owner does not dispute these contentions. We find that Petitioner has made a sufficient showing at this stage that this claim element is met by Sutardja '748. Dr. Horst testifies that "[a person of ordinary skill] would have been motivated to include multiple LP cores" in Sutardja's multi-core processor. Horst Decl. ¶ 91. He reasons that "it was well-known to include multiple low-power cores together with multiple high-power cores in a multi-core processor." *Id.* Dr. Horst backs up his opinion with citations to technical literature. *Id.* He testifies further that "Sutardja ['748] also provides explicit motivation for including multiple LP

[9] We do not express an opinion on whether the preamble is limiting.

cores." *Id.* ¶ 92. He continues, "[a]s Sutardja ['748] explains, various types of applications may be executed on Sutardja's multi-core processor." *Id.* (citing Ex. 1007 ¶ 226). This includes first applications "that require relatively low processing speed during operation" and second and third applications, "each with their own processing requirements." *Id.* ¶¶ 92–93 (citing Ex. 1007 ¶¶ 226–227). He testifies that a person of ordinary skill "seeking to implement Sutardja's teachings in a system in which a large number of applications that require relatively low processing speed during operation are expected to operate would therefore have been motivated to include multiple LP cores capable of handling the execution of such applications without needing to transfer the execution of any of the applications to the HP cores." *Id.* ¶ 98 (internal quotation marks omitted).

Alternatively, Petitioner relies on the teachings of Sutardja '785 for this claim element. Pet. 25–26.

We determine that on this record Petitioner demonstrates sufficiently that this imitation of claim 1 is taught or suggested by Sutardja.

c. Element 1[a][ii]: *wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores*

Petitioner relies on Sutardja '748 to meet this claim element. Pet. 26–27. Petitioner explains that "[t]he second cores (Sutardja's LP cores) consume less power, for a same applied operating frequency and supply voltage, than the first cores (Sutardja's HP cores)." *Id.* at 27; Horst Decl. ¶ 103.

Dr. Horst testifies that "the power consumption of a core with narrow transistors will be less than a core with wider transistors." Horst Decl.

¶ 103. He concludes that "[a person of ordinary skill] would recognize that Sutardja ['748]'s LP core will consume less power than its HP cores for the same reason." *Id*. (citing Ex. 1007 ¶ 230). His testimony is supported by Sutardja '748, which discloses that "[t]he transistors 106 of the HP core 24 tend to consume more power during operation in the active state than the transistors 110 of the LP core 28 . . . . Gates of the transistors 106 may be larger than gates of the transistors 110." Ex. 1007 ¶ 230 (quoted in Horst Decl. ¶ 103).

At this stage we find Dr. Horst's testimony to be credible in light of Sutardja '748. Patent Owner does not challenge Petitioner's contentions at this stage. We, therefore, find that, on this record Petitioner demonstrates sufficiently that Sutardja '748 meets this limitation.

d. Element 1[b][i]: *power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,*

Petitioner relies on Sutardja '748 to meet this element. Pet. 27–34; Horst Decl. ¶¶ 104–118. Specifically, Petitioner identifies the "hypervisor" in Sutardja '748 as disclosing this element. Pet. 32–34. Petitioner explains that "[a person of ordinary skill] would have understood that the hardware on which the disclosed hypervisor is installed corresponds to the claimed power management hardware." *Id.* at 33–34 (citing Horst Decl. ¶ 118).

We find also that Petitioner demonstrates sufficiently that Sutardja '748 discloses that the first and second plurality of cores are enabled and the first plurality of cores is disabled (but not the second plurality) when there is a drop in demand. Pet. 29–32. Referring to Figure 4 of Sutardja '748,

Petitioner explains that "[a person of ordinary skill] would have . . . understood that the transition from the HP mode (with both the HP and LP cores enabled) to the LP mode (with only the LP cores enabled) would occur without disabling any of the LP cores (the claimed second plurality of cores)." Pet. 31–32. Dr. Horst provides supporting testimony. Horst Decl. ¶¶ 112–113. Patent Owner does not challenge this assertion at this stage. We find that Petitioner has sufficiently shown on this record that Sutardja '748 meets this element.

e. Element 1[b][ii]: *wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.*

Petitioner asserts that Sutardja '748 meets this element. Pet. 34–35; Horst Decl. ¶¶ 119–124. Referring to Figure 5 of Sutardja '748, Petitioner identifies Kernel Module 220 and PMS Module 242 as the claimed operating system software. Pet. 34–35. Petitioner contends that "Sutardja '[748] further discloses that the operating system (kernel module and PMS module) controls the power management hardware (core switching module) based on the demand." *Id.* at 35 (citing Ex. 1007 ¶ 253).

Patent Owner does not challenge this assertion at this stage. On this record we find that Petitioner has sufficiently shown that Sutardja '748 meets this element.

f. Summary

We find, on this record, that Petitioner demonstrates a reasonable likelihood of prevailing on this challenge to claim 1.

2. Independent Claims 9 and 17

Petitioner's analysis of these claims incorporates its analysis of claim 1. Pet. 43–44. At this stage, Patent Owner does not address these claims. For the reasons given for claim 1, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

3. Dependent Claims 2–4, 7, 8, 10–12, 15, 16, 18–20, 23, and 24

Petitioner provides an analysis for each of these dependent claims in relation to Sutardja. Pet. 35–42 (claims 2–4, 7, 8), 44–45 (claims 10–12, 15, 16, 18–20, 23, 24). Patent Owner does not address these claims.

For the reasons given above and in the Petition, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

E. Obviousness of Claims 5, 6, 13, 14, 21, and 22 Based on Sutardja '748 and Rychlik

Petitioner provides an analysis for each of these dependent claims in relation to Sutardja '748 and Rychlik. Pet. 45–51. Petitioner asserts that Sutardja '748 and Rychlik teach each limitation of claims 5, 6, 13, 14, 21, and 22. *Id.*; Horst Decl. ¶¶ 161–177.

Petitioner provides a motivation for combining the teachings of Sutardja '748 and Rychlik. *See* Pet. 48 ("A [person of ordinary skill] would have been motivated to apply Rychlik's teachings to Sutardja's LP cores, to disable an additional core of Sutardja's LP cores (the claimed second plurality of cores), for each continued drop in workload (the claimed demand) below a next lower threshold, until only one LP core remained enabled."). Dr. Horst testifies that "[a person of ordinary skill] seeking to

implement Sutardja's teachings in a system with multiple of Sudardja's LP cores, would understand that . . . disabling one or more of those LP cores when demand is low, would save power." Horst Decl. ¶ 169.

At this stage, Patent Owner does not address these challenges. For the reasons given above and in the Petition, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

F. Obviousness of Claims 7, 15, and 23 Based on Sutardja '748 and Carmack

Petitioner provides an analysis for each of these dependent claims in relation to Sutardja '748 and Carmack. Pet. 51–52. Petitioner asserts that Sutardja '748 and Carmack teach each limitation of claims 7, 15, and 23. *Id.*; Horst Decl. ¶¶ 178–181. Petitioner provides a motivation for combining the teachings of Sutardja '748 and Carmack. *See* Pet. 52 ("A [person of ordinary skill] would have been motivated to set the high value to the maximum frequency of Sutardja's HP cores, as taught by Carmack, to maintain desired performance levels during periods of high demand.") (citing Horst Decl. ¶ 180).

At this stage, Patent Owner does not address Petitioner's arguments. For the reasons given above and in the Petition, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

G. Obviousness of Claims 1–4, 7–12, 15–20, 23, and 24 Based on Mathieson and Sutardja '748

Petitioner asserts that Mathieson and Sutardja '748 teach each limitation of claims 1–4, 7–12, 15–20, 23, and 24 and provides an element-

by-element analysis for each. Pet. 53–81; Horst Decl. ¶¶ 182–263. Petitioner contends that a person of ordinary skill would have been motivated to combine Mathieson with Sutardja '748 with a reasonable expectation of success. Pet. 53. Among other reasons, "each relates to the same well-known subject matter of power management in multi-core processors, both teaching techniques for reducing power consumption in response to decreased demand/workload." *Id.* (citing Horst Decl. ¶ 182).

Patent Owner does not challenge the motivation to combine these references. We find that on this record Petitioner has demonstrated sufficiently a motivation to combine Mathieson and Sutardja '748. In the analysis that follows we do not rely on 'Sutardja '785, and therefore we do not address the motivation to combine Mathieson with that reference at this time.

1. Independent Claim 1

Petitioner contends that Mathieson and Sutardja, together, meet the limitations of claim 1 and provides an element-by-element analysis. Pet. 53–67. Petitioner provides supporting testimony from Dr. Horst. Horst Decl. ¶¶ 184–219.

For example, Petitioner identifies Mathieson and Sutardja '748 as disclosing the claimed "first plurality of cores and a second plurality of cores that support a same instruction set" in claim element 1[a][i]. Pet. 55–57. Petitioner explains that Sutardja '748 also discloses that both the HP and IP cores may use the same ISAs [Instruction Set Architectures]. Pet. 57 ("Sutardja ['748] . . . provides express teachings to use the 'same instruction set' for different cores.").

Petitioner identifies Mathieson as teaching claim element 1[a][ii] ("wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores"). *Id.* at 58–59. Referring to Figure 6 of Mathieson, Petitioner asserts that "for a large frequency range . . . , the power consumed by Mathieson's second set of cores . . . is less than the power consumed by Mathieson's first set of cores . . . for the same operating frequency." *Id.* at 58 (citing Horst Decl. ¶ 196) (emphasis omitted).

Petitioner relies on Mathieson to meet the "power management hardware" limitation of element 1[b][i]. *Id.* at 59–65. Dr. Horst provides supporting expert testimony on this issue which is uncontradicted by any evidence from Patent Owner. Horst Decl. ¶¶ 202–208. Dr. Horst testifies that "Mathieson teaches a state where the first plurality of cores (Mathieson's first set of cores 210) and the second plurality of cores (Mathieson's second set of cores 220) are both enabled." Horst Decl. ¶ 203 (citing Ex. 1005 Fig. 4A). Still referring to Figure 4A, he testifies that "Mathieson teaches disabling all of the first plurality of cores (Mathieson's first set of cores 210) for a drop in demand (Mathieson's workload) below a threshold without disabling any of the second plurality of cores (Mathieson's second set of cores 220)." *Id.* ¶ 206. He testifies that "[a person of ordinary skill] would have understood that the second set of cores 220 would remain enabled throughout the switch from the first mode of operation (in which both the first set of cores 210 and the second set of cores 220 are enabled) to the second mode of operation (in which only the second set of cores 220 are enabled)." *Id.* ¶ 208.

For element 1[b][ii], Petitioner contends Mathieson, alone or in combination with the Sutardja References, discloses or suggests "wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand" as claimed. Pet. 65–67. Petitioner contends that controller 240 in Mathieson performs this function and is part of an operating system executing on CPU 102. *Id.* at 66. Mathieson discloses that the controller can be "implemented in software and is executed by the CPU 102." *Id.* (quoting Ex. 1005 ¶ 30).

As noted, Patent Owner provides no testimony or other evidence in rebuttal. We find that, at this stage, the evidence presented by Petitioner demonstrates sufficiently that Mathieson and Sutardja '748 meet the elements of claim 1. Further, we have addressed the motivation to combine these references *supra*. For the reasons given in the Petition and those summarized *supra*, we determine that on this record Petitioner has demonstrated a reasonable likelihood of prevailing on this challenge.

2. Independent Claims 9 and 17

Petitioner's analysis of these claims refers back to its analysis of claim 1. Pet. 79–80. At this stage, Patent Owner does not address these claims. For the reasons given for claim 1, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

3. Dependent Claims 2–4, 7, 8, 10–12, 15, 16, 18–20, 23 and 24

Petitioner provides an analysis for each of these dependent claims in relation to Mathieson and Sutardja '748. Pet. 67–78 (claims 2–4, 7, 8), 80–

81 (claims 10–12, 15, 16, 18–20, 23, 24). At this stage, Patent Owner does not address these claims.

For the reasons given in the Petition, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

1. Obviousness of Claims 5, 6, 13, 14, 21, and 22 Based on Mathieson, Sutardja '748, and Rychlik

Petitioner asserts that Mathieson, Sutardja '748, and Rychlik teach each limitation of claims 5, 6, 13, 14, 21, and 22. Pet. 81–83; Horst Decl. ¶¶ 264–271. Petitioner provides a motivation for combining the teachings of Mathieson, Sutardja '748, and Rychlik. *Id.* at 82–83; Horst Decl. ¶¶ 265–268.

At this stage, Patent Owner does not address these challenges. For the reasons given in the Petition, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

IV. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

V. MOTION FOR JOINDER

As discussed *supra*, Petitioner filed a motion for joinder with the '567 IPR in which Qualcomm was the remaining petitioner. Paper 2, 1. Petitioner presented its motion as "contingent"; that is, "should the

Qualcomm IPR be terminated prior to any institution decision or otherwise not instituted for any reason, Petitioner submits this motion for joinder would be moot, and requests the Board consider Petitioner's *inter partes* review petition on its own merits." *Id.* As discussed *supra*, the '567 IPR has been terminated as a result of a settlement. *See supra*. We therefore dismiss Petitioner's Contingent Motion for Joinder (Paper 2) as moot and proceed based on the merits of the Petition in this case.

VI. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '080 patent is hereby instituted for all of the challenged claims on all of the asserted grounds;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision; and

FURTHER ORDERED that Petitioner's Contingent Motion for Joinder is dismissed as moot.

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