

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,

Petitioner,

v.

DAEDALUS PRIME LLC,

Patent Owner.

Case No.: IPR2023-01333

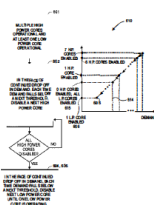
U.S. Patent No. 10,049,080

Patent Owner's Demonstrative Exhibits

MB USA v. Daedalus Prime IPR2023-01333
Patent Owner's Demonstrative Exhibits -- Not Evidence
Daedalus Ex. 2008

'080 Patent

(12) United States Patent George et al.	(10) Patent No.: US 10,049,080 B2 (45) Date of Patent: Aug. 14, 2018
(54) ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE	(56) References Cited U.S. PATENT DOCUMENTS
(71) Applicant: Intel Corporation , Santa Clara, CA (US)	7,992,020 B1 8/2011 Tuan et al. G06F 1/006 2006/0095907 A1* 5/2006 Grochowski 7/13/24
(72) Inventors: Varghese George , Folsom, CA (US); Sanjeev S. Jahagirdar , Folsom, CA (US); Deborah T. Marr , Portland, OR (US)	2006/0279152 A1* 12/2006 Ha 3/10/14 2006/0282692 A1 12/2006 Oh 2008/0127192 A1 5/2008 Capps et al. G06F 1/0203 2008/0263324 A1* 10/2008 Satajda 7/12/43
(73) Assignee: INTEL CORPORATION , Santa Clara, CA (US)	2008/0288748 A1 11/2008 Satajda et al. 2009/0055826 A1 2/2009 Bernstein et al. (Continued)
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(h) by 0 days.	FOREIGN PATENT DOCUMENTS CN 101076770 A 11/2007
(21) Appl. No.: 15/431,527	OTHER PUBLICATIONS
(22) Filed: Feb. 13, 2017	Final Office Action from U.S. Appl. No. 13/335,257, dated May 5, 2015, 13 pages.
(65) Prior Publication Data US 2017/0154012 A1 Jun. 1, 2017	(Continued)
Related U.S. Application Data (63) Continuation of application No. 13/335,257, filed on Dec. 22, 2011, now Pat. No. 9,569,278.	Primary Examiner—Eric Coleman (74) Attorney, Agent, or Firm—Nicholas De Vos Webster & Elliott LLP
(51) Int. Cl. G06F 15/80 (2006.01) G06F 13/40 (2006.01) G06F 1/32 (2006.01)	(57) ABSTRACT A method is described that entails operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set, a first core being higher performance and consuming more power than a second core under a same set of applied supply voltage and operating frequency.
U.S. CL. CPC G06F 15/80 (2013.01); G06F 1/3206 (2013.01); G06F 1/3291 (2013.01); G06F 1/3296 (2013.01); G06F 13/4022 (2013.01)	
(58) Field of Classification Search None See application file for complete search history.	24 Claims, 8 Drawing Sheets



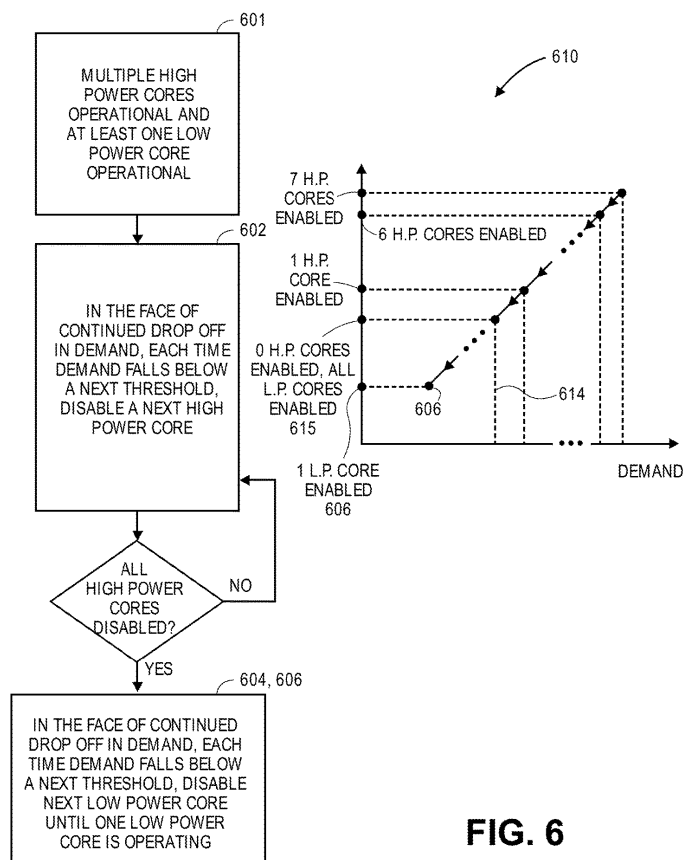
Rather than only relying on adjustments to operating frequency and/or voltage or employing low power states when a core is inactive, the '080 patent describes a multi-core processor that makes use of different types of processor cores that consume different amounts of power and offer different performance capabilities (for a given operating frequency and/or voltage), yet which support the same instruction set.

To achieve this, the different types of processor cores can employ different power consumption design features, such as different transistor technologies.

Consequently, while the different types of processor cores can each execute the same instructions, “low-power” cores will “exhibit inherently lower power consumption (and processing performance) than the higher power core(s),” even when the low-power core is operated at the same clock frequency as a high-power core.

Ex. 1001 at 3:50 – 4:16
POR at 6.

'080 Patent



In a multi-core processor in which multiple high-power cores and at least one low power core are operating, as demand on the processor decreases, the various high-power cores are disabled one at a time, until all are disabled. '080.

If all of the high-power cores are disabled and the demand on the processor continues to drop, then the low-power cores are disabled one by one until only one low-power core remains enabled and the processor's lowest power state is reached.

During this process, before a core (high-power or low-power) is disabled, its individual operating frequency and/or supply voltage, or the operating frequencies and/or supply voltages of some or all of the enabled cores, may be reduced in response to the drop in demand. And, if only one low power core is operating, its operating frequency and/or supply voltage may similarly be reduced until a lowest power consumption state is reached.

Ex. 1001 at 4:54 – 5:49
POR at 7-8.

'080 Claim Construction

What is claimed is:

1. A multi-core processor comprising:

a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

Microsoft Computer Dictionary

operating system *n.* The software that controls the allocation and usage of hardware resources such as memory, central processing unit (CPU) time, disk space, and peripheral devices. The operating system is the foundation software on which applications depend. Popular operating systems include Windows 98, Windows NT, Mac OS, and UNIX. *Acronym: OS. Also called: executive.*

Horst Deposition

2 Q We're using this term "operating system."
3 What would the person of ordinary skill in the
4 art understand an operating system is?
5 A An operating system is the software that
6 controls the dispatching of tasks and gives the
7 interfaces between the applications and the peripherals,
8 such as the disk drives.

...

10 THE WITNESS: The operating system must at
11 least include the software that monitors demand. So
12 that's the part of the operating system that's key to
13 the -- to these claims.

Ex. 2002 at 32:1 – 34:19
Ex. 2007 at 378
POR at 9, 12-13.

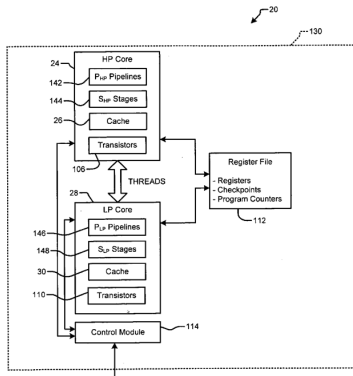
'080 Challenges

Ground	Basis	Claims	References
1	103	1-4, 7-12, 15-20, and 23-24	Sutardja
2	103	5-6, 13-14, and 21-22	Sutardja in view of Rychlik
3	103	7, 15, and 23	Sutardja in view of Carmack
4	103	1-4, 7-12, 15-20, and 23-24	Mathieson in view of Sutardja
5	103	5-6, 13-14, and 21-22	Mathieson/Sutardja in view of Rychlik

Pet. at 5-6.
POR at 13-14.

Sutardja

(19) United States		
(12) Patent Application Publication		
Sutardja et al.		
(54) DYNAMIC CORE SWITCHING		
(76) Inventors: Sehat Sutardja , Los Altos Hills, CA (US); Hong-Yi Chen , Fremont, CA (US); Premanand Sakarda , Acton, MA (US); Mark N. Fullerton , Austin, TX (US); Jay Heeb , Gilbert, AR (US)		
Correspondence Address: HARNES, DICKEY & PIERCE P.L.C. , 5445 CORPORATE DRIVE, SUITE 200 TROY, MI 48068 (US)		
(21) Appl. No.: 12/215,760		
(22) Filed: Jun. 30, 2008		
Related U.S. Application Data		
(63) Continuation of application No. 12/145,660, filed on Jun. 25, 2008, which is a continuation-in-part of application No. 11/523,996, filed on Sep. 20, 2006.		
(60) Provisional application No. 60/968,143, filed on Aug. 27, 2007, provisional application No. 60/978,936, filed on Oct. 10, 2007, provisional application No. 60/981,606, filed on Oct. 22, 2007, provisional application No. 61/022,431, filed on Jan. 21, 2008, provisional application No. 61/020,476, filed on Feb. 18, 2008, provisional application No. 61/049,641, filed on		
(10) Pub. No.: US 2008/0288748 A1		
(43) Pub. Date: Nov. 20, 2008		
May 1, 2008, provisional application No. 61/058,050, filed on Jun. 2, 2008, provisional application No. 60/825,368, filed on Sep. 12, 2006, provisional application No. 60/823,453, filed on Aug. 24, 2006, provisional application No. 60/822,015, filed on Aug. 10, 2006.		
Publication Classification		
(51) Int. Cl. G06F 15/00 (2006.01)		
G06F 9/00 (2006.01)		
(52) U.S. Cl. 712/20; 712/E09.001		
(57) ABSTRACT		
A core switching system includes a mode switching module that receives a switch signal to switch operation between a first mode and a second mode. During the first mode, instructions associated with applications are executed by a first asymmetric core, and a second asymmetric core is inactive. During the second mode, the instructions are executed by the second asymmetric core, and the first asymmetric core is inactive. A core activation module stops processing of the applications by the first asymmetric core after interrupts are disabled. A state transfer module transfers a state of the first asymmetric core to the second asymmetric core. The core activation module allows the second asymmetric core to resume execution of the instructions and the interrupts are enabled.		



Sutardja '748 relates to “dynamically switching cores of multi-core processing systems of mobile computing devices,” in which “cores are dynamically enabled (i.e., activated) or disabled (i.e., deactivated) based on the system load.”

When one core is active, other cores may be disabled (i.e., deactivated), e.g., by being put in a standby mode or completely shut down, to save power. In HP mode, the HP core is in the active state and processes threads. The LP core may also operate during the HP mode. “When applications demand still higher performance than that provided by one HP core, multiple HP cores may be used.”

Sutardja '748 incorporates by reference Sutardja '785, which describes a system on chip that includes first and second processors. Each processor has an active and inactive state, with the second processor consuming less power when operating in its active state than the first processor when operating in its active state. A control module communicates with the first and second processors and selectively transfers threads from one to the other and selects the inactive state of the first processor.

Ex. 1007 at [0002], [0009], [0218], [0219], [0223]
POR at 17-19.

Failings of Sutardja

What is claimed is:

1. A multi-core processor comprising:

a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

Sutardja does not teach or suggest an operating system executing on a multi-core processor to monitor a demand for the multi-core processor and control power management hardware based on the demand.

Ex. 1001 at 7:58 – 8:3
POR at 20.

Failings of Sutardja

Petition Argument

“Sutardja teaches that the transition from the HP mode to the LP mode is performed using hardware (the claimed power management hardware). [A] ‘core switching module’ is used to transition the system between the HP and LP modes. *The hardware controlled by the core switching module corresponds to the claimed power management hardware*[, which] Sutardja explains [] ‘may be integrated with [a] hypervisor module 213,’ as illustrated in Figure 5.”

“A POSITA would have understood that *the hardware on which the disclosed hypervisor is installed corresponds to the claimed power management hardware.*”

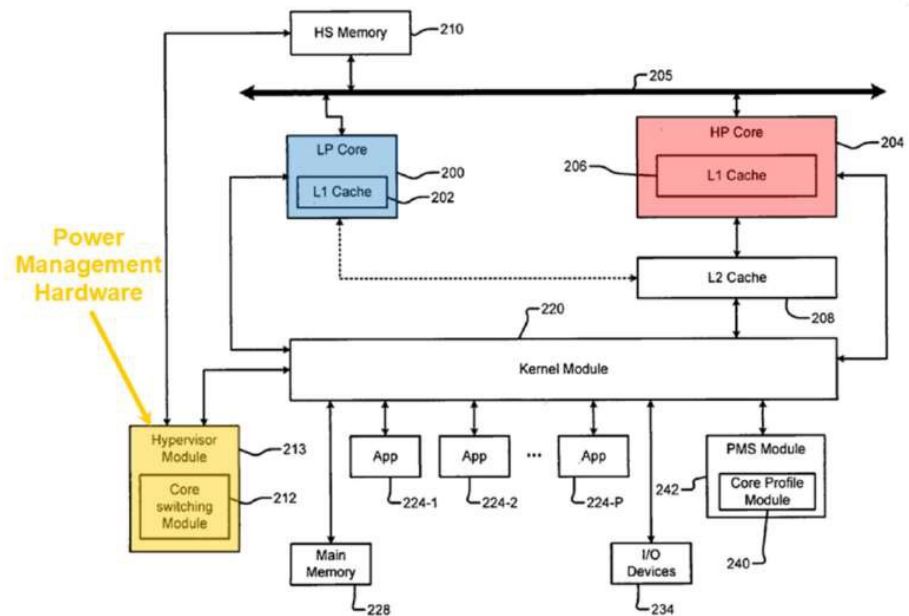


FIG. 5

Pet. at 32-34.

Failings of Sutardja

Hypervisor

A hypervisor is a component that abstracts one computer resource from another resource, allowing that other resource to operate in a self-contained fashion.

Horst Deposition

4		A hosted hypervisor is a hypervisor
5		that runs inside the operating
6		system. It is installed and runs
7		as an application on top of an
8		operating system.
9		The bare-metal hypervisor runs
10		directly on the hardware.
11		So a hypervisor is a way of determining and
12		migrating where processes run in a machine.

POR at 23-24.
Ex. 2006 at ¶¶ 46-47
Ex. 2002 at 20:4-12

Failings of Sutardja

Petition Argument

“Sutardja further discloses that *the operating system (kernel module and PMS module) controls the power management hardware (core switching module) based on the demand: ‘the PMS module 242, and/or the kernel module 220 ... generate[s] a system call to a ... core switching module 212 to trigger a transition.’”*

Flaws

1. Sutardja’s core switching module is not “hardware.”

“Depending on whether the core switching module 212 is integrated in the hypervisor module 213, the hypervisor module 213 or the core switching module 212 *is loaded into the high-speed memory 210 from RAM or other storage after bootup.*”

Hardware **cannot** be “loaded into high-speed memory from RAM or another storage device.”

Failings of Sutardja

Petition Argument

“A POSITA would have understood that *the hardware on which the disclosed hypervisor is installed corresponds to the claimed power management hardware.*”

Flaws

2. An Operating System cannot control hardware on which a hypervisor runs when the hypervisor “operates below the kernel.”

A hypervisor operating below the kernel is the thing that is “manag[ing] transfers between the processors and suspend[ing] operation of one asymmetric processor while the other asymmetric processor operates.”

Failings of Sutardja

Petition Argument

The hardware controlled by the core switching module corresponds to the claimed power management hardware[, which] Sutardja explains [] ‘may be integrated with [a] hypervisor module 213,’ as illustrated in Figure 5.”

Flaws

3. The kernel and the PMS module (“operating system”) do not “control” the core switching module or the hardware on which it runs. The core switching module does.

“When the LP core 200 reaches its highest operating speed and additional system loading occurs, the core profile module 240, the PMS module 242, and/or the kernel module 220 disable interrupts and generate a system call to a hypervisor module 213 or a core switching module 212 to trigger a transition. ***The core switching module 212 may transition (switch) the operation from the LP core 200 to the HP core 204 in response to the system call and return control to the kernel module 220 after the transition (switching) is complete.***”

Pet. at 32-33.
Ex. 1007 at [0253].
POR at 27-28.

Mathieson

Mathieson describes a “technique for reducing the power consumption required to execute processing operations” using a processing complex such as “a CPU or a GPU” that includes “a first set of cores comprising one or more fast cores and a second set of cores comprising one or more slow cores.”

(19) **United States**
(12) **Patent Application Publication** (10) Pub. No.: US 2011/0213950 A1
Mathieson et al. (43) Pub. Date: Sep. 1, 2011

(54) **SYSTEM AND METHOD FOR POWER OPTIMIZATION**

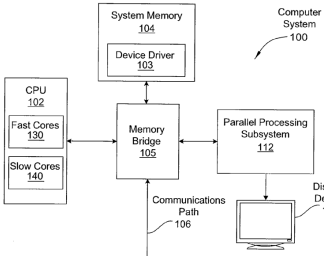
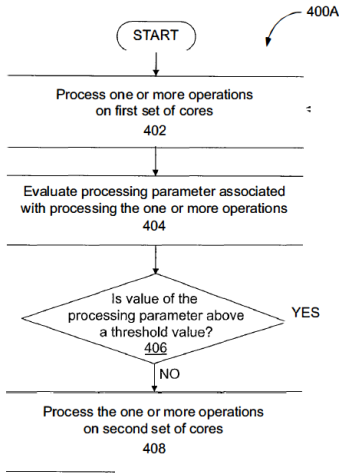
(76) Inventors: John George Mathieson, San Jose, CA (US); Phil Carmack, Santa Clara, CA (US); Brian Smith, Mountain View, CA (US)

(21) Appl. No.: 12/787,359

(22) Filed: May 25, 2010

Related U.S. Application Data
(63) Continuation-in-part of application No. 12/137,053, filed on Jun. 11, 2008.

Publication Classification
(51) Int. Cl. G06F 15/76 (2006.01)
G06F 9/02 (2006.01)
(52) U.S. Cl. 712/38; 712/E09.002
(57) **ABSTRACT**
A technique for reducing the power consumption required to execute processing operations. A processing complex, such as a CPU or a GPU, includes a first set of cores comprising one or more fast cores and second set of cores comprising one or more slow cores. A processing mode of the processing complex can switch between a first mode of operation and a second mode of operation based on one or more of the workload characteristics, performance characteristics of the first and second sets of cores, power characteristics of the first and second sets of cores, and operating conditions of the processing complex. A controller causes the processing operations to be executed by either the first set of cores or the second set of cores to achieve the lowest total power consumption.



The system includes a “central processing unit (CPU) 102,” which includes “one or more ‘fast’ cores 130 and one or more ‘shadow’ or slow cores 140.” [0020]. A controller evaluates a “least workload associated with one or more operations to be executed by the CPU 102,” and configures the CPU 102 to operate in either a first mode of operation (w/the only first set of cores enabled) or a second mode of operation (w/the only second set of cores enabled). “The transition from the first mode to the second mode, and vice versa, can be done transparently to high level software, such as the operating system.”

Ex. 1005 at Abst., [0030], [0043].
POR at 31-33.

Mathieson

Simultaneous operation of the first and second set of cores is limited to a “transition period when transitioning between the first mode and second mode, or vice versa.”

Determining which cores (the first set or second set of cores) to use when executing processing operations may be based on operating frequency. See Fig. 6 (showing power consumption (axis 604) as a function of operating frequency (axis 602) for both the “fast” cores (line 606) and “slow” cores (line 608)).

The controller determines whether to execute processes on the “fast” or “slow” cores by referencing a “particular operating frequency threshold 610” that signifies the operating frequency at which the “slow” cores no longer consume less power than the “fast” cores.

The controller then executes the tasks on the set of cores that would consume less power at that frequency.

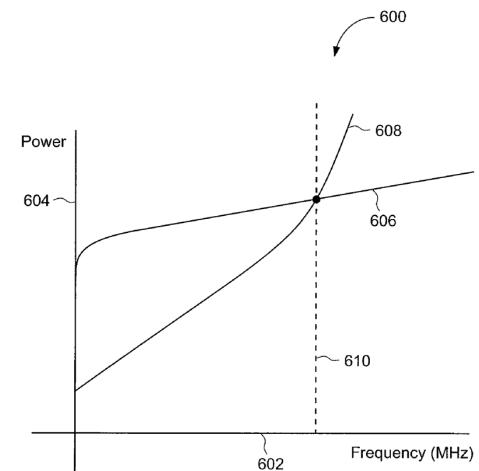


FIG. 6

Ex. 1005 at [0031], [0054], [0075], Fig. 6,
POR at 33-34.

Failings of Mathieson-Sutardja

Flaws

Petition Argument

Because the controller is implemented in software, is executed by the CPU 102, and both manages processing operations executing on CPU 102 and selects the underlying hardware (e.g., cores 210 and/or 220) on which those operations are executed, a POSITA would recognize that the controller performs the functions of an operating system, and thus would view controller 240 as being part of an operating system executing on CPU 102.

Mathieson notes,

The transition from the first mode to the second mode, and vice versa, can be done transparently to high level software, such as the operating system.

A POSITA would appreciate that if the transition between modes, which involves the controller transferring processor state from one set of cores to the other set of cores, is to be done *transparently* to the operating system, then it is **not** the operating system that is effecting the transition.

Hence, the controller does **not** perform the functions of an operating system in effecting the transition between modes.

Failings of Mathieson-Sutardja

Petition Argument

The power consumed by Mathieson's second set of cores (blue) is less than the power consumed by Mathieson's first set of cores (red) for the same operating frequency.

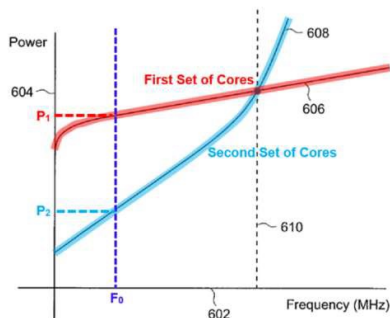


FIG. 6

Flaws

The claims require the same applied operating frequency *and* supply voltage.

Mathieson's Fig 6 does *not* address the supply voltage and therefore does not support an argument that the second plurality of cores consume less power, for a same *applied* supply voltage.

Mathieson does *not* compare power consumption of fast vs. slow cores for a same applied operating frequency and supply voltage. Rather, Mathieson discusses power consumption of cores **only on the basis of operating frequency**.

Pet. at 58.
POR at 38-39, 42-43.

Conclusion

The Petition has failed to prove the unpatentability of any of the challenged claims.

POR at 44.