



Mercedes's Hearing Demonstratives for *Mercedes vs. Daedalus Prime*

IPR2023-01333

U.S. Patent No. 10,049,080

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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Overview of the patent

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Mercedes EX1039
Mercedes-Benz USA, LLC
v. Daedalus Prime LLC
IPR2023-01333



'080 Representative Claim

1. A multi-core processor comprising:
a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and
power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

Claim 1 of '080 Patent

Claim 1 is representative. Claims 9 and 17 are also independent claims disclosing generally the same concept of a multi-core processor management scheme having:

- A **multi-core processor** with a first plurality of (high-power) cores and second plurality of (low-power) cores that support the same instruction set
- **Power management hardware** to disable the first plurality of (high-power) cores
- An **operating system to monitor demand** and to control the power management hardware based on the demand

Invalidity overview



Claims 1-4, 7-12, 15-20, 23, and 24	Claims 5, 6, 13, 14, 21, and 22	Claims 7, 15, and 23
Sutardja (Ex-1007 incorporating Ex-1008)	Sutardja in view of Rychlik (Ex-1007 in view of Ex-1009)	Sutardja in view of Carmack (Ex-1007 in view of Ex-1006)
Mathieson in view of Sutardja (Ex-1005 incorporating Ex-1006 in view of Ex-1007)	Mathieson in view of Sutardja and in view of Rychlik (Ex-1005 in view of Ex-1007 and in view of Ex-1009)	

Overview of Sutardja

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Mercedes EX1039
Mercedes-Benz USA, LLC
v. Daedalus Prime LLC
IPR2023-01333

Sutardja Overview



United States
Patent Application Publication
Sutardja et al.

(30) Pub. No.: **US 2008/0288748 A1**
 (43) Pub. Date: **Nov. 20, 2008**

(54) **DYNAMIC CORE SWITCHING**

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(21) Appl. No.: **12/215,760**
 (22) Filed: **Jun. 30, 2008**

Related U.S. Application Data

(63) Continuation of application No. 12/145,660, filed on Jun. 25, 2008, which is a continuation-in-part of application No. 11/523,996, filed on Sep. 20, 2006.

(60) Provisional application No. 60/968,143, filed on Aug. 27, 2007; provisional application No. 60/978,936, filed on Oct. 10, 2007; provisional application No. 60/981,696, filed on Oct. 22, 2007; provisional application No. 61/022,431, filed on Jan. 21, 2008; provisional application No. 61/029,476, filed on Feb. 18, 2008; provisional application No. 61/049,041, filed on Mar. 14, 2008.

Publication Classification

(51) Int. Cl. **G06F 15/00** (2006.01)
G06F 9/00 (2006.01)
 (52) U.S. Cl. **712/28; 712/199.001**
 (57) **ABSTRACT**

A core switching system includes a mode switching module that receives a switch signal to switch operation between a first mode and a second mode. During the first mode, instructions associated with applications are executed by a first asymmetric core, and a second asymmetric core is inactive. During the second mode, the instructions are executed by the second asymmetric core, and the first asymmetric core is inactive. A core activation module stops processing of the applications by the first asymmetric core after interrupts are disabled. A state transfer module transfers a state of the first asymmetric core to the second asymmetric core. The core activation module allows the second asymmetric core to resume execution of the instructions and the interrupts are enabled.

Sutardja discloses a multi-core processor with high-power and low-power cores, wherein power management hardware disables the high-power cores based on an operating system's control.

[0212] According to the present disclosure, both increased power savings and increased performance may be achieved in a mobile device by using a multi-core processing system with a low-speed, low-power (LP) core and a high-speed, high-power (HP) core. The LP core and the HP core may be implemented on the same IC or SOC or as separate ICs that are combined into a system-in-package (SIP). As will be described in further detail below, the multi-core processing system dynamically switches between the LP and HP cores depending on the type of applications being executed, the processing load, and/or other factors described herein.

[0213] Referring now to FIG. 2, the mobile device may include an asymmetric multi-processing (MP) system 10 comprising a LP core 12 and a HP core 16. An instruction set architecture (ISA) of the LP core 12 may differ from the ISA of the HP core 16. For example, the HP core 16 may execute floating point instructions while the LP core 12 may not. Additionally, the LP and HP cores (hereinafter cores) 12 and 16 have different performance and capabilities (e.g., different processing speeds, power consumption, etc.). Alternately, both may use the same ISA's

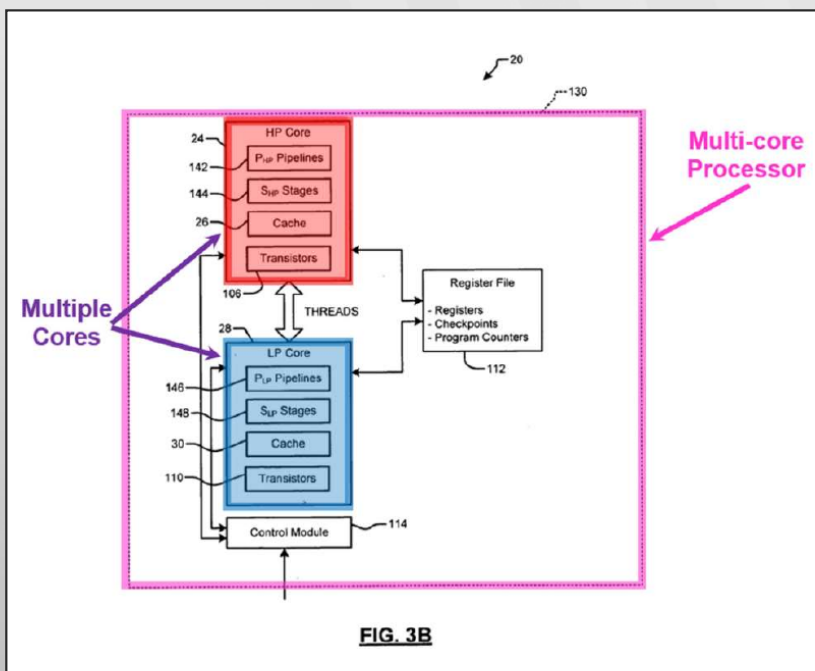
Sutardja Ex-1007 at [0212] and [0213]

[0215] Accordingly, an operating system (OS) and applications can run on both the LP and the HP cores 12 and 16. The asymmetric MP system 10 dynamically switches between the LP and the HP cores 12 and 16 depending on the processing load and the types of applications being executed to increase power savings and improve performance as needed. The asymmetric MP system 10 can be used for general purpose processing (GPP).

[0259] After executing instructions using the HP core 204, system loading may eventually decrease. When the system loading decreases to a predetermined point, the core switching module 212 may transition operation from the HP core 204 back to the LP core 200. As can be appreciated, systems employing core switching may benefit from the low power consumption of the LP core 200 when relatively low processing speed is required. When high speed processing is desired, the HP core 204 can be used and then turned off when the processing load decreases sufficiently.

Sutardja Ex-1007 at [0215] and [0259]

Sutardja Discloses a Multi-Core Processor

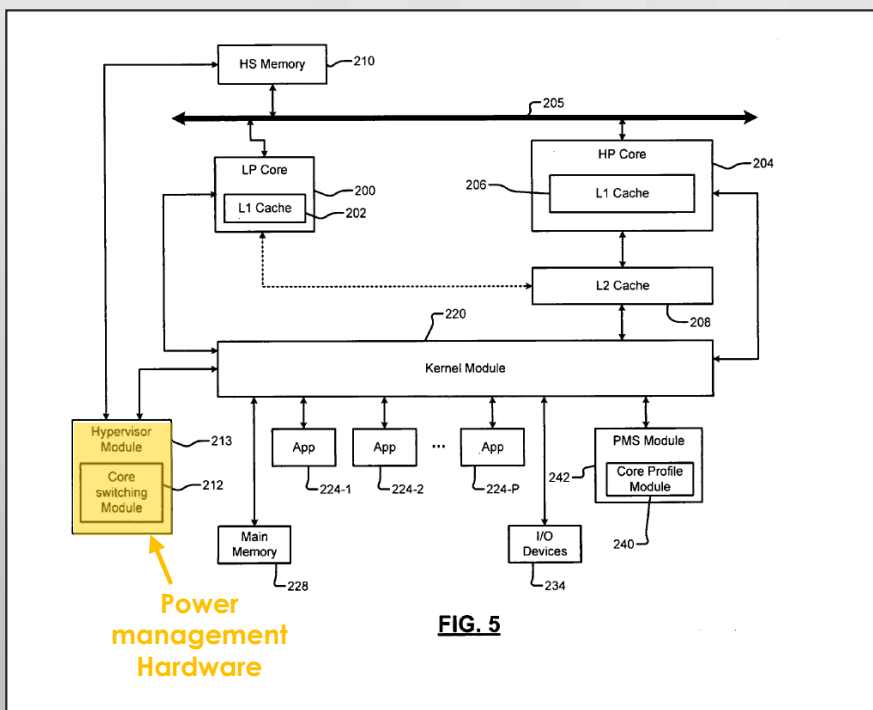


Sutardja Ex-1007 at Fig. 3B (annotated)

[0221] Before a detailed discussion, a brief overview of the figures is presented. FIGS. 3A and 3B show a multi-core processing system having a LP core and a HP core. FIG. 3C shows a control module that switches cores of the multi-core processing system. FIG. 3D shows a core utilization module of the control module. FIG. 4 illustrates a method for operat-

Sutardja Ex-1007 at [0221]

Sutardja Discloses Power Management Hardware (PMH)



Sutardja Ex-1007 at Fig. 5 (annotated)

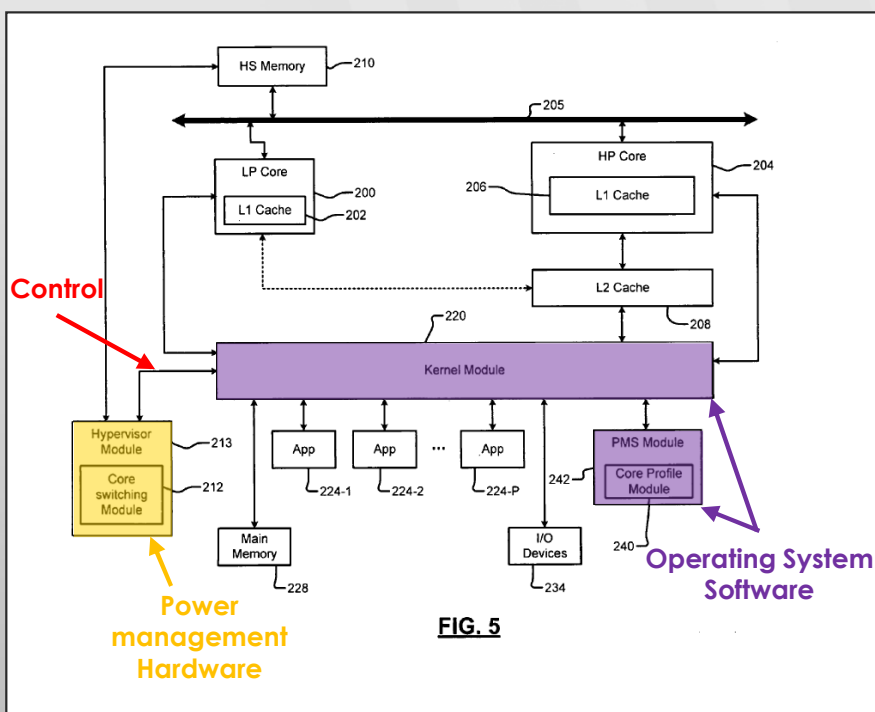
[0253] When the LP core 200 reaches its highest operating speed and additional system loading occurs, the core profile module 240, the PMS module 242, and/or the kernel module 220 disable interrupts and generate a system call to a hypervisor module 213 or a core switching module 212 to trigger a transition. The core switching module 212 may be standalone or may be integrated with the hypervisor module 213. The core switching module 212 may transition (switch) the operation from the LP core 200 to the HP core 204 in response to the system call and return control to the kernel module 220 after the transition (switching) is complete.

Sutardja Ex-1007 at [0253]

[0254] The term hypervisor generally refers to a virtualization platform that allows multiple operating systems to run at the same time on a host computer. The hypervisor may be used to safely suspend operation of one OS while the other OS is operating. The hypervisor typically operates above the kernel. Alternatively, the hypervisor may operate below the kernel.

Sutardja Ex-1007 at [0254]

Sutardja Discloses an Operating System to Control the PMH



Sutardja Ex-1007 at Fig. 5 (annotated)

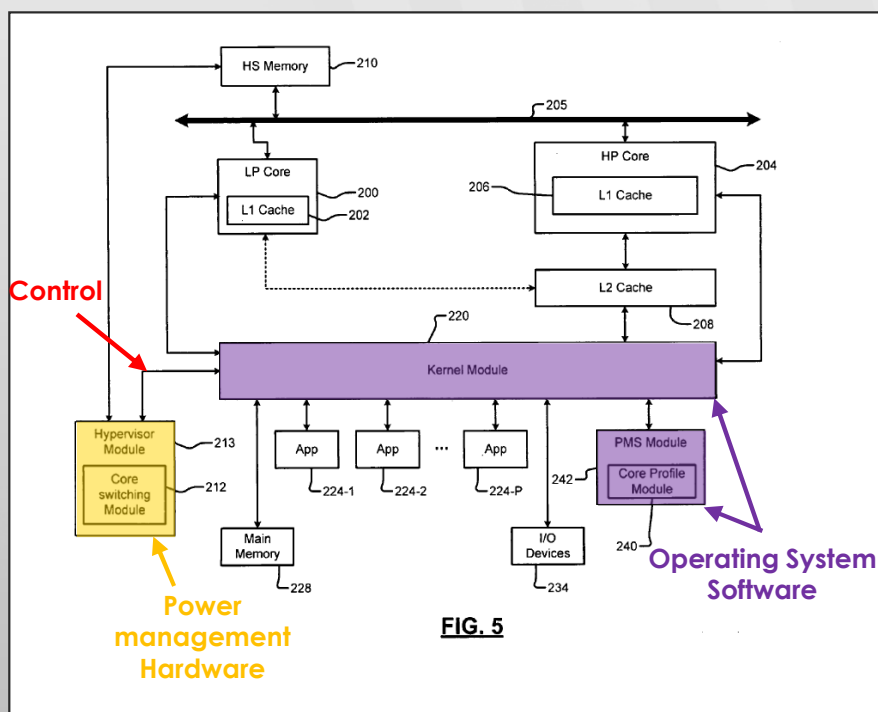
[0249] The LP and HP cores 200 and 204 may execute the same operating system (OS) with different ISAs and can execute the same code. A kernel module 220, which is a component of the OS, manages system resources. For example only, the OS may include Linux® or other suitable operating system. The kernel module 220 provides a lowest level abstraction layer for resources (e.g., the high-speed memory 210 or main memory 228, LP and HP cores 200 and 204, and input/output devices 234) that applications 224 (e.g., applications 224-1, 224-2, . . . and 224-P) control when performing their functions. The kernel module 220 typically provides these resources to processes of the applications 224 through inter-process communication mechanisms and system calls.

Sutardja Ex-1007 at [0249]

[0251] A power management system (PMS) module 242 may be provided to manage power consumption and to initiate or control changes in system operation based on the monitored system loading. A core profile module 240 may monitor system loading such as core loading, input/output loading, application loading, and/or loading based on other system operating parameters.

Sutardja Ex-1007 at [0251]

Sutardja Discloses an Operating System to control the PMH



Sutardja Ex-1007 at Fig. 5 (annotated)

[0253] When the LP core 200 reaches its highest operating speed and additional system loading occurs, the core profile module 240, the PMS module 242, and/or the kernel module 220 disable interrupts and generate a system call to a hypervisor module 213 or a core switching module 212 to trigger a transition. The core switching module 212 may be standalone or may be integrated with the hypervisor module 213. The core switching module 212 may transition (switch) the operation from the LP core 200 to the HP core 204 in response to the system call and return control to the kernel module 220 after the transition (switching) is complete.

Sutardja Ex-1007 at [0253]

Dispute 1 – Whether Sutardja Discloses the Claimed Power Management Hardware

All challenged claims

Sutardja Discloses Power Management Hardware



Patent Owner argues:

Sutardja's core switching module is not "power management hardware." In fact, it is not "hardware" at all.

[Instead,] the core switching module is software.

According to Sutardja, the core switching module in the hypervisor disables all of the HP cores for a drop in demand below a threshold without disabling any of the LP cores:

[0259] After executing instructions using the HP core **204**, system loading may eventually decrease. When the system loading decreases to a predetermined point, the core switching module **212** may transition operation from the HP core **204** back to the LP core **200**. As can be appreciated, systems employing core switching may benefit from the low power consumption of the LP core **200** when relatively low processing speed is required. When high speed processing is desired, the HP core **204** can be used and then turned off when the processing load decreases sufficiently.

Sutardja Ex-1007 at [0259]

Power management hardware is disclosed



Patent Owner argues:

Sutardja's core switching module is not "power management hardware." In fact, it is not "hardware" at all.

[Instead,] the core switching module is software.

But a POSITA would understand:

The claimed "power management hardware" is the hardware **controlled** by Sutardja's core switching module, *i.e.*, the "hypervisor" in which the core switching module is integrated, see Sutardja's ¶[0253]:

transition. The core switching module **212** may be standalone or may be integrated with the hypervisor module **213**. The

Sutardja Ex-1007 at [0253]

The hypervisor can run below the kernel, *i.e.*, below the operating system. Thus, a chip with the hypervisor is hardware as it runs below the lowest software level, *i.e.*, the kernel:

is operating. The hypervisor typically operates above the kernel. Alternatively, the hypervisor may operate below the kernel.

Sutardja Ex-1007 at [0254]

Power management hardware is disclosed



Patent Owner argues:

Sutardja's core switching module is not "power management hardware." In fact, it is not "hardware" at all.

[Instead,] the core switching module is software.

Dr. Horst explains in ¶117 of his declaration that a hypervisor below the kernel is installed directly on the hardware:

117. Sutardja teaches that the hypervisor may "operate[] above the kernel" or it "may operate below the kernel." Ex-1007 (Sutardja '748), ¶254. Because the kernel is the lowest level of the operating system, a POSITA would have understood that a hypervisor that "operate[s] below the kernel" is installed directly on the underlying hardware. Ex-1007 (Sutardja '748), ¶¶249, 254. For example, as explained in *Enabling the New Era of Cloud Computing: Data Security, Transfer, and Management*:

Decl. of Horst Ex-1034 at ¶117

Power management hardware is disclosed



Patent Owner argues:

Sutardja's core switching module is not "power management hardware." In fact, it is not "hardware" at all.

[Instead,] the core switching module is software.

Patent Owner suggests that the core switching module is software because "[h]ardware cannot be 'loaded into high speed memory from RAM or another storage device.'"

But Sutardja discloses this merely as an alternative.

[0256] Depending on whether the core switching module 212 is integrated in the hypervisor module 213, the hypervisor module 213 or the core switching module 212 is loaded into the high-speed memory 210 from RAM or other storage after boot up. The core switching module 212 switches cores in a trusted zone. The PMS module 242 disables interrupts to one of the LP and HP cores 200 and 204 when operation of one core is suspended and handed over to another core. The hypervisor module 213 and/or the core switching module 212 provide hardware abstraction by isolating the cores from the OS and applications and make switching cores transparent to the OS and applications.

Sutardja at ¶256

Power management hardware is disclosed



The Petitioner's position has not changed but remained constant:

runs inside the operating system"). A POSITA would have understood that the hardware on which the disclosed hypervisor is installed corresponds to the claimed power management hardware. Ex-1034, ¶118.

Pet. at 33-34

Turning to the latter argument first, as noted in the Petition, Sutardja's "power management hardware" is the "hardware controlled by the core switching module," i.e. the "hypervisor" in which the "core switching module" can be integrated. Petition, 32-33; POR, 24; see, e.g. Sutardja, [0271-72].

Pet. Reply at 3

Power management hardware is disclosed



- It should be noted that the '080 Patent itself does not strictly differentiate between “software” and “hardware”.
- For example, the '080 patent discloses in 4:47-53; 5:59-63 that “software” or “firmware” is an alternative for “hardware” accomplishing the same function.

FIG. 6 shows a power management process flow that can be executed, for example, with power management software that is running on the multi-processor (or another multi-processor or separate controller, etc.). Conversely, the power management process flow of FIG. 6 can be executed entirely in hardware on the multi-processor or by some combination of such hardware and software.

'080 Patent at 4:47-53

necessary. In various alternate implementations: 1) the hardware/machine readable firmware can monitor and control the core mix; or, 2) the hardware can relinquish control to the Operating system and let it monitor the demand and control the core mix.

'080 Patent at 5:59-63

Power management hardware is disclosed



- Further, a POSITA knows that hardware, such as a chip, may include software components, such as firmware and microcode, but it remains hardware.
- Thus, a POSITA reading Sutardja understands that the core switching module could be implemented on the bare metal hypervisor, which (together with its chip) is hardware.
- Patent Owner's experts agrees that a chip with microcode is hardware:

Q. Yeah. I don't think that you actually answered my question there.

I'm asking that if a manufacturer of a microprocessor had implemented part of the microprocessor with, say, microcode, is that microcode on hardware?

MR. FAHMI: Objection; form.

THE WITNESS: I guess I would say in this example within the -- for lack of a better term the box that's the microprocessor, the microcode is in the processor.

Brogioli Depo. (Ex-1038) at 51:21-52:4

Power management hardware is disclosed



Patent Owner argues:

Sutardja's core switching module is not "power management hardware." In fact, it is not "hardware" at all.

[Instead,] the core switching module is software.

Patent Owner's own citations show that a POSITA would understand hypervisor can run directly on the hardware.

Ex-1028 at 54

machine, that even if the physical machine that runs multiple virtual machines has failed all together, the virtual machines can be failed over to other physical machines immediately. (EMC Corporation, Cloud computing foundations)

Hypervisor

The hypervisor is a software that does server virtualization. It enables multiple operating systems to run concurrently on a physical host computer, and to interact directly with the physical resources of the host computer. Hypervisor provides the attributes for the physical server that lies underneath the virtualized machines, running different operating systems. Hypervisor is the primary component of virtualization that enables computer system to partition hardware resources, such as CPU and memory, into virtualized resources.

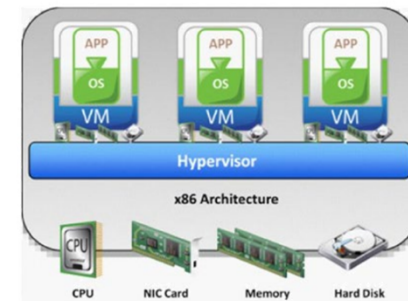
Hypervisor has two components: the kernel and the virtual machine manager. The kernel works as the operating system, handling such tasks as process creation, file system management,

resources scheduling, IO stack etc. The virtual machine monitor (VMM), which resides below the operating system layer, is responsible for handling and sending the virtual machines' requests, also executing commands. When a virtual machine is created, resources such CPU, memory and I/O devices are assigned to the virtual machine. To execute processes, these resources need to be managed according to a time schedule on the physical machine. The VMM handles these requests and communications from the virtual level down to the physical level. The VMM's job also includes allocating and managing the system processor, memory, IO devices and other hardware resources that correspond to each individual virtual machine. When a virtual machine starts running, the controls are transferred to the VMM.

There are chiefly two kinds of Hypervisor: the bare-metal hypervisor and the hosted hypervisor.

- For the bare-Metal hypervisor, the hypervisor runs directly on the hardware. The Hypervisor itself functions as an operat-

Figure 1. Bare-Metal Hypervisor
(EMC Corporation - Virtualized data center and cloud infrastructure)



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Power management hardware is disclosed



Patent Owner argues:

Sutardja's core switching module is not "power management hardware." In fact, it is not "hardware" at all.

[Instead,] the core switching module is software.

But a POSITA would understand:

Sutardja explicitly states in ¶[0209] that "modules" – like the core switching module – are ASICs or electronic circuits, i.e., hardware:

[0209] As used herein, the term module refers to an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor or core (shared, dedicated, or group) and memory that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality.

Sutardja Ex-1007 at [0209]

Power management hardware is disclosed



Patent Owner's expert admits that ASICs are hardware:

14	Q. Is an ASIC hardware?
15	A. If I've designed an ASIC and gone and
16	fabricated it into a, you know, 32-nanometer part or
17	something like that, I would generally consider that
18	hardware.

Brogioli Depo. (Ex-1038) at 11:14-18

18	Q. ASIC's a hardware, though, correct?
19	A. I would say generally yes, when someone thinks
20	of ASICs you think of custom circuits that do specific
21	things.

Brogioli Depo. (Ex-1038) at 27:18-21

Thus, Sutardja discloses that the core switching **module** is, in fact, hardware.

Dispute 2 – Whether Sutardja Discloses an Operating System Controlling Hardware

All Challenged Claims

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The operating system controls the hardware



Patent Owner argues:

According to the Patent Owner, “the operating system of Sutardja does not control [the] hardware” and “the kernel and the PMS module only make system calls to the core switching module.”

But a POSITA understands:

Sutardja discloses that the PMS module **and/or kernel module** of the operating system sends “system calls” to the “hypervisor module 213” or the “core switching module 212”, which in triggers a transition in the cores. Thus, the operating system triggers and thereby controls the hardware. Thus, triggering is **causal** for switching:

[0253] When the LP core 200 reaches its highest operating speed and additional system loading occurs, the core profile module 240, the PMS module 242, and/or the kernel module 220 disable interrupts and generate a system call to a hypervisor module 213 or a core switching module 212 to trigger a transition. The core switching module 212 may be standalone or may be integrated with the hypervisor module 213. The core switching module 212 may transition (switch) the operation from the LP core 200 to the HP core 204 in response to the system call and return control to the kernel module 220 after the transition (switching) is complete.

Sutardja Ex-1007 at [0253]

The operating system controls the hardware



Patent Owner argues:

According to the Patent Owner, “the operating system of Sutardja does not control [the] hardware” and “the kernel and the PMS module only make system calls to the core switching module.”

Fig. 5 of Sutardja shows that the Kernel module (i.e., the OS) controls the hypervisor/core switching module:

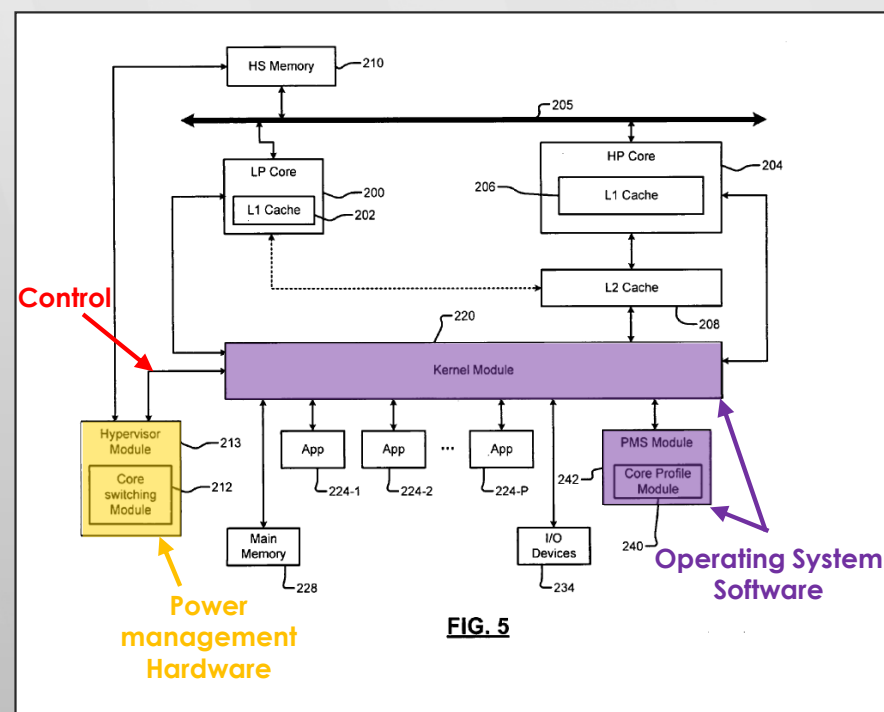


FIG. 5

Sutardja Ex-1007 at Fig. 5 (annotated)

“Return control” does not negate the OS’s control



Patent Owner argues:

“The fact that control must be returned to the kernel ... after switching from one core to another means the operating system was not in control of that switching; i.e., not in control of the subject hardware.”

Patent Owner’s interpretation is wrong because Sutardja teaches:

1. That the kernel (i. e., the OS) generates a system call to the hypervisor to trigger the transition. Thus, controls it.
2. The hypervisor performs the transition.
3. After the transition, the hypervisor “returns” the control to the kernel, i.e., confirms the successful transition to the kernel:

[0253] When the LP core 200 reaches its highest operating speed and additional system loading occurs, the core profile module 240, the PMS module 242, and/or the kernel module 220 disable interrupts and generate a system call to a hypervisor module 213 or a core switching module 212 to trigger a transition. The core switching module 212 may be standalone or may be integrated with the hypervisor module 213. The core switching module 212 may transition (switch) the operation from the LP core 200 to the HP core 204 in response to the system call and return control to the kernel module 220 after the transition (switching) is complete.

Sutardja Ex-1007 at [0253]

Overview of Mathieson

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Mathieson Overview



US 20110213950A1

(19) United States
(12) Patent Application Publication
Mathieson et al.

(36) Pub. No.: US 2011/0213950 A1
(43) Pub. Date: Sep. 1, 2011

(54) SYSTEM AND METHOD FOR POWER OPTIMIZATION

(51) Int. Cl. G06F 15/76 (2006.01)
(52) U.S. Cl. 712/230; 712/239; 712/239.002
(57) ABSTRACT

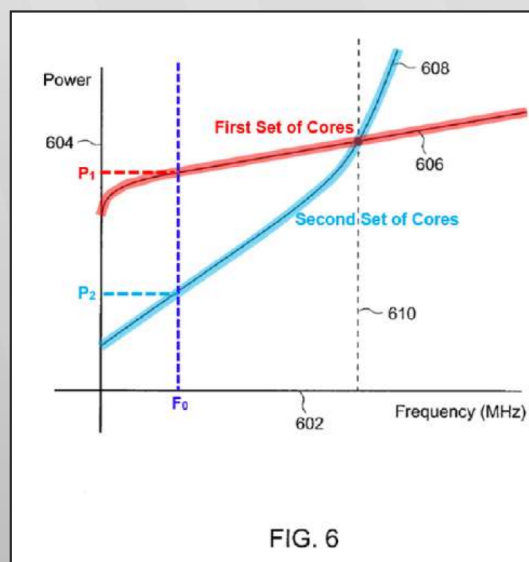
A technique for reducing the power consumption required to execute processing operations. A processing complex, such as a CPU or a GPU, includes a first set of cores comprising one or more fast cores and second set of cores comprising one or more slow cores. A processing mode of the processing complex can switch between a first mode of operation and a second mode of operation based on one or more of the workload characteristics, performance characteristics of the first and second sets of cores, power characteristics of the first and second sets of cores, and operating conditions of the processing complex. A controller causes the processing operations to be executed by either the first set of cores or the second set of cores to achieve the lowest total power consumption.

(76) Inventors: John George Mathieson, San Jose, CA (US); Phil Carmack, Santa Clara, CA (US); Brian Smith, Mountain View, CA (US)

(21) Appl. No.: 12/787,359
(22) Filed: May 15, 2010

Related U.S. Application Data
(63) Continuation-in-part of application No. 12/137,053, filed on Jun. 11, 2008.

Mathieson discloses a multi-core processor with high-power and low-power cores, wherein power management hardware disables the high-power cores based on an operating system's control.



Mathieson at Fig. 6 (annotated)

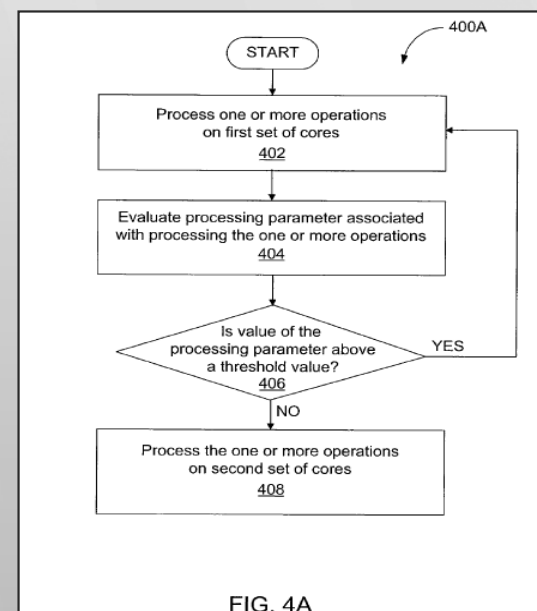
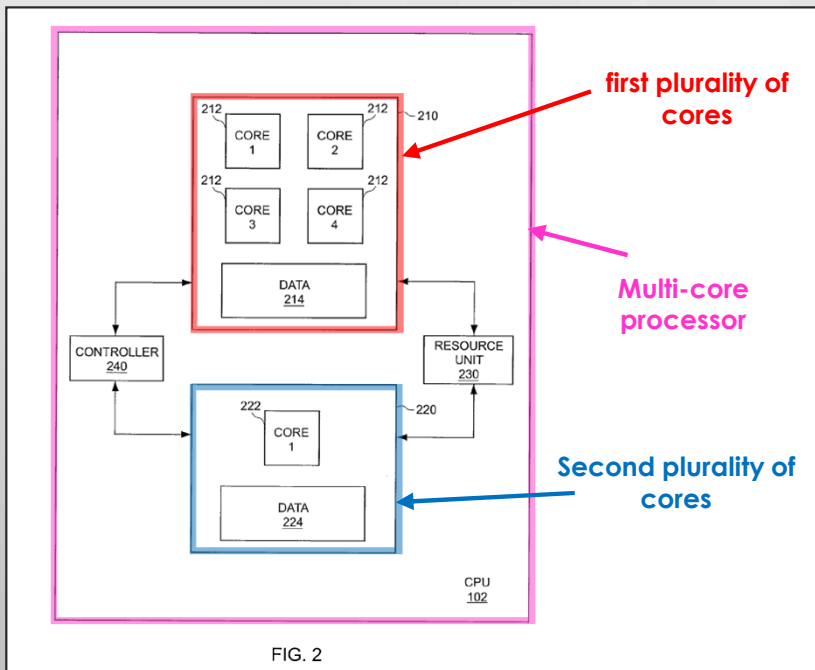


FIG. 4A

Mathieson at Fig. 4A

Mathieson Discloses a Multi-Core Processor



Mathieson at Fig. 2 (annotated)

[0025] The CPU 102 includes a first set of cores 210, a second set of cores 220, a shared resource 230, and a controller 240. Other components included within the CPU 102 are omitted to avoid obscuring embodiments of the invention. In some embodiments, the first set of cores 210 includes one or more cores 212 and data 214, and the second set of cores 220 includes one or more cores 222 and data 224. In some embodiments, the first set of cores 210 and the second set of cores 220 are included on the same chip. In other embodiments, the first set of cores 210 and the second set of cores 220 are included on separate chips that comprise the CPU 102.

Mathieson at [0025]

Mathieson Discloses Power Management Hardware (PMH)

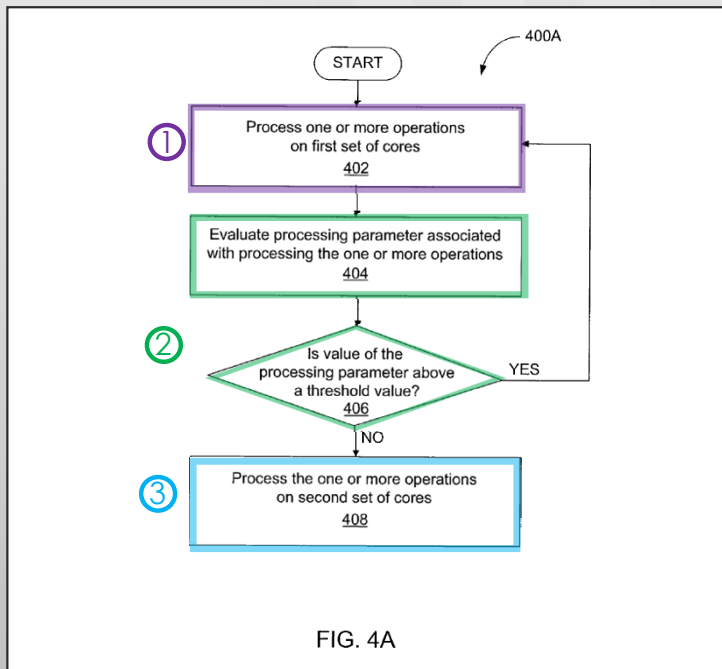


FIG. 4A

Mathieson at Fig. 4A (annotated)

[0043] When execution of the processing operations switches from the first set of cores to the second set of cores, in some embodiments, the controller 240 is configured to transfer the processor state from the first set of cores to the second set of cores. In one embodiment, the controller saves the processor state to the shared resource 230, triggers a hardware mechanism that stops and powers off the first set of cores 210, and boots the second set of cores 220. The second set of cores 220 then restores the processor state from the shared resource 230 and continues operation at the lower speed associated with the second set of cores 220. In other embodiments, the processing state may be stored in any memory unit when transferring execution of the operations between the two sets of cores. In still further embodiments, the processing state may be directly transferred to the other set of cores via a dedicated bus, where the processing state is not stored in any memory unit with switching between the two sets of cores. The transition from the first mode to the second mode, and vice versa, can be done transparently to high level software, such as the operating system.

Mathieson at [0043]

The “hardware mechanism” disclosed is the Power Management Hardware

Mathieson Discloses an Operating System to control the PMH

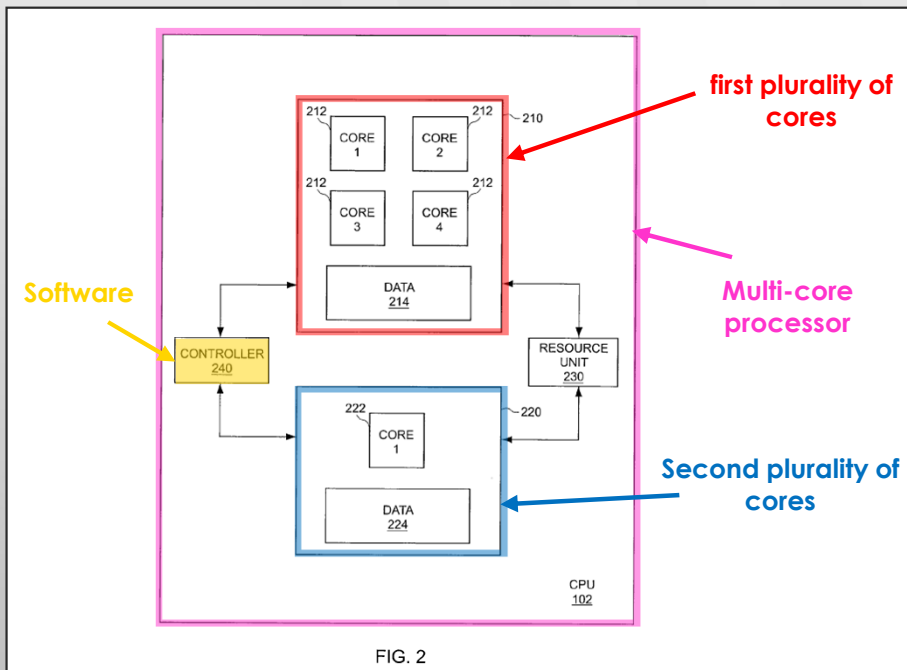


FIG. 2

Mathieson at Fig. 2 (annotated)

[0030] In some embodiments, a controller 240 included within the CPU 102 is configured to evaluate at least a workload associated with one or more operations to be executed by the CPU 102. In some embodiments, the controller is implemented in software and is executed by the CPU 102. Based on the evaluated workload, the controller 240 is able to configure the CPU 102 to operate in a first mode of operation or a second mode of operation. In the first mode of operation, the first set of cores 210 is enabled and operable and the second set of cores 220 is disabled. In the second mode of operation, the second set of cores 220 is enabled and operable and the first set of cores 210 is disabled. In addition, in various embodiments, the controller 240 is able to increase and/or decrease the operating frequency of the first processor and/or the second processor when operating the CPU 102 in each of the first and second modes. In one embodiment, the first set of cores 210 is disabled and powered off when the one or more operations are processed by the second set of cores 220. In alternative embodiments, the first set of cores 210 is clock gated and/or power gated when the one or more operations are processed by the second set of cores 220.

Mathieson at [0030]

Operating System controls PMH with controller 240

Dispute 3 – Whether Mathieson Discloses an Operating System Controlling Hardware

All challenged Claims

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

32

The operating system controls the hardware



Patent Owner argues:

Patent Owner argues that in Mathieson, “the controller does not perform the functions of an operating system in effecting the transition between modes” because it operates “transparently” to the operating system.

But a POSITA is aware:

A kernel of an operating system, i.e., the lowest level of the operating system, operates “transparently” to higher-level applications **within the same operating system**. To which the Patent Owner’s expert agrees:

Q. Earlier I used the word “transparently.” What does that word mean to you with respect to applications?

A. Well, in my declaration I talk about things happening transparently, for example, transparent to an operating system when lower-level things in the system are happening. I don't recall talking about applications in my declaration, but I guess an example might be if I have written an email client that's going and checking my email and there's bad memory cells happening on my solid-state hard drive, the email client generally isn't going to be aware of that. That will be taken care of transparently to the email client.

Brogioli Depo. (Ex-1038) at 31:8-21

The operating system controls the hardware



Patent Owner argues:

Patent Owner argues that in Mathieson, “the controller does not perform the functions of an operating system in effecting the transition between modes” because it operates “transparently” to the operating system.

But a POSITA is aware:

According to Dr. Horst, the kernel is the lowest level of the operating system, and the kernel executes modules which control processes and manage devices within the processor:

management. A POSITA would have understood that an operating system, in general, includes a kernel (the lowest level of the operating system) and one or more modules that the kernel executes to control processes and manage devices within the processor. A POSITA would have recognized that Mathieson’s controller corresponds to a software module that may be included as part of an operating system and executed by a kernel. Thus, at least because a POSITA would have recognized that Mathieson’s controller performs the functions of an operating system, the POSITA would have viewed controller 240 as being part of an operating system executing on CPU 102.

Horst Declaration at ¶217

Dispute 4 – Whether Mathieson teaches that
the second plurality of cores consume less
power than the first plurality of cores

All challenged Claims

The different types of cores consume different amounts of power



Patent Owner argues:

Patent Owner argues that Mathieson does not disclose cores which consume less power for the same “supply voltage,” because core power in Mathieson is described “only on the basis of operating frequency.”

But a POSITA knows:

The frequency of operation for a core is directly proportional to the voltage (i.e., f is proportional to V). Thus, higher frequency leads to higher power consumption:

48. There are two key relationships linking core frequency and voltage to core power consumption. They are: (1) power is proportional to V^2f – where V is the voltage to operate the core, and f is the frequency of operation of the core; and (2) the frequency of operation is directly proportional to the voltage (i.e., f is proportional to V). Thus, higher frequency requires a greater core voltage resulting in the consumption of much more power.⁵

Horst Declaration at ¶48

Thus, Mathieson's low power cores consume less power for the same supply voltage compared to the high-power cores.

Mathieson Discloses Power Management Hardware (PMH)



- Contrary to Patent Owner's assertion, it is not required that Mathieson expressly mentions that the power consumption is a function of the supply voltage as this is a **direct consequence of the underlying physics**.
- As Dr. Horst pointed out, the POSITA is aware of the physical correlations between frequency, voltage, and power.
- Further, the Patent Owner does also not dispute those physical correlations but merely states that Mathieson does "not make the contention".

The different types of cores consume different amounts of power



Patent Owner argues:

Patent Owner argues that Mathieson does not disclose cores which consume less power for the same “supply voltage,” because core power in Mathieson is described “only on the basis of operating frequency.”

Furthermore:

Mathieson discloses using known voltage and frequency scaling techniques (i.e. DVFS), where varying the voltage affects the power consumed.

[0076] In addition, in some embodiments, a controller may be configured to vary the voltage and/or operating frequency of the active cores before the number of active cores is increased or decreased. Any technically feasible technique, such a dynamic voltage and frequency scaling (DVFS), may be implemented to vary the voltage and/or operating frequency of the active cores. Again, according to various embodiments, vary the voltage and/or operating frequency of the active cores may cause the processor to operate at a lower total power consumption, thereby reducing the power required to executing the processing operations.

Mathieson at [0076]

Thus, Mathieson's low power cores consume less power for the same supply voltage compared to the high-power cores.

Other Disputes

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

39

Mercedes EX1039
Mercedes-Benz USA, LLC
v. Daedalus Prime LLC
IPR2023-01333

The level of the POSITA

All Challenged Claims

The level of the POSITA



Patent Owner argues:

The POSITA is a person with two years of experience, because people having “at least” two year of experience would include people with far greater level of experience.

The Patent Owner is incorrect:

- The level of the POSITA is the minimum requirement and not the maximum.
- A POSITA must have at least a certain experience. Persons with more experience are not excluded from being a POSITA.

Claim construction of “operating system”

All Challenged Claims

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

42

No claim construction required for “Operating System”



Patent Owner states:

The term “Operating System” must be construed as “software that controls the allocation and usage of hardware resources.”

No construction needed:

- The Patent Owner’s suggested construction corresponds to its plain and ordinary meaning. Hence, the Patent Owner’s admits that claim construction is not required.

MacOS, Microsoft’s Windows, UNIX, and others. *Id.* at 7:31-35. A person of ordinary skill in the art would thus understand that the term “operating system” is used in the ’080 patent in its conventional sense. Ex. 2006 at ¶ 40.

Patent Owner's Response at 13.

Microsoft’s Windows, UNIX, and others. *Id.* at 7:31-35. Therefore, I conclude that a person of ordinary skill in the art would understand that the term “operating system” is used in the ’080 patent in its conventional sense. Specifically, in the

Brogioli Decl. (Ex-2006) at ¶40

Sutardja '748 was not considered during prosecution

All Challenged Claims

Sutardja was not considered during prosecution



Sutardja was not considered:

- That Sutardja '748 was mentioned in the IDS does not mean that the document was considered during prosecution in the manner presented in this Petition.
- In fact, the prosecution history shows that neither Sutardja '748 nor Sutardja '324 was used to reject any of the independent claims.
- Thus, from the prosecution history it is apparent that neither Sutardja reference was considered in detail.