

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-01333
Patent 10,049,080 B2

Before WILLIAM V. SAINDON, THOMAS L. GIANNETTI, and
GREGG I. ANDERSON, *Administrative Patent Judges*.

GIANNETTI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background

Mercedes-Benz USA, LLC (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–24 (the “challenged claims”) of U.S. Patent No. 10,049,080 B2 (Ex. 1001, the “’080 patent”). Paper 1 (“Pet.”).¹ Daedalus Prime LLC (“Patent Owner”) waived filing of a preliminary response. Paper 9.

We determined that Petitioner established a reasonable likelihood that it would prevail with respect to at least one claim challenged in the Petition. Paper 10 (“Institution Dec.”). We therefore instituted *inter partes* review as to all of the challenged claims of the ’080 patent and all of the asserted grounds of unpatentability. *See SAS Inst. Inc. v Iancu*, 138 S.Ct. 1348, 1356 (2018); 37 C.F.R. § 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”).

Following institution of the trial, Patent Owner filed a Response (Paper 19, “PO Resp.”), Petitioner filed a Reply (Paper 23, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 24, “PO Sur-reply”).

¹ The Petition was accompanied by a “Contingent Motion for Joinder” seeking joinder with IPR2023-00567, a proceeding originally filed by Samsung and Qualcomm involving a challenge to the same claims of the ’080 patent as this proceeding. Paper 2. That proceeding was terminated and the joinder motion was therefore dismissed as moot. Institution Dec. 26–27.

An oral hearing was held on November 13, 2024. A transcript of the hearing is part of the record. Paper 30 (“Hearing Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision issued pursuant to 35 U.S.C. § 318(a). For the reasons we discuss below, we determine that Petitioner has proven by a preponderance of the evidence that all of the challenged claims of the ’080 patent are unpatentable.

B. Related Proceedings

The parties identify the following district court and ITC proceedings that have involved the ’080 patent: (1) *Daedalus Prime LLC v. Arrow Electronics, Inc.*, 1:22-cv-01107 (D. Del.); (2) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01109 (D. Del.); (3) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01108 (D. Del.); (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd.*, 2:22-cv-00352 (E.D. Tex.); (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (USITC); and (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (USITC). Pet. 1–2; Paper 5, 2.

As noted *supra*, the ’080 patent was also the subject of IPR2023-00567, now terminated.

C. Real Parties-in-Interest

Petitioner identifies the following real parties-in-interest: Mercedes-Benz USA, LLC; Mercedes-Benz Intellectual Property GmbH & Co. KG; Mercedes-Benz Group AG; and Mercedes-Benz AG. Pet. 1. Patent Owner

identifies itself, Daedalus Prime LLC, as the real party-in-interest. Paper 5, 2.

D. The '080 Patent

The '080 patent is titled “Asymmetric Performance Multicore Architecture with Same Instruction Set Architecture.” Ex. 1001, (54). The patent relates to multi-core processors in computing systems and methods of managing power in multi-core processors. *Id.* at 1:16–20; 2:30–42; 3:50–4:19. More specifically, the patent relates to asymmetric multi-core computer architectures with the cores having the same instruction set architecture. *Id.* at 1:16–20.²

According to the '080 patent, typically power management schemes for computer systems scale up processing performance as the system's workload increases and scale down processing performance as the system's workload decreases. *Id.* at 2:22–26. Scaling process performance with workload is usually accomplished by enabling or disabling entire cores and raising or lowering core supply voltages and operating frequencies in response to workload. *Id.* at 2:30–33. For example, all cores are enabled under a maximum performance/power consumption state, and only one core is enabled under a minimum performance/power consumption state. *Id.* at 2:33–41; *see also id.* Fig. 2.

The '080 patent explains that some prior art multi-core processor power management schemes have been implemented on processors whose

² “An asymmetric multicore processor (AMP) includes cores exposing the same instruction-set architecture, but differing in features, size, speed and power consumption.” Ex. 1025, 1 (citations omitted).

constituent cores are identical, while others have been implemented on processors in which the cores are radically different from each other (i.e., asymmetric). Ex. 1001, 3:34–39. For example, a processor with cores that are different from each other may have a low power core that lacks sizeable “chunks” of logic circuitry responsible for executing the program code instructions compared to the other cores in the processor and supports a reduced instruction set. *Id.* at 3:39–46. However, processors with cores that are different from each other can suffer from drawbacks because it is difficult for system software to adjust switch operation between processor cores having different instruction sets. *Id.* at 3:46–49.

The '080 patent purports to address this issue by disclosing multi-core processors in which at least one of the cores is designed to be lower performance and therefore consumes less power than other cores in the processor. *Id.* at 3:50–4:9. According to the '080 patent, the lower power cores have the same logic design as the higher power cores and support the same instruction set, but consume less power by having narrower drive transistor widths than the higher power cores or other power consumption-related design features. *Id.* at 3:50–62.

The '080 patent explains that the lower power core allows the multi-processor “to entertain a power management strategy that is the same/similar to already existing power management strategies, yet, still achieve an even lower power consumption in the lower/lowest performance/power states.” *Id.* at 4:20–46; *see also id.* Fig. 5. The process begins with a multi-core processor in which multiple high power cores and at least one low power core are operating. *Id.* Fig. 6 (610), 4:54–56. When the demand on the processor drops below a threshold, a high power core is disabled. *Id.* at

4:56–64. This process is repeated with the enabled high power cores each time demand reaches a lower threshold. *Id.* at 4:65–5:6. When all of the high power cores are disabled and the demand on the processor continues to drop, the low power cores are disabled one by one in the same manner until only one low power core is enabled and the lower-power state is reached. *Id.* at 5:25–35.

E. Illustrative Claim

The Petition challenges claims 1–24, of which claims 1, 9, and 17 are independent. Claim 1 is illustrative of the claimed subject matter and is reproduced below:³

1. [preamble] A multi-core processor comprising:
 - [a][i] a first plurality of cores and a second plurality of cores that support a same instruction set,
 - [a][ii] wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and
 - [b][i] power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,
 - [b][ii] wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

Ex. 1001, 7:56–8:3.

³ Paragraph labeling in brackets is based on labeling provided by Petitioner.

Independent claim 9 is directed to a method of operating a multi-core processor. Ex. 1001, 8:38–53. Independent claim 17 is directed to “[a] non-transitory machine readable medium containing program code” that causes the method of claim 9 to be performed. *Id.* at 9:24–41.

F. References and Other Evidence

The Petition relies on the following references:

Name	Reference	Publication Date	Exhibit(s)
Sutardja ’748 ⁴	US 2008/0288748 A1	Nov. 20, 2008	Ex. 1007
Sutardja ’785	US 2007/0083785 A1	Apr. 12, 2007	Ex. 1008
Carmack	US 2009/0309243 A1	Dec. 17, 2009	Ex. 1006
Rychlik	US 2011/0145615 A1	June 16, 2011	Ex. 1009
Mathieson ⁵	US 2011/0213950 A1	Sept. 1, 2011	Ex. 1005

In addition, Petitioner submits the Declaration of Dr. Robert Horst. Ex. 1034 (“Horst Decl.”). In his declaration, Dr. Horst incorporates the analysis and conclusions of Dr. Trevor Mudge (Ex. 1002), who served as the petitioners’ expert in IPR2023-00567. Horst Decl. ¶ 3. Patent Owner submits the Declaration of Michael C. Brogioli, Ph.D. Ex. 2006 (“Brogioli

⁴ Sutardja ’748 incorporates by reference the disclosure of Sutardja ’785 (Ex. 1008) in its entirety. *See* Ex. 1007, 1:8–12.

⁵ Petitioner represents that Mathieson incorporates by reference the disclosure of Carmack in its entirety. Pet. 5 n.5; *see also id.* at 18.

Decl.”). The parties have also submitted deposition transcripts for Dr. Horst and Dr. Brogioli.⁶

G. Asserted Grounds of Unpatentability

Petitioner asserts the challenged claims are unpatentable on the following grounds (Pet. 5–6):

Claims Challenged	35 U.S.C. §⁷	References
1–4, 7–12, 15–20, 23, 24	103	Sutardja ⁸
5, 6, 13, 14, 21, 22	103	Sutardja, Rychlik
7, 15, 23	103	Sutardja, Carmack
1–4, 7–12, 15–20, 23, 24	103	Mathieson, ⁹ Sutardja
5, 6, 13, 14, 21, 22	103	Mathieson, Sutardja, Rychlik

⁶ Ex. 1038 (“Brogioli Dep.”); Ex. 2002 (“Horst Dep.”).

⁷ Because the earliest application from which the ’080 patent claims priority was filed before March 16, 2013, the pre-AIA (“America Invents Act”) version of § 103 applies. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011).

⁸ Petitioner states that it relies on Sutardja ’748 and Sutardja ’785, combined, “as a single reference obviousness ground.” Pet. 5 n.4. Petitioner therefore refers to the combined references as “combined Sutardja” or just “Sutardja.” *See id.*; Horst Decl. ¶ 36 n.2.

⁹ References to Mathieson in this ground refer to Mathieson and Carmack (incorporated by reference into Mathieson). Pet. 5 n.5.

H. Overview of the Prior Art

1. Sutardja '748 (Ex. 1007)

Sutardja '748 is titled "Dynamic Core Switching." Ex. 1007, (54). Sutardja '748 relates to dynamically switching cores of multi-core processing systems for mobile computing devices. *Id.* ¶ 2. Sutardja '748 explains that processor systems in such computing devices may be asymmetric. *Id.* ¶ 7, Fig. 1A.

Sutardja '748 discloses obtaining increased power savings by using a multi-core processing system with a low-speed, low-power (LP) core and a high-speed, high-power (HP) core. *Id.* ¶¶ 212. The instruction set architecture (ISA) of the LP core may differ from the ISA of the HP core, or alternatively, both may use the same ISAs. *Id.* ¶ 213.

Sutardja '748 discloses using "core morphing" to optimize power consumption and improve performance. *Id.* ¶ 216. In core morphing, cores are dynamically enabled (i.e., activated) or disabled (i.e., deactivated) based on the system load. *Id.* ¶ 218. When one core is active, other cores may be disabled (i.e., deactivated) to save power. *Id.* For example, the other cores may be put in a standby mode, where the clock frequency and/or the supply voltage of the other cores may be decreased to values that are lower than when the cores are active. *Id.* Alternatively, the other cores may be completely shut down by disconnecting the power supply to the cores. *Id.*

Sutardja '748 discloses that "[c]ore morphing may be used in multi-core systems comprising one LP core and one HP core." *Id.* ¶ 219. "When applications demand still higher performance than that provided by one HP core, multiple HP cores may be used." *Id.* In the HP mode, the HP core is in the active state and processes threads. *Id.* ¶ 223. The LP core may also

operate during the HP mode. In other words, the LP core may be in the active state during all or part of the HP mode. *Id.* Sutardja '748 discloses that core morphing is useful for optimizing battery life and performance of mobile devices. *Id.* ¶¶ 217, 222.

2. Sutardja '785 (Ex. 1008)

Sutardja '785 is titled "System with High Power and Low Power Processors and Thread Transfer." Ex. 1008, (54). Sutardja '785 and Sutardja '748 are related in that the application for Sutardja '785, U.S. Patent Application No. 11/523,996 (the "'996 application"), is the grandparent (through a continuation and continuation in part) of the application for Sutardja '748. *Id.* (21).¹⁰ As previously noted, the entirety of the Sutardja '785 disclosure is incorporated by reference into Sutardja '748. *See supra*, Section I.F.

Sutardja '785 relates to low power data storage systems. *Id.* ¶ 3. Sutardja '785 discloses a computing device with a system on chip ("SOC") that includes first and second processors. *Id.* ¶ 9. The first processor implemented by the SOC has active and inactive states and processes first and second sets of threads during the active state. *Id.* The second processor implemented by the SOC also has active and inactive states. *Id.* Sutardja '785 explains that the second processor consumes less power when

¹⁰ Sutardja '748 is a publication of U.S. Patent Application No. 12/215,760, which is a continuation of U.S. Patent Application No. 12/145,660, which is a continuation-in-part of the '996 application. Ex. 1007, (21), (63).

operating in its active state than the first processor when operating in its active state. *Id.*

A control module implemented by the SOC communicates with the first and second processors and selectively transfers the second set of threads from the first processor to the second processor for processing and selects the inactive state of the first processor. *Id.*

3. Rychlik (Ex. 1009)

Rychlik is titled “System and Method for Controlling Central Processing Unit Power Based on Inferred Workload Parallelism.” Ex. 1009, (54). Rychlik discloses portable computing devices with multiple cores and methods of controlling power in such devices. *Id.* ¶¶ 3–4, 26–30. Rychlik discloses a computing device that includes an operating system with a scheduler that schedules tasks, threads, or a combination of the two for execution within the cores, a parallelism monitor that tracks the workload on the cores, and a controller that controls the power to the cores (i.e., powers them on or off). *Id.* ¶¶ 35–38. When the workload on the cores meets or exceeds a threshold value, the controller may wake up another core, and when the workload on the cores falls below a threshold value, the controller may power off or put a core into standby mode. *Id.* ¶¶ 39–40, 88, 95–96. According to Rychlik, this process can reduce power consumption. *Id.* ¶¶ 4, 95, 97.

4. Carmack (Ex. 1006)

Carmack is titled “Multi-core Integrated Circuits Having Asymmetric Performance Between Cores.” Ex. 1006, (54). Carmack discloses a multi-core integrated circuit with asymmetric cores that are each capable of

implementing substantially all the functionality of the integrated circuit. *Id.* Abstract, ¶ 3. Carmack specifies that the cores may have the same hardware design, but different component device designs such that the first core may be implemented using a high threshold voltage transistor with a lower leakage current, and the second core may be implemented using a low threshold voltage transistor with a lower switching delay and lower supply voltage. *Id.* ¶ 15.

Carmack also describes methods of controlling cores based on performance parameters such as workload, operating frequency, power consumption, quality of service, or operating temperature. *Id.* Abstract, ¶¶ 13, 21. Carmack explains that a core control circuit determines which one or more of the cores to use based on the performance parameters and then utilizes a first core and idles a second core if a performance parameter is within a first range, and utilizes a second core and idles a first core if a performance parameter is within a second range. *Id.* Abstract, ¶¶ 3–5, 23–25. A particular core may be idled by turning off its power rail, internally gating its power rail, back biasing its substrate, or gating its clock. *Id.* ¶ 16.

5. Mathieson (Ex. 1005)

Mathieson is titled “System and Method for Power Optimization.” Ex. 1005, (54). Mathieson is a continuation-in-part of U.S. Patent Application No. 12/137,053 (“the ’053 application”) and incorporates its disclosures. *Id.* (63), ¶ 1. Carmack issued from the ’053 application. Ex. 1006, (21).

Mathieson discloses a system and method for power optimization. *Id.* ¶ 3. Mathieson discloses a method for optimizing power in a multi-core

processing complex that includes a first set of cores comprising one or more fast cores, a second set of cores comprising one or more slow cores, and a controller that determines which mode of operation is more power efficient and causes processing operations to be executed by the first set of cores or the second set of cores to achieve the lowest total power consumption. Ex. 1005, Abstract, ¶¶ 20, 28, 38.

Mathieson explains that a controller within the CPU switches between a first mode of operation and a second mode of operation based on workload characteristics, performance characteristics of the cores, power characteristics of the cores, and operating conditions of the processing complex. *Id.* Abstract, ¶¶ 8–10, 25, 30, Fig. 2. Mathieson discloses that “[i]n the first mode of operation, the first set of cores is enabled and operable and the second set of cores is disabled,” and “[i]n the second mode of operation, the second set of cores is enabled and operable and the first set of cores is disabled.” *Id.* ¶ 30 (reference numbers omitted).

The method begins when a processor’s controller directs one or more operations to be executed by a first set of cores. *Id.* ¶ 55, Fig. 4A. Next, the controller evaluates a processing parameter associated with processing the operations, such as a processing frequency or instruction throughput, and determines whether the parameter is above a threshold value. *Id.* ¶¶ 55–56. If the parameter exceeds the threshold, the processor continues processing operations using the first set of cores. *Id.* If the parameter is not above the threshold value, the controller directs one or more operations to be executed by a second set of cores. *Id.*

II. ANALYSIS OF THE CHALLENGED CLAIMS

A. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art of the '080 patent would have possessed “a bachelor’s degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field” and would have had “at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.” Pet. 14–15 (citing Horst Decl. ¶ 31).

As noted, Patent Owner expressly waived filing a preliminary response. Paper 9. At the institution stage, therefore, Patent Owner did not dispute Petitioner’s description of a person of ordinary skill in the art or provide its own description.

We regarded Petitioner’s description as consistent with the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Thus, for the purpose of our Institution Decision, we adopted Petitioner’s proposal. Institution Dec. 14–15.

In its Response, Patent Owner takes exception to our definition as “flawed insofar as it encompasses people with more than ordinary skill in the art.” PO Resp. 12. Patent Owner explains that “by encompassing people with ‘at least’ two years of experience in the designated field, it includes persons with far greater levels of experience and, therefore, is not limited to just persons of *ordinary skill* in the art.” *Id.*

This subject was explored at the oral argument. Hearing Tr. 33:22–34:16; 37:17–39:1. Patent Owner’s counsel initially asserted that we should “throw out all of the testimony” of Petitioner’s expert, Dr. Horst, because of the “flawed” definition. *Id.* at 38:18–22.

We decline to “throw out” Dr. Horst’s testimony for several reasons. First and foremost, Patent Owner has not moved or otherwise sought to exclude his testimony, or even filed an objection. Hearing Tr. 46:19–47:1. Thus, the issue of whether the testimony should be excluded is not properly before us. Further, Petitioner asserts that “[t]his distinction is irrelevant.” Pet. Reply 2. We agree. Patent Owner has not pointed to any opinion by Dr. Horst that turns on the alleged “flaw” in the definition of the person of ordinary skill. *Id.* at 46:19–48:3. Finally, there is no prejudice. Patent Owner’s expert used the definition proposed by Patent Owner in his analysis. *See Brogioli Decl.* ¶ 25. Nor could Patent Owner show us with specificity any place in the record where resolving this dispute would make a difference in this case. Hearing Tr. 46:3–47:3.

For the reasons given, we do not see the need to modify our definition of a person of ordinary skill or to exclude or give little weight to Dr. Horst’s opinions.

B. Claim Construction

We construe claim terms only as relevant to the parties’ contentions and only to the extent necessary to resolve the issues in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Prior to institution, neither party proposed claim constructions for our consideration. Petitioner contended that it “does not believe that any term requires explicit construction.” Pet. 15 (citing Horst Decl. ¶¶ 84–85). Patent Owner filed no preliminary response, and thus did not dispute Petitioner’s position or address claim construction. We determined there were no claim terms that needed to be construed at institution. Institution Dec. 15.

Post-institution, Patent Owner proposes a construction for the term “operating system.” PO Resp. 12–13. Relying on the Microsoft Computer Dictionary, Patent Owner contends that “[a]n ‘operating system’ is, and would be understood by a person of ordinary skill in the art to be, ‘The software that controls the allocation and usage of hardware resources such as memory, central processing unit (CPU) time, disk space, and peripheral devices.’” PO Resp. 13 (citing Ex. 2007, 378). Dr. Brogioli’s testimony generally supports this construction, as does Dr. Horst’s. *See* Brogioli Dep. 8:17–22; Horst Dep. 32:3–8. Petitioner responds that the term “should be understood in accordance with its plain meaning,” and therefore does not require construction, but does not dispute Patent Owner’s proposed construction. Pet. Reply 2.

For the reasons given, we adopt Patent Owner’s construction for “operating system.” However, we do not see this construction as dispositive of the central issue of whether the operating system in Sutardja controls the transition of the cores. *See* Section II.D.1, *infra*.

C. Obviousness

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that

the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called “secondary considerations,” including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Neither party has presented any evidence on the fourth *Graham* factor.

D. Obviousness of Claims 1–4, 7–12, 15–20, 23, and 24 Based on Sutardja

Petitioner asserts that these claims would have been obvious in light of Sutardja. Pet. 21. Petitioner contends Sutardja teaches or suggests each element of claims 1–4, 7–12, 15–20, 23, and 24 and provides an element-by-element analysis for each claim, supported by expert testimony from Dr. Horst. *Id.* at 21–45; Horst Decl. ¶¶ 86–160.

Patent Owner and its expert Dr. Brogioli disagree with this analysis. PO Resp. 20–28; Brogioli Decl. ¶¶ 41–52. Patent Owner contends that Sutardja fails to disclose sufficiently the “operating system” limitation in the challenged claims: “wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.” PO Resp. 20–28; Brogioli Decl. ¶¶ 44–52. This limitation appears in independent

claim 1 and in each of the other independent claims. *See* Ex. 1001, 7:66–8:3 (claim 1), 8:49–53 (claim 9), 9:37–41 (claim 17).

Upon consideration of Petitioner’s explanations and supporting evidence in this record and Patent Owner’s arguments and supporting evidence, we are persuaded for the reasons that follow that Petitioner has demonstrated by a preponderance of the evidence that independent claims 1, 9, and 17 and their dependent claims 2–4, 7, 8, 10–12, 15, 16, 18–20, 23, and 24 would have been obvious in light of Sutardja. Pet. 21–45.

Our analysis focuses on claim element [1][b][ii] (“wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.”). *See supra*, Section I.E. As we discussed *supra*, independent claims 7, 9, and 17 contain recitations that are similar, if not identical, to disputed “operating system” element [1][b][ii]. The dispositive issue discussed *infra*, therefore, is whether Sutardja discloses the “operating system” limitation as recited in claim 1 and the other independent claims.

1. Independent Claim 1

Petitioner asserts that each element of claim 1 is disclosed by Sutardja and provides an element-by-element analysis. Pet. 22–35; Horst Decl. ¶¶ 86–124. In our Institution Decision, we discussed each of those contentions. *See* Institution Dec. 16–20. We summarize them below.

a. Preamble: *A multi-core processor comprising*

Petitioner contends that Sutardja ’748 teaches a multi-core processor. Pet. 22 (citing Ex. 1007 ¶ 221; Fig. 3B); Horst Decl. ¶ 87. Dr. Horst

testifies, “Sutardja [’748] teaches a multi-core processor in the form of ‘a multi-core processing system having a LP core and a HP core.’” Horst Decl. ¶ 87 (citing Ex. 1007 ¶ 221).

Patent Owner does not dispute this contention. We find for the reasons given that Petitioner demonstrates by a preponderance of the evidence that the preamble of claim 1 is taught or suggested by Sutardja.¹¹

- b. Element 1[a][i]: *a first plurality of cores and a second plurality of cores that support a same instruction set,*

Petitioner contends that Sutardja discloses this element. Pet. 22. Petitioner contends that Sutardja ’748 discloses a high-speed, high-power (HP) core and a low-speed, low-power (LP) core, both of which support the same instruction set. *Id.* (citing Ex. 1007 ¶ 225). Further, Petitioner contends that “Sutardja [’748] also teaches a plurality of HP cores and a plurality of LP cores.” *Id.* (citing Horst Decl. ¶¶ 90–101; Ex. 1007 ¶¶ 219, 248).

Further, Dr. Horst testifies that “[a person of ordinary skill] would have been motivated to include multiple LP cores” in Sutardja’s multi-core processor. Horst Decl. ¶ 91. He reasons that “it was well-known to include multiple low-power cores together with multiple high-power cores in a multi-core processor.” *Id.* Dr. Horst backs up his opinion with citations to technical literature. *Id.* He testifies further that “Sutardja [’748] also provides explicit motivation for including multiple LP cores.” *Id.* ¶ 92. He

¹¹ We do not express an opinion on whether the preambles of the challenged claims are limiting.

continues, “[a]s Sutardja [’748] explains, various types of applications may be executed on Sutardja’s multi-core processor.” *Id.* (citing Ex. 1007 ¶ 226). This includes first applications “that require relatively low processing speed during operation” and second and third applications, “each with their own processing requirements.” *Id.* ¶¶ 92–93 (citing Ex. 1007 ¶¶ 226–227). He testifies that a person of ordinary skill “seeking to implement Sutardja’s teachings in a system in which a large number of applications that require relatively low processing speed during operation are expected to operate would therefore have been motivated to include multiple LP cores capable of handling the execution of such applications without needing to transfer the execution of any of the applications to the HP cores.” *Id.* ¶ 98 (internal quotation marks omitted).

Alternatively, Petitioner relies on the teachings of Sutardja ’785 for this claim element. Pet. 25–26.

Patent Owner does not dispute these contentions. We find for the reasons given that Petitioner has proven by a preponderance of the evidence that this claim element is taught or suggested by Sutardja.

- c. Element 1[a][ii]: *wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores*

Petitioner relies on Sutardja to meet this claim element. Pet. 26–27; Horst Decl. ¶¶ 102–103. Petitioner explains that “[t]he second cores (Sutardja’s LP cores) consume less power, for a same applied operating frequency and supply voltage, than the first cores (Sutardja’s HP cores).” Pet. 27; Horst Decl. ¶ 103.

Dr. Horst testifies that “the power consumption of a core with narrow transistors will be less than a core with wider transistors.” Horst Decl.

¶ 103. He concludes that “[a person of ordinary skill] would recognize that Sutardja’s LP core will consume less power than its HP cores for the same reason.” *Id.* (citing Ex. 1007 ¶ 230). His testimony is supported by Sutardja ’748, which discloses that “[t]he transistors 106 of the HP core 24 tend to consume more power during operation in the active state than the transistors 110 of the LP core 28 Gates of the transistors 106 may be larger than gates of the transistors 110.” Ex. 1007 ¶ 230 (quoted in Horst Decl. ¶ 103).

We find Dr. Horst’s testimony to be credible in light of Sutardja ’748. Patent Owner does not challenge Petitioner’s contentions for this claim element. We find for the reasons given that Petitioner has proven by a preponderance of the evidence that Sutardja teaches or suggests this element.

- d. Element 1[b][i]: *power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,*

Petitioner relies on Sutardja to meet this element. Pet. 27–34; Horst Decl. ¶¶ 104–118. Petitioner explains that “[a person of ordinary skill] would have understood that the hardware on which the disclosed hypervisor is installed corresponds to the claimed power management hardware.” *Id.* at 33–34 (citing Horst Decl. ¶ 118). Patent Owner asserts that the “power management hardware” limitation is not met by Sutardja. PO Resp. 2, 22–27; PO Sur-reply 7–9. We disagree with Patent Owner. Patent Owner’s argument and our reasoning are discussed further in the following section.

Petitioner demonstrates also that Sutardja '748 discloses that the first and second plurality of cores are enabled and the first plurality of cores is disabled (but not the second plurality) when there is a drop in demand. Pet. 29–32. Referring to Figure 4 of Sutardja '748, Petitioner explains that “[a person of ordinary skill] would have . . . understood that the transition from the HP mode (with both the HP and LP cores enabled) to the LP mode (with only the LP cores enabled) would occur without disabling any of the LP cores (the claimed second plurality of cores).” *Id.* at 31–32. Dr. Horst provides supporting testimony. Horst Decl. ¶¶ 112–113. Patent Owner does not challenge this assertion.

We find for the reasons given here and in the following section that Petitioner has proven by a preponderance of the evidence that Sutardja teaches or suggests this element.

- e. Element 1[b][ii]: *wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.*

Petitioner asserts that Sutardja meets this element. Pet. 34–35; Horst Decl. ¶¶ 119–124. Referring to Figure 5 of Sutardja '748, Petitioner identifies Kernel Module 220 and PMS Module 242 as the claimed operating system software. Pet. 34–35. Petitioner asserts that a “core profile module” included in the PMS module monitors system performance. *Id.* at 35 (citing Ex. 1007 ¶¶ 251, 260).

Petitioner adds that “Sutardja '[748] further discloses that the operating system (kernel module and PMS module) controls the power management hardware (core switching module) based on the demand.” Pet. 35 (citing Ex. 1007 ¶ 253). Petitioner explains that the PMS module 242,

and/or the kernel module 220 generate a system call to a core switching module 212 to trigger a transition. *Id.* (citing Ex. 1007 ¶ 253; Horst Decl. ¶ 124). Dr. Horst testifies that “[t]he core switching module 212 may transition (switch) the operation from the LP core 200 to the HP core 204 in response to the system call and return control to the kernel module 220 after the transition (switching) is complete.” Horst Decl. ¶ 124 (quoting Sutardja ’748, Ex. 1007 ¶ 253).

Patent Owner challenges these assertions on several grounds. First, as noted *infra*, Patent Owner contends that Petitioner fails to identify in Sutardja a disclosure or teaching of “power management hardware” that meets this claim limitation. Second, and related, is Patent Owner’s argument that Petitioner fails to identify an “operating system” that controls power management hardware as claimed.

We find these arguments unavailing for the reasons that follow.

i. “power management hardware”

Patent Owner argues that “Sutardja does not teach or suggest an operating system executing on a multi-core processor to monitor a demand for the multi-core processor and control *power management hardware* based on the demand, as required by all of the challenged claims.” PO Resp. 21 (emphasis added). Patent Owner’s argument focuses on the hypervisor module shown in its annotation of Figure 5 of Sutardja (reproduced below). *Id.* at 23.

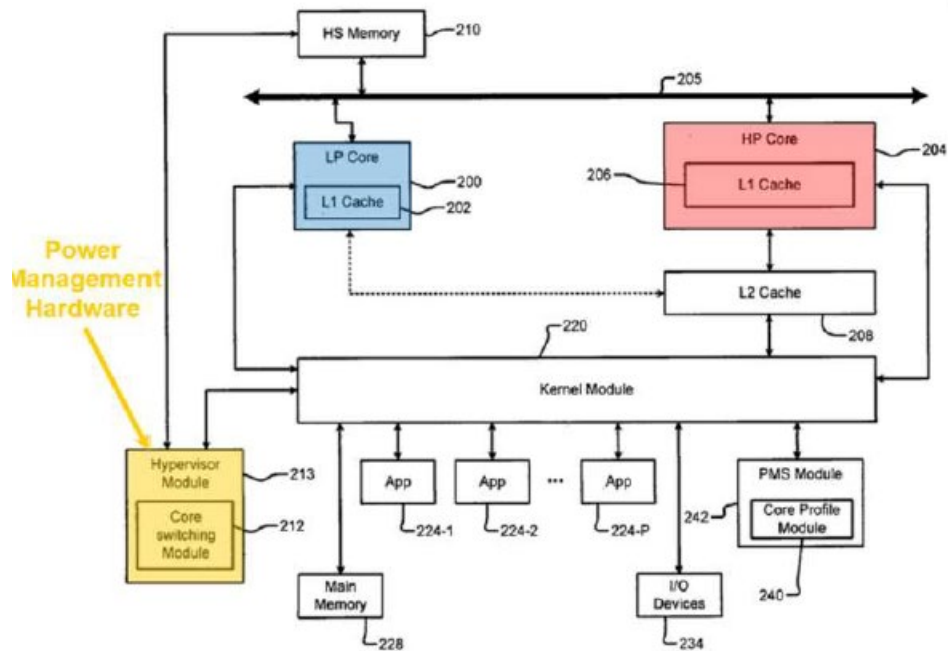


FIG. 5

Annotated Figure 5 from Sutardja '748 appearing above is a block diagram of a control module with first and second cores (highlighted in blue and red, respectively). Ex. 1007 ¶ 195. Core switching module 212 and hypervisor module 213 (highlighted in yellow) are identified by Petitioner as the claimed “Power Management Hardware.” Pet. 34–35.

Patent Owner’s argument focuses mainly on the hypervisor. PO Resp. 23–24. “In its most general form, a hypervisor is a component that abstracts one computer resource from another resource, allowing that other resource to operate in a self-contained fashion.” Brogioli Decl. ¶ 46. The Petition discusses two types of hypervisors: a “host” type that operates above the kernel (the lowest level of the operating system) and a “bare-metal” type that operates below the kernel (i.e., is installed on the underlying hardware). *See, e.g.*, Pet. 33 (citing Ex. 1007 ¶¶ 249, 254; Horst Decl. ¶ 117). According to

the Petition, “the hardware on which the disclosed hypervisor is installed corresponds to the claimed power management hardware.” *Id.* at 33–34; Horst Decl. ¶¶ 117–118.

Patent Owner argues “[a]ccording to the petition then, in Sutardja it is both the hardware controlled by the core switching module and the hardware on which the disclosed hypervisor is installed that correspond to the power management hardware recited in the challenged claims.” PO Resp. 24.

Patent Owner continues, “[t]his argument is deeply flawed and is fatal to Petitioner’s case for obviousness of the challenged claims.” *Id.* at 25. We disagree.

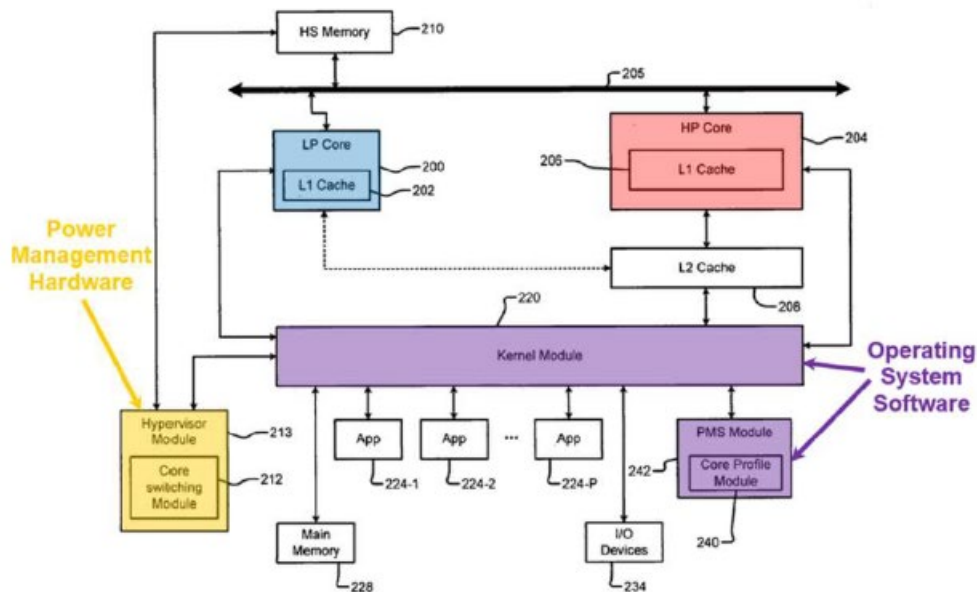
Patent Owner argues that Sutardja’s core switching module “is not ‘hardware’ at all”: “According to Sutardja, the core switching module is software.” PO Resp. 25–26. This argument is unavailing because it divorces the core switching software (including the hypervisor) from its underlying hardware. Sutardja discloses that the hypervisor module and core switching module may be integrated as shown in Figure 5. Pet. 32–33 (citing Ex. 1007 ¶ 253). Associated with the hypervisor is hardware, e.g., the “underlying hardware.” *See* Hearing Tr. 39:22–24 (Patent Owner’s counsel agreeing that for the hypervisor “to do anything, there has to be associated hardware.”). Patent Owner’s argument separating the core switching module software from its hardware ignores the necessary connection between the power management system software and its underlying hardware. For this reason, Patent Owner’s argument that Sutardja’s core switching module “is not ‘hardware’ at all” fails. For the core switching module “to do anything” there must be associated hardware. We therefore agree with Petitioner and find that the hardware associated

with the hypervisor in Sutardja is the claimed “power management hardware.” Pet. 33–34.

Patent Owner’s second argument fares no better. PO Resp. 26–27. Patent Owner argues (hypothetically) that if one assumes the hardware on which the hypervisor is installed operates below the kernel, “it cannot be that the operating system controls this hardware.” *Id.* at 26. This argument also is unavailing. Not all hypervisors operate “below the kernel.” *See* discussion *supra* and in Horst Decl. ¶ 117 (discussing “host” hypervisors that run “inside the operating system”). And even if that were not so, Patent Owner does not dispute that whether above the kernel or below, the hypervisor and core switching module control the associated hardware. Hearing Tr. 39:26–40:16. Patent Owner’s dispute is not whether the hypervisor controls the transition; it is whether that control is “handed over to the hypervisor [by Sutardja’s operating system] whether it’s above or below.” *Id.* at 40:13–16. This “hand off” argument is discussed in the following section. As is discussed in the following section, the operating system in Sutardja and the PMS and core profile modules monitor the cores and “trigger” the transition by sending a request to the hypervisor module. Ex. 1007 ¶ 253. In sum, Patent Owner’s argument that the operating system in Sutardja does not control the hardware because the hypervisor operates “below the kernel” is lacking in merit. Patent Owner’s argument that if the power management system “is the hardware on which the hypervisor is installed, then the operating system of Sutardja does not control the hardware” (PO Resp. 27) is further discussed in the following section.

ii “operating system”

Petitioner explains that “Sutardja’s operating system ‘controls’ a transition between cores when it sends a ‘system call’ to the ‘power management hardware’ to ‘trigger’ the transition.” Pet. Reply 1. This is illustrated by Petitioner’s annotation of Figure 5 of Sutardja ’748 following (Pet. 34):



In annotated Figure 5 above, kernel module 220, core profile module 240, and PMS module 240 (all highlighted in purple) are identified by Petitioner as “Operating System Software.” *Id.* Dr. Horst explains that “the operating system (including the kernel module and PMS module) controls the power management hardware (core switching module) based on the demand.” Horst Decl. ¶ 124. He explains further that “[w]hen the LP core 200 reaches its highest operating speed and additional system loading occurs, the core profile module 240, the PMS module 242, and/or the kernel module 220

disable interrupts and generate a system call to a hypervisor module 213 or a core switching module 212 to trigger a transition.” *Id.* (quoting Ex. 1007 (Sutardja ’748) ¶ 253; emphasis omitted).

Patent Owner responds that “Sutardja is clear that, the kernel and the PMS module do not ‘control’ the core switching module or the hardware on which it runs. Instead, the kernel and the PMS module only make system calls to the core switching module.” PO Resp. 27. We disagree that this is not sufficient control to meet this claim limitation. As Dr. Horst’s testimony (quoted *supra*) explains, the PMS module and kernel modules “trigger a transition” by generating a call to the hypervisor module or a core switching module. Horst Decl. ¶ 124. Patent Owner’s argument fails because it assumes the claims require direct control, when the claims recite no such restriction (nor have we been asked by either party to construe the claims as such).

Patent Owner’s Sur-rebuttal arguments on this issue are likewise unavailing. PO Sur-reply 1, 9–11. For example, we do not credit Dr. Brogioli’s testimony that “it is the core switching module, not the operating system (kernel and PMS module), that controls the hardware and makes the switch from one core to another.” Ex. 2006 ¶ 52 (quoted at PO Sur-reply 10). Dr. Brogioli’s testimony apparently adopts Patent Owner’s “direct control” theory, because it glosses over the fact that the core transition in Sutardja is triggered by the PMS module and kernel of the operating system. Horst Decl. ¶ 124. Similarly, Dr Brogioli testifies that the core switching module “returns control” to the operating system kernel after a transition. Brogioli Decl. ¶ 52. However, this description by Sutardja is not helpful to Patent Owner because it suggests that Sutardja’s operating system had

control of the transition process before calling on the core switching module to continue the process. Just as the claims do not call for direct control, they do not call for continuous control, only that the operating system “control the power management hardware.”

In sum, we find that for the reasons given, Petitioner has proven by a preponderance of the evidence that Sutardja teaches or suggests this claim element.

f. Summary – Claim 1

We find for the reasons given that Petitioner has proven by a preponderance of the evidence that each element of claim 1 is taught or suggested by Sutardja, and we further determine that the claim 1 would have been obvious in light of Sutardja.

2. Independent Claims 9 and 17

Petitioner’s analysis of these claims incorporates its analysis of claim 1. Pet. 43–44. Patent Owner does not separately address these claims, all of which recite the “operating system” limitation discussed in connection with claim 1 in Section II.D.1, *supra*. For the reasons given for claim 1, we determine that Petitioner has proven by a preponderance of the evidence that claims 9 and 17 would have been obvious in light of Sutardja.

3. Dependent Claims 2–4, 7, 8, 10–12, 15, 16, 18–20, 23, and 24

These claims depend from independent claims 1, 9, and 17, discussed *supra*. Petitioner provides an analysis for each of these dependent claims in relation to Sutardja. Pet. 35–42 (claims 2–4, 7, 8), 44–45 (claims 10–12, 15, 16, 18–20, 23, 24). Patent Owner addresses these claims by referring to its analysis of the independent claims and presents no new arguments. PO

Resp. 28–29. We need not separately address these claims because Patent Owner does not provide new arguments based on differences in the dependent claims. *Incept LLC v. Palette Life Scis., Inc.*, 77 F.4th 1366, 1375 (Fed. Cir. 2023)

For the reasons given for claims 1, 9, and 17, we determine that Petitioner has proven by a preponderance of the evidence that these dependent claims would have been obvious in light of Sutardja.

E. Obviousness of Claims 5, 6, 13, 14, 21, and 22 Based on Sutardja and Rychlik

Petitioner asserts that these dependent claims would have been obvious in light of Sutardja and Rychlik. Pet. 45. Petitioner provides an analysis for each of these claims in relation to Sutardja and Rychlik. *Id.* at 45–51. Petitioner asserts that Sutardja ’748 and Rychlik teach each element of claims 5, 6, 13, 14, 21, and 22. *Id.*; Horst Decl. ¶¶ 161–177.

Petitioner provides a motivation for combining the teachings of Sutardja ’748 and Rychlik. *See* Pet. 48 (“A [person of ordinary skill] would have been motivated to apply Rychlik’s teachings to Sutardja’s LP cores, to disable an additional core of Sutardja’s LP cores (the claimed second plurality of cores), for each continued drop in workload (the claimed demand) below a next lower threshold, until only one LP core remained enabled.”). Dr. Horst testifies that “[a person of ordinary skill] seeking to implement Sutardja’s teachings in a system with multiple of Sudardja’s LP cores, would understand that . . . disabling one or more of those LP cores when demand is low, would save power.” Horst Decl. ¶ 169.

Patent Owner does not challenge Petitioner's contentions regarding Rychlik or its combination with Sutardja, relying instead on its arguments for independent claims 1, 9, and 17, discussed *supra*. PO Resp. 29–30.

For the reasons given above including those given for the independent claims, we determine that Petitioner has proven by a preponderance of the evidence that these dependent claims would have been obvious in light of Sutardja and Rychlik. *Incept LLC*, 77 F.4th at 1375.

F. Obviousness of Claims 7, 15, and 23 Based on Sutardja and Carmack

Petitioner asserts that these claims would have been obvious in light of Sutardja and Carmack. Pet. 51. Petitioner provides an analysis for each of these dependent claims in relation to Sutardja and Carmack. *Id.* at 51–52. Petitioner asserts that Sutardja '748 and Carmack teach each element of claims 7, 15, and 23. *Id.*; Horst Decl. ¶¶ 178–181. Petitioner provides a motivation for combining the teachings of Sutardja '748 and Carmack. *See* Pet. 52 (“A [person of ordinary skill] would have been motivated to set the high value to the maximum frequency of Sutardja's HP cores, as taught by Carmack, to maintain desired performance levels during periods of high demand.”)(citing Horst Decl. ¶ 180).

Patent Owner does not challenge Petitioner's contentions regarding Carmack or its combination with Sutardja, relying instead on its arguments for independent claims 1, 9, and 17, discussed *supra*. PO Resp. 29–30.¹²

¹² Patent Owner's Response refers to claim 14 instead of claim 15. PO Resp. 30. From the context, this appears to be a typographical error, in that

For the reasons given above including those given for the independent claims, we determine that Petitioner has proven by a preponderance of the evidence that these dependent claims would have been obvious in light of Sutardja and Carmack. *Incept LLC*, 77 F.4th at 1375.

G. Obviousness Challenges Based on Mathieson and Sutardja and Mathieson, Sutardja, and Rychlik

Petitioner asserts that claims 1–4, 7–12, 15–20, 23, and 24 would have been obvious over Mathieson and Sutardja. Pet. 53–81; Horst Decl. ¶¶ 182–263. Similarly, Petitioner asserts that claims 5, 6, 13, 14, 21, and 22 would have been obvious over Mathieson and Sutardja, further in view of Rychlik. Pet. 81–83; Horst Decl. ¶¶ 265–268. Patent Owner challenges these contentions. PO Resp. 31–43.

Under the circumstances of this case, analyzing these additional grounds challenging the same claims that we have determined to be unpatentable would not be an efficient use of the Board’s time and resources. *See Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (“We agree that the Board need not address issues that are not necessary to the resolution of the proceeding.”). Accordingly, we do not reach these remaining grounds for claims 1–26. *Cf. In re Gleave*, 560 F.3d at 1338 (not reaching other grounds of unpatentability after affirming the anticipation ground); *see also Beloit Corp. v. Valmet Oy*, 742 F.2d 1421,

claim 15, not claim 14, refers to cores “operating at their peak frequency.” Ex. 1001, 9:14–16.

1423 (Fed. Cir. 1984) (determining once a dispositive issue is decided, there is no need to decide other issues). We therefore do not reach these grounds.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has proven by a preponderance of the evidence that claims 1–24 of the '080 patent are unpatentable. In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–4, 7–12, 15–20, 23, 24	103	Sutardja	1–4, 7–12, 15–20, 23, 24	
5, 6, 13, 14, 21, 22	103	Sutardja, Rychlik	5, 6, 13, 14, 21, 22	
7, 15, 23	103	Sutardja, Carmack	7, 15, 23	
1–4, 7–12, 15–20, 23, 24	103	Mathieson, Sutardja ¹³		
5, 6, 13, 14, 21, 22	103	Mathieson, Sutardja, Rychlik ¹⁴		
Overall Outcome			1–24	

¹³ We do not reach this ground because it challenges claims that we have determined to be unpatentable and would not be an efficient use of the Board's time and resources.

¹⁴ See footnote 13.

IV. ORDER

For the foregoing reasons, it is

ORDERED that Petitioner has demonstrated by a preponderance of the evidence that claims 1–24 of the '080 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.¹⁵

¹⁵ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

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