Trevor Mudge
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Education

- Ph.D. Computer Science, University of Illinois, Urbana, Illinois, 1977. Thesis: A Computer Hardware Design Language for Multiprocessor Systems.
- M.S. Computer Science, University of Illinois, Urbana, Illinois, 1973. Thesis: SEMANTRIX: A Semantically Guided Digital Electronic Machine.
- B.Sc. (Hons.) Cybernetics, University of Reading, England, 1969.

Work History

- 2002-present: The Bredt Family Chair of Computer Engineering and Professor Electrical Engineering and Computer Science, Dept. of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor
- 1990-2002: Professor Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor
- 1992-2002: Director of the Advanced Computer Architecture Lab., The University of Michigan, Ann Arbor
- 1984-1990: Associate Professor Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor
- 1977-1983: Assistant Professor Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor
- 1974-1977: Research Assistant, Digital Systems Research Group, Coordinated Science Laboratory, University of Illinois. Research in the areas of digital systems design languages, parallel processing, and fault tolerant computing.
- 1970-1974: Research Assistant, Information Engineering Group, Digital Computer Laboratory, University of Illinois. Design and construction of several digital machines.

Professional Society Membership

- Life Fellow IEEE and member of the IEEE Computer Society
- Fellow of the Association for Computing Machinery
- Member of the IET: The Institution of Engineering and Technology (was Institution of Electrical Engineers)
- Member of the British Computer Society
- Member of Sigma Xi

Awards

- **2021 Test of Time Award** for Razor: A low-power pipeline based on circuit-level timing speculation. 36th Ann. IEEE/ACM Symp. Microarchitecture (MICRO-36), Dec. 2003, pp. 7-18.
- **2021 Best paper** for: Prodigy: Improving the Memory Latency of Data-Indirect Irregular Workloads Using Hardware-Software Co-Design. *Int. Symp. on High Performance Computer Architecture (HPCA)*, Seoul, S. Korea, February 2021.
- **2018 Most Impactful Paper—25 years** Awarded at International Conference on High-Performance Computing (HiPC) Silver Jubilee in December 2018. "Power: A first class design constraint for future architectures." *Proc.*7th Int. Conf. on High Performance Computing - HiPC, (Springer Lecture Notes in Computer Science), Dec. 2000, Bangalore, India, pp. 215-224.
- **2017 ACM SIGARCH/IEEE-CS TCCA Influential ISCA paper award**, for "Dowsy Caches: Simple Techniques for Reducing Leakage Power" (with K. Flautner, N. Kim, S. Martin, D. Blaauw) from the *Proc. of the 29th Ann. Int. Symp. on Computer Architecture*, May 2002. The award recognizes the paper from the ISCA proceedings 15 years earlier that has had the most impact on the field during the intervening years.
- **2017 Fellow of the Association of Computing Machinery**, "For contributions to power aware computer architecture".
- **2015 Top Pick: selected as one of the 12 best papers in computer architecture for 2015** J. Hauswald, M. A. Laurenzano, Y. Zhang, C. Li, A. Rovinski, A. Khurana, R.G. Dreslinski, T. Mudge, V. Petrucci, L. Tang, J. Mars. Sirius: An Open End-to-end Voice and Vision Personal Assistant and Its Implications For Future Warehouse Scale Computers. *IEEE MICRO* May/June 2016, vol. 36, no. 3, pp. 42-53.
- **2014 International Conference on Supercomputing 25th Anniversary Issue 1987-2011 (35 most influential papers)**. For the paper: Improving data cache performance by pre-executing instructions under a cache miss. (James Dundas and Trevor Mudge) Proc. 1997 ACM Int. Conf. on Supercomputing, July 1997. Reprinted in the anniversary issue, U. Banerjee Editor, 2014.
- **2014 Best paper** for: Sources of Error in Full System Simulation. *2014 IEEE Int. Symp. on Performance Analysis of Systems and Software (ISPASS)*, Monterey, CA, March 2014, pp. 13-22.
- **2014 Distinguished Achievement Award** from the University of Illinois Computer Science Department as an "outstanding educator and researcher whose work has advanced the field of low-power computer architecture and its interaction with technology." Given at the Department's CS @ Illinois 50th Anniversary Celebration, October 20th , 2014.
- **2014 ACM/IEEE CS Eckert-Mauchly Award.** For pioneering contributions to low-power computer architecture and its interaction with technology. June 2014.
- **2014 Chartered IT Professional (CTIP),** British Computer Society, c. 2014.
- **2013 Life Fellow of the IEEE**, 2013
- **2012 International Conference on Computer-Aided Design's Ten Year Retrospective Most Influential Paper Award in 2012**. For the paper: Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads. (S. Martin, K. Flautner, D. Blaauw, and T. Mudge.) Appeared in *Proc. Int. Conf. of Computer Aided Design (ICCAD-2002)*, San Jose, CA, Nov. 2002, pp. 721-725.
- **2011 Winner in the 11th Annual International VLSI Symposium Low Power Design Contest.** For the paper: SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric. (S. Satpathy, R. Dreslinski, T. Ou, D. Sylvester, T. Mudge, D. Blaauw.) Appeared in the *Symposium on VLSI Technology and Circuits*. Kyoto, Japan, June 2011, pp.138-139.
- **2011 Winners of the DAC/ISSCC Student Design Contest for 2011** Mentor for (With David Blaauw and Dennis Sylvester) their project "Design and Implementation of Centip3De, a 7-layer Many-Core

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System", D. Fick, R. Dreslinski, B. Giridhar, G. Kim, S. Seo, M. Fojtik, S. Satpathy, Y. Lee, D. Kim, N. Liu, M. Wiekowski, G. Chen, T. Mudge, D. Sylvester, and D. Blaauw. Proc. of the ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, June, 2011.

- **2009 Top Pick: selected as one of the 12 best papers in computer architecture for 2009** M. Woh, S. Seo, S. Mahlke, T. Mudge, C. Chakrabarti, and K. Flautner. AnySP: Anytime Anywhere Anyway Signal Processing. *36th Int. Symp. on Computer Architecture*, Austin, TX, June, 2009, pp. 128-139.
- **2009 Ted Kennedy Family Team Excellence Award** for 2008-9 from the College of Engineering, University of Michigan, April 2009.
- **2008 Top Pick: selected as one of the 12 best papers in computer architecture for 2008** K. Lim, P. Ranganathan, J. Chang, C. Patel, T. Mudge, S. Reinhardt. Understanding and designing new server architectures for emerging warehouse-computing environments. *35th Int. Symp. on Computer Architecture*, Beijing, China, June, 2008, pp. 315-326.
- **2008 Best paper** for: From SODA to Scotch: The Evolution of a Wireless Baseband Processor. *41st IEEE/ACM Int. Symp. on Microarchitecture (MICRO*), Lake Como, Italy, Nov. 2008, pp. 152-163.
- **2007 Best Paper Nomination** for: B. Zhai, R. Dreslinski, D. Blaauw, T. Mudge, and D. Sylvester. Energy Efficient Near-threshold Chip Multi-processing. Int. Symp. on Low Power Electronics and Design - 2007 (ISLPED), Aug. 2007, pp. 32-37.
- **2007 Best paper** for: Next Generation Challenge for Software Defined Radio. M. Woh, S. Seo, H. Lee, Y. Lin, S. Mahlke, T. Mudge, C. Chakrabarti, and K. Flautner. *SAMOS VII,* Greece, April 2007, pp. 343-354.
- **2006 Top pick paper selected as one of the 12 best papers in computer architecture for 2006,** for: Y. Lin, H. Lee, M. Woh, Y. Harel, S. Mahlke, T. Mudge, C. Chakrabarti, K Flautner. SODA: A low-power architecture for software radio. *Proc. 33rd Ann. Int. Symp. on Computer Architecture*, Boston, MA USA, June 2006, pp. 89-101.
- **2007 Microprocessor Report Innovation Award:** "RAZOR—Error-Tolerant Approach Supports Speculative Correctness" MPR Analysts' Choice Award in the Innovation category – 2/26/07. (Microprocessor Report has been the leading technical publication for the microprocessor industry since 1987.)
- **2003 Top pick paper selected as one of the 12 best papers in computer architecture for 2003**, for: D. Ernst, N. Kim, S. Das, S. Pant, T. Pham, R. Rao, C. Ziesler, D. Blaauw, T. Austin, T. Mudge, and K. Flautner. Razor: A low-power pipeline based on circuit-level timing speculation. *36th Ann. IEEE/ACM Symp. Microarchitecture (MICRO-36)*, Dec. 2003, pp. 7-18.
- **2003 Best paper** for: D. Ernst, N. Kim, S. Das, S. Pant, T. Pham, R. Rao, C. Ziesler, D. Blaauw, T. Austin, T. Mudge, and K. Flautner. Razor: A low-power pipeline based on circuit-level timing speculation. *36th Ann. IEEE/ACM Symp. Microarchitecture (MICRO-36)*, Dec. 2003, pp. 7-18.
- **2003 Bredt Family Chair of Engineering**, conferred by the College of Engineering in 2003.
- **1997 Research Excellence Award** for 1995-96 from the College of Engineering, University of Michigan, Feb. 1997.
- **1996 Heaviside Premium**. Awarded by the Institution of Electrical Engineer for the best paper of the year: A comparison of two common pipeline structures. *Proc. Computers and Digital Techniques*, 1996.
- **1995 Fellow of the Institute of Electrical and Electronics Engineers**, "For contributions to the design and analysis of high performance processors," 1995.
- **1995 Research Excellence Award** for 1994-95 EECS Department , University of Michigan, Feb. 1995.
- **Best paper nomination** for "Analysis and design of latch-controlled synchronous digital circuits," (15 out of 377) at the 27-th Design Automation Conference, June 1990.
- **1986 Best IEEE MICRO article** of 1986 for "A Microprocessor-based Hypercube Supercomputer."

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- **1983 Outstanding Teaching** in Engineering. Awarded by the College of Engineering, University of Michigan, Dec.1983.
- **1982 Quest for Technology** Awards (2). Awarded by Control Data Corporation, Oct. 1982.
- **1981 Best paper runner-up**. Honorable mention from the editors of the IEEE Trans. on Education for runner-up best paper published in 1981: "A Course Sequence in Microprocessor-Based Digital Systems Design."
- **1981 John A. Curtis Award**. Awarded by The Computers in Education Division of the American Society of Engineering Educators, June 1981, for the paper: Teaching Assembly Language Using an Assembly Language Interpreter.
- **1981 Best paper**. Awarded by The Instrument Society of America at their 27-th Int. Symposium, Apr. 1981, for the paper: VLSI Implementation of a Numerical Processor for Robotics.

Miscellaneous Recognition

- **International Symposium on Computer Architecture Hall of Fame:**
  http://pages.cs.wisc.edu/~arch/www/iscabibhall.html
- **MICRO Hall of fame:**
  https://www.sigmicro.org/micro-hall-of-fame/
- **Erdős number = 3**

Post Docs

1. Xin He, November 2018 – May 2022. Current position: Senior Engineer at Tentorrent
2. Ronald G. Dreslinski Jr., April 2011 - January 2012 Current position: Associate Professor Department of Electrical Engineering and Computer Science, The University of Michigan
3. Reetuparna Das, September 2011- September 2015 Current position: Associate Professor Department of Electrical Engineering and Computer Science, The University of Michigan.
4. Yoonseo Choi, September 2007 – September 2010 Current position: Software Engineer Intel Corporation.

Ph.D. Theses Supervised

1. Optimizing Sparse Linear Algebra on Reconfigurable Architecture, Dong-hyeon Park, The University of Michigan, 2021. Current position: Military service in the Republic of Korea Army.
2. Rethinking Context Management of Data Parallel Processors in an Era of Irregular Computing, Jonathan Beaumont, The University of Michigan, 2019. Current position: Lecturer IV Dept Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor.
3. Architecting Memory System for Emerging Technologies, Byoungchan Oh, The University of Michigan, 2017. (Co-chairman Ronald G. Dreslinski Jr.) Current position: Senior Memory Architect, Intel Federal LLC.
4. Heterogeneous Mobile Platform Characterization and Accelerator Design, Cao Gao, The University of Michigan, 2017. (Co-chairman Ronald G. Dreslinski Jr.) Current position: Software Engineer, Google Inc.

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5. Studies in Exascale Computer Architecture: Interconnect, Resiliency, and Checkpointing, Sandunmalee Nilmini Abeyratne, The University of Michigan, 2017. (Co-chairman Ronald G. Dreslinski Jr.) Current position: Performance Architect Intel Corporation.
6. Designing Flexible, Energy Efficient and Secure Wireless Solutions for the Internet of Things, Yajing Chen, The University of Michigan, 2017. (Co-chairman Hun-Seok Kim) Current position: Digital Design Engineer, Intel Corporation.
7. Datacenter Design for Future Cloud Radio Access Network, Qi Zheng, The University of Michigan, 2016. (Co-chairman Ronald G. Dreslinski Jr.) Current position: Software Engineer, Square Inc., San Francisco, California.
8. Dense Server Architectures, Anthony Thomas Gutierrez, The University of Michigan, 2015. Current position: Member of Technical Staff, Design Engineer at AMD Research, Seattle Washington.
9. Scaling High-Performance Interconnect Architectures to Many-Core Systems, Korey LaMar Sewell, The University of Michigan, 2012. Current position: CPU Performance Architect, Apple.
10. Near-Threshold Computing: From Single Core to Many-Core Energy Efficient Architectures, Ronald G. Dreslinski Jr., The University of Michigan, 2011. Current position: Assistant Professor Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor.
11. Energy-efficient Architecture For Mobile Signal Processing, Sangwon Seo, The University of Michigan, 2011. Current position: Qualcomm Inc.
12. Architecture and Analysis For Next Generation Mobile Signal Processing, Mark Woh, The University of Michigan, 2011. Current position: Google Inc.
13. A Hardware/Software Approach for Alleviating Scalability Bottlenecks in Transactional Memory Applications, Geoffrey Wyman Blake, The University of Michigan, 2011. Current position: Senior System Development Engineer, Amazon Web Services.
14. Efficient Data Center Architectures Using Non-Volatile Memory and Reliability Techniques, David Andrew Roberts, The University of Michigan, 2010. Current position: Senior Member of Technical Staff at AMD.
15. Disaggregated Memory Architectures for Blade Servers, Kevin Te-Ming Lim, The University of Michigan, 2010. (Co-chairman Steven Reinhardt) Current position: Google Inc.
16. Cache Resource Allocation in Large Scale Chip Multiprocessors, Lisa Rufeng Hsu, The University of Michigan, 2009. (Co-chairman Steven Reinhardt) Current position: Staff Engineer in Qualcomm Datacenter Technologies.
17. Full-System Critical-Path Analysis and Performance Prediction, Ali Ghassan Saidi, The University of Michigan, 2009. (Co-chairman Steven Reinhardt) Current position: Principal System Development Engineer, Amazon Web Services.
18. Microarchitecture Choices And Tradeoffs For Maximizing Processing Efficiency, Deborah T. Marr, The University of Michigan, 2008. Current position: Senior Principal Engineer and Director of the Accelerator Architecture Research Lab, Intel Corporation.
19. Realizing Software Defined Radio – A Study in Designing Mobile Supercomputers, Yuan Lin, The University of Michigan, 2008. (Co-chairman Scott Mahlke) Current position: Senior Principal Engineer, Compiler Technical Lead, Sambanova Inc.
20. The Fast, Efficient, And Representative Benchmarking Of Future Microarchitectures, Jeffrey Stuart Ringenberg, The University of Michigan, 2008. Current position: Lecturer IV Dept Electrical Engineering and Computer Science, U Michigan, Ann Arbor.
21. Architecting Energy Efficient Servers, Tae Ho Kgil, The University of Michigan, 2007. Current position: Head of Cloud and Security Engineering at MagicCube.

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22. A Baseband Processor For Software Defined Radio Terminals, Hyunseok Lee, The University of Michigan, 2007. Current position: Assistant Research Professor Arizona State University, Tempe Arizona.
23. Improving Performance and Energy Consumption in Region-Based Caching Architectures, Michael J. Geiger, The University of Michigan, 2006. (Co-chairman Gary Tyson) Current position: Lecturer, Electrical & Computer Engineering Department, University of Massachusetts Lowell.
24. Application-Specific Architecture Framework for High-Performance Low-Power Embedded Computing, Allen Chao-Hung Cheng, The University of Michigan, 2006. (Co-chairman Gary Tyson)
25. Virtualizing Register Context, David W. Oehmke, The University of Michigan, 2005. Current position: Principal Engineer, Cray Inc. Minneapolis, Minnesota.
26. Circuit and Microarchitectural Techniques for Processor On-Chip Cache Leakage Power Reduction, Nam Sung Kim, The University of Michigan, 2004. Current position: Senior Vice-President Samsung, on leave as a Professor, Electrical and Computer Engineering, University of Illinois, Champaign-Urbana, Illinois.
27. Design, Implementation and use of an Experimental Compiler for Computer Architecture Research, David Anthony Greene, The University of Michigan, 2003. Current position: Senior Compiler Engineer, Cray Inc. Minneapolis, Minnesota.
28. Limits and Misconceptions in Branch Prediction, Avinoam Nomik Eden, The University of Michigan, 2001. Current position: Serial Entrepreneur.
29. Compiler and Microarchitecture Mechanisms for Exploiting Registers to Improve Memory Performance, Matthew Allan Postiff, The University of Michigan, 2001. Current position: Pastor of the Fellowship Bible Church, Ann Arbor, Michigan.
30. Automatic Monitoring for Interactive Performance and Power Reduction, Krisztian Flautner, The University of Michigan, 2001. Current position: VP Technology at Arm Holdings.
31. Modern DRAM Architectures, Brian Thomas Davis, The University of Michigan, 2001. (Co-chairman Bruce Jacob) Current position: Senior Vice President, Sales and Marketing, HAECO Americas.
32. Efficient Execution of Compressed Programs, Charles Robert Lefurgy, The University of Michigan, 2000. Current position: Research Staff Member, Austin Research Laboratory, Austin, Texas.
33. Pseudo-Vector Machines for Embedded Applications, Lea Hwang Lee, The University of Michigan, 2000. Current position: DSP Architect, ZTE Corp., Richardson TX.
34. The Impact of Computer Architecture Features on Image Processing Application Execution times: A Case Study Using MPEG Image Sequence Compression on the IBM SP2, Jeremy Alan Salinger, The University of Michigan, 2000. (Co-chairman Gregory Wakefield) Current position: Innovation Program Manager, General Motors R&D, Warren MI.
35. Functional Design Verification for Microprocessors by Error Modeling, David Van Campenhout, The University of Michigan, 1999. Current position: Senior Staff Engineer, Xilinx, Inc.
36. Improving Processor Performance by Dynamically Pre-Processing the Instruction Stream, James David Dundas, The University of Michigan, 1998.
37. Optimizing High Performance Dynamic Branch Predictors, Chih-Chieh Lee, The University of Michigan, 1997.
38. Enhancing Instruction Fetching Mechanism Using Data Compression, I-Cheng Chen, The University of Michigan, 1997.

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39. Software-Oriented Memory-Management Design, Bruce Ledley Jacob, The University of Michigan, 1997. Current position: Professor of Electrical & Computer Engineering, University of Maryland, College Park, Maryland.
40. Reducing the Penalty of Branch and Load Hazards in Pipelined Microprocessors, Michael Leonard Golden, The University of Michigan, 1995.
41. OS/Architecture Interactions and Influence on Computer Architecture, David Frederick Nagle, The University of Michigan, 1995.
42. Cache Behavior in the Presence of Speculative Execution - The Benefits of Misprediction, James E. Pierce, The University of Michigan, 1995.
43. Architectural Macro-Modeling of Processor Memory Components, Ghazanfar Ali Khan, The University of Michigan, 1995.
44. Trace-driven Memory Simulation, Richard Albert Uhlig, The University of Michigan, 1995. Current position: Intel Fellow and Managing Director of Intel Labs.
45. Architectural Trade-offs in a Latency Tolerant Gallium Arsenide Microprocessor, Michael Douglas Upton, The University of Michigan, 1994. (Co-chairman Richard Brown)
46. Loop Optimization Techniques on Multi-Issue Architectures, Dan Richard Kaiser, The University of Michigan, 1994.
47. Technology-Organization Trade-offs in the Architecture of a High Performance Processor, Oyekunle Ayinde Olukotun, The University of Michigan, 1991. Current position: Professor of Electrical Engineering and Computer Science at Stanford University and Director of the Pervasive Parallelism Laboratory.
48. Run-Time Support for Parallel Programs, Russell Mace Clapp, The University of Michigan, 1991.
49. Design of a Non-Interfering Debugger for Embedded Real-Time Systems, Venu Prabhakar Banda, The University of Michigan, 1990. (Co-chairman Richard Volz)
50. Machine Recognition and Attitude Estimation of Three-Dimensional Objects, Paul Gunther Gottschalk III, The University of Michigan, 1990.
51. A Distributed Real-Time Language and Its Operational Semantics, Padmanabhan Krishnan, The University of Michigan, 1989. (Co-chairman Richard Volz)
52. Parallel Processing of Best-First Branch and Bound Algorithms on Distributed Memory Multiprocessors, Tarek Saad Abdel-Rahman, The University of Michigan, 1989. Current position: Professor at The Edward S. Rogers Sr. Department of Electrical and Computer Engineering, U Toronto, Ontario, Canada.
53. Bus and Cache Memory Organizations for Multiprocessors, Donald Charles Winsor, The University of Michigan, 1989. Current position: Departmental Computing Organization Coordinator; Adjunct Professor Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor.
54. High Performance Communications for Hypercube Multiprocessors, Gregory Dean Buzzard, The University of Michigan, 1988.
55. Recognition of Partially Occluded Parts, Jerry Lee Turney, The University of Michigan, 1986.
56. A Study in Memory Interference Models, H.B. Humoud, The University of Michigan, 1985.
57. A Stochastic Model of Multiprocessing, Brad Alan Makrucki, The University of Michigan, 1984.

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Patents Issued

2020

- J. Kloosterman, J. Beaumont, D. Jamshidi, J. Bailey, T. Mudge, S. Mahlke. Dynamically Allocating Storage Elements to Provide Registers for Processing Thread Groups. USPTO 10,585,701 Issued March 10, 2020.
- K. Flautner, T. Austin, D. Blaauw, T. Mudge, D. Bull. Error Recovery within Integrated Circuit. USPTO 10,579,436 Issued March 3, 2020.
- K. Flautner, T. Austin, D. Blaauw, T. Mudge, D. Bull. Error Recovery within Integrated Circuit. USPTO 10,572,334 Issued February 25, 2020.

2019

- Y. Chen, T. Mudge, R. Dreslinski Jr., S. Lu, H.-S. Kim, D. Blaauw, F. Cheng. Configurable Arithmetic Unit. USPTO 10,409,615 Issued September 10, 2019.

2018

- S. Jeloka, S. Aberaytne, R. Dreslinski Jr., R. Das, T. Mudge, D. Blaauw. Apparatus and Methods for Generating a Selection Signal to Perform an Arbitration in a Single Cycle Between Multiple Signal Inputs Having Respective Data Send. USPTO 10,037,295. Issued July 31, 2018.
- B. Oh, S. Aberaytne, R. Dreslinski Jr., T. Mudge. Enhanced Memory Device. USPTO 10,002,657. Issued June 19, 2018.
- J. Pusdesris, T. Mudge, T. Manville. Data Processing Apparatus and Method for Decoding Instructions In Order to Generate Control Signals for Processing Circuitry of the Data Processing Apparatus. USPTO 9,880,843. Issued January 30, 2018.

2016

- S. Jeloka, S. Abeyratne, R. Dreslinski Jr., R. Das, T. Mudge D. Blaauw. Single Cycle Arbitration Within an Interconnect. USPTO 9,514,074. Issued December 6, 2016.
- T. Mudge, A. Pellegrini, B. VanderSloot, J. Pusdesris Y. Kang. Data Processing Apparatus with Memory Rename Table for Mapping Memory Addresses to Register. USPTO 9,471,480. Issued October 18, 2016.
- G. Blake, T. Mudge, S. Biles. Contention Management for a Hardware Transactional Memory. USPTO 9,513,959. Issued December 6, 2016
- K. Flautner, T. Austin, D. Blaauw, T. Mudge, D. Bull. Error Recovery within Integrated Circuit. USPTO 9,448,875. Issued September 20, 2016.

2015

- T. Mudge, T. Manville. Next Branch Table for Use with a Branch Predictor. USPTO 9,135,011. Issued September 15, 2015.
- K. Flautner, D. Blauuw, D. Bull, T. Austin, T. Mudge. Single Event Upset Tolerant Flip-Flop. USPTO 9,164,842. Issued October 20, 2015.

2014

- S. Satpathy, D, Blauuw, D, Sylvester, T. Mudge. Crossbar Circuitry for Applying an Adaptive Priority Scheme and Method of Operation of Such Circuitry. USPTO 8,868,817. Issued October 21, 2014.
- D. Bull, D. Blaauw, T. Austin, K. Flautner, T. Mudge. Error recovery within Integrated Circuit. USPTO 8,650,470. Issued February 11, 2014.

2013

- S. Satpathy, D. Blaauw, T. Mudge, D. Sylvester. Crossbar Circuitry and Method of Operation of Such Crossbar Circuitry. USPTO 8,549,207. Issued October 1, 2013; Japan Patent Number: 5816063. Issued October 2, 2015.
- K. Flautner, T. Austin, D. Blaauw, T. Mudge, D. Bull. Error recovery within processing stages of an integrated circuit. USPTO 8,407,537. Issued March 26, 2013.
- D. Blaauw, T. Mudge, D. Sylvester, R. Dreslinski Jr., D. Fick. Vertical Interconnect Patterns in Multi-Layer Integrated Circuits. USPTO 8,381,155. Issued February 19, 2013.
- T. Mudge, D. Blaauw, C. Tokunaga. Random Number Generator. USPTO 8,346,832; China Patent Number: 200710181971.0; Japan Patent Number: 4938612; United Kingdom Number: GB2442838. Issued January 1, 2013; March 6, 2013; March 2, 2012; May 11, 2011.

2012

- R. Dreslinski Jr., T. Mudge, D. Blaauw, D. Sylvester, G. Chen, Cache Memory System for a Data Processing Apparatus. USPTO 8,355,122. Issued December 18, 2012.
- D. Roberts, T. Mudge, T. Wenisch. Cache Memory with Power Saving State. USPTO 8,285,936. Issued October 9, 2012.
- S. Satpathy, D. Blaauw, T. Mudge, D. Sylvester, R. Dreslinski Jr. Crossbar Circuitry for Applying a Pre-selection Prior to Arbitration Between Transmission Requests and Method of Operation of Such Crossbar Circuitry. USPTO 8,255,610. Issued August 28, 2012.
- D. Roberts, T. Mudge, G. Dasika. Storage of Data in Data Stores Having Some Faulty Storage Locations. USPTO 8,230,277. Issued July 24, 2012.
- S. Satpathy, D. Blaauw, T. Mudge, D. Sylvester, R. Dreslinski Jr. Crossbar Circuitry and Method of Operation of Such Crossbar Circuitry. USPTO 8,230,152. Issued July 24, 2012.
- D. Roberts, T. Mudge, G. Dasika. Storage of Data in Data Stores Having Some Faulty Storage Locations. USPTO 8,145,960. Issued March 37, 2012.
- S. Satpathy, D. Blaauw, T. Mudge, D. Sylvester, R. Dreslinski Jr. Crossbar Circuitry and Method of Operation of Such Crossbar Circuitry. USPTO 8,108,585. Issued January 31, 2012.

2011

- T. Mudge, K. Flautner, D. Blaauw, T. Austin, D. Bull, S. Das. Cost Effective Razor Pipeline Recovery with micro-Architectural Support. China Patent Number ZL200580050138.1. Issued December 2, 2009; United Kingdom Patent Number: 2439019. Issued June 2, 2010; Japan Patent Number: 472299. Issued April 15, 2011.

2010

- K Flautner, D. Bull, T. Austin, D. Baauw, T. Mudge. Integrated circuit with error correction mechanisms to offset narrow tolerancing. USPTO 7,701,240. Issued April 20, 2010.
- K. Flautner, T. Austin, D. Blaauw, T. Mudge. Error Detection and Recovery Within Processing Stages of an Integrated Circuit. USPTO 7,650,551. Issued January 19, 2010; Israel Patent Number:168928. Issued May 31, 2010; Republic of Korea: 982461. Issued September 9, 2010.

2009

- K. Flautner, D. Blaauw, T. Mudge, N. Kim, S. Martin. Data processing memory circuit. USPTO 7,533,226. Issued May 12, 2009.
- K Flautner, T. Mudge. Performance Level Selection in a Data Processing System by Combining a Plurality of Performance Requests. USPTO 7,512,820. Issued March 31, 2009.
- K. Flautner, D. Blaauw, T. Austin, T. Mudge. Using Shadow Latches As Low Leakage Retention Latches. China Patent Number: ZL200480007397. Issued March 11, 2009; Japan Patent Number: 4335253. July 3, 2009.

2008

- T. Mudge, T. Austin, D. Blaauw, K Flautner. Systematic and Random Error Detection and Recovery Within Processing Stages of an Integrated Circuit. USPTO 7,337,356. Issued February 26, 2008; Germany, France, United Kingdom, Italy, Netherlands, and Europe Patent Number: 1604281. Issued August 9, 2006.
- K Flautner, T. Mudge, D. Flynn. Data Processing System Performance Counter. USPTO 7,321,942. Issued January 22, 2008.

2007

- T. Mudge, T. Austin, D. Blaauw, K. Flautner. Data Retention Latch Provision Within Integrated Circuits. USPTO 7,310,755. Issued December 18, 2007; India Patent Number: 7. Issued ?; Germany, Europe, France, Netherlands, Korea, Israel, and Italy Patent Number: 1604265. Issued June 14, 2006; China Number ?, Issued May 20, 2010; Japan ZL200480007397.1. March 11, 2009.
- K. Flautner, T. Austin, D. Blaauw, T. Mudge. Error Detection and Recovery Within Processing Stages of an Integrated Circuit. USPTO 7,278,080. Issued October 2, 2007; Malaysia Patent Number MY-136842-A. Issued November 28, 2008. China Patent Number: ZL200480007338.4. Issued July 9, 2008; India Patent Number: 225122. Issued October 31, 2008; Japan Patent Number: 4426571. Issued December 18, 2009.
- K Flautner, T. Mudge. Data Processor Memory Circuit. USPTO 7,260,694. Issued August 21, 2007.
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- Int. Symp. on High Performance Computer Architecture (HPCA): 2004 - present

Conference General Chair

- Int. Conf. on Compilers, Architectures and Synthesis for Embedded Systems (CASES) , Oct. 2002 (co-chair)
- Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-28), Dec. 1995

Program Chair

- 13th Int. Symp. on High Performance Computer Architecture (HPCA), 2006 (co-chair)

Petitioner Mercedes Ex-1003, 0039

- Int. Conf. on Compilers, Architectures and Synthesis for Embedded Systems (CASES), Nov. 2001 (co-chair)
- 24th Int. Symp. on Computer Architecture (1997), Ann Arbor, Michigan (vice-chair)
- Vice-Chair for the IPPS-94
- 21st Int. Conf. on Parallel Processing (ICPP), (co-chair)
- 11th Int. Symp. on Computer Architecture (1984), Ann Arbor, Michigan (vice-chair)

Program Committee

- Int. Symp. on Computer Architecture
- ISCA-33 2006; ISCA-28 2001; ISCA-26 1999; ISCA-24 1997; ISCA-23 1996; ISCA-20 1993; ISCA-18 1991; ISCA-16 1989; ISCA-15 1988; ISCA-7 1980
- Annual IEEE/ACM International Symposium on Microarchitecture
- MICRO-42 2009; MICRO-33 2000; MICRO-30 1997; MICRO-29 1996; MICRO-27 1994
- Int. Symp. on High Performance Computer Architecture
- HPCA-8 2002; HPCA-7 2001; HPCA-6 2000; HPCA-3 1996; HPCA-1 1994
- Int. Symp. on Low Power Electronics and Design (ISLPED) 2006
- Design Automation Conf. (DAC) 2005
- 5th International Conference on Supercomputing, Sorrento, Italy, June, 2001
- South African Inst. of Comp. Scientists & Info. Technologists, Ann. Res. Conf., 2000.
- Architectural Support for Programming Languages and Operating Systems IX (ASPLOS), Dec. 2000
- Advanced Research in VLSI, Sep. 1997
- 6th Ann. ACM Symp. on Parallel Algs and Archs (SPAA '94)
- Int. Symp. on High Performance Distributed Computing
- HPDC-3; HPDC-2

Workshops

- 4th Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC-4)
- Workshop Chairman 16th Symp. on Computer Architecture (1989), Eilat, Israel

Workshops and Reviewing--numerous

Consulting—upon request

LITIGATION RELATED EXPERIENCE

Case: Qualcomm v. Apple
Matter: Expert for IPR Qualcomm
Law Firm: Quinn Emanuel Urquhart
Contact: Andrew Holmes
Date closed:

Case: Netlist Inc. v. SK Hynix
Matter: Expert for IPR for SK Hynix
Law Firm: Sidley Austin
Contact: Michael Hatcher
Date closed:

Case: WARF v. Apple
Matter: Expert for Validity of WARF patent
Deposition and trial testimony
Law Firm: Irell and Manella
Contact: Gary Frischling
Date closed: September 2015
deposed
cross examined at trial

Case: Sony v. Microlinc
Matter: Supporting Sony in matter involving low power processor
Law Firm: Quinn Emanuel
Contact: Eric Huang
Date closed: August 2013

Case: ITC (Intellectual Ventures) v. Hynix and Elpida
Matter: Memory analysis, DRAM and FLASH
Depostion
Law Firm: Irell and Manella
Contact: Brian Ledahl
Date closed: October 2012
deposed

Matter: Invention and patent analysis
Law Firm: Intellectual Ventures

Contact: William Mangione-Smith
Date closed: Not active for some time

Case: Intel vs. Optimum Processing Solutions LLC
Law Firm: Kirkland & Ellis
Matter: Computer architecture.
Dates: 06/01/09 to 6/01/10

Case: Witchita Falls Power Management v. Intel
Matter: Supporting Intel in matter involving low power processors
Law Firm: Fish & Richardson
Contact: Neil McNabnay
Date closed: January 2006

Case: MicroUunity v. AMD
Matter: Supporting AMD in matter involving low power semiconductors
Law Firm: O'Melvney & Meyers
Date closed: Never started

Case: Paxar Corp. v. Zebra Technologies
Matter: Supported Zebra in case involving point of sale printers
Law Firm: Goodwin Procter - Started with Testa and Hurwitz, Boston, MA
Responsibilities: Wrote expert report and was deposed
Dates: 01/01/05 to 09/30/06
Deposed

Case: Cummins Allison v. Glory Ltd.
Matter: Supported Glory Ltd. in patent dispute
Responsibilities: Wrote expert report
Law Firm: Hogan & Hartson
Dates: 08/01/04 to 08/01/06

Case: Class Action v. Intel
Matter: Supported Intel in a case involving Pentium processor technology
Responsibilities: Was deposed
Contact: Terry Frenzl
Law Firm: Brown & Bain
Dates: 01/01/04 – 08/01/06
Deposed

Case: Rockwell v.
Law Firm: Barlit and Beck

Matter:	Representing HP printers, Boise ID
Responsibilities:	Printer hardware and software
Dates:	10/01/03 to 01/01/04

Case:	Representing Iomega Corp.
Law Firm:	Hale and Dorr, Boston, MA
Responsibilities:	Expert services for network hardware.
Dates:	09/01/99 to 12/31/02

Case:	Rockwell/Allen Bradley v. empolyees
Matter:	Supported Rockwell in case involving network cards
Responsibilities:	Wrote expert report and was deposed
Law Firm:	Foley & Lardner
Dates:	09/01/98 to 12/31/00

Deposed

Case:	DEC v. Intel
Matter:	Supported Intel in patent dispute
Responsibilities:	Wrote expert report
Law Firm:	Sughrue, Mion
Date closed:	1998

Responsibilities:	Expert services for the Intel-FTC case
Law Firm:	Sughrue, Mion, Zinn, Macpeak & Sears, Washington, DC
Dates:	08/1/98 to 09/30/98

Case:	DEC vs Intel
Law Firm:	Sughrue, Mion, Zinn, Macpeak & Sears, Washington, DC
Responsibilities:	Expert services for the DEC-Intel patent infringement case.
Dates:	08/1/97 to 01/31/98.