

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

Case IPR2023-01335
Patent 8,775,833 B2

Before WILLIAM V. SAINDON, ARTHUR M. PESLAK, and
GREGG I. ANDERSON, *Administrative Patent Judges*.

SAINDON, *Administrative Patent Judge*.

DECISION

Granting Institution of *Inter Partes* Review

35 U.S.C. § 314

Dismissing Contingent Motion for Joinder

35 U.S.C. § 315(c); 37 C.F.R. § 42.122

I. INTRODUCTION

Mercedes-Benz USA, LLC (“Petitioner”) filed a petition to institute *inter partes* review of claims 1–5, 7, and 13–18 of U.S. Patent No. 8,775,833 B2 (Ex. 1001, “the ’833 patent”). Paper 3 (“Petition” or “Pet.”). Petitioner also filed a Contingent Motion for Joinder to *Qualcomm Inc. v. Daedalus Prime LLC*, IPR2023-00550. Paper 2. Daedalus Prime LLC (“Patent Owner”) filed an Opposition to Petitioner’s Motion for Joinder (Paper 7) and waived any preliminary response (Paper 9).

We have authority under 35 U.S.C. § 314 to determine whether to institute an *inter partes* review. The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Upon considering the Petition and evidence of record, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of the challenged claims of the ’833 patent. Accordingly, we institute an *inter partes* review of claims 1–5, 7, and 13–18 of the ’833 patent on the grounds asserted in the Petition.

The following preliminary findings of fact and conclusions of law are made solely for determining whether to institute review. Any final decision will be based on the full trial record.

II. BACKGROUND

A. *Related Matters*

Petitioner identifies the following non-PTAB proceedings as related matters involving the ’833 patent:

- (1) *Daedalus Prime LLC v. Arrow Electronics, Inc. et al.*, 1:22-cv-01107 (D. Del.);
- (2) *Daedalus Prime LLC v. Mazda Motor Corporation et al.*, 1:22-cv-01109 (D. Del.);
- (3) *Daedalus Prime LLC v. Mazda Motor Corporation et al.*, 1:22-cv-01108 (D. Del.);
- (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352 (E.D. Tex.);
- (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, U.S. International Trade Commission (“ITC”) Inv. No. 337-TA-1335 (Violation); and
- (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, ITC Inv. No. 337-TA-1332 (Violation).

Pet. 2; *accord* Paper 6 (Patent Owner’s Mandatory Notices).

We note that the petition to which Petitioner has moved to join, IPR2023-00550, has been terminated after institution due to a settlement between the parties. *Qualcomm Inc. v. Daedalus Prime LLC*, IPR2023-00550, Paper 22 (entered Jan. 12, 2024).

B. Real Parties in Interest

Petitioner identifies Mercedes-Benz USA, LLC; Mercedes-Benz Intellectual Property GmbH & Co. KG; Mercedes-Benz Group AG; and Mercedes-Benz AG as its real parties in interest. Pet. 2.

Patent Owner identifies Daedalus Prime LLC as its real party in interest. Paper 6, 1.

C. Overview of the ’833 patent

The ’833 patent, titled “Dynamically Allocating a Power Budget Over Multiple Domains of a Processor,” relates to “a power balancing mechanism that can be implemented between the different domains of a multicore

processor.” Ex. 1001, code [54], 2:14–17. As background, the ’833 patent states that “[o]ne issue that arises” with multicore processors “is that the different circuitry can consume differing amounts of power based on their workloads,” but that “suitable mechanisms to ensure that these different units have sufficient power do not presently exist.” *Id.* at 1:22–26.

The ’833 patent purports to solve this problem by providing a power budget management (“PBM”) algorithm that dynamically apportions power among multiple domains at run time. *Id.* at 1:56–58; *see also id.* at 2:14–17 (“Thus embodiments provide a power balancing mechanism that can be implemented between the different domains of a multicore processor.”). According to the ’833 patent, the PBM algorithm “may be executed by logic such as logic of a power control unit (PCU) of a processor to control the power of an entire processor or an individual domain to a configured power limit.” *Id.* at 2:32–36. The algorithm is based, in part, on “various processor parameters.” *Id.* at 2:36–37. These parameters include guaranteed frequency (P1), “which is a frequency that a domain is guaranteed to operate at and not exceed power or thermal specifications of the product,” and maximum turbo frequency (P0), “which is a highest frequency at which a domain can operate.” *Id.* at 2:37–40, 3:1–3.

Figure 7, reproduced below, is a block diagram of one embodiment of a multicore processor according to the ’833 patent. *Id.* at 1:48–50.

400

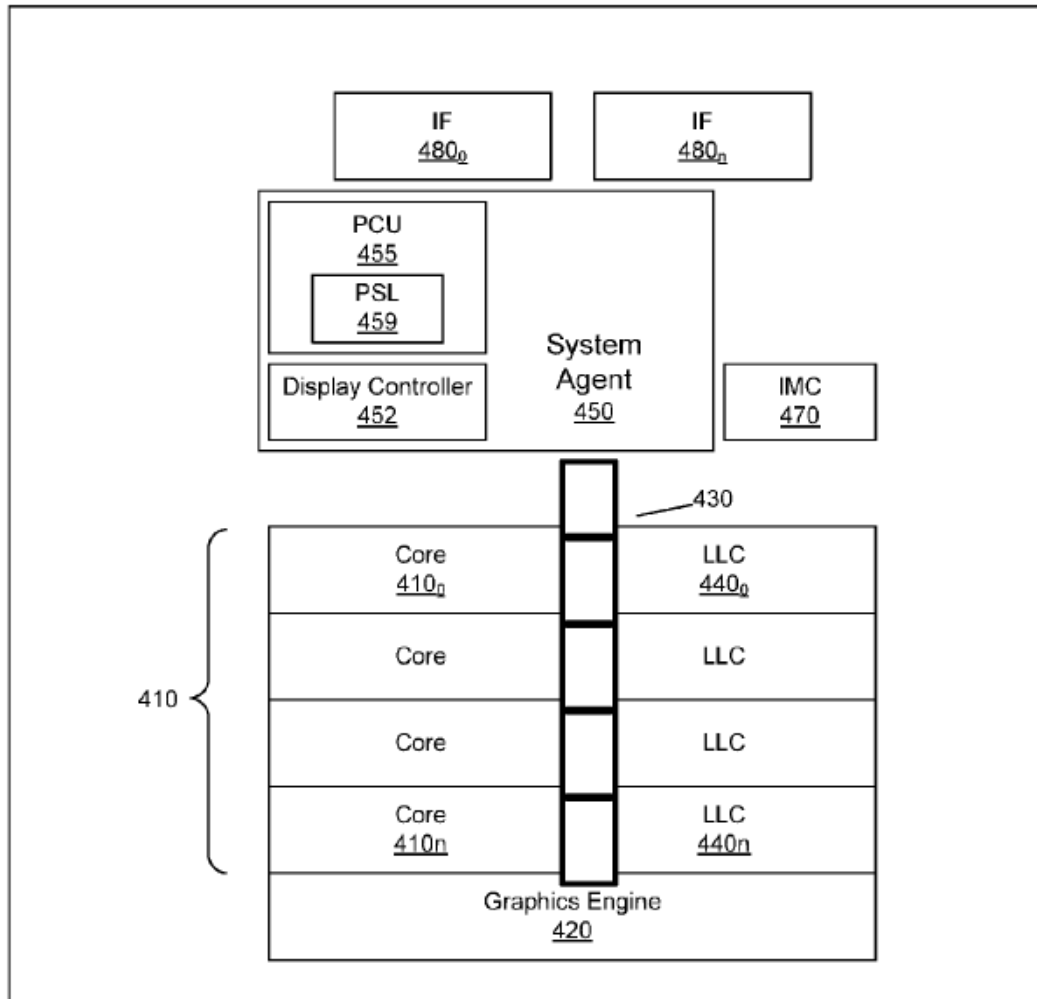


FIG. 7 is a block diagram of a processor according to the '833 patent.

As shown, processor 400 includes: (1) a core domain 410 having a plurality of cores 410_a–410_n; (2) last level caches (LLC) 440_o–440_n; (3) a graphics domain 420 having one or more graphics engines; and (4) a system agent domain 450. *Id.* at 9:10–15, 9:33–35. A ring interconnect 430 couples the cores, and further interconnects the cores, graphics domain 420, and system agent domain 450. *Id.* at 9:40–44.

The system agent domain 450 includes a display controller 452 that provides a user interface, and a power control unit 455 having power sharing logic 459 to “execute algorithms . . . to thus dynamically share an available package power budget between the core domain and the graphics domain.” *Id.* at 9:50–54. The ’833 patent states that system agent domain 450 “may execute at a fixed frequency and may remain powered on at all times to handle power control events and power management such that domains 410 and 420 can be controlled to dynamically enter into and exit low power states.” *Id.* at 9:16–21.

D. The Challenged Claims

Petitioner challenges claims 1–5, 7, and 13–18 of the ’833 patent. Pet. 6. Of the challenged claims, claims 1 and 13 are independent. Claims 1 and 13 are illustrative of the claimed subject matter and reproduced below with Petitioner’s added identifiers bolded and in brackets.

1. **[pre]** A processor comprising:

[A] a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency;

[B] a memory controller coupled to the first and second domains;

[C] at least one interface; and

[D.i] first logic to dynamically allocate a power budget for the processor between the first and second domains at run time **[D.ii]** according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.

Ex. 1001, 11:26–38; Pet. 16–26 (identifiers).

13. **[pre]** A system comprising:

[A.i] a multicore processor having a first domain including a plurality of cores, a second domain including a graphics engine, and [A.ii(1)] a third domain including system agent circuitry, [A.ii(2)] the third domain to operate at a fixed power budget and [A.ii(3)] including a power sharing logic to dynamically allocate a variable power budget between the first and second domains [A.ii(4)] based at least in part on a first power sharing value for the first domain stored in a first storage and a second power sharing value for the second domain stored in a second storage; and

[B] a dynamic random access memory (DRAM) coupled to the multicore processor.

Ex. 1001, 12:52–64.

E. Evidence

Petitioner submits the following evidence:

Evidence	Exhibit No.
U.S. Published Patent Appl. No. 2010/0115304 A1 (“Finkelstein”)	1005
U.S. Published Patent Appl. No. 2007/0049133 A1 (“Conroy”)	1006
U.S. Published Patent Appl. No. 2011/0022356 A1 (“Nussbaum”)	1007
U.S. Published Patent Appl. No. 2009/0089602 A1 (“Bose”)	1008

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Claims Challenged	35 U.S.C. §	Reference
1–5, 7	103(a) ¹	Finkelstein

¹ Congress amended §§ 102 and 103, among other sections, when it passed the Leahy-Smith America Invents Act (“AIA”). Pub. L. No. 112–29, § 3(c), 125 Stat. 284, 287 (2011). The AIA’s changes to §§ 102 and 103 impact applications filed on or after March 16, 2013. The ’833 patent is a

Claims Challenged	35 U.S.C. §	Reference
7	103(a)	Finkelstein, Conroy
13–15, 17, 18	103(a)	Nussbaum
16	103(a)	Nussbaum, Bose
13–15, 17, 18	103(a)	Conroy
16	103(a)	Conroy, Bose
1–5, 7, 13–15, 17, 18	103(a)	Conroy, Finkelstein

Pet. 6–7.

G. Overview of the Asserted Prior Art

This Decision involves an analysis of Petitioner’s Finkelstein obviousness ground. We provide a brief overview of Finkelstein before turning to our analysis.

Finkelstein “relates to power management for multiple processor cores.” Ex. 1005 ¶ 1. According to Finkelstein, the power management system improves over the prior art by utilizing local throttling techniques on a per core basis in response to detection of excessive temperature at one or more of the cores. *Id.* ¶ 9.

Figure 1, reproduced below, is a block diagram illustrating one embodiment of Finkelstein’s power management system. *Id.* ¶ 5.

continuation of an application filed on Sept. 6, 2011. Ex. 1001, code (63). Without finding that the ’833 patent is afforded this filing date, we apply it for purposes of this Decision, and use the pre-AIA statutes.

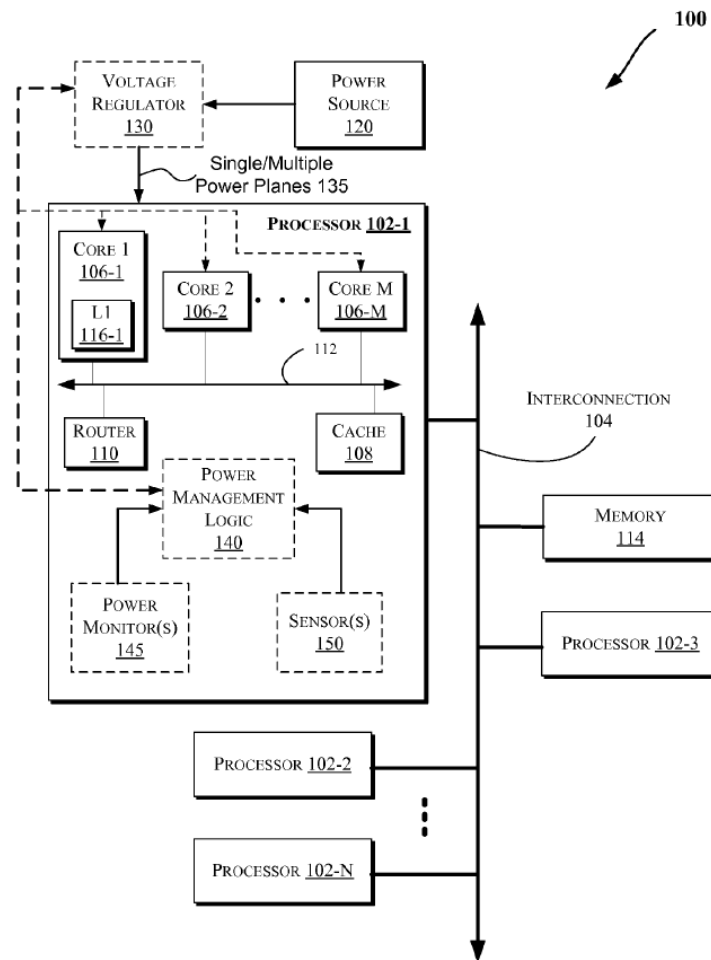


FIG. 1 is a block diagram of a power management system according to Finkelstein.

As shown, computing system 100 includes: (1) power source 120; (2) voltage regulator (“VR”) 130; (3) one or more processors 102-1 to 102-N (called “processor 102” or “processors 102”); (4) memory 114; and (5) bus 104 interconnecting processors 102 and memory 114. *Id.* ¶¶ 10, 13–14. Processor 102, in turn, includes: (1) one or more processor cores 106–1 to 106-M (called “core 106” or “cores 106”); (2) cache 108; (3) router 110, and (4) bus 112 connecting the cores 106, cache 108, and router 110. *Id.* ¶ 11. Processor 102 also includes power management logic 140 that controls power supply to the cores 106. *Id.* ¶ 16.

According to Finkelstein, power management logic 140 receives status information from sensors 150 monitoring the cores and interconnections for variations in, *e.g.*, temperature, operating frequency, operating voltage, power consumption, and inter-core communication activity. *Id.* The logic 140 causes the VR 130, power source 120, and/or individual components (*e.g.*, cores 106) to modify their operations, such as operating frequency and power consumption. *Id.*

III. DISCUSSION

Petitioner contends that claim 1 of the '833 patent is unpatentable under 35 U.S.C. § 103 as obvious over Finkelstein. Pet. 17–27. A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103(a) (2006); *see also KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

In an *inter partes* review, “the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). Petitioner ultimately bears the burden of persuasion to prove unpatentability of each challenged claim by a preponderance of the evidence. 35 U.S.C. § 316(e); *see also Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). The Board may authorize an *inter partes* review if we determine that

the information presented in the Petition and Patent Owner's Preliminary Response shows that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the claims challenged in the petition. 35 U.S.C. § 314(a).

We organize our discussion into three sections. First, we address the level of ordinary skill in the art. Second, we address claim construction. And third, taking account of the information presented, we consider whether the Petition satisfies the threshold requirement for instituting an *inter partes* review under 35 U.S.C. § 314(a).

A. Level of Ordinary Skill in the Art

In assessing the level of ordinary skill in the art, various factors may be considered, including (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983). Not all of these factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, “[t]hese factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art.” *Daiichi Sankyo Co. Ltd, Inc. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

Relying on the declaration testimony of Dr. Horst, Petitioner contends that an ordinarily skilled artisan for the '833 patent:

would have had a bachelor's degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field, and at least two years of experience in the research, design, development, or testing of

electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.

Pet. 9 (citing Ex. 1029 ¶¶ 29–30).

Based on the record presented, including our review of the '833 patent and cited prior art, we agree with Petitioner's proposed definition. Thus, we apply Petitioner's definition for this decision. *See, e.g.*, Ex. 1001, 1:9–26 (describing in the “Background” section of the '833 patent various conventional methods of computation and their alleged deficiencies).

B. Claim Construction

In interpreting the claims of the '833 patent, we “us[e] the same claim construction standard that would be used to construe the claim[s] in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). The claim construction standard includes construing claims in accordance with the ordinary and customary meaning of such claims as would have been understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (*en banc*).

Petitioner states that it “does not believe that any term requires explicit construction.” Pet. 10 (citing Ex. 1002 ¶ 66).

Having considered the record, we conclude that no terms require express interpretation at this time. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Asserted Grounds of Unpatentability

Petitioner contends that claims 1–5 and 7 of the ’833 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Finkelstein. Pet. 17–34. As stated above, Patent Owner did not file a preliminary response. We focus our analysis on independent claim 1.

As to the preamble² (i.e., “[a] processor comprising”), Petitioner has sufficiently shown that Finkelstein’s processor 102-1 satisfies the “processor” recited in the preamble. *See* Pet. 17–18 (citing Ex. 1005, Fig. 1; Ex. 1029 ¶¶ 68–70).

Limitation 1[A] recites “a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency.” Ex. 1001, 11:27–29. Petitioner contends that Finkelstein’s multiple power planes 135 satisfy this limitation. Pet. 18–20 (citing Ex. 1005 ¶¶ 14, 16, 24, 27, 32, 39, Fig. 1; Ex. 1029 ¶¶ 71–75). Specifically, Petitioner contends that Finkelstein’s multiple power planes (each including a set of processor cores) encompass the claimed first and second domains, and that each power plane operates at an independent voltage and frequency. *Id.* Petitioner contends that, because Finkelstein teaches that its power management logic can “throttle or modify an operational characteristic of *one* or more of the cores 106 (such as an operating voltage and/or an operating frequency of *a processor core* 106),” a person of ordinary skill in the art would have considered it obvious to operate the cores (and thus the

² Petitioner does not take a position on whether the preambles to the claims are limiting. At this stage of the proceeding, we accept Petitioner’s showing that the preamble is taught by the prior art, without deciding whether the preamble is limiting.

claimed domains) at independent voltages and frequencies. *Id.* at 20 (quoting Ex. 1005 ¶ 24). On this record, Petitioner’s position is persuasive. For example, Finkelstein discloses that its power management logic 140 can “throttle or modify” operating voltage and/or operating frequency “of a processor core 106.” Ex. 1005 ¶ 24 (emphasis added). This disclosure appears to support Petitioner’s contention that the domains can operate at an independent voltage and frequency as claimed.

As to limitation 1[B], (i.e., “a memory controller coupled to the first and second domains”), Petitioner has sufficiently shown that Finkelstein’s memory controller or hub satisfies this claim limitation. *See* Pet. 21–22 (citing Ex. 1005 ¶¶ 11, 13, 49, Figs. 1, 7; Ex. 1029 ¶¶ 76–79).

As to limitation 1[C] (i.e., “at least one interface”), Petitioner has sufficiently shown that Finkelstein’s disclosure of “buses or interconnections (such as a bus or interconnection 112)” satisfies this claim limitation. *See id.* at 22–23 (citing Ex. 1005 ¶¶ 10–13, 47, 48, Fig. 1; Ex. 1029 ¶¶ 80–82).

Limitation 1[D.i] recites “first logic to dynamically allocate a power budget for the processor between the first and second domains at run time.” Ex. 1001, 11:33–35. For this limitation, Petitioner relies on Finkelstein’s disclosure of the “processors having multiple power planes” that, because they “shar[e] the same power source 120,” also “share a common package power/energy budget.” Pet. 23–35 (citing Ex. 1005 ¶¶ 19, 22, 24, 26, 29–31, 35; Ex. 1029 ¶ 84). Petitioner contends that a person of ordinary skill in the art “would have recognized that Finkelstein teaches allocating a power budget between the first and second domains ‘at run time,’” because Finkelstein teaches that “unused processor core power” can be used for “more Graphics Effect(s) (GFX) performance in a GFX intensive

workload.” *Id.* at 24 (citing Ex. 1005 ¶ 26; Ex. 1029 ¶ 84). Petitioner correlates the “unused processor core power” as that from the claimed first domain, and the GFX performance to “a core in the second domain.” *Id.* Petitioner’s position is persuasive on this record. For example, Finkelstein discloses that processors having multiple power planes may share “the same power source 120” and, correspondingly, “a common package power/energy budget.” Ex. 1005 ¶ 26. We credit Dr. Horst’s un rebutted testimony that graphics effects are “being performed by a core in the second domain (e.g., Core 2)” as claimed. Ex. 1002 ¶ 84.

Turning to the final limitation of claim 1, limitation 1 [D.ii] recites “according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.” Ex. 1001, 11:35–38. For this limitation, Petitioner relies on two “approaches” in Finkelstein that Petitioner contends “dynamically allocate a power budget according to a first sharing policy value for the first domain and a second sharing policy value for the second domain.” *See* Pet. 25–27 (describing the “first approach” as involving a set of energy sharing policy values for each plane “i” and the “second approach” involving a set of sharing policy values based on Thermal Design Power (TDP) power limit).

We discuss the first approach as an example. In this approach, Petitioner relies on Finkelstein’s equation:

$$E^{k,i} = W_{ki} E^k$$

Id. at 25–26. Petitioner contends that $E^{k,i}$ represents the “budget” for a particular power plane i , and that vectors W_{ki} —which Petitioner asserts are

used to represent the claimed first and second sharing policy values—are used to determine $E^{k,i}$. *Id.* at 25 (citing Ex. 1005 ¶ 34). Petitioner also contends that W_{k1} and W_{k2} (i.e., the policy sharing values for the first domain and second domain, respectively), are controllable by user-level software, such as via a graphical interface. *Id.* at 26 (citing Ex. 1005 ¶¶ 34–35; Ex. 1029 ¶ 88).

Petitioner’s position is persuasive on this record. Petitioner sufficiently shows that Finkelstein teaches a power management approach where unused power from one power plane may be distributed to another power plane based on sharing policy values represented by W_{ki} . Indeed, Finkelstein teaches that, for “different power planes,” “user (or application defined) preferences that describe how budget E^k is distributed among power planes . . . may be provided as input in the form of vectors W_k .” Ex. 1005 ¶ 34. And Finkelstein teaches that, when power allocated to a particular power plane “is high enough to provide maximal turbo,” “the ‘unused’ budget for this power plane . . . may be distributed among the rest of the power planes proportionally to their weights” (i.e., W_{ki}). *Id.* at 35. Thus, Finkelstein’s disclosure—at least on this record—supports Petitioner’s contentions that the “power budget” is the unused power from one power plane that is available for distribution to the remaining power planes based on their weighted sharing policy values W_{ki} .

For similar reasons, we determine on the current record that Petitioner’s second approach is also persuasive.

Accordingly, for the reasons set forth above and based on the totality of the evidence currently in the record, we are persuaded that Petitioner has

demonstrated a reasonable likelihood of prevailing in its challenge to claim 1 of the '833 patent as unpatentable for obviousness over Finkelstein.

IV. CONCLUSION

After considering the Petition and the evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood of success in proving that at least one claim of the '833 patent is unpatentable. Thus, we institute an *inter partes* review of all challenged claims on all grounds set forth in the Petition. 37 C.F.R. § 42.108(a); *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute to require “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

Our determinations at this stage of the proceeding are based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which we have instituted an *inter partes* review. *See TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner’s burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving invalidity by a preponderance of the evidence at trial”). We will base any final decision on the full record developed during trial.

V. MOTION FOR JOINDER

As discussed *supra*, Petitioner filed a motion for joinder with the '550 IPR in which Qualcomm was the remaining petitioner. Paper 2, 1. Petitioner presented its motion as “contingent”; that is, “should the Qualcomm IPR be terminated prior to any institution decision or otherwise not instituted for any reason, Petitioner submits this motion for joinder

would be moot, and requests the Board consider Petitioner’s *inter partes* review petition on its own merits.” *Id.* As discussed *supra*, the ’550 IPR has been terminated as a result of a settlement. We therefore dismiss Petitioner’s Contingent Motion for Joinder (Paper 2) as moot and proceed based on the merits of the Petition in this case.

VI. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1–5, 7, and 13–18 of the ’833 patent on the unpatentability grounds asserted in the Petition;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision; and

FURTHER ORDERED that Petitioner’s Contingent Motion for Joinder (Paper 2) is dismissed as moot.

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FOR PETITIONER:

Celine Crowson
Celine.crowson@hoganlovells.com

Joe Raffetto
Joseph.raffetto@hoganlovells.com

Scott Hughes
Scott.hughes@hoganlovells.com

Helen Trac
Helen.trac@hoganlovells.com

Ryan Stephenson
Ryan.stephenson@hoganlovells.com

Nicholas Rotz
Nicholas.rotz@hoganlovells.com

FOR PATENT OWNER:

Tarek Fahmi
Tarek.fahmi@ascendalaw.com

Jonathan Tsao
Jonathan.tsao@ascendalaw.com