

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,

Petitioner,

v.

DAEDALUS PRIME LLC,

Patent Owner.

Case No.: IPR2023-01335

U.S. Patent No. 8,775,833

PATENT OWNER'S RESPONSE

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EXHIBIT LIST

EXHIBIT NO.	DESCRIPTION
2001	Transcript of Deposition of Dr. Horst
2002	Declaration of Michael C. Brogioli, Ph.D.
2003	U.S. PGPUB 2010/0162006
2004	U.S. Patent No. 8,924,758
2005	U.S. Patent No. 6,711,691

I. INTRODUCTION AND SUMMARY OF ARGUMENTS

Mercedes-Benz USA, LLC's ("MB USA" or "Petitioner") challenges to the claims of U.S. Patent No. 8,776,833 (the "'833 patent") fail to demonstrate that any challenged claim is unpatentable.

As to the challenges to claim 1 and its dependent claims based on Finkelstein, MB USA fails to demonstrate that Finkelstein teaches or suggests dynamic allocation of a power budget *for a processor*. The petition discusses allocation of "an 'unused' power budget for domain i," that is, $W_{ki}E^k - E_{high}^i$. But even if that distribution can be characterized as "dynamic," the 'unused' budget ($W_{ki}E^k - E_{high}^i$) is *not* a power budget *for an entire processor*. It is merely excess power of a given domain that can be used by another. So, even if the petition has correctly characterized Finkelstein, the petition fails to demonstrate that Finkelstein teaches or suggests dynamic allocation of a power budget for a processor, as recited in claim 1.

Challenges to claim 13 and its dependent claims that rely on Conroy and/or Nussbaum fare no better. For its part, Conroy fails to teach or suggest dynamic allocation of a power budget between domains of a multicore processor according to power sharing values of those domains stored in *different storages*. Conroy instead explains that "a power weighting strategy

is selected based on the load profile by selecting a power distribution table out of a plurality of power distribution tables stored in *a memory* of the system.” This use of a single memory distinguishes Conroy from the claimed subject matter and the petition offers no basis for concluding that a person of ordinary skill in the art would modify Conroy to adopt the claimed approach. Indeed, the petition does not describe any modifications to Conroy at all.

As to Nussbaum, the frequency sensitivities relied on by Petitioner for teaching the claimed power sharing values are not per-domain attributes. They are instead per-core or per-component attributes. Because claim 13 requires multiple cores for at least one domain, a per-core attribute cannot be considered a per-domain attribute, and so the challenge to the patentability of claim 13 in light of Nussbaum fails.

Finally, the challenge in view of a proposed Conroy-Finkelstein combination also fail. The petition fails to convincingly demonstrate that a person of ordinary skill in the art would have been motivated to combine the teachings of these references. And, if they were considered in combination, that combination does not yield the invention recited in the challenged claims. For example, the petition fails to show that the combination teaches

or suggests “each of the first and second domains to operate at an independent voltage and frequency,” as recited in claim 1.

For these and further reasons as discussed in this Patent Owner Response, the Board should not find any of the challenged claims unpatentable.

II. BACKGROUND, THE '833 PATENT, AND CLAIM CONSTRUCTION

A. Background

Modern computing devices make use of processors that combine previously-independent components within a single integrated circuit package. Ex. 1001 at 1:11-16. Consequently, multicore processors have become available and even these processors have been extended to include additional functionalities. *Id.* at 1:17-22. With this increase in functionality, however, complications arise. One such complication is the need to manage the differing amounts of power consumed by the different circuitry within the integrated circuit. *Id.* at 1:22-26; *and see* Ex. 1005 at [0002].

The amount of power consumed by a processor core or other component of an integrated circuit is impacted by, among other things, the voltage levels supplied to it and the frequency at which it operates. Ex. 1029 at ¶ 43. Generally, increased processing capabilities demand higher voltages

and operating frequencies and so correspond with higher power consumption *Id.* at ¶¶ 43-44. “But, increased power consumption leads to an increase in waste heat, which can damage an integrated circuit.” Ex. 2002 at ¶ 27 (citing Ex. 1005 at [0002]). Hence, there is a need for power management in modern integrated circuits.

B. The '833 Patent

The '833 patent proposes an approach for managing power consumption within integrated circuits, such as those used for multicore processors. Ex. 1001 at Abst.; 1:56 – 2:4. According to various embodiments, different componentry of the integrated circuit, such as processor cores, non-core processing engines such as graphics engines, and other units are divided into different “domains,” and each domain is dynamically allocated a portion of an overall power budget for the integrated circuit. *Id.* at 1:56 – 2:31. Figure 7 of the '833 patent, reproduced below, illustrates an example in which a multi-domain processor 400 includes a first domain that includes processor cores 410, a second domain that includes a graphics engine 420, and a third domain that includes system agent circuitry 450. *Id.* at 9:12-25. Allocating an overall power budget for processor

400

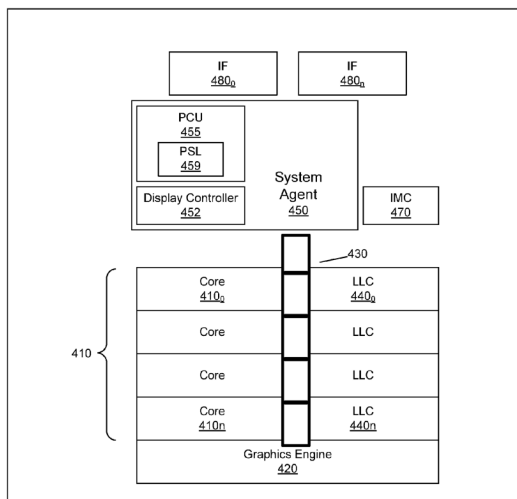


FIG. 7

400 allows dynamic redistribution of power between these different domains, “enabling flexibility to handle various different workload requirements.” *Id.* at 10:25-28.

This approach for power management represented a departure from previous approaches. For example, prior to the '833 patent, it was believed that a system-level approach to power management was inefficient: “[A] graphics subsystem might at certain times be unable to utilize additional power resources ... Similarly, the graphics subsystem might use the additional power but not provide a result that is valuable. In either case, it may be impractical to have a system-wide power management device determine the most efficient way to allocate an overall thermal budget.” Ex. 2003 at [0002]. Accordingly, earlier approaches focused on delivering set

amounts of power to various components, and giving consideration to how much of that power to use at the local component level.

The prior art also identified difficulties associated with dynamic power allocation. For example, dividing a system-on-a-chip (“SoC”) into separate power domains, as in embodiments of the ’833 patent, introduces interactions between components and delays associated with such management:

The on-die interaction of different processors and computational blocks within an integrated circuit such as an SOC may be complex and lead to inefficient communication and resource management. Power management and performance may each degrade due to these inefficiencies.

Ex. 2004 at 1:44–48. In fact, “conventional power management control of processing engines, [] simply acts to select one or more engines to be placed into a low power state, but does not provide for the dynamic power sharing of a power budget between domains” Ex.1001 at 10:8-13; *and see* Ex. 2005 at 1:46–49 (“[C]onventional power management for multi-processor computer systems has not been efficient. Hence, large amounts of power are consumed by these multiprocessor computer systems even when there is no activity.”).

As mentioned above, in embodiments of the '833 patent processing components are assigned to separate power domains and an overall power budget is dynamically allocated between those domains. In particular, the overall power budget is allocated between separate power domains according to *sharing policy values* for each of the domains. Ex. 1001 at 1:55 – 2:31; 4:1-56; 10:25-28. The sharing policy values identify preferences for power allocation, and are controllable by user-level software “to enable the software to determine how package power budget is shared between different domains.” *Id.* at 4:1-7. This allows the power budget to be intelligently allocated to domains that need processing power, and away from domains that do not. For example, one policy sharing value can indicate an amount of a power budget to supply to a CPU core domain, while a second sharing policy value can indicate an amount for a GPU domain. *Id.* at 4:21-56; 5:8-15; 6:29-39. Additionally, certain amounts of the power budget may be *reserved* for use by one or more domains. *Id.* at 5:49-64.

Allocation of the power budget is handled by power management logic on the integrated circuit. *Id.* at 9:48-54. The power management logic can account for not only the policy sharing values, but also the individual domains' respective workload. *Id.* at 2:11-14; 5:2-12. The use of a central

power management logic and policy sharing values allows a processor, such as processor 400 shown in Fig. 7, above, to shift power budget allocations between domains efficiently. For example, rather than components having set power allocations that are either used or unused, the power management logic can reallocate unused or inefficiently allocated power (e.g., in one domain) to other components (e.g., in a different domain). Therefore, “embodiments provide a mechanism to dynamically share the power budget between different compute components in the same die. As a result, a power budget or power headroom can be reallocated between cores and graphics engine when they are both integrated on the same die.” *Id.* at 10:16-18.

C. The Challenged Claims

In keeping with the above-described teachings, claim 1 of the '833 patent recites:

A processor comprising:

a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency;

a memory controller coupled to the first and second domains;

at least one interface; and

first logic to dynamically allocate a power budget for the processor between the first and second domains at run time according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.

Id. at 11:26-38.

Independent claim 13 recites,

A system comprising:

a multicore processor having a first domain including a plurality of cores, a second domain including a graphics engine, and a third domain including system agent circuitry, the third domain to operate at a fixed power budget and including a power sharing logic to dynamically allocate a variable power budget between the first and second domains based at least in part on a first power sharing value for the first domain stored in a first storage and a second power sharing value for the second domain stored in a second storage; and

a dynamic random access memory (DRAM) coupled to the multicore processor.

Id. at 12:52-64.

D. Claim Construction and the Level of Ordinary Skill in the Art

In *inter partes* reviews such as this one, the Board applies the same claim construction standard used to construe a claim in a civil action under 35 U.S.C. § 282(b). *Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51,340 (Oct. 11, 2018). Accordingly, the claims should be construed consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art as considered in the context in which the terms of the claims are used. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *see also ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) (“the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms”). “The ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Phillips*, 415 F.3d at 1313. Furthermore, constructions are needed only to the extent necessary to resolve any asserted ground in the petition. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (only “terms ‘that are in controversy, and only to the extent necessary to resolve

the controversy’” need be construed) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

In its Institution Decision, the Board assessed MB USA’s proposed level of ordinary skill in the art as being “consistent with the prior art.” Paper 10 at 15. That proposed level of ordinary skill is: a person with “a bachelor’s degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field” who would have had “at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.” Pet. 14–15. The proposed definition is flawed insofar as it encompasses people with more than ordinary skill in the art—that is, by encompassing people with “at least” two years of experience in the designated field, it includes persons with far greater levels of experience and, therefore, is not limited to just persons of *ordinary skill* in the art. Patent Owner therefore uses the proffered definition of a person of ordinary skill in the art, but limits such individuals to those with two years of experience in the designated field in the analysis below. *See* Ex. 2002 at ¶ 25.

Although the Board did not make any claim constructions as part of its Institution Decision, *see* Paper 10 at 12, certain terms of the claims will be important for understanding distinctions from the prior art cited by Petitioner:

1. An Independent Voltage and Frequency

Claim 1 recites “each of the first and second domains to operate at an *independent* voltage and frequency.” Ex. 1001 at 11:27-29 (emphasis added). At deposition, Petitioner’s declarant, Dr. Horst, testified that in this context “independent” means “different” and that this was how he interpreted the claims for purposes of his analysis. Ex. 2001 at 16:15 – 17:7. Dr. Horst is wrong.

The ’833 patent uses the term “independent” in several places:

Reference	Passage (emphasis added)
1:13-17	Over time, processor designs have evolved from a collection of <i>independent</i> integrated circuits (ICs), to a single integrated circuit, to multicore processors that include multiple processor cores within a single IC package.
1:63-66	Such processor can include at least two <i>independent</i> domains, one associated with the cores (referred to herein as a core

	domain) and one associated with a graphics engine (referred to herein as a graphics domain).
7:59-62	As seen, each domain may have an <i>independent</i> specification power level, which may correspond to a P1 or thermal design power level, which is the maximum guaranteed frequency at which the domain can execute.
8:27-31	In one embodiment, each such core may be of an <i>independent</i> power domain and can be configured to operate at an <i>independent</i> voltage and/or frequency, and to enter turbo mode when available headroom exists.
8:38-46	In various embodiments, power control unit 355 may include a power sharing logic 359 , which may be a logic to perform dynamic control and re-allocation of an available power budget between multiple <i>independent</i> domains of the processor. In the embodiment of FIG. 6, assuming that each core is of an <i>independent</i> power domain, logic 359 can calculate an available power budget for a given time interval and dynamically allocate portions of this available power budget to the different cores.

10:4-8	Thus in various embodiments, a technique is provided to enable selection of how much of a common power envelope can be allocated to each of multiple <i>independent</i> power domains of a semiconductor device.
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In each instance, the term “independent” is used in its ordinary sense to mean “separate.” *See* Ex. 2002 at ¶¶ 32-35. In other words, claim 1 is reciting, “a voltage and frequency of the first domain and the second domain that are controlled separately from one another.” *Id.* at ¶ 32.

Understanding the claim in this fashion comports with the use of the term “independent” in the ’833 patent. *See Phillips*, 415 F.3d at 1315 (“[T]he specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.”) (citation omitted). For example, the specification describes a “domain” as “a collection of hardware and/or logic that operates at the same voltage and frequency point.” Ex. 1001 at 1:58–60; 1:63–66 (in one embodiment, a “processor can include at least two independent domains, one associated with the [processor] cores (referred to herein as a core domain) and one associated with a graphics engine (referred to herein as a graphics domain)”; 2:22–25 (“As another example, each core can be

allocated to a different domain”). The specification further describes that each domain can consume a different “allocated portion[]” of a “power budget,” where the domain’s power consumption is dependent upon the voltage and frequency at which the domain is controlled to operate. *Id.* at Abst.; 1:56–58 (“a power budget of a processor including multiple domains can be dynamically apportioned at run time”); 7:20–24 (“[T]he graphics domain receives ... a portion of the budget [T]he core domain receives ... a portion of the budget”); 5:9–12 (describing that each respective portion of the processor’s power budget “*can be allocated to each of the domains by controlling their frequency and/or voltage accordingly*”) (emphases added). In one embodiment, “power sharing logic of a PCU [power control unit] or other power controller” controls “frequency and/or voltage of these domains ... based on the allocated portion of the power budget.” *Id.* at 2:34; 5:21, 40–44; 8:38–42; 2:32–36 (describing that the PCU can execute “a power budget management (PBM) algorithm” to “control the power”); 5:27–44 and Fig. 1 (referring to a processor’s ability to “Control First and Second Domain’s Frequency and Voltage ...” at step 120). Thus, a person of ordinary skill in the art would recognize that the ’833 patent is describing a situation in which voltages and/or frequencies of the different domains are controlled separately from one another. Ex. 2002 at ¶ 33.

But the fact that these voltages and/or frequencies are controlled *separately* does not require that they must be *different* from one another, as Dr. Horst apparently believes. According to the specification, in the general case of “N” domains, a power budget may be divided amongst the domains according to:

$$E_{domain(x)} = E_n * BIAS_x$$

Ex. 1001 at 4:50 (Equation (5)). The BIAS term is calculated based on each respective domain’s sharing policy value, *id.* at 5:53-56, but there is no prohibition against two (or more) domains each being allocated a same amount of power. Said differently, nothing requires the domains to have different power allocations. Ex. 2002 at ¶ 35.

Finally, to be clear, the requirement for the voltage and frequency of a first domain to be “independent” of (*i.e.*, controlled separately from) the voltage and frequency of a second domain does **not** preclude the voltage and frequency of the first domain from having a relationship to, or dependency on, the voltage and frequency of the second domain. For example, the specification describes the following embodiments of “equations [that] may govern how the package power budget is shared between core [IA] and graphics [GT] domains”:

$$\text{IA_percentage_of_package_budget} = 0.5 + (\text{POLICY_FIRST} - \text{POLICY_SECOND}) / 62 \quad [2]$$

$$\text{GT_percentage_of_package_budget} = 0.5 + (\text{POLICY_SECOND} - \text{POLICY_FIRST}) / 62 \quad [3]$$

Ex. 1001 at 4:33–42.

As shown by equation [2], the power allocated to the core (IA) domain can be dependent upon ***both*** “POLICY_FIRST,” which is a value indicative of the power to be allocated to the core domain, ***and*** “POLICY_SECOND,” which is a value indicative of the power to be allocated to the graphics domain. *Id.* at 4:1–56; 7:42–45. Likewise, equation [3] shows that the power allocated to the graphics (GT) domain can be dependent upon both “POLICY_FIRST” and “POLICY_SECOND.” *Id.* This indicates that while the voltage and frequency of the first domain can be controlled separately from the voltage and frequency of a second domain, these values can nonetheless depend on one another. For example, if the first domain is allocated more power (generally corresponding to setting a higher frequency and/or voltage for the first domain), then the second domain will be allocated less power (generally corresponding to setting a lower frequency and/or voltage for the second domain). *See id.* at 5:8-12 (describing that “based on these policy values and the above Equations 2 and 3” each respective portion of the processor’s power budget “can be allocated

to each of the domains by controlling their frequency and/or voltage accordingly”); 2:6–11 (“[T]he higher the frequency at which, e.g., the core domain is operating, the higher the power consumed by the core domain. And in turn, the higher the power consumed by the core domain, there is less power left for the graphics domain to consume and vice versa.”).

As another example, the specification describes embodiments wherein a domain can be controlled to operate in a “turbo mode” corresponding to a higher frequency when “available headroom exists” within a power budget shared by multiple domains. *See id.* at 8:27–31; 3:1–26. Thus, notwithstanding that a domain’s “turbo frequency ... can be set on a per domain basis,” whether a domain is controlled such that it is set at its turbo frequency at a particular point in time can depend on whether other domains of the processor are also operating, for example, in a turbo mode. *Id.* at 3:11–12; 7:62–65; 8:16–31.

Accordingly, because the specification describes that the voltage and frequency of the first domain can have a relationship to, or dependency on, the voltage and frequency of the second domain, these embodiments cannot be excluded from the scope of the claim term “an independent voltage and frequency.” *Ex. 2002 at ¶ 36; and see C.R. Bard, Inc. v. U.S. Surgical Corp.*,

388 F.3d 858, 865 (Fed. Cir. 2004) (a construction that excludes preferred embodiments is “rarely, if ever, correct”).

E. The IPR Petition

In its petition, MB USA presents multiple grounds for the alleged unpatentability of the claims of the ’833 patent. Pet. at 6-7. In particular,

Claims Challenged	35 U.S.C. §	References
1-5, 7	103	Finkelstein ¹
7	103	Finkelstein in view of Conroy ²
13-15, 17, 18	103	Nussbaum ³
16	103	Nussbaum in view of Bose ⁴
13-15, 17, 18	103	Conroy
16	103	Conroy in view of Bose
1-5,7, 13-15, 17, 18	103	Conroy in view of Finkelstein

Id.

¹ US PG PUB 1010/0115304 (Ex. 1005).

² US PG PUB 2007/0049133 (Ex. 1006).

³ US PG PUB 2011/0022356 (Ex. 1007).

⁴ US PG PUB 2009/0089602 (Ex. 1008).

III. THE PETITION FAILS TO DEMONSTRATE THAT ANY CHALLENGED CLAIM IS UNPATENTABLE

A petition must be judged as it is written. The Board may not overlook flaws in the petition or reformulate its challenges to enhance their suitability. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (“[I]t’s the petitioner, not the Director, who gets to define the contours of the proceeding.”); *see also id.* (“[T]he petitioner is master of its complaint . . .”); *see also id.* at 1353 (forbidding the Board from “curat[ing]” the petition). Furthermore, because all of the challenges in the petition rely on conclusions of obviousness, the analyses set forth in the petition must include “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR Int’l v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (*quoting In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). The challenger must supply the factual basis for the challenge and “may not resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis.” *In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967). Additionally, in cases such as the present, where the obviousness challenges involve a modification or combination of teachings, the Petitioner must also establish that one skilled in the art would have had a reasonable expectation of success to make the modification or combination. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367-

68 (Fed. Cir. 2016). The modification or combination must not “require a substantial reconstruction and redesign of the elements” in a reference or “a change in the basic principles under which [a reference] was designed to operate.” *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959). Nor can the modification or combination render a reference unsatisfactory or “inoperable for its intended purpose.” *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984).

Also, the prior art must be considered for all that it teaches, and a *prima facie* case of obviousness may be rebutted “by showing that prior art teaches away from claimed invention in any material respect.” *In re Peterson*, 315 F.3d 1325, 1331 (Fed. Cir. 2003).

Last but not least, obviousness cannot be established by hindsight combination to produce the claimed invention, as the Supreme Court has emphasized:

A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning. *See Graham [v. John Deere Co.]*, 383 U.S. [1,] 36, 86 S. Ct. 684, 15 L. Ed. 2d 545 [(1966)] (warning against a “temptation to read into the prior art the teachings of the invention in issue” and instructing courts to “guard against slipping into use of hindsight” (quoting *Monroe*

Auto Equip. Co. v. Heckethorn Mfg. & Supply Co.,
332 F.2d 406, 412 (6th Cir. 1964)).

KSR, 550 U.S. at 421.

As explained below, the petition’s challenge fails to demonstrate that any challenged claim is unpatentable.

A. Finkelstein Fails to Teach or Suggest the Invention Recited in Claim 1

MB USA’s first set of challenges are based on the teachings of Finkelstein. Pet. at 17 *et seq.*

1. Overview of Finkelstein

In the context of systems that employ multiple power planes, Finkelstein describes an approach to power distribution “among different power planes under energy-based definitions.” Ex. 1005 at [0009]; [0027]. Energy-based power management may be performed by controlling the energy budget, defined iteratively as follows:

$$E_{n+1} = \alpha E_n + (TDP_n - P_n)\Delta t_n$$

Id. at [0028]. In this expression, TDP_n is “the Thermal Design Power (TDP) power limit on step n ; P_n is the power spent on step n over time Δt_n , and α is the decay component . . . [and] is defined by the requirements of the time

window size.” *Id.* at [0029]. The TDP values may be provided by a software application or user in some embodiments. *Id.*

Finkelstein indicates that “the system [] may set TDP constraints on each of the power planes separately, or/and set TDP constraints on the whole IC package.” *Id.* at [0031]. Thus, “a set of energy budgets, E_n^k may be maintained, e.g., where k corresponds to a specific constraint, and n to the time step.” *Id.* For each power plane, i, a controller function $f^i(E)$ is defined. The controller function maps an energy budget for the power plane onto a set of discrete power states, for example:

$$f^i(E) = P_n^i, E \leq E_{low}^i$$

$$f^i(0) = P_1^1$$

$$f^i(E) = P_0^i, E \geq E_{high}^i$$

where P_0^i is the maximal turbo state for power plane i, and P_n^i is the maximal efficiency state in a case where a controller maps a range of energy values $[E_{low}^i, E_{high}^i]$ onto a discrete range of $[P_n^i, P_0^i]$. *Id.* at [0032].

For each constraint, k, user- or application-defined preferences that describe how budget E_k is distributed among the power planes may be determined and provided in the form of a vector, W_k , of length m, such that entry i corresponds to the portion of the budget that goes to power plane i.

Id. at [0034]. Thus, in the general case, power plane i may obtain the portion of the budget:

$$E^{k,i} = W_{ki}E^k$$

Id. And, in the event a power plane is allocated excess power budget, that excess, $W_{ki}E^k - E_{high}^i$, may be distributed among the rest of the power planes proportionally to their weights. *Id.* at [0035].

2. The petition fails to show that Finkelstein teaches or suggests dynamic allocation of a power budget for a processor, as claimed

To find a claim unpatentable for obviousness, even “single reference obviousness” as advanced by MB USA in its petition, *see* Pet. at 5 n.4, it is necessary to show that “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.” *Takeda Chem. Indus., Ltd. v. Alphapharm Pty, Ltd.*, 492 F.3d 1350, 1354-1355 (Fed. Cir. 2007) (quoting 35 U.S.C. §103(a)). This necessarily requires, among other things, determining the scope and content of the prior art. *KSR*, 550 U.S. at 406-407. And, while the obviousness analysis is flexible, what is not flexible is the need to consider all of the limitation of a claim and find, based on a reasoned analysis, they

are present, before concluding the claim is obvious. *See, e.g., Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016) (“[R]eferences to ‘common sense’—whether to supply a motivation to combine or a missing limitation—cannot be used as a wholesale substitute for reasoned analysis and evidentiary support, especially when dealing with a limitation missing from the prior art references specified.”).

In the present case, MB USA fails to demonstrate that Finkelstein teaches or suggests dynamic allocation of a power budget for a processor, as recited in claim 1. According to the petition,

Finkelstein discloses implementations in which an “unused” budget for domain i , defined as a variable $W_{ki}E^k - E_{high}^i$, is “distributed among the rest of the power planes [domains] proportionally to their weights,” defined as variables W_{ki} . A POSITA would have recognized such an allocation, where the power budget itself is a variable $(W_{ki}E^k - E_{high}^i)$ and the variable power budget is being distributed based on variable weights (W_{ki}) , as a “dynamic” allocation because the allocation can change during run-time to correspond to the then-present operating conditions.

Pet. at 24 (citing Finkelstein at ¶ 35). Assuming the petition accurately describes Finkelstein as teaching the distribution of “an ‘unused’ budget for

domain i,” that is, $W_{ki}E^k - E_{high}^i$, and even if that distribution can be characterized as “dynamic,” the ‘unused’ budget for domain i ($W_{ki}E^k - E_{high}^i$) is **not** a power budget *for a processor*, as required by claim 1. Ex. 2002 at ¶ 41.

Claim 1 is unambiguous in terms of its requirements. The recited “first logic” is to “dynamically allocate *a power budget for the processor* between the first and second domains at run time.” Ex. 1001 at 11:33-35. This is consistent with the specification at 4:43 *et seq.*, which describes allocation of a “package power budget” over N domains according to sharing policy values of those domains. Stated simply, the required power budget to be distributed is that for the entire processor, not merely a domain of the processor.

The petition fails to address this requirement of the claim and instead demonstrates how Finkelstein allegedly teaches the distribution of “an ‘unused’ budget for domain i,” $W_{ki}E^k - E_{high}^i$. Pet. at 24. The “unused” budget of a given domain “i” of a processor is **not** the power budget of the entire processor. Ex. 2002 at ¶ 41. So, even if the petition has correctly characterized Finkelstein, the petition fails to demonstrate that Finkelstein teaches or suggests dynamic allocation of a power budget for a processor, as recited in claim 1. As a result, the petition fails to set forth a prima facie case

of obviousness of claim 1 in view of Finkelstein, *CFMT, Inc. v. Yieldup Intern. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003), and likewise fails to satisfy its obligation to “specify where each element of the claim is found in the prior art.” 37 C.F.R. § 42.104(b)(4).

B. Claims Depending from Claim 1 are Not Obvious in View of Finkelstein

Challenged claims 2-5 and 7 depend, or indirectly, from claim 1. Each respective dependent claim is not unpatentable in view of Finkelstein for at least the same reasons as independent claim 1. *Hartness Int’l. Inc. v. Simplimatic Engineering Co.*, 819 F.2d 1100 (Fed. Cir. 1987).

C. Claim 7 is Not Obvious in View of Finkelstein and Conroy

Claim 7 depends from claim 1 and recites “wherein the first logic is to dynamically allocate substantially all of the power budget to the first domain for a first workload, and to dynamically allocate substantially all of the power budget to the second domain for a second workload executed after the first workload.” Ex. 1001 at 12:1-6. To the extent the petition alleges that claim 7 would have been obvious in view of the combined teachings of Finkelstein and Conroy, it relies on Finkelstein for teaching the limitations of claim 1 (which also are present in claim 7). See Pet. at 34-36. AS

demonstrated above, however, claim 1 is not unpatentable in view of Finkelstein, therefore, claim 7 remains patentable over Finkelstein and Conroy for at least these same reasons. *Hartness Int'l. Inc.*, 819 F.2d 1100.

D. Conroy Fails to Teach or Suggest the Invention Recited in Challenged Independent Claim 13

MB USA's challenge to claim 13 based on the teachings of Conroy fails to demonstrate that the claim is unpatentable.

1. Overview of Conroy

Conroy is directed to data processing systems in which “power is redistributed between the sub-systems while tracking [a] load profile.” Ex. 1006 at [0006]. Conroy describes example load profiles in which the power utilization ratio is used to determine the load profile: the load profile is identified based on a utilization factor for each of the subsystems. In one embodiment, “to determine the utilization factor, the actual power used by each of the subsystems is measured. ... the utilization factor is calculated as a ratio of the actual power used by the subsystem to the power allocated to the subsystem.” *Id.*

In Conroy, power throttling of the different components is coordinated and based on the history of power usage. For example, Conroy explains a situation in which a history of power usage affects future power usage:

After time instance (911), a high demand task is received.

The system becomes busy in processing (905) the high demand task. Since the system had low power consumption before the reception of the high demand task, the power management allows the system to remain in the top performance setting for a short period of time.

Thus, the actual power usage (917) increases to above the limit for average power usage. However, in average, the actual power usage is still below the limit.

Id. at [0135]. Conroy explains: “the subsystems may operate at bursts of substantially high power if there is a considerable low power operation, e.g., a [sic] idle time, during the averaging period.” *Id.* at [0195]. This is based on the estimation that prior low power consumption means the temperature is low, so temporary substantial power use will not overheat the component. Overall, therefore, Conroy is directed to short term over-performance based on power usage history during “the averaging period.” This means Conroy is only suitable for short term changes in power allocation. For example, Conroy states “under the control of the dynamic throttling system, the

system processes the high demand task as fast as possible within the limit of power constraint.” *Id.* at [0144].

2. Conroy does not teach or suggest dynamic allocation of a power budget between domains of a multicore processor according to power sharing values of those domains stored in different storages, as recited in claim 13

Claim 13 recites, in part:

a power sharing logic to dynamically allocate a variable power budget between the first and second domains based at least in part on a first power sharing value for the first domain stored in a first storage and a second power sharing value for the second domain stored in a second storage.

Ex. 1001 at 12:52-64. Aspects of this claim are explained in the specification:

[T]he following equations may govern how the package power budget is shared between core and graphics domains:

$$\text{IA_percentage_of_package_budget} = 0.5 + (\text{POLICY_FIRST} - \text{POLICY_SECOND}) / 62 \quad [2]$$

$$\text{GT_percentage_of_package_budget} = 0.5 + (\text{POLICY_SECOND} - \text{POLICY_FIRST}) / 62 \quad [3]$$

More generally, for the case of N domains over which an allocation of a package power budget is based on

priority over these N domains, the following equations can be used:

$$BIAS_x = \frac{POLICY_x}{\sum POLICY_i} \quad [4]$$

$$E_{domain(x)} = E_n * BIAS_x \quad [5]$$

Here a BIAS can be calculated for each domain x based on the policy value (x) of that domain and the sum of total policy values of all the domains, and again Ex is the energy budget at the instant n.

Id. at 4:33–58. As shown by equations [2] and [3], the power allocated to each of a core domain and a graphics domain is dependent upon the parameters “POLICY_FIRST,” which is a value indicative of the power to be allocated to the core domain, and “POLICY_SECOND,” which is a value indicative of the power to be allocated to the graphics domain. *Id.* at 4:1–56; 7:42–45. In the general case of N domains, the power to be allocated to any one domain is dependent upon “the sum of total policy values of all the domains.” *Id.* at 4:53-55; Ex. 2002 at ¶ 44.

With reference to Fig. 19, reproduced below, Conroy describes a “method to dynamically redistribute power by tracking a load profile of a system.” Ex. 1006 at [0198]. According to Conroy, “The method begins with operation 1901 by sensing an actual power used by each of the subsystems

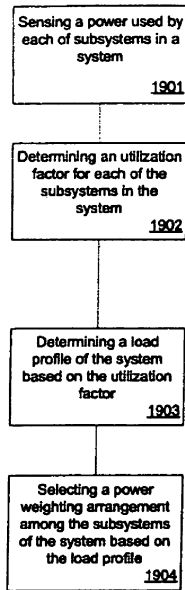


Fig. 19

in a system.” *Id.* from those power measurements, utilization factors for each of the subsystems are determined at 1902 (e.g., as a ratio of the measured power used by the subsystem to a power that is budgeted to the system or the individual subsystem). *Id.* Thereafter, at 1903, a load profile of the system is determined based on the various subsystems respective utilization factors. *Id.* at [0199]. The load profile so determined is then used, at 1904, to select a power weighting strategy, “which may be considered a power weighting arrangement among the subsystems.” *Id.* at [0200].

Conroy explains that “a power weighting strategy is selected based on the load profile by selecting a power distribution table out of a plurality of power distribution tables stored in *a memory* of the system.” *Id.* at [0201]

(emphasis added). Examples of these power distributions tables for a system with two subsystems (a CPU subsystem and a GPU subsystem) are provided in Figs. 21A-21C, reproduced below. *Id.* at [0203]. Each table corresponds to a different load profile and within each table, each row corresponds to a different setting (e.g., clock and voltage setting) for the system for the indicated load profile. *Id.* Each setting is associated with an allocated power, P. *Id.* Selecting the proper table depends on the load profile of the system at a given time. *Id.*

Balanced load profile K1 (e.g., 0.5, 0.5)

2100	2101	2102	2103	2104	
	Settings	CPU	GPU	Allocated Power	
2105	Setting 1	A1 (e.g., 10)	B1 (e.g., 10)	P1 (e.g., 20)	Fig. 21 A
	Setting 2	A2 (e.g., 7)	B2 (e.g., 7)	P2 (e.g., 14)	
	Setting 3	A3 (e.g., 5)	B3 (e.g., 5)	P3 (e.g., 10)	

CPU-heavy load profile K2 (e.g., 0.75, 0.25)

2110	2101	2102	2103	2104	
	Settings	CPU	GPU	Allocated Power	
2105	Setting 1	A1 (e.g., 15)	B1 (e.g., 5)	P1 (e.g., 20)	Fig. 21 B
	Setting 2	A2 (e.g., 10)	B2 (e.g., 4)	P2 (e.g., 14)	
	Setting 3	A3 (e.g., 7)	B3 (e.g., 3)	P3 (e.g., 10)	

GPU-heavy load profile K3 (e.g., 0.25, 0.75)

2120	2101	2102	2103	2104	
	Settings	CPU	GPU	Allocated Power	
2105	Setting 1	A1 (e.g., 5)	B1 (e.g., 15)	P1 (e.g., 20)	Fig. 21 C
	Setting 2	A2 (e.g., 3.5)	B2 (e.g., 10)	P2 (e.g., 14)	
	Setting 3	A3 (e.g., 3)	B3 (e.g., 7)	P3 (e.g., 10)	

The petition alleges,

Conroy further discloses selecting a “power weighting arrangement among the subsystems ... based on the load profile” and states that “the power weighting

arrangement ... may be a power distribution table selected out of a plurality of power distribution tables.” Examples of power distribution tables are illustrated in Figures 21A-C and 22, [] confirming that Conroy discloses dynamically allocating a power budget according to first and second sharing policy values (power weighting arrangement settings selected from a power distribution table based on load profile) for the first and second domains.

Pet. at 59-60 (citing Conroy at ¶¶ 6, 200, Figs. 21A-C, 22). That is, Petitioner’s position is that the contents of the load profile tables—the power weighting arrangement settings—are the power sharing values recited in claim 13.

If that is the case, however, then Conroy certainly does *not* teach or suggest that these alleged “power sharing values” are stored in different storages, as recited in claim 13. Ex. 2002 at ¶ 48. The claim is unambiguous: the first power sharing value for the first domain is stored in a first storage and the second power sharing value for the second domain is stored in a second storage. Conroy, on the other hand, makes clear that all of the power distribution tables, and, therefore, all of the contents of each table, are stored in *a memory*—that is, one memory. *Id.* (citing Conroy at [0201]). Petitioner fails to provide any convincing rationale as to why a person of ordinary skill

in the art would depart from these teachings and instead stored the power distribution tables, let alone the individual contents thereof, in different storages.

The Petition alleges, “Conroy describes an example where [the] power settings are stored in registers. Pet. at 61 (citing Conroy at ¶ 97 (“For example, the microcontroller may store [a] determined throttle setting in a register.”)). Here the petition fails to account for the fact that the “throttle settings” Conroy is referring to are *not* the contents of the power distribution tables, but instead are the actual powers consumed by each subsystem. Ex. 2002 at ¶ 49. With respect to the embodiment cited in the petition, Conroy explains that subsystems may be instrumented, e.g., using sensors, to determine their actual power consumptions, e.g., by measuring currents and or voltages. *Id.* (discussing Conroy at [0093]-[0097]). The microcontroller stores the throttle settings determined by the sensor measurements in registers and uses that information to control the subsystems. *Id.*

The petition goes on to allege, “a POSITA seeking to implement the teachings of Conroy would have found it obvious to use registers to store the various power settings depicted in Conroy’s Figures 7, 21, and 22.” Pet. at 61. This is pure speculation. Insofar as the petition relies on the testimony of Dr. Horst, his declaration testimony merely repeats the same bare allegation

contained in the petition, without any further explanation. Ex. 1029 at ¶ 185. Conclusory opinions of this kind are entitled to little or no weight. 37 C.F.R. § 42.65(a); *and see* PTAB Consolidated Trial Practice Guide at p. 35 (Nov. 2019).

On the other hand, Dr. Brogioli explains why a person of ordinary skill in the art would simply adopt Conroy’s teaching of using a single storage to store the power distribution tables and their contents, as specified. Ex. 2002 at ¶¶ 48, 50. Such an approach is in keeping with Conroy’s desire for simplicity and practices common in the art. *Id.*

Thus, the petition fails to demonstrate that Conroy teaches or suggests a power sharing logic to dynamically allocate a variable power budget between the first and second domains based at least in part on a first power sharing value for the first domain stored in a first storage and a second power sharing value for the second domain stored in a second storage, as recited in claim 13. *Id.* at ¶ 51; *CFMT, Inc.*, 349 F.3d at 1342.

E. Claims Depending from Claim 13 are Not Obvious in View of Conroy

Challenged claims 14, 15, 17, and 18 depend, or indirectly, from claim 13. Each respective dependent claim is not unpatentable in view of

Conroy for at least the same reasons as independent claim 13. *Hartness Int'l. Inc.*, 819 F.2d 1100.

1. Claim 14 has not been shown to be obvious in view of Conroy

Claim 14 depends from claim 13 and recites, “wherein the power sharing logic to determine the variable power budget for a current time interval and to allocate a first portion of the variable power budget to the first domain according to the first power sharing value, and to allocate a second portion of the variable power budget to the second domain according to the second power sharing value.” Ex. 1001 at 12:65 – 13:4. In addition to not being unpatentable in view of Conroy for the reasons set forth above with respect to claim 13, claim 14 has not been shown to be unpatentable for the additional reason that the petition fails to demonstrate that Conroy teaches “a power sharing logic to determine a variable power budget for a current time interval.” Ex. 2002 at ¶¶ 52-55.

With respect to this limitation, the petition alleges,

Conroy uses “the past power usage (e.g., measurements ... at times $T-(n-1)\Delta$, $T-(n-2)\Delta$, ... , T)” to “dynamically determine the allowable power budget” for time interval $T+\Delta$, and allocates this “dynamically determined” power budget to different components of the system. A POSITA

would have understood time interval $T+\Delta$ to be a
“current time interval” because Conroy refers to the time
intervals preceding $T+\Delta$ as being in the “past.”

Pet. at 63 (citations omitted). This is simply untrue. A person of ordinary skill in the art would appreciate that in the series, $T-(n-1)\Delta$, $T-(n-2)\Delta$, ... , T , the value “ T ” represents a *current time*. Ex. 2002 at ¶¶ 53-54 (citing Conroy at [0070]-[0071]). $T+\Delta$ is clearly *a next time interval*, not a current one, and Conroy specifically identifies it as such. *Id.*; Ex. 1006 at [0070]. The petition unconvincingly asserts that a measurement at time T must not be a measurement of current power usage because it is characterized as a “past power usage.” But if the text of Conroy is to be read as literally as the petition insists, then there is no justification for reading what is characterized as allowable power budget for a *next time interval*, $T+\Delta$, as a power budget for a *current* time interval. Ex. 2002 at ¶ 53. The petition cannot read out a statement like this while at the same time as insist that other statements must be accepted as written.

Dr. Brogioli explains that it is clear from Conroy that “actual power usages are measured and a history (n) of such usages are used as a basis to determine a next power usage.” *Id.* at ¶ 54 (citing Conroy at [0069]-[0071]). “For example, in the case of $n=5$, then Conroy would determine the power usage for time $T+\Delta$, the *next* time window, from measurements taken at

times $T-4\Delta$, $T-3\Delta$, $T-2\Delta$, $T-\Delta$, and T .” *Id.* It would make no sense in this scheme for the time $T+\Delta$ to be a *current time*, as the petition alleges, “because by the time that time window is ‘current’ the power allocated for that time period must already be determined and allocated.” *Id.* Conroy’s system for power budget allocation only makes sense if the power budget being determined for allocation is for a next time interval, $T+\Delta$, just as Conroy states, and a person of ordinary skill in the art would recognize as much. *Id.*

Thus, by mischaracterizing Conroy, the petition has failed to demonstrate how claim 14 is obvious in view of that reference and therefore fails to satisfy its obligation to “specify where each element of the claim is found in the prior art.” 37 C.F.R. § 42.104(b)(4).

2. Claim 16 has not been shown to be obvious in view of Conroy-Bose

Claim 16 depends from claim 14 and recites, “wherein the power sharing logic is to increment the first power sharing value when a request for a higher frequency for the first domain is not granted, and to increment the second power sharing value when a request for a higher frequency for the second domain is not granted.” Ex. 1001 at 13:11-16. Insofar as claim 16 depends, indirectly, from claim 13, and the petition relies on Conroy for

teaching or suggesting the limitations of claim 13, then claim 16 is not obvious in view of Conroy-Bose for at least the reasons set forth with respect to claim 13. *Hartness Int'l. Inc.*, 819 F.2d 1100.

Furthermore, claim 16 is separately patentable because a person of ordinary skill in the art would not combine the teachings of Conroy and Bose as alleged in the petition. Ex. 2002 at ¶¶ 56-58. The petition alleges “a POSITA would have understood that Conroy explicitly contemplates not granting a subsystem’s request to increase the system’s setting immediately; instead, Conroy teaches waiting till the next iteration to ‘move[] up’ its system’s setting.” Pet. at 67. This is a mischaracterization of Conroy. First, in Conroy, subsystems do not request increases in system settings. Ex. 2002 at ¶ 57. Instead, and as the petition actually admits, in Conroy, power is allocated among subsystems based on workloads of those subsystems. *Id.*; Ex. 1006 at [0006] (“[P]ower draw is allocated to and allowed for the subsystem having a higher workload.”). As was discussed above with respect to claim 14, Conroy monitors actual power usages to make predictions about the need for power in future time intervals. It is these predictions about power usage that govern how power is allocated among the subsystems. Ex. 1006 at [0072] (“The system is throttled to a setting that will not require power usage more than the dynamically determined budget

(205).”). These settings are used until new power measurements reveal the need for redistribution of the allocated power. *Id.* at [0130].

Thus, contrary to the statements in the petition, a person of ordinary skill in the art would have recognized that Conroy’s method of power budgeting does not rely on subsystems making “requests” for power. Ex. 2002 at ¶¶ 57-58. Consequently, the premise that a person of ordinary skill in the art would look to teachings of Bose to understand how to address such requests, Pet. at 67, is false. *Id.*

Moreover, a person of ordinary skill in the art would not combine the teachings of Conroy and Bose at all and the petition fails to demonstrate why it would be otherwise. The entire alleged motivation is a single sentence asserting that, “A POSITA would have been motivated to implement Conroy’s power manager with Bose’s teaching to not grant a subsystem’s request to increase the system’s setting immediately and, instead, wait till the next iteration to do so in order to keep the power supplied to the various subsystems stable within each integration.” Pet. at 67. Neither the petition nor Dr. Horst provide any explanation or justification for this assertion. Nor does the petition explain how any of the other teachings of the references affect the analysis. For example, no explanation is provided as to why a person of ordinary skill in the art would have combined the power allocation

tables of Conroy with a token-based allocation approach as described by Bose. *See* Ex. 1008 at [0013]. Petitioner does not allege that Bose provides a solution to a problem identified in Conroy. Nor does the proposed combination represent a substitution of any known elements from Conroy for an element in Bose. Nor is the proposed combination an example of use of a technique disclosed in Bose to improve Conroy. Nor does Petitioner identify any market or other factors creating incentive for a variation of Conroy.

In fact, Conroy conflicts with Bose. For example, whereas Conroy describes a system enacting a burst of high power following a period of low power, Bose describes the opposite—following low power usage, token count is decremented. Ex. 2002 at ¶ 68 (comparing Ex. 1006 at [0135] with Ex. 1008 at [0014]). And, in Conroy, it is overall system performance that determines whether or not a change in a change in operating parameters as specified in a power distribution table are employed, *id.* (citing Conroy at [0204]), while in Bose it is component-level power considerations that determine token allocation. *Id.* (citing Ex. 1008 at [0013]-[0014]). The petition provides no justification for modifying Conroy’s system-level approach according to Bose’s localized one.

Consequently, for at least the above reasons, claim 16 has not been shown to be unpatentable in view of Conroy and Bose.

F. Nussbaum Fails to Teach or Suggest the Invention Recited in Challenged Independent Claim 13

MB USA's challenge to claim 13 based on the teachings of Nussbaum fails to demonstrate that the claim is unpatentable.

1. Overview of Nussbaum

Nussbaum describes an “analysis of workload executed on computational units to help identify those computational units that are more performance sensitive to a change in performance capability caused by, e.g., a frequency change.” Ex. 1007 at [0005]. Nussbaum explains that “[s]electively distributing power among the active cores or other computational units based on [such] frequency sensitivity allows for greater overall system throughput on heterogeneous workloads or multi-threaded workloads with heterogeneous threads.” *Id.* at [0019]. Nussbaum is therefore directed to determining the frequency sensitivity of computational units to make use of sensitivity-based power allocation. As Nussbaum states, “[t]he rationale for that is to not waste power by boosting cores whose performance will not be increased.” *Id.* at [0040].

Nussbaum describes its approach to calculating the performance sensitivity:

[T]he computational units are operated at a first performance level, and respective first utilization metrics are determined. The computational units are then operated at a second performance level and respective second utilization metrics are determined. The sensitivity to performance capability change, e.g., a frequency change, is determined.

Ex. 1007, Abstract; [0006]. As mentioned, power distribution is then based on these measured frequency sensitivities. *Id.* at [0019].

Nussbaum distinguishes this approach from changing power consumption of CPU cores collectively. For example, Nussbaum identifies approaches that “opportunistically raise the performance level (e.g., raise the frequency) of CPU cores on multi-core processors, when the processor integrated circuit is running below its thermal design point (TDP):”

Such approaches allow the operating frequency of the CPU cores to be raised together when there is estimated power, current or thermal headroom in order to improve performance under a given TDP, and decreased when the operation is exceeding those limits. Such approaches have assumed all active CPU cores operate in their

maximum performance state when their frequency is raised in a coordinated fashion.

Ex. 1007, [0017]. Nussbaum then distinguishes those approaches from its own, explaining that its approach not only differs, but “allows for greater overall system throughput:”

The above approaches for homogenously increasing power to all cores or to one or more cores based on performance states of the cores, allow for power to be reallocated from idle computational units, such as the CPU or graphical processing unit (GPU), but treat all active units homogeneously when dithering frequency or boosting steady state frequency. However, some active cores or other computational units may be gaining little or no performance increase from a higher core frequency, while other cores or computational units may be running workloads with a higher sensitivity to an increase in core frequency. Selectively distributing power among the active cores or other computational units based on frequency sensitivity allows for greater overall system throughput on heterogeneous workloads or multi-threaded workloads with heterogeneous threads. That requires an effective approach to identify workload sensitivity to changes in core frequency.

Ex. 1007, [0019]. Nussbaum is therefore directed to a different approach than those that allocate power collectively for example.

2. Nussbaum does not teach or suggest dynamic allocation of a power budget between domains of a multicore processor according to power sharing values of those domains stored in different storages, as recited in claim 13

As discussed above, claim 13 recites power sharing logic to dynamically allocate a variable power budget between different domains based on each domain's respective power sharing value. Nussbaum fails to teach or suggest such a feature.

The petition alleges it is the power allocation controller 109 and performance analysis control logic 111 (the components highlighted in

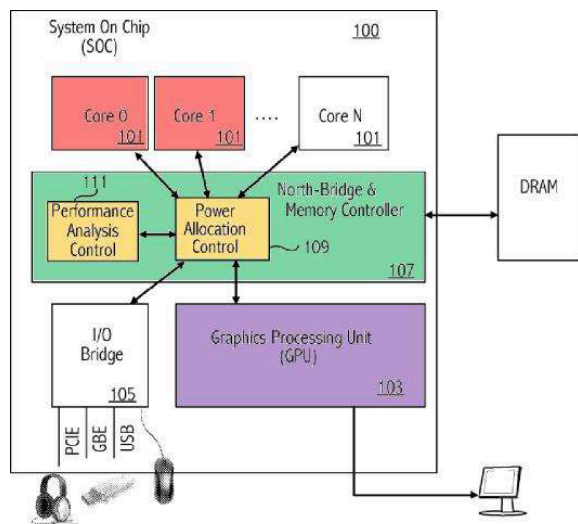


FIG. 1

yellow in the excepted Fig. 1) that jointly control allocation of Thermal Design Point (TDP) power headroom in Nussbaum. Pet. at 42. According to the petition, this power headroom is selectively distributed among different computational units

based on those computational units' sensitivities to frequency changes (so-

called “boost sensitivities”). *Id.* The boost sensitivities are also alleged to govern how power is allocated between computational units. *Id.* The petition further alleges that the frequency sensitivities are power sharing values of domains, as recited in claim 13. *Id.* at 44. This is incorrect. Ex. 2002 at ¶¶ 62-64.

In Nussbaum, frequency sensitivities are not per-domain attributes. Instead, they are per-component, e.g., per-core, attributes. *Id.* at ¶ 63. Nussbaum explains,

In order to evaluate which of the cores can better exploit an increase in performance capability, in one embodiment, ***performance sensitivity of each computational unit to frequency change***, and/or other change in performance capability, also referred to herein as boost sensitivity, ***is determined and stored on a computational unit basis.***

Ex. 1007 at [0025] (emphasis added).

In claim 13, the recited power sharing values are attributes of the respective domains. Ex. 2002 at ¶ 64. And, the recited first domain includes multiple cores. *Id.*; Ex. 1001 at 12:53-54. If Nussbaum is read in such a way so as to have a domain with multiple cores, as the petition desires, Pet. at 35-38, then it necessarily follows that each one of those cores in such a domain will have its own frequency sensitivity and any distribution of power

headroom among those cores will be based on those cores' individual sensitivities to frequency changes. Ex. 2002 at ¶¶ 63-64. This is in contrast to claim 13's requirement that a variable power budget is dynamically allocated based on respective *domains*' power sharing values. *Id.*

This result should not be surprising. Nussbaum actually criticizes domain-based power allocations: “treat[ing] all active units homogeneously when dithering frequency or boosting steady state frequency” is undesirable because “some active cores or other computational units may be gaining little or no performance increase.” Ex. 1007 at [0019]. Nussbaum further discourages using a collective boost sensitivity for multiple cores (i.e., a domain), and instead not only prefers, but even teaches how to calculate per-core boost sensitivities. *Id.* at [0025]-[0031]. Accordingly, a person of ordinary skill in the art reading Nussbaum would appreciate that it does not suggest the use of per-domain power sharing values as in claim 13. Ex. 2002 at ¶ 64.

It is also worth noting that, whereas the petition maps Nussbaum's “Thermal Design Point (TDP) power headroom” to the claimed “power budget,” Pet. at 41, Dr. Horst actually testifies that, “Nussbaum does not subdivide this ‘power headroom.’” Ex. 1029 at ¶ 150. Therefore, the

claimed power budget is not allocated *between* domains at all, as required by claim 13, let alone according to first and second sharing policy values.

Thus, the petition fails to demonstrate that Nussbaum teaches or suggests a power sharing logic to dynamically allocate a variable power budget between the first and second domains based at least in part on a first power sharing value for the first domain stored in a first storage and a second power sharing value for the second domain stored in a second storage, as recited in claim 13. *CFMT, Inc.*, 349 F.3d at 1342.

G. Claims Depending from Claim 13 are Not Obvious in View of Nussbaum

Challenged claims 14, 15, 17, and 18 depend, or indirectly, from claim 13. Each respective dependent claim is not unpatentable in view of Nussbaum for at least the same reasons as independent claim 13. *Hartness Int’l. Inc.*, 819 F.2d 1100.

Furthermore, each of claims 14 and 15 require allocation of a variable power budget to a domain. Ex. 1001 at 12:65 – 13:10. As noted above, the petition maps Nussbaum’s “Thermal Design Point (TDP) power headroom” to the claimed “variable power budget.” Pet. at 41. However, Nussbaum does not allocate power on a per-domain basis and, instead, does so on a per-computational unit basis. Ex. 2002 at ¶ 63. Accordingly, Nussbaum does not

teach or suggest the allocation of a variable power budget recited in either of claims 14 or 15 and, therefore, these claims are not unpatentable in view of Nussbaum. *Id.*

1. Nussbaum does not teach or suggest allocation of a variable power budget according to domain-specific minimum reservation values, as recited in claim 17

Claim 17 depends from claim 14 and recites, “wherein the power sharing logic is to further allocate the first portion of the variable power budget according to a first minimum reservation value for the first domain and allocate the second portion of the variable power budget according to a second minimum reservation value for the second domain.” Ex. 1001 at 13:17-22. The petition alleges that the recited “minimum reservation values” are met by Nussbaum disclosure of a “core power state,” referred to as “Deep Cstate,” in which a core is allocated “Core_DeepCState_Pwr.” Pet. at 49. This allegation is false.

Nussbaum’s Deep Cstate is characterized by “Clocks Off/Power Off.” At deposition, Dr. Horst confirmed this represented a state where the associated processor was off. Ex. 2001 at 43:7 – 44:2; *and see* Ex. 1007 at [0033] Table 3 (reproduced below).

TABLE 3			
Core Performance States	Operational point (F, V)	Power (dynamic and static) consumed in this point	Remarks
P-boost	F-boost/V-boost	CoreBoostPwr	Boost point. Power budget of the Core has been exceeded
P0	F0/V0	Core_Pwr0	Core Power Budget
P1	F1/V1	Core_Pwr1	
P2	F2/V2	Core_Pwr2	
P3	F3/V3	Core_Pwr3	
Idle	Clocks Off/Low voltage	Core_Idle_Pwr	
Deep Cstate	Clocks Off/Power Off	Core_DeepCstate_Pwr	Core is either power gated or deep voltage is applied

A state in which a processor is off does not correspond to a state where the processor has been allocated a minimum reservation value of power, which the specification of the '833 patent explains is a reserved amount of power to be allocated a domain. Ex. 2002 at ¶ 66 (citing Ex. 1001 at 5:49-64). It is instead a state when one can expect no power to be allocated. “Allocating power to a component that is off is pointless, because that power will not be used.” *Id.*

Still referring to Nussbaum’s Table 3, the petition makes the additional allegation that, “a POSITA would have understood that the operational point corresponding to the lowest performance state “P3” represents a minimum reservation value for the first domain when the cores are utilized to perform their operations.” Pet. at 49. And, now referring to

Nussbaum's Table 4, the petition remarks, "a POSITA would have understood that the operational point corresponding to 'GPU_P3' represents a second minimum reservation value for the second domain because it corresponds to the lower performance state the GPU in the second domain may be utilized to perform its operations." *Id.* at 49-50. But, this attempt at conjuring minimum reservation values in Nussbaum also fail.

As previously noted and as confirmed by Nussbaum's Tables 3 and 4, to the extent power is allocated to cores or GPUs in accordance with performance states, those allocations are made on a per-computational unit basis. Ex. 2002 at ¶ 67. These are not domain-based allocations as specified in claim 17. *Id.* That is, the performance states do not correspond to domains, but rather to individual computational units and inasmuch as claim 17 still requires claim 13's requirement of a domain including multiple cores, there is no teaching or suggestion in Nussbaum that power would be allocated to a domain according to the performance state needs of an individual computational unit. *Id.*

Thus, the petition has failed to demonstrate that claim 17 is obvious in view of Nussbaum. *CFMT, Inc.*, 349 F.3d at 1342.

2. Nussbaum does not teach or suggest allocation of a variable power budget according to preference values, as recited in claim 18

Claim 18 depends from claim 14 and recites, “wherein the power sharing logic is to further allocate the variable power budget according to a preference value, the preference value to favor the second domain over the first domain.” Ex. 1001 at 13:23-26. Referring to Nussbaum’s Fig. 6, the petition alleges, “if the output value of step 601 identifies an application as GPU-bounded, then CPU cores may be throttled to release power margin available to the GPU.” Pet. at 50 (citations omitted). The assertion is that, “a POSITA would have understood that an output value of step 601 being an identification of a ‘GPU-bounded’ application is a preference value to favor the second domain (which includes the GPU) over the first domain (which includes the cores).” *Id.* at 50-51.

This attempt to map the teachings of Nussbaum to the requirements of claim 18 fails. The “output value” of step 601 is not used to “allocate the variable power budget,” but rather to adjust the amount of power budget that is available. Ex. 2002 at ¶¶ 69-70. For example, as Petitioner admits, the output value is used to throttle CPU cores and create more power budget, but no power budget is allocated using the output of step 601. The output of step

601 is simply an identification. Ex. 1007 at [0047]. Hence, claim 18 is not obvious in view of Nussbaum.

3. Claim 16 has not been shown to be obvious in view of Nussbaum-Bose

Claim 16 depends from claim 14 and recites, “wherein the power sharing logic is to increment the first power sharing value when a request for a higher frequency for the first domain is not granted, and to increment the second power sharing value when a request for a higher frequency for the second domain is not granted.” Ex. 1001 at 13:11-16. Insofar as claim 16 depends, indirectly, from claim 13, and the petition relies on Nussbaum for teaching or suggesting the limitations of claim 13, then claim 16 is not obvious in view of Nussbaum-Bose for at least the reasons set forth with respect to claim 13. *Hartness Int’l. Inc.*, 819 F.2d 1100.

Furthermore, claim 16 is separately patentable because a person of ordinary skill in the art would not combine the teachings of Conroy and Bose as alleged in the petition. Ex. 2002 at ¶ 72. The petition alleges,

A POSITA would have been motivated to implement Nussbaum’s power allocation operations with Bose’s teaching to increment a boost sensitivity of a particular domain ... when a request for a higher frequency for that particular domain is not granted, especially if that

particular domain is operating below an expected performance level, so as to avoid continued denial of that particular domain's request for a higher frequency and to avoid starvation of that domain.

Pet. at 54. However, Petitioner does not identify any teaching or suggestion that would have provided that alleged motivation in the art, and merely relies on hindsight. Petitioner does not allege that Bose provides a solution to a problem identified in Nussbaum. Nor does the proposed combination represent a substitution of any known elements from Nussbaum for an element in Bose. Nor is the proposed combination an example of use of a technique disclosed in Bose to improve Nussbaum. Nor does Petitioner identify any market or other factors creating incentive for a variation of Nussbaum.

Nussbaum and Bose would not have been combined at least because they relate to different and generally incompatible approaches to power control. For example, Nussbaum is rooted in physical solutions and uses "boost sensitivities" that depend on physical characteristics of computational units, whereas Bose is rooted in software solutions and uses arbitrary "tokens" of power allocation. *See* Ex. 2002 at ¶ 72 (citing Ex. 1007 at [0029]-[0030]; Ex. 1008 at [0044]-[0046]). The references do not discuss how a person of ordinary skill in the art would adopt a token-approach, as in

Bose, in a system that relies on empirical measurements, as in Nussbaum.
Nor would it be apparent to a person of ordinary skill in the art how to do so.
Id.

Moreover, even if the teachings of Nussbaum were considered in combination with Bose, one would not arrive at the invention recited in claim 16. For example, such a combination does not teach or suggest “increment[ing] the first power sharing value” ever, let alone “when a request for a higher frequency for the first domain is not granted.” *Id.* at ¶ 73. The petition maps Nussbaum’s “boost values” to the claimed first and second power sharing values, but as Nussbaum explains, the “boost values” are physical characteristics that are calculated based on the performance level and utilization metrics. *Id.* (citing Ex. 1007 at [0006]). Although Nussbaum describes re-evaluating the boost sensitives, it does not describe intentionally “increment[ing]” them (i.e., raising the value) as in the ’833 patent. *Id.* And, “Bose explains that if no additional tokens can be allocated to the particular resource at the moment (i.e., a request for a higher frequency is not granted), that particular resource can wait for its token count to be increased in the next iteration of the process.” Pet. at 53 (citing Bose at ¶ 86). Thus, Bose teaches when a request for a higher token count is not granted, the component must “wait,” and cannot increase its token count.

Ex. 2022 at ¶ 73. Hence, a combination of Nussbaum and Bose does not lead to the invention recited in claim 15. *Id.*

Consequently, for at least the above reasons, claim 16 has not been shown to be unpatentable in view of Nussbaum and Bose.

H. Claims 1-5, 7, 13-15, 17, and 18 are Not Obvious in View of Conroy and Finkelstein

The petition asserts that claims 1-5, 7, 13-15, and 17-18 obvious in view of Conroy when considered in combination with Finkelstein. Pet. at 68 *et seq.*

1. A person of ordinary skill in the art would not combine the teachings of Conroy and Finkelstein and, even if they did, it would not yield the claimed invention

The petition fails to demonstrate that a person of ordinary skill in the art would have been motivated to combine the teachings of Conroy and Finkelstein, at least because they operate at different levels within a system. Ex. 2022 at ¶ 74. Finkelstein is directed at solutions for a processor, that is, it is describing a chip-level solution; Conroy, on the other hand, is describing solutions for implementation at a system level. *Id.* While the petition alleges, “a POSITA would have been motivated to implement

Conroy’s system on a chip, as in Finkelstein,” Pet. at 69, the only justification⁵ provided for this contention is that integrated circuits can accommodate “additional functionality.” *Id.* This is inadequate, particularly, explains Dr. Brogioli, given Conroy’s statement that it “is not intended to represent any particular architecture or manner of interconnecting the components as such details are not germane to the present invention.” Ex. 2022 at ¶ 74 (citing Ex. 1006 at [0186]).

Perhaps even more important, modifying Conroy in view of Finkelstein would not result in the claimed invention. *Id.* at ¶ 75. For example, “modifying Conroy with Finkelstein would merely add another (Finkelstein-like) component within Conroy’s system, but would not change the overall power management characteristics of Conroy.” *Id.* Conroy is agnostic when it comes to the manner in which power is allocated at the level of individual components/subsystems. *Id.* A person of ordinary skill in the art would therefore appreciate that there is no need to modify the power allocation approach of Conroy if and when components were added. *Id.*

⁵ The petition also cites Dr. Horst’s declaration, but the declaration merely repeats the allegations in the petition verbatim, without further explanation. *See* Ex. 1029 at ¶ 212.

Instead the person of ordinary skill in the art would appreciate that Conroy's approach of power management, in which "power is redistributed between the sub-systems while tracking [a] load profile," Ex. 1006 at [0006], would be perfectly acceptable. *Id.* Indeed, one of the benefits of Conroy's approach is its "modular" nature in which changes in power distribution can be made only when changes in a system's load profile (e.g., as occasioned by the addition of components) changes sufficiently to warrant such a change. *Id.* (citing Ex. 1006 at [0204]).

Accordingly, the petition fails to sufficiently explain why a person of ordinary skill in the art would even make the proposed combination of teachings and why, even if they did, it would lead to the claimed invention. Hence, the challenged claims are not obvious in view of Conroy-Finkelstein.

2. Claim 1 is not obvious in view of Conroy-Finkelstein

The proposed combination of Conroy-Finkelstein does not teach or suggest "each of the first and second domains to operate at an independent voltage and frequency," as recited in claim 1. *Id.* at ¶ 76. The petition alleges that in Conroy "subsystem A" and "subsystem B" serve as the claimed first and second domains, Pet. at 71, but even if that is so, there is no suggestion in Conroy that these subsystems operate at independent voltage and

frequency. Despite Conroy's statement that "components have independent throttle settings," Ex. 1006 at [0120], those throttle settings are merely variable, not separately controlled. As Dr. Brogioli notes, Conroy discloses throttle settings as being intertwined, not independent." *Id.* (citing Ex. 1006 at [0203]). Hence, the petition fails to demonstrate that claim 1 is objection in view of these references.

3. Claims 2-5 and 7 are not obvious in view of Conroy-Finkelstein

Claims 2-5 and 7 depend from claim 1 and are therefore patentable over Conroy-Finkelstein for at least the same reasons as claim 1.

Moreover, with respect to claims 2, 4, and 7, Petitioner does not allege that these claims obvious for any specific reasons not already addressed with respect to Conroy. Pet. at 79. Hence, for the reasons given above with respect to claim 1 and those with respect to Conroy, the petition fails to demonstrate any of claims 2, 4, or 7 are obvious in view of Conroy-Finkelstein.

4. Claims 13-15, 17, and 18 are not obvious in view of Conroy-Finkelstein

Petitioner does not allege that any of these claims is rendered obvious for any specific reasons. Instead, Petitioner merely refers back to discussion of these claims in connection with challenges based on Conroy alone.

Hence, for the reasons given above with respect to claims 13-15, 17, and 18 with respect to Conroy, the petition fails to demonstrate any of these claims are obvious in view of Conroy-Finkelstein.

IV. CONCLUSION

For at least the foregoing reasons, the Board should find that Petition has failed to prove the unpatentability of any of the challenged claims.

Harmonic Inc. v. Avid Tech., Inc., 815 F.3d 1356, 1363 (Fed. Cir. 2016) (“In an [inter partes review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.”) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (the burden of persuasion never shifts to the Patent Owner); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (a petitioner cannot satisfy its burden of proving

obviousness by employing “mere conclusory statements”).

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WORD-COUNT CERTIFICATE

I certify that the foregoing document complies with the type-volume limitation of 37 C.F.R. § 42.24(a) and (b) and contains 12,175 words (including words in drawings created by the Patent Owner or as annotations added by the Patent Owner to images reproduced in this document) based on the word count indicated by Microsoft® Word for Mac v. 16.84, excluding those portions exempted by the rule.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing:

PATENT OWNER'S RESPONSE

and its accompanying exhibits were served on May 24, 2024, by filing this document through the P-TACTS System as well as by delivering a copy via email directed to the attorneys of record for the Petitioner at the following addresses:

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