

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Mercedes-Benz USA, LLC,
Petitioner,

v.

Daedalus Prime LLC,
Patent Owner.

Case No. IPR2023-01335
U.S. Patent No. 8,775,833

**PETITIONER'S REPLY TO
PATENT OWNER'S RESPONSE**

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LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 8,775,833 (“the ’833 Patent”)
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Ex-1004	Prosecution History of the ’833 Patent
Ex-1005	U.S. Published Patent Application No. 2010/0115304 (“Finkelstein”)
Ex-1006	U.S. Published Patent Application No. 2007/0049133 (“Conroy”)
Ex-1007	U.S. Published Patent Application No. 2011/0022356 (“Nussbaum”)
Ex-1008	U.S. Published Patent Application No. 2009/0089602 (“Bose”)
Ex-1009	INTENTIONALLY LEFT BLANK
Ex-1010	INTENTIONALLY LEFT BLANK
Ex-1011	INTENTIONALLY LEFT BLANK
Ex-1012	INTENTIONALLY LEFT BLANK
Ex-1013	INTENTIONALLY LEFT BLANK
Ex-1014	INTENTIONALLY LEFT BLANK
Ex-1015	INTENTIONALLY LEFT BLANK
Ex-1016	INTENTIONALLY LEFT BLANK
Ex-1017	INTENTIONALLY LEFT BLANK

¹ Four-digit pin citations that begin with 0 are to the branded numbers added by Mercedes in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

Ex-1018	INTENTIONALLY LEFT BLANK
Ex-1019	INTENTIONALLY LEFT BLANK
Ex-1020	Claim Mapping Table
Ex-1021	INTENTIONALLY LEFT BLANK
Ex-1022	INTENTIONALLY LEFT BLANK
Ex-1023	U.S. Patent No. 7,263,457 (“White”)
Ex-1024	U.S. Patent No. 8,438,416 (“Koccev”)
Ex-1025	U.S. Patent No. 8,984,523 (“Vajda”)
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Ex-1027	Selected pages of Stefanos Kaxiras et al., <i>Computer Architecture Techniques for Power-Efficiency</i> (2008)
Ex-1028	U.S. Published Patent Application No. 2010/0162006 (“Therien”)
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I. Introduction

The arguments in Patent Owner’s Response (“POR”) reach their conclusions through misinterpretations of disclosures of the prior art references Petitioner presents. When Patent Owner’s isolated quotes are reunited with their contexts, it is clear that Finkelstein, Nussbaum, Conroy, and Bose disclose every element of the asserted claims.

First, Patent Owner dismisses Finkelstein’s clear disclosure of each element of claim 1 based on its alleged failure to dynamically allocate power budget “for a processor.” As the Board’s Institution Decision held and the Petition shows, Finkelstein is replete with disclosures of processor-wide dynamic budget allocation. Next, Patent Owner attacks Conroy, arguing its “power sharing values” are stored in “a memory” instead of in first and second storages as claim 13 requires, ignoring the implication from Conroy that multiple values in its memory are in fact in a “first storage” and “second storage” within that “memory.” Third, Patent Owner argues “per computational unit” power sharing values are not used for “domains,” but rather for cores, and dismisses Nussbaum’s disclosure on this basis. However, as the Board’s Institution Decision in related case IPR 2023-00550 held and Patent Owner’s expert admits, a “computational unit” can include more than one core and can be equivalent to a “domain.” Finally, Patent Owner argues that Conroy and Finkelstein do not render the claims obvious because Conroy’s “*independent* throttle

settings” are not “independent” by Patent Owner’s reinterpretation of that claim term. Not so. Conroy’s disclosures meet the plain meaning of “independent,” as described in the Petition, and as agreed to by Patent Owner’s expert.

Patent Owner presents arguments against the motivations to combine Finkelstein, Conroy, Nussbaum, and Bose, but none are convincing in light of the motivations to combine shown in the Petition and those apparent to persons of ordinary skill in the art.

II. Claim Construction and Level of Ordinary Skill in the Art

Patent Owner emphasizes that the Petition’s definition of a POSITA improperly encompasses people with *more* than ordinary skill in the art. POR, 11. This distinction is irrelevant. One with greater than “ordinary” skill necessarily meets the definition of a POSITA; the POSITA definition is a floor, not a ceiling.

Patent Owner alleges that Dr. Horst defined “independent” as “different.” POR, 16. This is a misquote. Dr. Horst explained that in the context of the claims, “independent” means “each domain *could have* a different voltage and frequency than the other domain.” Deposition Transcript of Dr. Robert Horst, Ex. 2001, at 17:4-7 (“Horst Dep.”) (emphasis added). At deposition, Patent Owner’s expert conceded that this definition is correct. Deposition Transcript of Dr. Michael Brogioli (“Brogioli Dep.”), 28:7-10 (“Q. So each domain could have a different voltage than frequency than the other domain, not necessarily saying that it would, but it could;

true? A. I think that sounds right.”). Patent Owner’s Response proposes a different definition of “independent” – “separately controlled” – a phrase which appears nowhere in the patent’s text. POR, 15-17. The definition includes a self-contradictory assertion that “independent” can in fact mean “dependent.” *Id.* Petitioner maintains that Dr. Horst’s definition, to which Dr. Brogioli agrees, represents the plain and ordinary meaning of the term “independent.” Petition, 10; Ex. 2001 at 16:15-17:7.

III. Finkelstein Discloses Dynamically Allocating Power Budget for a Processor

A. Independent Claim 1

Arguing that Finkelstein fails to dynamically allocate power budget *for a processor*, Patent Owner takes one sentence of Finkelstein out of context to the exclusion of the rest of the disclosure. POR, 1, 25-27. Specifically, Patent Owner argues that when Finkelstein allocates the unused power budget for domain i (

$W_{ki}E^k - E_{high}^i$), it is not allocating “the power budget of the entire processor.”

POR, 1, 25-27. Even if the distribution of $W_{ki}E^k - E_{high}^i$ is not processor-wide budget allocation, Patent Owner’s argument ignores both the Petition’s arguments and Finkelstein’s remaining disclosures. Finkelstein, [0035].

As the Board correctly pointed out in its Institution Decision, Finkelstein is replete with references to dynamically allocating a power budget *for a processor*.

Institution Decision (“DI”), 14-15; Petition, 23-25. Finkelstein as a whole is concerned with dynamically allocating power for “*processors* having multiple power planes” which share “the same power source 120” and “a common *package* power/energy budget.” Finkelstein, [0026] (emphasis added); Petition, 24; Brogioli Dep., 37:16-25; 42:23-45:12. At deposition, Patent Owner’s expert confirmed that this “package” is “the cores and other things that may be with them on the chip,” or, in other words, the entire processor. Brogioli Dep., 38:1-5.

In one example, Finkelstein dynamically allocates the package power budget so that “unused processor core power” from a first domain can be used “for more Graphics Effect(s) (GF) performance” in a second domain. Finkelstein, [0026]; Declaration of Dr. Robert Horst (“Horst Decl.”), EX. 1029, ¶84. As another example, Finkelstein dynamically allocates the processor’s total power budget E^k among domains i based on domain weights W_{ki} . POR, 23-24; Finkelstein, [0034]; Horst Decl., ¶88. The assertion that Finkelstein does not disclose allocating power budget for a processor is, therefore, incorrect.

B. Claims depending from Claim 1

Because Patent Owner presents no separate arguments for the patentability of claims 2-5 and 7, these claims rise and fall with Patent Owner’s argument regarding claim 1. POR, 27; Petition, 27-34. Patent Owner likewise presents no separate

arguments for the patentability of claim 7 over Finkelstein and Conroy. POR, 27-28; Petition, 34-36.

IV. Conroy Discloses Power Sharing Values in Different Storages

A. Independent Claim 13

Regarding claim 13, Patent Owner argues that Conroy's storage of "power sharing value[s]" in "*a memory of the system*" means Conroy cannot store values for respective domains in "a first storage" and "a second storage," or *different storages*. POR p. 1-2, 33-35. Patent Owner fails to explain why the two are inconsistent. In fact, both Conroy and the '833 Patent store "power sharing values" in separate registers ("storages") within a larger "memory." Conroy, Figs. 21-22; '833 Patent, 4:5-10, Table 1, 8:59-62; Petition, 60-61.

As Patent Owner's expert explains, as a "memory" decreases in size, "[a]t some point, ...it starts to become what we call 'registers' that still store bits of information." Brogioli Dep., 12:17-24. In other words, "a memory" is a larger space which contains separate "registers." The '833 Patent stores "power sharing value[s]" for domains in separate "register[s]," which it also refers to as "storages," within a single larger memory, "*a power control storage 357*." '833 Patent, 4:5-10, Table 1, 8:59-62 (referencing the values in the two columns as stored in "registers").

TABLE 1	
[31.5]	[4.0]
Primary Plane Turbo Power Policy	
Reserved	POLICY_FIRST
Secondary Plane Turbo Power Policy	
Reserved	POLICY_SECOND

Conroy does the same. As the Petition notes, Conroy uses a single memory to store a table of power sharing values, and Conroy’s individual “power sharing value[s]” would be contained in separate registers. Conroy, Figs. 21-22; Petition, 60-61.

In response to Petitioner’s argument that Conroy’s storage of “throttle settings” in “registers” teaches storage of “power sharing value[s]” in “registers,” Patent Owner asserts that Conroy’s “throttle settings” are the “actual powers consumed by each subsystem.” POR, 35-36; Petition, 60-61. This is a misunderstanding of Conroy. In Conroy, “actual powers consumed” are merely *used* “to *determine* the dynamic throttle setting.” Conroy, [0095]. “[A]ctual power[] consumed” cannot be the “throttle setting” itself because a “throttle setting” in Conroy is a voltage and/or frequency setting. Conroy, [0050], [0064-65], [0081]; POR, 59-60; Brogioli Dep., 47:24-48:14 (conceding that in paragraph 81 of Conroy, “throttle setting” refers to a voltage and frequency pair). Conroy stores its voltage and/or frequency settings, also referred to as “throttle settings,” in registers and therefore its “power sharing values” are stored in registers. Petition, 60-61.

B. Claims depending from claim 13

Claim 14 requires “the power sharing logic to determine the variable power budget *for a current time interval* and to allocate a first portion of the variable power budget ...and to allocate a second portion of the variable power budget...” Patent Owner argues that Conroy’s iterative determination of power budgets for a series of time intervals somehow skips over the power budget “for a current time interval.” POR, 37-39.

As Patent Owner’s expert admits, Conroy discloses an iterative process which determines power budgets for a sequence of time intervals, “ $T-(n-1)\Delta$, $T-(n-2)\Delta$, ..., T ” and “ $T+\Delta$.” Brogioli Dep., 58:8-61:10; Conroy, [0069-71]. Conroy describes each time interval as either “past” or “next” – “next” meaning that which comes after the past, *i.e.* the present. *Id.* Conroy’s choice of phrasing does not mean that *no* interval in Conroy corresponds to the “current time interval” in claim 14. Either, as Patent Owner argues, “ T ” is the “current” time interval, or else “ $T+\Delta$ ” corresponds to the “current” time interval. POR, 37-39; Petition, 63. Conroy’s iterative process determines and allocates power budgets for both, and it thereby discloses determining a power budget for a “current time interval.”

C. Dependent Claim 16: A POSITA Would be Motivated to Combine Conroy and Bose

Claim 16 refers to the “power sharing value[s]” of claim 14, and requires that “the power sharing logic is to increment” a respective “power sharing value” “when a request for a higher frequency” for the corresponding domain “is not granted.”

Patent Owner implicitly concedes that Conroy and Bose disclose each element of claim 16. Instead of drawing any distinction between the claim language and the references, Patent Owner instead argues a lack of motivation to combine Conroy with Bose. These arguments fail.

First, Patent Owner argues that Conroy is incompatible with methods which allocate power in response to “‘requests’ for power.” POR, 41. But Patent Owner ignores that Conroy itself discloses such methods: in embodiments, “the power management system *requests throttle setting changes* when necessary.” Conroy, [0131]. As shown in Figs. 21-22, a throttle setting change in Conroy corresponds to a change in “allocated power.” Conroy, Figs. 21-22, [0203], [0050], [0094-97].

Second, Patent Owner argues that the Petition’s explanation of the motivation to combine Conroy with Bose is insufficient. The Petition includes specific and sufficient reasons why a POSITA would combine Conroy with Bose. As the Petition explains, adding Bose’s token incrementing scheme to Conroy’s power manager would “keep the power supplied to the various subsystems stable within each integration.” Petition, 67. Dr. Horst notes that Conroy’s paragraph 130 maintains a selected throttle setting until the “next iteration” of dynamic throttling, just as Bose maintains a token count until the “next iteration” of its process. Horst Decl., ¶206; Conroy, [0130]; Bose, [0086].

Third, Patent Owner insists that Conroy “conflicts with” Bose because each responds to a decrease in workload in an opposite way. Despite Patent Owner’s selective citations, both Conroy and Bose increase power when workload increases and decrease power when workload decreases. Conroy, e.g., [0196-97]; Bose, e.g., [0014].

Last, Patent Owner argues that Conroy is inconsistent with Bose because Conroy does not allocate power based on “component-level considerations.” POR, 42. But, Patent Owner ignores Conroy’s disclosures, which note that “*components* have independent throttle settings” and that some “*components* may be busy so that [sic] require higher priority.” Conroy, [0120-22], *see also* Horst Decl. ¶ 219-220. Furthermore, Bose discloses component-level considerations as well, noting that “[e]ach managed component, in response to its own operating conditions (as evidenced by its utilization markers) can either attempt to donate one or more token(s)” or “read (receive) one or more token(s).” Horst Decl. ¶ 64 (citing Bose ¶¶ 38-39, 68). Therefore, Patent Owner’s component-level argument is of no moment in view of the disclosures of both Conroy and Bose.

V. Nussbaum Discloses Power Sharing Values for Respective Domains

A. Independent Claim 13

Patent Owner argues that Nussbaum’s boost sensitivities cannot be “power sharing values” for “domains,” because boost sensitivities are per “computational

unit.” POR, 2, 47-49. This argument relies on the assumption that the term “computational unit” in Nussbaum can only refer to a “core.” That assumption is incorrect.

The Board’s Institution Decision in related IPR 2023-00550 held that “each computational unit of Nussbaum may include a plurality of cores.” Institution Decision, IPR 2023-00550, 31-32. At deposition, Patent Owner’s expert confirmed this. Brogioli Dep., 50:20-51:19, 65:9-19. Nussbaum refers to “computational units, *such as the CPU* or graphical processing unit (GPU),” and states that the CPU “includes multiple [] processing cores.” Nussbaum, [0019-20]; Brogioli Dep., 50:20-51:19 (conceding that a “computational unit” is referring to a CPU or a GPU). Furthermore, Nussbaum repeatedly refers to “cores *or other computational units*,” phrasing that would be superfluous if a computational unit were merely a core. *Id. passim*. Therefore, Nussbaum contemplates that a “computational unit” can include more than one core, and boost sensitivities associated with a “computational unit” may be associated with more than one core.² Brogioli Dep., 51:23-52:19 (explaining

² Even if a “computational unit” is a “core” as Patent Owner suggests, a POSITA would nonetheless find it obvious to apply Nussbaum’s “boost sensitivities” to domains instead of to cores. (Horst Decl. ¶160.)

that frequency sensitivity in Nussbaum is applied to a computational unit, which is a “unit that performs computation, [the] CPU or...GPU”).

Next, Patent Owner uses a single, out-of-context quote to argue that Nussbaum does not allocate its TDP “power headroom” “between” domains. POR, 48-49. Quoting Dr. Horst’s statement that Nussbaum “does not subdivide” power headroom in *certain scenarios*, Patent Owner asserts that Nussbaum, as a whole, *never* subdivides power headroom. Neither Dr. Horst’s declaration nor Nussbaum itself support Patent Owner’s assertion. See, e.g., Horst Decl. ¶¶135-36, 139-40; Nussbaum, [0020, 0024, 0036, 0039]; Petition, 42-43. As Dr. Horst explains, Nussbaum “distribut[es]” TDP “power headroom among the computational units” and “allocate[s] power between” them. Horst Decl., ¶136; Petition, 42-43.

B. Claims depending from claim 13

Claim 17 requires allocation of portions of the power budget to respective domains based on those domains’ associated “minimum reservation value[s].” Patent Owner asserts that neither Nussbaum’s “Deep CState” nor its “P3” state corresponds to the claimed “minimum reservation value.” POR, 51-52.

Patent Owner’s only argument regarding the “P3” state is that this state is “per-computational unit” and not per-domain. *Id.* As explained above, Nussbaum contemplates that a “computational unit” can include more than one core; in other words, a “computational unit” can be equivalent to a domain. See *supra* Sec. V.A.

In addition, Patent Owner argues that the “Deep CState” of Nussbaum is a “power off” state, and therefore cannot be a “minimum reservation value.” POR, 50-51. This argument assumes that a domain with “power off” can consume no power and will receive no power. *Id.* Yet Nussbaum discloses a “Core_DeepCstate_Pwr” value which represents the “*Power...consumed*” at the “Deep Cstate” power setting. Nussbaum, Table 3; *see also* Petition, 49-50. Nussbaum also shows that at the “Deep Cstate” setting, “deep voltage” is applied. Brogioli Dep., 64:1-19 (explaining that “deep voltage” is a low voltage applied to the core to maintain internal functions). Therefore, a “Deep Cstate” core can receive its “minimum reservation value” of power even in this state.³ Nussbaum, Table 3.

Claim 18 requires that the power budget be allocated according to a “preference value,” which is used “to favor the second domain over the first domain.” Patent Owner argues that Nussbaum’s CPU-bounded/GPU-bounded determination in “step 601” is not a “preference value” because “[n]o power is allocated using the output of step 601.” POR, 53. Nussbaum explicitly states otherwise: “In 601, CPU-bounded or GPU-bounded applications are identified...*the power headroom made available through throttling is provided* in 609 to the

³ The ‘833 Patent does not say the minimum reservation value must be a non-zero number or an amount above a specific threshold.

computational unit(s) executing the CPU-bounded and/or GPU-bounded application.” Nussbaum, [0047]; *see also* Petition, 50-51, citing Nussbaum [0044-48], Fig. 6; Brogioli Dep., 65:4-72:2. The determination of whether an application is CPU-bounded or GPU-bounded serves as a “preference value” because it is used to favor the CPU/GPU in Nussbaum’s allocation of power. Horst Decl., ¶157.

C. Claim 16: A POSITA Would be Motivated to Combine Nussbaum and Bose to Increment the Power Sharing Value

Claim 16 refers to the “power sharing value[s]” of claim 14, and requires that “the power sharing logic is to increment” a respective “power sharing value” “when a request for a higher frequency” for the corresponding domain “is not granted.”

Patent Owner first argues that there is no motivation to combine Nussbaum with Bose to teach the limitations of this claim. POR, 55. This is incorrect. Nussbaum’s preference for boosting “cores with the highest [boost] sensitivity” provides a motivation to increment those “boost sensitivities” by use of Bose’s methods. Petition, 51-52; Nussbaum, [0040]. To increase the likelihood that a core in need of a higher frequency will be “boosted,” a POSITA implementing Nussbaum would “re-evaluate[]” the “boost sensitivity” of the core using Bose’s token count increase methods. Bose, [0086]. And contrary to Patent Owner’s argument, the “tokens” of Bose are not “arbitrary” “software solutions.” POR, 55. Like the “boost sensitivities” of Nussbaum, Bose’s “tokens” are tied to the power utilization of

components. Bose, [0056, 0060, 0083]; Brogioli Dep., 54:4-55:3 (explaining that Bose’s “busy bit” indicates “whether a unit’s idle.”)

Patent Owner next argues that Nussbaum and Bose do not “increment” token count “ever,” because a component in Bose must “wait” when a request for increased power is not granted. POR, 56-57. But Bose does not respond to a request for increased power with a command for a component to “wait” indefinitely. When a component in Bose requests an increase in power, Bose responds by increasing the token count (“power sharing value”) of the component. Bose, [0086], Fig. 13; Petition, 52-54. Only when “no additional tokens can be allocated” does Bose ever ask a component to “wait,” and even then, only until “the next iteration of the process.” Bose, [0086]. As Bose’s Fig. 13 illustrates, step 1316 is a request for additional tokens that, if denied, triggers a loop leading back to step 1316. Bose, Fig. 13; Brogioli Dep., 74:16-75:8. Thus, the request will remain open until it is granted and the power sharing value can be increased, or until the resource is no longer “below expected performance level.” *Id.*

VI. CONROY AND FINKELSTEIN DISCLOSE DOMAINS WITH INDEPENDENT VOLTAGES AND FREQUENCIES

A. Independent Claim 1

Patent Owner argues first that there is no motivation to combine Conroy with Finkelstein, and attacks Conroy’s disclosure of domains with “independent” voltage and frequency. POR, 57-60.

Patent Owner argues that “the only justification” the Petition provides to implement Conroy’s system on a chip, as in Finkelstein, is “that integrated circuits can accommodate ‘additional functionality.’” POR 57-58. Patent Owner mischaracterizes the Petition. As the Petition explains, a POSITA would implement Conroy’s system on a chip to “reduce the size and weight of a system with a given set of functionality” and to improve “the reliability and power efficiency of the system.” Petition, 69.⁴ Patent Owner further argues that “‘modifying Conroy with Finkelstein would merely add another (Finkelstein-like) component within Conroy’s system.” POR, 58-59. That Conroy and Finkelstein overlap only creates a stronger motivation to combine the two, especially to enhance embodiments of Conroy that operate at the component level, such as where Conroy’s “components have independent throttle settings.” Conroy, [0120-22].

According to Patent Owner, Conroy’s “subsystem A” and “subsystem B” are not “domains” operating at “independent” voltages and frequencies because their voltages and frequencies are “intertwined.” POR, 59-60; Declaration of Dr. Michael

⁴ Patent Owner cites boilerplate language, that Conroy “is not intended to represent any particular architecture,” to argue against implementation on a chip. To the extent this phrase has meaning at all, it certainly does not exclude implementation on a chip. POR, 58.

Brogioli (“Brogioli Decl.”), ¶76. Patent Owner’s argument that domains are not “independent” if they are “intertwined” is at odds with both the plain meaning of “independent” and with Patent Owner’s proposed definition of that term. According to the plain meaning of “independent,” the domains “could have” different voltages and frequencies. Horst Dep. at 17:4-7; Brogioli Dep. at 28:7-10 (agreeing). That does not mean they cannot be “intertwined,” as such an interpretation would not read on the ’833 Patent itself. This is because the domains disclosed in the ’833 Patent themselves are intertwined—they “collectively share a single power budget [where] the higher the power consumed by the core domain, there is less power left for the graphics domain to consume and vice versa.” ’833 Patent at 2:5-11. Furthermore, by Patent Owner’s own argument, “while the voltage and frequency of the first domain can be controlled separately from the voltage and frequency of a second domain, *these values can nonetheless depend on one another.*” POR, 17. As detailed in the Petition, Conroy’s subsystems A and B are “independent,” and Patent Owner’s additional “not intertwined” limitation should be disregarded. *See* Petition, 72-73.

Specifically, the Petition explains that claim 1 requires domains to operate at “independent voltage and frequency;” and this is exactly how Conroy describes the voltage and frequency of its components. Petition, 72-73; Conroy, [0120]. Conroy says its “components have *independent* throttle settings,” a phrase which Patent Owner quotes, reinterprets as failing to mean “independent,” and dismisses. POR,

59-60; Conroy, [0120].⁵ Conroy’s “independent” and the claim term “independent” are the same, and Conroy’s domains have “independent” voltages and frequencies at least because they have “independent throttle settings.” Petition, 71-73.

B. Independent Claim 13, Dependent Claims 2-5, 7, 14-15, 17, and 18

Because Patent Owner presents no separate arguments for the patentability of claims 2-5, 7, 13-15, and 17, Patent Owner implicitly agrees with Petitioner’s arguments that those claims are unpatentable over Finkelstein and Conroy. POR, 60-61; Petition, 79-82.

VII. Conclusion

For the reasons above and in the Petition, the Board should find the challenged claims unpatentable.

⁵ Even if Patent Owner’s definition were to control (which it does not), evidence that Conroy’s subsystems are not “separately controlled” is brought from a figure which is unrelated to Conroy’s disclosure of “independent throttle settings.” Furthermore, Conroy discloses that for a given global throttle setting, a variety of different component-level throttle settings can be used. (Conroy, [0120].) In other words, the global throttle setting or power setting is a constraint, not a determination of the throttle settings for each independent subsystem.

Dated: August 16, 2024

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Certificate of Word Count

The undersigned certifies, in accordance with 37 C.F.R. § 42.24(d), that the foregoing **PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE** complies with the type-volume limitation of 5,600 words, comprising 3,668 words, excluding the parts exempted by § 42.24(c).

Dated: August 16, 2024

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Certificate of Service

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, the foregoing **PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE** was served on August 16, 2024, electronically via e-mail upon the following parties:

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