

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-01335
Patent 8,775,833 B2

Before WILLIAM V. SAINDON, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

SAINDON, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Mercedes-Benz USA, LLC (“Petitioner”) filed a petition (Paper 3, “Pet.”) to institute *inter partes* review of claims 1–5, 7, and 13–18 of U.S. Patent No. 8,775,833 B2 (Ex. 1001, “the ’833 patent”). We instituted *inter partes* review on February 26, 2024. Paper 10. Subsequent to institution, Daedalus Prime LLC (“Patent Owner”) filed a Response (Paper 16, “PO Resp.”), after which Petitioner filed a Reply (Paper 19, “Pet. Reply”) and Patent Owner filed a Sur-reply (Paper 20, “Sur-reply”). An oral argument was held on December 3, 2024, a transcript of which is found in Paper 26 (“Tr.”).

We have authority to enter this final written decision under 35 U.S.C. § 318(a). The standard for review is set forth in 35 U.S.C. § 316(e), which provides that “the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.” For the reasons provided below, we determine that Petitioner has met the burden of establishing unpatentability of some, but not all, challenged claims. In particular, we determine that Petitioner has established the unpatentability of claims 1–5, 7, and 13, but not claims 14–18.

B. Real Parties in Interest

Petitioner states that its real parties in interest are Mercedes-Benz USA, LLC, Mercedes-Benz Intellectual Property GmbH & Co. KG, Mercedes-Benz Group AG, and Mercedes-Benz AG. Pet. 2. Patent Owner states that its real party in interest is Daedalus Prime LLC. Paper 4, 2 (Patent Owner’s Mandatory Notice).

C. Related Matters

The parties both identify the following related matters outside the USPTO: *Daedalus Prime LLC v. Mazda Motor Corp.*, Case No. 1-22-cv-01109 (D. Del.), filed August 23, 2022, and dismissed against certain defendants—including Mercedes-Benz Group AG, Mercedes-Benz AG, and Mercedes-Benz USA, LLC—on March 20, 2023; *In the Matter of Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (U.S. International Trade Commission), filed September 12, 2022; *Daedalus Prime LLC v. Arrow Electronics, Inc.*, Case No. 1-22-cv-01107 (D. Del.), filed August 23, 2022, and dismissed on March 1, 2023; *Daedalus Prime LLC v. Mazda Motor Corp.*, Case No. 1-22-cv-01108 (D. Del.), filed August 23, 2022, and dismissed on November 14, 2022; *In the Matter of Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (U.S. International Trade Commission), filed August 23, 2022, and terminated on February 27, 2023; and *Daedalus Prime LLC v. Samsung Electronics Co.*, Case No. 2:22-cv-352 (E.D. Tex.), filed September 12, 2022, and dismissed as to the '833 patent on June 6, 2023. Pet. 2; Paper 4, 2.

The parties both identify the following related matters within the USPTO: *Qualcomm Inc. v. Daedalus Prime LLC*, IPR2023-00550 (PTAB), filed on February 2, 2023 (previously captioned as “*Samsung Electronics Co., v. Daedalus Prime LLC*”) (terminated on January 12, 2024 due to settlement). Pet. 3; Paper 4, 3.

D. Prior Art and Asserted Grounds

Petitioner's grounds rely on the following prior art references:

Name	Reference	Exhibit No.
Conroy	U.S. Pat. App. Pub. 2007/0049133 A1, pub. Mar. 1, 2007	1006
Bose	U.S. Pat. App. Pub. 2009/0089602 A1, pub. Apr. 2, 2009	1008
Finkelstein	U.S. Pat. App. Pub. 2010/0115304 A1, pub. May 6, 2010	1005
Nussbaum	U.S. Pat. App. Pub. 2011/0022356 A1, pub. Jan. 27, 2011	1007

Petitioner asserts that the challenged claims would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–5, 7	103	Finkelstein
7	103	Finkelstein, Conroy
13–15, 17, 18	103	Nussbaum
16	103	Nussbaum, Bose
13–15, 17, 18	103	Conroy
16	103	Conroy, Bose
1–5, 7, 13–15, 17, 18	103	Conroy, Finkelstein

Petitioner relies on the testimony of Robert W. Horst, Ph.D (Ex. 1029). Patent Owner relies on the testimony of Michael C. Brogioli, Ph.D (Ex. 2002).

E. Overview of the '833 Patent

The '833 patent is directed to a processor having multiple power domains sharing a single power budget. Ex. 1001, 2:5–6. A “power domain,” or simply “domain,” is described in the '833 patent as “a collection of hardware and/or logic that operates at the same voltage and frequency

point.” *Id.* at 1:58–61. Processors described in the ’833 patent typically have a first domain for the processor cores and a second domain for the graphics engine. *Id.* at 1:63–66. Because the processors and graphics are in different power domains, at any moment in time they can be allocated different amounts of power. This means that, depending on the nature of the workload (e.g., graphics-intensive or core-intensive), the power budget can allocate more power to one domain over the other. *Id.* at 2:5–31.

F. Challenged Claims

Claims 1–5, 7, and 13–18 are challenged. Claims 1, 8, and 13 are independent. Claims 1 and 13 are reproduced below.

1. A processor comprising:

a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency;

a memory controller coupled to the first and second domains;

at least one interface; and

first logic to dynamically allocate a power budget for the processor between the first and second domains at run time according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.

13. A system comprising:

a multicore processor having a first domain including a plurality of cores, a second domain including a graphics engine, and a third domain including system agent circuitry, the third domain to operate at a fixed power budget and including a power sharing logic to dynamically allocate a variable power budget between the first and second domains based at least in part on a first power sharing value for the first domain stored in a first

storage and a second power sharing value for the second domain stored in a second storage; and

a dynamic random access memory (DRAM) coupled to the multicore processor.

II. ANALYSIS

A. Legal Standards Used in the Merits Analysis

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious . . . to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that:

A person of ordinary skill in the art at the relevant time (“POSITA”) would have had a bachelor’s degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.

Pet. 9 (citing Ex. 1029 ¶¶ 29–30). Patent Owner applies the same definition, but modifies it to remove the words “at least” in the phrase, “at least two years of experience.” PO Resp. 11. Patent Owner argues that a person of ordinary skill in the art would have two years of experience, and argues that “at least two years of experience” means that they could have many more years of experience. *Id.* at 8.

As we understand it, Patent Owner is arguing that the phrase “at least [X] years of experience” creates a definition of the level of ordinary skill that has no upper bound, and that such unbounded definitions are improper. We believe an example of this would be that, because “20 years” is “at least 2 years,” then a person with 20 years of experience would be considered a person of ordinary skill, when perhaps in reality they have extraordinary skill.

We are not inclined to adopt Patent Owner’s proposal to require a specific number of years (or a fully bounded range) in the definition of the level of ordinary skill in the art. First, Patent Owner has not offered any legal authority supporting or justifying its position. Second, using the term “at least [X] years” is common practice and generally understood to be an

approximation regarding the minimum level of skill of a *hypothetical* person—in other words, no precision can truly be expected of the specific number of years in this context. *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (“The person of ordinary skill in the art is a hypothetical person.”). The point of the exercise is to provide context for a holistic obviousness analysis. *See id.* (setting out “various factors” used to analyze the level of ordinary skill); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991) (“The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.”); *Kimberly-Clark Corp. v. Johnson & Johnson*, 745 F.2d 1437, 1453 (Fed. Cir. 1984) (the hypothetical person is an “an imaginary being possessing ‘ordinary skill in the art’ created by Congress to provide a standard of patentability”). We are not persuaded of a need for strict precision in the number of years of experience of a hypothetical person used in our analysis in this case. Third, Patent Owner asks for no particular relief based upon its argument. That is, even if we agreed to remove “at least,” Patent Owner does not argue that the outcome of the Decision would be any different.¹

In conclusion, we apply Petitioner’s proposed level of ordinary skill because it is reasonably consistent with the level of skill implied in the disclosure of the ’833 patent and the cited prior art.

¹ For example, setting the level of skill to exactly two years of experience would not serve to automatically disqualify an expert having ten years. *Kyocera Senco Ind’l Tools v. Int’l Trade Com’n*, 22 F.4th 1369, 1377 (Fed. Cir. 2022) (requiring that “a witness must at least have ordinary skill in the art” and stating that “it would be improper to require an expert witness to possess ordinary skill in the art and *nothing more*”).

C. Claim Construction

Under 37 C.F.R. § 42.100(b), we apply the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). That is, “the words of a claim ‘are generally given their ordinary and customary meaning’ . . . that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1312–13.

Petitioner asserts that no claim terms require explicit construction. Pet. 10. Patent Owner provides a construction for the term “independent” of claim 1. PO Resp. 12–18. For context, claim 1 requires first and second domains, wherein “each of the first and second domains [] operate at an independent voltage and frequency.” Patent Owner provides its analysis and concludes that claim 1 requires that the voltage and frequency of the first and second domains to be “controlled separately from one another.” PO Resp. 14, 15. We disagree with Patent Owner’s conclusion. In particular, we note that Patent Owner is attempting to add a “control” limitation to the claim. The claim does not require independent control of the first and second domains, it requires them “to operate at an independent voltage and frequency.” That is, by the plain language of the claims, what is independent is the voltage and frequency of the first domain compared to the voltage and frequency of the second domain.

Patent Owner identifies many passages in the ’833 patent specification allegedly supporting its position, but we do not find any of these passages persuades us to agree with Patent Owner’s position. *See* PO Resp. 12–14 (citing Ex. 1001, 1:13–17, 1:63–66, 7:59–62, 8:27–31, 8:38–46, 10:4–8). These passages mostly state that the domains are independent,

which we understand to mean “separate” in this context. Ex. 1001, 1:63–66, 7:59–62, 8:27–31, 8:38–46, 10:4–8; *accord* PO Resp. 14 (summarizing these citations and concluding that “the term ‘independent’ is used in its ordinary sense to mean ‘separate.’”); Ex. 2002 ¶ 33 (same). One passage is similar to the claim language, and recites that a core can be “of an independent power domain and can be configured to operate at an independent voltage and/or frequency.” *Id.* at 8:27–31. We see nothing in these passages that would require independent *control* as opposed to “operate at an independent voltage and frequency” as claimed. Instead, in the one passage that is similar to the claim language, it is clear that what is “independent” is the “voltage and/or frequency.” *Id.* at 8:27–31.

Patent Owner then cites to another batch of passages from the ’833 patent and concludes that “a person of ordinary skill in the art would recognize that the ’833 patent is describing a situation in which voltages and/or frequencies of the different domains are controlled separately from one another.” PO Resp. 14–15 (citing Ex. 1001, 1:56–60, 1:63–66, 2:22–25, 2:32–36, 5:9–12, 5:21, 5:27–44, 7:20–24, 8:38–42, Fig. 1; Ex. 2002 ¶ 33). Most of these passages describe the domains being allocated portions of a power budget. *See* Ex. 1001, 1:56–60, 2:22–25, 5:28–40, 7:20–24, 8:38–42. One passage is similar to the prior batch of citations, stating that the domains themselves are independent. *Id.* at 1:63–66. Other passages describe a power control unit doing the allocation, and refers to this as “control.” *Id.* at 2:32–36, 5:27–26, 5:21, 5:40–44. Last cited by Patent Owner is Figure 1, which has a box labeled “Control First and Second Domains Frequency and Voltage.” *Id.*, Fig. 1 (item 130). Reviewing the cited passages and the figure, we find that the power control unit allocates or controls power.

However, the claim is not directed to the power control unit and it does not use the word “control.” The claim requires the first and second domains to have independent voltages and frequencies, and we fail to see any support in the specification to add an additional requirement for independent *control* of the first and second domains.

In view of the above, we are not persuaded by Patent Owner’s arguments or its expert’s testimony regarding the term “independent.” Instead, we give the term its plain meaning. In particular, for the first and second domains “to operate at an independent voltage and frequency,” that means that the first domain is able to operate at a separate voltage and frequency compared to the voltage and frequency of the second domain.²

With this understanding, we can turn to the prior art dispute, as no other terms require construction at this time. *Realtime, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

² We agree with both parties that the claim does not require the domains to actually operate at different voltages or frequencies, nor do they preclude the domains’ voltages or frequency from having a relationship with one another (they are sharing a common budget on a common piece of hardware). PO Resp. 16–19; Reply 2 (agreeing that “‘independent’ means ‘each domain *could have* a different voltage and frequency than the other domain.’”); Tr. 7:11–12 (“Petitioner actually agrees that the domains can have dependency on each other for the voltage and frequencies, or they can be different.”); 33:23–34:1 (Patent Owner’s counsel stating that, “while the voltages and frequencies may be different, they don’t have to be different. And I think the parties are agreed on that point.”).

D. Obviousness Analysis Roadmap

Independent claims 1 and 13 are both directed to a processor that dynamically allocates a power budget between first and second domains by using power sharing policy values. The differences relevant to this proceeding are that claim 1 requires that the domains operates at *independent voltages and frequencies*, whereas claim 13 requires that the *first domain contains a plurality of cores*, and that the first and second power sharing policy values are *stored in first and second storage* respectively. Reflecting these differences, two of the obviousness grounds focus on claim 1 and its dependents (Finkelstein, Finkelstein-Conroy) and four grounds focus on claim 13 and its dependents (Nussbaum, Nussbaum-Bose, Conroy, Conroy-Bose). Pet. 6–7. One ground covers both independent claims (Conroy-Finkelstein). *Id.* at 7. Below, we analyze the claim 13-only grounds led by Nussbaum and Conroy, then the joint claim 1-and-claim 13 ground of Conroy-Finkelstein. We do not reach the claim 1-only grounds led by Finkelstein because they are subsumed by the Conroy-Finkelstein ground, as will be made clear later.

*E. Asserted Obviousness Over Nussbaum (Claims 13–15, 17, and 18)
and
Nussbaum and Bose (Claim 16)*

Petitioner asserts that claims 13–15, 17, and 18 are unpatentable in view of Nussbaum (Pet. 36–51) and claim 16 is unpatentable in view of Nussbaum and Bose (*id.* at 51–54). Among these claims, claim 13 is independent, and requires that the multicore processor has a first domain that has a plurality of cores and a second domain that has a graphics engine. Each domain is given a power sharing value that determines its power

allocation. A dispositive issue for these grounds is whether Nussbaum teaches a first domain “including a plurality of cores.”

1. The Parties’ Positions on Nussbaum

Petitioner asserts that Nussbaum teaches a multicore processor that distributes power among various computational units such Core0, Core1, Core2, Core3, and a GPU (graphics processing unit). Pet. 37 (citing, e.g., Ex. 1007, Fig. 1); *see also id.* at 37–38 and Pet. Reply 9–11 (entire argument). Nussbaum provides an example allocation in Table 1, reproduced below:

TABLE 1	
On-die component	Allocated Power
Core0	8 w
Core1	8 w
Core2	8 w
Core3	8 w
GPU	5 w
Memory Controller	2 w
I/O Bridge	1 w
Total	40 w

Ex. 1007 ¶ 21 (Table 1). In this example, Cores 0–3 are allocated 8 Watts of power, a GPU is allocated 5 Watts, and other components are allocated 3 Watts, for total of 40 Watts.

Petitioner asserts that it would have been obvious that multiple cores, such as Core0 and Core1, are in the same power domain. Pet. 37 (citing Ex. 1029 ¶ 122). Petitioner points to Table 2 of Nussbaum, reproduced below:

TABLE 2

On-die component	Allocated Power	Remarks
Core0	16.75 w	Core can run at higher F, V to fill new power headroom
Core1	16.75 w	Core can run at higher F, V to fill new power headroom
Core2	0.5 w	Assume that idle core consumes 0.5 w
Core3	0.5 w	Assume that idle core consumes 0.5 w
GPU	2.5 w	
Memory Controller	2 w	
I/O Bridge	1 w	
Total	40 w	

Ex. 1007 ¶ 23 (Table 2). In this example, Core0 and Core1 have been allocated 16.75 Watts, Core2 and Core3 have been allocated 0.5 Watts, and the total allocation remains 40 Watts.

Patent Owner responds that Nussbaum does not teach multiple cores in the same power domain. *See* PO Resp. 46–49; Sur-reply 14–15. That is, even if Core0 and Core1 were bumped up to 16.75 Watts in Table 2, Patent Owner argues that they are not part of the same power domain but rather remain two separate power domains. PO Resp. 47 (arguing that the power allocation settings “are not per-domain attributes” but rather “per-core[] attributes”). Patent Owner bolsters its position by arguing that Nussbaum criticizes domain-based allocations. *Id.* at 48 (citing Ex. 1007 ¶ 19). At the cited paragraph, Nussbaum states that “treat[ing] all active units homogenously” means that “some active cores or other computational units may be gaining little to no performance increase.” Ex. 1007 ¶ 19. Nussbaum contrasts this by stating that “[s]electively distributing power among the active cores or other computational units . . . allows for greater overall system throughput.” *Id.*

Petitioner replies that Nussbaum assigns power allocations to computational units, and those computational units may include multiple cores. Pet. Reply 10 (citing Ex. 1007 ¶ 19–20). Patent Owner’s Sur-reply disputes this and argues that the power settings “are per-component, e.g., per-core, attributes, *not* per-domain attributes.” Sur-reply 14 (citing Ex. 2002 ¶ 63). In support, Patent Owner’s expert points to a passage in Nussbaum that states that the power settings of each computational unit are determined “[i]n order to evaluate which of the *cores* can better exploit an increase in performance capability.” Ex. 1007 ¶ 25 (emphasis added) (cited in Ex. 2002 ¶ 63).

2. Analysis of the Parties’ Positions on Nussbaum

Claim 13 requires a first domain that includes a plurality of cores. In claim 13, it is the domain that is allocated the power budget (as opposed to the domain’s individual cores). See Ex. 1001, 12:57–59 (“allocate a variable power budget between the . . . domains”), 1:56–66 (explaining domains—“the term ‘domain’ is used to mean a collection of hardware and/or logic that operates at the same voltage and frequency point”). We agree with Patent Owner and credit its expert that Nussbaum is concerned with the power settings of each individual core, GPU, or other computational unit. Ex. 2003 ¶ 63. Even if, in one passage, Nussbaum talks about power reallocation in “computational units, such as the CPU or [GPU],” in context it is clear that the allocations remain on the individual, e.g., core, level. Ex. 1007 ¶¶ 19–20, 21 (Table 1), 23 (Table 2), 24. First, in the sentence just cited, Nussbaum disparages treating units homogenously, i.e., adjusting them in groups or domains (as required by claim 13). *Id.* ¶ 19. Then, Nussbaum praises distributing power “among the active cores or other computational

units,” i.e., on an individual or core level. *Id.* In this phrase, Nussbaum is not using “computational units” as a word meaning “CPU,” because Nussbaum already directly references the “cores” in the phrase. *Id.* Nussbaum later discusses figuring out how each core reacts to power changes, in order to determine which cores can better exploit additional power. *Id.* ¶¶ 25–28. For these reasons, we credit the testimony of Patent Owner’s expert that Nussbaum does not disclose allocating power to a plurality of cores as a single domain (Ex. 2002 ¶ 63), which is consistent with the above-noted disclosures of Nussbaum.

As to Petitioner’s argument that Nussbaum says that a CPU includes multiple processing cores (Pet. Reply 10), the passage cited instead says that the “System on a Chip” includes multiple CPU processing cores (Ex. 1007 ¶ 20). We are not persuaded that Nussbaum shows, by a preponderance of the evidence, grouping multiple CPU cores to allocate power to them as a single domain.

Petitioner’s expert does not appear to believe that Nussbaum shows the claimed power domain either, and instead says that a person of ordinary skill in the art “would have understood [Tables 1 and 2] to mean that Core 0 and Core 1 are operating in the same power domain.” Ex. 1029 ¶ 122 (cited at Pet. 37). Petitioner’s expert’s logic appears to be that because Core0 and Core1 have the same power level, they must be in the same domain. To support this, Petitioner’s expert says that the ’833 patent describes a domain as “a collection of hardware and/or logic that operates at the same voltage and frequency point.” *Id.* (quoting Ex. 1001, 1:58–60). However, it is a logical fallacy to state that *A yields B* means that *B yields A*. That is, even if a domain is something that operates at the same voltage and frequency point,

that does not mean that everything that operates at the same voltage and frequency point is within the same domain. Following Petitioner's logic, Cores 0–3 are in the same domain in Table 1 of Nussbaum, but then Cores 0 and 1 are suddenly in a different domain from Cores 2 and 3 in Table 2. For all the above reasons, we do not find Petitioner's or its expert's logic persuasive, and we do not credit the testimony of its expert on this point.

3. Conclusion as to the Nussbaum-Led Grounds

We find that Petitioner has not established by a preponderance of the evidence that Nussbaum teaches claim 13's first domain including a plurality of cores. This deficiency affects all of the claims in the Nussbaum and Nussbaum-Bose grounds.

F. Asserted Obviousness Over Conroy (Claims 13–15, 17, and 18) and Conroy and Bose (Claim 16)

Petitioner asserts that claims 13–15, 17, and 18 are unpatentable in view of Conroy, and claim 16 is unpatentable in view of Conroy and Bose. Pet. 55–67. The parties' briefs focus on claims 13 and 14. *See generally* PO Resp. 28–43; Pet. Reply 5–9; Sur-reply 8–13. We will address claim 13 in full before turning to claim 14 and the claims that depend therefrom. For the reasons expressed below, we determine that Petitioner has shown that claim 13 is unpatentable, but has not shown that claim 14 or claims 15–18, which depend from claim 14, are unpatentable.

1. Conroy Ground — Claim 13

Claim 13 requires a first domain including a plurality of cores, a second domain including a graphics engine, and a third domain including a power sharing logic. In addition, a variable power budget between the first

and second domains is based on a first power sharing value stored in a first storage, and a second power sharing value stored in a second storage. The dispute for claim 13 involves whether Conroy teaches the claimed first and second storage. PO Resp. 28–37; Pet. Reply 4–6; Sur-reply 8–10.

a) The Parties’ Positions on Conroy (Claim 13)

Petitioner asserts that the claimed “first domain including a plurality of cores” reads on the main microprocessors (CPUs) in Conroy. Pet. 55–56. In particular, Petitioner states that the main microprocessors are controlled by a throttle setting that indicates that the cores are operating in the same domain using the same throttle setting. *Id.* at 56 (citing, e.g., Ex. 1006 ¶¶ 167, 225; Ex. 1029 ¶ 170).

Petitioner asserts that the claimed “second domain including a graphics engine” reads on the GPU in Conroy. *Id.* at 57 (citing Ex. 1006 ¶ 225). Petitioner notes that the GPU operates in a second domain because it can receive a different amount of power from the main microprocessors of the first domain. *Id.* (citing Ex. 1006 ¶¶ 196–197, 203; Ex. 1029 ¶ 171).

Petitioner asserts that the claimed “third domain including system agent circuitry . . . to operate at a fixed power budget and including a power sharing logic” reads on the power manager in Conroy. *Id.* at 57–59 (citing, e.g., Ex. 1006 ¶¶ 94, 168, 225; Ex. 1029 ¶ 174). Petitioner here cites to passages explaining that the power manager 3708 in Conroy is a microcontroller (Ex. 1006 ¶ 225), which is also described as microcontroller 411 (*id.* ¶ 94) and power manager/microcontroller 1207 (*id.* ¶ 168). Petitioner asserts that Conroy’s power manager is “used to budget the power usage dynamically” and is a “non-throttled component.” Pet. 57–58 (quoting Ex. 1006 ¶¶ 81, 94).

Petitioner asserts that the claimed “dynamic random access memory (DRAM) coupled to the multicore processor” reads on the “volatile RAM” in Conroy. *Id.* at 62 (citing Ex. 1006 ¶ 225, Fig. 37). In particular, Petitioner points out that, in Conroy, “volatile RAM” is “typically implemented as dynamic RAM (DRAM).” *Id.* (quoting Ex. 1006 ¶ 187).

Patent Owner does not dispute Petitioner’s contentions as to these limitations.

As to the disputed limitation, requiring first and second power sharing values stored in first and second storage, Petitioner points to Conroy’s teachings of power weighting values for the subsystems (e.g., CPU and GPU), which are stored in power distribution tables. Pet. 59–61 (citing, e.g., Ex. 1006 ¶¶ 6, 200, 203, Figs. 21A–C, 22). For example, Petitioner identifies a table of a “Balanced load profile” in Figure 21A of Conroy, reproduced below:

Balanced load profile K1 (e.g., 0.5, 0.5)

2100 2105 {		2101	2102	2103	2104
		Settings	CPU	GPU	Allocated Power
		Setting 1	A1 (e.g., 10)	B1 (e.g., 10)	P1 (e.g., 20)
		Setting 2	A2 (e.g., 7)	B2 (e.g., 7)	P2 (e.g., 14)
		Setting 3	A3 (e.g., 5)	B3 (e.g., 5)	P3 (e.g., 10)

Fig. 21 A

Ex. 1006 ¶ 21A. Figure 21A of Conroy depicts the various power settings for a CPU and a GPU, wherein the power allocated to each of them is equal. *Cf. id.* at Fig. 21B (depicting a CPU-heavy load profile), Fig. 21C (depicting a GPU-heavy load profile). These settings include clock and voltage settings for the components, as identified in various figures, such as Figure 7. *Id.* at 203. As to Figure 7, Petitioner directs our attention to “multiple components” that identify the different settings as “Throttle Setting[s].” *Id.*

at Fig. 7, ¶ 120. Petitioner points to a teaching in Conroy that “the microcontroller may store [a] determined throttle setting in a register.” Pet. 61 (quoting Ex. 1006 ¶ 97). Petitioner asserts that a person of ordinary skill in the art “would have found it obvious to use registers to store the various power settings depicted in Conroy’s Figures 7, 21, and 22.” *Id.* at 61 (citing Ex. 1006 ¶¶ 97, 225; Ex. 1029 ¶ 185). Petitioner asserts that, as a result of storing the settings in registers, Conroy would store, for example, the CPU setting in a first register and the GPU setting in a second register. *Id.* (citing Ex. 1006 ¶ 97; Ex. 1029 ¶¶ 183–186).

Patent Owner’s first argument is that storing two power sharing values in *a* memory is not storing them in *first* and *second* storages. PO Resp. 34, 35–36; Sur-reply 8–10. Petitioner replies that Conroy’s single memory stores a table of power sharing values, and within that table, the individual power sharing values would be stored in separate registers. Pet. Reply 5–6. Petitioner points out that the ’833 patent similarly stores the power sharing values in a table with the values stored in separate registers in that table. *Id.* (citing Ex. 1001, 4:5–10, Table 1, 8:59–62).

Patent Owner’s second argument is that the “throttle settings” in Conroy “are *not* the contents of the power distribution tables, but instead are the actual powers consumed by each subsystem.” PO Resp. 35; Sur-reply 10. As we understand it, Patent Owner’s position is that the contents of the tables in Conroy are the power quantities consumed by each subsystem, rather than prescriptive power settings. Petitioner replies that the “throttle settings” and the “actual powers consumed” are different things in Conroy. Pet. Reply 6. In particular, Petitioner states that “[a]ctual power[] consumed’ cannot be the ‘throttle setting’ itself because a ‘throttle setting’ in

Conroy is a voltage and/or frequency setting.” *Id.* (citing Ex. 1006 ¶¶ 50, 64–65, 81; Ex. 1032, 47:24–48:14).

b) Analysis of Conroy (Claim 13)

(1) Storage

We are unpersuaded by Patent Owner’s first argument that Conroy stores its power allocation settings in one memory, and therefore not first and second storages. The claim requires the two power sharing values to be stored in first and second storages, but says nothing about the physical location of these storages. A “storage” is a generic term that includes memories and registers. Ex. 1001, 4:1–20 (describing the policy values stored in different cells in a table as stored in “registers”); Tr. 34:16–17 (Patent Owner’s counsel stating, “I don’t think anyone would disagree that memory is a form of storage”). Thus, storage in different registers is storage in different storages, even if individual registers may be subcomponents of some larger data-storage structure such as a memory that is also a storage. As Petitioner points out (Pet. Reply 5–6), the ’833 patent stores its values in a single location, yet calls out how the specific values are in “registers” (emphasis added). Ex. 1001, 8:59–62 (policy values are stored in “power control storage 357 [of Fig. 6].”), 4:7–25 (depicting a single table storing the policy values and describing the two values in that table as “two such configuration registers”). We agree with Petitioner that the values in the table in Conroy are in separate registers, and thus separate storages, in the same way that the values in the table of the ’833 patent are in separate registers, and thus separate storages. Pet. Reply 5–6. For example, Table 21A (reproduced earlier) shows “Setting 1” with a CPU value of “A1 (e.g., 10)” and a GPU value of “B1 (e.g., 10).” Ex. 1006, Fig. 21A. These

different settings represent different clock (frequency) and voltage settings as described in earlier figures, such as Figures 6 and 7, that are also called “throttle settings.” *Id.* ¶¶ 120, 203. Conroy states that a throttle setting is stored in a register. *Id.* ¶ 97. Taking into account these facts, we credit the testimony of Petitioner’s expert that the first and second power sharing values in Conroy are stored in first and second storage. Ex. 1029 ¶¶ 183–186. We do not credit the testimony of Patent Owner’s expert, who instead makes an overly semantic argument that does not properly account for the above facts and instead reads “a memory” out of context and in a manner ignores the actual arrangement of components of the ’833 patent and the prior art. *See* Ex. 2002 ¶ 48. Thus, we find that the various values stored in Conroy are stored in multiple storages.³

(2) Power Sharing Values

Patent Owner’s second argument, that the values stored in Conroy are not power sharing values, is also unpersuasive. Claim 13 requires the power budget to be allocated based at least in part on the first and second power sharing values. Ex. 1001, 12:58–61. Petitioner relies on the “power weighting arrangement” set out in the power distribution tables of Conroy.

³ Further, although Patent Owner did not make the argument, we note that Petitioner’s understanding of the claim does not render the first and second storage limitations superfluous. Given that the third domain is fixed, one could have used a single power sharing value in a single storage to calculate the budget for both the first and second domain. For example, if the system only had a power sharing value for the first domain, then the second domain’s budget is equal to the total budget minus the allocations for the first and third domains. The ’833 patent distinguishes from such systems, as it allows for more domains by having a policy for each domain. Ex. 1001, 4:43–56.

Pet. 59–60. The tables label the various entries as *settings* (*see, e.g.*, Ex. 1006, Figs. 6, 7, 21A–C), such that we find Patent Owner’s arguments that they are instead the “actual powers consumed by each subsystem” unpersuasive. *See, e.g.*, PO Resp. 35 (citing Ex. 2002 ¶ 49). Even if we assume Patent Owner and its expert are correct that Conroy discusses storing a measured throttle “setting” in one passage (*see* Ex. 1006 ¶¶ 94–97), it is clear that the settings of the tables relied on by Petitioner are not measured values but rather prescribed settings. For example, Figure 7 depicts “Setting 1 for Component A” as applicable to “Global Throttle Setting” 1 and 2. If Figure 7 were depicting measured values, there would be no reason to list different global settings or settings for component A multiple times. *See* Ex. 1006, Fig. 7. Conroy further describes these entries as being “arranged by the designer of the system,” something that would be impossible if these were present-time, measured values. *Id.* ¶ 121. Similarly, in Figures 21A–C, Conroy depicts multiple settings for the same component in each table, which would make no sense if this were merely storing measured values. Indeed, Conroy describes the various entries as a “strategy,” not as measurements. *Id.* ¶¶ 201, 203. Accordingly, we do not credit the testimony of Patent Owner’s expert on this issue. Instead, we agree with and credit Petitioner’s expert that Conroy discloses its tables having power sharing values as claimed. Ex. 1029 ¶¶ 183–186.

c) Conclusion for Conroy (Claim 13)

In summary of the above, we noted that Petitioner has identified where Conroy teaches each of the undisputed limitations. We found these uncontested positions adequately supported by the record, and adopt them as our own findings. As to the disputed limitation, whether Conroy teaches

first and second power sharing values stored in first and second storage, we found that the power weighting strategies that allocate power to various domains such as the CPU and GPU in Conroy disclose the claimed first and second power sharing values. Further, we found that these tables store the values in registers, disclosing the claimed first and second storage. Having reviewed the arguments and evidence before us, we determine that Petitioner has established by the preponderance of the evidence that Conroy teaches or suggests each element of claim 13.

2. Conroy Ground — Claim 14

Claim 14 depends from claim 13 and adds that the power sharing logic determines a power budget for a “current time interval.” The dispute for claim 14 is whether Conroy teaches the claimed current time interval. PO Resp. 37–39; Pet. Reply 7–9; Sur-reply 11.

a) The Parties’ Positions on Conroy (Claim 14)

Petitioner’s position is that Conroy teaches the claimed “determin[ing] the variable power budget for a current time interval” based on the following passage in Conroy:

In one embodiment of the present invention, with the knowledge of the past power usage (e.g., measurements 211, 213, . . . , 219 at times $T-(n-1)\Delta$, $T-(n-2)\Delta$, . . . , T) the system can dynamically determine the allowable power budget for the next time interval (e.g., for time $T+\Delta$).

Ex. 1006 ¶ 70 (discussed at Pet. 63, Pet. Reply 7); Ex. 1029 ¶ 191. This passage describes what is shown in Figure 2 of Conroy, where the “past power usage” is considered when determining the power budget 205. Ex. 1006 ¶ 70. Petitioner notes that, in this passage, the *past* power usage includes past time intervals up to time T . Pet. 63. Petitioner reasons that, if

the *past* includes all the times up to time T , then the *current* time interval must be the *next period of time that comes after the past*, which is time $T+\Delta$. *Id.*; Pet. Reply 7. Thus, according to Petitioner, time $T+\Delta$ is the current time interval.

Patent Owner's position is that Conroy explicitly describes time $T+\Delta$ as the "next time interval," not the current time interval. PO Resp. 38–39; Sur-reply 11.

b) Analysis of Conroy (Claim 14)

We are not persuaded by Petitioner and its expert's logic that the time interval $T+\Delta$ in Conroy is the same as the claimed "current time interval." Conroy explicitly describes $T+\Delta$ as the *next* time interval. Ex. 1006 ¶ 70. Petitioner and its expert would have us ignore that, but do not persuasively explain why. Certainly, in some abstract context, the present follows the past and the future follows the present. However, the context here is not an abstract ordering of time intervals, but rather a power budgeting process. Petitioner and its expert do not persuasively explain, nor do we see, why Conroy needs to set a current time interval budget. Instead, Conroy tracks "actual *past* power usage information to ensure that even if the computer is fully busy in the *next* time interval . . . the [power] limit [] will not be violated." *Id.* ¶ 63 (emphasis added). The past, actual power usage is used to "dynamically determine the allowable power budget for the *next* time interval." *Id.* ¶ 70 (emphasis added). In other words, the budget Conroy creates is a budget for the next time interval; the budget in use now was set sometime in the past. *See id.* This is exactly what Petitioner's above-quoted paragraph of Conroy states when it lists time interval T , presumably the current time, to be part of the "past power usage" when considering what

budget to set next. *See id.* Conroy continues with this theme when it says that once the next time period is reached, actual power is measured, and that information is used for setting the power budget and throttle setting for a *future* time period. *Id.* ¶ 73.

Because his testimony is consistent with the above, we credit the testimony of Patent Owner’s expert, that the power budget in Conroy is being determined for the *next* time interval, not the current time interval as claimed. Ex. 2002 ¶¶ 53–54 (discussing Ex. 1006 ¶¶ 69–71). Petitioner’s expert’s testimony is less consistent with the teachings of Conroy, and we do not credit it over the testimony of Patent Owner’s expert. Ex. 1029 ¶ 191.

c) Conclusion for Conroy (Claim 14)

We determine that Petitioner has not met its burden to show that Conroy teaches the “current time interval” of claim 14. Petitioner’s analysis for claims 15–18, which depend from claim 14, relies on its analysis for claim 14. Pet. 63–67. Thus, we determine that Petitioner has not met its burden to show that Conroy teaches the limitations of claims 15–18.

*G. Asserted Obviousness Over Conroy and Finkelstein
(Claims 1–5, 7, 13–15, 17, and 18)*

Petitioner asserts that claims 1–5, 7, 13–15, 17, and 18 are unpatentable over Conroy in view of Finkelstein. Pet. 68–82. Because the scope of independent claim 1 differs from that of independent claim 13, as discussed above, we will address the ground for claims 1 and 13 separately.

1. Conroy-Finkelstein Ground — Claims 1–5, 7

Independent claim 1 is directed to a processor comprising a first and second domain, where each of the first and second domains operates at an

independent voltage and frequency. In addition, the processor includes a memory controller, an interface, and a first logic to dynamically allocate a power budget for the processor. The dispute between the parties over claims 1–5 and 7 is limited to claim 1; we focus our analysis on that claim.

a) The Parties’ Positions on Conroy-Finkelstein (Claims 1–5, 7)

Petitioner asserts that Conroy teaches “a first domain and a second domain” as claimed. Pet. 71–73. In particular, Petitioner asserts that Conroy’s CPU is the first domain and its GPU is the second domain. *Id.* (citing, e.g., Ex. 1006, Fig. 37). This aspect of the ground is not challenged. Claim 1 further requires these domains to have “independent voltage and frequency,” which Patent Owner challenges and we address later on, after discussing the remaining limitations of claim 1.

Petitioner asserts that Conroy teaches “a memory controller coupled to the first and second domains” as claimed. *Id.* at 73–75. In particular, Petitioner asserts that Conroy discloses a system that includes an “interconnect (e.g., a bus)” as well as a “memory,” and asserts that a person of ordinary skill in the art implementing these teachings would have found it obvious to implement Conroy by ensuring the interconnect included a bus connected to the memory controller. *Id.* (quoting Ex. 1006 ¶¶ 187, 225). This aspect of the ground is not challenged.

Petitioner next asserts that Conroy discloses “at least one interface” as claimed. *Id.* at 75–76. In particular, Petitioner asserts that the previously mentioned interconnect is an interface “because an ‘interconnection’ that interconnects the various components of [a] system [] together serves as an interface between these components.” *Id.* at 76 (citing Ex. 1006 ¶¶ 187, 225; Ex. 1029 ¶ 228). This aspect of the ground is not challenged.

Petitioner then asserts that Conroy discloses a “first logic to dynamically allocate a power budget for the processor between the first and second domains at run time [using] . . . first . . . and second sharing policy value[s]” as claimed. *Id.* at 59–61, 76–77. In particular, Petitioner points to Conroy’s teaching of the microcontroller to “dynamically budget power usage and determine throttle settings.” Ex. 1006 ¶ 190 (quoted at Pet. 59). Petitioner then points to Conroy’s teaching that these various throttle settings allocate power between the CPU and GPU, i.e., the first and second domains. Pet. 76–77 (citing Ex. 1006 ¶¶ 196–197, 203). Petitioner also points to Conroy’s teaching of various tables setting out policy sharing values for the first and second domain. *Id.* at 59–61 (citing, e.g., Ex. 1006, Figs. 7, 21, and 22). Patent Owner does not dispute this aspect of the ground.

Finally, Petitioner turns to Finkelstein for the limitation requiring that “the first and second sharing policy values [are] controllable by user-level software.” Pet. 23–27, 77–78. Petitioner points to two teachings in Finkelstein for this. The first is a passage that states that, for a given constraint, “user (or application defined) preferences [] describe how [the power] budget E^k is distributed among power planes.” Ex. 1005 ¶ 34. The second is a passage that states that a given power limit can be “changed on-the-fly (e.g., by a software application or a user).” *Id.* ¶ 31. These aspects of the ground are not challenged. However, Patent Owner does challenge Petitioner’s reasons for combination. We turn now to Patent Owner’s arguments.

Patent Owner’s first argument is that the subsystems in Conroy do not operate at an independent voltage and frequency. PO Resp. 59–60; Sur-

reply 17–18. Patent Owner acknowledges that Conroy states that “components have independent throttle settings” (*id.* at 60 (quoting Ex. 1006 ¶ 120)), but argues that those throttle settings are “merely variable, not separately controlled” (*id.* at 60). Put another way, a Patent Owner argues that Conroy’s throttle settings are “intertwined, not independent.” *Id.* at 60. Petitioner replies that Patent Owner’s arguments are not founded on the plain meaning of “independent.” Pet. Reply 15–17. Petitioner also replies that Conroy explicitly states its “components have *independent* throttle settings.” *Id.* at 16 (quoting Ex. 1006 ¶ 120, with added emphasis). In its Sur-reply, Patent Owner again asserts that “independent” means “separately controllable.” Sur-reply 17–18 (citing Ex. 2002 ¶ 75).

Patent Owner’s second argument is that Petitioner has not established a reason to combine the teachings of Conroy and Finkelstein. PO Resp. 57–59. Patent Owner asserts that Conroy and Finkelstein “operate at different levels within a system.” *Id.* at 57. Patent Owner also asserts that “Conroy is agnostic when it comes to the manner in which power is allocated,” such that “there is no need to modify the power allocation approach of Conroy.” *Id.* at 58. Petitioner replies that “Patent Owner mischaracterizes the Petition.” Pet. Reply 15. In its Sur-reply, Patent Owner states that Petitioner’s reasons for combination are “generalized considerations [that] do not support a motivation to combine.” Sur-reply 17.

b) Analysis of Conroy-Finkelstein (Claims 1–5, 7)

For the reasons set out below, we do not find Patent Owner’s arguments persuasive. We address these arguments and then turn to the dependent claims, which Patent Owner does not argue separately.

(1) *First Argument — “independent voltage and frequency”*

Claim 1 recites “a first domain and a second domain, each . . . to operate at an independent voltage and frequency.” As explained in the Petition (Pet. 71–73), Conroy discloses power distribution tables of “components [that] have independent throttle settings” (Ex. 1006 ¶ 120), such as the CPU and GPU (*e.g.*, *id.* at Fig. 21A), and that the tables “may include various operating frequencies or voltages that correspond to different system settings” (*id.* ¶ 205). *See also id.* ¶ 116 (describing a table of CPU throttle settings and noting that, “when a throttle setting is determined, both the CPU core voltages and frequencies are determined”); Ex. 1029 ¶¶ 220–221 (explaining the relationship between power and voltage/frequency).

Patent Owner argues that the systems in Conroy “are merely variable, not separately controlled,” and that the systems in Conroy are intertwined, not independent. PO Resp. 59–60 (citing Ex. 2002 ¶ 76). Patent Owner and its expert both cite to the same passage in Conroy as support. PO Resp. 60; Ex. 2002 ¶ 76. At that passage, Conroy states that the tables cited by Petitioner are “built [in] such a way that if a system moves from one system setting . . . to another system setting . . . , the power needed to operate each of the subsystems increase or decrease at the same time.” Ex. 1006 ¶ 203.

Reviewing the parties’ citations to Conroy in context, Patent Owner’s argument is unavailing. We will use Figure 21B of Conroy as an example to explain why. Figure 21B is reproduced below:

CPU-heavy load profile K2 (e.g., 0.75, 0.25)

2105 {	2110	2101	2102	2103	2104
	Settings	CPU	GPU	Allocated Power	
	Setting 1	A1 (e.g., 15)	B1 (e.g., 5)	P1 (e.g., 20)	
	Setting 2	A2 (e.g., 10)	B2 (e.g., 4)	P2 (e.g., 14)	
	Setting 3	A3 (e.g., 7)	B3 (e.g., 3)	P3 (e.g., 10)	

Fig. 21 B

Ex. 1006, Fig. 21B. Figure 21B of Conroy depicts a “CPU-heavy load profile,” where the power in each setting is largely apportioned to the CPU over the GPU (i.e., first and second domains). *Id.* ¶ 203. What the passage cited by Patent Owner is talking about is that the system can move from Setting 1, having 15 power distributed to the CPU and 5 to the GPU, to Setting 2, having 10 power distributed to the CPU and 4 to the GPU, and it will retain that CPU-heavy load profile. *Id.* ¶ 203. As Conroy explains in the next sentence, “when performance of the system transitions between system power settings 1–3 within the same power distribution table, the load profile of the system does not change.” *Id.* Notably, the passage says nothing about the voltage and frequency of the CPU being determined by the voltage and frequency of the GPU, which is what the claim precludes. Instead, it is merely saying that when the system selects different settings from the “CPU-heavy load profile” table, for example, the power allocation between the CPU and GPU remains CPU-heavy. *Id.*

To the extent Patent Owner is arguing that the tables in Conroy show that *both* the CPU and the GPU power levels are changed when one moves from one setting to the other, and that this means there is no “independent control,” then we note that, as we have already explained in our claim construction section, the claim does not require independent *control* (e.g., a step of modifying the voltage and/or frequency of the first domain and the first domain only). The claim does not include the word “control,” nor is it a method claim. Instead, the claim requires that the domains are able to *operate at* an independent voltage or frequency. The fact that both domains are set at the same time says nothing about the voltage and frequency at which they operate. And Conroy makes clear that, ultimately, the various

settings in the table are different clock/frequency and voltage settings. Ex. 1006 ¶¶ 120 (“In FIG. 7, multiple components have independent throttle settings.”), 203 (“Settings of the system may be, e.g., different clock, and different core voltage settings, as described above with respect to FIGS. 1–17”). In light of the above, we do not credit the testimony of Patent Owner’s expert (Ex. 2002 ¶ 76) because it is not based on the claim language. Instead, we find that Conroy discloses a first and second domain that operate at independent voltages and frequencies.

(2) Second Argument — Reason to Combine

As we explained in our overview of the parties’ positions, Petitioner uses the teachings of Finkelstein in order to add user-level control to the power management scheme in Conroy. *See* Pet. 77–88. In the Petition, Petitioner states that “Conroy itself contemplates certain levels of designer/user control over the recorded settings,” because they can be arranged manually by the designer of the system. *Id.* at 78 (citing Ex. 1006 ¶¶ 121, 225). Petitioner adds that Finkelstein explicitly discloses “‘user (or application defined) preferences’ that describe how to distribute the power budget between the first and second domains.” *Id.* at 77–78 (quoting Ex. 1005 ¶ 34). Petitioner asserts that a person of ordinary skill in the art “would have been motivated to combine the teachings of Conroy with the teachings of Finkelstein to provide a user with abilities to arrange or adjust the settings recorded in Conroy’s power distribution tables,” and would have a reasonable expectation of success in doing so. *Id.* at 78 (citing Ex. 1029 ¶¶ 236). Petitioner adds that the proposed combination “would have been nothing more than providing a routine user interface to edit and/or revise values in [the] table[s].” *Id.*

Patent Owner’s arguments against Petitioner’s reason to combine do not address these passages of the Petition. *See generally* PO Resp. 57–59, Sur-reply 17–18. Instead, Patent Owner challenges a separate, general rationale that Petitioner made at the beginning of its ground. *See* Pet. 69. Rationales that are broad and general may be persuasive. *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797 (Fed. Cir. 2021) (“[R]ationale[s] [are] not inherently suspect merely because [they’re] generic in the sense of having broad applicability or appeal. Quite the opposite.”). We need not evaluate Petitioner’s general rationale here, however, because we find Petitioner’s *unrebutted*, specific rationale arguments about providing a user interface to edit or revise the power sharing values to be persuasive. *See* Pet. 77–78 (citing, e.g., Ex. 1029 ¶ 236). In particular, we agree with Petitioner that providing a user interface to allow a user to edit the power tables, as taught in Finkelstein, would have been a routine and obvious modification to Conroy. As Petitioner’s expert points out, even beyond the teachings of Finkelstein, it was known in the art to allow users control over power allocation. Ex. 1029 ¶ 236 (citing Ex. 1026, 11:13–27 (describing a “user preferences database” containing “parameters and procedures for how to apportion power among various devices”); Ex. 1028 ¶ 17 (“The [power allocation] preference might be determined . . . based on a selection by a user of the system (e.g., via a graphical interface).”)). Thus, Petitioner’s proposed combination is an example of using a known feature to provide a known benefit. The known feature is a user interface, and the known benefit is allowing the user to indicate their preferences through the interface. *See* Ex. 1029 ¶ 236; *KSR*, 550 U.S. at 417 (“[A] court must ask whether the

improvement is more than the predictable use of prior art elements according to their established functions.”).

Based on the record before us, we determine that Petitioner has established a reason with rational underpinnings for combining the user level control interface of Finkelstein with the power management system of Conroy.

(3) Unargued Claims

For the Conroy-Finkelstein ground, Patent Owner does not separately argue dependent claims 2–5 and 7. PO Resp. 60. We deem any argument Patent Owner has not raised to challenge Petitioner’s grounds to have been forfeit, and every material fact not specifically denied to have been admitted. *See also* 37 C.F.R. § 42.23(a) (in a reply, “[a]ny material fact not specifically denied may be considered admitted”); Paper 11, 9 (Scheduling Order) (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived”). We briefly review Petitioner’s unchallenged positions on these claims.

Claim 2 requires “the first logic [] to determine a portion of the power budget to allocate to the first domain based on the first sharing policy value.” Petitioner points to Conroy’s power weighting arrangements in the power distribution tables as being the claimed sharing policy values. Pet. 59–61, 76–78, 79. For example, the CPU could be the first domain, the GPU the second domain, and a power distribution table shows that the CPU receives 75% of the power budget, whereas the GPU receives 25% of the power budget. *Id.* at 59–60 (discussing, e.g., Ex. 1006, Fig. 21B). Petitioner’s unchallenged assertion is persuasive. We agree that the power allocation tables in Conroy teach the claimed sharing policy values.

Claim 3 requires “the first logic [] to dynamically allocate the power budget [] according to a first . . . and a second minimum reservation value[s] for the [first and] second domain[s].” Claim 3 also requires that the “minimum reservation values [are] controllable by the user-level software.” Petitioner points to Conroy’s disclosure of a “power usage range” between a “minimum possible power consumption” and a “maximum power consumption.” Pet. 64–65, 79 (quoting Ex-1006 ¶ 53, Fig. 1). Petitioner also points to Finkelstein’s disclosure of making the power budget values controllable by the user. *Id.* at 28–30, 79–80 (citing, e.g., Ex. 1029 ¶¶ 240–241). Petitioner’s unchallenged assertions are persuasive. We agree that the “minimum possible power consumption” in Conroy teaches the claimed minimum reservation values. We have already determined that it would have been obvious to add a user interface to modify the power settings in Conroy, as taught in Finkelstein. Thus, we also agree that it would be obvious to make the minimum power level settings available in that user interface. *KSR*, 550 U.S. at 417.

Claim 4 requires “the first logic [] to provide at least a first portion of the power budget to the first domain, . . . corresponding to the first minimum reservation value.” Petitioner again points to Conroy’s disclosure of a “minimum possible power consumption” value. Pet. 76–78, 79–80. Petitioner’s unchallenged assertion is persuasive for the same reasons as its unchallenged assertion for claim 3.

Claim 5 requires “the first logic [] to determine the power budget for a current time interval based at least in part on a power budget carried forward from a previous time interval, . . . and a power budget decay value.” Pet. 23–27, 30–32, 62–63, 80–81. Petitioner refers back to its analysis for claim

14 in the Conroy-alone ground to teach a current time interval. Pet. 80. As we explained in our analysis of the Conroy-alone ground, we are not persuaded by a preponderance of the evidence that Conroy discloses a power budget for a current time interval. Notwithstanding, Petitioner has an alternative position based on Finkelstein. *Id.* at 80–81. In particular, Petitioner points out that in Finkelstein, an “energy budget may be managed and/or power setting(s) (e.g., voltage and/or frequency changes) may be made according[] to a current budget.” Ex. 1005 ¶ 28 (quoted at Pet. 30). The power budget E at the time $n+1$ is “defined iteratively” based on time n . *Id.* (formula 1). The formula includes a parameter α that is described as the “decay component.” *Id.* ¶ 29. These disclosures are consistent with Petitioner’s expert’s unchallenged testimony asserting that Finkelstein teaches the claimed power budget and decay value. *See* Ex. 1029 ¶¶ 102–105. We credit his testimony walking through these passages of Finkelstein and explaining in greater detail how they teach the limitations of claim 5. *See id.* Petitioner’s unchallenged assertions are persuasive. We agree with Petitioner that it would been obvious to incorporate these teachings of Finkelstein into Conroy’s budget system in order to take into account the way that past power allocations affect what is available for present power allocations. Pet. 81; Ex. 1005 ¶ 27 (criticizing “power-based management schemes [that] miss the temporal aspect of power management” and proposing a system that “takes temporal aspects into account”); *KSR*, 550 U.S. at 417.

Claim 7 requires “the first logic [] to dynamically allocate substantially all of the power budget to the first domain for a first workload, and . . . to the second domain for a second workload.” Petitioner asserts that

Conroy teaches scenarios where substantially all of the workload will first be on the CPU, and then substantially all of the workload will be on the GPU, and allocating the budgets accordingly. Pet. 63–64, 81–82. For example, Conroy teaches that some applications “present an alternating high workload to the CPU and to the GPU that results in an alternating asymmetric load profile of the system.” Ex. 1006 ¶ 196 (quoted at Pet. 64). Petitioner’s unchallenged assertions are persuasive. We agree that Conroy teaches alternating between giving substantially all of the power allocation to the CPU and GPU. *Id.*

c) Conclusion for Conroy-Finkelstein (Claims 1–5, 7)

As explained above, Petitioner has shown where each limitation of independent claim 1 is found in Conroy and Finkelstein, and provides reasons with rational underpinnings for this combination. Petitioner has made a similarly persuasive showing for claims 2–5 and 7, which are unchallenged. We determine that Petitioner has established, by the preponderance of the evidence, that claims 1–5 and 7 are unpatentable because they would have been obvious in view of Conroy and Finkelstein.

2. Conroy-Finkelstein Ground — Claims 13–15, 17, 18

Petitioner’s Conroy-Finkelstein ground for claims 13–15, 17, and 18 refers back to, and relies on, its earlier Conroy-alone ground for these claims. Pet. 82. The parties’ positions are effectively the same as for the Conroy-alone ground. PO Resp. 61; Pet. Reply 17; Sur-reply 18. Accordingly, we reach the same conclusion here as we did there, that Petitioner has established the unpatentability of claim 13, but not claims 14, 15, 17, or 18.

*H. Asserted Obviousness Over Finkelstein (Claims 1–5 and 7)
and
Finkelstein and Conroy (Claim 7)*

We have already determined that Petitioner has shown that claims 1–5 and 7 are unpatentable under Conroy-Finkelstein. Thus, we determine that we need not rule on whether those same claims are unpatentable under Finkelstein alone, or Finkelstein and Conroy.

III. CONCLUSION

For the reasons given above, we determine that Petitioner has established by a preponderance of the evidence that claims 1–5, 7, and 13 are unpatentable, but has not established by a preponderance of the evidence that any of claims 14–18 are unpatentable.

The following table summarizes the outcome of this proceeding:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–5, 7	103	Finkelstein ⁴		
7	103	Finkelstein, Conroy ⁵		
13–15, 17, 18	103	Nussbaum		13–15, 17, 18
16	103	Nussbaum, Bose		16
13–15, 17, 18	103	Conroy	13	14, 15, 17, 18
16	103	Conroy, Bose		16
1–5, 7, 13– 15, 17, 18	103	Conroy, Finkelstein	1–5, 7, 13	14, 15, 17, 18
Overall Outcome			1–5, 7, 13	14–18

IV. ORDER⁶

In consideration of the foregoing, it is hereby

ORDERED that the record shows that Petitioner has *not* established the unpatentability of claims 14–18 over Nussbaum, Conroy, or the combinations of Nussbaum and Bose or Conroy and Finkelstein;

FURTHER ORDERED that the record shows that Petitioner has established the unpatentability of claims 1–5 and 7 over the combination of

⁴ As explained above, we do not reach the Finkelstein-alone ground because we have already found claims 1–5 and 7 unpatentable over the Conroy-Finkelstein ground.

⁵ As explained above, we do not reach the Finkelstein-Conroy ground because we have already found claim 7 unpatentable over the Conroy-Finkelstein ground.

⁶ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding after the issuance of this Final Written Decision, we draw Patent Owner's attention to the April 2019

Conroy and Finkelstein, and the unpatentability of claim 13 over Conroy;
and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. §§ 42.8(a)(3), (b)(2).

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