

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,

Petitioner,

v.

DAEDALUS PRIME LLC,

Patent Owner.

Case No.: IPR2023-01343

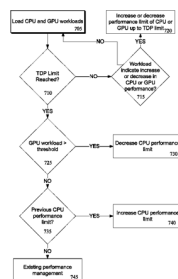
U.S. Patent No. 8,898,494

Patent Owner's Demonstrative Exhibits

MB USA v. Daedalus Prime IPR2023-01343
Patent Owner's Demonstrative Exhibits -- Not Evidence
Daedalus Ex. 2003

'494 Patent

(12) United States Patent Schluessler et al.	(10) Patent No.: US 8,898,494 B2 (45) Date of Patent: *Nov. 25, 2014
(54) POWER BUDGETING BETWEEN A PROCESSING CORE, A GRAPHICS CORE, AND A BUS ON AN INTEGRATED CIRCUIT WHEN A LIMIT IS REACHED	USPC 713/300, 320 See application file for complete search history.
(75) Inventors: Travis T. Schluessler , Hillsboro, OR (US); Russell J. Fenger , Beaverton, OR (US)	(56) References Cited U.S. PATENT DOCUMENTS 5,758,133 A * 5/1998 Every 713/501 7,558,966 B2 7/2009 Durham et al. 7,692,457 B2 4/2010 To et al. 7,818,596 B2 10/2010 Fenger et al. 7,917,789 B2 3/2011 Fenger et al. 8,185,215 B2 * 5/2012 Burchard et al. 700/22 8,281,170 B1 * 10/2012 Donovan 713/322 2004/0121797 A1 * 6/2004 Gupta 455/50.1
(73) Assignee: Intel Corporation , Santa Clara, CA (US)	(Continued)
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 108 days. This patent is subject to a terminal disclaimer.	OTHER PUBLICATIONS Schluessler et al., "Limiting CPU Power Consumption for Efficient Computation of 3D Workloads", IEEE International Conference on Energy Aware Computing, IEEE, Dec. 3-5, 2012, Guozelyurt, Cyprus.
(21) Appl. No.: 13/398,641	Primary Examiner — Thomas Lee Assistant Examiner — Danny Chan
(22) Filed: Feb. 16, 2012	(74) Attorney, Agent, or Firm — Trop, Pruner & Hu, P.C.
(65) Prior Publication Data US 2013/0159741 A1 Jun. 20, 2013	(57) ABSTRACT An apparatus, method and system is described herein for efficiently balancing performance and power between processing elements based on measured workloads. If a workload of a processing element indicates that it is a bottleneck, then its performance may be increased. However, if a platform or integrated circuit including the processing element is already operating at a power or thermal limit, the increase in performance is counterbalanced by a reduction or cap in another processing elements performance to maintain compliance with the power or thermal limit. As a result, bottlenecks are identified and alleviated by balancing power allocation, even when multiple processing elements are operating at a power or thermal limit.
Related U.S. Application Data (63) Continuation-in-part of application No. 13/327,670, filed on Dec. 15, 2011. (51) Int. Cl. <i>G06F 1/32</i> (2006.01) <i>G06F 9/50</i> (2006.01) (52) U.S. Cl. <i>CPC</i> <i>G06F 1/3203</i> (2013.01); <i>G06F 9/50</i> (2013.01); <i>G06F 9/5094</i> (2013.01) USPC 713/320 ; 713/300 (58) Field of Classification Search CPC <i>G06F 1/08</i> ; <i>G06F 1/3203</i> ; <i>G06F 1/206</i> ; <i>G06F 9/50</i> ; <i>G06F 9/5094</i>	18 Claims, 10 Drawing Sheets



The '494 patent proposes improved power management techniques in integrated circuits, such as computer processors, by balancing power allocation between processing cores and other elements, including other processing elements and communication buses.

In an integrated circuit, power is allocated between processing components, such as a communication bus and a processor core, based on a power limit and a workload threshold comparison. A component's activity may be taken as being indicative of its workload:

Determining a workload includes any known method for determining activity of hardware, a workload of software, a number of instructions executed or to execute, or any other metric for determining use of a processing element. As one example, a workload for core 505 includes an amount time core 505 is active during a period of time. Activity may be determined as when core 505 is in an active performance state versus a sleep or low power state or a number of cycles executing or performing operations.

Ex. 1001 at 9:47-57.
POR at 5-6.

'494 Patent

In the '494 patent, power allocation is tuned between various components:

In one embodiment, power control module 160, which may include hardware, firmware, software, or a combination thereof, is able to balance and allocate power/frequency between devices of IC 100 to achieve maximum performance; even when IC 100 is under a power limit. Additionally, such allocation, in one scenario is based on actual workload of devices, instead of assumptions of workload or power consumption. For example, a power limit (either a maximum power limit or a reduced limit during power saving modes) is provided for IC 100. Previously, a maximum current (and as a corollary frequency) was reduced for all processing elements of IC 100 to meet the power limit. Instead, in this scenario, a device that is determined to be a bottleneck for performance, such as throughput performance as viewed from the perspective of an application, is allocated more current/frequency, while the other competing device is capped/limited to ensure the power limit is still met. In other words, a dynamic balance is continuously [struck] between devices to ensure the device that needs more resources for better overall performance is allocated such extra resources, while other devices are 'balanced' (reduced in performance) to meet a given power limit.

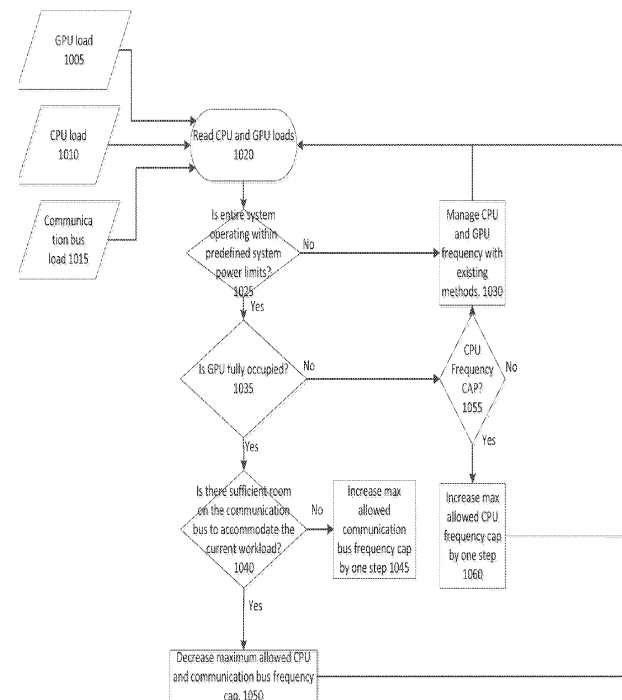


FIG. 10

Ex. 1001 at 7:40-61, Fig. 10.
POR at 7-8, 10.

'494 Claim Construction

1. A processor comprising:
 - an integrated circuit including:
 - a first core;
 - a cache memory;
 - a communication bus coupled to the first core, the communication bus to connect the first core and the cache memory;
 - a core workload monitor configured to determine a core workload for the first core;
 - a bus workload monitor configured to determine a bus workload for the communication bus; and
 - balancing control adapted to receive the bus workload from the bus workload monitor and to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and a comparison between the bus workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit, wherein a power consumption of one of the first core and the communication bus is to be reduced, the power consumption reduction to be limited to maintain operation of the one of the first core and the communication bus above a low limit.

Workload

A person of ordinary skill in the art would understand that in the '494 patent, the term “workload” means “an amount of activity over a quantum or period of time.”

3	Q	Is that how a person of ordinary skill in
4		the art would understand the term "workload," that
5		it's referring to an amount of activity over a
6		period of time?
7	A	Yeah. There's lots of definitions for
8		"workload." And specifically, I think what '494 is
9		trying to do here is to define how they measure it
10		and how they quantify it.

'494 Challenges

Claims Challenged	35 U.S.C. §	References
1	102/103	Bose
3, 14-15	103	Bose, White, Simeral
2	103	Bose, Anderson
13	103	Bose, Anderson, Naffziger
4, 7	103	White
5, 6	103	White, Anderson
17, 18	103	White, Anderson, Naffziger
1, 3, 14, 15	103	White, Simeral
2	103	White, Simeral, Anderson
13	103	White, Simeral, Anderson, Naffziger

Bose

(12) **United States Patent**
Bose et al.

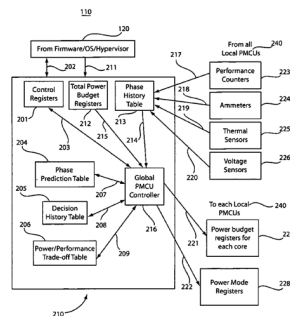
(10) **Patent No.:** US 7,421,601 B2
(45) **Date of Patent:** Sep. 2, 2008

(54) **METHOD AND SYSTEM FOR CONTROLLING POWER IN A CHIP THROUGH A POWER-PERFORMANCE MONITOR AND CONTROL UNIT**
(75) Inventors: **Pradip Bose**, Yorktown Heights, NY (US); **Alper Buyuktosunoglu**, White Plains, NY (US); **Chen-Yong Cher**, Port Chester, NY (US); **Prabhakar N. Kudva**, New York, NY (US)
(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 414 days.
(21) Appl. No.: 11/357,612
(22) Filed: Feb. 17, 2006
(65) **Prior Publication Data**
US 2007/0198863 A1 Aug. 23, 2007
(51) **Int. Cl.**
G06F 1/26 (2006.01)
G06F 1/32 (2006.01)
(52) **U.S. Cl.** 713/320; 713/300
(58) **Field of Classification Search** 713/320
See application file for complete search history.
(56) **References Cited**
U.S. PATENT DOCUMENTS
5,903,717 A 5/1999 Wardrop
5,923,830 A 7/1999 Fuchs et al.

OTHER PUBLICATIONS
T. Simunic et al., "Managing Power Consumption in Networks on Chips", Proceedings of the 2002 Design Automation and Test in Europe Conf. and Exhibition, 2002, 7 pages
J. Srinivasan et al., "Predictive Dynamic Thermal Management for Multimedia Applications", ICS'03, Jun. 23-26, 2003; San Francisco, CA; pp. 109-120.
(Continued)
Primary Examiner—Thuan N Du
(74) **Attorney, Agent, or Firm**—Keusey, Tutunjian & Bitetto, P.C.; Mark Wardas

(57) **ABSTRACT**
A system and method for controlling power and performance in a microprocessor system includes a monitoring and control system integrated into a microprocessor system. The monitoring and control system includes a hierarchical architecture having a plurality of layers. Each layer in the hierarchical architecture is responsive to commands from a higher level, and the commands provide instructions on operations and power distribution, such that the higher levels provide modes of operation and budgets to lower levels and the lower levels provide feedback to the higher levels to control and manage power usage in the microprocessor system both globally and locally.

1 Claim, 7 Drawing Sheets



Bose describes “systems and methods for a power/performance monitoring and control unit.”

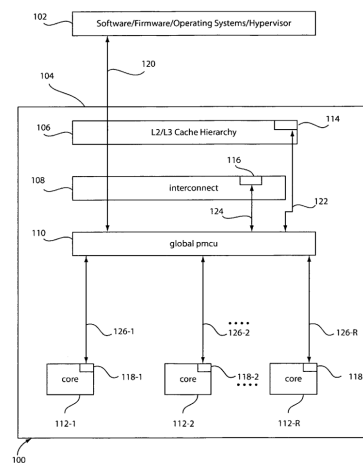


FIG. 1

The system includes a global power-performance monitor and control unit (PMCU) 110, that “chooses appropriate power optimizations” for various core elements, an L2/L3 cache hierarchy, and an interconnect. The global PMCU receives reports of power usage and temperature usage from local PMCUs associated with these elements.

Power optimizations are “packaged” into different power modes according to power vs. performance tradeoffs.

Ex. 1005 at 1:16-22, 6:67 – 7:13, Fig. 1.
POR at 19-20.

Bose

The global PMCU “operates in a looping manner.”

Following initialization, the global PMCU checks whether the actual total power being used by the system is at or below the total system power budget (303). If so, all cores are run in the highest power mode and the power budget is divided equally among the cores (312).

Otherwise, if the actual power being used exceeds the system power budget, a power mode is selected given consideration to the total system power budget, real time statistics reported by the local PMCUs, and power vs. performance tradeoffs of the various power modes (311).

A lower power mode is assigned to a core if its assigned portion of the power budget is insufficient, and a higher power mode is assigned to a core if that core is exceeding its assigned portion of the power budget such that “the sum of power usage for all components fits into the overall power budget.”

The local PMCUs operate with the newly assigned power modes/budgets and continue to report information back to the global PMCU.

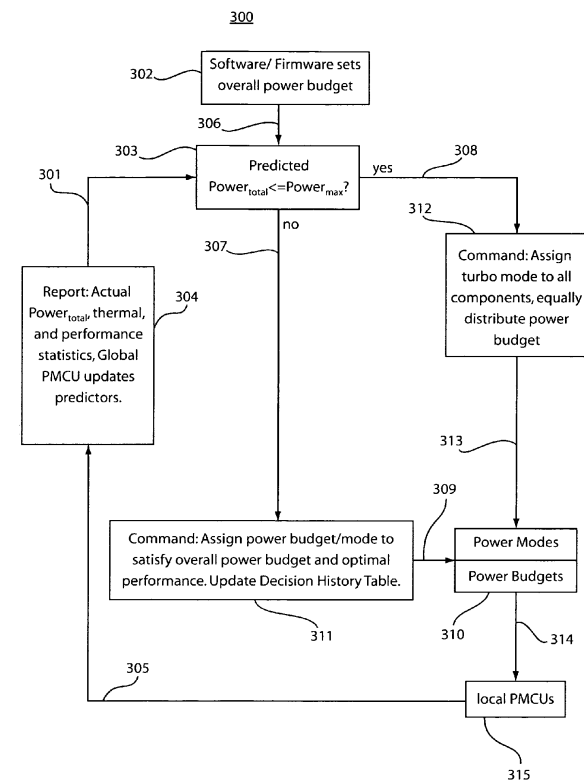
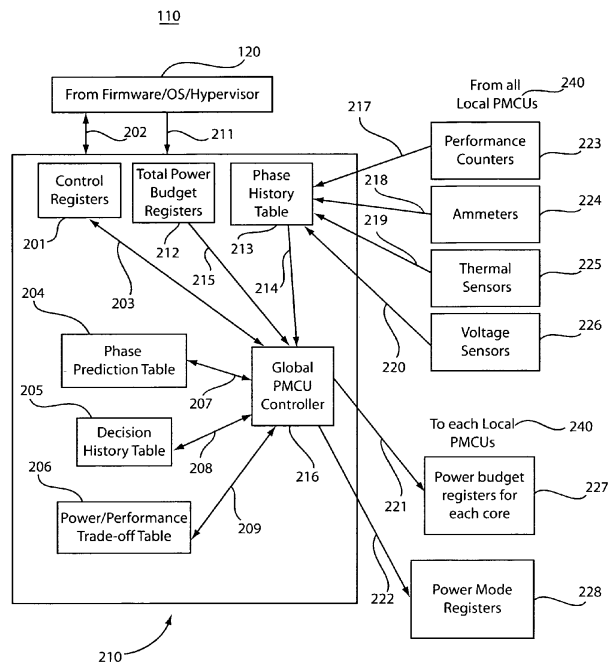


FIG. 3

Ex. 1005 at 8:62 – 9:43, Fig. 3.
POR at 21-22.

Bose

The global PMCU stores information used in making power budget allocation decisions in a collection of registers and tables.



Connections from sensors associated with the local PMCUs 240 supply performance information (power, temperature, voltage, etc.) for a phase history table, 213, while phase prediction information is stored in a phase prediction table, 204.

Information concerning the overall power budget is stored in total power budget register 212.

A power-performance tradeoff table 206 “includes the predicted power and performance for each power mode” as “a structure (with update semantics and control) maintained to record the information needed to perform accurate prediction of the changes and duration of distinct workload phases, characterized by power and performance data as recorded within the [phase history table].”

Previous decision information is stored in a decision history table, 205.

Ex. 1005 at 7:41 – 8:51, 12:49-58, Fig. 2.
POR at 22-23.

Failings of Bose

1. A processor comprising:
an integrated circuit including:
a first core;
a cache memory;
a communication bus coupled to the first core, the communication bus to connect the first core and the cache memory;
a core workload monitor configured to determine a core workload for the first core;
a bus workload monitor configured to determine a bus workload for the communication bus; and
balancing control adapted to receive the bus workload from the bus workload monitor and to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and a comparison between the bus workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit, wherein a power consumption of one of the first core and the communication bus is to be reduced, the power consumption reduction to be limited to maintain operation of the one of the first core and the communication bus above a low limit.

Bose does not teach or suggest a “balancing control adapted to receive the bus workload from the bus workload monitor and to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and a comparison between the bus workload and a bus workload threshold.”

Failings of Bose

Petition Argument

“Bose discloses dynamic tuning of power allocation based on a comparison between bus workload and bus workload threshold [because a] POSITA would have understood that in Bose, selecting or adjusting power mode for a component entails comparing a workload threshold, such as predicted power and performance associated with each power mode with real time statistics, such as the monitored workload of a component.”

The “predicted power and performance represents a workload threshold for a given component working in the associated power mode.”

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Mercedes-Benz USA, LLC,
Petitioner,

v.

Daedalus Prime LLC,
Patent Owner.

Case IPR2023-01343
Patent 8,898,494

**PETITION FOR *INTER PARTES* REVIEW OF
CLAIMS 8, 10-18, AND 24-47 OF U.S. PATENT NO. 8,898,494
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §42.100 *et seq.***

Failings of Bose

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,

Petitioner,

v.

DAEDALUS PRIME LLC,

Patent Owner.

Case No.: IPR2023-01343

U.S. Patent No. 8,898,494

DECLARATION OF MICHAEL C. BROGIOLI, PH.D.
IN SUPPORT OF PATENT OWNER'S RESPONSE

“The global PMCU controller 216 updates the Power/Performance Trade-off Table 206 through connection 209, after considering information from the Phase Prediction Table 204 and the Decision History Table 205.”

Bose at 8:39-43.

Bose’s power-performance tradeoff table is dynamically updated over time. Dynamically changing data of this kind, which is apparently derived algorithmically from historical information and current data samples, does not represent a threshold, a singular value against which a measured quantity is evaluated, and a person of ordinary skill in the art would appreciate as much.

Bose indicates, “The [phase prediction table] includes a structure (with update semantics *and control*),” Bose at 12:54-55, and a POSITA would appreciate that if a structure includes semantics and control, that is likely something pertaining to the algorithm itself to be used rather than data (like a threshold) to use in variables.

Brogioli at ¶¶ 44-49.

Ex. 1005 at 8:39-43.
Ex. 2001 at ¶¶ 44-49.
POR at 25.

Failings of Bose

Petition Argument

“A POSITA would have understood global PMCU compares a workload threshold as exemplified by the predicted power and performance of each power mode and the monitored workload to select and adjust the power mode of a component.”

Pet. at 26.
Ex. 1005 at 9:14-24; 12-37– 13:4, 2:62-65
POR at 27-28.

Flaws

A POSITA would not come to this “understanding.”

Bose: Power modes are assigned with consideration of power vs. performance tradeoffs associated with each mode. The “information needed to perform accurate prediction of the changes and duration of distinct workload phases, characterized by power and performance data,” is maintained in a phase prediction table, and a power mode transmitted to a monitored resource will be “acted upon to place that resource into a specified configuration, such that its power level is decreased or increased (with a corresponding decrease or increase in net performance).”

So, no *comparison* of bus workload to a bus workload threshold is needed because direct information concerning actual power level decreases or increases for different power modes is available from the power-performance tradeoff table and the global PMCU can directly determine whether a power level associated with a prospective power mode will “fit” within a total power budget.

Failings of Bose

Flaws

The petition fails to account for differences between Bose and the claimed invention and fails to explain any modifications of Bose or why they would be done.

Petition Argument

Claim 1 is obvious in view of Bose.

1. Bose is architected in a hierarchical manner, with each layer of the hierarchy having its own control.
2. The architecture of the various monitors within Bose vary, and overall are heterogeneous in nature. Some monitors can communicate upstream and downstream, while others can only communicate downstream.
3. The phase prediction table is not a threshold, and a POSITA would appreciate that the values in this table (as well as the others described by Bose) would be consumed via Bose's distributed and heterogeneous algorithm to make power management decisions.
4. The information in the tables includes update semantics and control, and a POSITA would appreciate they are algorithmic information, not thresholds.
5. By providing a power-performance tradeoff table with information concerning actual power level decreases or increases for different power modes, no *comparison* with a threshold is needed.

Pet. at 15-27.
Ex. 1005 at 2:25-35.
POR at 29-32.

White

(12) **United States Patent**
White et al.

(10) **Patent No.:** US 7,263,457 B2
(45) **Date of Patent:** Aug. 28, 2007

(54) **SYSTEM AND METHOD FOR OPERATING COMPONENTS OF AN INTEGRATED CIRCUIT AT INDEPENDENT FREQUENCIES AND/OR VOLTAGES**

(75) **Inventors:** Scott A. White, Austin, TX (US);
William A. Hughes, San Jose, CA (US); Philip E. Madrid, Round Rock, TX (US)

(73) **Assignee:** Advanced Micro Devices, Inc., Sunnyvale, CA (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** 11/925,054

(22) **Filed:** Jan. 3, 2006

(65) **Prior Publication Data**
US 2007/0156370 A1 Jul. 5, 2007

(51) **Int. Cl.**
G01K 1/08 (2006.01)

(52) **U.S. CL.** 702/132

(58) **Field of Classification Search** 702/132
See application file for complete search history.

(56) **References Cited**
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6,901,303 B2 * 5/2005 Larson et al. 700/108
7,228,242 B2 * 6/2007 Read et al. 702/57
2003/0115013 A1 * 6/2003 Dendinger 702/132
2006/0161375 A1 * 7/2006 Dabirian et al. 702/132
* cited by examiner

(74) **Attorney, Agent, or Firm:** Robert C. Kowert; Meyerson, Hood, Kiwin, Kowert & Goetzl, P.C.

(57) **ABSTRACT**
Multiple logic cores of integrated circuits and processors may be configured to operate at frequencies and voltages independently of each other. Additionally, other components, such as a common bridge configured to interface with the logic cores, may operate at a voltage and frequency independent of the voltage and frequency at which the logic cores are operating. The operating frequency and/or voltage of a logic core may be independently adjusted for various reasons, including power management and temperature control. Logic circuitry at an interface between the controller and the logic cores may translate logic signals from one voltage and/or frequency to another to enable communication between the bridge and the logic core when the two are operating at different voltages and/or frequencies.

32 Claims, 9 Drawing Sheets

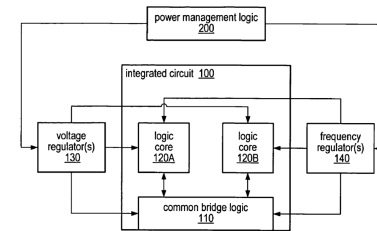
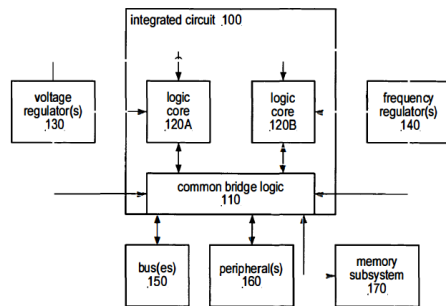


FIG. 2A

The operating voltage and/or operating frequency of the various logic cores of integrated circuit 100 may be controlled by power management logic 200. In this way, overall power consumption for the integrated circuit may be adjusted.

Ex. 1006 2:15-18, 8:61-65, Fig. 2A.
POR at 35-36.

White

When a need to change an operating characteristic, e.g., frequency (FIG. 4) or voltage (FIG. 5), of a logic core is detected (400, 500), power management logic 200 determines a new operating voltage/frequency for the core (410, 510). New frequencies may be determined based on a “standard algorithm” or “from a look-up table.” New voltages may be determined via a voltage determining algorithm based upon current operating conditions for the system or a fixed table of operating voltages.

Assuming the new frequency is compatible with the operating voltage of the core (420), or after making adjustments therefor (430, 440), the power management logic sets the new operating frequency for the core (450 and then adjusts the operating conditions for the common bridge logic to be compatible with the new operating frequency (460).

In the case of a new operating voltage, the power management logic sets the new voltage (520), determines whether the operating frequency of the core is compatible with the new voltage (530), and adjusts the operating frequency as necessary (540, 550).

Thereafter, the power management logic adjusts the operating conditions for the common bridge logic to be compatible with the new operating voltage and/or frequency of the core (560).

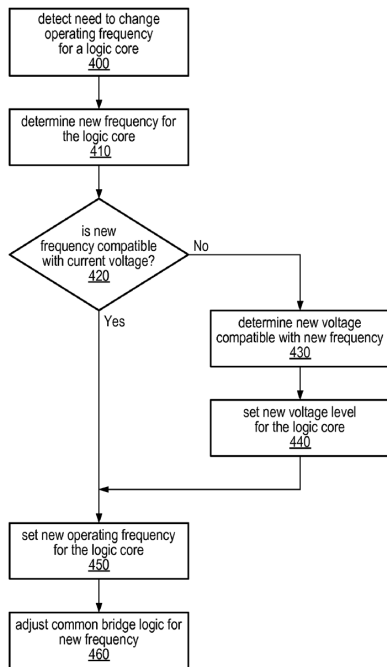


FIG. 4

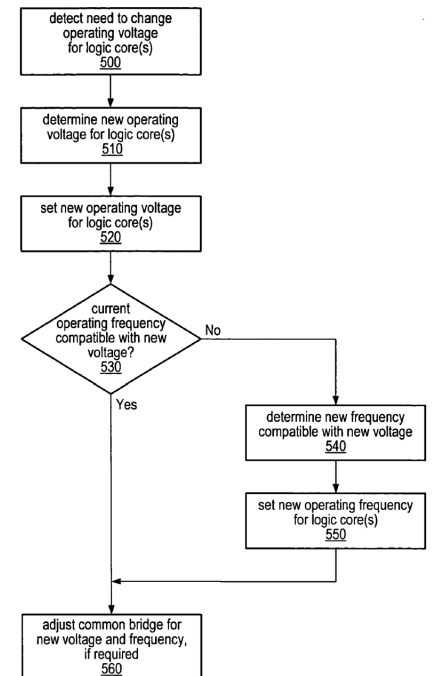
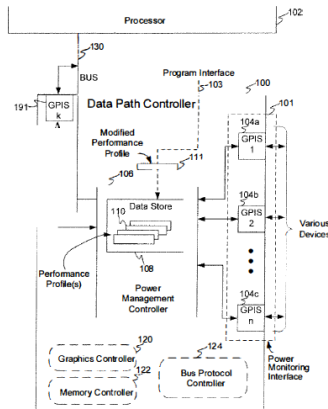


FIG. 5

Ex. 1006 at 15:42 – 20:57, Figs. 4, 5.
POR at 36-38.

Simeral

- (19) **United States**
 (12) **Patent Application Publication**
 Simeral et al.
- (10) Pub. No.: **US 2009/0150689 A1**
 (43) Pub. Date: **Jun. 11, 2009**
- (54) **DATA PATH CONTROLLER WITH INTEGRATED POWER MANAGEMENT TO MANAGE POWER CONSUMPTION OF A COMPUTING DEVICE AND ITS COMPONENTS**
- Related U.S. Application Data**
 (63) Continuation of application No. 11/305,816, filed on Dec. 16, 2005, now Pat. No. 7,487,371.
- Publication Classification**
 (51) Int. Cl. **G06F 1/32** (2006.01)
 (52) U.S. Cl. **713/300**
 (57) **ABSTRACT**
- A data path controller, a computer device, an apparatus and a method are disclosed for integrating power management functions into a data path controller to manage power consumed by processors and peripheral devices. By embedding power management within the data path controller, the data path controller can advantageously modify its criteria in-situ so that it can adapt its power management actions in response to changes in processors and peripheral devices. In addition, the data path controller includes a power-managing interface that provides power-monitoring ports for monitoring and/or quantifying power consumption of various components. In one embodiment, the data path controller includes a power-monitoring interface for selectively monitoring power of a component. It also includes a controller for adjusting operational characteristics of the component to comply with a performance profile, which generally specifies permissible power consumption levels for the component.
- (76) Inventors: **Brad W. Simeral**, San Francisco, CA (US); **David C. Reed**, Saratoga, CA (US); **Dmitry Vyshetsky**, Cupertino, CA (US); **Roman Surgutichik**, Santa Clara, CA (US); **Robert William Chapman**, Mountain View, CA (US); **Joshua Titus**, Sunnyvale, CA (US); **Anand Srinivasan**, San Jose, CA (US); **Hari U. Krishnan**, Newark, CA (US)
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 Washington, DC 20001 (US)
- (21) Appl. No.: **12/342,865**
 (22) Filed: **Dec. 23, 2008**



Simeral describes “a method for integrating power management functions into a data path controller to manage power consumption of processors and peripheral devices.”

The “data path controller,” “resides in a computing device” and “forms data paths over which data are exchanged among components of a computing device.”

These “components” might be a processor and devices with which a processor communicates, e.g., peripherals, graphics processors, hard drive controllers, display drivers, and “regulatory devices” such as voltage regulators or frequency/clock generators.

The data path controller can be “reactive,” taking action to decrease power consumption as a result of low or negligible activity levels by modifying operational characteristics of the components to conserve power while providing sufficient resources to support a specific workload, or “proactive,” taking action to decrease power consumption by decreasing activities levels of a component through modification of operational characteristics of the component as a corrective action to bring one or more noncompliant activity levels back into compliance.

Simeral

“[D]ata path controller 100 can manage power for a computing device by first monitoring the activity level of the bus (e.g., the data transfer rate of the bus), and then disabling (e.g., shutting down) components that have very low (i.e., negligible) activity levels to save power. So if the data rate is below some threshold (i.e., low amounts of data are passing over the bus), then data path controller 100 can either decrease (i.e., “throttle down”) the bus width or shut down one or more bus controllers, thereby conserving power that would otherwise be expended by maintaining a higher bandwidth.”

“[P]ower management controller 106 monitors the activity levels of the component, such as the data being exchanged between a component and data path controller 100 . . . compares that monitored activity level to a threshold activity level set forth in [a] performance profile, [and] if the monitored activity level falls out of compliance, then power management controller 106 initiates corrective action . . . include[ing] modifying the behavior of the noncompliant component so that it complies with its threshold activity level [or] recalibrate[ing] activity levels of other less essential components to compensate for the increased activity level of the noncompliant component.”

A performance profile can include operational characteristics such as voltages, frequencies, data throughput on buses, etc.

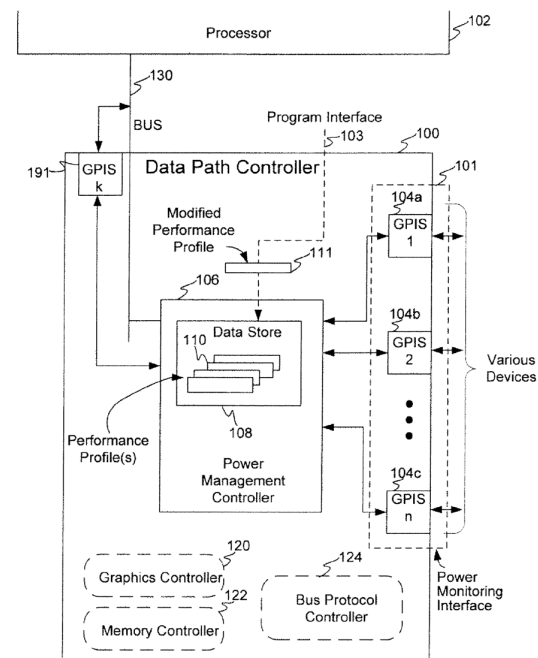


FIG. 1A

Ex. 1008 at [0021], [0024], [0026], Fig. 1A.
POR at 40-52.

Failings of White-Simeral

Petition Argument

In White-Simeral, White discloses a core workload monitor configured to determine a core workload for the first core, as recited in claim 1.

“A POSITA would have understood White monitoring the operating voltages and frequencies of the logic core 120A and common bridge logic 110 is monitoring the workload of those components.”

Pet. at 72
Ex. 1001 9:50-57
POR at 42-45.

Flaws

A POSITA would not conflate White’s monitoring of operating characteristics (voltage or frequency) with monitoring of workload, as required by claim 1.

1. The ’494 patent makes clear that one is not a substitute for the other because performance metrics such as frequency can be altered independently of workload. Hence, operating characteristics need not reflect the actual workload of a core.

2. Monitoring core workload involves “determining activity of hardware, a workload of software, a number of instructions executed or to execute, or any other metric for determining use of a processing element. . . . Activity may be determined as when core 505 is in an active performance state versus a sleep or low power state or a number of cycles executing or performing operations.”

3. A POSITA would understand that White’s power management logic controls adjustments to a core’s operating characteristics by monitoring the core’s current power consumption. When adjusting the operating voltage or frequency of a core, the power management logic uses a table of compatible or desirable voltage-frequency pairs to ensure desired operating characteristics are feasible.

Failings of White vis-à-vis Claim 4

Petition Argument

Claim 4 is obvious in view of White.

“A POSITA would have understood that operating voltage/frequency reflect the activity and use, or workload, of a component.”

Pet. at 7, 53.
Ex. 1008 at 10:43-46
Ex. 2001 at ¶¶ 67-72.
POR at 46-49.

Flaws

Independent claim 4 recites “*receiving* a bus workload for a communication bus and a first processing element workload for a first processing element based on an integrated circuit reaching a limit.”

White’s focus on operating voltage and operating frequencies is an indication that White’s power management logic makes decisions regarding future operating characteristics of a core based on present operating characteristics.

Monitoring operating characteristics, as is done by White’s power management logic, is not the same as monitoring a processing element’s workload using a workload monitor.

Further, in White the power management logic receives current operating voltages and operating frequencies, *not* workload – i.e., *not* activity levels.

Failings of White vis-à-vis Claim 4

Flaws

White does not teach or suggest this requirement.

In another embodiment, a system including a multi-core processor may be operating from battery power and power management logic 200 may be configured to detect when the system is operating on battery power and adjust the operating frequency of one or more of the logic cores. Additionally, power management logic 200 may be configured to detect when the system transitions from battery power to wall power and adjust the operating frequency of one or more logic cores to a higher frequency to take advantage of the fact that the system is no longer on battery power.

There is no mention of a battery power limit and, if anything, the power management logic detects when the system is operating on battery power, irrespective of any “limit.”

Petition Argument

Claim 4 is obvious in view of White.

White discloses the power management unit receiving operating voltages/frequencies based on an integrated circuit reaching a limit, such as a battery power limit.

Pet. at 54.

Pet. at 54.
Ex. 1008 at 15:54-64.
POR at 50.

Failings of White vis-à-vis Claim 4

Flaws

The petition confuses the power management logic with different “temperature control logic.”

Petition Argument

Claim 4 is obvious in view of White.

“White discloses that power management logic 200 receives workload information based on the integrated circuit reaching a thermal design power limit, such as ‘a predetermined maximum operating temperature.’”

Pet. at 55.
Ex. 1008 at 11:61-64, 12:38-58, Fig. 2B.
POR at 51.

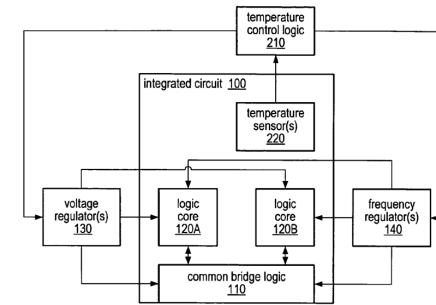


FIG. 2B

Operating characteristics (voltage / frequency) for the logic cores may be controlled by temperature control logic 210. The temperature control logic, not the power management logic, is configured to read current operating temperatures and request changes in operating characteristics of the cores based on readings from temperature sensors.

The petition mistakenly attributes such actions to the power management logic

Conclusion

The Petition has failed to prove the unpatentability of any of the challenged claims.