



Mercedes's Hearing Demonstratives for *Mercedes vs. Daedalus*

IPR2023-01343

U.S. Patent No. 8,898,494

Mercedes EX1011
Mercedes-Benz USA, LLC
v. Daedalus Prime LLC

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

IPR2023-01343

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Introduction

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Overview of the '494 Patent




 US898494B2

(12) **United States Patent**
 Schlusser et al.

(16) **Patent No.:** US 8,898,494 B2
 (45) **Date of Patent:** *Nov. 25, 2014

(54) **POWER BUDGETING BETWEEN A PROCESSING CORE, A GRAPHICS CORE, AND A BUS ON AN INTEGRATED CIRCUIT WHEN A LIMIT IS REACHED**

(75) **Inventors:** Travis T. Schlusser, Hillsboro, OR (US); Russell J. Fenger, Beaverton, OR (US)

(73) **Assignee:** Intel Corporation, Santa Clara, CA (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 108 days.
 This patent is subject to a terminal disclaimer.

(21) **Appl. No.:** 13/598,641

(22) **Filed:** Feb. 16, 2012

(65) **Prior Publication Data**
 US 2013/0159741 A1 Jun. 20, 2013

Related U.S. Application Data

(66) Continuation-in-part of application No. 13/527,670, filed on Dec. 15, 2011.

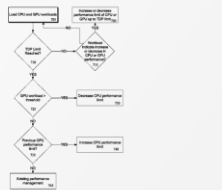
(51) **Int. Cl.** (2006.01)
 G06F 1/30 (2006.01)

(52) **U.S. Cl.** (2006.01)
 G06F 1/30 (2006.01)

USPC G06F 1/30 (2006.01)
 CPC G06F 1/30 (2006.01)

(57) **Field of Classification Search**
 CPC G06F 1/30 (2006.01); G06F 1/30 (2006.01); G06F 1/30 (2006.01)

18 Claims, 18 Drawing Sheets



- The '494 Patent discloses an apparatus, method, and system for balancing performance and power between components of an integrated circuit based on measured workloads.
- If the component is identified as a bottleneck, its performance may be increased.
- If the integrated circuit is already operating at a power or thermal limit, the increase in performance is counterbalanced by a reduction or cap in another component's performance.

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Overview of the '494 Patent



1. A processor comprising:
an integrated circuit including:
a first core;
a cache memory;
a communication bus coupled to the first core, the communication bus to connect the first core and the cache memory;
a core workload monitor configured to determine a core workload for the first core;
a bus workload monitor configured to determine a bus workload for the communication bus; and
balancing control adapted to receive the bus workload from the bus workload monitor and to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and a comparison between the bus workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit, wherein a power consumption of one of the first core and the communication bus is to be reduced, the power consumption reduction to be limited to maintain operation of the one of the first core and the communication bus above a low limit.

Claim 1 generally recites an integrated circuit including:

- A first core
- A cache memory
- A communication bus to connect the first core and cache memory
- A core workload monitor to determine a core workload for the first core
- A bus workload monitor to determine a bus workload for the communication bus
- Balancing control to tune the power allocation between the first core and the communication bus

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Overview of the '494 Patent



4. A non-transitory storage medium including code, when executed, to cause a machine to perform the energy efficiency operations of:

receiving a bus workload for a communication bus and a first processing element workload for a first processing element based on an integrated circuit reaching a limit, the integrated circuit including the communication bus and the first processing element, wherein the communication bus is to connect the first processing element with at least one other device of the integrated circuit;

determining if the first processing element workload indicates the first processing element is a performance bottleneck;

determining if the communication bus is able to accommodate the bus workload;

capping a bus frequency of at least the communication bus and a frequency of a second processing element in response to determining the first processing element workload indicates the first processing element is the performance bottleneck and determining the communication bus is able to accommodate the bus workload; and

increasing a previous cap on the bus frequency of at least the communication bus in response to determining the first processing element workload indicates the first processing element is the performance bottleneck and determining the communication bus is not able to accommodate the bus workload.

Claim 4 generally recites:

- Receiving a bus workload and a first processing element workload
- Determining if the processing element is a performance bottleneck
- Determining if the communication bus is able to accommodate the bus workload
- Capping a bus frequency of the communication bus and a second processing element
- Increasing a cap on the bus frequency of the communication bus

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Overview of the '494 Patent



- Fig. 9 depicts an integrated circuit that dynamically balances power between cores 910/905 and communication bus 950.
- GPU Cores 910 and CPU cores 905 are associated with GPU workload monitor 911 and CPU workload monitor 935, respectively, to monitor workload of the cores. Similarly, communication bus 950 is associated with bus workload monitor 951.
- Power is balanced among the components based on the workload measured by the workload monitors.

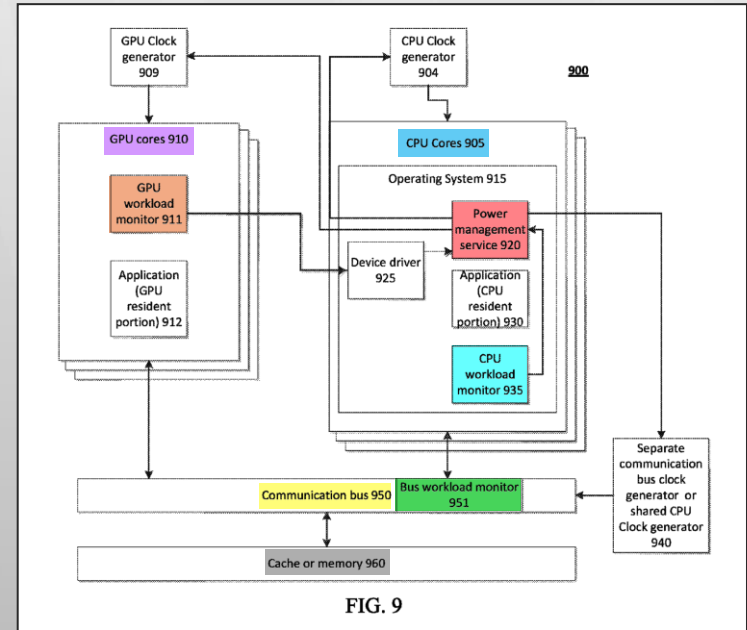


FIG. 9

'494 Patent at Fig. 9 (annotated)

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“Workload” in the '494 Patent



- The '494 Patent broadly describes determining a workload to include *any known method* for determining activity of hardware, or any other metric for determining use
- The '494 Patent further explains that there are a multitude of potential workload measurements, and the components to measure workload may also vary

Determining a workload includes any known method for determining activity of hardware, a workload of software, a number of instructions executed or to execute, or any other metric for determining use of a processing element. As one example, a workload for core **505** includes an amount time core **505** is active during a period of time. Activity may be determined as when core **505** is in an active performance state versus a sleep or low power state or a number of cycles executing or performing operations.

As a corollary to the multitude of potential workload measurements, the components to measure such workload may also vary. To further discussion of the potential components for workload measurement, it's assumed below that workload is measured as a number of active cycles over a period of time (i.e. a total number of cycles for measurement). As a first

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'494 Patent at 9:47-67

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Dispute 1 – Whether Bose discloses the “balancing control” limitation

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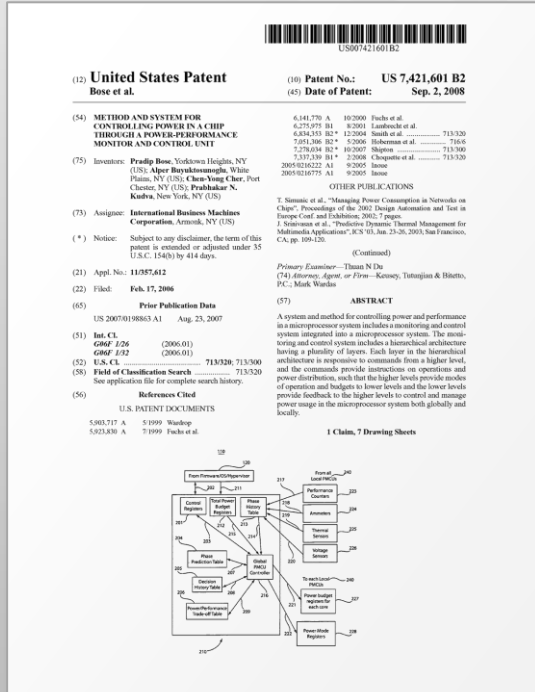
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Overview of Bose



- Bose discloses a system and method for controlling power and performance in a microprocessor system.
- Particularly, Bose discloses “a power/performance monitoring and control unit (PMCU),” which “can dynamically manage chip power between the components ... to meet the power limit with the expectation of increased system performance.” Bose at 4:30-32.
- “One objective of PMCU is to address the challenge of reducing power by exploiting the variability within a workload and between different workloads.” Bose at 4:30-32



Overview of Bose

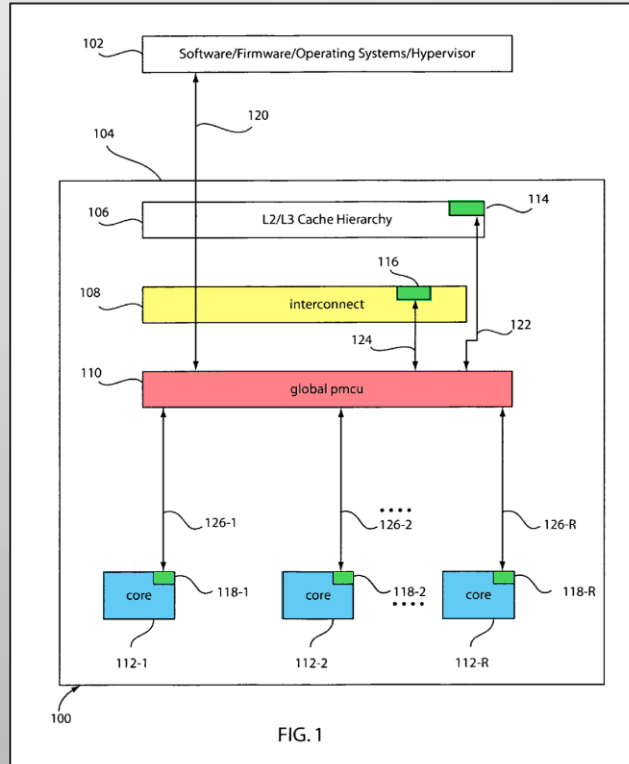


FIG. 1

Bose at Fig. 1 (annotated)

- Fig. 1 depicts a high-level overview of PMCU organization, which includes:
 - Processing cores 112-1, 112-2, and 112-R
 - Interconnect 116 (i.e., a communication bus)
 - L2/L3 Cache Hierarchy 106 (i.e., a cache memory)
 - Local PMCUs 118-1, 118-2, 118-R, 116, 114 that “monitor activities in each core 112-1, 112-2, 112-R, L2/L3 cache hierarchy 106 and interconnect 108”
Bose at 6:56-58
- Global PMCU 110 that dynamically adjusts power mode for each element based on various considerations.

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The “Balancing Control” Limitation



Claim 1 recites “balancing control adapted to receive the bus workload from the bus workload monitor and to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and a comparison between the bus workload and a bus workload threshold”

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Bose Discloses Monitoring “Workload”



- Bose discloses that the local PMCU monitor performance statistics, like instructions per cycle.
- The global PMCU stores the monitored performance statistics in the Phase History Table 213 and uses them in adjusting power mode.

The local PMCUs 114, 116, 118-1, 118-2, 118-R monitor activities in each core 112-1, 112-2, 112-R, L2/L3 cache hierarchy 106 and interconnect 108 and carry out power-reducing optimizations as commanded by the global PMCU 110. The local PMCUs 114, 116, 118-1, 118-2, 118-R monitor performance statistics such as cache miss rates, branch misprediction rates, instructions per cycle (IPCs), etc. It can

Bose at 6:56-62

Q. What about instructions per second, would that be a workload according to your definition?

...

A. So that may be something that falls under "workload" that I talk about in Paragraph 38.

Brogioli Depo. (EX1010) at 49:14-50:1

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Bose Discloses “Workload Threshold”



The predicted power and performance represents a workload threshold for a given component working in the associated “power mode.”

Wyatt Decl. (EX1003) at ¶53

Based on the information and the objective of the system 100, the global PMCU 110 chooses appropriate power optimizations for each core element 112-1, 112-2, 112-R, 106, and 108. For design simplicity, these optimizations can be packaged into different power modes based on their power-performance trade-off characteristics. A power mode may be defined to be higher if it is expected to consume more power and to achieve higher performance, and to be lower if it is expected to consume less power and to achieve lower performance, relative to other power modes.

Bose at 7:8-17

The Power/Performance Trade-off Table 206 includes the predicted power and performance for each power mode, where the global PMCU controller 216 reads through connection 209 to assist in calculating the power modes and power budgets for each core. The global PMCU controller

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Bose at 8:35-39

Bose Discloses “Comparison” of Workload to Workload Threshold



- Bose assigns power mode based on (1) “real time statistics” and (2) “power/performance trade-off of each mode.”
- The real time statistics stored in Power History Table 213 includes the monitored performance statistics, i.e., monitored workload.
- The “power performance trade-off of each mode” stored in Power/Performance Trade-off Table 206 is the predicted power and performance, i.e., workload threshold.
- By comparing monitored workload and workload threshold, the global PMCU determines whether it needs to assign a new power mode and adjusts accordingly.

From state **303**, if the actual total power is not below or equal to the total power budget, the loop transitions through edge **307** into state **311**, and the **state 311** assigns power budget and power mode with consideration of: the commands from OS **120** (stored, e.g., in Control Registers **201** and total power budget from the Total Power Budget Registers **212**, both depicted in FIG. 2), the real time statistics (stored e.g., in the Phase History Table **213** depicted in FIG. 2) and the power/performance trade-off of each mode for each thread in each core (stored, e.g., in the Power/Performance Trade-off Table **206**, depicted in FIG. 2).

With these considerations, the state **311** assigns a lower power mode for a core if the power budget assigned to the core is insufficient and increases to higher power modes if the cores are exceeding the power budget, such that the sum of power usage for all components fits into the overall power budget. Considerations for assigning power modes include

Bose at 9:14-30

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Bose Discloses “Workload Threshold”



Patent Owner argues:

The predicted power and performance does not represent workload threshold because it is “dynamically updated over time” and thus cannot be a threshold which has to be a singular or fixed value.

But:

- But Patent Owner’s assertion that the “workload threshold” must be a singular fixed value has no basis in the claims or the ’494 Specification.
- While the predicted power and performance may be dynamically updated, this in no way precludes it from being used as a threshold.

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Bose Discloses “Comparison” of Workload to Workload Threshold



Patent Owner also argues:

“Bose has no need for any comparison of workload to workload threshold because direct information concerning power levels is available from various tables.”

PO Sur-reply at 1

But:

- The global PMCU needs to determine when a higher or lower power mode is required, which is done via comparing the monitored power and performance level (“monitored workload”) to the predicted power and performance (“workload threshold”).

With these considerations, the state **311** assigns a lower power mode for a core if the power budget assigned to the core is insufficient and increases to higher power modes if the cores are exceeding the power budget, such that the sum of power usage for all components fits into the overall power budget. Considerations for assigning power modes include

Bose at 9:25-30

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Dispute 2 – Whether White discloses a “core workload monitor”

Claims 1, 2, 3, 13, 14, and 15

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White Overview



(12) **United States Patent**
White et al.

(10) **Patent No.:** US 7,263,457 B2
(45) **Date of Patent:** Aug. 28, 2007

(54) **SYSTEM AND METHOD FOR OPERATING COMPONENTS OF AN INTEGRATED CIRCUIT AT INDEPENDENT FREQUENCIES AND/OR VOLTAGES**

(75) **Inventor:** Scott A. White, Austin, TX (US);
William A. Hughes, San Jose, CA (US); Philip E. Madrid, Round Rock, TX (US)

(73) **Assignee:** Advanced Micro Devices, Inc., Sunnyvale, CA (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** 11/025,054

(22) **Filed:** Jan. 3, 2006

(65) **Prior Publication Data**
US 2007/015670 A1 Jul. 5, 2007

(51) **Int. Cl.**
G06F 1/08 (2006.01)

(52) **U.S. Cl.**
702/132

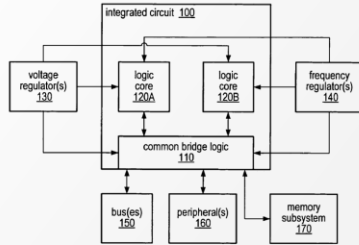
(58) **Field of Classification Search**
See application file for complete search history.

References Cited
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7,228,542 B2* 6/2007 Bad et al. 702/97
2003/015013 A1* 6/2003 Doudgill 702/132
2006/0041277 A1* 7/2006 Osherson et al. 702/132
* cited by examiner

Primary Examiner—John Barlow
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(74) **Attorney, Agent, or Firm—Robert C. Kowert,**
Meyerson, Flood, Kivlin, Kowert & Conrad, P.C.

(57) **ABSTRACT**
Multiple logic cores of integrated circuits and processors may be configured to operate at frequencies and voltages independently of each other. Additionally, other components, such as a common bridge configured to interface with the logic cores, may operate at a voltage and frequency independent of the voltage and frequency at which the logic cores are operating. The operating frequency and/or voltage of a logic core may be independently adjusted for various reasons, including power management and temperature control. Logic circuitry at an interface between the controller and the logic cores may translate logic signals from one voltage and/or frequency to another to enable communication between the bridge and the logic core when the two are operating at different voltages and/or frequencies.

32 Claims, 9 Drawing Sheets



- White discloses a system and method for operating components of an integrated circuit at independent frequencies and/or voltages.
- Particularly, White discloses “multiple logic cores of integrated circuits and processors . . . configured to operate at frequencies and voltages independently of each other.” White at Abstract.
- “The operating frequency and/or voltage of a logic core may be independently adjusted for various reasons, including power management and temperature control.” *Id.*

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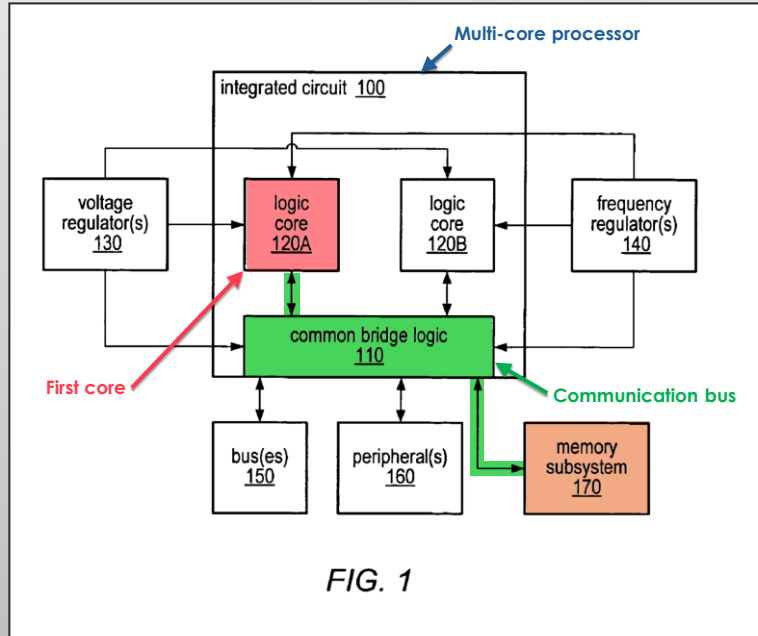


FIG. 1

White at Fig. 1 (annotated)

- Fig. 1 depicts a high-level block diagram of an integrated circuit, which includes:
 - Logic cores 120A and 120B
 - Common bridge logic 110 (i.e., communication bus)
 - Memory subsystem 170
- White also indicates its system includes an L2 cache memory

White Discloses a Core Workload Monitor

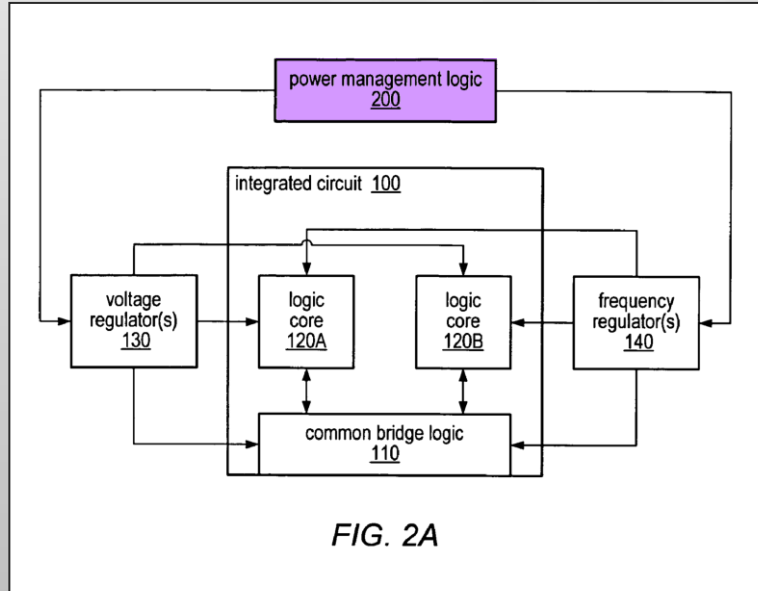


FIG. 2A

White at Fig. 2A (annotated)

Fig. 2A depicts an embodiment of a multi-core integrated circuit in which the operating voltages and/or frequencies for each of multiple logic cores are controlled by power management logic.

Please note that in some embodiments, temperature control logic 210, and power management logic 200 may both be part of a single set of logic, implemented in hardware, firmware, software, or a combination thereof, that is configured to monitor and adjust the operating frequency and/or voltage of various portions of integrated circuit 100, such as the logic cores 120 and common bridge logic 110.

White at 14:32-38

White Discloses the Claimed Core Workload Monitor



Claim 1 recites:

“a core workload monitor configured to determine a core workload for the first core”

The '494 Patent Specification explains:

Determining a workload includes any known method for determining activity of hardware, a workload of software, a number of instructions executed or to execute, or any other metric for determining use of a processing element. As one example, a workload for core **505** includes an amount time core **505** is active during a period of time. Activity may be determined as when core **505** is in an active performance state versus a sleep or low power state or a number of cycles executing or performing operations.

'494 Patent at 9:47-57

White Discloses the Claimed Core Workload Monitor



- White discloses power management logic that monitors and adjusts the operating frequency and/or voltage of various components to adjust their power consumption.
- Operating voltage and frequency of a component reflect the workload of that component.

Please note that in some embodiments, temperature control logic 210, and power management logic 200 may both be part of a single set of logic, implemented in hardware, firmware, software, or a combination thereof, that is configured to monitor and adjust the operating frequency and/or voltage of various portions of integrated circuit 100, such as the logic cores 120 and common bridge logic 110.

White at 14:32-38

Operating Voltage/Frequency Reflects Activity and Use or Workload



103. The '494 Patent indicates that “workload” is “any [] metric for determining use of a [component].” (*See e.g.*, '494 Patent, 9:47-52.) Thus, a POSITA would have understood the power management logic 200 in White monitoring the operating voltages and frequencies of the logic core 120A and common logic bridge 110 is monitoring the workload of those components. It was well understood that operating frequency and voltage of a component reflect the activity and use, or workload, of that component. Further, a POSITA would have

Wyatt Decl. (EX1003) at ¶103
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White Discloses the Claimed Core Workload Monitor



Patent Owner argues:

Monitoring operating characteristics, such as operating voltage and operating frequencies, is not the same as monitoring workload because metrics such as frequency can be altered independently of workload.

But:

- As previously explained, the '494 Patent broadly describes **any metric** for determining use of a component as a determination of workload.
- The '494 Patent even indicates frequency can be monitored as an indication of “workload”:

However, if workload module 520 determines the GPU 505's frequency is below a threshold (i.e. not working/consume at maximum capacity), then any CPU 505's frequency cap or limit is increased to cause more production, such that GPU cores 510 workload increases accordingly.

'494 Patent at 10:65-11:2

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Dispute 3 – Whether White discloses receiving workloads based on an integrated circuit limit

Claims 4, 5, 6, 7, 17, and 18

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Claim 4 recites “receiving a bus workload for a communication bus and a first processing element workload for a first processing element based on an integrated circuit reaching a limit”

White Discloses Receiving a Bus Workload



Patent Owner argues:

1. Operating voltage/frequency cannot reflect workload.
2. “receiving” workload requires receiving the actual “activity level” and cannot be anything that reflects the workload of a component

But:

- As shown previously, operating voltage/frequency does reflect workload.
- Activity level is only one of the potential ways to measure workload.

As a corollary to the multitude of potential workload measurements, the components to measure such workload may also vary. To further discussion of the potential components for workload measurement, it's assumed below that workload is measured as a number of active cycles over a period of time (i.e. a total number of cycles for measurement). As a first

'494 Patent at 9:57-67

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White Discloses Receiving Workload Based on an Integrated Circuit Limit



Patent Owner additionally argues:

White does not disclose receiving workload *based on an integrated circuit limit* because:

1. White does not mention battery power limit, and
2. Only the temperature control logic is configured to request changes in operating characteristics of the cores.

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Battery Power Indicates a Power Supply Limit



- White adjusts operating characteristics of components to reduce overall power consumption when the system is on battery power.
- Because the system can increase the frequency of logic cores when transitioning from battery power to wall power, battery power indicates a power supply limit.

tion of the system. In another embodiment, a system including a multi-core processor may be operating from battery power and power management logic 200 may be configured to detect when the system is operating on battery power and adjust the operating frequency of one or more of the logic cores. Additionally, power management logic 200 may be configured to detect when the system transitions from battery power to wall power and adjust the operating frequency of one or more logic cores to a higher frequency to take advantage of the fact that the system is no longer on battery power.

White at 15:54-64

White Receives Workload Information Based on the Integrated Circuit Reaching a Power Supply Limit



- White discloses the power management logic 200 detects when the system is operating on battery power and adjusts the operating frequency of the logic cores.
- Thus, power management logic receives workload information based on the integrated circuit reaching a power supply limit.

tion of the system. In another embodiment, a system including a multi-core processor may be operating from battery power and power management logic 200 may be configured to detect when the system is operating on battery power and adjust the operating frequency of one or more of the logic cores. Additionally, power management logic 200 may be configured to detect when the system transitions from battery power to wall power and adjust the operating frequency of one or more logic cores to a higher frequency to take advantage of the fact that the system is no longer on battery power.

White at 15:54-64

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The Temperature Control Logic and Power Management Logic Are Part of a Single Set of Logic



- White discloses the temperature control logic and power management logic may be part of a single set of logic.
- Thus, the power control logic can also request changes in operating characteristics of the cores.

Please note that in some embodiments, temperature control logic 210, and power management logic 200 may both be part of a single set of logic, implemented in hardware, firmware, software, or a combination thereof, that is configured to monitor and adjust the operating frequency and/or voltage of various portions of integrated circuit 100, such as the logic cores 120 and common bridge logic 110.

White at 14:32-38

White Also Discloses Receiving Workload Information Based on the Integrated Circuit Reaching a *Thermal Design Power Limit*



- White discloses that an integrated circuit may have a predetermined maximum operating temperature.
- The operating characteristics of components may be adjusted to lower the operating temperature.
- Thus, power management logic also receives workload information based on the integrated circuit reaching a thermal design power limit.

cool down to an acceptable operating temperature. For example, the processor, or other integrated circuit, may have a predetermined maximum operating temperature, above which the performance of the processor may be erratic or above which damage to the processor may potentially occur.

White at 2:34-38

38.) A POSITA would have recognized that a rise in the temperature (of a sub-unit, core, or package) is in fact a direct result of insufficient cooling to remove the thermal power generated at said unit/core/package level. This is a direct result and indication of exceeding a thermal design power (TDP) limit.

Wyatt Decl. (EX1003) at ¶105

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