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Explorations of optimal core and cache placements for Chip Multiprocessor

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Abstract: In this paper, we study and analyse optimal core and cache placements for modern Chip Multiprocessors (CMPs). As the number of cores increases, traditional on-chip interconnects such as bus and crossbar suffer from poor scalability and low efficiency. Ring based design has been proposed and implemented to mitigate these problems. However, the continuation growth of number of cores will render the ring interconnect infeasible. Network based designs are therefore proposed for future CMPs for better scalability. In this paper, we explore the interconnect of a state-of-the-art CMP. We analyse and compare the implementation of the ring-based and the network-based interconnect. The placement of cores and caches in a network is proved crucial for system performance. We investigate optimal core/cache placement for CMPs. The benchmark results are presented by using a cycle accurate full system simulator. Results show that, by using the optimal network interconnect, compared with the ring interconnect, the average network latency and execution time are reduced by 11.93% and 19.53% respectively, for four configurations and two applications.

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I. Introduction

We have witnessed multi-core processors emerging with increasing number of cores and complex on-chip interconnect in the past few years. The constraints of chip clock frequency, power consumption and heat dissipation have pushed the chip designers to integrate multiple cores rather than to improve single-core performance. A prevalent approach to increase chip performance is to add more cores. Normally, each core has its own computational units, registers and private caches. A last level cache will be shared by all cores. Intel Pentium D 1 is one of the first CMP which embedded two dies on a processor package. No-cache CMPs such as Intel Core i5, i7 [1] and AMD Phenom II [2] are mainstream for desktop systems. The integration of more cores on a CMP is under intensive research. For example, AMD has announced its twelve-core Opteron CMP with two dies on a chip, each of which has six cores [3]. The newest Xeon, based on Westmere-EX architecture, has been fabricated by Intel with ten cores [4]. Sun and IBM have their own CMP design as well [5], [6]. It is predictable that in the future, the integration of more cores on a single chip will move on.

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