

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Mercedes-Benz USA, LLC,
Petitioner,

v.

Daedalus Prime LLC,
Patent Owner.

Case No. IPR2023-01344
Patent 9,575,895

**PETITIONER'S REPLY TO
PATENT OWNER'S RESPONSE**

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1002	File History for the ’895 Patent
1003	IBM POWER7 multicore server processor to Sinharoy et al. (“ Sinharoy ”)
1004	DMA Cache: Using On-Chip Storage to Architecturally Separate I/O Data from CPU Data for Improving I/O Performance to Tang et al. (“ Tang ”)
1005	Explorations of Optimal Core and Cache Placements for Chip Multiprocessor to Thomas Canhao Xu et al. (“ Xu ”)
1006	U.S. Patent Application Publication No. 2009/0164739 to Harikumar (“ Harikumar ”)
1007	Declaration of Dr. Robert Horst
1008	Curriculum Vitae of Dr. Robert Horst
1009	Declaration of Gordon MacPherson, IEEE, Re Sinharoy
1010	Sinharoy IEEE Xplore Page
1011	Declaration of Gordon MacPherson, IEEE, Re Tang
1012	Tang IEEE Xplore Page
1013	Declaration of Gordon MacPherson, IEEE, Re Xu
1014	Xu IEEE Xplore Page
1015	File History for the ’895 Patent Parent Application U.S. Application No. 13/324,053
1016	Architectural Implications of Cache Coherence Protocols with Network Applications on Chip Microprocessors to Kyueun Yi et al. (“ Yi ”)

1017	Supplementary Declaration of Dr. Robert Horst
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I. Introduction

In its Patent Owner's Response ("POR"), Patent Owner disputes only whether the cited prior art, Sinharoy (EX1003) and Tang (EX1004), discloses one element of the challenged claims: a "single caching agent." (*See generally*, POR.) Patent Owner bases its arguments on incorrect assumptions and readings of Sinharoy and Tang, and an unduly narrow interpretation of "single" caching agent that would omit a "logical" single caching agent with distributed portions as expressly contemplated by U.S. Pat. No. 9,575,895 (the "895 Patent"). However, under a correct reading of these references, as described in the Petition and supported by the initial declaration of Dr. Robert Horst (EX1007) and supplemental declaration of Dr. Horst (EX1017) submitted herewith, it is clear both Sinharoy and Tang disclose "single" caching agents as claimed.

With respect to Sinharoy, Patent Owner's incorrect characterization of the reference is misleading and appears to be an attempt to create confusion. (POR, 15-22.) Patent Owner argues Sinharoy includes individual, structurally separate cache controllers for the L2 and L3 caches that allegedly do not work together, and as such does not disclose a "single" caching agent. (*Id.*) However, this argument misinterprets the Petition, which clearly states that "the cache controllers for the L2 and L3 caches, including RC and write machines, form a **logical single caching controller**." (Pet., 18 (emphasis added).) These cache controllers in Sinharoy do not

work independently from each other but work together to perform cache coherence operations as a single, logical caching agent. (Pet., 16-18; EX1007, ¶¶65-66.) Patent Owner attempts to create confusion by “cherry-picking” some snooping operations in Sinharoy, alleging that they suggest that the cache controllers work independently. (POR, 18-20.) However, Patent Owner ignores other relevant disclosures in Sinharoy, which show that the cache controllers in L2 and L3 caches of Sinharoy coordinate with each other and form a logical “single caching agent.”

With respect to Tang, Patent Owner again mischaracterizes the reference, misreads and misrepresents the Petition and Dr. Horst’s initial declaration, and incorrectly interprets Tang’s Figure 10. (POR, 27-32.) The Response first incorrectly asserts that the “petition, and Petitioner’s declarant, allege that that these two coherence controllers [of Tang] are part of the same ‘logical’ unit.” (POR, 29.) However, neither the Petition nor the initial declaration makes such an argument. Next, Patent Owner erroneously claims that Figure 10 depicts only one processor and alleges the “coherence link” shown means the two “coherence controllers” shown do not operate as a single unit, but rather operate independently and communicate with each other. (POR, 30.) However, the claims only require a “single” caching agent for one processor (’895, Claims 1, 11, 15), and Tang explicitly describes Figure 10 as a “multiprocessor system” that includes two processors each with its own “single” caching agent as explained in the Petition.

(Pet., 53-55.) Patent Owner's expert confirmed this during his deposition. (Deposition Transcript of Dr. Michael Brogioli (EX1018), 60:11-62:15.) In Tang, the last level cache (LLC) controller and the cache coherence controller within each processor form a "single caching agent" for that processor including "distributed portions," each associated with a corresponding core as shown in Figure 10. (Pet., 50-51 (clearly annotating in a dashed line box the "single" caching agent of just the processor on the left), 53-54.) Whether a caching controller of one processor communicates with the caching controller of the other through the coherence link is irrelevant.

II. Claim Construction

In the Institution Decision, the Board construed the term a "single caching agent" consistently with the disclosures of the '895 to mean "one caching agent for the processor, which may be formed from distributed portions." (Institution Decision, Paper 7 at 12.) Patent Owner argues that the term should be understood as "a solitary, that is one, caching agent for an entire processor (or multicore processor or first multicore processor)" and that the Board should revise its construction of "single caching agent" to mean "one caching agent." (POR, 8, 10.) Rather than provide clarification, Patent Owner's proposed construction merely introduces ambiguity as to when a caching agent is "solitary" and what qualifies as "one" caching agent when it can be formed of a plurality of distributed portions. This is

unnecessary, especially given the clear language in the claim and used by the Board in its construction that the “single caching agent” is “one caching agent for the processor, which may be formed from distributed portions.” (Paper 7 at 12.)

Here, the Board’s construction of “single caching agent” is the ordinary and customary meaning in light of the claim language itself and the specification. The term “single caching agent” appears in the claim language as “the caching agent is a single caching agent for the processor and includes a plurality of distributed portions each associated with a corresponding one of the plurality of cores.” (’895 Patent, Claim 1; *id.*, Claims 11 and 15 (similar language).) And, as the Board has corrected noted, the “description of Figure 6 [of the ’895 Patent] explains that a ‘single caching agent’ may be formed from distributed portions.” (Paper 7 at 12 (quotation omitted).) The ’895 Patent explicitly discloses that a processor 700 includes a distributed configuration having “partitions or slices each including a core 710 and a partition of a caching agent 715 and a LLC 720.” (’895 Patent, Figure 6, 6:33-35.) “[W]hile distributed caching agents are shown, understand that these distributed portions **form** a single cache agent.” (*Id.*, 6:35-37 (emphasis added); *see also* EX1018, 52:3-53:10 (agreeing that the caching agent can be “formed by distributed portions”).) The ’895 Patent does not discuss a particular structure or circuit implementation for the “single caching agent,” except that it discusses the caching agent can be formed from distributed portions and that it “may be logic.” (*See* ’895 Patent, 2:43-44, 6:35-

39; EX1018, 53:11-54:8.) Indeed, the specification of the '895 Patent does not even mention the word “solitary” as argued by the Patent Owner. (*See* '895 Patent; EX1018, 46:8-47:8 (admitting that the term “solitary” may be his own word).)

As such, based on the claim context and the specification of the '895 Patent, a person of ordinary skill in the art reading the term “single caching agent” would understand it means “one caching agent for the processor, which may be formed from distributed portions,” as adopted by the Board. ('895 Patent, 6:30-49; EX1017, ¶¶5-9.)

III. The Challenged Claims Are Unpatentable Over Sinharoy

A. Independent Claim 1

Patent Owner argues that because Sinharoy allegedly does not disclose a “single cache controller” (i.e., the “single caching agent for the processor” in claim limitation 1g), Sinharoy does not disclose claim 1. (POR, 16.) Patent Owner presents two arguments: (1) because L2 and L3 caches in Sinharoy have structurally separate cache controllers, there is no “single cache controller”; and (2) because there are some snooping operations in Sinharoy’s L2 and L3 caches, the cache controllers for them “operate independent of one another.” (POR, 16, 18.) Both arguments are incorrect.

As an initial matter, because Patent Owner did not argue Sinharoy fails to disclose any other elements of Claim 1, Patent Owner has waived any such

arguments. *See In re NuVasive*, 842 F.3d 1376, 1380–81 (Fed. Cir. 2016) (holding that the patent owner waived arguments that were not raised in its response after institution); *see also Hum Indus. Tech., Inc. v. Amsted Rail Co., Inc.*, IPR2023-00540, Paper 43 (PTAB Aug. 6, 2024) (“Patent Owner is cautioned that any arguments for patentability not raised in the response will be deemed waived.”). In addition, Patent Owner did not argue Sinharoy fails to disclose the other elements in claim 1g of the ’895 Patent (i.e., “wherein the caching agent . . . includes a plurality of distributed portions each associated with a corresponding one of the plurality of cores”). (POR, 15-22 (only discussing the “single caching agent” element).) Thus, Patent Owner has waived such arguments. *In re NuVasive*, 842 F.3d at 1380–81.

1. Patent Owner’s Argument that L2 and L3 Caches Have Structurally Individual Cache Controllers Misses the Point.

Patent Owner first asserts that because Sinharoy’s L2 and L3 caches have structurally individual cache controllers, there is no “single cache controller.” (POR, 16-18.) This assertion is a red herring. Petitioner does not contend that the L2 caches and L3 cache regions in Sinharoy are structurally one single caching agent. Instead, the Petition states that “the caching agent, comprising the centralized cache controllers for the L2 and L3 caches including RC and write machines, is formed as a single caching agent for the processor.” (Pet., 18; *see also* EX1007, ¶65.) And, in particular, these cache controllers for the L2 caches and L3 cache regions form one logical “single caching agent” with distributed portions. (Pet., 18; *see also* EX1007,

¶65.) The Board correctly noted this in its Institution Decision, finding that the “cache controllers for the L2 and L3 caches, including RC and write machines, form a logical single caching controller, with the single cache controller including a plurality of distributed portions each associated with one of the cores.” (Paper 7 at 17 (quotation omitted), 18 (finding “Petitioner’s argument that the L2 and L3 caches form a ‘logical single caching agent’ persuasive”).)

2. Sinharoy’s Cache Controllers for the L2 And L3 Caches Together Form a “Single Caching Agent” and Do Not Work Independently From Each Other.

Patent Owner also appears to argue that because there are some snooping operations in the L2 and L3 caches in Sinharoy, the cache controllers for the L2 and L3 caches work independently and do not form a “single caching agent.” (*See, e.g.*, POR, 18 (“Dr. Brogioli explains that it is through these individual snooping actions that overall coherency among the caches is maintained, notwithstanding that the individual cache controllers are and operate independent of one another.”).) This argument is incorrect, because Patent Owner has ignored other key disclosures in Sinharoy, which show that the cache controllers in L2 and L3 caches do work together and form a logical “single caching agent.”

Sinharoy explicitly discloses that the snooping operations can be avoided in a number of instances, and therefore Sinharoy’s cache controllers for the L2 and L3 caches work together with each other and form a logical “single caching agent.”

(EX1017, ¶¶13-14.) For example, Sinharoy discloses “[s]torage accesses that miss both the L2 cache and the 4-MB local L3 region are broadcast to the coherence fabric and snooped by the memory controller, other L2 caches, **possibly** other L3 caches, and by the seven remote 4-MB L3 regions that comprise the remaining 28 MB of the on-chip L3 cache.”¹ (EX1003, 1:19 (emphasis added).) That is, not all of the other L3 caches need to be snooped. (EX1017, ¶15; EX2001, 18:3-16.) It is clear from Sinharoy that the cache controllers for the L2 and L3 caches do not work independently from each other, and cannot handle read and write misses without coordinating with each other. (EX1017, ¶15.; EX2001 17:11-14 (“[T]here has to be some high-level logic that does that coordination.”)) Again, a POSITA would have understood that “possibly other L3 caches, and by the seven remote 4-MB L3 regions that comprise the remaining 28 MB of the on-chip L3 cache” means the cache controllers do not act independently. (EX1017, ¶15; EX2001, 18:6-7.) For example, a POSITA would have understood that the cache controller for a L3 region has knowledge about whether the lines in its local L3 region are held in any other L2 and L3 caches as well. (EX1017, ¶15; EX2001, 18:3-9.) That is, each of them has to have knowledge of what is in the other caches to be able to avoid snooping in other regions. (EX1017, ¶15; EX2001, 18:3-16.)

Furthermore, Sinharoy also discloses “[w]hen the associated core and L2 are

¹ Patent Owner also discusses this disclosure in its Response. (POR, 17.)

enabled, a number of heuristics cooperate to give precedence to the associated L2 cache while allowing load and capacity balancing among all eight L3 regions on the chip, thereby causing them to behave as a highly set-associative (64-way) adaptive 32-MB L3 cache.” (EX1003, 1:20.) The coordination to perform capacity balancing means that there is a single logic for all the caches to do the load balancing. (EX1017, ¶16; EX2001, 17:5-8.) Such single logic is formed by the cache controllers of the L2 and L3 caches. (EX1017, ¶16.) Patent Owner appears to assert that the “primary heuristic”² of “heuristics” in Sinharoy suggests otherwise. (POR, 19-20.) However, this ignores other explicit disclosures from Sinharoy. Right before Sinharoy’s disclosure of the “heuristics,” Sinharoy discloses that the “capacity, data flow logic, and control flow logic of a 4-MB local L3 region are shared between the L2 cache to which the local L3 region is coupled, and the other seven 4-MB L3 regions on the chip.” (EX1003, 1:19.) Sinharoy then discloses that “when the core and L2 associated with a given L3 region are disabled, the remaining L3 regions enjoy full access to the L3 region.” (*Id.* (emphasis added).) The reason why the remaining L3 regions still enjoy full access to the disabled L3 region is that the other cache controllers still have knowledge about the disabled L3 cache region. (EX1017, ¶16;

² Petitioner notes that Sinharoy using the term “primary heuristic” indicates there are other heuristics also used. (EX1017, ¶16.)

See also EX1018, 80:8-11 (admitting the “remaining L3 regions enjoy full access to the L3 region”).) Thus, the cache controllers for L2 and L3 caches coordinate with each other and form a logical “single caching agent.”

In addition, Patent Owner’s arguments are contradicted by Table 2 of Sinharoy, which is a table for different cache states in the L2 and L3 caches in the POWER7. (EX1003, 1:17.) The Response completely disregards Table 2 and related disclosures in Sinharoy. (*See* POR.) Table 2 shows that, in certain cases, a local L3 region does not need to snoop all the other L2 or L3 regions to obtain a shared cache line. (*Id.*; EX1017, ¶17; *see also* Pet., 17, 37-38.) Sinharoy discloses that the “POWER7 L2 and L3 caches support the same 13-cache-state protocol as the POWER6 design point,” and if “a given core’s L2 cache or local L3 region owns a copy of the targeted cache line (i.e., holds the line in an M, ME, MU, T, TE, TN, or TEN cache state), the data will be installed into the local L3 region.” (EX1003, 1:17.) Under the “Sharers and scope” column in Table 2 for the “T” state (Description, “Formerly MU, now shared”), Sinharoy specifies “Yes, probably global.” (*Id.*) For the “TEN” state (Description, “Formerly ME, now shared”), it specifies “Yes, local.” (*Id.*)³ A POSITA would have understood that “probably global” for the “T” state

³ During his deposition, Dr. Brogioli admitted that he is unfamiliar with the TEN cache state. (EX1018, 85:4-16.)

means that when a cache line is in this state and is potentially shared with other L3 cache regions, accesses to the local L3 regions need to snoop the remote L3 regions. (EX1017, ¶17.) A POSITA would have understood that “local” in the entry for the “TEN” state means that means that the targeted cache line is shared but it is known that the other non-local cores have not modified that cache line, so the local L3 cache region does not need to snoop other regions. (EX1017, ¶17.) The difference between the “T” and “TEN” states shows that snooping can be avoided in certain scenarios and that the cache controllers coordinate with each other and form a logical single caching agent. (EX1017, ¶17.)

Finally, Patent Owner’s Response is silent about Sinharoy’s description of the read/claim (RC) machines within the cache controllers. (See POR.) However, Sinharoy’s descriptions of the RC machines in the cache controllers for the L2 and L3 caches indicate the cache controllers coordinate with each other. (EX1003, 1:18-1:21; EX1017, ¶18.) Sinharoy discloses that “the read/claim (RC) machines, which have been utilized in prior designs to manage core fetches, read–modify–write operations on behalf of core stores, and core prefetch operations, have been divided into two classes: 1) a set of eight fully functional RC machines that are incorporated into the L2 cache controller and manage core fetches and stores that hit the L2 cache and 2) a set of 24 more energy-efficient ‘lightweight’ RC machines that are incorporated into the L3 cache controller and manage prefetches and stores that miss

the L2 cache.” (EX1003, 1:18.) The L2 RC machines and L3 lightweight RC machines “aggressively reorder storage operations,” thereby “enabling the high volume of system coherence traffic needed to scale robustly to a large number of sockets.” (*Id.*, 1:18-19; EX1017, ¶18; *see also* Pet., 25.) Thus, these RC machines are shared across all L3 regions and hence are part of a single logical cache controller. (EX1017, ¶18.) If the L3 regions had separate independent cache controllers, they would each need their own RC machines and there would be no opportunity to globally reorder the storage operations. (EX1017, ¶18.) There is not an independent controller per core in Sinharoy, and the shared and portioned parts of the cache controllers form a logical “single caching agent.” (EX1017, ¶18.)

Thus, as explained in the Petition, the cache controllers for the L2 and L3 caches in Sinharoy, including RC and write machines, form a logical “single caching controller.” (Pet., 18.) Furthermore, the cache controllers coordinate with each other and do not work independently from each other. (EX1017, ¶¶12-19.)

B. Independent Claims 11 and 15 and Other Dependent Claims

Patent Owner presents no separate arguments for the patentability of (1) independent claims 11 and 15 over Sinharoy (other than that they too require a “single caching agent” allegedly not disclosed in Sinharoy), (2) dependent claims 3-7, 12-13, and 16-17 over Sinharoy, and (3) dependent claims 8-9 and 14 over Sinharoy in view of Tang. (POR, 23.) Patent Owner’s arguments for claims 3-9 and

11-17 rise or fall with its arguments as to the “single caching agent” element claim

1. Furthermore, as discussed in Section III.A *supra*, Patent Owner has waived any arguments that Sinharoy or Sinharoy in view of Tang does not disclose the other elements of these claims. *In re NuVasive*, 842 F.3d at 1380–81.

C. Dependent Claims 2 and 10 and Public Availability of Xu

Patent Owner presents no separate arguments for the patentability of dependent claims 2 and 10 over Sinharoy in view of Xu.⁴ Instead, Patent Owner only argues Xu is not prior art. (POR, 24.) This is incorrect and Petitioner respectfully submits that Xu is prior art to the ’895 Patent. (Pet., 33.)

The Board has found that “[a]llowing IPR petitioners to rely on the IEEE publication date in an IPR proceeding . . . serves the interests of justice.” *Ericsson Inc. v. Intellectual Ventures I LLC*, IPR2014-00527, Paper 41, at 12 (PTAB May 18, 2015). Patent Owner contends that the effective filing date of the ’895 Patent is December 31, 2011. (POR, 26.) Petitioner has already submitted a declaration by Gordon MacPherson, Director, Board Governance & Policy Development, at IEEE. (EX1013.) The declaration clearly states that Xu was “published in 2011 NORCHIP,

⁴ As discussed in Section III.A *supra*, Patent Owner has waived any arguments that Sinharoy in view of Xu does not disclose the elements of claims 2 and 10. *In re NuVasive*, 842 F.3d at 1380–81.

date of conference November 14-15, 2011. Copies of the conference proceedings were made available no later than the last day of the conference.” (EX1013, ¶13.) Patent Owner attempts to create confusion and cites to the date when Xu was added to IEEE Xplore page. (POR, 26.) This argument is unavailing.

First, Mr. MacPherson’s declaration explicitly states Xu was “published in 2011 NORCHIP, date of conference November 14-15, 2011. Copies of the conference proceedings were made available no later than the last day of the conference.” (EX1013, ¶13.) In other words, Xu was publicly available at least by November 15, 2011 based on evidence. Second, even according to the copyright record of the physical copy of 2011 NORCHIP, the book of *2011 NORCHIP* was published at least by December 22, 2011. (EX1019 (Copyright Record of *2011 NORCHIP* with the U.S. Copyright Office).) Both publishing dates are before the effective filing date of the ’895 Patent. Thus, Xu is prior art to the ’895 Patent under at least pre-AIA 35 U.S.C. § 102(a), and Sinharoy in view of Xu discloses claims 2 and 10.

IV. The Challenged Claims are Unpatentable Over Tang

A. Independent Claim 1

Patent Owner argues that because (1) Tang allegedly does not disclose a “single cache controller” (i.e., “wherein the caching agent is a single caching agent for the processor” in claim limitation 1g) and (2) Tang allegedly does not disclose

that its caching agent “includes a plurality of distributed portions each associated with a corresponding one of the plurality of cores,” Tang does not disclose claim 1. (POR, 29-32.) As discussed in detail below, both arguments fail.⁵

1. The Response Misreads and Misinterprets the Petition Along with its Supporting Declaration and Figure 10 of Tang.

Based on Patent Owner’s Response, it has misread and misrepresented the Petition and Dr. Horst’s supporting declaration. First, the Response states that the “petition alleges that the cache coherence controller and the LLC controller are collectively a ‘single caching agent for the processor’ as recited in the challenged independent claims.” (POR, 29.) This representation of the Petition appears to be correct. However, following that, the Response notes that Tang’s Figure 10 shows a “pair of cache controllers which communicate with one another via a ‘coherence link’,” and states that the “petition, and Petitioner’s declarant, allege that these two coherence controllers are part of the same ‘logical’ unit, but Tang makes no such claim.” (*Id.*) Neither the Petition nor Dr. Horst’s initial declaration makes such an

⁵ As an initial matter, because Patent Owner did not argue that Tang does not disclose other elements of Claim 1, Patent Owner has waived any such arguments. *See In re NuVasive*, 842 F.3d at 1380–81.

argument.⁶ (See Pet., 53-55 (noting the LLC controller and the cache coherence controller on the left side of Figure 10 of Tang form a logical single caching agent and making no representations regarding the “pair” of coherence controllers being a single logical unit); EX1007, ¶¶127-29 (same).)⁷ Instead, the Petition has clearly laid out that the cache controller and the LLC controller of, for example, just the processor on the left of Figure 10 form a “single caching agent” for that processor. (Pet., 51.)

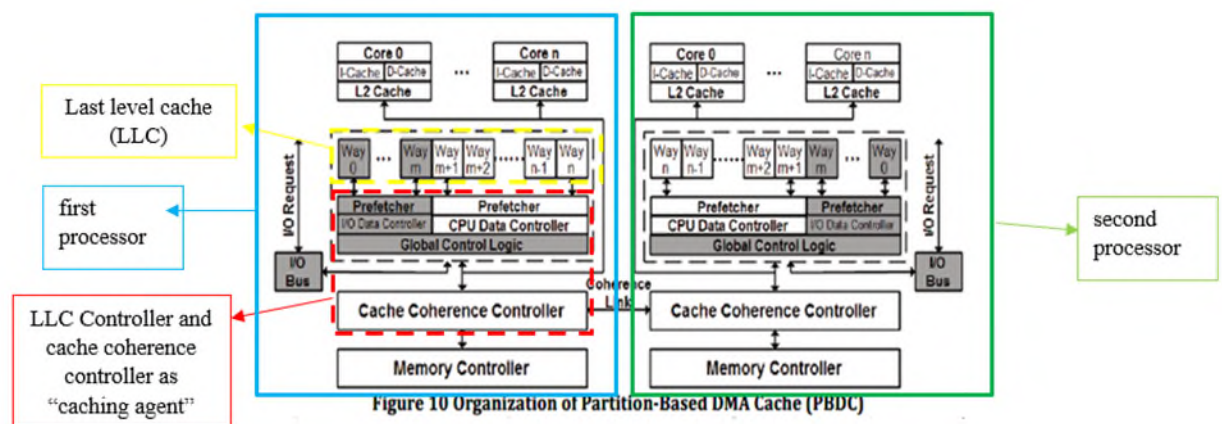
This can be clearly seen on Page 51 of the Petition, where, for example, it annotates Figure 10 with a red dotted line box around the single caching agent of that one processor. (*Id.*) Thus, as explained in the Petition, the claimed feature of a “single caching agent” for one processor is clearly met by Tang. The Petition also explains that Tang has a second processor shown on the right side with its own single caching agent comprised of its own cache controller and LLC controller. (Pet., 59-60.) Thus, the two cache coherence controllers Patent Owner references are, in fact,

⁶ Patent Owner did not ask Dr. Horst about his opinions regarding Tang during his deposition. (See EX2001.)

⁷ Furthermore, a POSITA would have understood the “coherence link” in Figure 10 connects the two processors together to form a cluster, and that it is not a connection internal to a processor. (EX1017, ¶26.)

each a part of a separate “single caching agent” for the respective processors in Figure 10.

Moreover, that Figure 10 of Tang discloses two processors, each with its own “single caching agent,” is readily apparent. Section 3.2 of Tang discloses a partition-based DMA cache (PBDC) design. (EX1004, §3.2.) Tang clearly states that “Figure 10 ... illustrates the organization of PBDC in a **multiprocessor** system.” (*Id.*, §3.2.1. (emphasis added). Even Patent Owner’s expert, Dr. Michael C. Brogioli, admitted in his deposition that Tang discloses a processor on the left side of Figure 10, and another processor on the right side with the same structure. (EX1018, 60:11-63:10 (calling the processor on the right side a “clone” of the one on the left side).) He also admitted that the processor on the left includes an LLC controller and a cache coherence controller (*id.*, 61:22-62:15), which the Petition indicated form the logical “single caching agent” for the processor on the left. (Pet., 51.) This can be seen in Figure 10 annotated below:



(EX1004, Figure 10 (annotated).)

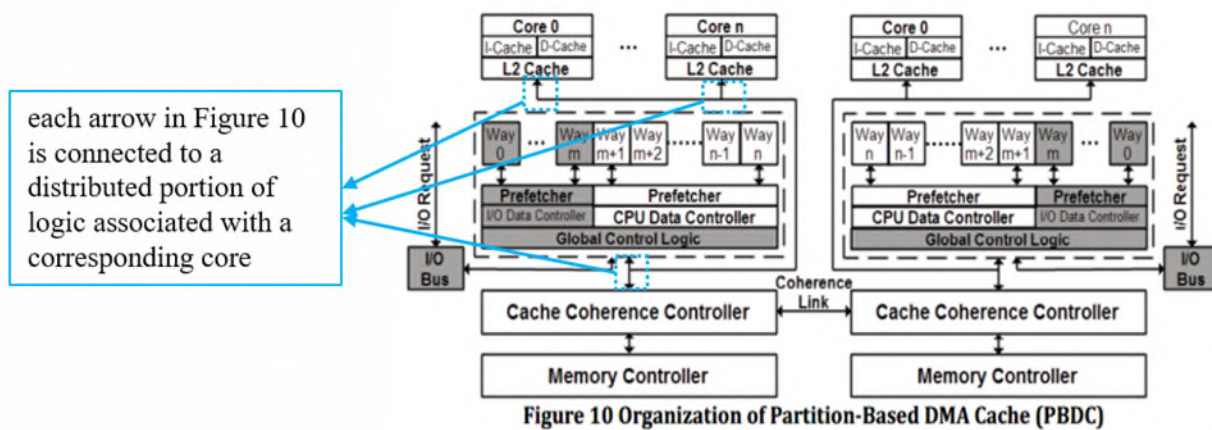
Because Patent Owner's argument is based on a misread of the Petition and Tang itself, it fails.

2. Tang's LLC Controller and Cache Coherence Controller Form a Logical "Single Caching Agent," Which has Distributed Portions, Each Associated with A Corresponding Core.

Patent Owner then argues "[e]ven if Tang can be read as disclosing a single caching agent for the processor, it is evident that that caching agent does not include a plurality of distributed portions *each associated with a corresponding one of the plurality of cores*, as further required by the challenged claims." (POR, 31.) This is incorrect based on Tang's disclosures, in particular Figure 10 and Section 3.2.2.

As the Petition explains, in the PBDC design, the LLC is partitioned into "several ways" as the "dedicated DMA Cache." (Pet., 54; EX1004, §3.2.1.) The cache coherence controller and the LLC controller form the "single caching agent." (Pet., 53-54.) According to Figure 10 of Tang, the LLC controller and the cache coherence controller (i.e., the "single caching agent") include signals and logic (depicted as arrows in Figure 10) that are each connected to core 0 to core n. (EX1004, Figure 10 (annotated below); EX1017, ¶¶28-29.) As shown in Figure 10, each signal (depicted as a single arrow going into a given core in Figure 10) is associated with logic in a single given core, which is a "distributed portion" of the caching agent. (EX1004, Figure 10 (annotated below), §§3.2.1-3.2.2; EX1017, ¶¶28-

29.) Thus, because the cache coherence controller, as part of the logical “single caching agent”, sends different signals to the different cores, it has “distributed portions” of its logic that connect to these signals. (EX1017, ¶¶28-29.) That is, the cache coherence controller has “distributed portions” corresponding to each core, allowing it to separately address and send signals to the different cores. (*Id.*)



(EX1004, Figure 10 (annotated).)

Thus, the LLC controller and cache coherence controller of Tang, as a logical “single caching agent,” include a “plurality of distributed portions each associated with a corresponding one of the plurality of cores.” (EX1017, ¶¶23-30.)

B. Independent Claims 11 and 15 and Other Dependent Claims

Patent Owner presents no separate arguments for the patentability of (1) independent claims 11 and 15 over Tang, (2) dependent claims 5-9, 13-14, and 17 over Tang, and (3) dependent claims 2-4, 10, and 16 over Tang in view of Harikumar. (POR, 33.) Patent Owner’s arguments for these claim limitations of

these claims rise or fall with its arguments as to the claim 1g limitation of claim 1.

Furthermore, as discussed in Section III.A *supra*, Patent Owner has waived any arguments that Tang or Tang in view of Harikumar does not disclose the other elements of those claims. *In re NuVasive*, 842 F.3d at 1380–81.

V. Conclusion

For the reasons above and in the Petition, the Board should find the challenged claims unpatentable.

Dated: September 11, 2024

Respectfully submitted,

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Certificate of Word Count

The undersigned certifies, in accordance with 37 C.F.R. § 42.24(d), that the foregoing **PETITIONER’S REPLY TO PATENT OWNER’S RESPONSE** complies with the type-volume limitation of 5,600 words, comprising 4,521 words, excluding the parts exempted by § 42.24(c).

Dated: September 11, 2024 Respectfully submitted,

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Certificate of Service

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, the foregoing **PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE** was served on September 11, 2024, electronically via e-mail upon the following parties:

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