

UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA )  
LLC, )  
Petitioner, )  
) IPR2023-01344  
VS. ) US Patent No. 9,575,895  
)  
DAEDALUS PRIME LLC, )  
Patent Owner. )

\*\*\*\*\*

ORAL AND VIDEOTAPED DEPOSITION OF

MICHAEL C. BROGIOLI, PhD

SEPTEMBER 4, 2024

(REPORTED REMOTELY)

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ORAL AND VIDEOTAPED DEPOSITION OF  
MICHAEL C. BROGIOLI, PhD, produced as a  
witness at the instance of the Petitioner,  
and duly sworn, was taken in the above-styled  
and numbered cause on September 4, 2024, from  
8:55 a.m. to 11:17 a.m., at 303 Colorado  
Street, Suite 2400, Austin, Texas, before  
Donna Wright, CSR in and for the State of  
Texas, reported by machine shorthand,  
pursuant to the Federal Rules of Civil  
Procedure and any stipulations or agreements  
stated on the record or attached hereto.

A P P E A R A N C E S

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## MICHAEL BROGIOLI, PhD

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## EXHIBITS

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1 THE VIDEOGRAPHER: Here begins  
2 the deposition of Dr. Michael  
3 Brogioli. Today's date is  
4 September 4th, 2024. The time is  
5 8:55 a.m.

6 Will counsel please identify  
7 themselves for the record, after which  
8 the court reporter will swear in the  
9 witness.

10 MR. HUGHES: Scott Hughes with  
11 Hogan Lovells on behalf of petitioner.  
12 And --

13 MR. FAHMI: Tarek -- I'm  
14 sorry.

15 MR. HUGHES: No, that's all  
16 right. I was saying, with me is Kyle  
17 Xu.

18 MR. FAHMI: Tarek Fahmi of  
19 Ascenda Law Group on behalf of the  
20 patent owner.

21 MICHAEL BROGIOLI, PhD,  
22 having been first duly sworn, testified as  
23 follows:

24 EXAMINATION

25 BY MR. HUGHES:

1           Q.       Good morning, Dr. Brogioli.  
2       How are you?

3           A.       Good.

4           Q.       Could you please state your  
5       full name for the record?

6           A.       Yes, it's Michael Charles  
7       Brogioli.

8           Q.       And you understand that you are  
9       being deposed today in connection with the  
10       declaration you submitted in an IPR  
11       proceeding, right?

12          A.       Yes.

13          Q.       And that IPR proceeding is  
14       IPR2023-01344, correct?

15          A.       That sounds correct, yes.

16          Q.       And this proceeding is related  
17       to a patent, US Patent No. 9,575,895,  
18       correct?

19          A.       That's correct.

20          Q.       If I refer to this today as the  
21       '895 patent, will you understand that?

22          A.       Yes.

23          Q.       Okay. Have you been deposed  
24       before?

25          A.       I have.

1           Q.       About how many times have you  
2       been deposed?

3           A.       Maybe in the range of 55 to 60  
4       or so.

5           Q.       When was the last time you were  
6       deposed?

7           A.       The last time we were here,  
8       maybe two weeks ago.

9           Q.       And that was for another IPR  
10      proceeding?

11          A.       Yes, that's right.

12          Q.       Okay. And you understand that  
13      you're under oath today?

14          A.       Yes.

15          Q.       Is there anything that would  
16      prevent you from testifying truthfully and  
17      accurately today?

18          A.       No, there isn't.

19          Q.       So I would like to just first  
20      go over a couple ground rules. I know if  
21      you've been deposed 50, 60 times, you're  
22      probably well aware of this. But if you  
23      don't understand a question, please just ask  
24      me for clarification.

25                   Your counsel may object to

1 certain questions, but you still need to  
2 answer unless specifically instructed not to.

3 We should avoid talking over  
4 each other for the court reporter and for the  
5 transcript here.

6 And in answering questions, you  
7 know, please do not nod or use hand gestures.  
8 We need an audible answer so that the court  
9 reporter can transcribe.

10 Does all of that sound fair to  
11 you?

12 A. It does. I understand.

13 Q. Okay. So you're aware that  
14 Daedalus Prime LLC is the owner of the '895  
15 patent, right?

16 A. That's my understanding, yes.

17 Q. If I refer to Daedalus Prime  
18 LLC as Daedalus, will you understand that?

19 A. Yes.

20 Q. And you were retained by  
21 Daedalus in this matter?

22 A. Yes, that's what I recall the  
23 engagement letter says.

24 Q. Who approached you about  
25 providing a declaration for this?

1           A.       I believe it would be  
2       Mr. Fahmi, who is here today.

3           Q.       Okay. And how many times did  
4       you speak with him?

5           A.       In total?

6           Q.       About being engaged.

7           A.       About the engagement, I think  
8       maybe we only spoke once or maybe twice  
9       before I would have received a letter and  
10      signed it.

11          Q.       And when were you retained?

12          A.       So that would be in my  
13      invoices. I want to say early this year.  
14      Might have to go back and look, but probably  
15      in the spring, early -- maybe late winter.

16          Q.       And you mentioned earlier the  
17      last time you testified was for another IPR  
18      proceeding. That was another IPR proceeding  
19      related to a Daedalus patent, right?

20          A.       That's correct.

21          Q.       And were you retained for all  
22      of those Daedalus matters at the same time?

23          A.       All of the ones that people  
24      from your firm have been deposing me on the  
25      last six weeks or so, yes.

1 Q. Are you retained in any other  
2 matter that's related to the '895 patent?

3 A. No, not that I'm aware of.

4 Q. And how much are you charging  
5 for your work on this?

6 A. I think it's 750 per hour.

7 Q. Dr. Brogioli, what did you do  
8 to prepare for your deposition today?

9 A. I reviewed my declaration, the  
10 '895 patent, the prior art references that I  
11 discuss in my declaration and probably  
12 certain sections of -- I think it's  
13 Dr. Horst's declaration, at least portions  
14 that I discuss in my declaration.

15 And then Mr. Fahmi and I met, I  
16 think, last week briefly and then yesterday  
17 as well.

18 Q. Okay. Did you meet with anyone  
19 besides Mr. Fahmi?

20 A. No.

21 Q. And how long did you meet?

22 A. I think yesterday -- well, we  
23 met this morning as well, so maybe a half  
24 hour this morning, maybe a half hour  
25 yesterday and, I don't recall, maybe an hour

1 the -- at some point the week prior.

2 Q. And was that in person or  
3 remote?

4 A. Last week was remote, yesterday  
5 was remote, as I think he had some travel  
6 issues that came up, and then this morning  
7 was in person.

8 Q. And you mentioned you reviewed  
9 certain materials. How did you select those  
10 materials that you reviewed to prepare?

11 A. I would say a standard process  
12 that I use in reviewing my declaration -- for  
13 an IPR where I would review my declaration  
14 and the references I discuss.

15 Q. Did you review any material  
16 that is not discussed in your declaration?

17 A. No.

18 Q. And you mentioned that you just  
19 reviewed portions of Dr. Horst's declaration,  
20 correct?

21 A. That sounds right.

22 Q. How did you select which  
23 portions to review?

24 A. They -- it would have been  
25 based on if I'm citing to something in

1 Dr. Horst's declaration in my declaration.

2 One example was I recall  
3 referring back to his claim construction  
4 definition that I believe I adopted in my  
5 declaration.

6 Q. We will get to that.

7 So as we discussed earlier, you  
8 are aware you are being deposed with respect  
9 to that declaration you submitted in the '895  
10 patent, right?

11 A. Yes.

12 Q. About how many hours did you  
13 spend preparing that declaration?

14 A. So I would go back to my  
15 invoices on it, and the reason I say that is,  
16 as I recall, the preparation for the '895  
17 probably overlapped with one or two of the  
18 other IPRs in this matter. So it's difficult  
19 for me to recall which hours per day were  
20 spent on one or more of them.

21 Q. Which other IPRs would you have  
22 reviewed at the same time?

23 A. So I recall submitting  
24 declarations for a '588 patent, an '080, an  
25 '833 patent and maybe a '494. I think a

1       number of those dates somewhat overlap in  
2       time.

3               Q.       When -- did the work overlap or  
4       you're saying you were just working on one of  
5       the Daedalus IPRs?

6               A.       I would say the work overlapped  
7       in the sense of I may have been working on  
8       multiple declarations in parallel.

9               Q.       Was there anything in any of  
10      those other declarations that you recall  
11      using for the '895 patent?

12              A.       No.

13              Q.       And who drafted the  
14      declaration?

15              A.       I did.

16              Q.       Did you do the first draft of  
17      it?

18              A.       As I recall, yes. I put -- I  
19      think I put first versions together, which is  
20      typically what I do, and then may have filled  
21      in subsequent sections, things like that.

22              Q.       Did anyone else help with the  
23      drafting of the declaration?

24              A.       In the sense of someone may  
25      have helped on tying up cites and formatting

1 or things like that or dropped in the legal  
2 standards. But other than that, no.

3 Q. And who would have helped to  
4 drop in the cites or do the other work on it?

5 A. To the extent someone did, I'm  
6 not sure who that was. I didn't have staff  
7 on my end doing that.

8 Q. So who did you send the  
9 declaration to fill in those cites as you  
10 were working on it?

11 A. The only person I communicated  
12 with was Mr. Fahmi.

13 Q. Did Mr. Fahmi do any drafting  
14 in the declaration?

15 A. I don't know that I would say  
16 drafting. He may have done, just as I was  
17 referring to, some cites or things like that,  
18 or we may have discussed something along the  
19 way.

20 Q. And just to confirm, you said  
21 you don't have any staff or anyone else who  
22 worked with you on this, correct?

23 A. Not on these matters, no.

24 Q. Okay. And having reviewed your  
25 declaration, is there anything in your

1 declaration that you wish to change?

2 A. Not that I'm aware of, no.

3 Q. Are there any errors or  
4 mistakes in your declaration that you're  
5 aware of?

6 A. Not that I recall seeing, no.  
7 Usually I see one or two typos, but I don't  
8 recall seeing that this time.

9 Q. No substantive changes you  
10 would like to make?

11 A. No.

12 Q. We're going to mark this as  
13 Exhibit 1.

14 (Exhibit 1 marked)

15 Q. Okay. Do you recognize this as  
16 a copy of the declaration you submitted in  
17 IPR2023-01344?

18 A. Yes, that looks correct.

19 Q. And does it look to be  
20 complete?

21 A. It does. And just as a note, I  
22 brought a paper copy as well with me.

23 Q. Okay. So if you turn to  
24 Appendix A of this document here, it's after  
25 page 26, this is a copy of your CV; is that

1 correct?

2 A. That -- excuse me. That looks  
3 correct. It looks like a copy from May of  
4 this year.

5 Q. And the information in your CV  
6 accurately reflects your education and work  
7 experience, right?

8 A. Yes. It's possible there is  
9 one or two maybe minor things that aren't in  
10 this version from this time, but yes, that's  
11 true.

12 Q. And what kind of minor things  
13 might that be?

14 A. I figured you would ask that.  
15 There may have been a patent  
16 issued, or two, that I was an inventor on,  
17 something of that nature.

18 Q. Okay. But no -- no other work  
19 experience or engagements?

20 A. I don't -- I don't think so.  
21 There may have been one other consulting  
22 engagement, but I don't recall specifics.

23 Q. Was there anything about your  
24 CV that you would like change?

25 A. Not that I'm aware of, no.

1           Q.       Your CV shows that you are  
2 currently managing director of Polymathic  
3 Consulting; is that right?

4           A.       That's correct.

5           Q.       What does Polymathic Consulting  
6 do?

7           A.       So a mix of consulting work, so  
8 some matters like expert work, as I'm here  
9 today for, other engineering leadership or  
10 development.

11                   We have also worked at times  
12 with various early-stage companies or  
13 startups, if you will . I think there have  
14 been interim CTO positions, or chief  
15 technology officer positions under there as  
16 well.

17           Q.       How many employees are there at  
18 Polymathic Consulting?

19           A.       It's myself, some  
20 administrative folks, and then others have  
21 been brought in based on projects on a  
22 selective basis.

23           Q.       Are they employees or are they  
24 brought in as contractors?

25           A.       They have typically been

1 brought in as contractors.

2 Q. And what is your role as  
3 managing director of Polymathic Consulting?

4 A. So I would say decisions as to  
5 what projects are taken on, what roles we may  
6 fill, whether or not there is bandwidth and  
7 timeline to work with other groups in town or  
8 other -- other organizations, I would say.

9 Q. And do you conduct any research  
10 as part of your role there?

11 A. I would say typically my, I  
12 would say, engineering research falls under  
13 other entities, although research in the  
14 sense of more like business or market  
15 research sometimes falls under the Polymathic  
16 Consulting role.

17 Q. What -- what do you mean when  
18 you say "engineering research would fall  
19 under other entities"?

20 A. So as I recall, there have been  
21 things such as various publications or  
22 engineering books that sometimes fell under  
23 Polymathic and sometimes didn't.

24 Other work might fall under my  
25 role at Rice University, other work, like

1 development of technology which patents have  
2 been issued on, falls under separate  
3 companies that --

4 Q. So when you say the engineering  
5 research falls under other entities, you are  
6 talking about your own engineering research?

7 A. I guess I was answering to the  
8 extent I was personally conducting any  
9 research, it would be perhaps on another  
10 company that I'm a founder on or involved  
11 with, or something like that.

12 Q. Does Polymathic Consulting work  
13 with any of those other entities in research?

14 A. No.

15 Q. Does Polymathic Consulting work  
16 with any other entities in general?

17 A. That are just on a client basis  
18 or an engineering sort of client  
19 relationship, typically.

20 Q. Okay. What -- what areas does  
21 your consulting work at Polymathic Consulting  
22 focus on?

23 A. So it's been things from  
24 semiconductor design, computer networking  
25 technology, various types of low power

1       computing, some things around cloud computing  
2       or a company is trying to get to a large  
3       level of scale in that area.

4               There have been some  
5       publications, like IEEE, or textbook  
6       publications that I think in some years fell  
7       under that role as well.

8               Q.       Any research or consulting in  
9       multicore processors?

10              A.       For -- I would say consulting  
11       for a number of clients, yes.

12              Q.       What would that consulting  
13       involve?

14              A.       Everything from consulting work  
15       on technology or expert work on patents or  
16       research on the market or things of that  
17       nature.

18              Q.       When you say "expert work on  
19       patents," does that include your work as an  
20       expert witness in IPRs like today?

21              A.       Yes.

22              Q.       Any research or consulting in  
23       cache coherence operations?

24              A.       Various types over the years,  
25       yes.

1           Q.       With Polymathic Consulting or  
2 with other entities?

3           A.       I would say multiple. Work  
4 under Polymathic Consulting, work in -- or I  
5 guess I'll answer, at times I have worked on  
6 caching issues, it would be other issues in  
7 the industry, rules and academia, et cetera.

8           Q.       And in academia, you're  
9 currently also an adjunct professor at Rice  
10 University, correct?

11          A.       That's correct.

12          Q.       What is the focus of your  
13 research at Rice University?

14          A.       The focus of my work there is  
15 less research and more facing areas in the  
16 industry or future facing areas. So it's  
17 been things like GPUs or emerging chip  
18 technology, emerging programming languages,  
19 things that, for lack of a better term, were  
20 cloud computing related.

21                    There has also been grant  
22 proposals and leading various engineering  
23 projects and things like that.

24          Q.       Do you teach any courses at  
25 Rice University?

1           A.       Yes, typically they have been  
2       like graduate level, so PhD candidate or  
3       master's student level seminar-facing formats  
4       that sometimes were published under. And  
5       then at other times, I have -- I typically  
6       don't take on like an undergraduate circuit  
7       design class, but I may come in to handle a  
8       class or two, if it makes sense.

9           Q.       And, for example, for those  
10       graduate students, is any of that work  
11       focused on multicore processors?

12          A.       It has been over the years,  
13       yes.

14          Q.       About how much of that work has  
15       been on multicore processors?

16          A.       I don't recall. I mean, we  
17       have looked at multicore systems,  
18       heterogenous multicore, GPU-type  
19       architectures, hardware accelerators. So it  
20       comes and goes over the years.

21          Q.       Okay. If you could turn to  
22       page 2 of your CV.

23          A.       Okay.

24          Q.       And at the top, do you see this  
25       is -- this is still under the heading of Rice

1 University, adjunct professor, correct?

2 A. Yes.

3 Q. Okay. Do you see where it  
4 says, "Embedded computing software, embedded  
5 computer hardware, and software/hardware  
6 optimization in modern computing systems  
7 utilizing modern high level programming  
8 languages"?

9 A. Yes.

10 Q. What is embedded computing  
11 software and hardware?

12 A. So in that capacity, those  
13 things were typically less software  
14 applications, like a Microsoft Word, or  
15 something, or desktop PC applications and  
16 more multiprocessor type things.

17 The other types of hardware  
18 that go into those systems, like DMA and I/O  
19 that some of the references talk about, how  
20 to optimize hardware for certain workloads,  
21 how to optimize software, so not application  
22 software, but like system level software,  
23 modems, codecs, things like that for these  
24 types of systems.

25 And then it looks like an

1 example of high level programming languages  
2 would be things around how to use C++ or when  
3 CUDA was new coming out of Nvidia to do  
4 things in novel ways.

5 Q. What is CUDA?

6 A. It's a programming language  
7 that people use for GPU-based applications.

8 Q. So was most of this work  
9 involving the programming side of it or the  
10 computer architecture side?

11 A. Probably 70 percent computer  
12 architecture and 30 percent programming,  
13 roughly.

14 Q. Was any of it related to  
15 multicore processor hardware?

16 A. Yes.

17 Q. And what would that be?

18 A. Various architectures that came  
19 in and out of the curriculum over the years.  
20 If I remember, we had folks from Arm come in  
21 and contribute --

22 THE REPORTER: From where?

23 THE WITNESS: Arm, A-R-M.

24 THE REPORTER: Okay.

25 THE WITNESS: And probably

1 Intel, Texas Instruments at the time,  
2 analog devices, things like that.

3 Q. (BY MR. HUGHES) Okay. And  
4 anything on cache coherency operations?

5 A. I would say almost certainly,  
6 but I don't recall specifically. That wasn't  
7 something that I was doing separate classes  
8 on. Students can get that elsewhere.

9 Q. So in addition to being an  
10 adjunct professor at Rice University, that's  
11 where you obtained your doctorate degree,  
12 correct?

13 A. That's right.

14 Q. And your dissertation was on  
15 heterogenous DPS-FPGA based embedded  
16 architecture, correct?

17 A. That sounds right, yes.

18 Q. Do you want to --

19 A. I guess the title is on page 1.  
20 It's reconfigurable heterogenous DSP-FPGA  
21 based embedded architectures for numerically  
22 intensive computing workloads.

23 Q. And that's not related to  
24 processor hardware, right?

25 A. No, it is. The majority of

1       that work was designing multicore systems  
2       comprised of at least three flavors of  
3       processors that I was designing. So some  
4       were DSPs, some were accelerators, some were  
5       MIPS R4000 based and systems with cache and  
6       DRAM and DMA engines included in there to  
7       move data around really quickly and things  
8       like that.

9               Q.       If we go on page 2 of your CV,  
10       it states you worked for Freescale  
11       Semiconductor, correct?

12              A.       That's right.

13              Q.       And you started to work for  
14       them in 2007, after your PhD, right?

15              A.       That's right, late -- I think I  
16       it was late 2007.

17              Q.       And according to your CV, you  
18       started there as a senior -- senior compiler  
19       engineer; is that right?

20              A.       That and processor architecture  
21       for what was the new -- well, system-on-chip  
22       plus another system not on chip that I think  
23       went to market very late 2010 or 2011.

24              Q.       Okay. And you then became  
25       chief architect, senior member technical

1 staff, right?

2 A. That's right.

3 Q. And what did you do in that  
4 role?

5 A. So a mix of -- similar to the  
6 other role, but sort of leading a bigger  
7 group. So a mix of system software for these  
8 multicore heterogenous -- highly heterogenous  
9 systems, programming language support,  
10 architecture of the new processor core that  
11 was a pretty big departure from the previous  
12 generation, integration of that six-way  
13 multicore system with -- memory system with a  
14 flavor of our own power architecture chips;  
15 basically next generation silicon on that  
16 side.

17 And then some other roles like  
18 with the Semiconductor Research Consortium  
19 and things like that, sort of with a broader  
20 industry integration or industry involvement,  
21 partnership type role.

22 Q. So during your work there, did  
23 you work on the hardware, such as the  
24 processors, yourself?

25 A. Yes.

1           Q.       And did you design any  
2 multicore processors yourself?

3           A.       Aspects of them and aspects of  
4 the system.

5           Q.       What do you mean by "aspects of  
6 them"?

7           A.       Things like how -- well, so we  
8 needed to get a lot more performance versus  
9 what we had. And so that involved making the  
10 processors a lot more powerful, being able to  
11 do a lot more math. The way that the memory  
12 system worked between the six processor  
13 system we were designing, plus the custom  
14 hardware accelerators, probably other things  
15 along the way.

16          Q.       And what do you mean by  
17 "aspects of the system"?

18          A.       So part of the hardware-facing  
19 role was getting multiples of performance out  
20 of the processor cores, but then also making  
21 sure the system was going to be much more  
22 performant as well.

23                   These systems worked in  
24 telecom, so what they are doing is taking  
25 massive amounts of data in off of cell tower

1 signals and things, digital network, Internet  
2 backbone and pushing it out. So as you can  
3 imagine, there is a lot of how does data come  
4 in and go out fast enough to do the types of  
5 things we needed them to do.

6 Q. Now, you also worked at Texas  
7 Instruments in 2005, correct?

8 A. That's right.

9 Q. What kind of work did you do  
10 there?

11 A. So Texas Instruments was  
12 funding my PhD work, and I was in-house at  
13 Texas Instruments in '05. And we were  
14 working on the DaVinci system, which was a  
15 bunch of DSP processors, coupled with a bunch  
16 ARM processors, working together for -- well,  
17 it did a lot of things, like computer vision  
18 or set-top boxes or what have you.

19 And I was working on the  
20 hardware -- SystemC hardware modeling so that  
21 we could explore different design  
22 alternatives as to how to make the next  
23 generation of these things.

24 Q. When you say "hardware  
25 modeling," what's involved in hardware

1 modeling?

2 A. In that role, it was, I guess,  
3 building components that were hardware  
4 accurate and then connecting them together to  
5 perform -- or to implement full systems and  
6 then doing iterative research and simulation  
7 to see where performance gains can be had in  
8 the system and then designing new models.

9 So things like buses, buses of  
10 various flavors, chip interconnects, there  
11 are a ton of processor models, DMA engines,  
12 things like that.

13 Q. Okay. So if we can go back in  
14 your declaration to paragraph 7.

15 A. Okay.

16 Q. This is -- it starts on page 2  
17 and goes on to page 3.

18 Do you see that?

19 A. Yes.

20 Q. So in paragraph 7, you say you  
21 developed Spinach, a computer architecture  
22 design and modeling toolset, right?

23 A. That's right.

24 Q. What is that?

25 A. It is a toolset that someone

1       designing -- well, okay, I'll back up.

2               It's a -- it's not a simulator,  
3       it's something that allows a computer  
4       architect to design simulators really  
5       quickly, so whether that's out of preexisting  
6       components or if you want to build new CPU  
7       models or memory models.

8               And there's two versions of it,  
9       but the basic gist is we started out making  
10      the first version where you could  
11      psycho-accurately model a multicore network  
12      interface. So I think it was Gigabit  
13      Ethernet or something. There was a product  
14      for sale and then the tool was expanded so  
15      that if you were looking at, say, a 12-core  
16      processor system to do ten Gigabit Ethernet  
17      back in the day, you could very quickly and  
18      iteratively build the hardware models for  
19      whatever new system you wanted to look at,  
20      say it was 13 processors or more cache or  
21      less DRAM or something like that.

22              And then you could write your  
23      application that would run on that multicore  
24      system and run it on top of the system  
25      that -- the simulator that the system built

1       you.

2               Q.       So Spinach is related more  
3       towards chip design. It's not itself  
4       computer hardware; is that right?

5               A.       It's related to computer  
6       hardware design, but rather than constantly  
7       prototyping in, for example, VHDL and cadence  
8       tools, you can turn the crank more quickly  
9       with this system is one of the things we were  
10      going for.

11              Q.       Okay. And if you go to  
12      paragraph 14 of your declaration, do you see  
13      there where you state, "In the mid" -- this  
14      is down towards the bottom, "In the mid  
15      2000s, I designed various cache systems,  
16      cache controllers, interconnects and  
17      multicore processing architectures using said  
18      technology"?

19              A.       Yes.

20              Q.       Do you recall what companies  
21      you were working for at that time?

22              A.       So that work would have been, I  
23      would say roughly, from 2002 through 2000,  
24      let's say, seven. So it would include the  
25      work at Texas Instruments, it would include

1 earlier work.

2 I may have been funded by Nokia  
3 on configurable cache systems and then work  
4 that -- when I mention those network  
5 interface processors was with a company  
6 called -- or jointly with a company called  
7 Alteon WebSystems, maybe, and then there was  
8 work in there that overlapped with -- I think  
9 funded work at the University of Houston as  
10 well, and I think work that overlapped with  
11 Purdue and some folks at Purdue as well. I'm  
12 sorry, I take that back. People at  
13 Princeton. I don't think Purdue was part of  
14 that group.

15 Q. When you say "designed," do you  
16 mean using the EDA software to design the  
17 chips?

18 A. Not in this role. It was more  
19 SystemC-type modeling, which is a little bit  
20 higher level of abstraction.

21 Q. What is SystemC-type modeling?

22 A. It was us using a custom  
23 language where you can model or design  
24 hardware components psycho-accurately how  
25 they would operate in hardware. And then, as

1 I recall, there was a tool chain path to take  
2 the SystemC model and create like the  
3 networks for hardware out of it, et cetera,  
4 or you could run it in a faster simulation  
5 mode.

6 Q. And did you work on any of  
7 those models that was done in the hardware?

8 A. Yes, that's, I guess, what I've  
9 been talking about the last five or ten  
10 minutes or so. So it was models or designing  
11 new models for new -- everything from  
12 processors to buses and interconnects to  
13 bridges to cache memory and cache controllers  
14 and all of that.

15 Q. And if we look a little bit  
16 more in that paragraph, you state that you've  
17 specifically worked in areas of caches,  
18 direct memory access, DMA, and memory system  
19 optimization since the late 1990s.

20 What is DMA, or direct memory  
21 access?

22 A. So it's a way in a computer  
23 to -- let me start over.

24 It's a way in the computer to  
25 quickly move chunks of memory around in the

1       system. So rather than have a CPU -- if I  
2       want to move a kilobyte of data, rather than  
3       do a -- load one 32-bit entry, store it here,  
4       implement the addresses, load another one, et  
5       cetera, there's inefficiencies that come from  
6       doing that.

7                        So what DMA allows, in a simple  
8       answer, is to say, hey, go get this chunk of  
9       memory, stick it here and I'm just going to  
10      tell you to go away and finish it, and then  
11      when you're done, an interrupt goes off.

12                      So it's a lot faster and you  
13      don't keep the CPU tied up the whole time.  
14      And so I first started working with that  
15      probably in 1998 or nine or so.

16              Q.       Okay. And what is a cache?

17              A.       It's generally a small area of  
18      fast memory that can be used by a CPU for  
19      storing of data or storing of instructions,  
20      things like that.

21              Q.       Is that different than DMA?

22              A.       Yeah, in the sense that the DMA  
23      is typically used to move data around. For  
24      example, you can move it into a cache or into  
25      another place in memory.

1           Q.       So, Dr. Brogioli, in your  
2       declaration, including at page 10, you  
3       discuss a person of ordinary skill in the  
4       art, which you call a POSITA; is that  
5       correct?

6           A.       That's right.

7           Q.       What is your understanding of a  
8       person of ordinary skill in the art?

9           A.       It is, as I say in this  
10      paragraph, a person of skill who has a  
11      working knowledge of the technology space in  
12      this example that the patent talks about,  
13      and -- at the time that the patent was filed,  
14      and as I discuss in paragraph 25,  
15      someone who, in this example, would have the  
16      characteristics or level of technical  
17      understanding that I describe here.

18          Q.       Okay. And you opine in this  
19      paragraph that you have adopted Dr. Horst's  
20      definition of a POSITA; is that correct?

21          A.       That's correct, about halfway  
22      down.

23          Q.       And his definition of a POSITA  
24      was someone with an undergraduate degree in  
25      computer science, computer engineering,

1       electrical engineering or similar  
2       disciplines, along with two years of  
3       experience working with multicore processor  
4       systems, central processing unit, CPU, cache  
5       and memory systems is that right?

6             A.       That's right.

7             Q.       Now, earlier in this paragraph,  
8       you say that you have been asked to apply a  
9       somewhat more rigorous version of this  
10      description of a person of ordinary skill in  
11      the art for the purposes of this declaration;  
12      is that right?

13            A.       Right, about halfway down,  
14      referring to the definition of 0 -- as I  
15      recall, the definition that the petitioner  
16      had put out, which is in the second and third  
17      lines.

18            Q.       And so you believe that  
19      Dr. Horst's definition is more rigorous than  
20      that?

21            A.       Yes.

22            Q.       In what ways?

23            A.       It is -- Dr. Horst's definition  
24      is, in my opinion, more well defined in terms  
25      of the skill set that this person of skill in

1 the art would have rather than what I felt  
2 was a little bit more generic definition the  
3 petitioner had put forth.

4 Q. And you consider yourself a  
5 POSITA, right?

6 A. Yes.

7 Q. In your declaration, you  
8 actually state, in paragraph 26, that you met  
9 and exceeded this definition of a POSITA; is  
10 that right?

11 A. That's right.

12 Q. And what do you mean by  
13 "exceeded this definition"?

14 A. That at the time, I would have  
15 met what is described in Dr. Horst's and my  
16 definition and had additional experience in  
17 that at the time.

18 Q. And what type of additional  
19 experience would that be?

20 A. As I recall, more than an  
21 undergraduate degree, I probably worked in  
22 the industry a number of years as well at  
23 that point, I think I probably had finished a  
24 master's degree that overlapped with this  
25 area, a number of publications and things

1       like that.

2               Q.       Okay. Dr. Brogioli, in your  
3       declaration you also mention some legal  
4       standards.

5                       Do you recall that?

6               A.       Yes.

7               Q.       And I can direct you to page 7.

8               A.       Okay.

9               Q.       In this section, you go through  
10      your understanding of some general principles  
11      concerning patent law; is that right?

12              A.       That's right.

13              Q.       What was this understanding of  
14      these general principles based on?

15              A.       I would say these would have  
16      been things that I would have discussed with  
17      counsel for a declaration like this, and it's  
18      probably a similar section that I have used  
19      and discussed in the past in prior  
20      engagements.

21              Q.       So you consider yourself  
22      familiar with general principles of patent  
23      law?

24              A.       As described in this section,  
25      yes.

1           Q.       And one of those legal  
2 principles is obviousness, right?

3           A.       Yes.

4           Q.       What is the standard for  
5 obviousness?

6           A.       It looks like that's what I  
7 address in paragraph 19 where it involves  
8 things such as -- when looking at -- at the  
9 references, what's the scope of a prior art  
10 reference or what's the content, what are the  
11 differences between what the claims of the  
12 patent are talking about and what the subject  
13 matter of a prior art reference is talking  
14 about, and then taking into account this  
15 level of skill that someone in the art would  
16 have in looking at these references.

17          Q.       What do you mean by "taking  
18 into account this level of skill"?

19          A.       I would say that the -- when I  
20 defined or Dr. Horst defined the level of a  
21 person of skill in the art, that's sort of  
22 the lens that someone is looking at the  
23 patent with the prior art references and  
24 whether or not something would be understood  
25 by them or obvious by them when reading those

1 references.

2 Q. In paragraph 19, you mention  
3 the fourth is objective indicia of  
4 nonobviousness.

5 Do you see that?

6 A. Yes.

7 Q. And you talk about that a  
8 little bit in paragraph 22 where you talk  
9 about prior art teaching away; is that right?

10 A. It looks like that's one thing  
11 discussed in paragraph 22, yes.

12 Q. Do you discuss any other  
13 objective indicia of nonobviousness?

14 A. It looks like I also discuss  
15 obviousness in paragraph 20.

16 Q. My question was on the  
17 objective indicia of nonobviousness.

18 A. Oh.

19 Q. Do you opine on any objective  
20 indicia of nonobviousness?

21 A. It looks like that's what I'm  
22 discussing in that paragraph 22 or in this  
23 section as well. It wouldn't be anything  
24 beyond what's in this section.

25 Q. Do you know what some of the

1 objective indicia of nonobviousness are?

2 A. I think that's exactly what I  
3 talk about in 22, if I'm understanding you.  
4 For instance, references teaching away from  
5 combining a certain -- certain known  
6 elements.

7 If a patent is talking about  
8 one thing and then, you know, this  
9 combination points this person of skill in  
10 the art in another direction or leading with  
11 another result is what I'm discussing in  
12 paragraph 22.

13 Q. And you're not aware of any  
14 other objective indicia of nonobviousness  
15 that would be relevant here?

16 A. I would say if there is  
17 something in that portion of the law that I  
18 haven't talked about in this section, I don't  
19 know that it's something I would have  
20 considered in this declaration or I would  
21 have intended to include it here.

22 Q. I'm going to hand you what  
23 we're going to mark as Exhibit 2, and this is  
24 a copy of the '895 patent.

25 (Exhibit 2 marked)

1 Q. Do you recognize this document?

2 A. Yes, this is the '895 patent I  
3 talk about in my declaration.

4 Q. And you've reviewed and  
5 analyzed this in preparation for your  
6 deposition today?

7 A. That's correct.

8 Q. In the context of the '895  
9 patent, what is a caching agent?

10 A. So one of the things the patent  
11 talks about is this integration of an I/O  
12 onto a multicore processor and issues that  
13 come up there in terms of scale.

14 And so one of the things the  
15 patent talks about is having a caching agent  
16 that's performing -- the cache coherence  
17 operations among the cores on the processor  
18 in this I/O -- IIO module and benefits that  
19 come from that, such as better scalability  
20 and things like that.

21 Q. When you say "I/O," what do you  
22 mean by I/O?

23 A. What the patent talks about is  
24 I/O data coming to this multicore chip. For  
25 example, I think things it talks about is

1       like a disk drive or something like that.

2               Q.       And just for clarification,  
3       when you say "I/O" here, you're referring to  
4       input/output; is that correct?

5               A.       That's right, and that's what  
6       the patent talks about as well.

7               Q.       Okay. And so the caching agent  
8       is doing cache coherence operations for the  
9       cores and an IIO module in the context of the  
10      '895 patent; is that right?

11              A.       There is a caching agent that's  
12      supporting both that CPU and I/O traffic  
13      within the device and coherency operations.

14              Q.       What is a cache coherency  
15      operation?

16              A.       So cache coherency is the  
17      notion of, you know, if we use a simple  
18      example, you might have two CPUs with an  
19      associated cache and coherency is what's used  
20      to make sure each CPU's, in this example,  
21      cache are maintained consistently or have the  
22      same view of the world or don't get out of  
23      sync.

24                      THE REPORTER:   Of the world --  
25              at the end, what did you say?

1 THE WITNESS: I was just saying  
2 they don't get out of sync.

3 THE REPORTER: Okay.

4 Q. (BY MR. HUGHES) So what is the  
5 coherency operation then?

6 A. It depends what type of -- so  
7 there are different coherency protocols that  
8 have different states associated with them,  
9 like data being modified or exclusive or  
10 things like that.

11 And so there are various  
12 operations that are required, for example,  
13 moving data from a cache out to a main memory  
14 or moving it from one cache to another or --  
15 I think things that the patent talks about,  
16 like merging cache lines, things like that.

17 Q. So merging cache lines would be  
18 a cache coherency operation?

19 A. I was saying I think that's one  
20 thing the patent talks about. But depending  
21 on -- there's various operations that happen  
22 to move data around or say someone has it  
23 exclusively or someone has modified it,  
24 things like that.

25 Q. And do you still have a copy

1       your declaration in front of you as well?

2               A.       Yes.

3               Q.       Can you go to paragraph 30 of  
4       your declaration, which I believe starts on  
5       page 13.

6               A.       Okay.

7               Q.       Are you there?

8               A.       Yes.

9               Q.       So in paragraph 30, you state  
10       in about -- I think the fourth line down, "A  
11       person of ordinary skill in the art would  
12       understand the phrase 'single caching agent'  
13       as specifying one such caching agent"; is  
14       that correct?

15              A.       Yes.

16              Q.       And then if we go down towards  
17       the end of paragraph 30, on page 14, your  
18       last sentence, you state that, "Thus  
19       understanding each of the independent claims  
20       as reciting a solitary, that is one, caching  
21       agent for an entire processor or multicore  
22       processor or first multicore processor  
23       comports with the way in which the term is  
24       used in the '895 patent."

25                      Do you see that?

1           A.       Yes.

2           Q.       So in your understanding,  
3           you're saying that the '895 patent requires a  
4           solitary caching agent?

5           A.       Each of those independent  
6           claims, as we're saying that's a solitary or  
7           singular caching agent.

8           Q.       When we look at the '895  
9           patent, it doesn't use the terms "one caching  
10          agent" or "solitary caching agent," does it?

11          A.       Well, the independent claim 1,  
12          for example, at, I guess, column 7, line 59,  
13          uses the language "a single caching agent,"  
14          and continues on.

15                   And I'm, in my paragraph here,  
16          talking about why this single caching agent  
17          that's shared by the IIO module and the cores  
18          of the processor is -- is what the patent is  
19          describing.

20                   I think your question was about  
21          the word "solitary." That may be my word  
22          to -- to describe what's being described in  
23          the patent. I would have to go back and  
24          check for you about words in the  
25          specification.

1           Q.       But that may be your word and  
2 not something that's actually used in the  
3 '895 patent, correct?

4           A.       I would say to the extent it's  
5 not used in the patent, I'm using it to  
6 describe why the claims should be interpreted  
7 the way they are and that it's talking about  
8 a single caching agent.

9           Q.       So if we can go to the '895  
10 patent, can you turn to figure 6 of this  
11 patent?

12          A.       Okay.

13          Q.       And if you look in column 6, at  
14 about line 30, do you see at the end in  
15 describing figure 6, this states that what's  
16 shown may form a single caching agent?

17          A.       Let me just look at the  
18 paragraph.

19                   That it says, roughly at  
20 line 36, understand that these distributed  
21 portions form a single caching agent.

22          Q.       So if we go -- if we go back to  
23 figure 6 here, figure 6, you would agree, is  
24 a block diagram of a multicore processor,  
25 correct?

1           A.       That's right, that's how it's  
2 described in column 1 as well.

3           Q.       And this block diagram depicts  
4 multiple cores, right?

5           A.       That's right, cores 710, for  
6 example.

7           Q.       And, for example, those are  
8 marked as 710-0 through, I believe, 710-n; is  
9 that right?

10          A.       That's correct.

11          Q.       And those are just shown as  
12 kind of a box in the figure; is that right?

13          A.       In this figure, yes.

14          Q.       That's kind of a representation  
15 of the hardware corresponding to each core;  
16 is that fair?

17          A.       I think it's just intending to  
18 show us that in this example, there is N  
19 cores on this particular device in figure 6.

20          Q.       Okay. And figure 6 also has  
21 some blocks that are labeled as caching  
22 agent.

23                    Do you see that?

24          A.       It looks like the 17 -- sorry,  
25 715-0 to 715-n illustration.

1           Q.       And those 715-0 to 715-n  
2       caching agent boxes are put next to the 710  
3       core boxes; is that right?

4           A.       The way those are visualized,  
5       and then in column 6 again, almost where we  
6       were, it says at 44, "Via caching agent  
7       715-0 - 715-n."

8           Q.       Okay. And when we look at this  
9       figure, the number of caching agent blocks  
10      matches the number of core blocks; is that  
11      right?

12          A.       In terms of how it was  
13      visualized and that they -- the core ones end  
14      with an n subscript and the caching agents  
15      end with an n subscript, similar to the LLC  
16      caches.

17          Q.       And the -- excuse me -- the  
18      caching agent is being depicted with separate  
19      blocks; is that right?

20          A.       I guess I would say that's just  
21      the visualization of figure 6. But even as I  
22      just pointed out on column 6, it refers to a  
23      caching agent.

24          Q.       And in figure 6, we have  
25      caching agents that are -- for example, we

1 have caching agents 715-0, right?

2 A. That's -- that's right, on the  
3 upper left.

4 Q. And then there is also, on the  
5 lower right, a caching agent 715-n; is that  
6 correct?

7 A. Then it's saying -- well, the  
8 way I interpret this, and the patent says  
9 explicitly, "Via caching agent 715-0-715-n."  
10 But they are, in figure 6 anyhow, showing as  
11 different squares in the figure.

12 Q. Okay. So I think we were  
13 looking at, and I believe you were just  
14 looking at column 6 of the patent. If we  
15 could go there, we have at column 6, around  
16 line 42, and I believe this may be where we  
17 were reading, it says, "The various cores may  
18 be coupled to each other and to a shared  
19 caching" -- sorry -- "to a shared cache  
20 memory formed by plurality of units of a LLC  
21 7400-740n, via caching agent 7150 to 715-n."

22 Did I read that correctly?

23 A. I think so, yes.

24 Q. What is a unit of LLC?

25 A. LLC is -- let me make sure I'm

1 speaking correctly.

2 It's a last level cache. Just  
3 to cite us back to column 2, line 23. And so  
4 it's saying at 43 that there is a shared  
5 cache memory formed by -- formed of a  
6 plurality of units of the last level cache.

7 Q. So looking, again, at figure 6,  
8 we have -- for example, looking at -- I guess  
9 starting with the core 710-0, we have got  
10 blocks going across and we have a core 710-0,  
11 a caching agent 715-0, and an LLC 720-0,  
12 correct?

13 A. No, the way it's being  
14 described is there is the core 710-0. And  
15 going back to two places in column 6, one,  
16 column 6 at 36, where it says, "Note that  
17 while distributed caching agents are shown,  
18 understand that these distributed portions  
19 form a single caching agent."

20 And then also where we just  
21 were in column 6 at 44, where it says, "Via  
22 caching agent 715-0 - 715-n."

23 So there's a core block,  
24 there's a caching agent, and there's the LLC  
25 where you were pointing to, which is referred

1 to as -- that would, I guess, be one of the  
2 plurality agreements of an LLC.

3 Q. And what you just said, I  
4 believe, is that the caching agent, though,  
5 can be formed by distributed portions, right?

6 A. That's what it's saying -- I'll  
7 back up.

8 In column 6 at 35, it's saying,  
9 "Note that while distributed caching are  
10 shown, understand that these distributed  
11 portions form a single caching agent."

12 Q. And each distributed portion is  
13 distinct from the others, right?

14 A. I guess those portions form the  
15 single caching agent for the cores and the  
16 I/O module in that figure.

17 Q. And there are multiple  
18 portions; is that right?

19 A. I guess the way it's being  
20 visualized in six is showing -- that's what  
21 it's saying is shown for figure 6, but that  
22 they are a single caching agent themselves.

23 Q. So, for example, 715-0 shown in  
24 figure 6 is one portion of the caching agent,  
25 correct?

1           A.       In terms of how this is  
2 visualized, that looks like it's correct.

3           Q.       And 715-n would be another  
4 portion of the caching agent as it's  
5 visualized, correct?

6           A.       It looks like how that's --  
7 that is how it's being visualized in  
8 figure 6; the distributed caching agents are  
9 shown, but understand that these distributed  
10 portions form a single caching agent.

11          Q.       The '895 patent does not  
12 discuss the structure of the single caching  
13 agent except that it has these distributed or  
14 partitioned portions, correct?

15          A.       Well, I mean, the patent goes  
16 on at length to discuss the caching agent and  
17 I would say various aspects of it and  
18 functionality that it performs.

19          Q.       My question, though, was does  
20 it discuss the particular structure for the  
21 single caching agent?

22          A.       I don't recall that it  
23 describes it in terms of a circuit  
24 implementation or something at that level.

25          Q.       But it does indicate that it

1       can be formed from distributed portions,  
2       correct?

3             A.       It looked like at least  
4       figure 6 uses the language that the single  
5       caching agent may be formed from distributed  
6       portions, and that's in column 6 of 35. It  
7       looks like that's what I'm addressing in my  
8       Paragraph 31.

9             Q.       The '895 just shows these  
10       distributed portions as the boxes in  
11       figure 6, correct?

12            A.       In figure 6, it's showing the  
13       caching agent is comprised of those 715  
14       boxes.

15            Q.       And, again, like you said, for  
16       the caching agent it doesn't talk about any  
17       circuitry or hardware for these portions  
18       either, does it?

19            A.       I guess I would say I don't  
20       discuss that in my declaration. I don't  
21       recall that the patent talked about a  
22       specific circuit implementation for that. It  
23       probably describes it a number of other ways.

24            Q.       What do you mean by "a number  
25       of other ways"?

1           A.       In terms of things that --  
2       functions it performs, like handling things  
3       like non-posted leads, and so forth,  
4       requests, probably circumventing deadlocks,  
5       things like that.

6           Q.       So it may be describing the  
7       functionality of it, but not the  
8       implementation?

9           A.       I don't think I have discussed  
10      implementation issue in my declaration, at  
11      least for the arguments of Dr. Horst's that I  
12      addressed.

13          Q.       We're going to move on to  
14      another one. I don't know if you want to do  
15      a break or --

16          A.       I could use a restroom break.

17                 THE VIDEOGRAPHER:   Going off  
18      the record. The time is 10:05.

19                 (Recess from 10:05 a.m. to  
20      10:19 a.m.)

21                 THE VIDEOGRAPHER:   Back on the  
22      record. The time is 10:19.

23          Q.       (BY MR. HUGHES) Dr. Brogioli,  
24      in preparing your declaration, do you recall  
25      analyzing a prior art reference by Tang

1       titled "DMA Cache: Using On-Chip Storage to  
2       Architecturally Separate I/O Data from CPU  
3       Data for Improving I/O Performance"?

4             A.       Yes.

5             Q.       If I refer to that reference as  
6       Tang, will you understand that?

7             A.       Yes, I will.

8             Q.       So I'm going to hand you what  
9       we're going to mark as Exhibit 3.

10                    (Exhibit 3 marked)

11            Q.       Do you recognize this as a copy  
12       of the Tang reference you reviewed for your  
13       declaration?

14            A.       I do. It looks like the same  
15       reference.

16            Q.       What does DMA mean in this  
17       reference?

18            A.       It looks like there's memory on  
19       the device and Tang is using what he refers  
20       to as a decoupled DMA cache or another design  
21       that's a partition-based DMA cache.

22                    It's, as I recall, moving data  
23       around in the system and there's certain  
24       types of -- what I talk about the I/O data  
25       controller and the CPU controller related to

1       some of this functionality.

2               Q.       Okay. What is a DMA cache,  
3       according to Tang?

4               A.       It looks like I talk about some  
5       of this on the bottom of 22, that Tang talks  
6       about using a -- so the DMA is to move these  
7       chunks of information and data back and  
8       forth, and he talks about having a dedicated  
9       DMA cache for referring to the storing of I/O  
10      data, or input/output data.

11              Q.       And Tang also talks about CPU  
12      data, correct?

13              A.       That's right.

14              Q.       And CPU data is separate from  
15      the I/O data?

16              A.       In Tang's context, yes.  
17      There's your I/O data that is data -- Tang  
18      refers to as coming from an I/O device  
19      directly; and then CPU data is not something  
20      produced by an I/O. But, as I recall, it's  
21      something that's updated or computed by the  
22      CPU.

23              Q.       When you say "by the CPU," what  
24      do you mean?

25              A.       It would be the compute cores

1 in Tang's design, so the cores we see in  
2 Tang's -- that I show on my page 22, Tang's  
3 figure 10, it shows cores.

4 Q. So Tang actually discloses two  
5 different designs for the DMA cache, correct?

6 A. I think it's correct that he  
7 discloses two different techniques that I  
8 mentioned earlier.

9 Q. Okay. And if we turn to page 5  
10 of Tang, do you see the heading, "3. Two  
11 Designs of the DMA Cache"?

12 A. That's right, yes.

13 Q. And the first design is  
14 decoupled DMA cache DDC, right?

15 A. That's correct. If we look in  
16 that same paragraph under three, it says the  
17 second design is partition-based DMA cache  
18 PBDC; is that right?

19 A. Yes.

20 Q. So if -- excuse me -- if you  
21 can turn to section 3.2.1 of Tang, it starts  
22 at the bottom of page 6.

23 Do you see that?

24 A. Yes.

25 Q. And this is about the PBDC

1 design, right?

2 A. That looks right. It starts --  
3 he starts talking about the overview of the  
4 PBDC.

5 Q. And I believe like you just  
6 mentioned in paragraphs 40 and 41 in your  
7 declaration, you were looking at this PBDC  
8 design, correct?

9 A. In 40 and 41 of my declaration,  
10 that's correct.

11 Q. And 42 as well?

12 A. That's correct, yes.

13 Q. So is it fair to say that in  
14 your declaration, you were opining on Tang's  
15 PBDC design in comparison to the claims?

16 A. I'm just skipping ahead to the  
17 next couple of paragraphs.

18 That looks right. The  
19 subsequent paragraphs under my -- I guess my  
20 subheading 2, it looks like I talk about that  
21 figure 10 of Tang, which is -- as Tang shows,  
22 referring to the PBDC design.

23 Q. Okay. So if we can go back to  
24 the bottom of page 6 in Tang, under the 3.2.1  
25 heading, it states, "From Figure 10 that

1 illustrates the organization of PBDC in a  
2 multiprocessor system, PBDC can use several  
3 ways of the processor's LLC as the dedicated  
4 DMA cache."

5 Do you see that?

6 A. Yes.

7 Q. So Tang is talking about, for  
8 this PBDC, a multiprocessor system, right?

9 A. That's what he's referring to,  
10 yes, at the very bottom of the prior page.

11 Q. And figure 10, like that  
12 section we just read, indicates -- is  
13 depicting this multiprocessor system,  
14 correct?

15 A. It looks like it's a -- a  
16 diagram showing, as I mentioned earlier,  
17 cores and various L2 caches and components  
18 that go into his -- what he's describing as a  
19 multiprocessor type system.

20 Q. So figure 10 is illustrating a  
21 multiprocessor system, correct?

22 A. He's saying it's PBDC in a  
23 multiprocessor system, yes.

24 Q. And if we look at figure 10, we  
25 can see, for example, on the left side of the

1 figure, we would have a processor with Core 0  
2 to Core n; is that right?

3 A. That's correct, on the top  
4 left.

5 Q. And according to section 3.2.2  
6 of Tang, if you look at that, that 3.2.2 is  
7 "The Design of the Last Level Cache  
8 Controller (LLC-Ctrler)," correct?

9 A. That's the heading of 3.2.2,  
10 yes.

11 Q. And if we look at that, that  
12 processor on the left side includes a shared  
13 LLC with n ways; is that correct?

14 A. Did you say m or n?

15 Q. N.

16 A. I'm just going back to see how  
17 it's articulating these ways.

18 Yes, that looks right. This is  
19 what I discuss in my 45. So it's the zero to  
20 n, as in Nancy, ways illustrated in the left  
21 portion of Tang's figure 10.

22 Q. If we look a section 3.2.2, the  
23 processor includes an LLC controller, which  
24 consists of a global control logic, GCL; I/O  
25 data controller, IOD-Ctrler; CPU data

1 controller, CPUD-Ctrler; two prefetchers and  
2 a configuration module, correct?

3 A. That looks like what Tang says  
4 in that first paragraph under 3.2.2.

5 Q. And we can see those on the  
6 left-hand side of figure 10, I believe in  
7 that -- the box with the dashed line outline.

8 Do you see that?

9 A. I do. That looks like what  
10 they're showing.

11 Q. And then looking at this  
12 section in figure 10, this processor on the  
13 left also has a cache coherence controller,  
14 correct?

15 A. That is correct.

16 Q. And a memory controller as  
17 well, right?

18 A. That's correct.

19 Q. And then if we go now looking  
20 at the right-hand side of the figure, this is  
21 depicting another processor with those same  
22 structures, right?

23 A. It looks like it is showing  
24 another -- sort of a clone of the  
25 architecture on the left where there are

1 dissimilar components we talked about a  
2 moment ago, such as a global control logic,  
3 cache coherence controller, et cetera.

4 Q. And it's depicting those as  
5 part of the multiprocessor system of  
6 figure 10, correct?

7 A. It looks like it is, yes. That  
8 figure 10, Tang says, "From figure 10 that  
9 illustrates the organization of PBDC in a  
10 multiprocessor system."

11 Q. You can set that aside.

12 So I'm now going to hand you a  
13 copy of what we're going to mark as  
14 Exhibit 4, and I believe this might be  
15 Exhibit 1003 to the petition. This was a  
16 reference called Sinharoy. Do you recall  
17 working on Sinharoy?

18 A. I do.

19 (Exhibit 4 marked)

20 Q. And do you recognize what I  
21 just handed you as the Sinharoy reference you  
22 reviewed in preparing your declaration?

23 A. Yes, this is the reference that  
24 I reviewed.

25 Q. And if I refer to this as

1       Sinharoy, will you understand that?

2             A.       Yes.

3             Q.       All right. And Sinharoy  
4 discloses a POWER7 multicore processor,  
5 right?

6             A.       That's right. It's an IBM  
7 product that was -- that was on the market at  
8 the time of this reference, or shortly  
9 thereafter, perhaps.

10            Q.       And the POWER7 processor has  
11 eight cores, right?

12            A.       That looks right, it's an  
13 eight-core processor.

14            Q.       And if we look at page 1:2 of  
15 Sinharoy, this also has two memory  
16 controllers, right?

17            A.       Just give me one minute.

18                    That looks right. On the same  
19 page, roughly three-quarters of the way down  
20 the first column, it's showing that the  
21 POWER7 has two memory controllers on each  
22 side of the chip, and that looks like what's  
23 in figure 1.

24            Q.       And when you say "figure 1,"  
25 are you referring to figure 1 of the Sinharoy

1 reference in the right column of page 1:2?

2 A. Yes.

3 Q. Okay. And if we look at that  
4 figure and the description here, there is  
5 also eight L2 caches, correct?

6 A. It looks like there are eight  
7 blocks in that figure showing L2 cache.

8 Q. And each of those blocks  
9 showing L2 cache is associated with one of  
10 the blocks -- I'm sorry.

11 Each of those blocks labeled  
12 "L2 cache" is associated with a block labeled  
13 "Core," correct?

14 A. Those are -- I think these are  
15 discussed, as I talk about in my declaration,  
16 roughly 16 to 19 of Sinharoy. But there's an  
17 L2 cache that's denoted as private, so it is  
18 for that -- private for that core, is my  
19 understanding.

20 Q. And the POWER7 also has a  
21 shared 32-megabyte L3 cache, correct?

22 A. It's on 1:16 of Sinharoy and  
23 the right-most column, and he states that --  
24 I guess about halfway down, there is the  
25 256 kilobyte L2 cache and a four-megabyte

1 local L3 region in the POWER7 processor.

2 Q. And if you go to page 1:19 of  
3 Sinharoy, do you see on the left side it  
4 says, "L3 cache"?

5 A. Yes.

6 Q. And this indicates that it's a  
7 shared 32-megabyte L3 cache, correct?

8 A. The shared 32-megabyte composed  
9 of eight four-megabyte L3 regions.

10 THE REPORTER: Of eight --

11 THE WITNESS: Four-megabyte L3  
12 regions.

13 Q. (BY MR. HUGHES) So let's go  
14 back to figure 1 in Sinharoy.

15 Do you see in the middle of the  
16 figure it says, "L3 cache"?

17 A. L3 cache and chip interconnect.

18 Q. So this is depicting the L3  
19 cache shared among the cores, right?

20 A. It looks like it's showing  
21 those eight L3 regions in that sort of  
22 central purple region. I guess it's  
23 all somewhat purple, but the L3 cache and  
24 chip interconnect, so it's each of those L3  
25 regions with their -- their own centralized

1 controller.

2 Q. If we look on the left-hand  
3 column of page 1:2, do you see -- let's  
4 see -- about -- in the second paragraph,  
5 after the bullet points, this talks about the  
6 32 megabyte shared L3 cache, correct?

7 A. That -- it talks about the  
8 technology used for the cache, eDRAM, and  
9 then this allows the large 32-megabyte shared  
10 L3 cache to be on chip.

11 Q. And Sinharoy indicates that  
12 this provides some advantages, correct?

13 A. He does.

14 Q. Including improved L3 latency  
15 by elimination of off-chip drivers and  
16 receivers?

17 A. I see that, yes.

18 Q. And improved L3 bandwidth?

19 A. And improved L3 bandwidth per  
20 core, yes.

21 Q. And less area and power  
22 compared with SRAM, right?

23 A. Yes.

24 Q. Now, when we look at figure 1,  
25 it does not depict separate cache controllers

1 for the L2 caches and the shared L3 cache,  
2 correct?

3 A. One more time.

4 Q. If we look back at figure 1, it  
5 does not depict separate cache controllers  
6 for the L2 caches and the shared L3 cache,  
7 correct?

8 A. Well, Sinharoy describes those  
9 when he talks about figure 1. They are  
10 probably one of the small blocks shown in  
11 this -- this dye photo. But at this  
12 resolution, it's probably difficult to see.

13 Q. When you say "describes those,"  
14 what do you mean?

15 A. So, for example, when I quote  
16 Sinharoy in my paragraph 34, stating, "The  
17 private 256-kilobyte POWER7 L2 cache utilizes  
18 128 byte lines and is eight-way set  
19 associative. It is comprised of a single  
20 centralized controller..." and then,  
21 "Likewise, each L3 cache region has its own  
22 controller."

23 Those descriptions come from  
24 Sinharoy, pages 18 and 19.

25 Q. Okay. Let's go to page 18.

1 When you say 18, you mean 1:18, correct?

2 A. I apologize. Yes,  
3 and 1:19.

4 Q. For ease of the record, if  
5 you're okay with it, we can just refer to the  
6 number coming after the colon, if that works.

7 A. Sure.

8 Q. Thank you.

9 So if we could go to page 18 of  
10 Sinharoy, then. And I think this is what you  
11 were just talking about where it says, "The  
12 private 256-KB POWER7 L2 cache utilizes 128  
13 byte lines and is eight-way set associative.  
14 It is comprised of a single centralized  
15 controller"; is that right?

16 A. That's right.

17 Q. Now, if we can go to  
18 paragraph 36 of your declaration, which was  
19 Exhibit 1 to this deposition, you opined here  
20 that, "Each core's L2 cache has its own  
21 controller. There is no indication that the  
22 separate controllers are distributed portions  
23 of one cache controller for the entire L2 and  
24 L3 cache hierarchy."

25 Do you see that?

1 A. Yes.

2 Q. What do you mean by "own  
3 controller"?

4 A. That, for example, one of the  
5 L2 private caches has its own cache  
6 controller. Similarly, a separate L2 cache  
7 for a different core has -- a private L2  
8 cache has its own cache controller.

9 Q. And do you mean that these are  
10 physically separate controllers?

11 A. That these are separate  
12 controllers and I would say they are going to  
13 be physically separate in the sense that they  
14 are comprised of their own logic blocks and  
15 logic cells that implement the cache  
16 controller for that private L2 or that  
17 particular private L2 or that instance.

18 Q. If we look at the right-hand  
19 side of that page, do you recall Sinharoy  
20 discussing read/claim, or RC machines?

21 A. Yes.

22 Q. And if we look at the fourth  
23 paragraph down on Page 18, the RC machines in  
24 Sinharoy are divided into two classes, right?

25 A. I see that, yes.

1           Q.       And the first class includes a  
2       set of eight fully functional RC machines  
3       that are incorporated into the L2 cache  
4       controller and manage core fetches and stores  
5       that hit the L2 cache, right?

6           A.       I see that, yes.

7           Q.       And the second class includes a  
8       set of 24 more energy-efficient lightweight  
9       RC machines that are incorporated into the L3  
10      cache controller and manage prefetches and  
11      stores that miss the L2 cache. These  
12      lightweight RC machines stage data through  
13      the L3 cache," and it indicates, "Will be  
14      described more fully in the section on L3  
15      cache."

16                   Do you see that?

17          A.       I do.

18          Q.       So Sinharoy is indicating that  
19      these are three machines of two separate  
20      classes that perform different functions,  
21      right?

22          A.       So he says they are divided  
23      into the two classes; one, the first one,  
24      numerical one, is used for L2 -- in L2 cache  
25      controller -- or the L2 cache controller; and

1        then the second one are targeted for  
2        functionality for an L3 cache controller.

3            Q.        And the first class manages  
4        core fetches and stores that hit the L2  
5        cache, right?

6            A.        That's part of what it says,  
7        yes.

8            Q.        Okay. And if we go to -- just  
9        turn to the next page, page 19, if we look at  
10       the first full paragraph, Sinharoy indicates  
11       that there is a symbiotic relationship  
12       between the fully functional L2 RC machines  
13       and the lightweight L3 RC machines, right?

14          A.        Right, because of the  
15       relationship, what he calls a tight coupling,  
16       between a given L2 cache and its  
17       corresponding local L3 and the  
18       interrelationship between them.

19          Q.        So as part of that  
20       interrelationship, the L2 RC machines and the  
21       L2 cache controllers and the L3 RC machines  
22       and the L3 cache controllers work together,  
23       right?

24          A.        I would say that the L2 level  
25       are RC machines and the L3 R machines --

1 L3 RC machines have a relationship in terms  
2 of data being a victim from one cache and  
3 perhaps being placed into another cache and  
4 things going back and forth.

5 So it sounds like he's  
6 describing they are used to better manage  
7 capacity in the various caches and  
8 performance and things like that.

9 Q. And this is related to cache  
10 coherence as well, correct?

11 A. It looks like that's some of  
12 what he's saying in the next paragraph in the  
13 sense if something can move from the  
14 four-megabyte local L3 region to a  
15 256-kilobyte L2 instead of invalidating the  
16 L3, so that would be coherence related.

17 And so the various cache  
18 controllers are going to move that data back  
19 and forth and do the related bookkeeping.

20 Q. And those various cache  
21 controllers include the L2 cache controllers  
22 and the L3 cache controllers as well,  
23 correct?

24 A. It sounds like he's saying for  
25 this scenario, there is an L2 controller for

1       that respective L2 private cache and there is  
2       an L3 controller for that L3 four-megabyte  
3       region.

4               Q.       And those two sets of  
5       controllers together are what's going to  
6       perform those -- I believe what you said were  
7       some of the caching operations to move the  
8       data?

9               A.       In the limited scenario of a  
10      cache line moving from this particular L3's  
11      line up to its -- the L2 cache above that and  
12      moving the cache line to the L2.

13              Q.       That's one example of a  
14      scenario that Sinharoy gives, correct?

15              A.       That's correct.

16              Q.       That's not the only -- Sinharoy  
17      doesn't limit it to being the only operation,  
18      right?

19              A.       Right, and I talk about that in  
20      my declaration. For example, if data in a  
21      given L3 cache region needs to go somewhere  
22      else in the system, how the logic performs  
23      that and different cache controllers perform  
24      that functionality.

25              Q.       If we can turn to page 19 of

1       Sinharoy.

2               A.       Okay.

3               Q.       Do you see the heading, "L3  
4       Cache"?

5               A.       Yes.

6               Q.       So under that, do you see where  
7       it states that each -- where it says, sorry,  
8       "A given L3 region comprises a single  
9       centralized controller"?

10              A.       Yes.

11              Q.       Can we go to paragraph 36 of  
12       your declaration as well? Let me know when  
13       you're there.

14              A.       Okay.

15              Q.       And do you see where you opine  
16       that each core's L3 region have its own  
17       controller, right?

18              A.       Yes, about the third line down.

19              Q.       And going from page 18 to  
20       page 19 of your declaration, you also cite a  
21       paragraph from Sinharoy that opined that the  
22       read request is already missed in both of the  
23       cores' L2 and L3 caches, but before it is  
24       transferred to main memory the miss is  
25       broadcast to other cores' L2 caches and L3

1 cache regions, right?

2 A. Yes.

3 Q. Now, the quoted portion from  
4 Sinharoy, it states, "Storage accesses that  
5 miss both the L2 cache and the four-megabyte  
6 local L3 region are broadcast to the  
7 coherence fabric and snooped by the memory  
8 controller, other L2 caches, possibly other  
9 L3 caches and by the seven remote  
10 four-megabyte L3 regions."

11 Do you see that?

12 A. I was listening to you, but  
13 where are you reading from?

14 Q. Sorry about that. So page 19,  
15 the fourth full paragraph in the right-hand  
16 column, it begins, "Storage accesses that  
17 miss both the L2 cache ..."

18 A. Okay.

19 Q. So did I -- did I read that  
20 correctly, that Sinharoy states that storage  
21 accesses that miss both the L2 cache and the  
22 four-megabyte local L3 region are broadcast  
23 to the coherence fabric and snooped by the  
24 memory controller, other L2 caches, possibly  
25 other L3 caches and by the seven remote

1 four-megabyte L3 regions, right?

2 A. Yes.

3 Q. Where it says "possibly other  
4 L3 caches," that means it may not be snooped  
5 by the other L3 caches, right?

6 A. It looks like it's saying in  
7 this scenario, once the access misses in that  
8 L3 or the -- sorry, the L2 or the local L3,  
9 this transaction goes out to the fabric and  
10 that snooping occurs from a memory controller  
11 going to DRAM, for example.

12 The other L2s and my  
13 understanding is the seven remote nonlocal  
14 four-megabyte L3 regions on the device.

15 Q. But where it says "possibly  
16 other L3 caches," that indicates that the  
17 other L3 caches don't need to do the snooping  
18 as well, right?

19 A. I'm not sure if that means that  
20 or something else. I don't recall discussing  
21 this. I see that it says possibly other L3  
22 caches.

23 Q. But different -- for example,  
24 when it's talking about being snooped by the  
25 memory controller, it doesn't say "possibly

1 the memory controller," correct?

2 A. Agreed, it doesn't say that.

3 Q. Same for other L2 caches, it  
4 doesn't say "possibly," right?

5 A. That's right, it doesn't.

6 Q. But for the L3 caches, it does  
7 say possibly other L3 caches, right?

8 A. It does say that, and then  
9 explicitly says without possibly -- "... and  
10 by the seven remote four-megabyte L3  
11 regions."

12 Q. Okay. So I would like to go  
13 now towards the bottom of page 19. So if we  
14 look at the last paragraph, this is  
15 discussing figure 10. And towards the bottom  
16 of the last full sentence on this page, do  
17 you see where it says, "Note that when the  
18 core and L2 associated with a given L3 region  
19 are disabled, the remaining L3 regions enjoy  
20 full access to the L3 region."

21 Do you see that?

22 A. Yes.

23 Q. So here, the other cache  
24 controllers for the remaining L3 regions are  
25 in communication with the cache controller of

1 the disabled L3 region, right?

2 A. So what it seems to be saying  
3 is if we disable the core and in addition  
4 it's local or the private L2, the -- when  
5 those two pieces associated with a given L3  
6 region are disabled, it says -- it sounds  
7 like it's saying the other L3 regions can use  
8 that first L3 region I was talking about.  
9 You might as well still use that storage.

10 Q. And they would be using the  
11 cache controller for that disabled L3 region,  
12 correct?

13 A. Well, they would each be  
14 using -- the L3 regions would each use their  
15 own cache controller and then transactions  
16 may go out over the fabric, the interconnect  
17 fabric, and then it sounds like that L3 would  
18 also use its own cache controller.

19 Q. So the -- what they call the  
20 remaining L3 controllers would be in  
21 communication with the cache controller of  
22 the disabled L3 region, correct?

23 A. One more time.

24 Q. So the cache controllers for  
25 those nondisabled L3 regions would be in

1 communication with the cache controller for  
2 the disabled L3 region, right?

3 A. So I'm not sure those words are  
4 accurate. What the reference says in the  
5 last sentence is when the core and L2  
6 associated with a given L3 region are  
7 disabled, so the core of the L2.

8 The remaining L3 regions enjoy  
9 full access to the L3 region. So the L3  
10 region with the disabled -- disabled core in  
11 L2.

12 Q. And to access that L3 region,  
13 they would interact with the cache controller  
14 of that L3 region, right?

15 A. That if transactions were  
16 coming over the interconnect fabric and  
17 arriving at that L3 region we have been  
18 talking about that was associated with a core  
19 and L2, they are now disabled, that L3 region  
20 would use its cache controller to figure out  
21 what to do.

22 Q. Where would the transactions  
23 coming over the interconnect fabric come  
24 from?

25 A. So it looks like, at least in

1 part, I think Sinharoy talks about it coming  
2 from the L3 based on how its ports are  
3 designed.

4 Q. When you say "the L3," that may  
5 be some of the non -- the other nondisabled  
6 L3s?

7 A. That if they are a missed  
8 transaction being broadcast on the  
9 coherence fabric, that it may be coming from  
10 the L3 region controller associated with  
11 another of the cores that isn't disabled.

12 Q. Okay. Can you turn to page 17  
13 of Sinharoy, and do you see table 2 on this  
14 page?

15 A. Yes.

16 Q. This is a table of the cache  
17 states for the IBM POWER7 processor, right?

18 A. That looks correct, based on  
19 that title.

20 Q. And if we look in the  
21 right-hand column, it indicates that, "As  
22 shown in Table 2, the POWER7 L2 and L3 caches  
23 support the same 13-cache-state protocol as  
24 the POWER6 design point," right?

25 A. That's right, that, I guess,

1 first full paragraph on the right-hand side.

2 Q. And the POWER6 being just the  
3 previous version of this processor?

4 A. That's -- that sounds right.  
5 There may have been minor tweaks along the  
6 way.

7 Q. Okay. And in this table, the  
8 different columns are state, description,  
9 authority, shares and scope, source data,  
10 data cast-out and scope cast-out, right?

11 A. That's right.

12 Q. And then this table is listing  
13 the different cache states and indicating  
14 what their properties are under each of those  
15 columns, correct?

16 A. Yes, these are states  
17 associated with the particular protocol that  
18 the POWER7 is supporting and the different  
19 states -- that the cache contents can be in  
20 and how -- there is a way that the cache  
21 controller goes about managing how you go  
22 between the states.

23 Q. And do you see the last entry  
24 of the table, TEN state?

25 A. Yes.

1           Q.       And then do you see in the  
2 shares and scope column, it says, "Yes,  
3 local," correct?

4           A.       Yes.

5           Q.       What does "yes, local" mean?

6           A.       Based on that same page 1:17,  
7 first full paragraph on the right, maybe  
8 eight or nine lines from the bottom, it says,  
9 "If a given core's L2 cache or local L3  
10 region owns a copy of the targeted line," to  
11 one strip in the cache, and it says, "(i.e.,  
12 holds the line in an M, ME ... or TEN cache  
13 state), the data will be installed into the  
14 local L3 region."

15          Q.       Okay. And on the TEN state,  
16 under description, it says, "Formerly ME, now  
17 shared," correct?

18          A.       Yes.

19          Q.       And then shares and scope, we  
20 agreed it said, "Yes, local," correct?

21          A.       Yes.

22          Q.       And could this mean that the  
23 cache line has shared copies, but all are  
24 local?

25                   MR. FAHMI:    Objection, form.

1                   THE WITNESS: It looks like on  
2                   the description of TEN, it's saying,  
3                   "Formerly ME, now shared," and ME,  
4                   about halfway up, says, "Exclusive,"  
5                   and shares and scope is, "No." And  
6                   TEN is now described as, "Formerly ME,  
7                   now shared," and saying it's local.

8                   So it seems to be, based on the  
9                   description of that paragraph, local  
10                  to that L3 region.

11                Q.           (BY MR. HUGHES) So is it local  
12                  to that L3 region and shared?

13                A.           That may be what it's saying,  
14                  that perhaps it used to be exclusive when it  
15                  was ME and not -- has a "No" in the shares  
16                  and scope section, and now it's saying,  
17                  "Formerly ME, now shared," and it's saying,  
18                  "Yes, local."

19                So there may be, perhaps,  
20                  unmodified copies shared in other L3 cache  
21                  regions in the system.

22                Q.           Do you see the state T,  
23                  described as, "Formerly MU, now shared"?

24                A.           Yes.

25                Q.           In the shares and scope column

1       there Sinharoy states, "Yes, probably  
2       global," correct?

3               A.       Yes.

4               Q.       And for the TEN state, that  
5       column had, "Yes, local," correct?

6               A.       Correct.

7               Q.       If a cache line is in the TEN  
8       state, are other caches snooped?

9               A.       I don't know that it says here  
10       one way or the other.

11              A.       It's pretty -- so usually there  
12       is, you know, a couple-hundred page document  
13       that describes how these various states work  
14       in sort of the broader memory system. It  
15       seems to be just giving a very high level  
16       summary here.

17                      MR. HUGHES: Can we go off the  
18       record?

19                      THE VIDEOGRAPHER: Going off  
20       the record. The time is 11:12.

21                      (Recess from 11:12 a.m. to  
22       11:14 a.m.)

23                      THE VIDEOGRAPHER: Back on the  
24       record. The time is 11:14.

25                      MR. HUGHES: Thank you,

1 Dr. Brogioli. We don't have any  
2 further questions.

3 THE WITNESS: Okay.

4 MR. FAHMI: I just have a  
5 couple of questions, Dr. Brogioli.

6 EXAMINATION

7 BY MR. FAHMI:

8 Q. Do you have the '895 patent  
9 with you?

10 A. Yes.

11 Q. Do you recall discussing the  
12 '895 patent earlier today with Mr. Hughes?

13 A. Yes.

14 Q. And do you recall Mr. Hughes  
15 asking you to look at figure 6 and answer  
16 some questions?

17 A. I do.

18 Q. If a person of ordinary skill  
19 in the art were reviewing the '895 patent,  
20 would that person of ordinary skill in the  
21 art look to the text of the patents to  
22 understand how to interpret the figures?

23 A. Yes, they would.

24 Q. Referring -- do you recall  
25 Mr. Hughes asking you if the structure of a

1        caching agent was shown in the '895 patent?

2            A.        I do.

3            Q.        If you would take a look at  
4        column 1, lines 43 to 44, it indicates  
5        figure 2 is a block diagram of a caching  
6        agent in accordance with one embodiment or an  
7        embodiment of the present invention.

8            Do you see that?

9            A.        Yes.

10          Q.        Figure two is also discussed in  
11        column 2, beginning about line 41.

12          Do you see that?

13          A.        Yes.

14          Q.        In your opinion, does figure 2  
15        of the '895 patent show the structure of a  
16        caching agent?

17          A.        That looks right. It goes on  
18        to talk about logic being interposed between  
19        one or more cores, et cetera.

20                  MR. FAHMI:    I don't have any  
21        other questions.

22                  MR. HUGHES:   Okay.

23                  THE VIDEOGRAPHER:   This  
24        concludes the deposition of  
25        Dr. Michael Brogioli.   Going off the

1 record. The time is 11:17.

2 THE REPORTER: Mr. Fahmi, would  
3 you like a rough draft?

4 MR. FAHMI: No, I don't think  
5 it's necessary. Thanks.

6 (Proceedings concluded at  
7 11:17 a.m.)

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UNITED STATES DISTRICT COURT  
NORTHERN DISTRICT OF CALIFORNIA

MERCEDES-BENZ USA )  
LLC, )  
Petitioner, )  
 ) IPR2023-01344  
VS. ) US Patent No. 9,575,895  
 )  
DAEDALUS PRIME LLC, )  
Patent Owner. )

REPORTER'S CERTIFICATION OF THE ORAL  
DEPOSITION OF MICHAEL C. BROGIOLI, PhD  
SEPTEMBER 4, 2024

I, Donna Wright, a Certified Shorthand  
Reporter and Notary Public in and for the  
State of Texas, hereby certify to the  
following:

That the witness, MICHAEL C. BROGIOLI,  
PhD, was duly sworn by the officer and that  
the transcript of the oral deposition is a  
true record of the testimony given by the  
witness;

That the original deposition was  
delivered to Mr. Tarek Fahmi;

That a copy of this certificate was  
served on all parties and/or the witness  
shown herein on \_\_\_\_\_;

I further certify that pursuant to FRCP  
Rule 30(3) that the signature of the deponent:

1           \_\_X\_\_ was requested by the deponent or  
2 a party before the completion of the  
3 deposition and that the signature is to be  
4 before any notary public and returned within  
5 30 days from date of receipt of the  
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7 Changes and Signature Page contains any  
8 changes and the reasons therefore:

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10 or a party before the completion of the  
11 deposition.

12           I further certify that I am neither  
13 counsel for, related to, nor employed by any  
14 of the parties or attorneys in the action in  
15 which this proceeding was taken, and further  
16 that I am not financially or otherwise  
17 interested in the outcome of the action.

18           Certified to by me on this, the 8th  
19 day of September, 2024.

20  
21 

22 DONNA WRIGHT, Texas CSR 1971  
23 Expiration Date: 11/30/24  
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Firm Registration No. 571

1 Tarek Fahmi, Esq.

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3 September 8, 2024

4 RE: Mercedes-Benz USA LLC v. Daedalus Prime LLC  
5 9/4/2024, Michael C. Brogioli , PhD (#6880939)

6 The above-referenced transcript is available for  
7 review.

8 Within the applicable timeframe, the witness should  
9 read the testimony to verify its accuracy. If there are  
10 any changes, the witness should note those with the  
11 reason, on the attached Errata Sheet.

12 The witness should sign the Acknowledgment of  
13 Deponent and Errata and return to the deposing attorney.  
14 Copies should be sent to all counsel, and to Veritext at  
15 cs-midatlantic@veritext.com.

16 Return completed errata within 30 days from  
17 receipt of testimony.

18 If the witness fails to do so within the time  
19 allotted, the transcript may be used as if signed.

20  
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22 Yours,

23 Veritext Legal Solutions  
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Mercedes-Benz USA LLC v. Daedalus Prime LLC

Michael C. Brogioli, PhD (#6880939)

E R R A T A S H E E T

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REASON\_\_\_\_\_

Michael C. Brogioli, PhD

Date

Mercedes-Benz USA LLC v. Daedalus Prime LLC

Michael C. Brogioli, PhD (#6880939)

ACKNOWLEDGEMENT OF DEPONENT

I, Michael C. Brogioli, PhD, do hereby declare that I have read the foregoing transcript, I have made any corrections, additions, or changes I deemed necessary as noted above to be appended hereto, and that the same is a true, correct and complete transcript of the testimony given by me.

\_\_\_\_\_  
Michael C. Brogioli, PhD

\_\_\_\_\_  
Date

\*If notary is required

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\_\_\_\_\_ DAY OF \_\_\_\_\_, 20\_\_\_\_.

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| <b>0</b> 36:14 61:1<br><b>05</b> 28:13<br><b>080</b> 11:24                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <b>19</b> 39:7 40:2<br>65:16 68:24<br>72:9 74:25<br>75:20 76:14<br>78:13                                                                                                                                                                                                                                  | <b>2150</b> 2:13<br><b>22</b> 40:8,11,22<br>41:3,12 57:5<br>58:2                                                                                                                                                                                                                                                          | <b>4</b>                                                                                                                                                                                                                                                                                |
| <b>1</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | <b>19082</b> 90:21<br><b>1971</b> 90:22<br><b>1990s</b> 33:19<br><b>1998</b> 34:15                                                                                                                                                                                                                        | <b>23</b> 51:3<br><b>24</b> 71:8<br><b>2400</b> 1:19<br><b>25</b> 35:14<br><b>256</b> 65:25<br>68:17 69:12<br>73:15                                                                                                                                                                                                       | <b>4</b> 1:10,17 2:8<br>3:7,16 63:14<br>63:19 89:8<br><b>40</b> 59:6,9<br><b>41</b> 3:14 59:6,9<br>87:11<br><b>415</b> 2:10<br><b>42</b> 50:16 59:11<br><b>420</b> 2:13<br><b>43</b> 51:4 87:4<br><b>44</b> 49:6 51:21<br>87:4<br><b>45</b> 61:19<br><b>494</b> 11:25<br><b>4th</b> 4:4 |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | <b>2</b>                                                                                                                                                                                                                                                                                                  | <b>3</b>                                                                                                                                                                                                                                                                                                                  | <b>6</b>                                                                                                                                                                                                                                                                                |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | <b>2</b> 3:3,14 21:22<br>25:9 29:16<br>41:23,25 51:3<br>59:20 81:13,22<br>87:5,11,14<br><b>20</b> 40:15 93:15<br><b>2000</b> 31:23<br><b>20004</b> 2:4<br><b>2000s</b> 31:15<br><b>2002</b> 31:23<br><b>2005</b> 28:7<br><b>2007</b> 25:14,16<br><b>2010</b> 25:23<br><b>2011</b> 25:23<br><b>202</b> 2:5 | <b>3</b> 3:15 29:17<br>56:9,10 58:10<br>89:25<br><b>3.2.1</b> 58:21<br>59:24<br><b>3.2.2</b> 61:5,6,9<br>61:22<br><b>3.2.2.</b> 62:4<br><b>30</b> 23:12 45:3,9<br>45:17 47:14<br>89:25 90:5<br>91:16<br><b>300</b> 90:23<br><b>303</b> 1:18<br><b>31</b> 54:8<br><b>32</b> 34:3 65:21<br>66:7,8 67:6,9<br><b>34</b> 68:16 | <b>6</b> 47:10,13,15<br>47:23,23 48:19<br>48:20 49:5,21                                                                                                                                                                                                                                 |

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Federal Rules of Civil Procedure

Rule 30

(e) Review By the Witness; Changes.

(1) Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A) to review the transcript or recording; and

(B) if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2) Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

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THE ABOVE RULES ARE CURRENT AS OF APRIL 1, 2019. PLEASE REFER TO THE APPLICABLE FEDERAL RULES OF CIVIL PROCEDURE FOR UP-TO-DATE INFORMATION.

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