

1 UNITED STATES PATENT AND TRADEMARK OFFICE

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3 BEFORE THE PATENT TRIAL AND APPEAL BOARD

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5
6 Mercedes-Benz USA, LLC,

7 Petitioner,

8 v.

9 Daedalus Prime LLC,

10 Patent Owner.

11 * * *

12 Case IPR2023-01344

13 Patent 9,575,895

14 * * *

15
16 VIDEOCONFERENCED (BY ZOOM) DEPOSITION OF

17 ROBERT W. HORST, PH.D.

18 Bellevue, Washington

19 Wednesday, October 2, 2024

20 8:57 a.m. Pacific Daylight Time

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22

1 Pursuant to notice, pursuant to the
2 Code of Federal Regulations and
3 Federal Rules of Civil Procedure,
4 before April L. Crites, RMR, CRR, CSR, CCR,
5 and Notary Public in and for the State of Ohio.
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I N D E X
EXAMINATIONS CONDUCTED

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* * *

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11
12 * * *

1 VIDEO TECHNICIAN: Zoom will now prompt
2 you for your consent to video-record this meeting
3 for backup purposes.

4 Thank you to everyone for attending this
5 proceeding remotely, which we anticipate will run
6 smoothly.

7 Please remember to speak slowly, and do
8 your best not to talk over one another.

9 Please be aware that we're recording this
10 proceeding for backup purposes. Any off-the-record
11 discussions should be had away from the computer.
12 Please remember to mute your mic for those
13 conversations.

14 Please have your video enabled to help the
15 reporter identify who is speaking. If you are
16 unable to connect with the video, and are
17 connecting via phone, please identify yourself each
18 time before speaking.

19 We will provide a complimentary unedited
20 recording of this deposition with the purchase of
21 the transcript.

22 I apologize in advance for any

1 technical-related interruptions.

2 Thank you.

3 ///

4 ROBERT W. HORST, Ph.D.

5 of lawful age, Witness herein, having been first

6 duly cautioned and sworn, as hereinafter

7 certified, was examined and said as follows:

8 CROSS-EXAMINATION

9 BY MR. FAHMI:

10 Q Good morning, Dr. Horst.

11 This is Tarek Fahmi. I'm here

12 representing the patent owner, Daedalus Prime.

13 Can you hear me okay?

14 A Yes -- well -- audio is -- yes, now I can
15 hear you.

16 Q Great.

17 Thanks for appearing for a deposition
18 today.

19 As you know, we're here for your
20 deposition in connection with IPR2023-01344, and
21 that concerns U.S. patent 9,575,895. And you
22 provided a declaration in support of the

1 petitioner's reply in this proceeding; is that
2 right?

3 A That's right.

4 Q Okay. And it's that reply declaration
5 that we're here in today's deposition for.

6 I know you have been through deposition
7 several times. I just want to go over a couple of
8 ground rules so that we have a common understanding
9 of today's proceeding.

10 I'll be asking questions, and you'll be
11 providing answers. But if you need clarification
12 of any question -- if you didn't understand it or
13 if you didn't hear it -- we're -- we're on a video
14 link, so sometimes the audio can be garbled. If
15 you need any clarification or if you need me to
16 repeat a question, just let me know, and I'll be
17 happy to do so.

18 Is that okay?

19 A Yes.

20 Q By the same token, if I ask a question and
21 you answer it, I'm going to assume that you've
22 answered the question that I've asked.

1 Is that fair?

2 A Yes.

3 Q Do you have any materials in the room with
4 you today?

5 A Yes. I have hard copies of my
6 supplementary declaration and two of the exhibits:
7 The Sinharoy and the Tang references.

8 Q Okay. Do you have a copy of the '895
9 patent with you?

10 A I don't have that in front of me.

11 Q That's fine. If we need it, we can bring
12 it up on the screen.

13 The materials that you do have, are they
14 clean copies?

15 A Yes, they're clean.

16 Q So no annotations or notes or any other
17 marks on them?

18 A That's right.

19 Q Okay. You should feel free to refer to
20 those notes. Sometimes it's easier to look at the
21 hard copy than a copy that's on the screen.

22 If, at any point, you're reading from one

1 of those materials, I just ask that you let us know
2 that you're reading from it and where you're
3 reading from.

4 Is that okay?

5 A Yes.

6 Q Is there anyone in the room with you
7 today?

8 A No.

9 Q Just a reminder that while the deposition
10 is ongoing, and even during the break, if there is
11 one, you're not to have any communications with
12 anyone concerning the substance of your testimony.

13 Do you -- do you understand that?

14 A Yes.

15 Q Other than this videoconference, do you
16 have any side-channel communications with either
17 Mr. Hughes or Mr. Xu?

18 A No, not at this time.

19 Q If you do need to take a break during the
20 proceeding, just let us know; we'll be happy to
21 take a break. And all I would ask is that if
22 there's a question pending, that we get an answer

1 to the question before we take that break.

2 Is that okay?

3 A Yes.

4 Q Is there any reason why you can't give us
5 your full, honest, and complete testimony in this
6 matter today?

7 A No.

8 Q Did you do any preparation for today's
9 deposition?

10 A Yes. I read through the documents in
11 front of me and some of the other documents in the
12 case, like the patent itself, and I had a Zoom
13 conference with the attorneys.

14 Q Do you know how much time you spent,
15 roughly, preparing for this deposition?

16 A I didn't add it up, but it's probably less
17 than ten hours.

18 Q In terms of the materials that you have
19 with you, when is the last time you had a chance
20 to review those materials?

21 A I read through them completely yesterday
22 and looked at portions today.

1 Q I'd like to start with the Sinharoy
2 reference that's been previously marked as
3 Exhibit 1003.

4 I think you indicated that's one of the
5 materials you have a copy of with you; is that --

6 A Yeah. That's right.

7 Q Okay.

8 (Deposition Exhibit 1003, IBM POWER7
9 multicore server processor, having been previously
10 marked, was presented for purposes of
11 identification.)

12 BY MR. FAHMI:

13 Q So you recognize this exhibit as the
14 Sinharoy reference that is discussed in your reply
15 declaration; is that right?

16 A That's right.

17 Q And Sinharoy discusses a multicore
18 processor called the IBM POWER7; is that right?

19 A That's right.

20 Q And that processor has eight cores,
21 correct?

22 A Yes, each processor has eight cores.

1 Q And then there's also a multilevel cache
2 structure for that processor, correct?

3 MR. XU: Objection to the extent it
4 mischaracterizes the reference.

5 THE WITNESS: The -- it describes a
6 level 1, level 2, and level 3 caches, yes.

7 BY MR. FAHMI:

8 Q And each core has its own level 1 cache,
9 correct?

10 A That's right.

11 Q Each core also has its own level 2 cache;
12 is that right?

13 A Yes. The level 2 cache is only accessed
14 by its individual core.

15 Q Well, a level 3 cache is shared by all the
16 cores; is that correct?

17 A That's right.

18 Q If you look at page 18 of Sinharoy,
19 there's a heading, L2 Cache.

20 Do you see that?

21 A Yes.

22 Q And the second sentence under there says

1 that the L2 cache "Is comprised of a single
2 centralized controller with two address-hashed
3 cache data arrays."

4 Do you see that?

5 A I see that, yes.

6 Q So the single centralized controller, is
7 that one controller for all of the L2 caches?

8 A That's a controller that has a physical
9 partition of its control function for each L2
10 cache.

11 Q Okay. I want to make sure I understand
12 what you're saying.

13 So there's one controller for all of the
14 L2 caches, correct?

15 MR. XU: Objection to the extent it
16 mischaracterizes prior testimony.

17 THE WITNESS: The -- in my supplementary
18 report, in paragraph 12, I state that the cache
19 controllers to the L2 and L3 caches form a single
20 logical caching agent. So there's a single
21 logical caching agent but the un-structurally
22 individual cache controllers.

1 BY MR. FAHMI:

2 Q Right. So Sinharoy itself doesn't say
3 anything about a single logical controller, right?

4 It doesn't use the word "logical" at all,
5 correct?

6 A I haven't searched for that word. I don't
7 know for sure.

8 Q Right.

9 So Sinharoy actually says the L2 cache is
10 comprised of a "single centralized controller,
11 correct"?

12 A That's one sentence from the -- from the
13 reference.

14 Q Right.

15 And that single centralized controller's
16 what I'm asking about. Is that one controller for
17 all of the L2 caches?

18 A That's -- they're structurally
19 individualized cache controllers for each L2
20 cache.

21 Q Okay. Each L2 cache has its own
22 individual controller. Is that what you said?

1 A The way I phrased it in my expert report
2 is they have structurally individual cache
3 controllers.

4 Q Okay. Let's look at the next page. It's
5 page 19. And there's a heading in the left-hand
6 column, L3 Cache.

7 Do you see that?

8 A Yes.

9 Q And in the third sentence under that
10 heading, Sinharoy states that, A given L3 region
11 comprises a single centralized controller.

12 Do you see that?

13 A It says, A given L3 region comprises a
14 single centralized controller, with four address
15 hashed eDRAM cache data banks and four address
16 hashed SRAM directory banks.

17 Q First of all, what does Sinharoy mean by
18 "given L3 region"?

19 A The L3 cache is partitioned with regions
20 associated with each core. So the -- it uses the
21 term "region" to mean the portion of the L3 cache
22 that's closest to that core.

1 Q So the L3 cache is shared but each core
2 has its own assigned region; is that right?

3 MR XU: Objection to the extent it
4 mischaracterizes prior testimony.

5 THE WITNESS: Those regions are not
6 assigned, the term you used. Those are -- those
7 regions are shared among all the caches. They're
8 physically closer to one cache, but they can be
9 shared among all the cache -- all the cores.

10 BY MR. FAHMI:

11 Q Okay. And each region has its own
12 controller in the L3; is that correct?

13 A Each region has control logic that's
14 partitioned from the -- from the controller that's
15 controlling the L3 cache. So there's a portion of
16 the logic that controls each region and a portion
17 of the logic that's global to all the L3 regions.

18 Q Where does Sinharoy say there's a portion
19 that's global to all the L3 regions?

20 A There's quite a bit in my report, starting
21 at paragraph 13, that talks about different
22 functions of the L3 cache that could only be done

1 with global control, and that couldn't be done if
2 the cache controllers were completely independent
3 of each other for each of the regions.

4 Q So it's your declaration that says there's
5 a global controller, not Sinharoy; am I right?

6 MR. XU: Objection to the extent it
7 mischaracterizes prior testimony.

8 THE WITNESS: My report points to portions
9 of Sinharoy that describe functions that would
10 have to be global functions, because they couldn't
11 be done if those regions were independent.

12 BY MR. FAHMI:

13 Q But Sinharoy doesn't say there's a global
14 control, correct?

15 A Sinharoy may not use the term "global,"
16 but the full reading of Sinharoy, someone of
17 ordinary skill would understand that there is
18 global control for some of those functions.

19 Q In fact, Sinharoy says exactly the
20 opposite; that there is a single centralized
21 controller for each given L3 region; isn't that
22 true?

1 MR. XU: Objection. Asked and answered.

2 THE WITNESS: There are portions of
3 Sinharoy that discuss other parts of the L3 cache
4 other than the sentence that you quoted. And
5 those portions of Sinharoy make it clear that
6 there is some global control over the L3 cache.

7 BY MR. FAHMI:

8 Q What portions of Sinharoy are you
9 referring to?

10 A My report has several parts of Sinharoy
11 that it quotes, but one of the parts is on page
12 1:20 of Sinharoy, which says, When the associated
13 core and L2 are enabled, a number of heuristics
14 cooperate to give precedence to the associated
15 L2 cache while allowing load and capacity
16 balancing among all eight L3 regions on the chip,
17 thereby causing them to behave as a highly
18 set-associative (64-way) adaptive 32-megabyte L3
19 cache.

20 So that's an indication that there's a
21 single set-associative L3 cache.

22 Q So this paragraph that you read from is

1 indicating that the heuristics -- and I take it
2 the heuristics are the centralized controllers for
3 the L3 cache region; is that correct?

4 MR. FAHMI: Objection. Vague as to
5 "heuristics."

6 THE WITNESS: The heuristics would be part
7 of that centralized control.

8 BY MR. FAHMI:

9 Q So we established earlier that each L3
10 region has a controller, correct?

11 A Those -- that's the way you phrased it.
12 But I phrased it differently that -- that there's
13 portions of the cache control that are assigned to
14 each L3 cache.

15 Q Well, I'm just looking at Sinharoy.
16 Sinharoy says, A given L3 region has a single
17 centralized control.

18 That's on page 19, right?

19 MR. XU: Objection. Asked and answered.

20 THE WITNESS: That's the part of
21 Sinharoy -- that's a sentence from Sinharoy, but
22 there are other sentences in Sinharoy.

1 BY MR. FAHMI:

2 Q And each of those centralized controllers
3 are made up of heuristics, correct?

4 MR. XU: Objection to the extent it
5 mischaracterizes prior testimony.

6 THE WITNESS: That isn't at all what I
7 said.

8 The heuristic has to be part of
9 centralized control. The heuristics couldn't be
10 executed independently in one region without
11 knowledge of what's going on in the other regions.

12 Q So it's impossible for them to pass
13 messages back and forth to let one another know
14 what they're doing; is that what you're saying?

15 A Cache controllers, if they had to pass
16 messages between them, the cache operation would
17 be so slow it could not be usable.

18 Q So it's impossible is what you're saying?

19 A The -- someone of ordinary skill who
20 understands Sinharoy and reads -- re-reads the
21 Sinharoy reference would understand that there
22 would be some centralized control to make these

1 heuristics work.

2 Q And Sinharoy tells us that each L3 region
3 has one of those single centralized controllers;
4 isn't that right?

5 A The portion of the L3 controller that's
6 for each region is a partition of the total cache
7 controller, which includes other functions as
8 well, like the heuristics.

9 Q So what is an heuristic?

10 A An heuristic is an algorithm that performs
11 some function based on information that it has,
12 but it may not be the total information that it
13 would need to make it an optimal or -- an optimal
14 decision. It's making a good decision based on
15 the amount of information it has.

16 Q So is it fair to say that the heuristics
17 are the rules by which the cache controller
18 operates?

19 A The heuristics include some of the rules
20 that the cache controller would operate.

21 Q And each one of the controllers associated
22 with the L3 regions has its set of rules; is that

1 right?

2 MR. XU: Objection to the extent it
3 mischaracterizes prior testimony.

4 THE WITNESS: For a function like load
5 balancing, each controller could not make -- could
6 not have a rule that would do load balancing on
7 its own. The load balancing requires a global --
8 some global rules to understand what's happening
9 in the other cache regions as well.

10 BY MR. FAHMI:

11 Q So one controller couldn't ask another
12 controller, Do you have space available?

13 A A cache memory can't operate based on
14 messages passed back and forth between
15 controllers. That could -- that would not be a
16 way to make a cache operate efficiently.

17 Caches operate on a cycle or a few cycle
18 basis, a few nanoseconds. So there's no way to
19 pass messages back and forth to do something like
20 that load balancing.

21 Q Well, the caches operate slower than the
22 core itself, don't they?

1 A The caches operate at the -- at the speed
2 that's very close to the operating speed of the
3 processors. They have to be able to handle a load
4 instruction from a cache very quickly, because the
5 processor is stopped during the point that it's
6 waiting for that data to arrive.

7 Q So there's nothing preventing
8 message-passing from one controller to another,
9 correct?

10 A Well, I've studied a lot of cache
11 controllers, and I've never heard of one that
12 passes messages back and forth in a processor of
13 this class.

14 Q Other than the Sinharoy reference, did you
15 study the caches in the POWER7 processor?

16 A I have read about the POWER7 from some
17 other references as well and understand, in
18 general, how caches work.

19 Q What other references have you read
20 concerning the POWER7 processor?

21 A I read some of the -- or one of the POWER6
22 references, which describes the cache in the

1 POWER6, which is, essentially, very similar to the
2 cache in the POWER7.

3 Q Well, one of the main differences between
4 the POWER6 and the POWER7 was that the POWER7
5 moved the L3 cache on-chip; isn't that true?

6 MR. XU: Objection to the extent it
7 mischaracterizes the reference itself.

8 THE WITNESS: You'll note the cache
9 on-chip, so there's a physical difference between
10 the POWER6 and POWER7 --

11 (Audio and video difficulties.)

12 (Court reporter clarification.)

13 THE WITNESS: There's a -- physically, the
14 POWER6 and POWER7 are different because of the
15 on-chip cache. But the cache states of the POWER6
16 and POWER7 are the same, and that describes how
17 the cache operates. So the POWER6 and POWER7
18 caches operate substantially similar.

19 BY MR. FAHMI:

20 Q Which reference did you read concerning
21 the POWER6 processor?

22 A I can -- I don't have it in front of me.

1 I can look it up if you want it.

2 Q Was it noted in any of your reports?

3 A I don't recall if I noted it in the
4 reports.

5 Q Let's just focus on Sinharoy for the
6 moment and not worry about another reference.

7 Let's --

8 A Sinharoy itself references the POWER6.

9 Q It does, and that's how we know that one
10 of the differences between the POWER6 and the
11 POWER7 is moving the cache -- the L3 cache on-chip
12 in the POWER7, correct?

13 A That's how we know that. But it -- it
14 also references the POWER6 when it's talking about
15 the states, the cache states.

16 Q Those cash states are reported in the
17 table on page 17; is that right?

18 A Yes, that's the table on page 17.

19 Q And what do those states represent?

20 A Those states represent that the
21 information about the cache lines -- whether those
22 cache lines contain modified data, for instance,

1 or shared data, or invalid data, for instance.

2 Q How does the cache controller recognize
3 which state a cache line is in?

4 A There's a lookup, and there's some
5 hardware that looks up the cache state based on
6 the address of the memory reference.

7 Q So correct me if I'm wrong, but,
8 essentially, the controller would reference a set
9 of bits to understand the state of a particular
10 cache line; is that correct?

11 MR. XU: Objection to the extent it
12 mischaracterizes prior testimony.

13 THE WITNESS: The controller would
14 reference those bits to understand the cache
15 state, that's right.

16 BY MR. FAHMI:

17 Q And each time a controller wanted to
18 access a particular cache line, it would have to
19 look at those bits to know what the state of that
20 cache line is; is that true?

21 A Depending on the operation, it generally
22 needs to access that to know what to do.

1 Q That's to make sure it's not operating on
2 data that shouldn't be used; is that right?

3 A Well, there's -- and it needs to know
4 that -- that the information is valid if it's
5 reading it, or that the cache is in a state that
6 it's allowed to modify that information. So
7 there's a number of different bits of information
8 that it reads about the cache state.

9 Q One of the things it would have to know
10 about the cache line is whether or not it is
11 shared; is that correct?

12 A Yeah, it needs to know if it's shared.
13 And in the case of the POWER7, there are multiple
14 different sharing states that have different --
15 that tell the processor different things about
16 what it can do and how to manage the cache.

17 Q What does it mean when a cache line is
18 shared?

19 A It means that there is more than one core
20 that can access that cache line.

21 Q Let's go back to page 19, please. This is
22 the section on the L3 cache.

1 A Nineteen of Sinharoy, are you asking?

2 Q Yes, please.

3 A Okay. I'm there.

4 Q About midway down the page in the
5 right-hand column, there's a paragraph that
6 begins, Storage accesses that miss both the L2
7 cache and the four-megabyte local L3 regions are
8 broadcast to the coherence fabric.

9 Do you see that?

10 A Yes, I see that sentence.

11 Q What does it mean when it says a storage
12 accesses -- excuse me, a storage access misses the
13 L2 cache?

14 A It means that the memory reference is not
15 valid in that L2 cache, so that it will need to
16 access that information from a higher-level cache
17 or from memory.

18 Q And an access that misses both the L2
19 cache and the 4-megabyte local L3 region is
20 broadcast to the coherence fabric, and we're also
21 told that it's snooped by the memory controller,
22 the other L2 caches, possibly other L3 caches, and

1 by the seven remote four-megabyte L3 regions that
2 comprise the remaining 28 megabytes of the on-chip
3 L3 cache.

4 Do you see that?

5 A I see that.

6 Q So let's say that a storage access for one
7 of the cores -- let's just call it core 1 --
8 misses that core's L2 cache and its local L3
9 region. According to Sinharoy, that storage
10 access would be broadcast to the coherence fabric,
11 correct?

12 A In some cases, it's broadcast to the
13 coherence fabric. But depending on the cache
14 state, it doesn't always need to be broadcast to
15 the coherence fabric.

16 Q Well, I'm just looking at what Sinharoy
17 says, and it says that if the storage access from
18 one of the cores misses the L2 and the local L3,
19 it's broadcast to the coherence fabric.

20 Am I missing something?

21 A This is -- this is describing one case of
22 how a storage access can be handled. But there

1 are other cache states that could be handling a
2 cache miss in L2 that did not require broadcasting
3 and snooping other caches.

4 Q Well, sure; if that cache line were
5 present in the core's L3, you wouldn't need to
6 broadcast it, but that's not what this paragraph
7 is talking about, is it?

8 A The cache line -- the cache can still
9 understand that that cache line could not be valid
10 in one of those remote caches. And in that case,
11 it would not have to broadcast and snoop those
12 other caches.

13 Q Where does Sinharoy describe that?

14 A That's in Table 2, the column about
15 Sharers and Scope.

16 Q How does this Sharers and Scope column
17 tell you what you're claiming?

18 A The difference between the TE row and the
19 TEN row is that in -- if the cache is in the TEN
20 state, it knows that it's local and that it is not
21 global; it can't -- it couldn't have been modified
22 by one of the other cores. So in that case, then

1 it knows that it doesn't need to snoop any of
2 those.

3 Q So let's look at Table 2, the TE state,
4 Sharers and Scope, says: Yes, probably global.

5 Do you see that?

6 A Yes.

7 Q What does that mean?

8 A That means it's a shared cache line, and
9 there's probably some other cache that has that
10 information in it, or, at least, it's unknown if
11 there's another cache that has it, so that it has
12 to snoop to make sure that there's no other copy
13 that's been updated.

14 Q And the TEN state says, Sharers and Scope:
15 Yes, local.

16 Do you see that?

17 A Yes.

18 Q Now, that's also a shared state, right?

19 A It's shared, but in that case, it's known
20 that no other cache has modified it, so that
21 there's no need to do that snooping.

22 Q So you're saying that a cache line that

1 misses -- in other words, it's not in the cache --
2 nevertheless somehow the cache knows it doesn't
3 have to check anywhere else?

4 MR. XU: Objection to the extent it
5 mischaracterizes prior testimony.

6 THE WITNESS: If the -- if the cache -- if
7 it misses, it needs to obtain that cache line from
8 somewhere. But if it's in this state, it knows
9 that the -- it can get that from memory and that
10 no other cache is going to have that.

11 BY MR. FAHMI:

12 Q Well, if a cache access misses, then the
13 controller doesn't have any of these cache state
14 information, does it? Because the cache line
15 isn't in the cache.

16 A Can you repeat the question for me? I
17 found some other information I wanted to just
18 include in my answer.

19 Q Yeah. My question was that if a cache
20 access misses, the cache controller doesn't have
21 any of this cache state information in Table 2,
22 because that cache line is not present in the

1 cache; isn't that correct?

2 A When the memory reference misses, it
3 doesn't have the information for that cache line,
4 but it does have information for the other cache
5 lines that own -- that are held in the location
6 that needs to be replaced with the correct cache
7 line.

8 So there's a process of evicting the cache
9 line that's there, if necessary, and replacing it
10 with the memory reference that's being requested.

11 Q Okay. So I think what you're saying is
12 you agree with me; that on a cache miss -- that is
13 the information is -- the information that's being
14 requested is not in the cache -- the cache
15 controller doesn't have the state information for
16 the cache line that missed; is that right?

17 A The cache --

18 MR. XU: Objection to the extent it
19 mischaracterizes prior testimony.

20 Sorry, Dr. Horst.

21 THE WITNESS: It has the information for
22 the line to be replaced, but it doesn't have

1 the state information for the line that's being
2 accessed.

3 BY MR. FAHMI:

4 Q All right. So now let's go back to
5 page 19 in Sinharoy, and back to that paragraph
6 that we were looking at earlier.

7 Here we have the situation of an access, a
8 storage access, that misses both the core's L2
9 cache and the core's local L3 region, and that
10 access is broadcast to the coherence fabric,
11 correct?

12 A In some cases, it's broadcast to the
13 coherence fabric, but elsewhere in Sinharoy, they
14 talk about heuristics to reduce the amount of
15 broadcast to the coherence fabric as well.

16 Q For this example, in this paragraph,
17 Sinharoy's not making any qualifications. He says
18 an access that misses a core's L2 and the core's
19 local L3 is broadcast to the coherence fabric,
20 right?

21 A For this example, it broadcasts to the
22 coherence fabric.

1 Q And that broadcast is then snooped by the
2 memory controller, correct?

3 A It's snooped by the memory controller,
4 yes.

5 Q It's also snooped by the other L2 caches,
6 correct?

7 A That's correct.

8 Q It's also snooped by possibly other L3
9 caches, correct?

10 A Correct.

11 Q And it's also snooped by the seven remote
12 four-megabyte L3 regions that comprise the
13 remaining 28 megabytes of the on-chip L3 cache,
14 correct?

15 A The word "possibly" here says, Possibly
16 other L3 caches and by the seven remote
17 four-megabyte L3 regions.

18 So the writing of the sentence is not
19 clear; if the "possibly" applies to both the L3
20 caches and to the seven remote L3 regions.

21 Q Well, there's a comma. Do you see the
22 comma after "caches," before "and"?

1 Do you see that, Dr. Horst?

2 A Yes.

3 Q So that's setting up a list, right? And
4 the "possibly" isn't modifying the seven remote
5 four-megabyte L3 regions.

6 Don't you think that's correct?

7 A That's one way to interpret it.

8 It's also possible that the "possibly"
9 modifies both.

10 Q It's only possible because that's the
11 version that fits with the theory that you've
12 espoused in your declaration, correct?

13 A It's because of the other declarations in
14 Sinharoy that indicate that it doesn't always have
15 to snoop all L3 cache regions.

16 Q Where does Sinharoy say that?

17 A It's the Table 2 information that we were
18 discussing earlier.

19 Q The part we discussed about how if there's
20 a cache miss, the controller doesn't have access
21 to the state information for the cache line
22 associated with the miss; is that what you're

1 referring to?

2 A Well, there is a much longer discussion
3 than what you just paraphrased.

4 Q But that's the conclusion you came to,
5 right, is on a cache miss, a controller doesn't
6 have access to the cache line that was the subject
7 of the miss because that cache line is not in the
8 cache; isn't that true?

9 MR. XU: Objection to the extent it
10 mischaracterizes prior testimony.

11 THE WITNESS: It has access to the cache
12 line that's currently mapped to that location but
13 not to the referenced location.

14 BY MR. FAHMI:

15 Q Do you mean not to the referenced cache
16 line? I think you misspoke. I'm not trying to
17 put words in your mouth, but I think you misspoke.

18 The cache controller certainly has access
19 to the cache line, but that cache line might not
20 include the data that is the subject of the cache
21 request, right?

22 A It always has access to that cache line,

1 but that cache line might or might not be the
2 reference that's being requested.

3 Q In your declaration, you discuss the RC
4 machines that are described in Sinharoy.

5 Do you remember that?

6 A Yes.

7 Q What's an RC machine?

8 A I discuss the RC machines in paragraph 18
9 of my report.

10 The RC machine stands for the read/claim
11 machines, and they're -- they manage the core
12 fetches read-modify-write operations on behalf of
13 the cores and the core pre-fetch operations.

14 Q Are these state machines?

15 A The reference doesn't go into the details
16 on exactly how they're implemented, but they could
17 be considered state machines.

18 Q And just generally what is a state
19 machine?

20 A A state machine is a piece of logic that
21 accepts a current state of some variables and uses
22 that to determine what the next state should be of

1 those variables.

2 Q Are these different than the heuristics
3 that we discussed earlier?

4 A These could be part of the heuristics
5 we've -- we discussed earlier, but there's not a
6 clear definition of which parts of the logic the
7 heuristics affect.

8 Q If you refer to page 18 of Sinharoy, we're
9 back in the section that discusses the L2 cache.
10 And in the right-hand column, about midway down,
11 there's a discussion of the RC machines. I think
12 it begins in the paragraph that says, To further
13 reduce energy usage, the reclaim, and then in
14 parentheses, "RC machines."

15 Do you see that?

16 A Yes, I see that.

17 Q In that paragraph, it says there's a set
18 of eight fully functional RC machines that are
19 incorporated into the L2 cache controller.

20 Do you see that?

21 A Yes.

22 Q What does the L2 cache controller mean in

1 this description?

2 A That it's not clear if those eight apply
3 to a single L2 cache or that eight is spread
4 across all of the L2 caches.

5 Q Okay. And then the next item, "2", it
6 indicates that there's a set of 24 more
7 energy-efficient lightweight RC machines that are
8 incorporated into the L3 cache controller.

9 Do you see that?

10 A Yes.

11 Q In this context, do you know what's meant
12 by "the L3 cache controller"?

13 A The L2 cache controller is talking about
14 the control of -- about over all of the L3
15 regions. So it applies to all of the L3 regions.

16 Q So these 24 RC machines are shared across
17 all of the L3 cache controllers; is that correct?

18 A My understanding was that they were shared
19 among all of the L3 regions. It's not very
20 precise about exactly how those 24 machines are
21 allocated.

22 MR. XU: Tarek, I saw we are sliding over

1 one hour. When you finish your line of
2 questioning, can we take a quick break?

3 MR. FAHMI: Yeah, we can take a break
4 right now if you like.

5 Let's go off the record.

6 (A brief recess was taken.)

7 MR. FAHMI: Let's go back on the record,
8 please.

9 BY MR. FAHMI:

10 Q Dr. Horst, I'd like to turn to the Tang
11 reference. This is Exhibit 1004, previously
12 marked in this proceeding.

13 (Deposition Exhibit 1004, DMA Cache:
14 Using On-Chip Storage to Architecturally Separate
15 I/O Data from CPU Data for Improving I/O
16 Performance, having been previously marked, was
17 presented for purposes of identification.)

18 BY MR. FAHMI:

19 Q Do you have a copy of that reference with
20 you?

21 A Yes, I do.

22 Q You offered testimony concerning the Tang

1 reference as part of your declaration in support
2 of the petitioner's reply; is that right?

3 A That's right.

4 Q I'd like to turn to Figure 10. It's on
5 page 7?

6 A Yes, I have it.

7 Q Figure 10 is showing the organization of
8 Tang's "Partition-Based DMA Cache"; is that right?

9 A That's right.

10 Q How many processors are shown in this
11 diagram?

12 A There are two processors, and each of the
13 processors has N cores.

14 Q So if we look at the processor on the
15 left, as you say, there are cores zero to N,
16 correct?

17 A That's right.

18 Q And each one of those cores has an L1
19 cache that's made up of an I-cache and a D-cache;
20 is that right?

21 A That's right.

22 Q The I-cache is the instruction cache, and

1 the D-cache is the data cache, correct?

2 A Correct.

3 Q Each of the cores also has its own L2
4 cache; is that correct?

5 A That's correct.

6 Q And then shown in the dashed box below the
7 cores, is that an L3 cache?

8 A I believe that Tang calls it an LLC, the
9 "last level cache." But it is an L3 cache.

10 Q The last level cache is shared by all the
11 cores in this processor; is that right?

12 A That's right.

13 Q And the last level cache includes a set of
14 ways. It's also marked zero to N; is that right?

15 A That's right.

16 Q Is it correct that each of these ways is
17 just a portion of the cache memory?

18 A Each of those ways is a portion of the
19 cache memory where a single memory reference might
20 be stored in one of those ways.

21 Q Okay. This last level cache also has a
22 last level cache controller; is that correct?

1 A The way this diagram is shown -- in my
2 expert report, on page 14, I show that the last
3 level cache controller can include what's called
4 the cache coherence controller in this diagram and
5 the part in that dotted line above.

6 Q The part that's in the dotted line has the
7 global control logic, right?

8 A Yes, that has the global control logic in
9 that box.

10 Q And there's also an I/O data controller,
11 correct?

12 A Yes, that's also in that box.

13 Q And there's also a CPU data controller; is
14 that right?

15 A That's right.

16 Q And there are two pre-fetchers, correct?

17 A Yes, it shows that -- the pre-fetchers in
18 the diagram, also.

19 Q The I/O data controller and the
20 pre-fetcher that's above it in the diagram,
21 they're associated with ways zero through M of the
22 last level cache; is that right?

1 A Yes, that's what the shaded portions show.

2 Q And the CPU data controller and the
3 pre-fetcher that's above it is associated with
4 ways M + 1 through N; is that right?

5 A That's right.

6 Q So is it correct that the ways zero
7 through M are controlled by the I/O data
8 controller and the ways M + 1 through N are
9 controlled by the CPU data controller?

10 A There's -- those are indicating the parts
11 of the -- of the controller that correspond to
12 each of those sections. Those are -- the entire
13 control for those -- that -- those ways include
14 what's called the I/O data controller as well as a
15 portion of the global control logic.

16 Q Okay. So the ways zero through N that are
17 the I/O ways are controlled by the I/O data
18 controller and a portion of the global control
19 logic; is that correct?

20 MR. XU: Object to the extent it
21 mischaracterizes prior testimony.

22 THE WITNESS: It includes what's labeled

1 the I/O data controller and the global control
2 logic and the box below it, the cache coherence
3 controller.

4 BY MR. FAHMI:

5 Q And ways M + 1 through way N are
6 controlled by the CPU data controller, the global
7 control logic, and the cash coherence controller;
8 is that right?

9 A That's right.

10 Q And there's only one cache coherence
11 controller per processor; is that right?

12 A That's what it shows here, yes.

13 Q And that one cache coherence controller
14 communicates with each of the cores; is that
15 right?

16 A Yes, it communicates with the cores.

17 Q And the one last level cache -- and all of
18 its associated ways and controllers and
19 pre-fetchers -- communicates with each of the
20 cores; is that right?

21 A The sum of all that control logic
22 communicates with each of the cores.

1 Q If you would turn to page 11 in Tang.

2 A I don't have page numbers on my copies, so
3 can you tell me a section number?

4 Q Yes, it's Section 6. It's on the
5 penultimate page.

6 A Okay.

7 Q It's section 6, Related Work.
8 Do you see that?

9 A Yes.

10 Q In this section, one of the approaches is
11 the partitioned cache approach in the right-hand
12 column.

13 Do you see that?

14 A Yes.

15 Q And right at the end of that section, or
16 towards the end of that section, I guess -- let me
17 see if I can find it -- Tang indicates that
18 they're proposing the PBDC -- that is the
19 partitioned-based data cache -- scheme that
20 applies the column-based cache partition technique
21 to the processor last level cache.

22 It's the last -- or second-to-last

1 sentence in that section under "Partitioned Cache
2 Approaches."

3 Do you see that?

4 A Yes, I see that.

5 Q Okay. So the column-based cache partition
6 technique that he's referring to, is that the
7 segregation of the I/O ways and the CPU data ways
8 that we looked at in Figure 10?

9 A I believe that's what he's referring to
10 there.

11 Q So the partitioning is some of the ways
12 are allocated for I/O data, and the remaining ways
13 are allocated for CPU data; is that right?

14 A That's what he has proposed as one way of
15 using this cache organization, yes.

16 (Deposition Exhibit 1017, Supplementary
17 Declaration of Dr. Robert W. Horst in Support of
18 Petitioner's Reply for U.S. Patent No. 9,575,895;
19 was marked and presented for purposes of
20 identification.)

21 BY MR. GERBER:

22 Q Okay. Do you have a copy of your reply

1 declaration with you, Dr. Horst? I think it's
2 Exhibit Number 1017.

3 A This is the supplementary declaration,
4 right, you're speaking of?

5 Q Yes, that's right.

6 A Yes, I have that.

7 Q Okay. Could you turn to paragraph 9,
8 please, on page 4?

9 A Okay.

10 Q So here, paragraph 9, you say that you
11 agreed with the Board's adopted construction for a
12 single caching agent as meaning: "One caching
13 agent for the processor, which may be formed from
14 distributed portions."

15 Is that correct?

16 A That's right.

17 Q Okay. I'm going to ask the technician to
18 bring up a copy of the '895 patent on the screen.
19 This is Exhibit 1001.

20 VIDEO TECHNICIAN: One moment, please.

21 (Deposition Exhibit 1001, United States
22 Patent No. US 9,575,895 B2, having been previously

1 marked, was presented for purposes of
2 identification.)

3 MR. FAHMI: And if you wouldn't mind, can
4 we go to claim number 1, please? It's in Column 7
5 at the end of the document.

6 VIDEO TECHNICIAN: In regards to page 7?

7 MR. FAHMI: Well, it's column 7. I think
8 it's actually the last page -- or the
9 second-to-last page; I forget which.

10 There you go.

11 And claim 1 is towards the bottom of that
12 column, if we could zoom in so that it's readable
13 there.

14 BY MR. FAHMI:

15 Q Can you see that on the screen, Dr. Horst?

16 A Yes, I can read it.

17 Q Okay. At the end of claim 1, it reads,
18 Wherein the caching agent is a single caching
19 agent for the processor and includes a plurality
20 of distributed portions.

21 Do you see that?

22 A Yes.

1 Q So isn't the Board's construction for
2 single caching agent redundant when it says it's
3 one caching agent which may be formed from
4 distributed portions? Those distributed portions
5 are already cited in the claim, aren't they?

6 A The distributed portions is in the claim,
7 and it's in the Board's definition.

8 Q So just the term "single caching agent,"
9 we don't need to say formed from distributed
10 portions, because we're already told in the claim
11 a single caching agent includes a plurality of
12 distributed portions; wouldn't you agree?

13 A The Board's construction is consistent
14 with the useness claim, so I don't -- it seems
15 like it could include that or not include it. But
16 it -- it's consistent with the usage and the
17 description and the specification of the patent.

18 Q Okay. So if I substitute the Board's
19 construction in this phrase, it's going to say,
20 Wherein the caching agent is one caching agent for
21 the processor, which may be formed from
22 distributed portions for the processor and

1 includes a plurality of distributed portions?

2 Does that make sense?

3 A Yes.

4 Q So are the distributed portions
5 distributed portions of the processor or
6 distributed portions of the caching agent?

7 A That the distributed portions are of the
8 caching agent.

9 Q And you're talking about the distributed
10 portions in the claim as it reads on the page,
11 correct?

12 A It's consistent with both the way the
13 claim reads here and with the Board's definition.

14 Q Okay. Let's go back to the Board's
15 definition. Single caching agent means one
16 caching agent for the processor, which may be
17 formed from distributed portions.

18 Correct?

19 A That's the Board's definition. That's
20 right.

21 Q In that definition, read literally, it's
22 the processor that might be formed from

1 distributed portions, isn't it?

2 A I read it as it -- it's the caching agent
3 is formed from distributed portions, not the
4 processor that's formed from distributed portions.

5 Q Well, that's actually not what it says,
6 right? "Which is referring directly to the
7 processor"?

8 A One caching agent for the processor, which
9 may be formed from distributed portions.

10 So the processor doesn't have
11 distributed -- I don't believe the Board is
12 referring to the cores as distributed portions of
13 the processor. I believe it's talking about the
14 caching agent as having distributed portions.

15 Q Wouldn't it just be simpler to say that
16 single caching agent means one caching agent? And
17 then let the rest of the claim majority says: For
18 the processor and includes a plurality of
19 distributed portions.

20 Just let that part speak for itself
21 without causing this extra confusion in the
22 definition of single caching agent?

1 MR. XU: Objection. Asked and answered.

2 THE WITNESS: It sounds like you're asking
3 me to make a legal determination of --

4 BY MR. FAHMI:

5 Q No, I'm not.

6 I'm saying for you, viewing the claim from
7 the standpoint of a person of ordinary skill in
8 art, wouldn't it be simpler to just say single
9 caching agent means one caching agent?

10 A I don't see that there's a difference in
11 the way I would analyze the claim either way.

12 Q As it's written on the page, Claim 1
13 requires that each of the distributed portions of
14 the caching agent is associated with a
15 corresponding one of the plurality of cores of the
16 processor; is that correct?

17 A It says, Wherein the caching agent has a
18 single caching agent for the processor and
19 includes a plurality of distributed portions each
20 associated with the corresponding one of the
21 plurality of the cores.

22 Q A person of ordinary skill in the art

1 reading that would read it to say that there's a
2 one-to-one relationship between a distributed
3 portion of the caching agent and one of the cores
4 of the processor; is that right?

5 A You've rephrased the claim. I would use
6 the language as it's written.

7 Q Well, each associated means the one-to-one
8 relationship, right? For every core, there's a
9 distributed portion of the single caching agent.

10 Is that what the claim says?

11 A It says each associated with the
12 corresponding core.

13 So there's one caching agent or -- I -- I
14 don't want to try to rephrase the claim language.
15 I would use the claim language as it's written.

16 Q So as written, the claim literally says,
17 Each distributed portion of the single caching
18 agent is associated with one of a plurality of
19 cores, right?

20 There's -- there's -- each distributed
21 portion of the single caching agent has a
22 corresponding one of the cores.

1 That's what it says, right?

2 MR. XU: Objection to the extent it
3 mischaracterizes the claim language.

4 THE WITNESS: Again, you paraphrase the
5 claim. But there is one distributed portion of
6 the caching agent that's associated with -- out of
7 the plurality of the cores.

8 BY MR. FAHMI:

9 Q Sorry. Did you say there was one
10 distributed portion of the caching agent
11 associated with all of the plurality of cores?

12 A No. The caching agent is a single caching
13 agent, and it has a plurality of distributed
14 portions, and each of those distributed portions
15 is associated with a core.

16 Q The word "logical" doesn't appear in
17 claim 1, does it?

18 A I don't see the word "logical" in claim 1.

19 Q Okay.

20 MR. FAHMI: Thanks for your time,
21 Dr. Horst. I don't have any other questions this
22 morning.

1 MR. XU: Tarek, can we have a five-minute
2 break?

3 MR. FAHMI: Yeah. That's fine.

4 Let's go off the record.

5 (A brief recess was taken.)

6 MR. XU: Can we go on the record?

7 Dr. Horst, we have no further questions.

8 And, Tarek, we have no further questions on our
9 side.

10 MR. FAHMI: Thanks, Kyle.

11 Dr. Horst, thank you very much for your
12 time today. Appreciate it.

13 This concludes the deposition.

14 (The deposition was concluded at
15 10:35 a.m.)

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1 I, ROBERT W. HORST, Ph.D., do hereby
2 certify that the foregoing is a true and accurate
3 transcription of my testimony.

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Dated

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STATE OF OHIO)
COUNTY OF CLERMONT) §§: CERTIFICATE

I, April L. Crites, RPR, RMR, CRR, a
Notary Public within and for the state of Ohio,
duly commissioned and qualified,

DO HEREBY CERTIFY that the above-named
ROBERT W. HORST, Ph.D. was by me first duly sworn
to testify the truth, the whole truth, and nothing
but the truth.

I further certify that the adverse party was represented by counsel at the deposition.

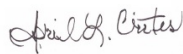
I further certify that the deposition of Robert W. Horst, Ph.D. occurred remotely on WEdnesday, October 2nd, 2024, commencing at 8:57 a.m. to 10:35 a.m.

Said testimony was reduced to writing by me stenographically in the presence of the witness and thereafter reduced to typewriting.

I FURTHER CERTIFY that I am not a relative
or attorney of either party, in any manner

1 interested in the event of this action, nor am I,
2 or the court reporting firm with which I am
3 affiliated, under a contract as defined in Civil
4 Rule 28(D).

5 IN WITNESS WHEREOF, I have hereunto set my
6 hand and seal of office at Amelia, Ohio, on this
7 8th day of October, 2024.

8
9   APRIL L. CRITES
Notary Public
State of Ohio
My Comm. Expires
October 3, 2027

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11 APRIL L. CRITES, RPR, RMR, CRR
12 NOTARY PUBLIC, STATE OF OHIO
My commission expires 10/3/2027
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