

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

Case IPR2023-01345
U.S. Patent No. 10,705,588

**PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT NO. 10,705,588
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.100 *et seq.***

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PETITIONER'S EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 10,705,588 (the "'588")
1002	The '588 Prosecution History
1003	Declaration of Robert W. Horst, Ph.D. ("Horst Decl.")
1004	Curriculum Vitae of Robert W. Horst, Ph.D.
1005	U.S. Patent No. 7,263,457 to White et al. (" <i>White</i> ")
1006	U.S. Patent No. 7,392,411 to Shakkarwar (" <i>Shakkarwar</i> ")
1007	U.S. Patent Pub. No. 2011/0022356 to Nussbaum et al. (" <i>Nussbaum</i> ")
1008	U.S. Patent No. 10,037,067 (the "'067")
1009	The '067 Prosecution History
1010	U.S. Patent No. 9,354,692 (the "'692")
1011	Chetana Keltcher, et al., <i>AMD Athlon Northbridge with 4x AGP and Next Generation Memory Subsystem</i> (1999)
1012	U.S. Patent Pub. No. 2010/0115304 to Finkelstein et al. (" <i>Finkelstein</i> ")

I. INTRODUCTION

Mercedes-Benz USA, LLC (“MBUSA,” “Mercedes,” or “Petitioner”) petitions for *inter partes* review of Claims 1-20 of U.S. Patent No. 10,705,588 (“the ’588”). (Ex-1001.) the ’588’s claimed processors, systems, and apparatuses are made up of five well-known components: first and second processing cores, graphics processing circuitry, a memory, and an interconnect between the graphics processing circuitry and the memory. Each of the cores, graphics processing circuitry, and interconnect are operable at independent frequencies, and the two cores are operable at independent voltages. Yet none of these features were new in October 2011, at the time of the alleged invention, when multi-core processing was already widespread.

By then, numerous solutions for improving processor efficiency had been disclosed that involve operating the same various components at different frequencies and voltages, as the prior art and Declaration of circuitry expert Dr. Robert Horst¹ illustrate. The first primary reference cited herein providing such a solution is U.S. Patent No. 7,263,457 (“White”) (Ex-1005), which discloses a “System and Method for Operating Components of an Integrated Circuit at Independent Frequencies and Voltages.” (White, Title.) Specifically, White

¹ The Declaration of Dr. Robert Horst (the “Horst Decl.”) is Ex-1003.

describes how processor cores, graphics circuitry, and interconnects may operate at independent frequencies and voltages depending on power and thermal requirements. (*Id.*, Abstract.) The second primary reference, U.S. Patent Publication No. 2011/0022356 (“Nussbaum”), discloses adjusting the frequencies and voltages of various components—including processing cores, a GPU, and interconnects—of a System on a Chip (SOC) to maximize performance while remaining below thermal design thresholds. (Nussbaum, Abstract, [0020].)

Nussbaum was not considered during prosecution of the ’588. And although White was submitted prior to issuance of the ’588, it was provided only in an Information Disclosure Statement (“IDS”) containing over 180 other references and was never addressed substantively during prosecution.

Each claim of the ’588 is anticipated and/or obvious over the prior art cited herein. Petitioner accordingly respectfully requests institution of *inter partes* review and cancellation of claims 1-20 of the ’588.

II. MANDATORY NOTICES (37 C.F.R. § 42.8(A)(1))

REAL PARTY-IN-INTEREST: The real parties-in-interest are Petitioner Mercedes-Benz USA, LLC; Mercedes-Benz Intellectual Property GmbH & Co. KG; Mercedes-Benz Group AG; and Mercedes-Benz AG.

RELATED MATTERS: The ’588 is the subject of the following pending actions:

- *Qualcomm Inc. v. Daedalus Prime LLC*, IPR2023-00547 (PTAB), filed on February 2, 2023 (hereinafter the “Qualcomm IPR,” previously captioned as “*Samsung Electronics Co., v. Daedalus Prime LLC*”);
- *Daedalus Prime LLC v. Mazda Motor Corp.*, Case No. 1-22-cv-01109 (D. Del.), filed August 23, 2022, and dismissed against certain defendants—including Mercedes-Benz Group AG, Mercedes-Benz AG, and Mercedes-Benz USA, LLC—on March 20, 2023; and
- *In the Matter of Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (U.S. International Trade Commission), filed September 12, 2022.

The ’588 was previously subject to the following dismissed or otherwise terminated actions:

- *Daedalus Prime LLC v. Arrow Electronics, Inc.*, Case No. 1-22-cv-01107 (D. Del.), filed August 23, 2022, and dismissed on March 1, 2023;
- *Daedalus Prime LLC v. Mazda Motor Corp.*, Case No. 1-22-cv-01108 (D. Del.), filed August 23, 2022, and dismissed on November 14, 2022;
- *In the Matter of Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (U.S. International Trade Commission), filed August 23, 2022, and terminated on February 27,

2023; and

- *Daedalus Prime LLC v. Samsung Electronics Co.*, Case No. 2:22-cv-352 (E.D. Tex.), filed September 12, 2022, and dismissed as to '588 on June 6, 2023.

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III. GROUNDS FOR STANDING (37 C.F.R. § 42.104(A))

Petitioner certifies that the '588 is available for *inter partes* review.

Petitioner is not barred or estopped from requesting *inter partes* review on the grounds herein.

IV. FEE AUTHORIZATION

Fees are submitted herewith. If additional fees are due during the proceeding, the undersigned authorizes the Office to charge them to Deposit Account No. 50-1349.

V. PRECISE RELIEF REQUESTED

The relief requested is cancellation of the challenged claims, as follows, supported by a declaration from Dr. Robert Horst (Ex-1003):

Ground	References	Claims ²	Basis
1.	White (Ex-1005)	1-4, 7, 8-11, 14-20	102/103
2.	White (Ex-1005) in view of Shakkarwar (Ex-1006)	5-6, 12-13	103

² Independent claims in **bold**.

Ground	References	Claims ²	Basis
3.	Nussbaum (Ex-1007)	1-4, 7, 8-9, 10, 11, 14-20	102/103
4.	Nussbaum (Ex-1007) in view Shakkarwar (Ex-1006)	5-6, 12-13	103

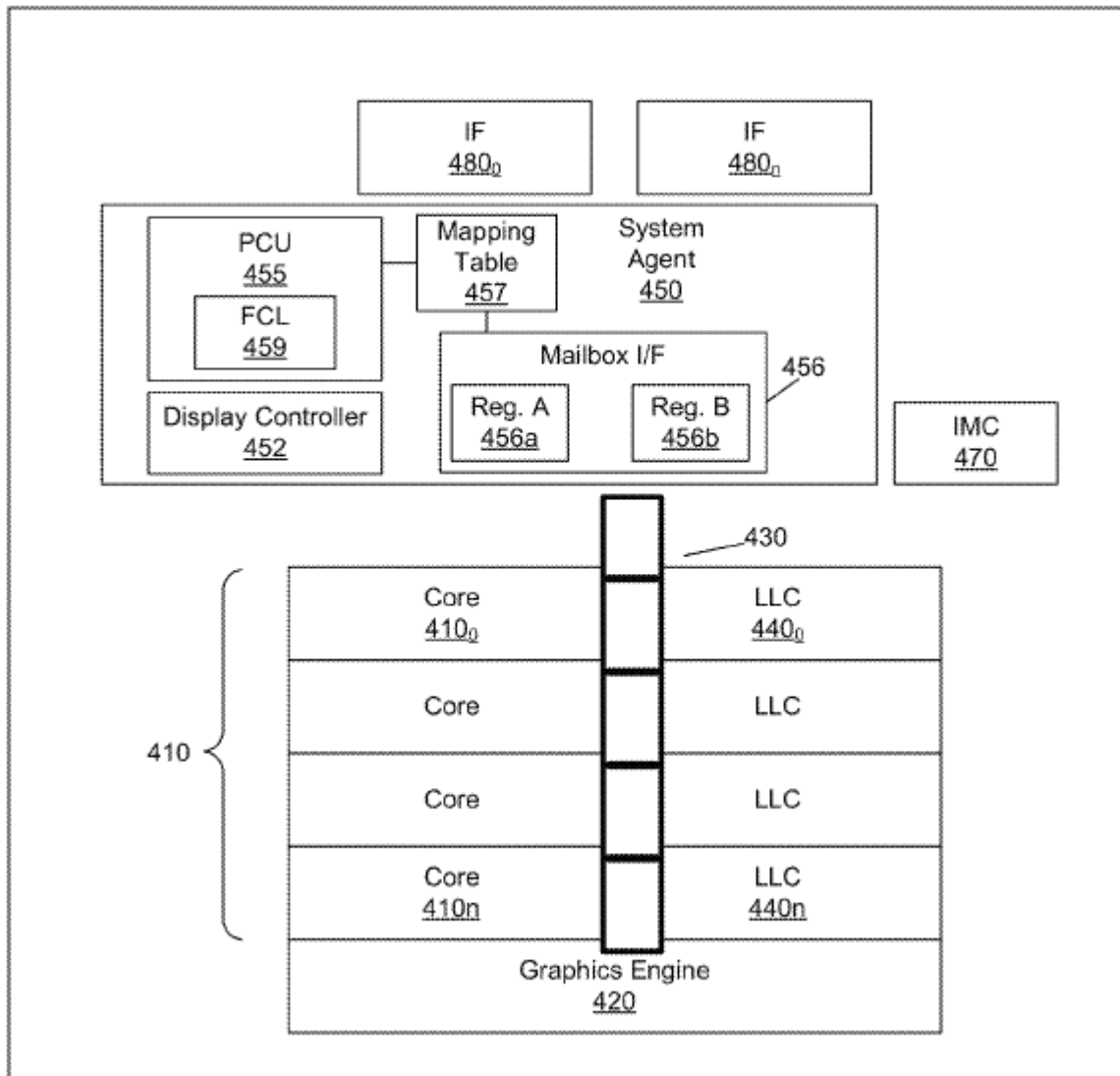
VI. THE '588

A. Overview

Independent Claims 1, 8, and 20 of the '588 recite a processor, system, and apparatus, respectively, having five basic components. The claimed processor and system have a plurality of processing cores including (1) a first core and (2) a second core, each independently operable at a first frequency and voltage and a second frequency and voltage, respectively. The claimed processor and system also include (3) graphics processing circuitry and (4) an interconnect to couple the graphics processing circuitry to (5) a system memory or memory device. The graphics processing circuitry is independently operable at a third frequency, and the interconnect is operable at a fourth frequency, wherein the third and fourth frequencies are different from the first and second frequencies. Dependent claims 2, 4-7, 9, and 11-14 additionally require power management circuitry and/or logic to cause the components to operate the respective frequencies, and dependent Claims 3 and 10 further require a cache shared by the plurality of cores.

The '588's Figure 4 illustrates elements of Claims 1 and 8. It depicts first

core 410₀, second core 410_n, and graphics engine 420, which the '588 describes as operating at different voltages and/or power. ('588, 6:11-24.) Figure 4 also shows interconnect 430, which provides a connection between the cores 410, graphics domain 420, and system agent circuitry 450 (including PCU (power control unit) 455). (*Id.*, 6:37-44.) A last level cache (LLC) is shown which is shared among cores 410. (*Id.*, 6:30-37.) And integrated memory controller (IMC) 470 is depicted, which provides an interface to a system memory such as a DRAM (not shown in Figure 4). (*Id.*, 7:20-24.)



(*Id.*, Figure 4 (annotated).)

B. Prosecution History

The '588 was filed January 16, 2019, as US16/249,103 and is related to the following patents and applications:

- US16/249,103 is a continuation of US15/381,241, filed Dec. 16, 2016, now US10,248,181;

- US15/381,241 is a continuation of US15/138,505, filed Apr. 26, 2016, now US10,037,067 (the “’067”);
- US15/138,505 is a continuation of US14/451,807, filed Aug. 5, 2014, now US9,354,692 (the “’692”); and
- US14/451,807 is a continuation of US13/282,896, filed Oct. 27, 2011, now US8,832,478.

The ’588 (US16/249,103) received a single Office Action rejection prior to allowance, in which as-issued Claims 1, 8, and 20 were rejected only because of obviousness-type double patenting over Claim 11 of the ’067. (Ex-1002, 0046-50; *see also* Ex-1008, 0013.)

The Examiner objected to as-issued claims 2 and 9 for depending from a rejected base claim but noted they would be allowable if rewritten in independent form. (Ex-1002, 0049.) With respect to these claims, the Examiner concluded that the “prior arts, cited in its entirety, or in combination, do not teach first power management circuitry and/or logic to cause the first core to operate at the first frequency and to cause the second core to independently operate at the second frequency.” (*Id.*, 0049-50.) In response, the applicant terminally disclaimed the pending claims over the ’067 and requested reconsideration. (*Id.*, 0028-0029, 0037-0039.) On March 2, 2020, the Examiner allowed all pending claims. (*Id.*, 0017-0021.)

The '067 likewise received a single Office Action rejection prior to allowance, in which as-issued Claim 11 was rejected only because of obvious-type double patenting over Claim 1 of the '692. (Ex-1009, 0151-0156.) The applicant terminally disclaimed the '067 over the '692, and the Examiner allowed all pending claims. Because the Examiner issued only obviousness-type double patenting rejections, he never identified novel elements in as-issued '588 Claims 1, 8, and 20 and '067 Claim 11 that were absent from the prior art.

C. Priority Date

The earliest possible priority date for the '588 is October 27, 2011. Petitioner takes no position in this Petition on the proper priority date for each claim of the '588. Assuming this earliest date, all prior art references asserted in this Petition are prior art.

VII. CLAIM CONSTRUCTION AND LEVEL OF ORDINARY SKILL IN THE ART

A. Claim Construction

Claims in an *inter partes* review “shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Elements in a claim containing the word “means” “create[] a rebuttable

presumption that § 112, ¶6 applies.” *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015). Under 37 C.F.R. § 42.104(b)(3) and Rule 42.104, Petitioner’s proposed constructions for these claim elements using the words “means” are below.³ All other claim terms herein are given their ordinary and customary meaning.

1. Claim 20: “means for operating a first core at a first voltage...”

Recited Function: “operating a first core at a first voltage and at a first frequency while concurrently operating a second core at a second voltage independent of the first voltage frequency and at a second frequency different from the first frequency and independently operating a graphics processor at a third frequency different from the first frequency and the second frequency”

Corresponding Structure and Equivalents: “power control unit (PCU)

³ For each means-plus-function element below, Petitioner identified the closest structure in the ’588 that relates to the recited function. But in doing so, Petitioner does not waive any argument that the ’588 does not disclose sufficient structure for performing the claimed function of each term and hereby reserves the right to raise such arguments at a future time, understanding that this is not the proper forum for the same.

355/455” and equivalents. (’588, 5:46-55, 6:45-19, Figures 3-4.)

2. Claim 20: “means for independently operating a graphics processor...”

Recited Function: “independently operating a graphics processor at a third frequency different from the first frequency and the second frequency”

Corresponding Structure and Equivalents: “power control unit (PCU) 355/455” and equivalents. (’588, 5:46-55, 6:45-19, Figures 3-4.)

3. Claim 20: “interconnect means to couple the graphics processor to a memory device...”

Recited Function: “to couple the graphics processor to a memory device, the interconnect means operable at a fourth frequency different from the first, second, and third frequencies”

Corresponding Structure and Equivalents: “interconnect 315” and equivalents. (’588, Figure 3, 5:44-50.)

B. Definition of a Person of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) of the ’588 would have had a bachelor’s degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for

experience and additional experience substituting for formal education. (Horst Decl., ¶¶26-30.)⁴

VIII. GROUNDS OF UNPATENTABILITY

A. Grounds Based on White

White was filed January 3, 2006, and issued on August 28, 2007. White is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e).

White discloses a “System and Method for Operating Components of an Integrated Circuit at Independent Frequencies and/or Voltages.” (White, Title.) White’s “operating components of an integrated circuit” include processor logic cores “configured to operate at frequencies and voltages independently of each other.” (White, Abstract.) White’s Figure 1 depicts an integrated circuit 100 having logic cores 120A and 120B, the first and second cores, and shows how common bridge logic 110 connects the integrated circuit 100 with other components, such as bus(es) 150, peripheral(s) 160, and a memory subsystem 170:

⁴ Dr. Robert Horst is an expert in electrical engineering and electronic circuit control, among other things.

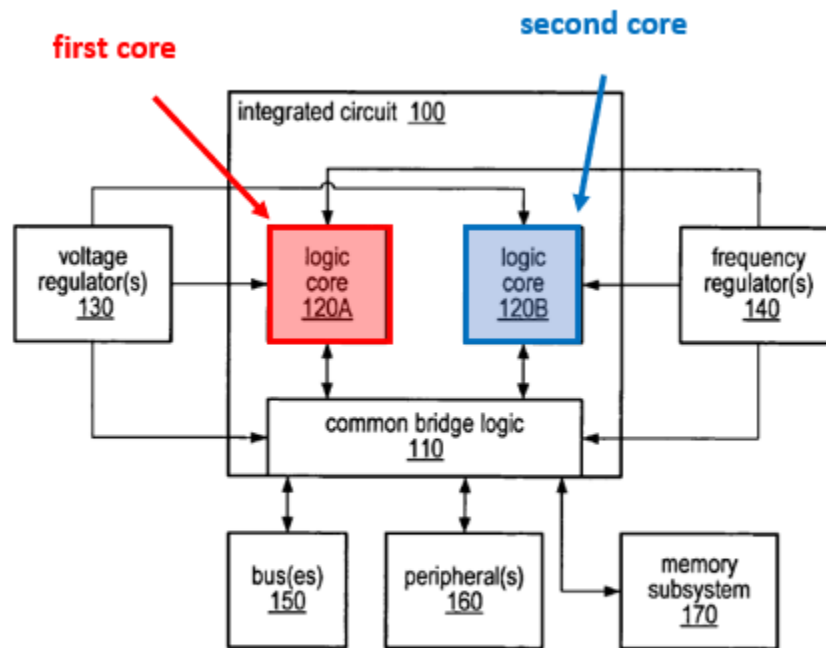


FIG. 1

(*Id.*, Figure 1 (annotated); *see also* 5:28-30, 6:41-8:58.)

White discloses power management logic 200 (Figure 2A) and temperature control logic 210 (Figure 2B) that control the frequencies and voltages of the logic cores 120 and common bridge logic 110 through voltage and frequency regulators 130, 140:

power management circuitry and/or logic

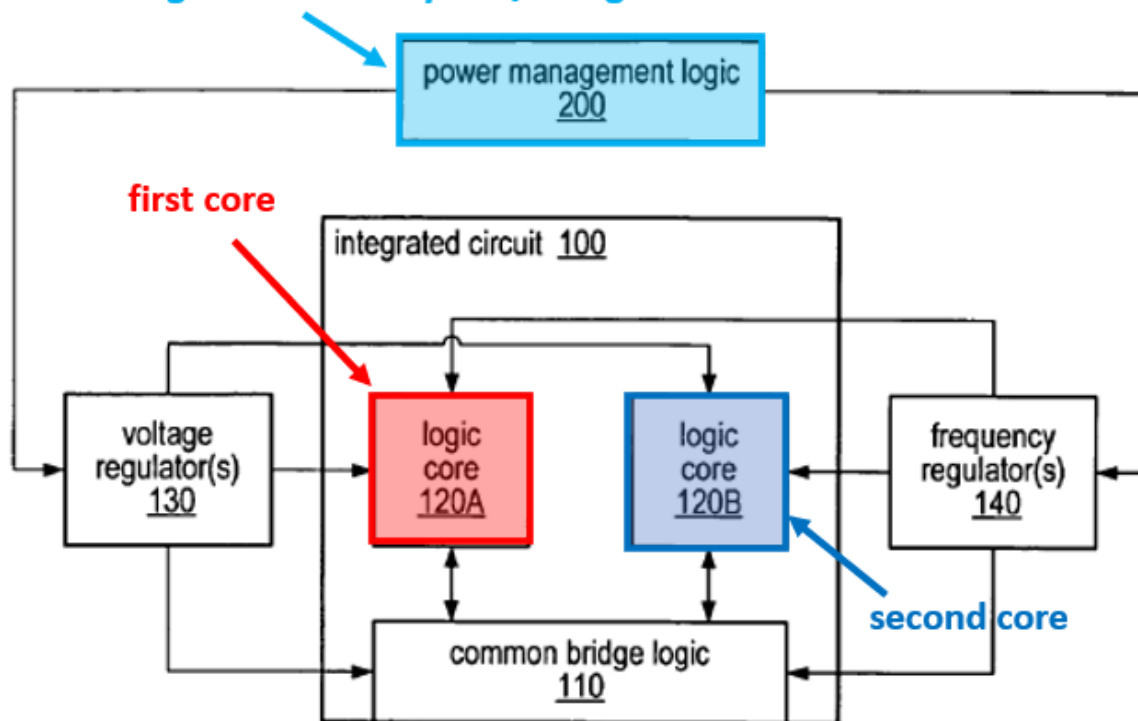


FIG. 2A

(*Id.*, Figure 2A (annotated); *see also* 5:32-35, 8:59-11:60.)

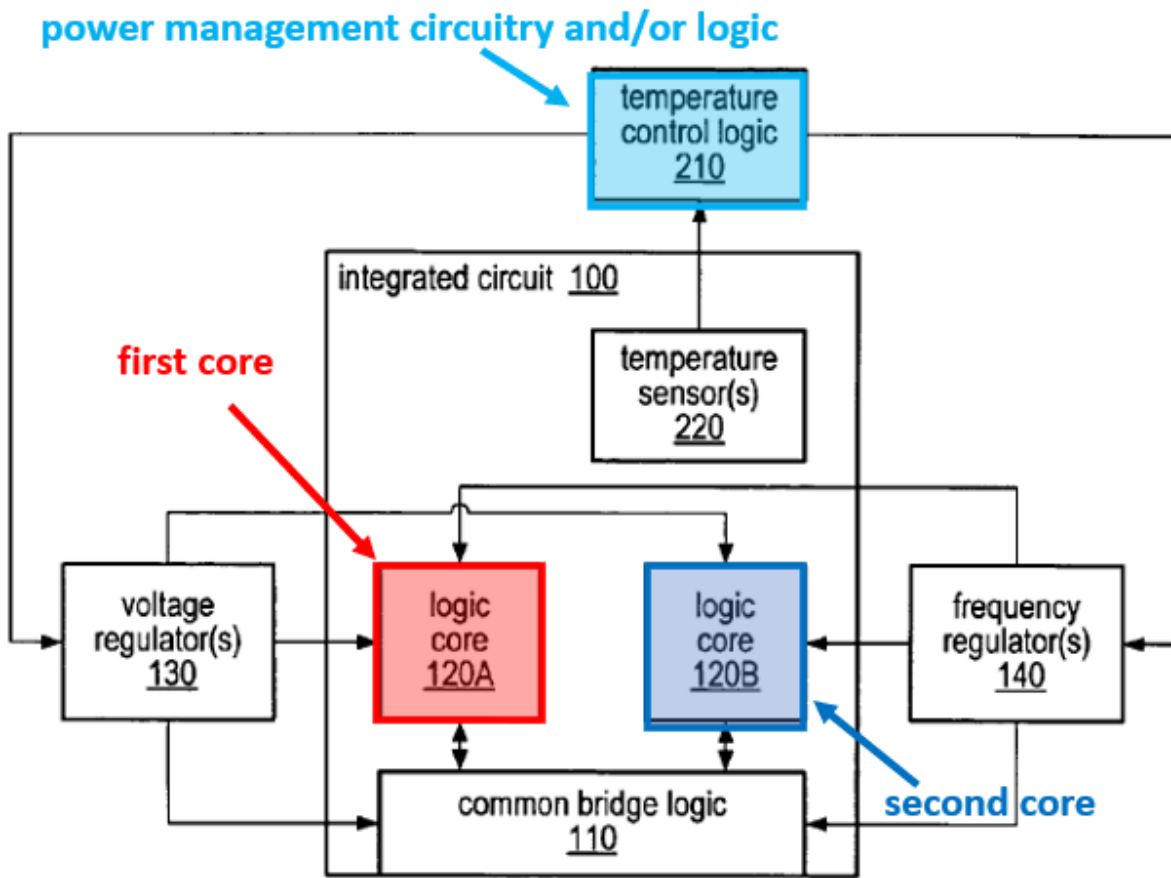
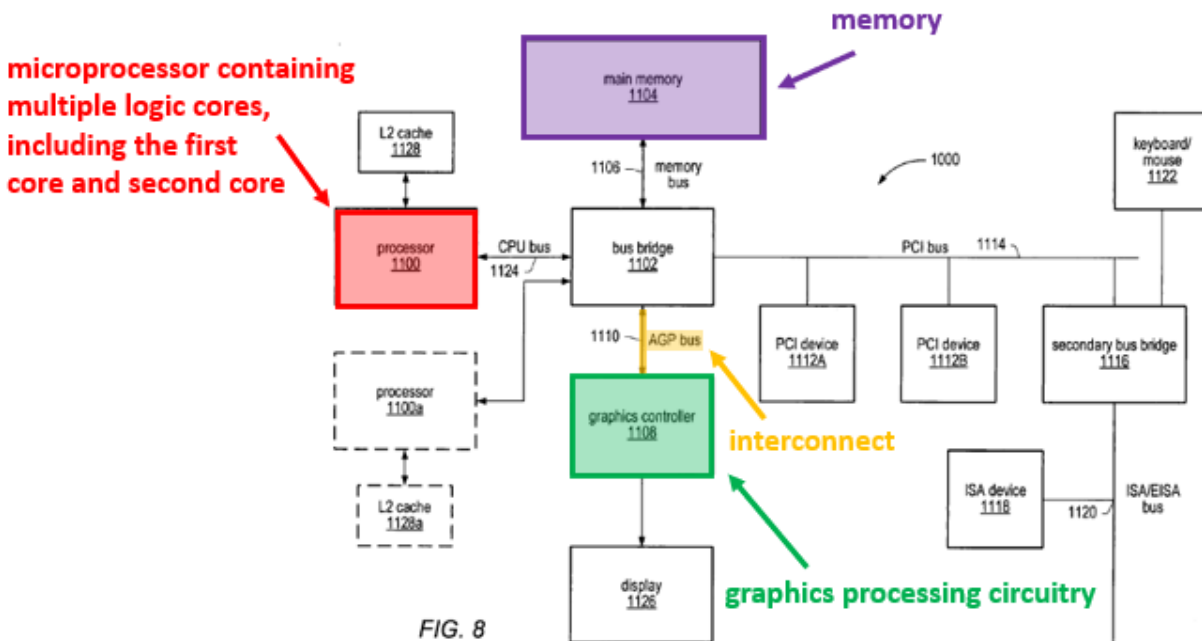


FIG. 2B

(*Id.*, Figure 2B (annotated); *see also* 5:36-39, 11:61-14:20.)

White's Figure 8 depicts an overall system having microprocessors with multiple cores 1100, graphics processing circuitry 1108, interconnect AGP (accelerated graphics port) bus 1110, memory 1104, PCI bus 1114 and ISA/EISA bus 1120 to couple to I/O devices, and various exemplary I/O devices (such as a display 1126 and keyboard/mouse 1122):



(*Id.*, Figure 8 (annotated); *see also* 24:30-26:30.) White discloses that microprocessor 1100 and graphics controller 1108 each contain multi-core integrated circuits, such as integrated circuit 100 depicted in Figures 1-2 and described above. (*Id.*, 24:33-41 (“processor 1100 may include integrated circuit 100, one or more logic cores 120, common bridge logic 110, and/or one or more temperature sensors 220, described above. Additionally, system 1000 may include power management logic 200 and/or temperature control logic 210 both of which may be configured to control or adjust the operating frequency and/or voltage for logic core(s) 120, and possible common bridge logic 110, according to various embodiments, and as described herein.”), 24:49-54 (“graphics controller 1108 may include one or more multi-core integrated circuits and each logic core within such

an integrated circuit may be configured to operate at independent frequencies and/or voltages, as described herein”); Horst Decl., ¶59.)

1. Ground 1: Claims 1, 2, 3, 4, 7-11, and 14-20 are anticipated or obvious over White

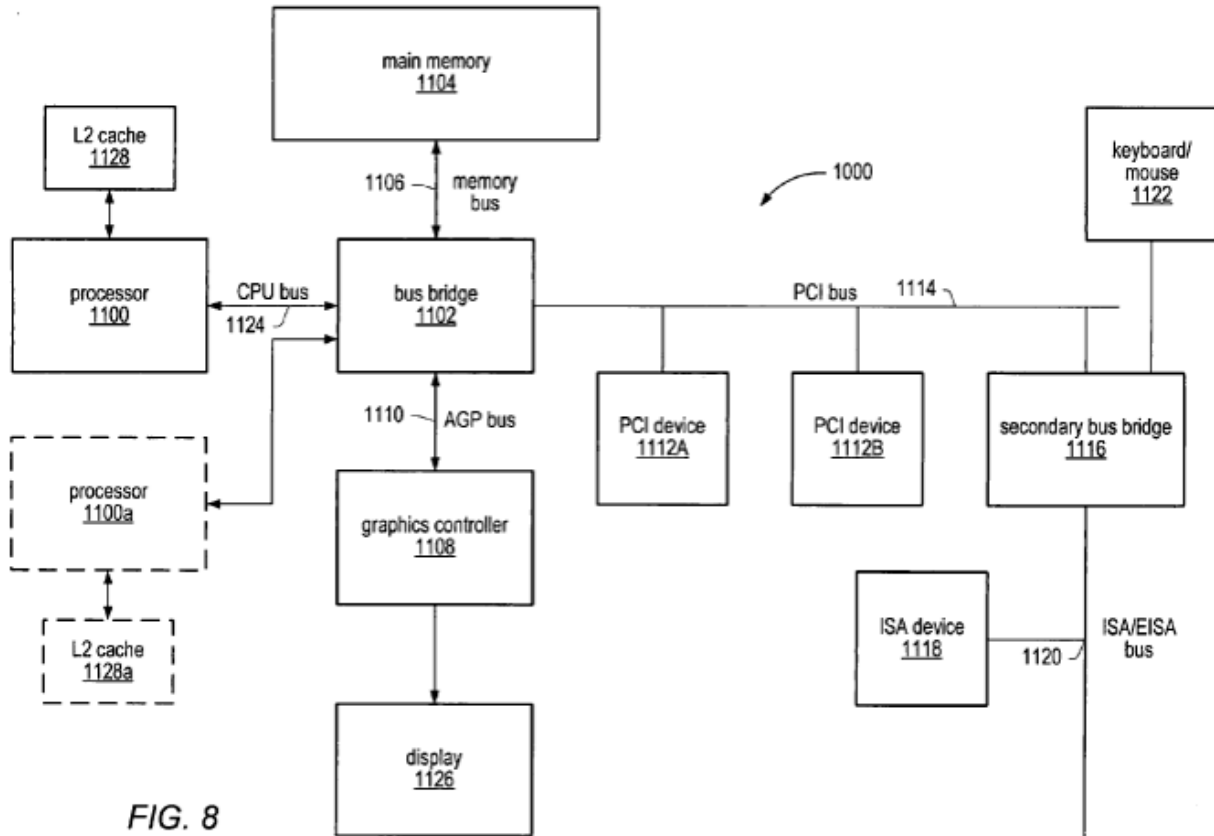
(a) Independent Claim 1

White anticipates and/or renders obvious Claim 1. (Horst Decl., ¶¶60-91.)

1[p]: A processor comprising:

White anticipates and/or renders obvious Claim 1[p]. (Horst Decl., ¶¶60-63.)

White discloses a computer processor system that includes “[m]ultiple logic cores of integrated circuits and processors...” (White, Abstract.) These integrated circuits and processors have multiple logic cores that make up the overall processor in White. (Horst Decl., ¶61.) As can be seen below, the processor of Figure 8 includes, among other components, microprocessors 1100 and 1100a, a bus bridge 1102, a main memory 1104, a graphics controller unit 1108, and caches 1128 and 1128a. (*Id.*, 24:30-26:30.)



(*Id.*, Figure 8 (annotated).)

Microprocessors 1100 and 1100a “include multiple logic cores” that are “configured to operate at voltages and/or frequencies independent of the voltages and/or frequencies at which others of the cores may operate.” (*Id.*, 24:33-36, 26:21-25.) Moreover, White discloses that these microprocessors may include the integrated circuit 100, logic cores 120, common bridge logic 110, and temperature sensors 220 from Figure 1. (*Id.*, 24:33-46, 26:18-25.) Similarly, White discloses that graphics controller unit 1108 may include “one or more multi-core integrated circuits,” with each logic core within the circuits “configured to operate at

independent frequencies and/or voltages, as described herein.” (*Id.*, 24:47-54, 6:42-46 (“an integrated circuit may include multiple logic cores, such as logic cores 120A and 120B each of which may be configured to operate at an independent voltage and frequency”)); *see also* Horst Decl., ¶62.) Integrated circuit 100 is depicted in, for example, Figure 1:

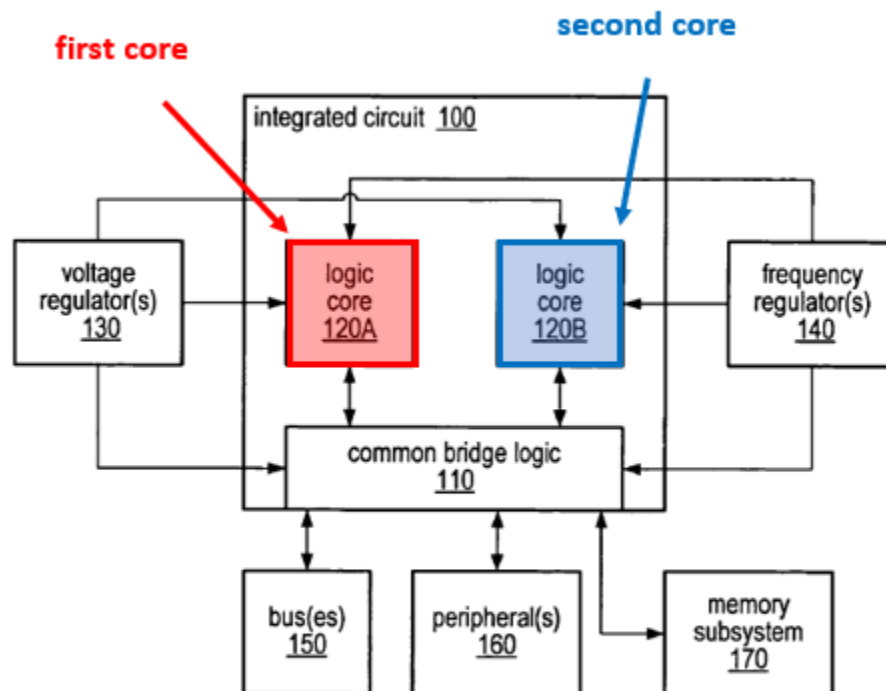


FIG. 1

(White, Figure 1 (annotated); *see also* 5:28-30, 6:41-8:58.) Integrated circuit 100 “include[s] multiple logic cores, such as logic cores 120A and 120B each of which may be configured to operate at an independent voltage and frequency.” (*Id.*, 6:42-46; *see also* 2:15-18.) Moreover, the “multi-core integrated circuit or processor

may include a common bridge or interface unit, such as common bridge logic 110, configured to communicate with the logic cores as well as with other elements or peripherals either internal or external to integrated circuit 100.” (*Id.*, 7:1-6.)

1[A]: a plurality of cores including a first core operable at a first voltage and at a first frequency, and

White anticipates and/or renders obvious Claim 1[A]. (Horst Decl., ¶¶64-71.) White discloses a plurality of cores, and in particular “multiple logic cores,” each of which “may be configured to operate at a particular voltage and frequency regardless of whether other logic cores in the processor are also operating at the same voltage and/or frequency.” (*Id.*, 2:15-22, *see also* 2:22-44, 3:8-60, 6:43-49, 7:18-22, 8:61-9:53, 13:27-14:20, 15:42-16:21, Figures 4-7, Abstract.) For example, White discloses reducing the voltage and/or frequency for an individual logic core (the first core) when higher than optimal temperature or power consumption is detected for the processor containing the logic core. (*Id.*, 3:24-45, *see also* 2:15-44 (explaining that one core could operate at a “lower” frequency and/or voltage).) White further explains that, because “the operating frequency of a logic core is related to the operating voltage of that logic core, when an operating voltage for a logic core is adjusted, such as to lower the operating temperature, the operating frequency for the logic core may also be adjusted.” (*Id.*, 3:53-57; *see also* Horst Decl., ¶67.)

White discloses a first core in Figure 1, showing logic core 120A within integrated circuit 100:

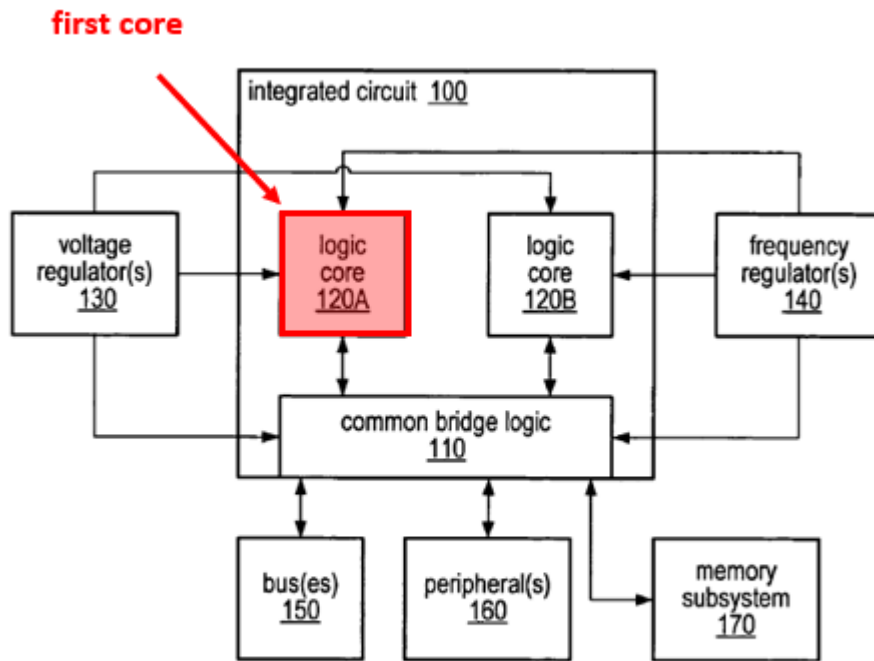


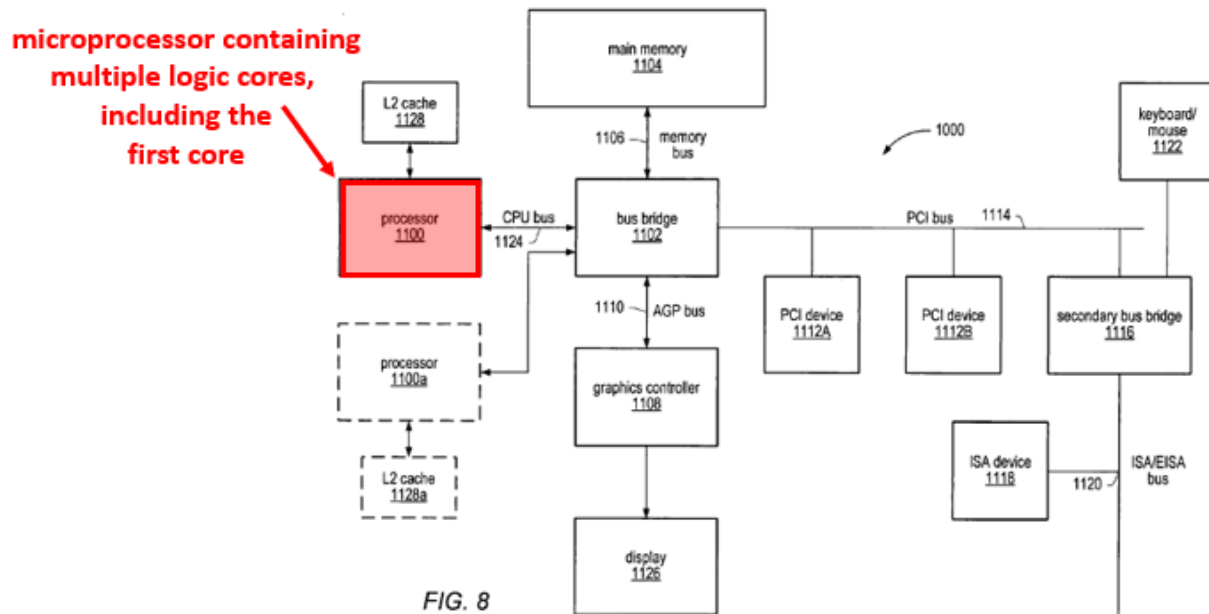
FIG. 1

(White, Figure 1 (annotated); *see also* 5:28-31, 6:41-8:58, 10:50-56, 13:27-14:20.)

White discloses that the first core, logic core 120A, can be “configured to operate at an independent voltage and frequency. In other words, each logic core may operate at a voltage and/or frequency independently from the voltage and/or frequency at which other logic cores, such as logic core 120B, may operate.” (*Id.*, 6:43-46.)

White’s Figure 8 also depicts microprocessor 1100 containing multiple logic

cores, including the first core:



(*Id.*, Figure 8 (annotated); *id.*, 24:30-26:30.) As discussed above, *see supra* Section VIII.A.1(a) (Ground 1, Claim 1[p]), microprocessor 1100 includes integrated circuit 100 as well as the one or more logic cores 120A and 120B therein. (*Id.*, 24:33-39.)

Thus, one of the logic cores in White, such as logic core 120A, is a “first core,” and as White discloses, the particular voltage and frequency at which this logic core operates would be a first voltage and first frequency. (*Id.*; *see also* Horst Decl., ¶71.)

1[B]: a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

White anticipates and/or renders obvious Claim 1[B]. (Horst Decl., ¶¶72-

77.) Because White discloses “multiple logic cores” it discloses “a second core” of a processor or integrated circuit. (White, 2:15-18; *see also* Abstract.) As with the first core, the second core in White “may be configured to operate at a particular voltage and frequency regardless of whether other logic cores in the processor are also operating at the same voltage and/or frequency.” (*Id.*, 2:19-22, 6:44-46.) For example, White discloses that, when higher than optimal temperature or power consumption is detected, the voltage and/or frequency of a logic core 120B—the second core—remains unchanged, while independently reducing the voltage and/or frequency of another logic core, 120A—the first core. (*Id.*, 13:27-14:20; *see also* 3:24-45; Horst Decl., ¶73.) White likewise discloses adjusting operating voltage and/or frequency “for one logic core to a lower level than the operating characteristics of another logic core.” (White, 9:1-6, 9:25-30; *see also* 9:13-18.) White accordingly contemplates that each logic core—such as the first and second cores—may “us[e] a different voltage level and/or clock frequency.” (*Id.*, 2:55-57; *see also* 4:11-17, 8:4-10, 10:28-32, 11:31-35.)

White discloses a second core in Figure 1, showing logic core 120B within integrated circuit 100:

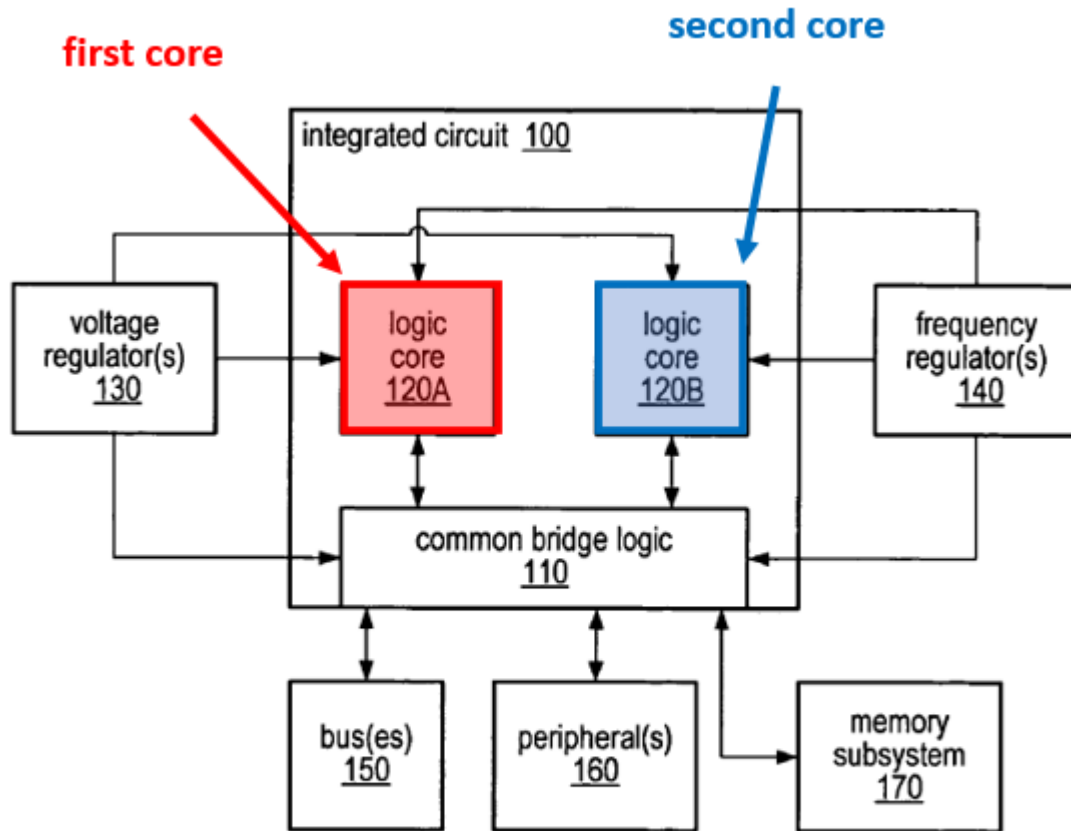
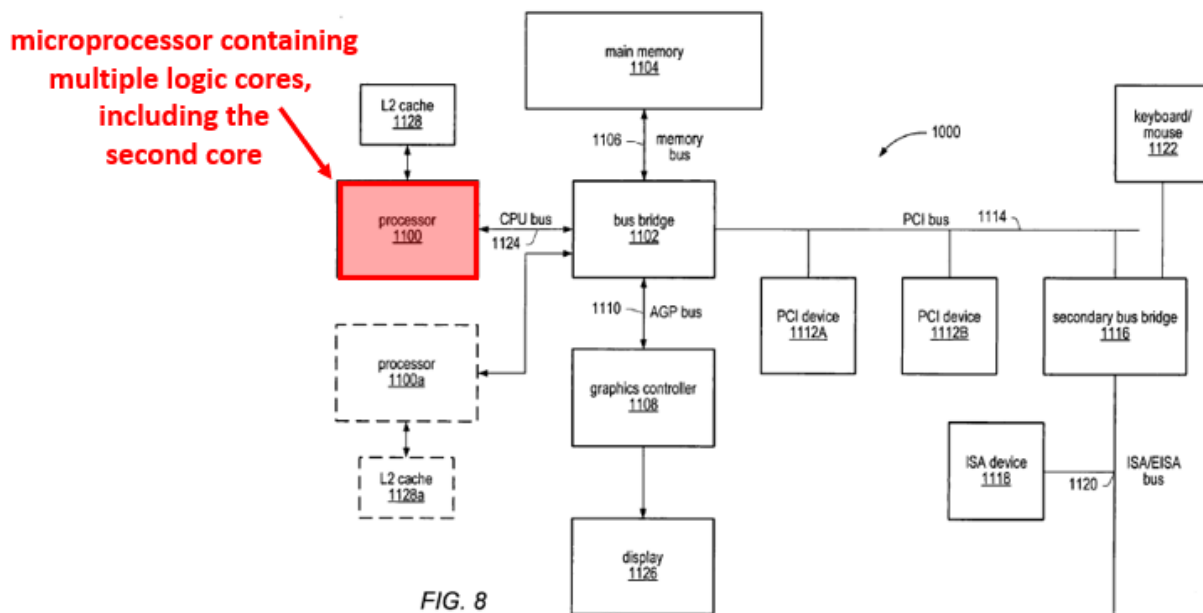


FIG. 1

(*Id.*, Figure 1 (annotated); *id.*, 5:28-31, 6:41-8:58, 10:50-56, 13:27-14:20.) White discloses that logic core 120B, the second core, can operate independently from each other logic core. (*Id.*, 6:43-46; Horst Decl., ¶¶74-75.)

White's Figure 8 also illustrates microprocessor 1100 containing multiple logic cores, including the second core:



(*Id.*, Figure 8 (annotated), 24:30-26:30.) As discussed above, *see supra* Section VIII.A.1(a) (Ground 1, Claim 1[p]), microprocessor 1100 includes integrated circuit 100 as well as the one or more logic cores 120A and 120B. (*Id.*, 24:33-39.)

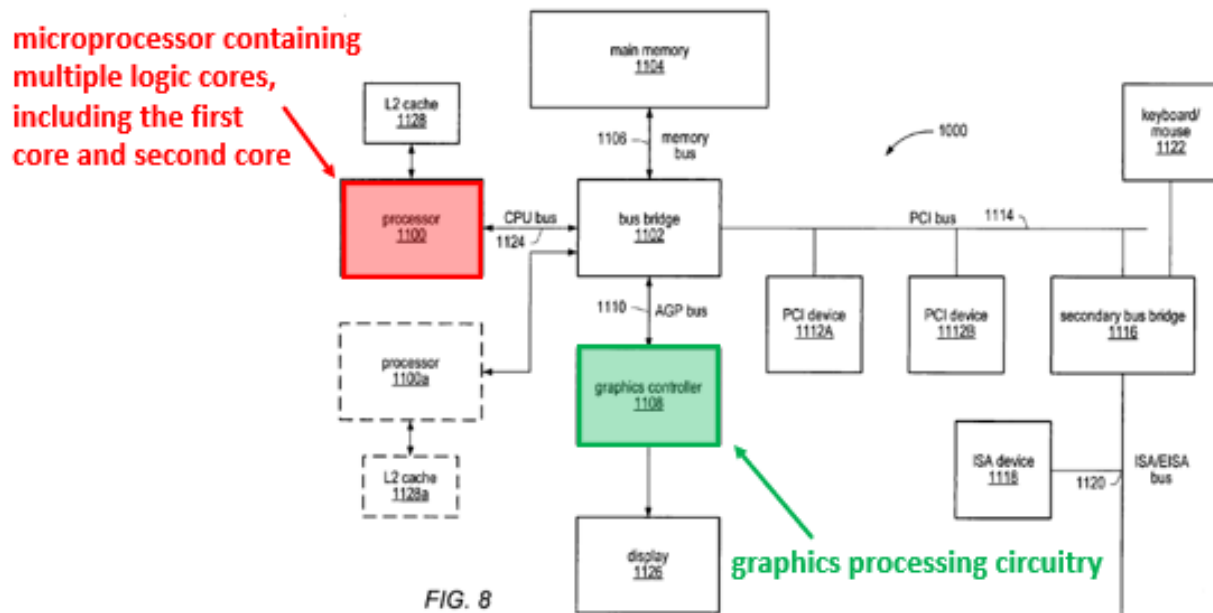
Thus, one of the logic cores in White, such as logic core 120B, is a “second core,” and as White discloses, the particular voltage and frequency at which this logic core operates would be a second voltage and second frequency. (*Id.*; *see also* Horst Decl., ¶77.)

1[C]: graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and

White anticipates and/or renders obvious Claim 1[C]. (Horst Decl., ¶¶78-81.) White discloses that the processor may include graphics processing circuitry

(e.g., “graphics controller 1108”). (White, 24:47-54.) Graphics controller 1108 is circuitry that performs graphics processing and operations, such as “control[ing] the rendering of text and images on a display,” and “may embody a typical graphics accelerator generally known in the art to render three-dimensional data structures that can be effectively shifted into and from main memory.” (*Id.*, 25:64-26:2; Horst Decl., ¶79.)

Graphics controller 1108 is coupled to the plurality of cores—*e.g.*, the aforementioned first and second cores such as logic cores 120A and 120B in processor 1100—through CPU bus 1124, bus bridge 1102, and AGP bus 1110. (*Id.*, 25:1-23.)



(*Id.*, Figure 8 (annotated) (illustrating graphics controller 1108 coupled through AGP bus 1110, bus bridge 1102, and CPU bus 1124 to microprocessor 1100,

which includes first core 120A and second core 120B), 25:21-23 (“Bus Bridge 1102 may provide an interface between microprocessor 1100, main memory 1104, graphics controller 1108, and devices attached to PCI bus 1114.”), 25:3-4 (“[G]raphics controller 1108 is coupled to Bus Bridge 1102 through an AGP bus 1110.”), 25:11-12 (“[M]icroprocessor 1100 may be coupled to Bus Bridge 1102 through a CPU bus 1124”).)

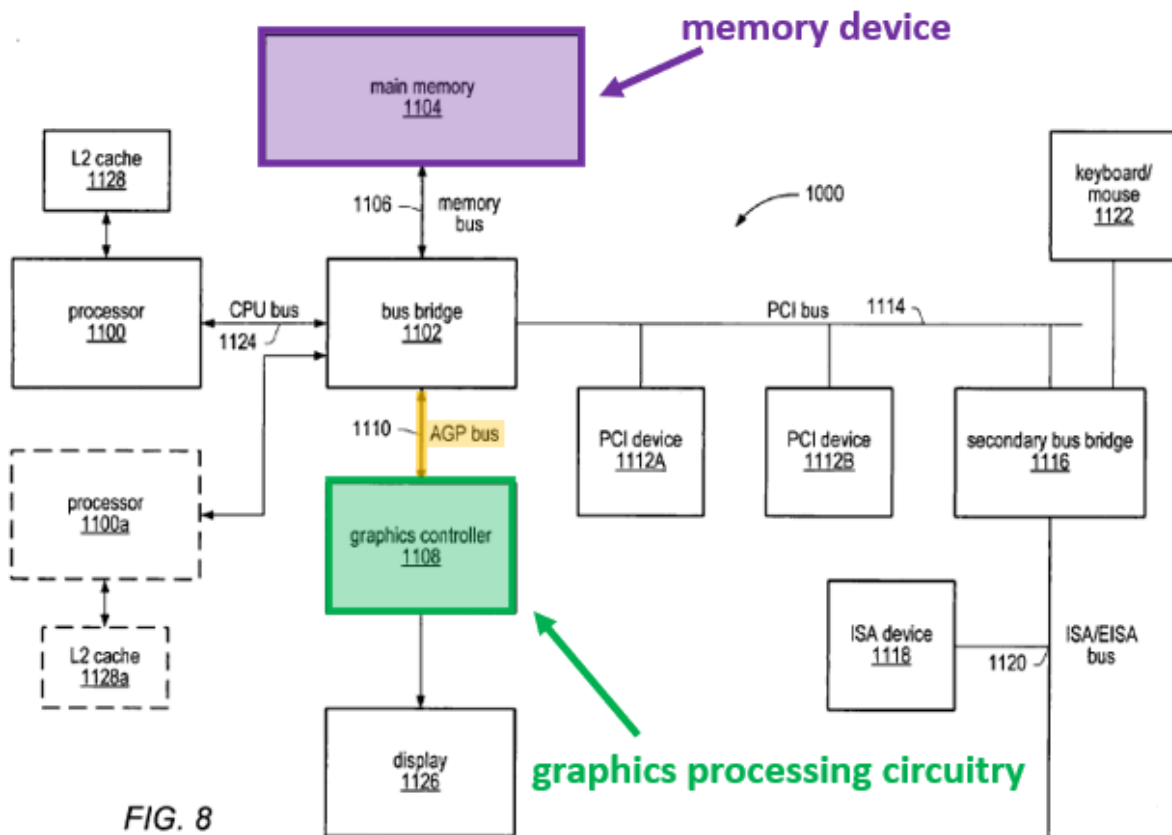
White discloses that the “graphics controller 1108 may include one or more multi-core integrated circuits and each logic core within such an integrated circuit may be configured to operate at independent frequencies and/or voltages, as described herein.” (White, 24:50-54, 6:42-46 (“an integrated circuit may include multiple logic cores, such as logic cores 120A and 120B each of which may be configured to operate at an independent voltage and frequency”).)

Thus, the cores of graphics controller 1108 may operate at an independent third frequency that is different from the first and second frequencies of the first and second cores, respectively. (*Id.*, 24:47-54; *see also* 2:55-57, 4:11-17, 10:28-32, 11:31-35; Horst Decl., ¶81.)

1[D]: an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first, second, and third frequencies.

White anticipates and/or renders obvious Claim 1[D]. (Horst Decl., ¶¶82-92.) White discloses an “interconnect” to couple the graphics processing circuitry

to a memory device that is operable at a fourth frequency different from the first, second, and third frequencies. For example, White discloses AGP (accelerated graphics port) bus 1110, bus bridge 1102, memory bus 1106, and common bridge logic 110. (White, 6:28-33, 7:1-11; 24:49-54, 25:1-4, 25:21-23, 25:50-55, 26:2-7, Figures 1 and 8.) White further discloses main memory 1104 and memory subsystem 170. (*Id.*, 7:1-7, Figures 1 and 8.) White discloses that “main memory 1104 is coupled to bus bridge 1102 through a memory bus 1106, and a graphics controller 1108 is coupled to bus bridge 1102 through an AGP bus 1110,” as depicted in Figure 8:



(*Id.*, Figure 8 (annotated); 25:1-4; 25:21-23, 25:50-54; 26:2-5; Horst Decl., ¶¶84-85.) White additionally discloses, in Figure 1, coupling logic cores of integrated circuit 100 (within graphics processing circuitry 1108) and memory subsystem 170 through common bridge logic 110:

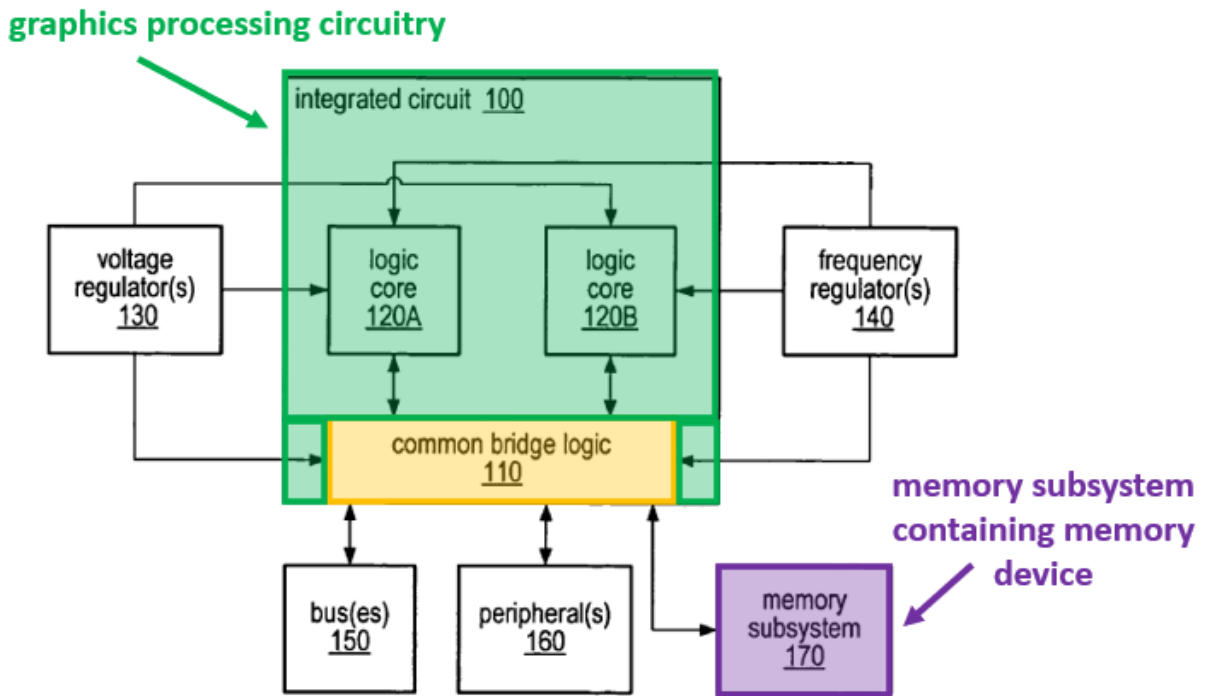


FIG. 1

(*Id.*, Figure 1 (annotated), 6:28-33; 7:1-11, 24:50-54; 25:1-23.) The common bridge logic can be a Northbridge, which is a “common component of many processors and may include separate interfaces to communicate with and route communication from multiple logic cores of an integrated circuit to other sub-systems, components or peripherals external to the integrated circuit.” (White,

2:48-53; *see* White 4:3-10, 7:46-49, 17:29-32; Horst Decl., ¶¶ 87-88.)

Main memory 1104 is a “memory in which application programs are stored and from which microprocessor 1100 primarily executes.” (*Id.*, 25:50-55.) It may be, for example, Dynamic Random Access Memory (DRAM), a plurality of banks of Synchronous DRAM (SDRAM), Rambus DRAM (RDRAM), or another suitable memory. (*Id.*) A POSITA would understand that memory subsystem 170 includes a memory device. (Horst Decl., ¶89.)

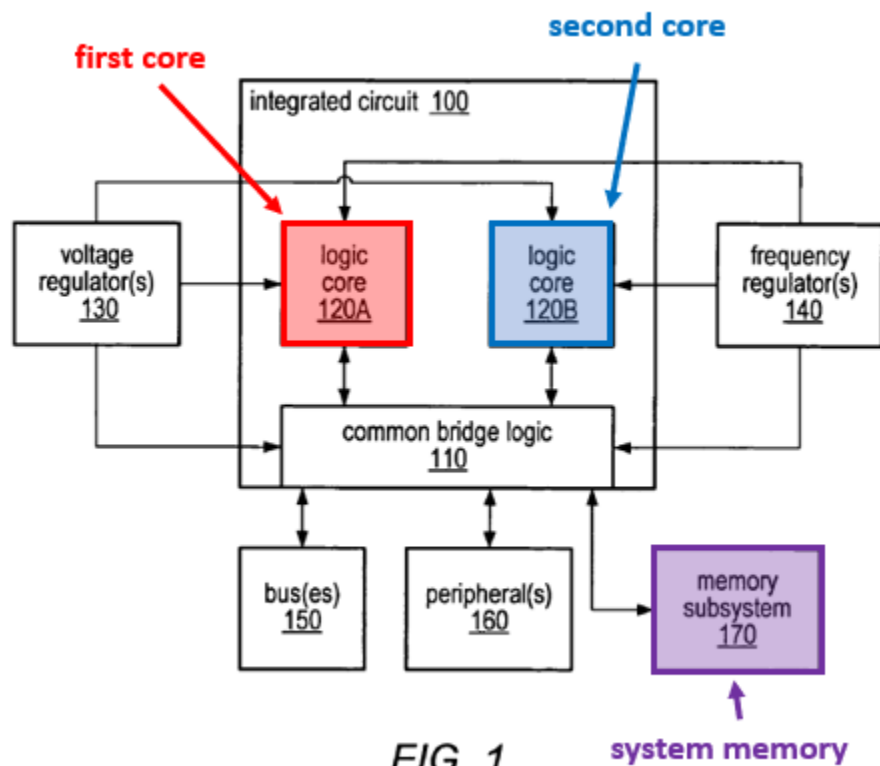
Common bridge logic 110 can “operate at a frequency and voltage different from any particular voltage or frequency at which the individual logic cores may be currently operating.” (White, 2:65-67, Abstract, 2:45-67, 7:1-22, 7:46-62, 8:10-26, 9:25-53.) A POSITA would also know that AGP bus operates at a frequency independent of the frequency of the cores within processors 1100 and graphics controller 1108. (Horst Decl., ¶¶90-92.)

(b) Independent Claim 8

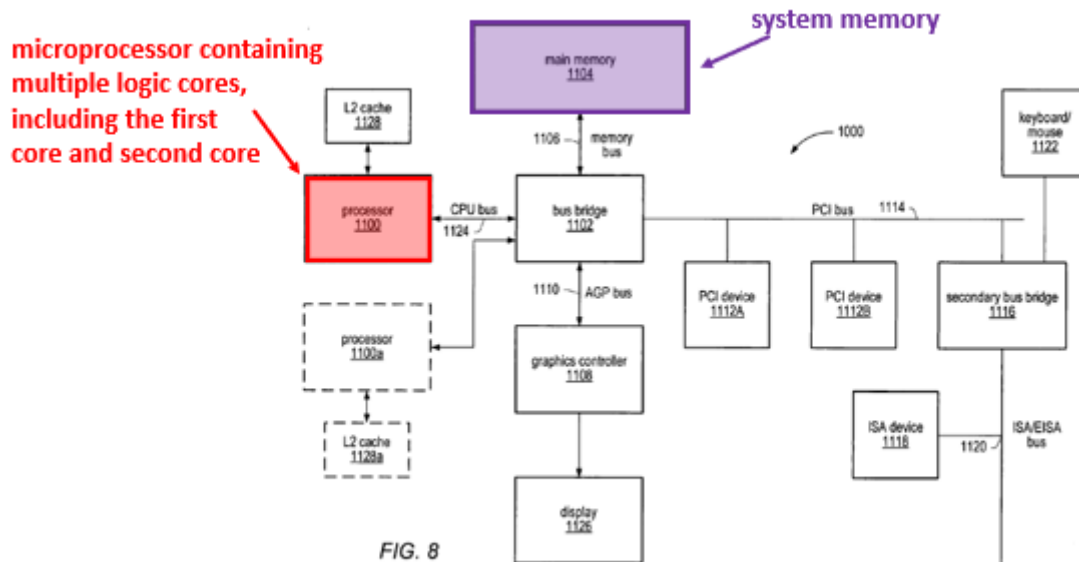
White anticipates and/or renders obvious Claim 8. (Horst Decl., ¶¶93-97.) For purposes of this Petition, there are no substantive differences between Claim 1 and Claim 8, and White anticipates and/or renders obvious Claim 8 for the same reasons as Claim 1. *See supra* VIII.A.1(a) (Ground 1, Claim 1). (*See also* Horst Decl., ¶¶60-92, 94.)

A redline comparison between Claim 1 and Claim 8 is shown in Appendix

A. As shown, Claim 8 recites features of a “system memory” (instead of a “memory device”) and that a “plurality of cores” is coupled to this system memory. Within the ’588, the “system memory” in Claim 8 is not distinguished from the “memory device” of Claim 1, and a POSITA would understand a “memory device” to include “system memory.” (Horst Decl., ¶¶96.) Thus, White discloses the “system memory” in Claim 8 for the same reasons it discloses the “memory device” in Claim 1. *See supra* VIII.A.1(a) (Ground 1, Claim 1[D]). In particular, White discloses that its processor includes system memory as memory subsystem 170 in Figure 1 or “main memory 1104” in Figure 8:



(White, Figure 1 (annotated)).



(White, Figure 8 (annotated).) As can be seen above, White discloses that the “system memory” is coupled to a plurality of cores. (*Id.*, Figures 1, 8, 2:28-34, 7:1-7, 25:21-23, 25:50-53; Horst Decl., ¶97.) In particular, White discloses that memory subsystem 170 is coupled to logic cores 120A and 120B through common bridge logic 110. (White, 7:1-7, Figure 1). White further discloses that main memory 1104 is coupled to the plurality of cores in processor 1100 (having integrated circuit 100) through memory bus 1106, bridge bus 1102, CPU bus 1124, and common bridge logic 110. (*Id.*, 7:1-7, 24:37-41, 25:10-14 Figures 1, 8; *see also* 25:50-53 (explaining that that main memory 1104 contains application programs that microprocessor 1100 executes), 25:16-20, Horst Decl., ¶97.)

(c) Independent Claim 20

White anticipates and/or renders obvious Claim 20. (Horst Decl., ¶¶98-108.)

Claim 20 is directed to an apparatus and was written in “means-plus-function” form to perform the functions of system Claim 1. A redline comparison between Claim 1 and Claim 20 is shown in Appendix B. The “functions” recited in Claim 20 are the same as those recited in Claim 1, so the analysis below cross-references the prior art analysis for Claim 1. (Horst Decl., ¶¶98-99.)

20[p]: An apparatus comprising:

White anticipates and/or renders obvious Claim 20[p]. (Horst Decl., ¶¶100-101.) *See supra* Section VIII.A.1(a) (Ground 1, Claim 1[p]). For example, White discloses a computer processor system that includes “[m]ultiple logic cores of integrated circuits and processors...” (White, Abstract.) White also discloses that its “[c]omputer system 1000 and/or integrated circuit 100...may be part of any of various types of devices including...in general any type of computing device.” (*Id.*, 24:59-67; *see also* Horst Decl., ¶¶100-101.)

20[A]: means for operating a first core at a first voltage and at a first frequency while concurrently operating a second core at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

White anticipates and/or renders obvious Claim 20[A]. (Horst Decl., ¶¶102-103.) As described above and herein, White discloses power management logic 200, temperature control logic 210, voltage regulator(s) 130, and frequency regulator(s) 140 configured to operate the first core 120A and second core 120B of

microprocessor 1100 at voltages and frequencies independent and distinct from each other. (White, 10:11-24, 13:27-43, Figures 2A-2B.) *See supra* Section VIII.A.1(a) (Ground 1, Claims 1[A]-1[B]); *see infra* VIII.A.1(d) (Ground 1, Claims 2 and 9). The corresponding structure of the '588 for operating first and second cores at different and independent frequencies and voltages is power control unit (PCU) 355/455. *See supra* Section VII.A.1 (Claim Construction). White discloses such a PCU, as it discloses power management logic 200, temperature control logic 210, voltage regulator(s) 130, and frequency regulator(s) 140. (*Id.*, Horst Decl., ¶103.)

20[B]: means for independently operating a graphics processor at a third frequency different from the first frequency and the second frequency; and

White anticipates and/or renders obvious Claim 20[B]. (Horst Decl., ¶¶104-105.) As described above and herein, White discloses power management logic 200, temperature control logic 210, voltage regulator(s) 130, and frequency regulator(s) 140 are configured to operate processing cores 120 of the graphics controller 1008 at an independent and distinct voltage and frequency. (White, 10:11-24, 13:27-43, Figures 2A-2B; Horst Decl., ¶105.) *See supra* Section VIII.A.1(a) (Ground 1, Claim 1[C]); *see infra* VIII.A.1(f) (Ground 1, Claims 4 and 11). The corresponding structure of the '588 for operating a graphics processor at a frequency different from the frequencies of processing cores is power control unit

355/455. *See supra* Section VII.A.2 (Claim Construction). White discloses such a PCU, as it discloses power management logic 200, temperature control logic 210, voltage regulator(s) 130, and frequency regulator(s) 140. (*Id.*, Horst Decl., ¶105.)

20[C]: interconnect means to couple the graphics processor to a memory device, the interconnect means operable at a fourth frequency different from the first, second, and third frequencies.

White anticipates and/or renders obvious Claim 20[C]. (Horst Decl., ¶¶106-108.) As described above, White discloses AGP bus 1110, bridge bus 1102, memory bus 1106, and common bridge logic 110 couple the graphics controller 1108 with main memory 1104 and memory subsystem 170. (White, 2:45-67, 6:28-33; 7:1-11, 24:50-54; 25:1-23, Figures 1-2B, 8.) *See supra* Section VIII.A.1(a) (Ground 1, Claim 1[D]). The corresponding structure of the '588 for coupling a graphics processor to a memory device, operable at a different frequency than the processing cores or graphics processor, is interconnect 315. *See supra* VII.A.3 (Claim Construction). White discloses such an interconnect, as it discloses AGP bus 1110, bridge bus 1102, memory bus 1106, and common bridge logic 110. (Horst Decl., ¶108.)

(d) Dependent Claims 2 and 9

The [processor/system] of claim [1/8], further comprising: first power management circuitry and/or logic to cause the first core to operate at the first frequency and cause the second core to independently operate at the second frequency.

White anticipates and/or renders obvious Claims 2 and 9. (Horst Decl., ¶¶109-112.) White discloses “power management logic and/or temperature control logic both of which may be configured to control or adjust the operating frequency and/or voltage for logic core(s) 120, and possible common bridge logic 110, according to various embodiments, and as described herein.” (White, 24:41-46; *see also* 8:59-9:24, 9:25-53, 9:54-10:10, 10:11-24, 11:24-55, 11:56-60, 11:61-12:58.) For example, “power management logic 200 may be configured to adjust the operating characteristics for one logic core to a lower level than the operating characteristics of another logic core depending upon the overall power consumption or depending upon the specific nature of the system.” (*Id.*, 9:25-30; *see also* 23:1-7, 3:37-41, 13:7-63.) White’s Figure 2A illustrates power management logic 200 that causes logic core 120A and logic core 120B to independently operate at different frequencies through frequency regulator 140:

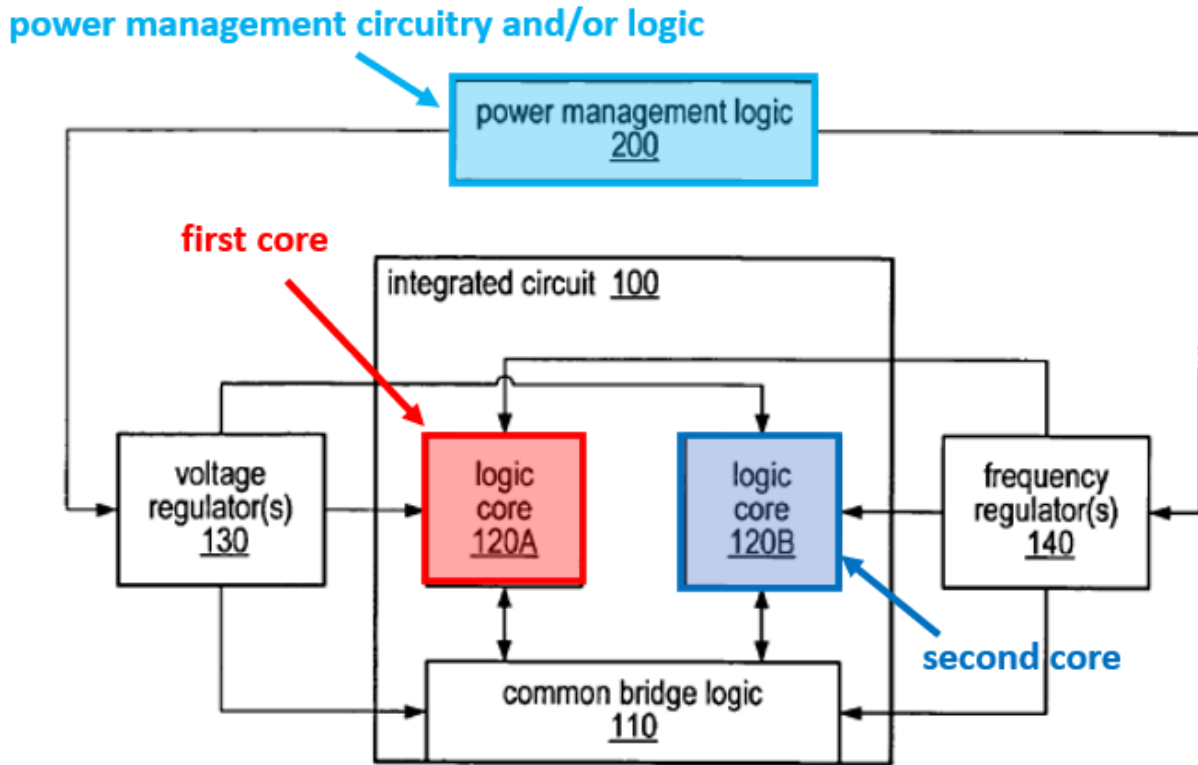


FIG. 2A

(*Id.*, Figure 2A (annotated).) Further, White's Figure 2B illustrates temperature control logic 200 that causes logic core 120A and logic core 120B to independently operate at different frequencies through frequency regulator 140:

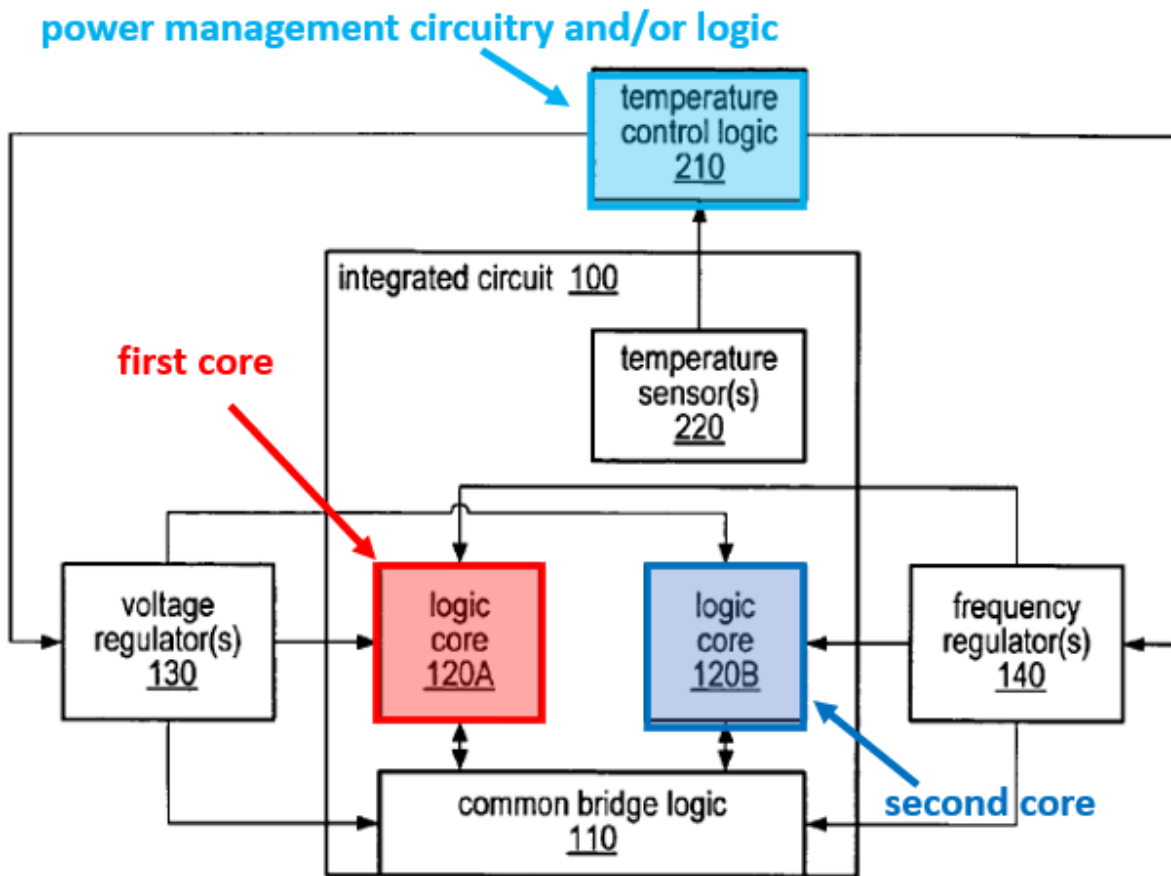


FIG. 2B

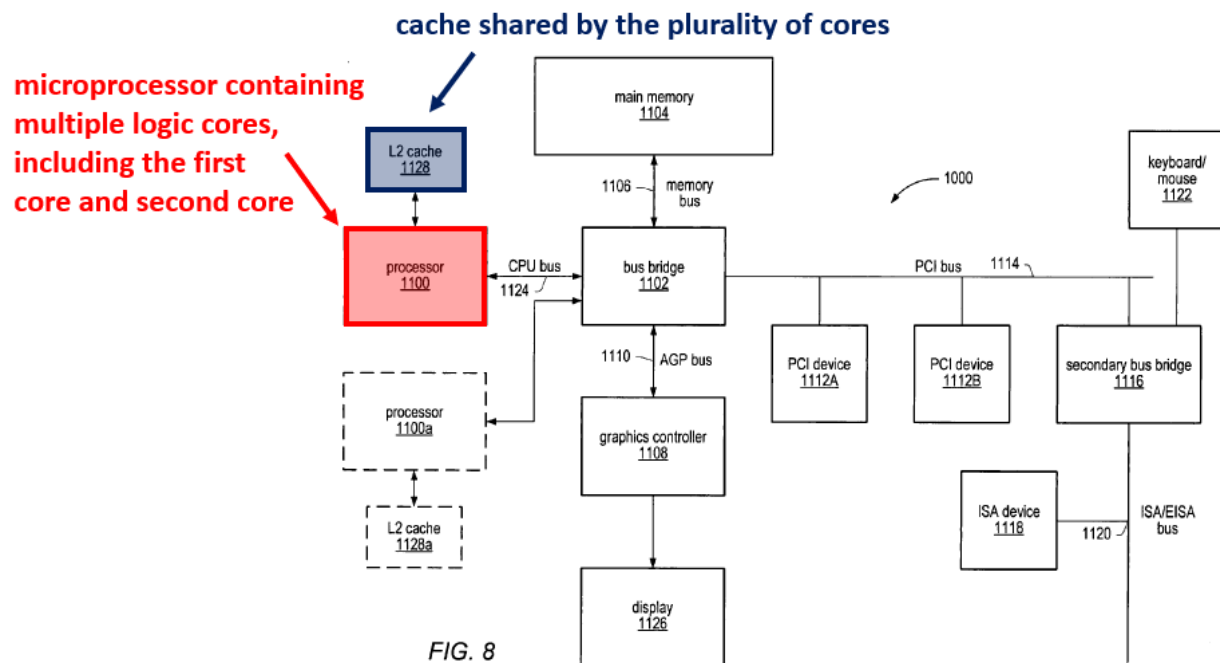
(*Id.*, Figure 2B (annotated); *see also* 11:61-12:15, 18:9-16, 12:16-37, 12:38-58, 13:7-26, 13:27-43, 13:44-63, 13:64-14:20, 14:21-38.)

(e) Dependent Claims 3 and 10

The [processor/system] of claim [1/8], further comprising: a non-core power domain comprising a cache shared by the plurality of cores.

White anticipates and/or renders obvious Claims 3 and 10. (Horst Decl., ¶¶113-114.) White discloses that “microprocessor 1100...may...be coupled to an optional L2 cache 1128[.]” (White, 25:10-14; *see also* 25:44-49, 26:28-30.) A

POSITA would understand that an L2 cache is a cache that is shared among processing cores. (Horst Decl., ¶114.) L2 cache is within a “non-core power domain” because it “may be separate from microprocessor 1100, integrated into a cartridge (e.g., slot 1 or slot A) with microprocessor 1100, or even integrated into a semiconductor substrate with microprocessor 1100.” (Horst Decl., ¶114; White, 25:44-49.) Further, Figure 8 depicts that “microprocessor 1100 may include multiple logic cores” that share the L2 cache (within a “non-core power domain”):



(White, Figure 8 (annotated), 24:33-34; Horst Decl., ¶114.)

(f) Dependent Claims 4 and 11

The [processor/system] of claim [2/9], further comprising: second power management circuitry and/or logic to cause the graphics processing circuitry to operate at the third frequency.

White anticipates and/or renders obvious Claims 4 and 11. (Horst Decl., ¶¶115-117.) White discloses circuits containing a power management logic 200 and a temperature control logic 210 to control the operating frequency of logic core(s). (*Id.*, 24:41-46, *see also* 14:32-38.) White discloses a graphics controller 1108 that includes “one or more multi-core integrated circuits,” wherein “each logic core within such an integrated circuit may be configured to operate at independent frequencies and/or voltages, as described herein.” (White, 24:50-54, 8:61-65 (“[P]ower management logic 200 may be configured to control the operating characteristics, such as the operating voltage and/ or operating frequency, of each of multiple logic cores 120 of integrated circuit 110.”), 12:41-45.) Accordingly, a POSITA would understand that White’s power management logic 200 and temperature control logic 210 are able (*e.g.*, have logic) to independently control the frequencies of the logic cores of graphics controller 1108. (Horst Decl, ¶¶116-117; *see, e.g.*, White 8:59-9:24, 9:25-53, 9:54-10:10, 10:11-24, 11:24-55, 11:56-60, 11:61-12:15, 12:16-37, 12:38-58, 13:7-26, 13:27-43, 13:44-63, 13:64-14:20, 14:21-38, 18:9-16.) *See supra* VIII.A.1(d) (Ground 1, Claims 2 and 9). Figure 2A discloses that power management logic 200 controls the logic cores 120A and 120B of graphics processing circuitry through frequency regulator 140:

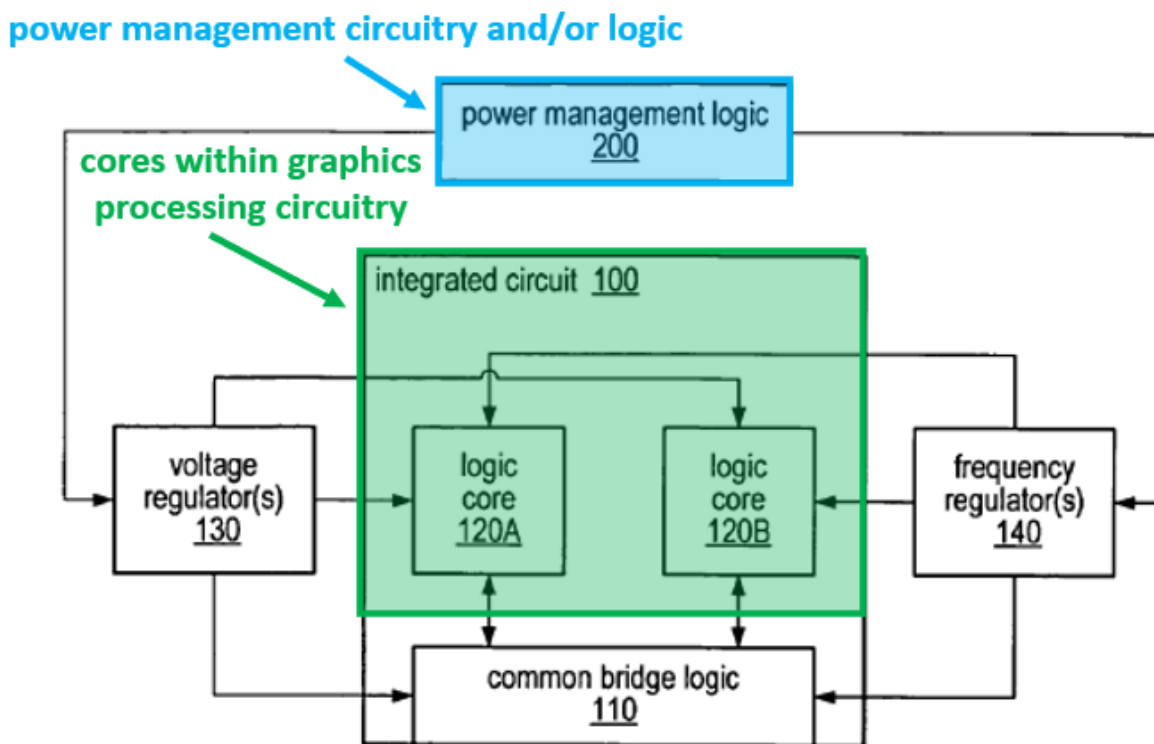


FIG. 2A

(*Id.*, Figure 2A (annotated).) Figure 2B discloses that temperature control logic 210 controls the frequency of logic cores 120A and 120B of the graphics processing circuitry through frequency regulator 140:

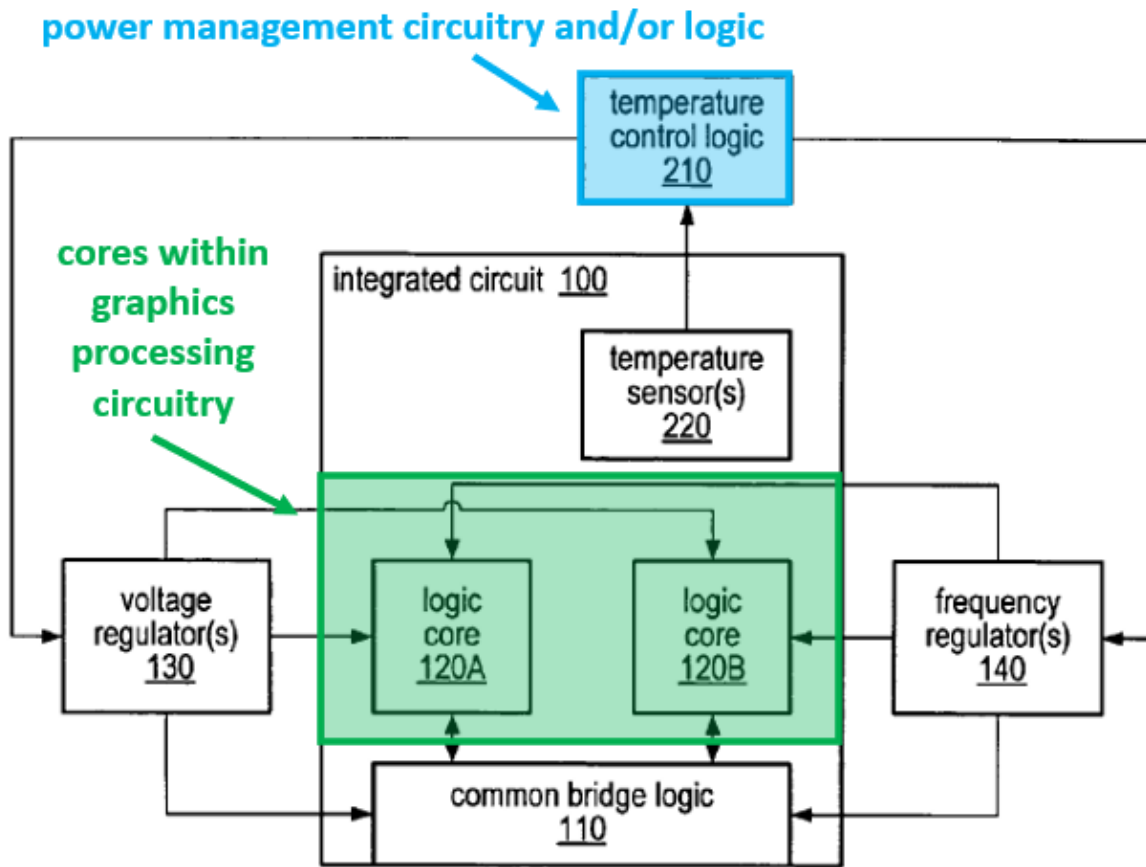


FIG. 2B

(*Id.*, Figure 2B (annotated).)

(g) Dependent Claims 7 and 14

The [processor/system] of claim [3/10], further comprising: power management circuitry and/or logic to cause the non-core power domain to operate at a different frequency from the first and second frequencies of the first and second cores, respectively.

White anticipates and/or renders obvious Claims 7 and 14. (Horst Decl., ¶¶118-120.) In discussing the common bridge logic 110, White discloses that “the operating frequency of a controller may be adjusted to be higher than the current

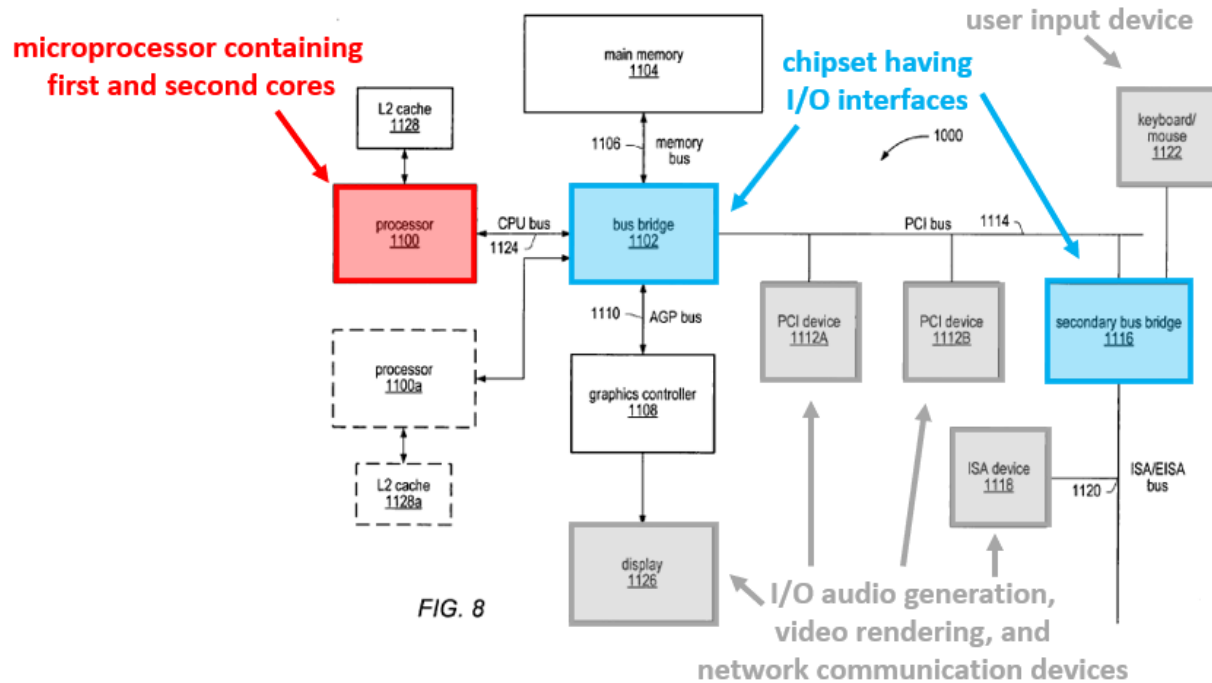
operating frequency of all the logic cores in the processor.” (White, 4:21-30, *see also* 9:36-53 (describing how “power management logic 200 may be configured to supply higher voltages and/or frequencies to common bridge logic 110 than to the logic cores”).) A POSITA would recognize that the controller (*i.e.*, common bridge logic 110) is within a non-core power domain because it is not a logic core and because it is operable at a voltage independent of the voltages of the logic cores. (*Id.*, 10:25-35, Horst Decl., ¶¶119-120.) And a POSITA would understand that White includes power management circuitry and/or logic, as it can adjust the operating frequency of the controller. (Horst Decl., ¶¶119-120, White, 4:21-30, 9:30-32 (“power management logic 200 may be configured to adjust the voltages and/or frequencies supplied to common bridge logic 110”).)

(h) Dependent Claims 15-19

15: The system of claim 8, further comprising a chipset coupled to the plurality of cores, the chip set comprising a plurality of interfaces to couple the cores to a plurality of I/O devices.

White anticipates and/or renders obvious Claims 15. (Horst Decl., ¶¶121-124.) White discloses “a processor or integrated circuit...includ[ing] separate interfaces to communicate with and route communication from multiple logic cores of an integrated circuit to other sub-systems, components, or peripherals external to the integrated circuit.” (White, 2:45-53.) White’s Figure 8 further discloses that microprocessor 1100 (which includes multiple cores) is coupled

through CPU bus 1124 to chipset bus bridge 1102, which “provide[s] an interface between microprocessor 1100...graphics controller 1108[] and devices attached to PCI bus 1114.” (*Id.*, 25:21-23, *see also* 25:1-31.):



(White, Figure 8 (annotated), *see generally* 24:30-26:30.) Bus bridge 1102 is further coupled by PCI bus 1114 to secondary bus bridge 1116 that is coupled to ISA/EISA bus 1120. (*Id.*, 25:7-10, Figure 8.) PCI bus 1114, secondary bus bridge 1116, and ISA/EISA bus 1120 can be coupled with various I/O devices. (*Id.*, Figure 8.) White’s disclosure of bus bridge 1102, PCI bus 1114, secondary bus bridge 1118, and ISA/EISA bus 1120 is a disclosure of “chipsets” comprising “interfaces” that couple the cores to peripherals, because such buses provide an interface and manage data flow between the processor and peripherals. (Horst

Decl., ¶124; *see also* 25:21-23.)

16: The system of claim 15, wherein one of the I/O devices comprises an audio generation device.

White anticipates and/or renders obvious Claim 16. (Horst Decl., ¶¶125-126.) As shown in Figure 8 (annotated above), White discloses “PCI devices 1112A-1112B [that] are illustrative of a variety of peripheral devices such as...audio cards...and telephony cards,” (White, 25:56-60), and “ISA device 1118 [that] is illustrative of various types of peripheral devices such as a...sound card[.]” (*Id.*, 25:60-62.) White’s disclosed audio cards, telephony cards, and sound cards are “audio generation devices” because they are capable of generating audio signals. (Horst Decl., ¶126.)

17: The system of claim 16, wherein one of the I/O devices comprises a video rendering device.

White anticipates and/or renders obvious Claim 17. (Horst Decl., ¶¶127-129.) As shown in Figure 8 (annotated above), White discloses “PCI devices 1112A-1112B [that] are illustrative of a variety of peripheral devices such as...video accelerators” and a “display 1126” that renders text and images. (White, 25:56-60, 64-65.) “Display 1126 is any electronic display upon which an image or text can be presented. A suitable display 1126 includes a cathode ray tube (‘CRT’), a liquid crystal display (‘LCD’), etc.” (*Id.*, 26:12-15.) White’s disclosed video

accelerators and display are “video rendering devices” because they render video.

(Horst Decl., ¶¶128-129.)

18: The system of claim 17, wherein one of the I/O devices comprises a user input device.

White anticipates and/or renders obvious Claim 18. (Horst Decl., ¶¶130-131.) As shown in Figure 8 (annotated above), White discloses keyboard and mouse 1122 coupled with secondary bus bridge 1116. (*See also* White, 25: 34-38 (“An input/output controller (not shown), either external from or integrated with secondary Bus Bridge 1116, may also be included within computer system 1100 to provide operational support for a keyboard and mouse 1122.”).) White also discloses “PCI devices 1112A-1112B [that] are illustrative of a variety of peripheral devices such as...floppy disk drives[.]” (White, 25:56-58.) Such keyboards, mice, and floppy disk drives are user input devices because they enable user input to the system. (Horst Decl., ¶131.)

19: The system of claim 18, wherein one of the I/O devices comprises a network communication device.

White anticipates and/or renders obvious Claim 19. (Horst Decl., ¶¶132-133.) As shown in Figure 8 (annotated above), White discloses “PCI devices 1112A-1112B [that] are illustrative of a variety of peripheral devices such as network interface cards...and telephony cards,” (White, 25:56-60), and “ISA device

1118 [that] is illustrative of various types of peripheral devices such as a modem.”

(*Id.*, 25:60-62; *see also* 24:65-66.) White’s network interface cards, telephony cards, and modems are each a “network communication device” because they enable communication over a network. (Horst Decl., ¶133.)

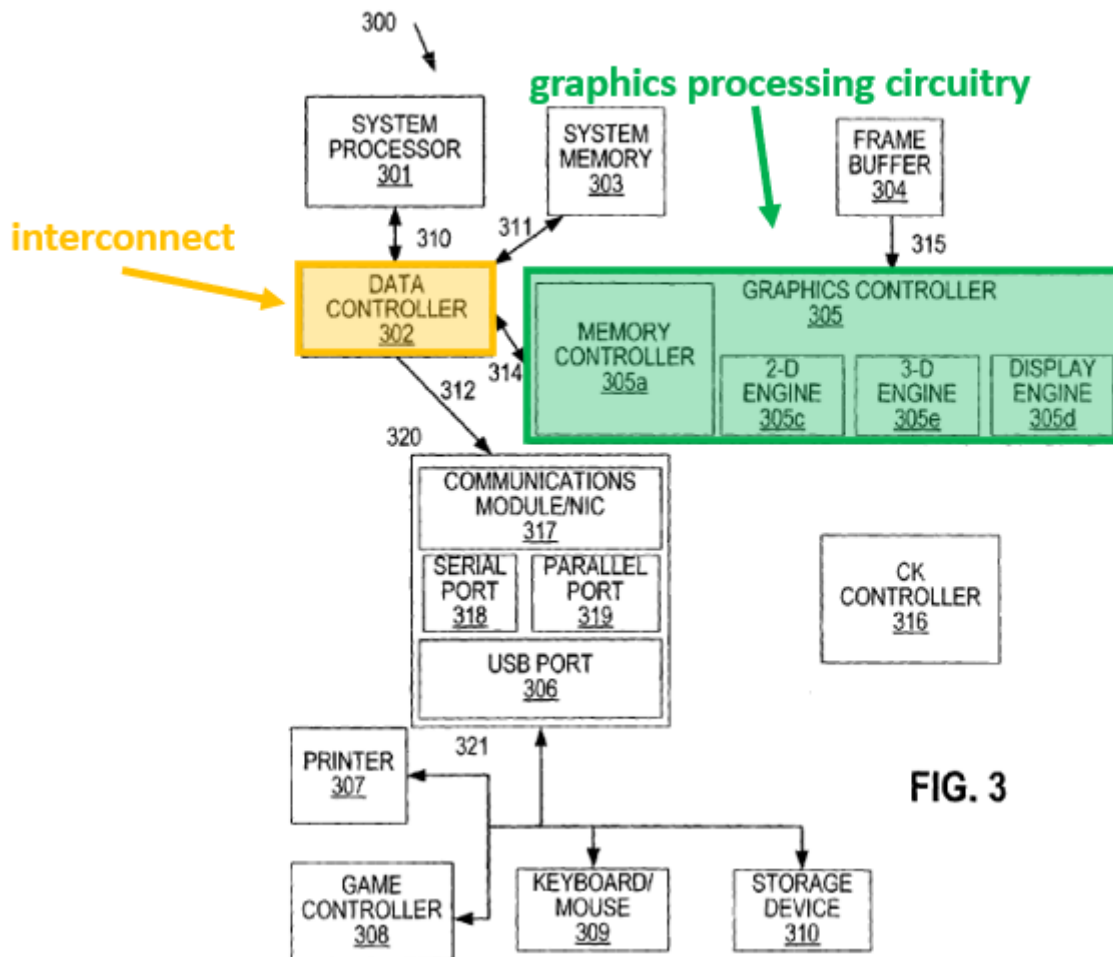
2. Ground 2: Claims 5-6 and 12-13 are obvious over White in view of Shakkarwar

(a) Dependent Claims 5 and 12

The [processor/system] of claim [4/11], wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.

White in view of Shakkarwar renders obvious Claims 5 and 12. (Horst Decl., ¶¶134-141.) As explained above, White discloses both graphics processing circuitry and an interconnect. *See supra* Section VIII.A.1(a) (Ground 1, Claims 1[C]-1[D]). Additionally, White discloses a second power management circuitry and/or logic. *See supra* Section VIII.A.1(f) (Ground 1, Claims 4 and 11). White in view of Shakkarwar further teaches that this power management circuitry can include a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect. (Horst Decl., ¶135.)

Shakkarwar’s dynamic power management system includes data controller 302 connected to graphics controller 305 through data connection 314, as illustrated in Figure 3:



(Shakkarwar, Figure 3 (annotated).)

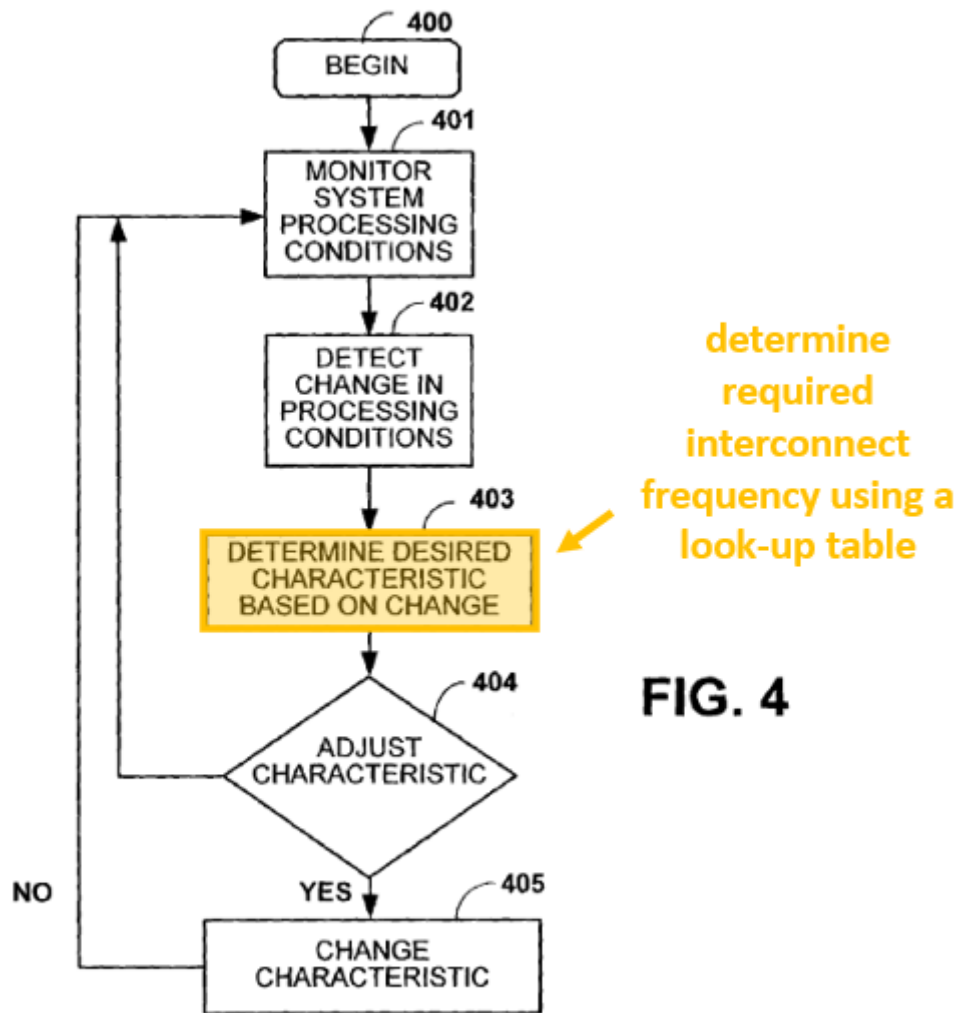
Data controller 302 connects graphics controller 305 and other components within Shakkarwar to each other and to system memory 303. (Shakkarwar, 5:10-15, Fig. 4.) Graphics controller 305 includes a “3-D engine 305e” and performs “3-D graphics operations....” (*Id.*, 6:7-16.) A POSITA would have understood that data controller 302 and data connection 314 are an “interconnect,” and the “graphics controller 305” is “graphics processing circuitry.” (Horst Decl., ¶137.)

Shakkarwar also maps selectable frequencies of the graphics processing

circuitry to selectable frequencies of the interconnect in a look-up table. (Horst Decl., ¶138; Shakkarwar, 7:5-10.) At step 401 (shown below), Shakkarwar monitors “bandwidth for a component,” such as the interconnect or graphics processing circuitry, for “increasing or decreasing communication requirements.” (Shakkarwar, 6:41-43.) For example, “when an application that is known to use 3-D graphics is opened, system software can determine if the bus rate between the data controller [the ‘interconnect’] and the graphics controller [the ‘graphics processing circuitry’] is high enough to support the graphics requirements.” (*Id.*, 6:49-52; *see also* 7:5-10 (describing determining data connection bandwidth 403 (*i.e.*, clock speeds/frequencies) required to process information for specific devices/groups of devices).)

At step 402, the system detects “a change in processing condition[s]” for a specific component, and upon detecting a change, it “determines bandwidth 403 for an associated data connection ***based on the active components.***” (Shakkarwar, 6:63-7:7; *see also* 7:7-10 (explaining that bandwidth can be determined with a look-up table containing “a list of clock speeds...required to process information for specific devices and/or groups of devices”).) To determine the appropriate bandwidth for a data connection, Shakkarwar utilizes “***a look-up table*** [that] may include ***a list of clock speeds, and/or voltage levels required to process information for specific devices and/or groups of devices.***” (*Id.*, 7:7-10.) Figure 4

illustrates this process:



(*Id.*, Figure 4 (annotated).) Shakkarwar thus teaches determining the appropriate bandwidth for a data connection to a module (e.g., graphics controller 305), utilizing a look-up table that includes a list of appropriate clock speeds. (*Id.*, 7:5-10; Horst Decl., ¶140.) It also considers other active components, such as the data controller 302 (e.g., the “interconnect”) and its clock speeds. (White, 7:5-10; Horst

Decl., ¶140.) As such, a POSITA would have understood that Shakkarwar teaches to map selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect using look-up tables. (Horst Decl., ¶140.)

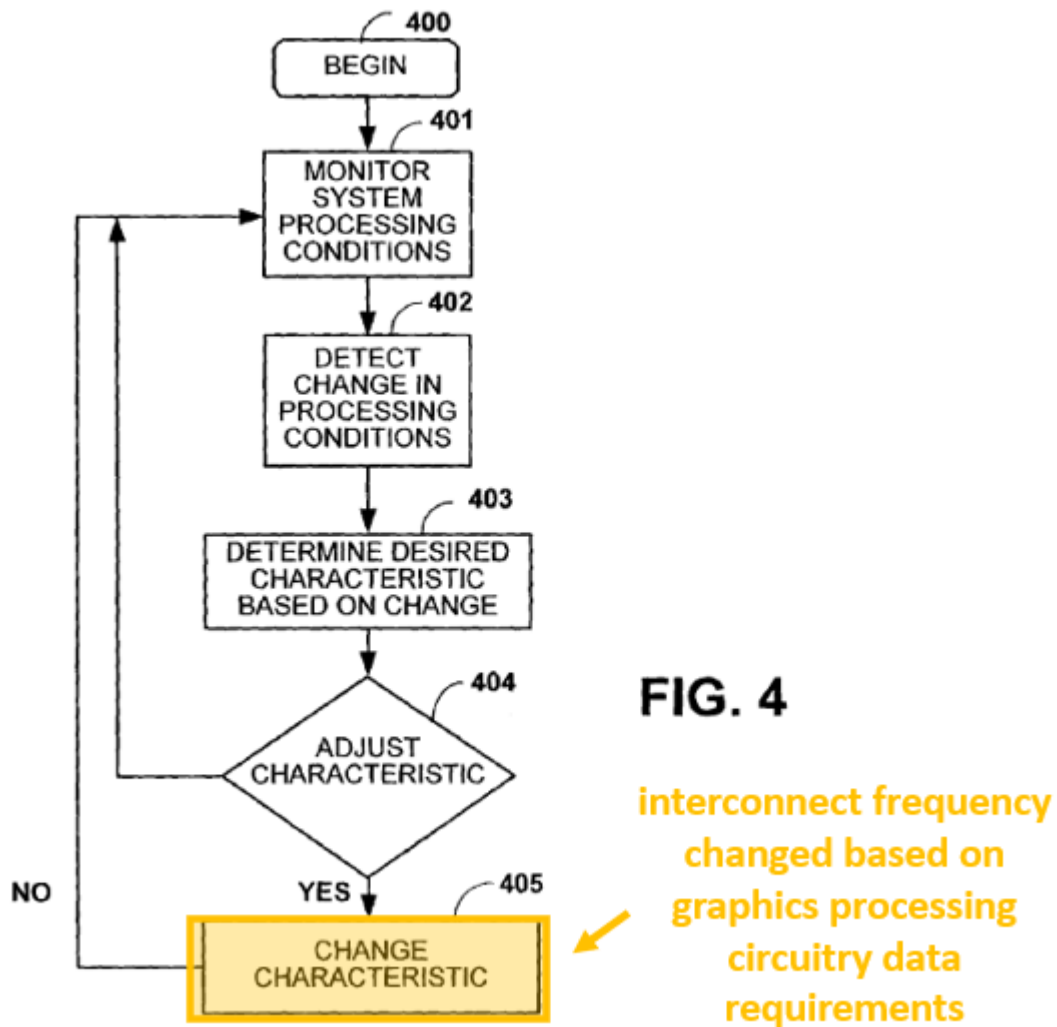
A POSITA would have been motivated to implement these teachings of Shakkarwar, such as a look-up table, in White for the reasons described below in Section VIII.A.2(c) (Ground 2, Rationales to Combine White and Shakkarwar), including because Shakkarwar teaches that an advantage to its system is that it dynamically “manag[es] power consumption of electronic devices while satisfying bandwidth requirements for communicating and/or processing information.” (Shakkarwar, 2:34-39.) A POSITA would have been motivated to include this advantage in White’s power management logic 200 and/or temperature control logic 210 to improve responsiveness and increase the ability of the system to respond to dynamically changing conditions, including the changing bandwidth requirements of White’s components during various activity states. (Horst Decl., ¶141.)

(b) Dependent Claims 6 and 13

The [processor/system] of claim [5/12], wherein the second power management circuitry and/or logic is to select the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.

White in view of Shakkarwar renders obvious Claims 6 and 13. (Horst Decl., ¶¶142-143.) As explained above, White in view of Shakkarwar disclose second

power management circuitry that determines bandwidth for an associated data connection based on the other active components by using a look-up table of clock speeds required to process information for specific devices. *See supra* Section VIII.A.2(a) (Ground 2, Claims 5 and 12). Shakkarwar further discloses that “[a]t step 405, the data rate of a data connection is adjusted. In one embodiment, the data rate can be adjusted by adjusting operating of a clock generation device.” (Shakkarwar, 7:26-29.) Figure 4 illustrates adjusting the data rate of a data connection:



(*Id.*, Figure 4 (annotated).)

Shakkarwar also specifically discloses selecting “the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.” (Horst Decl., ¶144.) Shakkarwar discloses that “when an application that is known to use 3-D graphics is opened, system software can determine if *the bus rate between the data controller [e.g., “interconnect”] and the graphics controller [e.g., “graphics processing circuitry”] is high enough to*

support the graphics requirements.” (Shakkarwar, 6:49-52 (emphasis added); *see also* Shakkarwar 7:5-10 (describing determining data connection bandwidth 403 (*i.e.*, clock speeds/frequencies) required to process information for specific devices/groups of devices).) A POSITA would have understood that by applying these teachings from Shakkarwar to White, the fourth frequency for the interconnect would be selected based on detecting the third frequency of the graphics processing circuitry. (Horst Decl., ¶144.)

(c) Combining White’s and Shakkarwar’s teachings would have been obvious to a POSITA.

In addition to the reasons set forth above, combining the teachings of White and Shakkarwar would have been obvious to a POSITA, a POSITA would have been motivated to do so, and a POSITA would have had a reasonable expectation of success in doing so because each relates to the same well-known technologies. (Horst Decl., ¶¶145-149.) Both relate to and describe similar methods for optimizing performance between multiple components within a computer system. (White, Abstract; Shakkarwar, Abstract.) White discloses a “[s]ystem and method for operating components of an integrated circuit at independent frequencies and/or voltages.” (White, Title.)

White discloses a system wherein the “operating frequency and/or voltage of a logic core may be independently adjusted for various reasons, including power

management and temperature control.” (*Id.*, Abstract.) White discloses adjusting the frequency of common bridge logic 110 to account for the new operating frequency of the logic cores and ensure compatibility. (White, Figures 4-7; 23:59-24:6, 17:29-18:8, 20:39-57.) White further discloses that its power management logic can “determine a new operating voltage using various methods, such as an algorithm or a look up table of compatible pairs of voltage and frequencies.” (*Id.*, 10:61-11:2, 16:57-17:15, 19:35-42.)

Similarly, Shakkarwar relates to the “efficient use of electronic devices and, more particularly, to systems and methods for power management of electronic devices.” (Shakkarwar, 1:8-10.) Shakkarwar discloses “[s]ystems and methods for dynamic power management of electronic devices” so that “power consumption of the system may be dynamically managed while providing sufficient bandwidth for the system.” (Shakkarwar, Abstract.) Shakkarwar dynamically manages power by monitoring a component’s “bandwidth...for increasing or decreasing communication requirements.” (*Id.*, 6:41-43.) The system then detects “a change in processing condition[s]” for a component, and upon detecting a change, “determines bandwidth 403 for an associated data connection based on the active components.” (*Id.*, 6:63-7:7; *see also* 7:7-10 (explaining that bandwidth can be determined with a look-up table containing “a list of clock speeds...required to process information for specific devices and/or groups of devices”).) The data rate

“of a data connection is [then] adjusted,” including by adjusting a clock frequency or voltage, to reach optimal performance levels. (*Id.*, 7:26-29.) In this manner, “power consumption associated with communicating and processing information via data buses may be optimized while satisfying bandwidth requirements for the computer system.” (*Id.*, 3:17-20; *see also* 2:12-15, Claim 21.)

A POSITA would have been motivated to combine the teachings of White in view of Shakkarwar because she would have recognized the predictable benefit of implementing the known technique of a look-up table for dynamically managing power, such as taught by Shakkarwar, to optimize performance of components within a processor as taught by White. (Horst Decl., ¶148.) As noted, Shakkarwar teaches that an advantage to its system is that it dynamically “manag[es] power consumption of electronic devices while [also] satisfying bandwidth requirements for communicating and/or processing information.” (Shakkarwar, 2:34-39.) By using a lookup table, Shakkarwar additionally teaches “determin[ing] bandwidth 403 for an associated data connection based on the active components,” “[u]pon detecting a change in processing.” (*Id.*, 7:5-7.) Shakkarwar thereby implements White’s suggested step of adjusting common bridge logic to operate at a frequency that is compatible with the frequency of a given logic core, such as the frequency in graphics circuitry. (*See* White, Figures 4-7; 23:59-24:6, 17:29-18:8, 20:39-57; Horst Decl., ¶148.) White already discloses using lookup tables in its power

management methods, (White, 10:61-11:2, 16:57-17:15, 19:35-42,) so a POSITA would be motivated to use and find it obvious to try such tables to choose map selectable frequencies of graphics controller 1108 to selectable frequencies of the common bridge logic 110. (Horst Decl., ¶148.)

A POSITA would also have had a reasonable expectation of success in combining the teachings of White in view of Shakkarwar. (Horst Decl., ¶149.) A POSITA would have understood that these references disclose interrelated teachings based on routine technologies that would have been amenable to various well-understood and predictable combinations, as explained below. (*Id.*) The teachings of Shakkarwar are compatible and incorporating such teachings into White would be well within the expertise of a POSITA using known methods for fabricating computer systems. (*Id.*)

B. Grounds based on Nussbaum

Nussbaum was filed July 24, 2009, and published on January 27, 2011. Nussbaum is prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and (e).

Nussbaum discloses “Determining Performance Sensitivities of Computational Units,” (Nussbaum, Title), in addition to an integrated circuit including a plurality of computational units and control logic to determine such performance sensitivities, (*id.*, [0007]). Nussbaum discloses an exemplary System on a Chip (SOC) 100 integrated circuit to implement its disclosed method. (*Id.*,

[0020].) SOC 100 is shown in Fig. 1, which includes multiple CPU processing cores 101, a Graphics Processing Unit (GPU) 103, an I/O Bridge (South-Bridge) 105, and a North-Bridge 107:

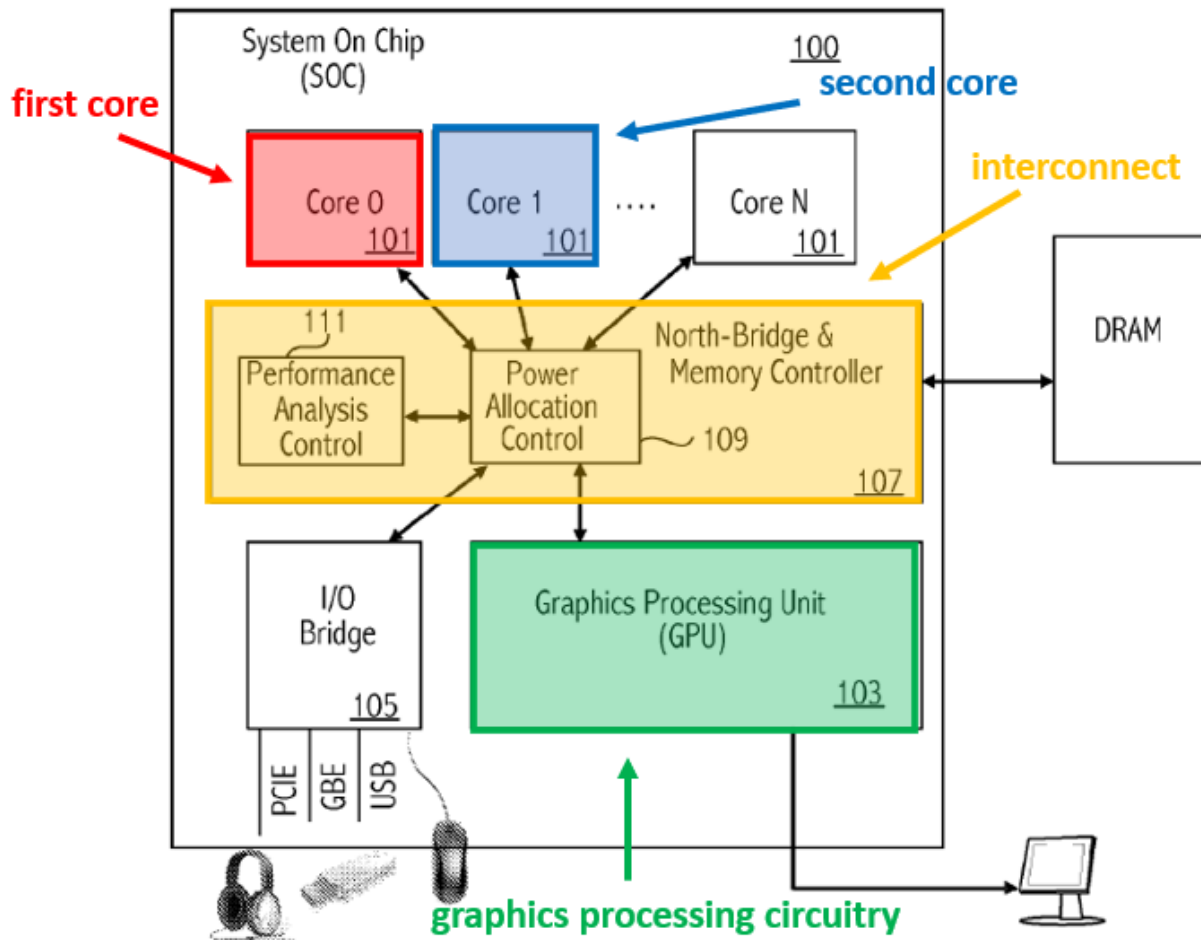


FIG. 1

(*Id.*, Figure 1 (annotated), [0020], [0035].) Nussbaum discloses independently adjusting the frequency and voltage of SOC components to improve performance while remaining below the SOC's Thermal Design Point (TDP), which is the

threshold of power that the SOC can consume. (*Id.*, [0021]-[0024].) Nussbaum accomplishes this by allocating power (thereby increasing operational parameters frequency and voltage) to CPU or GPU cores that will yield the largest performance improvement for the given task from the additional power (*i.e.*, to the cores that are the “most sensitive” to the boosted power). (*Id.*, [0024]-[0025], [0032].)

1. Ground 3: Claims 1-4, 7-11, and 14-20 are anticipated or obvious over Nussbaum

(a) Independent Claim 1

Nussbaum anticipates and/or renders obvious Claim 1. (Horst Decl., ¶¶153-175.)

1[p]: A processor comprising:

Nussbaum anticipates and/or renders obvious Claim 1[p]. (Horst Decl., ¶¶154-155.) Nussbaum discloses a System on Chip (SOC) that “includes multiple CPU processing cores 101, a GPU (Graphics Processing Unit) 103, an I/O Bridge 105 (named South-Bridge in some embodiments) and a North-Bridge 107 (which may be combined with the Memory Controller in some embodiments).”

(Nussbaum, [0020].) As can be seen, the “processor” of Figure 1 includes, among other components, SOC 100, Core 0 101, Core 1 101, power allocation control 109, North-Bridge & Memory Controller 107, I/O Bridge 105, GPU 103, dynamic

random-access memory (DRAM), and performance analysis control logic 111:

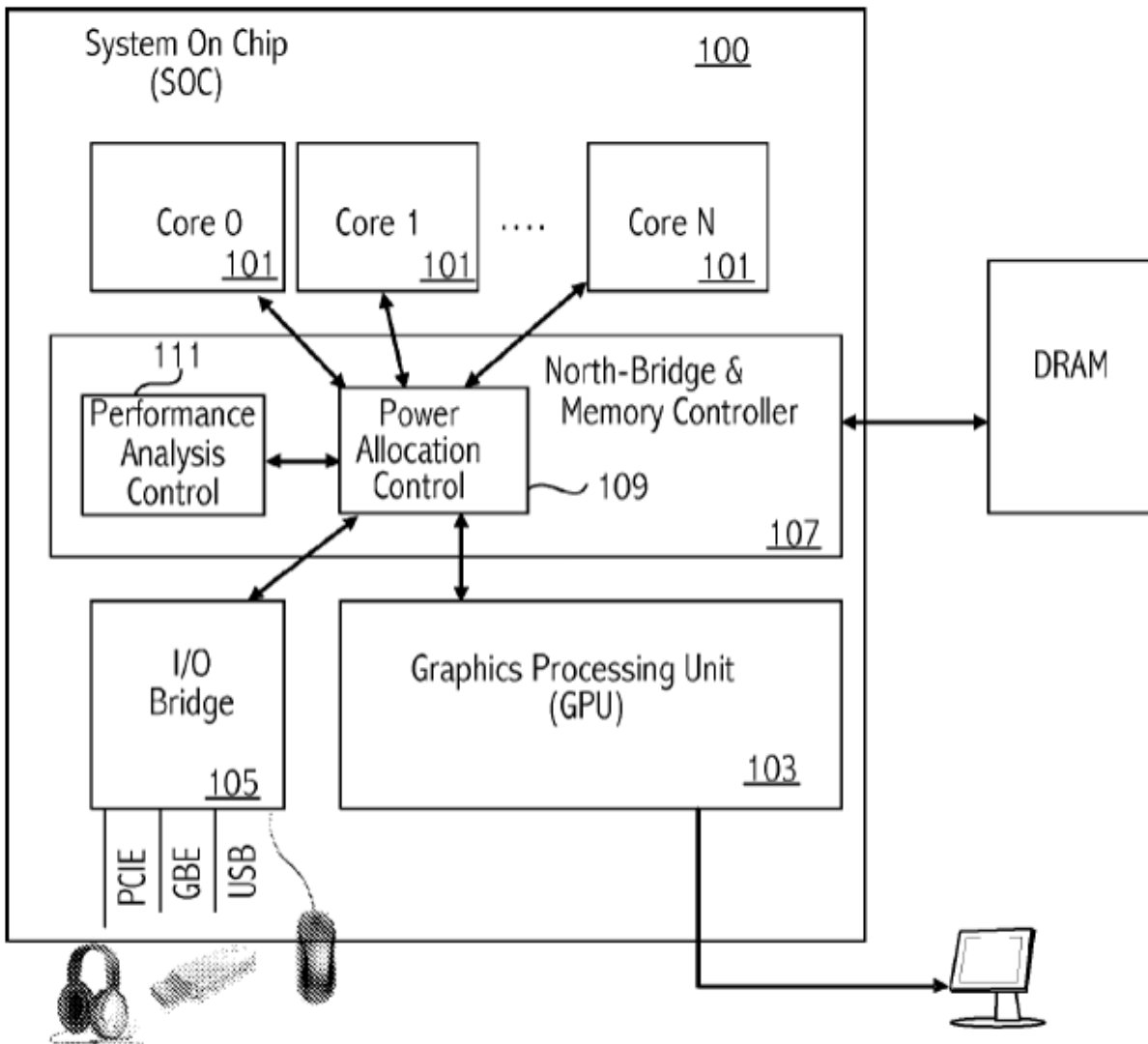


FIG. 1

(*Id.*, Figure 1 (annotated), [0020].)

1[A]: a plurality of cores including a first core operable at a first voltage and at a first frequency, and

Nussbaum anticipates and/or renders obvious Claim 1[A]. (Horst Decl., ¶¶156-159.) Nussbaum discloses that the processor includes a plurality of cores,

and in particular “multiple CPU processing cores 101,” among which power may be selectively distributed “based on frequency sensitivity [to] allow[] for overall greater system throughput.” (Nussbaum, [0019], [0020].) Specifically, Nussbaum discloses a first core in Figure 1, showing Core 0 101 within SOC 100:

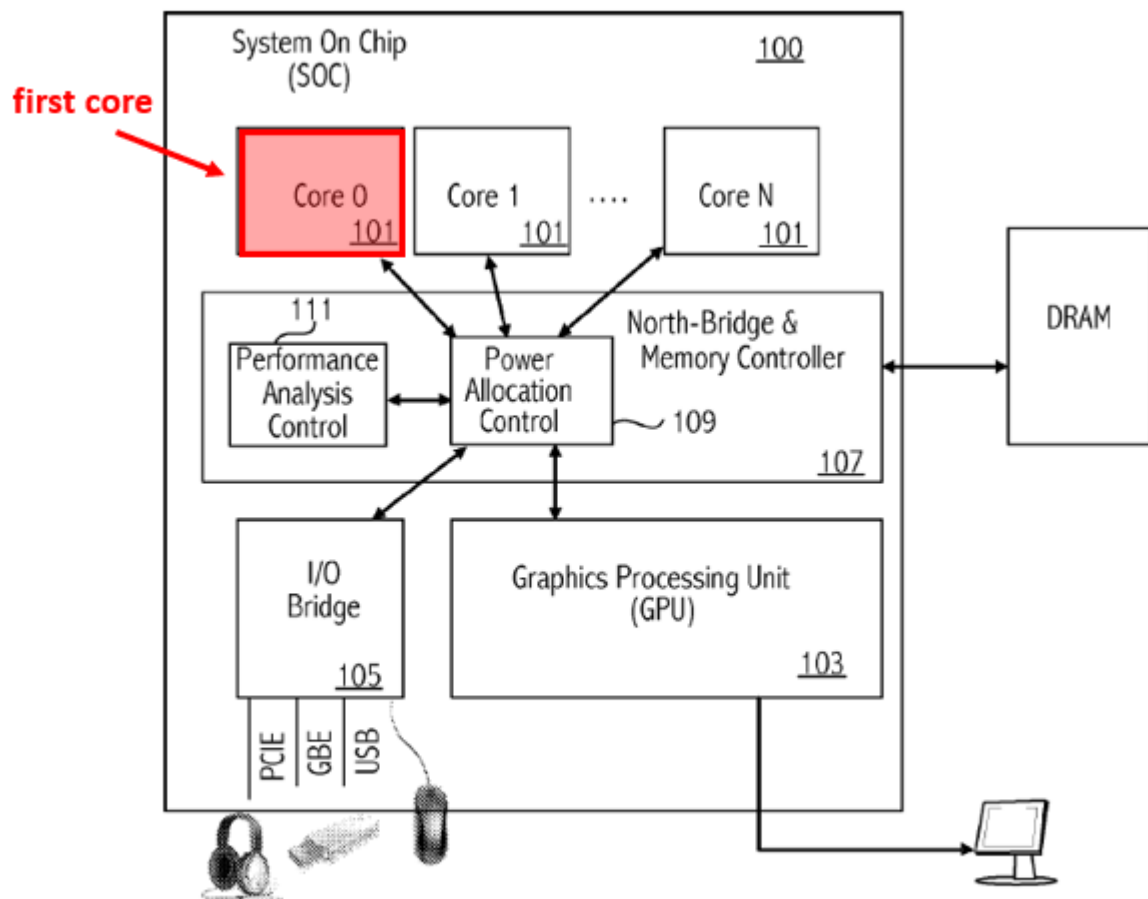


FIG. 1

(*Id.*, Figure 1 (annotated).) Nussbaum discloses that a “particular processor core may be in one of N performance states. A performance state is characterized by a unique pair of core voltage and frequency values.” (*Id.*, [0033].) Seven exemplary

performance states are described in Table 3:

TABLE 3

Core Performance States	Operational point (F, V)	Power (dynamic and static) consumed in this point	Remarks
P-boost	F-boost/V-boost	CoreBoostPwr	Boost point. Power budget of the Core has been exceeded
P0	F0/V0	Core_Pwr0	Core Power Budget
P1	F1/V1	Core_Pwr1	
P2	F2/V2	Core_Pwr2	
P3	F3/V3	Core_Pwr3	
Idle	Clocks Off/Low voltage	Core_Idle_Pwr	Core is either power gated or deep voltage is applied
Deep Cstate	Clocks Off/Power Off	Core_DeepCstate_Pwr	

(*Id.*, Table 3, [0033].) The seven listed performance states correspond to possible operational points of Core 0 having different frequencies (ranging from idle to F-Boost) and voltages (ranging from powered off to V-boost). (*Id.*) Additionally, Nussbaum discloses that the first core, Core 0, can be allocated a power budget of 8 W, 16.75 W, or 25.5 W and operate at a frequency or voltage that meets that budget. (*Id.*, [0021]-[0024], Tables 1-2.)

Thus, Core 0 is a “first core,” and as Nussbaum discloses, the particular voltage and frequency at which this core operates would be a first voltage and first

frequency, for example F0 and V0. (*Id.*; see also Horst Decl., ¶159.)

1[B]: a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

Nussbaum anticipates and/or renders obvious Claim 1[B]. (Horst Decl., ¶¶160-163.) Because Nussbaum discloses use of a plurality of logic cores, the “multiple CPU processing cores 101,” it discloses “a second core.” (Nussbaum, [0019], [0020].) Specifically, Nussbaum discloses a second core in Figure 1, showing Core 1 through Core N within SOC 100:

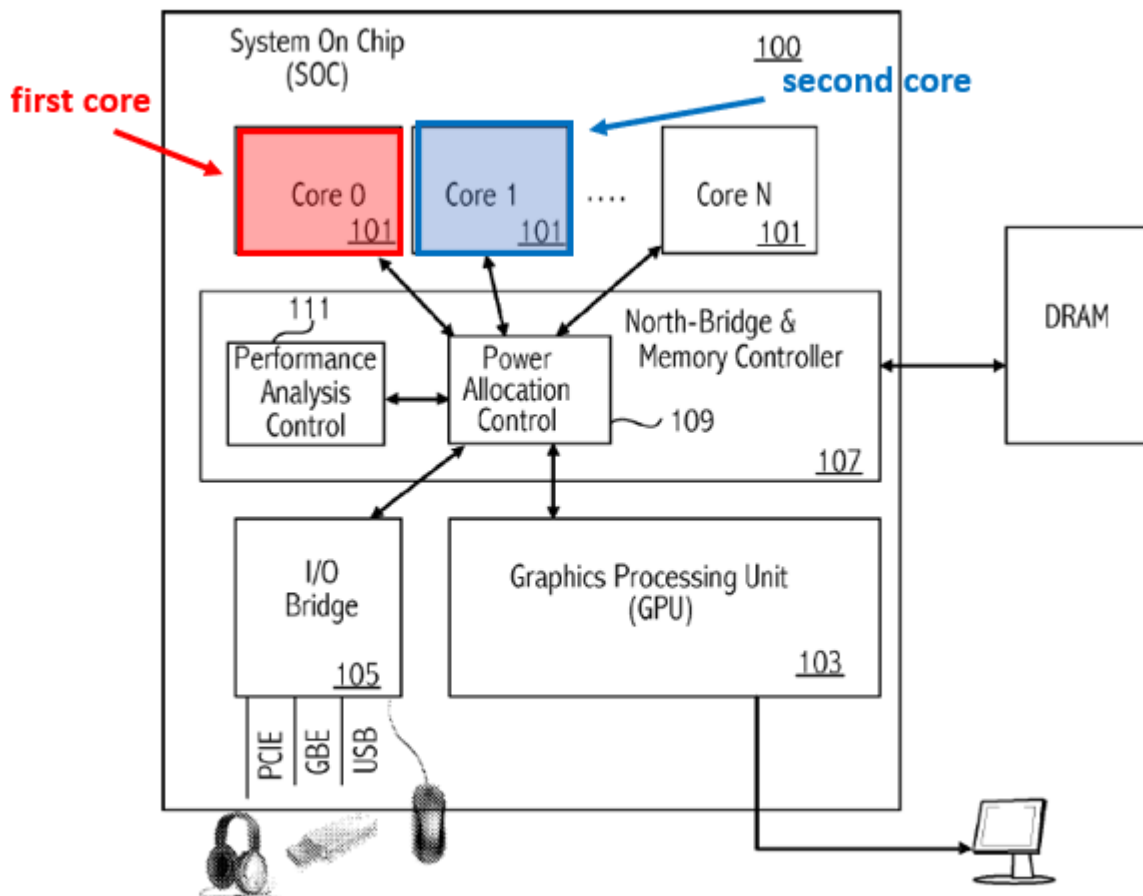


FIG. 1

(*Id.*, Figure 1 (annotated); *id.*, [0019], [0020].) As with Core 0, Nussbaum discloses that Core 1 through Core N can operate at one of “N performance states,” corresponding to the seven states shown in Table 3:

TABLE 3

Core Performance States	Operational point (F, V)	Power (dynamic and static) consumed in this point	Remarks
P-boost	F-boost/V-boost	CoreBoostPwr	Boost point. Power budget of the Core has been exceeded
P0	F0/V0	Core_Pwr0	Core Power Budget
P1	F1/V1	Core_Pwr1	
P2	F2/V2	Core_Pwr2	
P3	F3/V3	Core_Pwr3	
Idle	Clocks Off/Low voltage	Core_Idle_Pwr	Core is either power gated or deep voltage is applied
Deep Cstate	Clocks Off/Power Off	Core_DeepCstate_Pwr	

(*Id.*, Table 3, [0033].) The seven listed performance states correspond to possible operational points of Core 1 through Core N having different frequencies (ranging from idle to F-Boost) and voltages (ranging from powered off to V-boost). (*Id.*) Additionally, Nussbaum discloses that the second core, Core 1 through Core N, can be allocated a power budget of 0.5 W, 8 W, or 16.75 W each and operate at a frequency or voltage that meets that budget. (*Id.*, [0021]-[0024], Tables 1-2.)

Thus, one of Core 1 through Core N is a “second core,” and as Nussbaum discloses, the particular voltage and frequency at which this core operates would be a second voltage and second frequency, for example F1 and V1. (*Id.*; *see also* Horst Decl., ¶163.)

1[C]: graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and

Nussbaum anticipates and/or renders obvious Claim 1[C]. (Horst Decl., ¶¶164-170.) Nussbaum discloses that the SOC 100 may include “graphics processing circuitry” GPU 103. (Nussbaum, [0020].) GPU 103 is circuitry that performs graphics processing and operations that may, for example, interface with a graphics driver, graphics-related engine, or display. (*Id.*, [0034], Figure 1; Horst Decl., ¶165.)

As shown in Figure 1, GPU 103 is coupled to the plurality of cores—the aforementioned first and second cores such as Core 0 and Core 1 in SOC 100—through North-Bridge & Memory Controller 107:

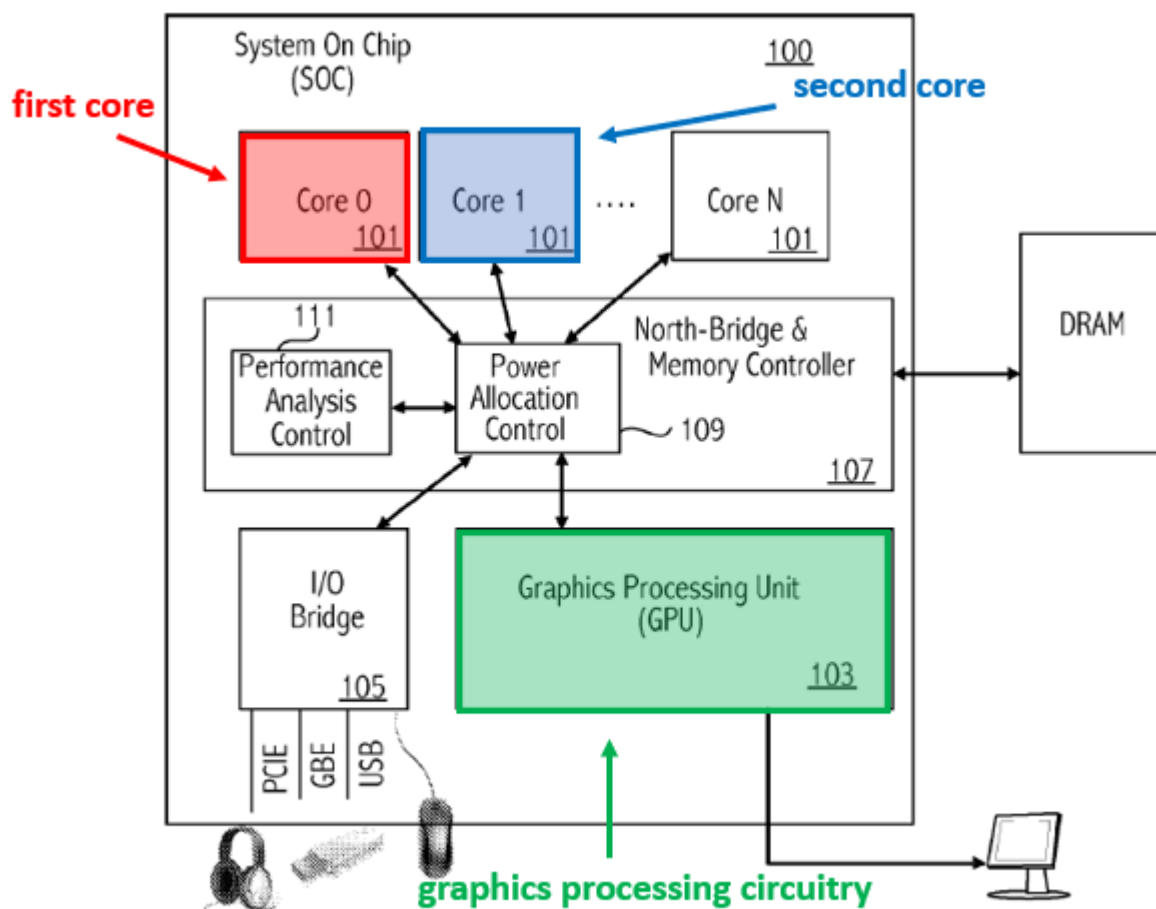


FIG. 1

(*Id.*, Figure 1 (annotated) [0020].) Nussbaum discloses that the GPU may operate in one of four performance states as shown in Table 4:

TABLE 4

GPU Performance States	GPU Power (dynamic and static) consumed in this point
GPU-boost	GPUBoostPwr
GPU_P0	GPU_Pwr0
GPU_P1	GPU_Pwr1
GPU_P2	GPU_Pwr2
GPU_P3	GPU_Pwr3

(*Id.*, Table 4, [0034].) Each of these performance states refers to a pair of “voltage and frequency values.” (*Id.*, [0033].) Additionally, Nussbaum discloses that GPU 103 can receive a power budget of 2.5 W or 5 W and operate at a frequency or voltage that meets that budget. (*Id.*, [0022]-[0023], Tables 1-2.)

Nusbaum further discloses throttling or boosting GPU performance compared to CPU cores depending on whether the SOC is executing a GPU-bounded or CPU-bounded application, which can be identified based on GPU and CPU utilization. (*Id.*, [0044]-[0049].) And the GPU and CPU cores may alternatively both be boosted by reallocation of the I/O module’s and memory controller’s unused power budget. (*Id.*, [0035].)

Thus, GPU 103 may operate at an independent third frequency that is different from the first and second frequencies of the first and second cores, respectively. (Horst Decl., ¶170.)

1/D]: an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first,

second, and third frequencies.

Nussbaum anticipates and/or renders obvious Claim 1[D]. (Horst Decl., ¶¶171-175.) Nussbaum discloses an interconnect, North-Bridge & Memory Controller 107, which couples the graphics processing circuitry—GPU 103—to a memory device, namely dynamic random-access memory (DRAM). (*Id.* ¶172; Nussbaum, Figure 1; [0020], [0049].) Figure 1 illustrates this coupling:

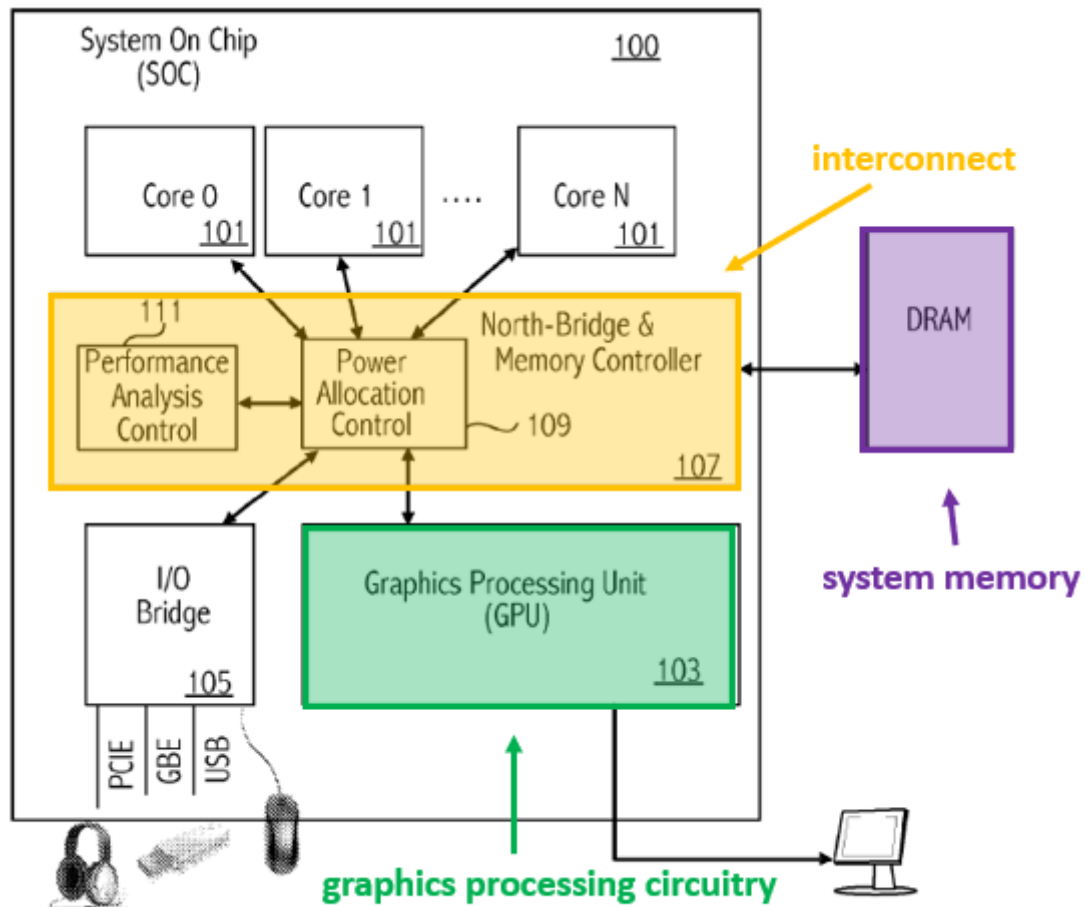


FIG. 1

(*Id.*, Figure 1 (annotated); [0020].)

Nussbaum further discloses that the North-Bridge & Memory Controller 107

can be independently throttled or boosted to operate at a higher or lower frequency depending on whether its power is being reallocated to another component, such as the CPU cores or GPU. (*Id.*, [0035] (explaining that “the memory controller may contribute to the boosting process of the cores or the GPU by reallocating its ‘unused’ power budget to these components” and “the memory controller may be boosted as well by transitioning the Dynamic Random Access Memory (DRAM) and its own frequency to a higher operational point”); *see also* [0023], Tables 1-2 (describing Memory Controller power budget of 2 W).)

A POSITA would understand that the power of a DRAM increases with higher frequency (a higher operational point). (Horst Decl., ¶175.) When a DRAM operates faster, the interconnect to memory must send or receive its data at a higher rate. (*Id.* ¶175.) Memory systems are typically designed such that the width of connection to memory cannot be dynamically changed, hence a change in the DRAM frequency necessarily means changing the frequency of sending or receiving data to the DRAM. (*Id.* ¶175.) Thus, the higher or lower frequencies of North-Bridge & Memory Controller 107 control the *interconnect* from the graphics processor to memory to be *operable at a (fourth) frequency different from the first, second, and third frequencies*. (*Id.* ¶175.)

(b) Independent Claim 8

Nussbaum anticipates and/or renders obvious Claim 8. (Horst Decl., ¶¶176-

180.) For purposes of this Petition, there are no substantive differences between Claim 1 and Claim 8, and Nussbaum anticipates and/or renders obvious Claim 8 for the same reasons as Claim 1. *See supra* VIII.B.1(a) (Ground 3, Claim 1). (*See also* Horst Decl., ¶177.)

A redline comparison between Claim 1 and Claim 8 is shown in Appendix A. As shown, Claim 8 recites features of a “system memory” (instead of a “memory device”) and that a “plurality of cores” is coupled to this system memory. Within the ’588, the “system memory” in Claim 8 is not distinguished from the “memory device” recited in Claim 1, and a POSITA would understand a “memory device” to include “system memory.” (Horst Decl., ¶179.) Thus, Nussbaum discloses the “system memory” in Claim 8 for the same reasons it discloses the “memory device” in Claim 1. *See supra* VIII.B.1(a) (Ground 3, Claim 1[D]). In particular, Nussbaum discloses that its “processor” includes system memory in the form of DRAM. (Nussbaum, Figures 1, [0035], [0049].)

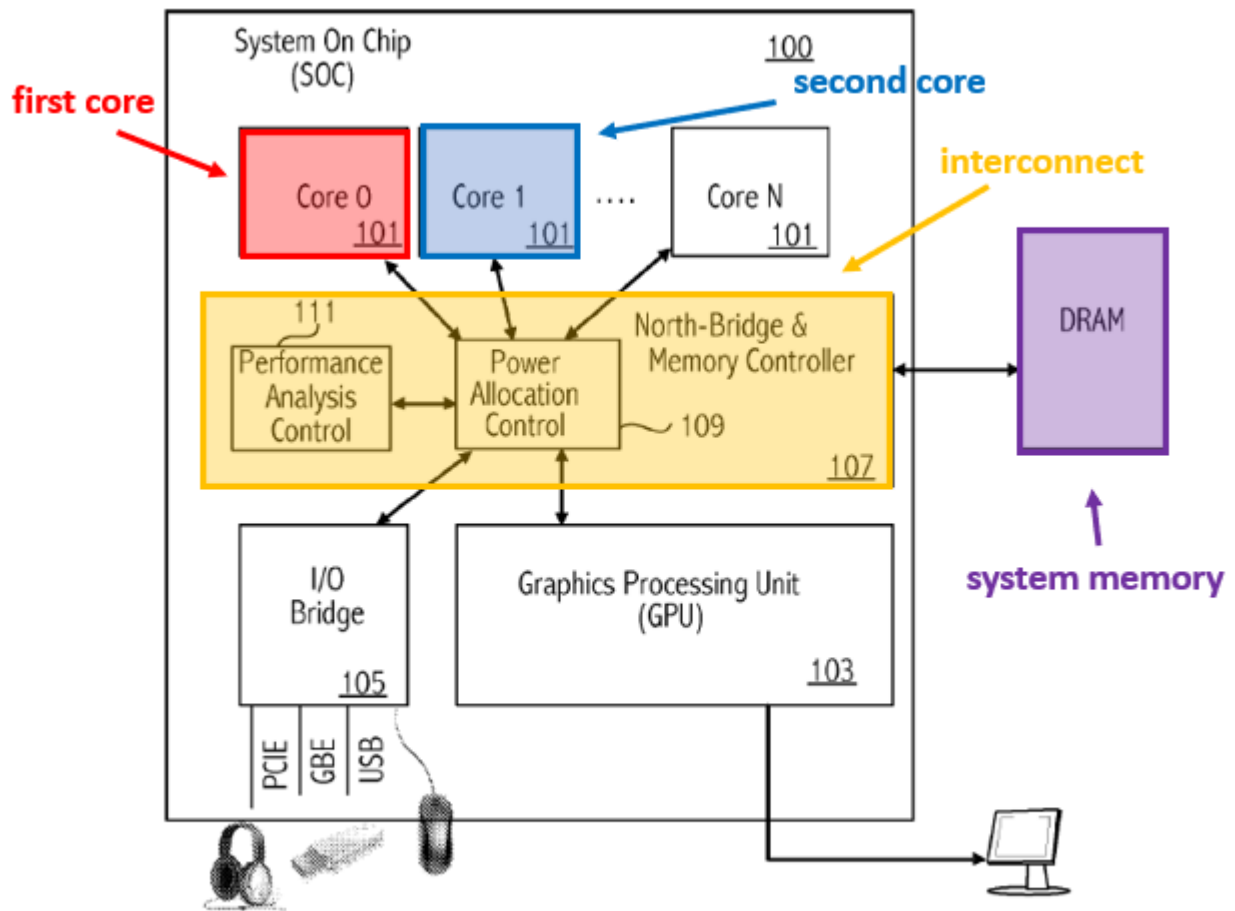


FIG. 1

(*Id.*, Figure 1 (annotated).)

As can be seen in Figure 1 above, Nussbaum also discloses that the DRAM (“system memory”) is coupled to a plurality of cores. (*Id.*, Figure 1; Horst Decl., ¶¶179-180.) In particular, DRAM is coupled to Core 0 and Core 1 through North-Bridge & Memory Controller 107. (Nussbaum, Figure 1.) Nussbaum further discloses that software executed by the cores is stored in the memory of Figure 1, which includes the disclosed DRAM. (*Id.*, Figure 1, [0043]; Horst Decl., ¶¶179-

180.)

(c) Independent Claim 20

Nussbaum anticipates and/or renders obvious Claim 20. (Horst Decl., ¶¶181-190.) Claim 20 is directed to an apparatus and was written in “means-plus-function” form to perform the functions of system Claim 1. A redline comparison between Claim 1 and Claim 20 is shown in Appendix B. The “functions” recited in Claim 20 are the same as those recited in Claim 1, so the analysis below cross-references the prior art analysis for Claim 1. (Horst Decl., ¶182.)

20[p]: An apparatus comprising:

Nussbaum anticipates and/or renders obvious Claim 20[p]. (Horst Decl., ¶¶183-184.) *See supra* Section VIII.B.1(a) (Ground 3, Claim 1[p]). For example, Nussbaum discloses System on a Chip (SOC) 100 having “multiple CPU processing cores 101, a GPU (Graphics Processing Unit) 103, an I/O Bridge 105 (named South-Bridge in some embodiments)[,] a North-Bridge 107 (which may be combined with the Memory Controller in some embodiments)[,]” DRAM, and a “power allocation controller 109.” (Nussbaum, [0020], Figure 1.)

20[A]: means for operating a first core at a first voltage and at a first frequency while concurrently operating a second core at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

Nussbaum anticipates and/or renders obvious Claim 20[A]. (Horst Decl., ¶¶185-186.) As described above and herein, Nussbaum discloses power allocation

control 109 configured to operate Core 0 and Core 1 at independent and distinct voltages and frequencies. (Nussbaum, [0020], [0039]-[0041], [0047], Figures 1, 5-6.) *See supra* Section VIII.B.1(a) (Ground 3, Claims 1[A]-1[B]); *see infra* Section VIII.B.1(d) (Ground 3, Claims 2 and 9). The corresponding structure of the '588 for operating first and second cores at different and independent frequencies and voltages is power control unit (PCU) 355/455. *See supra* Section VII.A.1 (Claim Construction). Nussbaum discloses such a PCU, as it discloses power allocation control 109. (*Id.*, Horst Decl., ¶186.)

20[B]: means for independently operating a graphics processor at a third frequency different from the first frequency and the second frequency; and

Nussbaum anticipates and/or renders obvious Claim 20[B]. (Horst Decl., ¶¶187-188.) As described above and herein, Nussbaum discloses power allocation control 109, graphics driver, and hardware tracking GPU activity to operate GPU 103 at an independent and distinct voltage and frequency. (Nussbaum, [0020], [0034], [0039]-[0041], [0047], Figures 1, 5-6.) *See supra* Section VIII.B.1(a) (Ground 3, Claim 1[C]); *see infra* Section VIII.B.1(f) (Ground 3, Claims 4 and 11). The corresponding structure of the '588 for operating a graphics processor at a frequency different from the frequencies of processing cores is power control unit (PCU) 355/455. *See supra* Section VII.A.1 (Claim Construction). Nussbaum discloses such a PCU because it discloses power allocation control 109, graphics

driver, and hardware tracking GPU activity. (*Id.*, Horst Decl., ¶188.)

20[C]: interconnect means to couple the graphics processor to a memory device, the interconnect means operable at a fourth frequency different from the first, second, and third frequencies.

Nussbaum anticipates and/or renders obvious Claim 20[C]. (Horst Decl., ¶¶189-190.) As described above, Nussbaum discloses North-Bridge & Memory Controller 107 that couples GPU 103 with DRAM and is operable at a fourth frequency different from the first, second, and third frequencies. (Nussbaum, Figure 1, [0020], [0035]-[0036], Tables 1-2; Horst Decl., ¶190.) *See supra* Section VIII.B.1(a) (Ground 3, Claim 1[D]). The corresponding structure of the '588 for coupling a graphics processor to a memory device, operable at a different frequency than the processing cores or graphics processor, is interconnect 315. *See supra* VII.A.3 (Claim Construction). Nussbaum discloses such an interconnect, as it discloses North-Bridge & Memory Controller 107. (Horst Decl., ¶190.)

(d) Dependent Claims 2 and 9

The [processor/system] of claim [1/8], further comprising: first power management circuitry and/or logic to cause the first core to operate at the first frequency and cause the second core to independently operate at the second frequency.

Nussbaum anticipates and/or renders obvious Claims 2 and 9. (Horst Decl., ¶191-192.) As discussed, Nussbaum discloses that processing cores 101 can operate at different voltages and frequencies, providing exemplary operational

points and power allocations. *See supra* Section VIII.B.1(a) (Ground 3, Claims 1[A]-1[B]). Nussbaum discloses that this is accomplished via “power management circuitry” in the form of power allocation controller 109, which controls the frequency and voltage of cores 101 by allocating power among components of SOC 100. (Nussbaum, [0020], [0024], [0033], [0039]-[0041], [0047], Tables 1-3, Figures 1, 5-6.) Nussbaum’s Figure 1 illustrates power allocation control 109 that causes Core 0 and Core 1 to independently operate at such different frequencies:

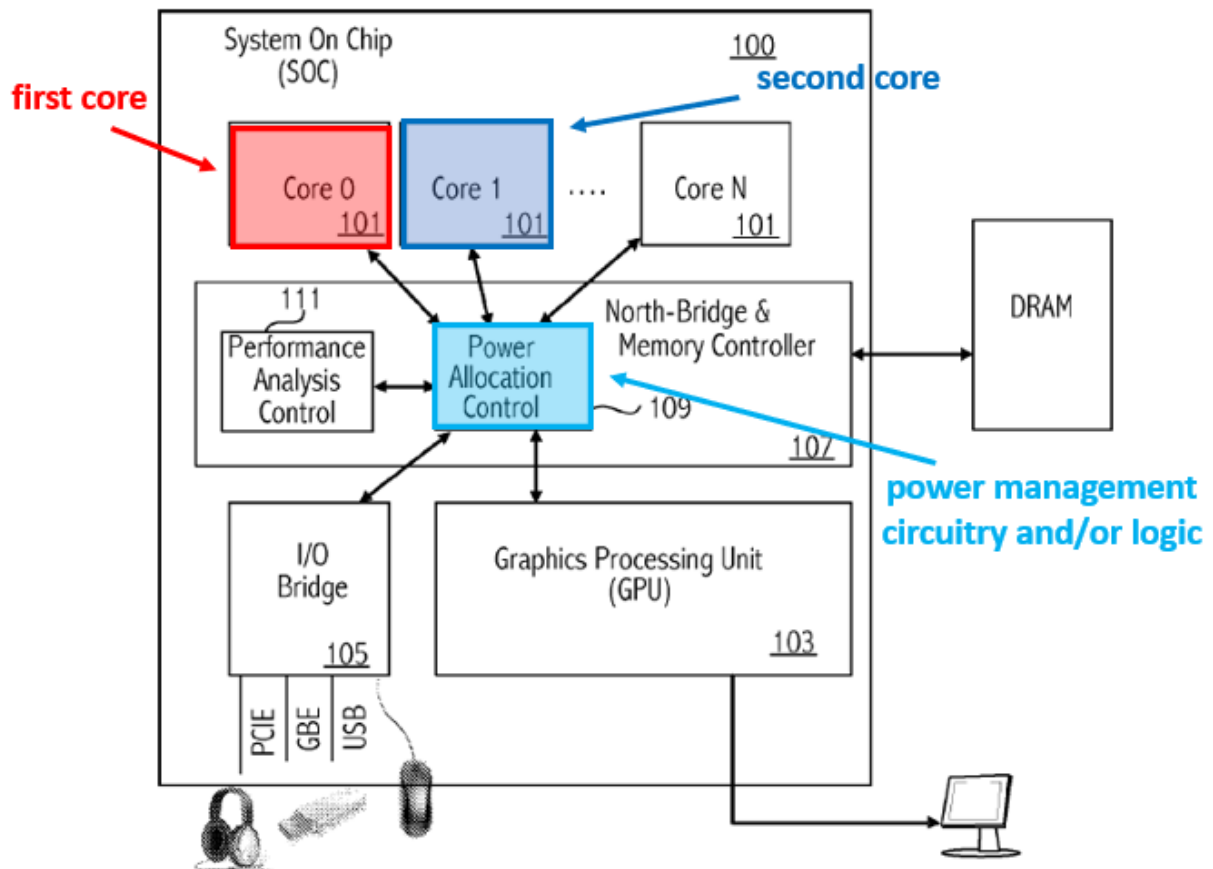


FIG. 1

(*Id.*, Figure 1 (annotated); *see also* Figures 5-6, [0020], [0039]-[0041].)

(e) Dependent Claims 3 and 10

The [processor/system] of claim [1/8], further comprising: a non-core power domain comprising a cache shared by the plurality of cores.

Nussbaum anticipates and/or renders obvious Claims 3 and 10. (Horst Decl., ¶¶193-194.) Nussbaum discloses System on a Chip (SOC) 100 having multiple CPU processing cores 101, GPU 103, I/O Bridge 105, and North-Bridge & Memory Controller 107. (Nussbaum, [0020], Figure 1, Tables 1-2.) A POSITA would understand that such a system on a chip would include a last level cache shared by multiple processing cores. (Horst Decl., ¶194.) Nussbaum moreover explicitly discloses that “[c]hanges in performance capability may also be provided by, e.g., a change in the amount of *cache* available to a core.” (Nussbaum, [0025] (emphasis added), *see also* [0047] (discussing “the amount of cache available to a core”), Claim 2 (describing change in “cache size” for a core).) Thus, A POSITA would understand Nussbaum to disclose a cache that is shared by the plurality of processing cores that is part of a non-core power domain. (Horst Decl., ¶194.)

(f) Dependent Claims 4 and 11

The [processor/system] of claim [2/9], further comprising: second power management circuitry and/or logic to cause the graphics processing circuitry to operate at the third frequency.

Nussbaum anticipates and/or renders obvious Claims 4 and 11. (Horst Decl., ¶¶195-196.) Nussbaum discloses that SOC 100 of Figure 1 includes “power

allocation control 109.” (Nussbaum, [0020], [0039]-[0041], [0047], Figures 1, 5-6.) Nussbaum further discloses that “GPU Power state is...controlled by software (the graphics driver)...[or] by hardware tracking the GPU activity and receiving information from other graphic-related engines (Unified Video Decoder (UVD), Display, etc.).” (*Id.*, [0034].) Nussbaum’s Figure 1 illustrates power allocation control 109 that causes GPU 103 to independently operate at different frequencies:

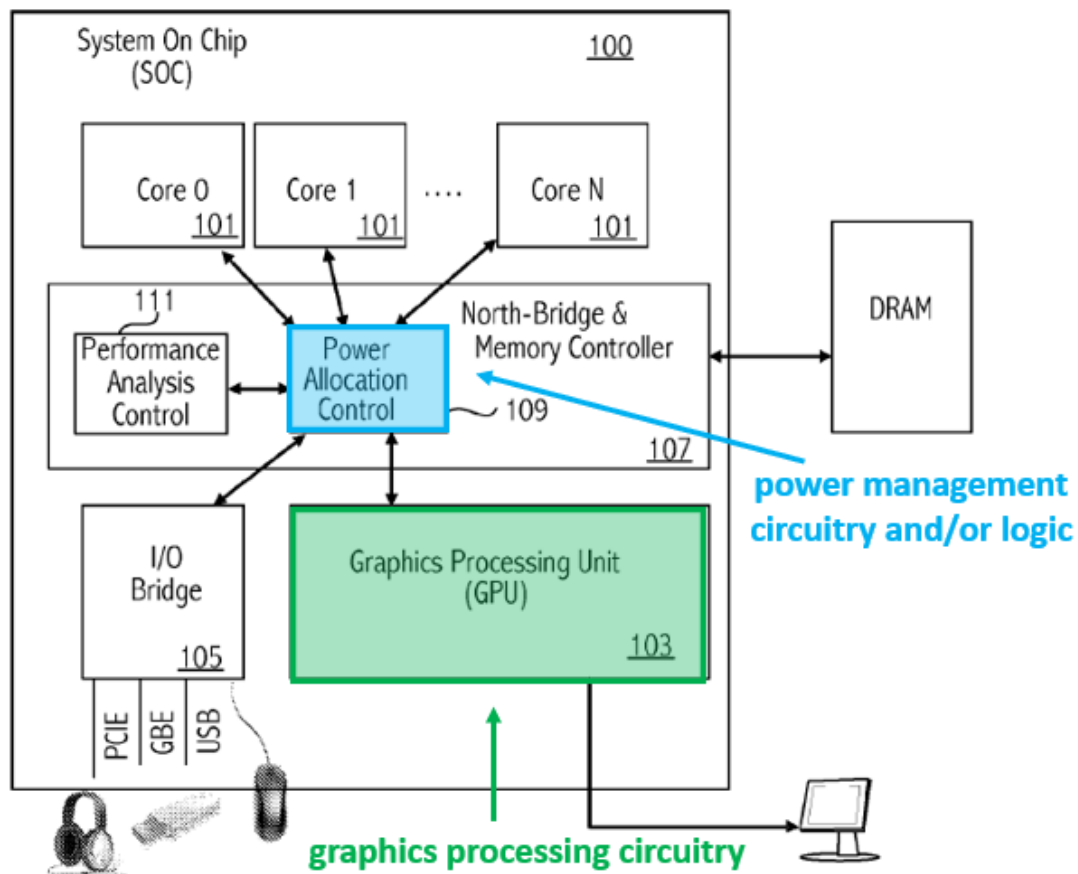


FIG. 1

(*Id.*, Figure 1 (annotated); see also Figures 5-6, [0020], [0039]-[0041].) See *supra* VIII.B.1(d) (Ground 3, Claims 2 and 9).

(g) Dependent Claims 7 and 14

The [processor/system] of claim [3/10], further comprising: power management circuitry and/or logic to cause the non-core power domain to operate at a different frequency from the first and second frequencies of the first and second cores, respectively.

Nussbaum anticipates and/or renders obvious Claims 7 and 14. (Horst Decl., ¶¶197-200.) Nussbaum discloses power allocation control 109, which allocates power among components of the SOC 100. (Nussbaum, Figure 1; Horst Decl., ¶198.) Nussbaum also discloses at Tables 1 and 2 that non-core I/O bridge 105 remains at 1 W despite a change in power allocated to the first and second cores:

TABLE 1	
On-die component	Allocated Power
first core → Core0	8 w
second core → Core1	8 w
Core2	8 w
Core3	8 w
GPU	5 w
Memory Controller	2 w
non-core → I/O Bridge	1 w
Total	40 w

(Nussbaum, Table 1 (annotated).)

TABLE 2

	On-die component	Allocated Power	Remarks
first core →	Core0	16.75 w	Core can run at higher F, V to fill new power headroom
second core →	Core1	16.75 w	Core can run at higher F, V to fill new power headroom
	Core2	0.5 w	Assume that idle core consumes 0.5 w
	Core3	0.5 w	Assume that idle core consumes 0.5 w
	GPU	2.5 w	
	Memory Controller	2 w	
non-core →	I/O Bridge	1 w	
	Total	40 w	

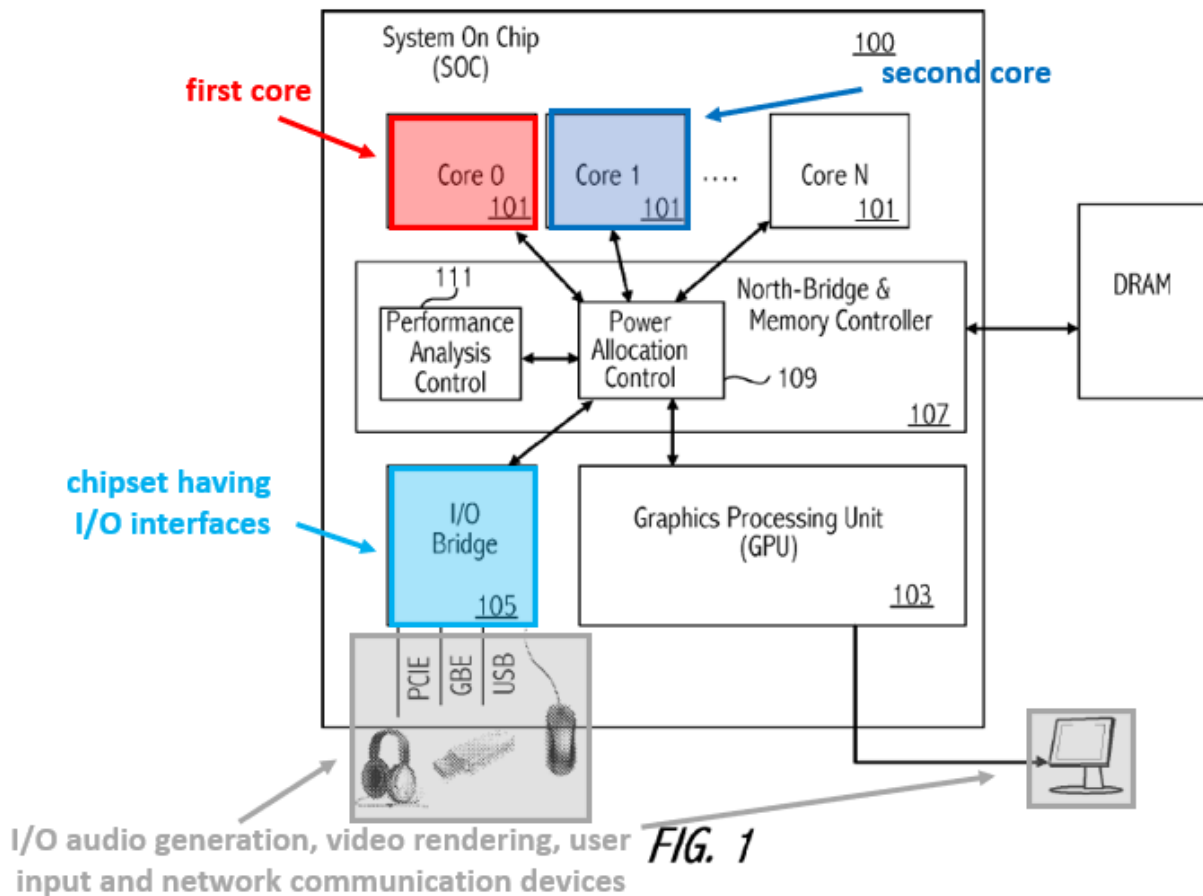
(*Id.*, Table 2 (annotated).) As seen above, each of Core0 – Core3 are allocated 8W of power and I/O Bridge is allocated 1W of power in the scenario shown in Table 1. (*Id.*; *see also* [0020]-[0024].) And in the exemplary scenario shown in Table 2, Core0-Core1 are allocated 16.75W of power, Core2-Core3 are allocated 0.5W power in idle state, and I/O Bridge is still allocated 1W of power. (*Id.*; *see also* [0020]-[0024].) Thus, the power allocation controller 109 can cause non-core I/O Bridge 105 “to operate at a different frequency from the first and second frequencies of the first and second cores, respectively,” because its allocated power (and thus frequency) remains constant when the allocated power (and frequency) of Core0-Core3 change. (Horst Decl., ¶¶199-200.)

(h) Dependent Claims 15-19

15: The system of claim 8, further comprising a chipset coupled to the plurality

of cores, the chip set comprising a plurality of interfaces to couple the cores to a plurality of I/O devices.

Nussbaum anticipates and/or renders obvious Claims 15. (Horst Decl., ¶¶201-203.) Nussbaum discloses, as seen in annotated Figure 1 below, that the SOC 100 includes a chipset I/O Bridge 105 (South-Bridge) to interface with peripherals, such as input/output devices, (Nussbaum, [0020]):



(Nussbaum, Figure 1 (annotated); [0020], [0034].) A POSITA would understand that I/O Bridge 105, as a southbridge, contains interfaces to couple the plurality of cores 101 (*i.e.*, Core0, Core1, et al.) to peripherals including input-output (I/O)

devices. (Horst Decl., ¶203.) Figure 1 discloses that such I/O devices can include PCIE devices, GBE (Gigabit Ethernet) devices, USB devices, mice, flash drives, and headphones. (*Id.* ¶¶202-203; Nussbaum, Figure 1.)

16: The system of claim 15, wherein one of the I/O devices comprises an audio generation device.

Nussbaum anticipates and/or renders obvious Claim 16. (Horst Decl., ¶¶204-205.) As shown in Figure 1 (annotated above), Nussbaum discloses PCIE and USB devices as well as audio headphones interfacing with the SOC through I/O Bridge 105. (Nussbaum, [0020], Figure 1.) A POSITA would understand that headphones are audio generation devices and PCIE and USB devices encompass audio generation devices, such as microphones, audio cards, and speakers. (Horst Decl., ¶205.)

17: The system of claim 16, wherein one of the I/O devices comprises a video rendering device.

Nussbaum anticipates and/or renders obvious Claim 17. (Horst Decl., ¶¶206-207.) As shown in Figure 1 (annotated above), Nussbaum discloses PCIE devices interfacing with the SOC through I/O Bridge 105 and a display. (Nussbaum, [0020], [0034].) A POSITA would understand that PCIE devices encompass video graphics cards, displays, and other devices that render video. (Horst Decl., ¶207.)

18: The system of claim 17, wherein one of the I/O devices comprises a user input device.

Nussbaum anticipates and/or renders obvious Claim 18. (Horst Decl., ¶¶208-209.) As shown in Figure 1 (annotated above), Nussbaum discloses PCIE and USB devices, a computer mouse, and a USB flash drive, and a POSITA would understand that PCIE and USB devices are capable of including microphones, audio cards, keyboards, and joysticks, among other peripherals interfacing with the SOC through I/O Bridge 105. (Nussbaum, [0020], Figure 1; Horst Decl., ¶209.) A POSITA would understand that these components are user input devices because they facilitate a user inputting information. (Horst Decl., ¶209.)

19: The system of claim 18, wherein one of the I/O devices comprises a network communication device.

Nussbaum anticipates and/or renders obvious Claim 19. (Horst Decl., ¶¶210-211.) As shown in Figure 1 (annotated above), Nussbaum discloses PCIE devices, GBE (Gigabit Ethernet) devices, and USB devices interfacing with the SOC through I/O Bridge 105. (Nussbaum, [0020], Figure 1.) A POSITA would understand that such PCIE devices, GBE devices, and USB devices include “network communication devices,” because each of PCIE, GBE, and USB support networking capabilities such as communicating over a wired ethernet or wireless Wi-Fi or Bluetooth network. (Horst Decl., ¶211.)

2. Ground 4: Claims 5-6 and 12-13 are obvious over Nussbaum in view of Shakkarwar

(a) Dependent Claims 5 and 12

The [processor/system] of claim [4/11], wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.

Nussbaum in view of Shakkarwar renders obvious Claims 5 and 12. (Horst Decl., ¶¶212-219.) As explained above in Section VIII.B.1(f) (Ground 3, Claims 4 and 11), Nussbaum discloses a second power management circuitry and/or logic. Nussbaum in view of Shakkarwar teaches that this power management circuitry would have been implemented to include a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect. (*Id.* ¶213.) *See* Section VIII.B.2(c) (Ground 4, Rationales to Combine Nussbaum and Shakkarwar).

Shakkarwar's dynamic power management system includes data controller 302 connected to graphics controller 305 through data connection 314, as illustrated in Figure 3:

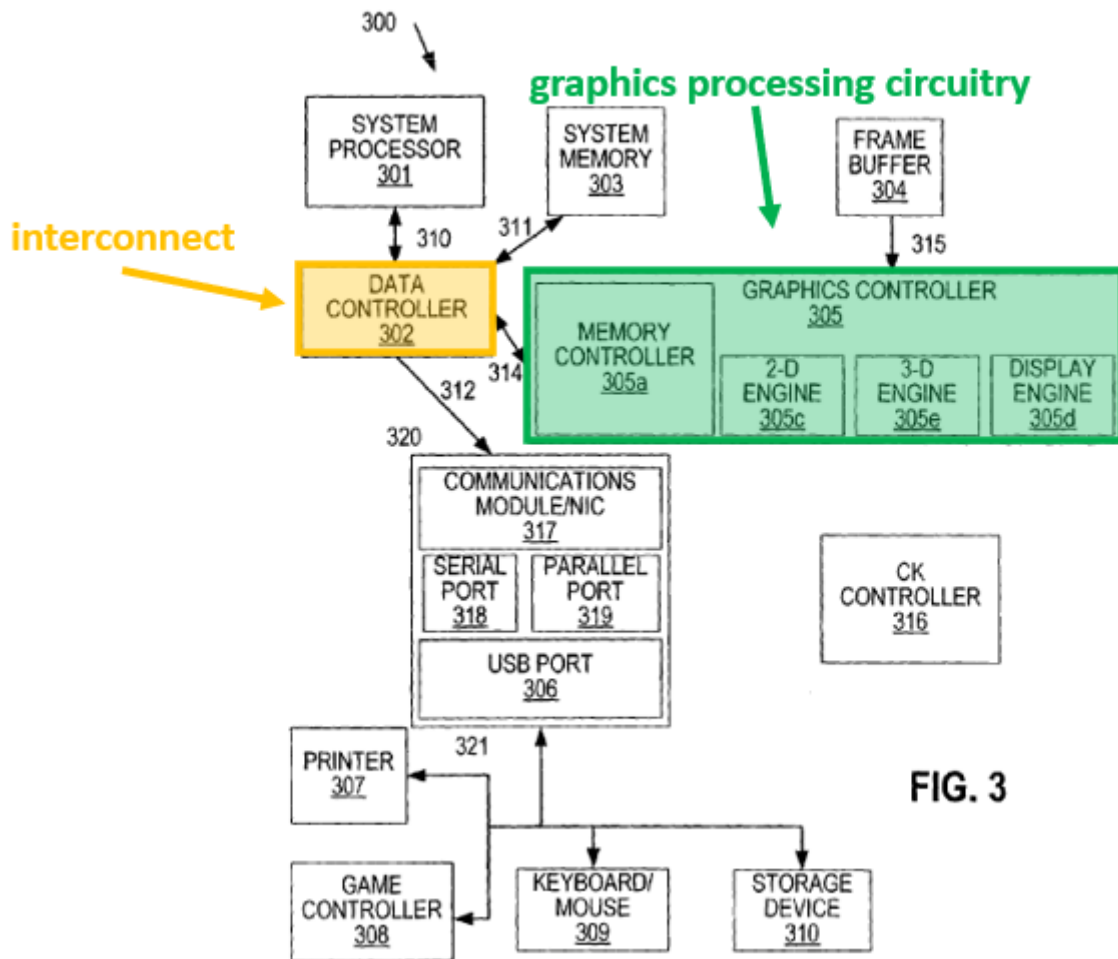


FIG. 3

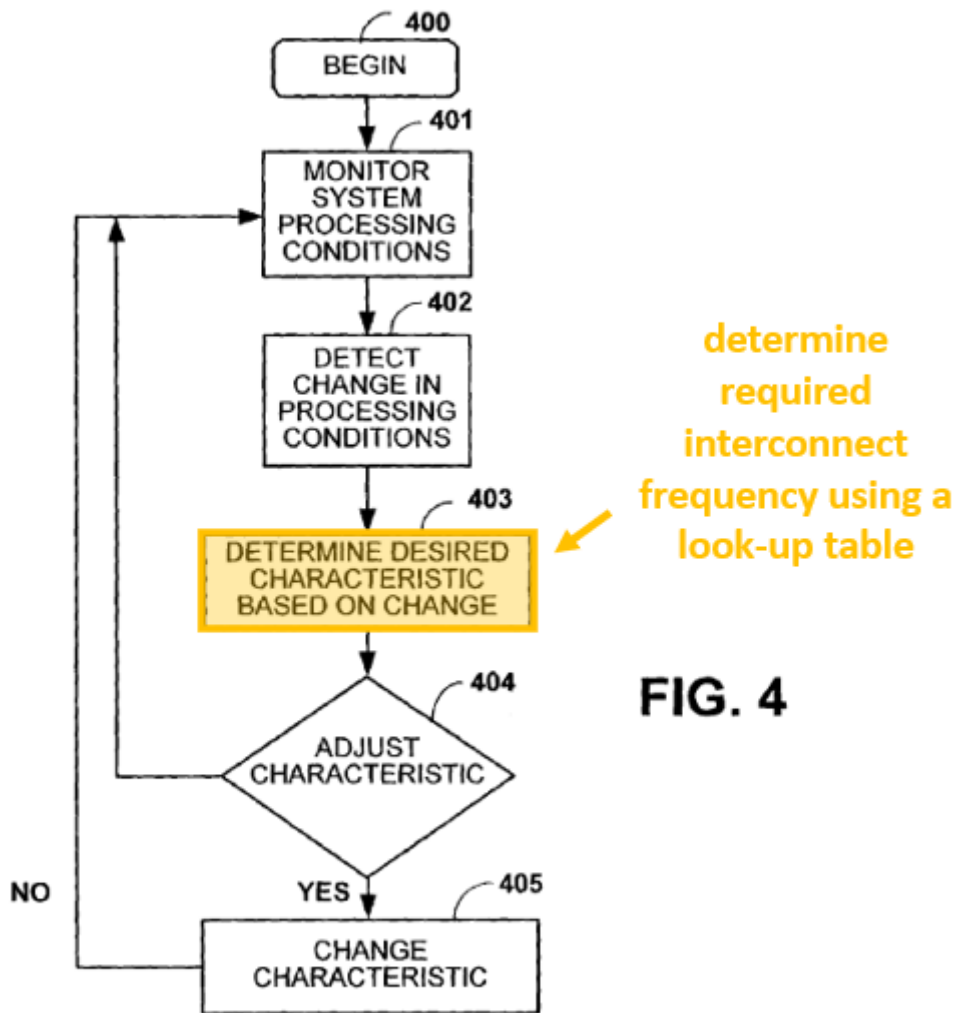
(Shakkarwar, Figure 3 (annotated).)

Data controller 302 connects graphics controller 305 and other components within Shakkarwar to each other and to system memory 303. (Shakkarwar, 5:10-15, Fig. 4.) Graphics controller 305 includes a “3-D engine 305e” and performs “3-D graphics operations...” (*Id.*, 6:7-16.) A POSITA would have thus understood that data controller 302 and data connection 314 are an “interconnect,” and the “graphics controller 305” is “graphics processing circuitry.” (Horst Decl., ¶215.)

Shakkarwar also maps selectable frequencies of the graphics processing

circuitry to selectable frequencies of the interconnect in a look-up table. (Horst Decl., ¶216; Shakkarwar, 7:5-10.) At step 401, Shakkarwar monitors “bandwidth for a component,” such as the interconnect or graphics processing circuitry, for “increasing or decreasing communication requirements.” (Shakkarwar, 6:41-43.) For example, “when an application that is known to use 3-D graphics is opened, system software can determine if the bus rate between the data controller [the ‘interconnect’] and the graphics controller [the ‘graphics processing circuitry’] is high enough to support the graphics requirements.” (*Id.*, 6:49-52; *see also* 7:5-10 (describing determining data connection bandwidth (*i.e.*, clock speeds/frequencies) required to process information for specific devices/groups of devices).)

At step 402, the system detects “a change in processing condition[s]” for a specific component, and upon detecting a change, it “determines bandwidth 403 for an associated data connection ***based on the active components.***” (Shakkarwar, 6:63-7:7; *see also* 7:7-10 (explaining that bandwidth can be determined with a look-up table containing “a list of clock speeds...required to process information for specific devices and/or groups of devices”).) To determine the appropriate bandwidth for a data connection, Shakkarwar utilizes “***a look-up table*** [that] may include ***a list of clock speeds, and/or voltage levels required to process information for specific devices and/or groups of devices.***” (*Id.*, 7:7-10.) Figure 4 illustrates this process:



(*Id.*, Figure 4 (annotated).) Shakkarwar thus teaches determining the appropriate bandwidth for a data connection to a module (e.g., graphics controller 305), utilizing a look-up table that includes a list of appropriate clock speeds. (*Id.*, 7:5-10; Horst Decl., ¶218.) It also considers other active components, such as the data controller 302 (the “interconnect”) and its clock speeds. (White, 7:5-10; Horst Decl., ¶218.) As such, a POSITA would have understood that Shakkarwar teaches

to map selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect using look-up tables. (Horst Decl., ¶218.)

A POSITA would have been motivated to implement these teachings of Shakkarwar, such as a look-up table, in Nussbaum for the reasons described above in Section VIII.B.2(c) (Ground 4, Rationales to Combine Nussbaum and Shakkarwar), including because Shakkarwar teaches that an advantage to its system is that it dynamically “manag[es] power consumption of electronic devices while satisfying bandwidth requirements for communicating and/or processing information.” (Shakkarwar, 2:34-39.) A POSITA would have been motivated to include this advantage in Nussbaum’s power allocation controller 109 to improve responsiveness and increase the ability of the system to respond to dynamically changing conditions, including the changing bandwidth requirements of Nussbaum’s components during various activity states. (Horst Decl., ¶219.)

(b) Dependent Claims 6 and 13

The [processor/system] of claim [5/12], wherein the second power management circuitry and/or logic is to select the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.

Nussbaum in view of Shakkarwar renders obvious Claims 6 and 13. (Horst Decl., ¶¶220-222.) As explained above, Nussbaum in view of Shakkarwar disclose second power management circuitry that determines bandwidth for an associated data connection based on the other active components by using a look-up table of

clock speeds required to process information for specific devices. *See* Section VIII.B.2(a) (Ground 4, Claims 5 and 12). Shakkarwar further discloses that “[a]t step 405, the data rate of a data connection is adjusted. In one embodiment, the data rate can be adjusted by adjusting operating of a clock generation device.” (Shakkarwar, 7:26-29.) Figure 4 illustrates adjusting the data rate of a data connection:

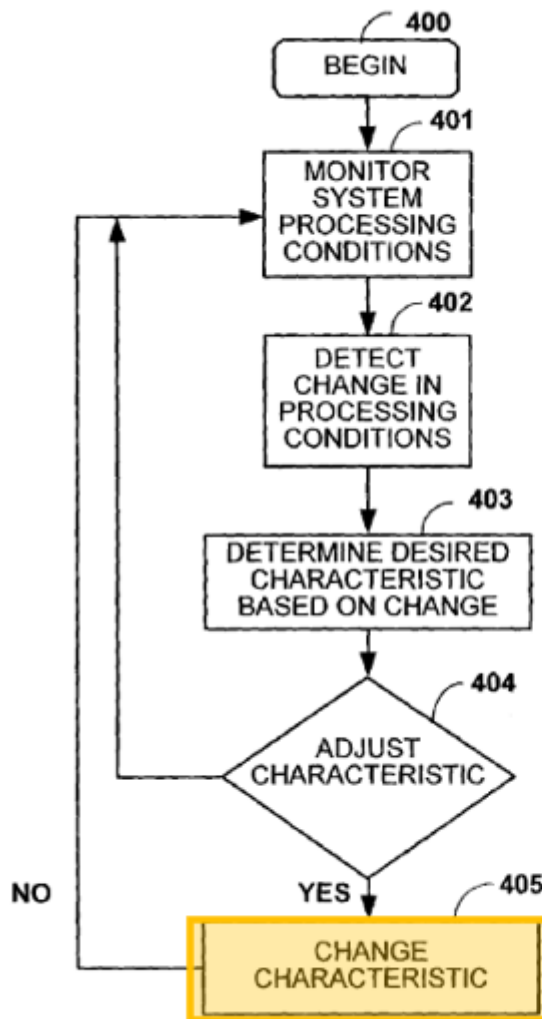


FIG. 4

interconnect frequency
changed based on
graphics processing
circuitry data
requirements

(*Id.*, Figure 4 (annotated).)

Shakkarwar also specifically discloses selecting “the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.” (Horst Decl., ¶222.) Shakkarwar discloses that “when an application that is known to use 3-D graphics is opened, system software can determine if *the bus rate between the data controller [the “interconnect”] and the graphics controller [the “graphics processing circuitry”] is high enough to support the graphics requirements.*” (Shakkarwar, 6:49-52 (emphasis added); *see also* Shakkarwar 7:5-10 (describing determining data connection bandwidth 403 (*i.e.*, clock speeds/frequencies) required to process information for specific devices/groups of devices).) A POSITA would have understood that by applying these teachings from Shakkarwar to Nussbaum, the fourth frequency for the interconnect would be selected based on detecting the frequency of the graphics processing circuitry. (Horst Decl., ¶222.)

(c) Combining Nussbaum’s and Shakkarwar’s teachings would have been obvious to a POSITA.

In addition to the reasons set forth above, combining the teachings of Nussbaum and Shakkarwar would have been obvious to a POSITA, a POSITA would have been motivated to do so, and a POSITA would have had a reasonable expectation of success in doing so because each relates to the same well-known technologies. (Horst Decl., ¶¶223-227.) Both relate to and describe similar

methods for optimizing performance between multiple components within a computer system. (Nussbaum, [0002]; Shakkarwar, Abstract.)

Nussbaum discloses a system where power is allocated among computing components to improve performance and efficiency. (Nussbaum, [0019].)

Nussbaum discloses adjusting the frequency, voltage, and power of CPU processors, GPU, and North-Bridge & Memory Controller 107 to optimize thermal budget and efficiently use computing power. (Nussbaum, Figures 1, 5-6, [0019]-[0024], [0033], [0035], [0039], [0044].) Nussbaum also relies on preparing and updating boost sensitivity tables to best allocate power during operation. (*Id.*, [0026]-[0032].)

Similarly, Shakkarwar relates to the “efficient use of electronic devices and, more particularly, to systems and methods for power management of electronic devices.” (Shakkarwar, 1:8-10.) Shakkarwar discloses “[s]ystems and methods for dynamic power management of electronic devices” so that “power consumption of the system may be dynamically managed while providing sufficient bandwidth for the system.” (Shakkarwar, Abstract.) Shakkarwar dynamically manages power by monitoring a component’s “bandwidth...for increasing or decreasing communication requirements.” (*Id.*, 6:41-43.) The system then detects “a change in processing condition[s]” for a component, and upon detecting a change, “determines bandwidth 403 for an associated data connection based on the active

components.” (*Id.*, 6:63-7:7; *see also* 7:7-10 (explaining that bandwidth can be determined with a look-up table containing “a list of clock speeds...required to process information for specific devices and/or groups of devices”).) The data rate “of a data connection is [then] adjusted,” including by adjusting a clock frequency or voltage, to reach optimal performance levels. (*Id.*, 7:26-29.) In this manner, “power consumption associated with communicating and processing information via data buses may be optimized while satisfying bandwidth requirements for the computer system.” (*Id.*, 3:17-20; *see also* 2:12-15, Claim 21.)

A POSITA would have been motivated to combine the teachings of Nussbaum in view of Shakkarwar because she would have recognized the predictable benefit of implementing the known technique of a look-up table for dynamically managing power, such as taught by Shakkarwar, to optimize performance of components within a processor as taught by Nussbaum. (Horst Decl., ¶226.) As noted, Shakkarwar teaches that an advantage to its system is that it dynamically “manag[es] power consumption of electronic devices while [also] satisfying bandwidth requirements for communicating and/or processing information.” (*Id.*, 2:34-39.) Nussbaum already discloses using tables in its power management methods, (*id.*, [0026]-[0032],) so a POSITA would be motivated to use and find it obvious to try such tables to choose map selectable frequencies of the North-Bridge & Memory Controller 107 to selectable frequencies of GPU 103.

(Horst Decl., ¶¶226.)

A POSITA would also have had a reasonable expectation of success in combining the teachings of Nussbaum in view of Shakkarwar. (Horst Decl., ¶227.) A POSITA would have understood that these references disclose interrelated teachings based on routine technologies that would have been amenable to various well-understood and predictable combinations, as explained below. (*Id.*) The teachings of Shakkarwar are compatible and incorporating such teachings into Nussbaum would be well within the expertise of a POSITA using known methods for fabricating computer systems. (*Id.*)

IX. DISCRETIONARY CONSIDERATIONS UNDER 35 U.S.C. § 314(A) AND 325(D) FAVOR INSTITUTION.

A. *Fintiv*

The Board should institute review because Petitioner has been diligent in filing the Petition, and the circumstances surrounding the parallel district court cases and International Trade Commission investigations do not warrant discretionary denial under § 314(a). *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 11-21 (Dec. 1, 2020) (precedential) (citing *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar 20, 2020) (precedential)). A *Fintiv* analysis shows that discretionary denial is not applicable to this proceeding, as Petitioner has been dismissed from any pending litigation in district court and

terminated from any pending ITC investigations. *See, e.g., Boss Corp. v. Koss Corp.*, IPR2021-00680, Paper 15 at 14 (PTAB Oct. 13, 2021). Moreover, any parallel district court and ITC proceedings were dismissed early-on, before *Markman* or any substantive decisions. The remaining district court and ITC actions do not include Petitioner, and it is purely speculative that any tribunal will address the distinct invalidity challenges raised in this Petition.

B. *General Plastic*

The *General Plastic* factors do not weigh in favor of denying institution. *Gen. Plastic Industrial Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (Sept. 6, 2017) (Section II.B.4.i precedential).

Factor 1 examines whether the same petitioner or a related petitioner previously filed a petition directed to the same claims of the same patent. *Gen. Plastic at 16; see also Valve Corp. v. Electronic Scripting Products, Inc.*, IPR2019-00062, Paper 11 (PTAB Apr. 2, 2019) (precedential) (“*Valve I*”); *Valve Corp. v. Electronic Scripting Products, Inc.*, IPR2019-00064, Paper 10 (PTAB May 1, 2019) (precedential) (“*Valve II*”). Factor 1 strongly favors institution. Petitioner here has not filed any previous petitions challenging the ’588. While this Petition challenges the same claims at issue in the previously filed Qualcomm IPR, Petitioner has no relationship with Qualcomm and Samsung (the original petitioners in the Qualcomm IPR), and Petitioner played no role in the preparation

or filing of the Qualcomm IPR. Moreover, Petitioner was not a party to the pending parallel ITC case involving Qualcomm (and in fact is not a party to any currently pending case), and Petitioner was sued separately on distinct products in ITC Inv. No. 337-TA-1332 as compared to the products at issue in the pending ITC case against Qualcomm. Thus, unlike in *Valve*, there is no evidence that there is a “significant relationship” between Petitioner and Qualcomm.

Factors 2, 4, and 5 examine Petitioner’s knowledge of the prior art, and the elapse of time between filings of the petitions. These factors weigh in favor of institution. This is Petitioner’s first petition against the ’588, and thus the issue of whether Petitioner could have raised the prior art at issue here in the earlier Qualcomm IPR is not relevant. (Petitioner, having no relationship with Qualcomm or the Qualcomm IPR, could not have done so.) Further, this Petition relies on distinct combinations of references as compared to those used in the Qualcomm IPR. This Petition relies on White and Nussbaum as the primary references in its challenges to the claims, neither of which are at issue in the Qualcomm IPR. Moreover, there is no unreasonable delay in the filing of this petition, as Petitioner is not a party to any pending litigation involving the ’588.

Factor 3 examines “roadmapping” concerns, which are not present here. This Petition relies on separate combinations of references than the Qualcomm IPR, Petitioner had no involvement in the Qualcomm IPR, and no Institution

Decision has issued in the Qualcomm IPR.

Factors 6 and 7, addressing the finite resources of the Board, favor institution or at most neutral. This is Petitioner's first Petition challenging the '588, and the separate grounds presented in the Petition provide a basis for timely resolving the issues of this review.

C. 35 U.S.C. § 325(d).

Denial of institution under § 325(d) is not appropriate. Shakkarwar and Nussbaum were not presented to the patent office during prosecution of the '588. And although White was cited during prosecution of the '588 (among over 180 references submitted by the Applicant in an April 3, 2019, IDS) White was not discussed or mentioned by the Examiner in any Office Action. Ex-1002, 0046-50, 0106-137 (citing White in IDS at 0120). Thus, the Examiner erred "in a manner material to the patentability of challenged claims" in allowing the patent to issue without substantively discussing White or considering the arguments presented by Petitioner herein. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 at 8-9 (PTAB Feb. 13, 2020) (precedential).

"The Board has frequently held that a reference that 'was neither applied against the claims nor discussed by the Examiner' does not weigh in favor of exercising the Board's discretion under § 325(d) to deny a petition." *RTI Surgical, Inc. v. LifeNet Health*, IPR2019-00572, Paper 20, at 40 (PTAB Aug. 12, 2019)

(citations omitted); *see also Microsoft Corp. v. Parallel Networks*, IPR2015-00486, Paper 10, 2015 WL 4760578, at *8 (PTAB July 15, 2015) (rejecting argument that institution be denied under Section 325(d) because, though listed on an IDS, “the references were not applied against the claims and there is no evidence that the Examiner considered the particular disclosures cited by...the Petition”). Indeed, nothing suggests such undiscussed references received anything more than “[c]ursory consideration [that] weighs against exercising discretion to deny under § 325(d).” *See Intex Recr. Corp. v. Team Worldwide Corp.*, IPR2018-00871, Paper 14 at 13 (PTAB Sept. 14, 2018); *see also Mylan Pharma. Inc. v. Bayer Parma AG*, IPR2022-00517, Paper 15 at 12 (PTAB Aug. 9, 2022) (noting that “we cannot speculate as to why the Examiner did not apply the references from those search results to the claims”).

Should Patent Owner attempt to analogize any previously considered art or arguments to those presented here, Petitioner reserves the right to respond.

The Board should institute review because the merits are strong, and the circumstances here do not support discretionary denial policy considerations. Should Patent Owner raise any discretionary denial theory not addressed above, Petitioner reserves the right to respond before institution.

X. CONCLUSION

For the reasons above, petitioner respectfully requests institution of *inter*

partes review and cancellation of claims 1-20 of U.S. Patent No. 10,705,588 as
anticipated or obvious over the prior art.

Date: August 23, 2023

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APPENDIX A

Redline Comparison Between Claims 1 and 8 of the '588 Patent

Claim ~~8~~ 1
A ~~processor-system~~ comprising:
~~a system memory;~~
a plurality of cores ~~coupled to the system memory;~~
~~including~~ a first core ~~of the plurality of cores~~ operable at a first voltage and at a first frequency, and
a second core ~~of the plurality of cores~~ operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;
graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and
an interconnect to couple the graphics processing circuitry to ~~the system memory~~ a memory device , the interconnect operable at a fourth frequency different from the first, second, and third frequencies.

APPENDIX B

Redline Comparison Between Claims 1 and 20 of the '588 Patent

Claim ~~20~~
~~An~~ <u>processor apparatus</u> comprising:
~~a plurality of cores including means for operating~~ a first core ~~operable~~ at a first voltage and at a first frequency ~~while concurrently, and~~
~~operating~~ a second core ~~operable~~ at a second voltage independent of the first voltage and at a second frequency different from the first frequency;
~~graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry means for~~ independently ~~operating a graphics processor~~ ble at a third frequency different from the first frequency and the second frequency; and
~~an~~ interconnect ~~means~~ to couple the graphics process ~~ing circuitry~~ to a memory device, the interconnect ~~means~~ operable at a fourth frequency different from the first, second, and third frequencies.

CERTIFICATE OF COMPLIANCE

The undersigned hereby certifies that the foregoing **Petition for *Inter Partes* Review** contains 13,991 words, excluding those portions identified in 37 C.F.R. § 42.24(a), as measured by the word-processing system used to prepare this paper.

/s/ Joseph J. Raffetto
Joseph J. Raffetto (Reg. No. 66,218)
*One of the attorneys for Petitioner
Mercedes-Benz USA, LLC*

CERTIFICATION OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, the foregoing were served on August 23, 2023, by filing this document through the Patent Trial and Appeal Board P-TACTS System and by Priority Mail Express[®] or by means at least as fast and reliable as Priority Mail Express[®] at the following address of record for the '588:

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