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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/138,505	07/31/2018	10037067	ITL.2492C2US (P38407C2)	3621

47795 7590 07/11/2018

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 79 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Avinash N. Ananthakrishnan, Portland, OR;
Intel Corporation, Santa Clara, CA;
Inder M. Sodhi, Folsom, CA;
Efraim Rotem, Haifa, ISRAEL;
Doron Rajwan, Rishon Le-Zion, ISRAEL;
Eliezer Weissmann, Haifa, ISRAEL;
Ryan Wells, Folsom, CA;

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Petitioner Mercedes Ex-1009, 0001

PTO/SB/47 (03-09)
Approved for use through 07/31/2018. OMB 0651-0016
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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☒ Customer Number: 00197

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	15/138,505

Completed by (check one):

☐ Applicant/Inventor

☒ Attorney or Agent of record 42,117 (Reg. No.)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☐ Assignee recorded at Reel Frame

/Mark J. Rozman/
Signature

Mark J. Rozman
Typed or printed name

512-418-9944
Requester's telephone number

2018-05-29
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ * Total of forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15138505
Filing Date:	26-Apr-2016
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth In A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/David Hopper
Attorney Docket Number:	ITL.2492C2US (P38407C2)

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	32740899
Application Number:	15138505
International Application Number:	
Confirmation Number:	3621
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth In A Processor
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/David Hopper
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2492C2US (P38407C2)
Receipt Date:	29-MAY-2018
Filing Date:	26-APR-2016
Time Stamp:	13:03:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	052918INTEFSW13044500
Deposit Account	201504
Authorized User	David Hopper

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	ITL2492C2US-Fee-Trans.pdf	1048661 ec9bf7d2f48fd66cbfdbbab0f5863c94a9691a15	no	1
Warnings:					
Information:					
2	Maintenance Fee Address Change	ITL2492C2US-Fee-Address.pdf	1031775 0ed1172dedfa262336aaaf1c224b13ae28d2959e	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30797 ef126b1998b3089577f126ec6557421b08491bfb	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2111233		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

47795 7590 03/28/2018
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1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/138,505	04/26/2016	Avinash N. Ananthakrishnan	ITL.2492C2US (P38407C2)	3621

TITLE OF INVENTION: Enabling A Non-Core Domain To Control Memory Bandwidth

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	06/28/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAN, RAYMOND NGAN	2185	713-320000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Trop, Pruner & Hu, P.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Intel Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 20-1504 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Mark J. Rozman/ Date 2018-05-29

Typed or printed name Mark J. Rozman Registration No. 42,117

Petitioner Mercedes Ex-1009, 0008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
Serial No.:	15/138,505	§		
		§	Examiner:	Unassigned
Filed:	April 26, 2016	§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Under 35 U.S.C. §120, this application relies on the earlier filing date of application serial number 14/451,807, filed August 5, 2014, which is a continuation of U.S. Patent Application Serial No. 13/282,896, filed October 27, 2011, now U.S. Patent No. 8,832,478, issued September 9, 2014. To the extent that any following foreign patent or non-patent literature references were submitted to and/or cited by the Office in the prior application, they are not provided in this application (pursuant to 37 C.F.R. §1.98(d) and M.P.E.P. §609.02(A)(2)).

Please apply any charges or credits to Deposit Account No. 50-4238.

Respectfully submitted,

Date: July 8, 2016

/Mark J. Rozman/
Mark J. Rozman
Registration No. 42,117
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, Texas 77057-2631
(512) 418-9944 [Phone]
(713) 468-8883 [Fax]
Customer No.: 47795

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8832478		2014-09-09	Ananthakrishnan, et al.	

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.N.P/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2 (P38407C2)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7434073		2008-10-07	Magklis	
	2	6792392		2004-09-14	Knight	
	3	7194643		2007-03-20	Gonzalez, et al.	
	4	7010708		2006-03-07	Ma	
	5	5621250		1997-04-15	Kim	
	6	7412615		2008-08-12	Yokota, et al.	
	7	5163153		1992-11-10	Cole, et al.	
	8	5590341		1996-12-31	Matter	

Petitioner Mercedes Ex-1009, 0011

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(P38407)

	9	5931950		1999-08-03	Hsu	
	10	7454632		2008-11-18	Kardach, et al.	
	11	5522087		1996-05-28	Hsiang	
	12	7272730		2007-09-18	Acquaviva, et al.	
	13	7529956		2009-05-05	Stufflebeam	
	14	7730340		2010-06-01	Hu, et al.	
	15	7539885		2009-05-26	Ma	
	16	6748546		2004-06-08	Mirov, et al.	
	17	6829713		2004-12-07	Cooper, et al.	
	18	7111179 ~~71111179~~		2006-09-19	Girson, et al.	
	19	6823516		2004-11-23	Cooper	

Petitioner Mercedes Ex-1009, 0012

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	20	7437270		2008-10-14	Song, et al.	
	21	7093147		2006-08-15	Farkas, et al.	
	22	7043649		2006-05-09	Terrell	
	23	6996728		2006-02-07	Singh	

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090150695		2009-06-11	Song, et al.	
	2	20090150696		2009-06-11	Song, et al.	
	3	20110154090		2011-06-23	Dixon, et al.	
	4	20070214342		2007-09-13	Newburn	
	5	20070079294		2007-04-05	Knight	

Petitioner Mercedes Ex-1009, 0013

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.N.P/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(2)/P38407(2)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6908227		2005-06-21	Fusu, et al.	
	2	7797512		2010-09-14	Cheng, et al.	
	3	7146514		2006-12-05	Kaushik, et al.	
	4	8015427		2011-09-06	Miller, et al.	
	5	7966511		2011-06-21	Naveh, et al.	
	6	7434073		2008-10-07	Magklis, et al.	

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U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear

Petitioner Mercedes Ex-1009, 0014

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2(P38407C2)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7603577		2009-10-13	Yamaji, et al.	
	2	7624215		2009-11-24	Axford, et al.	
	3	7752467		2010-07-06	Tokue	

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	1	20120096288		2012-04-19	Bates, et al.	
	2	20080136397		2008-06-12	Gunther, et al.	
	3	20080307240		2008-12-11	Dahan, et al.	

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Doc description: Information Disclosure Statement (IDS) Filed

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	1	7624215		2009-11-24	Axford, et al.	
	2	7752467		2010-07-06	Tokue	
	3	7146514		2006-12-05	Kaushik, et al.	

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	1	20080136397		2008-06-12	Gunther, et al.	
	2	20080307240		2008-12-11	Dahan, et al.	
	3	20120116599		2012-05-10	Arndt, et al.	

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	1	7949887		2011-05-24	Gunther, et al.	
	2	8370551		2013-02-05	Ohmacht, et al.	
	3	8407319		2013-03-26	Chiu, et al.	
	4	6983389		2006-01-03	Filippo	
	5	7263457		2007-08-28	White, et al.	

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	1	20060053326		2006-03-09	Naveh, et al.	

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	1	7574321		2009-08-11	Kernahan, et al.	
	2	8601288		2013-12-03	Brinks, et al.	
	3	7596464		2009-09-29	Hermerding, et al.	

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	1	20090271646		2009-10-29	Talwar, et al.	
	2	20070101174		2007-05-03	Tsukimori, et al.	
	3	20080307240		2008-12-11	Dahan, et al.	

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	1	5287292		1994-02-15	Kenny, et al.	

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	1	20050288886		2005-12-29	Therien, et al.	
	2	20070106428		2007-05-10	Omizo, et al.	
	3	20080077282		2008-03-27	Hartman, et al.	
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	5	20120114010		2012-05-10	Branch	

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	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C3US (P38407C2)

	4	20100058078		2010-03-04	Branover, et al.	
	5	20110093733		2011-04-21	Kruglick	
	6	20070168151		2007-07-19	Kernahan, et al.	
	7	20060006166		2006-01-12	Chen, et al.	
	8	20100250856		2010-09-03	Owen, et al.	

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	1	I342498	TW		2011-05-21	Asustek Comp Inc.		☒
	2	I344793	TW		2011-07-01	IND TECH RES INST		☒

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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(2)P38407(2)

	6	20060117202		2006-06-11	Magklis, et al.	
	7	20070016817		2007-01-18	Albonesi, et al.	
	8	20060053326		2006-03-09	Naveh	
	9	20070005995		2007-01-04	Kardach, et al.	
	10	20040098560		2004-05-02	Storvik, et al.	
	11	20060050670		2006-03-09	Hillyard, et al.	
	12	20060059286		2006-03-16	Bertone, et al.	
	13	20060184287		2006-08-17	Belady, et al.	
	14	20070106827		2007-05-10	Boatright, et al.	
	15	20080028240		2008-01-31	Arai, et al.	
	16	20090158061		2009-06-18	Schmitz, et al.	

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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	17	20010044909		2001-11-22	Oh, et al.	
	18	20050022038		2005-01-27	Kaushik, et al.	
	19	20070156992		2007-07-05	Jahagirdar	
	20	20050033881		2005-02-10	Yao	
	21	20040064752		2004-04-01	Kazachinsky, et al.	
	22	20040139356		2007-07-15	Ma	
	23	20070239398		2007-10-11	Song, et al.	
	24	20060069936		2006-03-30	Lint, et al.	
	25	20020194509		2002-12-19	Plante, et al.	
	26	20050132238		2005-06-16	Nanja	
	27	20070245163		2007-10-18	Lu, et al.	

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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(P38407)

	28	20040268166		2004-12-30	Farkas, et al.	
	29	20090006871		2009-01-01	Liu, et al.	
	30	20100115309		2010-05-06	Carvalho, et al.	
	31	20100191997		2010-07-29	Dodeja, et al.	
	32	20100146513		2010-06-10	Song	
	33	20090235105		2009-09-17	Branover, et al.	
	34	20090172428		2009-07-02	Lee	
	35	20090172375		2009-07-02	Rotem, et al.	
	36	20090158067		2009-06-18	Bodas, et al.	
	37	20080250260		2008-10-09	Tomita	
	38	20030061383		2003-03-27	Zilka	

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Application Number	11513850S
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

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	1	20090292935		2009-11-26	Hallnor, et al.	
	2	20080316950		2008-12-25	Damnjanovic	
	3	20080168287		2008-07-10	Berry, et al.	

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	1	201009567	TW		2010-03-01	Hallnor, et al.		X

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	Examiner Name	
	Attorney Docket Number	ITL.2492C2US (P38407C2)

	2	200917694	TW		2009-04-16	Damnjanovic		☒
	3	200839497	TW		2008-10-01	Berry, et al.		☒

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	1	Taiwan Intellectual Property Office, Office Action mailed November 2, 2015 in Taiwan Patent Application no. 103146274.	X

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	1	20110022865		2011-01-27	Gunther, et al.	
	2	20080005603		2008-01-03	Deep, et al.	
	3	20090070605		2009-03-12	Nijhawan, et al.	

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	4	20120116599		2012-05-10	Arndt, et al.	

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	Attorney Docket Number	ITL.2492C2P38407(C2)

	1	20090313489		2009-12-17	Gunther, et al.	
	2	20100332927		2010-12-30	Kurts, et al.	
	3	20070234083		2007-10-04	Lee	
	4					
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	6					
	7	20110072429		2011-03-24	Celeskey, et al.	
	8	20050046400		2005-03-03	Rotem	
	9	20090271646		2009-10-29	Talwar, et al.	

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	Attorney Docket Number	ITL.2492C2(P38407C2)

	6	20070260895		2007-11-08	Aguilar, et al.	
	7	20060041766		2006-02-23	Adachi	

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	2	20080005603		2008-01-03	Buch, et al.	

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Petitioner Mercedes Ex-1009, 0030

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	4	20090271141		2009-10-29	Coskun, et al.	
	5	20080028778		2008-02-07	Millet	
	6	20120053897		2012-03-01	Naffziger	
	7	20050223258		2005-10-06	Watts	
	8	20050046400		2005-03-03	Rotem	
	9	20120110352		2012-05-03	Branover, et al.	
	10	20090235108		2009-09-17	Gold, et al.	
	11	20120066535		2012-03-15	Naffziger	
	12	20080077813		2008-03-27	Keller, et al.	
	13	20110283124		2011-11-17	Branover, et al.	
	14	20120173907		2012-07-05	Moses, et al.	

Petitioner Mercedes Ex-1009, 0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	15	20130246825		2013-09-19	Shannon	

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Petitioner Mercedes Ex-1009, 0032

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

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	1	101403944	CN	A	2009-04-08	Gunther, et al.		☒
	2	101351759	CN	A	2009-01-21	ADVANCED MICRO DEVICES INC		☒
	3	101010655	CN	B	2010-05-26	INTEL CORP		☒

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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Application Number	15138505
Filing Date	2016-04-26
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Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

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	1	201120628	TW		2011-06-16	Hansquine, et al.		☒
	2	201040701	TW		2010-11-16	Pedersen, et al.		☒

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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
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	1	EP 1 282 030	EP	A1	2003-05-02	Mitsubishi Kenki Kabushiki Kaisha		☐

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	1	U.S. Patent Application No. 12/889,121, "Providing Per Core Voltage and Frequency Control," filed September 23, 2010, by Pakaj Kumar.	☐
	2	SPEC-Power and Performance, Design Overview V1.10, Standard Performance Information Corp., October 21, 2008, 6 pages.	☐
	3	U.S. Patent Application No. 13/070,700, "Obtaining Power Profile Information With Low Overhead," filed March 24, 2011, by Robert Knight.	☐
	4	ANOOP IYER, et al., "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors," 2002, pages 1-11.	☐
	5	GREG SEMERARO, et al., "Hiding Synchronization Delays In A GALS Processor Microarchitecture," 2004, pages 1-13.	☐
	6	JOAN-MANUEL PARCERISA, et al., "Efficient Interconnects for Clustered Microarchitectures," 2002, pages 1-10.	☐

Petitioner Mercedes Ex-1009, 0035

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	Application Number	15 138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	1	KR 10-2006-012846	KR		2006-12-14	LG Electronics Inc.		☐

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	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	7	GRIGORIOS MAGKLIS, et al., "Profile-Based Dynamic Voltage and Frequency Scalling for a Multiple Clock Domain Microprocessor," 2003, pages 1-12.	☐
	8	GREG SEMERARO, et al., "Dynamic Frequency and Voltage Control for a Multiple Clock Domain Architecture," 2002, pages 1-12.	☐
	9	GREG SEMERARO, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," 2002, pages 29-40.	☐
	10	DIANA MARCULESCU, "Application Adaptive Energy Efficient Clustered Architectures," 2004, pages 344-349.	☐
	11	L. BENINI, et al., "System-Level Dynamic Power Management," 1999, pages 23-31.	☐
	12	RAVINDRA JEJURIKAR, et al., "Leakage Aware Dynamic Voltage Scaling For Real-Time Embedded Systems," 2004, pages 275-280.	☐
	13	RAVINDRA JEJURIKAR, et al., "Dynamic Slack Reclamation With Procrastination Scheduling In Real-Time Embedded Systems," 2005, pages 13-17.	☐
	14	R. TODLING, et al., "Some Strategies For Kalman Filtering and Smoothing," 1996, pages 1-21.	☐
	15	R.E. KALMAN, "A New Approach To Linear Filtering and Prediction Problems," 1960, pages 1-12.	☐
	16	INTEL TECHNOLOGY JOURNAL, "Power and Thermal Management in the Intel Core Duo Processor," May 15, 2006, pages 109-122.	☐
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	AVINASH N. ANANTHAKRISHNAN, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	1	U.S. Patent Application Serial No. 13/285,414, filed October 31, 2011, entitled "CONTROLLING A TURBO MODE FREQUENCY OF A PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2494)	☐
	2	U.S. Patent Application Serial No. 13/225,677, filed September 6, 2011, entitled "DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2495)	☐
	3	U.S. Patent Application Serial No. 13/247,580, filed September 28, 2011, entitled "CONTROLLING TEMPERATURE OF MULTIPLE DOMAINS OF A MULTI-DOMAIN PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2496)	☐
	4	U.S. Patent Application Serial No. 13/285,465, filed October 31, 2011, entitled "DYNAMICALLY CONTROLLING CACHE SIZE TO MAXIMIZE ENERGY EFFICIENCY," by AVINASH N. ANANTHAKRISHNAN, et al. (2497)	☐
	5	U.S. Patent Application Serial No. 13/282,947, filed October 27, 2011, entitled "CONTROLLING OPERATING FREQUENCY OF A CORE DOMAIN VIA A NON-CORE DOMAIN OF A MULTI-DOMAIN PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2493)	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C3US (P38407C3)

	1	U.S. Patent and Trademark Office, Office Action mailed July 31, 2014, in U.S. application no. 13/247,564. (2491)	☐
	2	U.S. Patent and Trademark Office, Office Action mailed January 16, 2014, with Reply filed April 9, 2014, in U.S. application no. 13/247,564. (2491)	☐
	3	U.S. Patent and Trademark Office, Office Action mailed June 6, 2014, with Reply filed September 4, 2014, in U.S. application no. 13/282,947. (2493)	☐
	4	U.S. Patent and Trademark Office, Office Action mailed May 16, 2014, with Reply filed August 12, 2014, in U.S. application no. 13/285,414. (2494)	☐
	5	U.S. Patent and Trademark Office, Final Office Action mailed May 14, 2014, with Request for Continued Examination filed August 13, 2014, in U.S. application no. 13/247,580. (2496)	☐
	6	U.S. Patent and Trademark Office, Office Action mailed August 18, 2014, in U.S. application no. 13/285,465. (2497)	☐

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Petitioner Mercedes Ex-1009, 0039

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	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	2184
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	1	Taiwan Patent Office, Office action mailed August 21, 2014, in Taiwan application no.101135884.	☐
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	1	DAVID L. HILL, et al., "The Uncore: A Modular Approach To Feeding The High-Performance Cores," Intel Technology Journal, 2010, Vol 14, Issue 3, pages 30-49.	☐
	2	INTERNATIONAL SEARCHING AUTHORITY, "Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority," mailed March 28, 2013, in International application no. PCT/US2012/057655.	☐

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	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2492C2US (P38407C2)

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

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Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2016-07-08
Name/Print	Mark J. Rozman	Registration Number	42,117

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15/138,505	04/26/2016	2185	1740	ITL.2492C2US (P38407C2)	1	1

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Inventor(s)

Avinash N. Ananthakrishnan, Portland, OR;
Inder M. Sodhi, Folsom, CA;
Efraim Rotem, Haifa, ISRAEL;
Doron Rajwan, Rishon Le-Zion, ISRAEL;
Eliezer Weissmann, Haifa, ISRAEL;
Ryan Wells, Folsom, CA;

Applicant(s)

Intel Corporation, Santa Clara, CA;

Power of Attorney: The patent practitioners associated with Customer Number 47795

Domestic Priority data as claimed by applicant

This application is a CON of 14/451,807 08/05/2014 PAT 9354692
which is a CON of 13/282,896 10/27/2011 PAT 8832478

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Petitioner Mercedes Ex-1009, 0043

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/09/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/138,505**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

Enabling A Non-Core Domain To Control Memory Bandwidth In A Processor

Preliminary Class

713

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Petitioner Mercedes Ex-1009, 0046

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

47795 7590 03/28/2018

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
PHAN, RAYMOND NGAN	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 03/28/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/138,505	04/26/2016	Avinash N. Ananthakrishnan	ITL.2492C2US (P38407C2)	3621

TITLE OF INVENTION: Enabling A Non-Core Domain To Control Memory Bandwidth

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	06/28/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Petitioner Mercedes Ex-1009, 0047

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

47795 7590 03/28/2018
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/138,505	04/26/2016	Avinash N. Ananthakrishnan	ITL.2492C2US (P38407C2)	3621

TITLE OF INVENTION: Enabling A Non-Core Domain To Control Memory Bandwidth

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	06/28/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAN, RAYMOND NGAN	2185	713-320000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Petitioner Mercedes Ex-1009, 0048

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/138,505	04/26/2016	Avinash N. Ananthakrishnan	ITL.2492C2US (P38407C2)	3621

47795 7590 03/28/2018

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 03/28/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Petitioner Mercedes Ex-1009, 0049

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/138,505	Applicant(s) ANANTHAKRISHNAN ET AL.	
	Examiner RAYMOND PHAN	Art Unit 2185	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Terminal Disclaimer filed on January 26, 2018*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *22-41*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 012618
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/RAYMOND PHAN/
Primary Examiner, Art Unit 2185

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	RAYMOND PHAN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/29/2017	03/22/2018							
	1	-	-							
	2	-	-							
	3	-	-							
	4	-	-							
	5	-	-							
	6	-	-							
	7	-	-							
	8	-	-							
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1	22	=	=							
2	23	=	=							
3	24	=	=							
8	25	=	=							
4	26	=	=							
5	27	=	=							
6	28	=	=							
7	29	=	=							
9	30	=	=							
10	31	=	=							
11	32	✓	=							
12	33	✓	=							
13	34	✓	=							
14	35	✓	=							
17	36	✓	=							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	RAYMOND PHAN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/29/2017	03/22/2018							
15	37	✓	=							
16	38	✓	=							
18	39	=	=							
19	40	=	=							
20	41	=	=							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	RAYMOND PHAN	2185

CPC							
Symbol						**Type**	**Version**
G06F		1	/	324		F	2013-01-01
G06F		1	/	3293		I	2013-01-01
G06F		1	/	3203		I	2013-01-01
G11C		7	/	22		I	2013-01-01
G06F		13	/	4282		I	2013-01-01
G06F		1	/	3296		I	2013-01-01
G06F		13	/	4068		I	2013-01-01
Y02D		10	/	122		A	2018-01-01
Y02D		10	/	126		A	2018-01-01
Y02D		10	/	151		A	2018-01-01
			/				
			/				
			/				
			/				
			/				

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/RAYMOND PHAN/ Primary Examiner.Art Unit 2185	03/22/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

Petitioner Mercedes Ex-1009, 0054

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	RAYMOND PHAN	2185

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
710	320	G 0 6 F 1 / 26 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/RAYMOND PHAN/ Primary Examiner.Art Unit 2185	03/22/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	**Art Unit**
	RAYMOND PHAN	2185

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17	12	33										
	2		18	13	34										
	3		19	14	35										
	4		20	17	36										
	5		21	15	37										
	6	1	22	16	38										
	7	2	23	18	39										
	8	3	24	19	40										
	9	8	25	20	41										
	10	4	26												
	11	5	27												
	12	6	28												
	13	7	29												
	14	9	30												
	15	10	31												
	16	11	32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/RAYMOND PHAN/ Primary Examiner.Art Unit 2185 (Primary Examiner)	03/22/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 5

Petitioner Mercedes Ex-1009, 0056

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	Art Unit
	RAYMOND PHAN	2185

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 1/26; 1/30	09/25/17	RP
UPDATED CPC	03/20/18	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
G06F 1/3203	09/25/17	RP
UPDATED ABOVE CPC	03/20/18	RP

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300-340	09/25/17	RP
	UPDATED CL;ASS/SUBCLASSES	03/20/18	RP

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST SEARCHES	09/25/17	RP
CHECK PALM FOR DOUBLE PATENTING	09/25/17	RP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
713	320	03/22/18	RP
G06F	1/3203	03/22/18	RP

	/RAYMOND PHAN/ Primary Examiner.Art Unit 2185

Petitioner Mercedes Ex-1009, 0057

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.N.P/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2185
Examiner Name	Raymond Ngan Phan
Attorney Docket Number	ITL.2492C2US (P38407C2)

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20100238693		2010-09-23	Jeddeloh	
	2	20100115304		2010-05-06	Finkelstein, et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	201040962	TW		2010-11-16	Jeddeloh		☓
	2	201022923	TW		2010-06-16	Finkelstein, et al.		☒

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.N.P/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	2185
	Examiner Name	Raymond Ngan Phan
	Attorney Docket Number	ITL.2492C2US (P38407C2)

If you wish to add additional Foreign Patent Document citation information please click the Add button [Add]

NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Taiwan Intellectual Property Office, First Office Action mailed January 8, 2018 in Taiwanese Patent Application no. 105140882. (Translation Redacted)	X

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature	/RAYMOND N PHAN/	Date Considered	03/24/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	2185
	Examiner Name	Raymond Ngan Phan
	Attorney Docket Number	ITL.2492C2US (P38407C2)

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2018-01-26
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2185
Examiner Name	Raymond Ngan Phan
Attorney Docket Number	ITL.2492C2US (P38407C2)

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	Attorney Docket Number	ITL.2492C2US (P38407C2)

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Taiwan Intellectual Property Office, First Office Action mailed January 8, 2018 in Taiwanese Patent Application no. 105140882. (Translation Redacted)	X

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Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2018-01-26
Name/Print	Mark J. Rozman	Registration Number	42,117

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Espacenet

Bibliographic data: TW201040962 (A) — 2010-11-16

Configurable bandwidth memory devices and methods

Inventor(s): JEDDELOH JOE M [US] ± (JEDDELOH, JOE M)

Applicant(s): MICRON TECHNOLOGY INC [US] ± (MICRON TECHNOLOGY, INC)

Classification: - international: *G11C11/34*
- cooperative: G06F13/4234; G11C11/4093; G11C5/02; G11C5/063; Y02B60/1228; Y02B60/1235; Y02D10/14; Y02D10/151

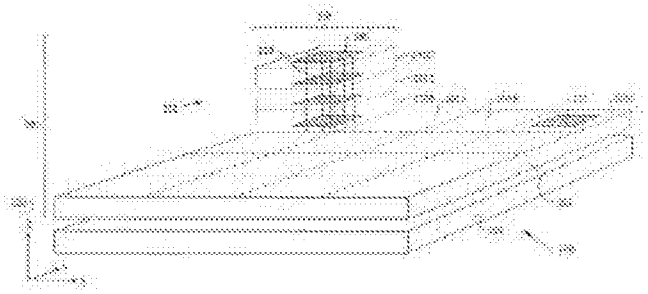
Application number: TW20100108537 20100323

Priority number(s): US20090408906 20090323

Also published as: CN102405498 (A) CN102405498 (B) EP2411981 (A2) EP2411981 (A4) EP2411981 (B1) JP2012521612 (A) JP5784582 (B2) KR101600447 (B1) KR20120001771 (A) TWI512722 (B) US2010238693 (A1) US2011267865 (A1) US2012257434 (A1) US2014112046 (A1) US8018752 (B2) US8203901 (B2) US8681523 (B2) US9293170 (B2) WO2010111281 (A2) WO2010111281 (A3) less

Abstract of TW201040962 (A)

Memory devices and methods are described, such as those that include a stack of memory dies and an attached logic die. Method and devices described provide for configuring bandwidth for selected portions of a stack of memory dies. Additional devices, systems, and methods are disclosed.



(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201040962 A1
(43)公開日： 中華民國 99 (2010) 年 11 月 16 日

(21)申請案號：099108537 (22)申請日： 中華民國 99 (2010) 年 03 月 23 日
(51)Int. Cl.： *G11C11/34 (2006.01)*
(30)優先權：2009/03/23 美國 12/408,906
(71)申請人：美光科技公司 (美國) MICRON TECHNOLOGY, INC. (US)
美國
(72)發明人：傑德羅 喬M JEDDELOH, JOE M. (US)
(74)代理人：陳長文
申請實體審查：無 申請專利範圍項數：25 項 圖式數：6 共 30 頁

(54)名稱

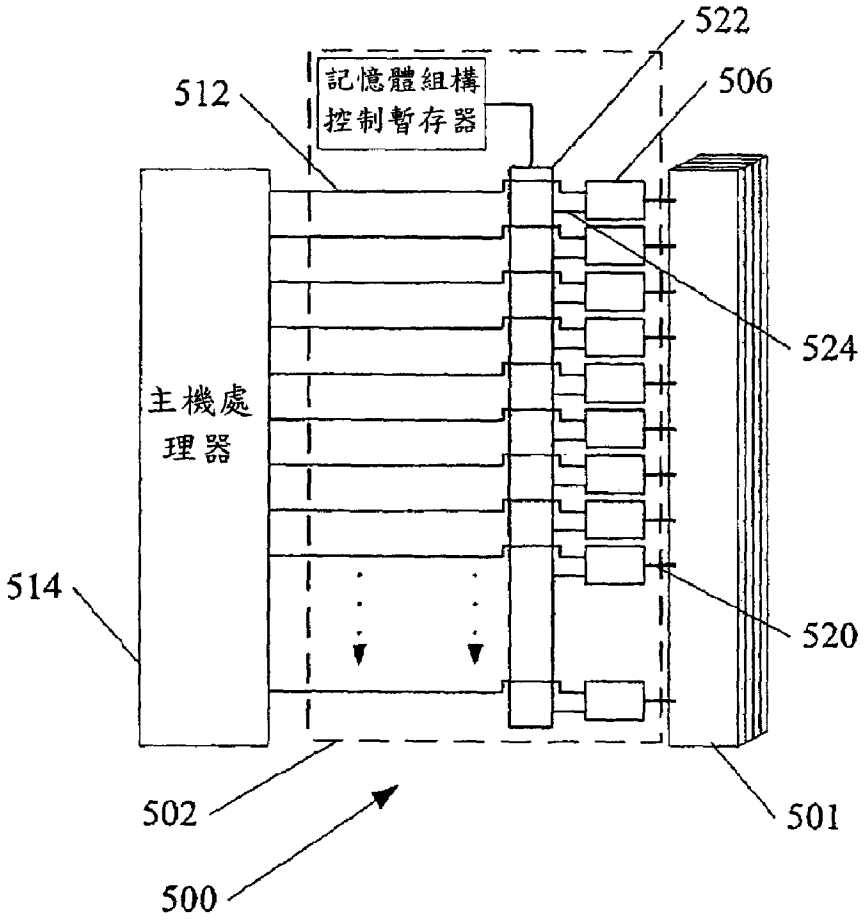
可組態頻寬記憶體裝置及方法

CONFIGURABLE BANDWIDTH MEMORY DEVICES AND METHODS

(57)摘要

本發明闡述記憶體裝置及方法，例如包含一記憶體晶粒堆疊及一所附接邏輯晶粒之記憶體裝置及方法。所闡述之方法及裝置達成組態針對一記憶體晶粒堆疊之選定部分之頻寬。本發明亦揭示額外裝置、系統及方法。

Petitioner Mercedes Ex-1009, 0067



500：記憶體裝置
501：堆疊式晶粒 3D 記憶體陣列
502：邏輯晶粒
506：MVC
512：第一鏈路
514：主機
520：第二鏈路
522：動態鏈路控制器
524：緩衝連接

(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201040962 A1
(43)公開日： 中華民國 99 (2010) 年 11 月 16 日

(21)申請案號：099108537 (22)申請日： 中華民國 99 (2010) 年 03 月 23 日
(51)Int. Cl.： *G11C11/34 (2006.01)*
(30)優先權：2009/03/23 美國 12/408,906
(71)申請人：美光科技公司 (美國) MICRON TECHNOLOGY, INC. (US)
美國
(72)發明人：傑德羅 喬M JEDDELOH, JOE M. (US)
(74)代理人：陳長文
申請實體審查：無 申請專利範圍項數：25 項 圖式數：6 共 30 頁

(54)名稱

可組態頻寬記憶體裝置及方法

CONFIGURABLE BANDWIDTH MEMORY DEVICES AND METHODS

(57)摘要

本發明闡述記憶體裝置及方法，例如包含一記憶體晶粒堆疊及一所附接邏輯晶粒之記憶體裝置及方法。所闡述之方法及裝置達成組態針對一記憶體晶粒堆疊之選定部分之頻寬。本發明亦揭示額外裝置、系統及方法。

Petitioner Mercedes Ex-1009, 0069

六、發明說明：

【發明所屬之技術領域】

本文中所闡述之各種實施例係關於與半導體記憶體相關聯之設備、系統及方法。

【先前技術】

微處理器技術已以比半導體記憶體技術之速率快的一速率演變。因此，在現代主機處理器與半導體記憶體子系統之間通常存在效能方面之一不匹配，該處理器配接至該半導體記憶體子系統以接收指令及資料。舉例而言，據估計，某些高端伺服器閒置四分之三時脈循環來等待對記憶體請求之回應。

另外，隨著處理器核心及執行緒之數目繼續增加，軟體應用程式及作業系統技術之演變增加了對較高密度記憶體子系統之需求。然而，當前技術記憶體子系統通常表示效能與密度之間的一折衷。較高頻寬可限制在不超出聯合電子裝置工程會議(JEDEC)電氣規範之情形下於一系統中可連接之記憶卡或記憶體模組之數目。

已提出對JEDEC介面標準(例如，雙倍資料速率(DDR)同步動態隨機存取記憶體(SDRAM))之擴展，但對於未來所預期記憶體頻寬及密度通常可發現其不足。缺點包含缺少記憶體電力最佳化及主機處理器與記憶體子系統之間的介面之唯一性。隨著處理器及/或記憶體技術發生改變，後一缺點可導致需要重新設計該介面。

【實施方式】

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在本發明之以下實施方式中，參照形成本發明之一部分且其中以圖解說明方式顯示其中可實踐本發明之具體實施例之隨附圖式。充分詳細地闡述此等實施例以使熟習此項技術者能夠實踐本發明。可利用其他實施例且可做出結構、邏輯及電改變。

圖1包含根據本發明之各種實例性實施例之一記憶體裝置100之一方塊圖。記憶體裝置100運作以在一個或多個始發裝置及/或目的地裝置(舉例而言，一主機，例如包括一個或多個處理器之主機)與一組堆疊式陣列記憶體「儲存庫」110之間大致同時傳送複數個傳出及/或傳入命令串流、位址串流及/或資料串流。可導致增加之記憶體系統密度、頻寬、平行性及可比例縮放性。

多晶粒記憶體陣列實施例聚合了在先前設計中通常位於每一個別記憶體陣列晶粒上之控制邏輯。一堆疊式晶粒群組之子區段(在本發明中稱為記憶體儲存庫)在圖1中顯示為實例性儲存庫110且在圖2中顯示為實例性儲存庫230。在所圖解說明之實例中所顯示之記憶體儲存庫共享共同控制邏輯。記憶體儲存庫架構戰略性地分割記憶體控制邏輯以增加能量效率同時提供已通電記憶體庫之一較精細粒度。所顯示之實施例亦達成一標準化主機處理器至記憶體系統介面。隨著記憶體技術的演變，該標準化介面可減少重新設計循環次數。

圖2係根據各種實例性實施例與一邏輯晶粒202堆疊在一起以形成一記憶體裝置100之一堆疊式晶粒3D記憶體陣列

200之一剖面概念視圖。記憶體裝置100併入有產生堆疊式晶粒3D記憶體陣列200之一個或多個記憶體陣列203堆疊。將多個記憶體陣列(例如，記憶體陣列203)製造至複數個晶粒中之每一者(例如，晶粒204)上。接著，堆疊該等記憶體陣列晶粒以形成堆疊式晶粒3D記憶體陣列200。

將該堆疊中之每一晶粒劃分成多個「晶粒塊」(例如，與堆疊式晶粒204相關聯之晶粒塊205A、205B及205C)。每一晶粒塊(例如，晶粒塊205C)可包含一個或多個記憶體陣列203。記憶體陣列203並不限於任一特定記憶體技術且可包含動態隨機存取記憶體(DRAM)、靜態隨機存取記憶體(SRAM)、快閃記憶體等。

一堆疊式記憶體陣列晶粒塊組208可包含來自該等堆疊式晶粒中之每一者之一單個晶粒塊(例如，晶粒塊212B、212C及212D，其中基底晶粒塊於圖1中被隱藏而看不到)。電力、位址及/或資料以及類似共同信號可沿「Z」維度220在傳導路徑(例如，傳導路徑224)(例如，「貫通晶圓互連件」(TWI))上橫越堆疊式晶粒塊組208。注意，一TWI未必需要完全穿過一特定晶圓或晶粒。

將一個組態中之堆疊式晶粒3D記憶體陣列200分割成一組記憶體「儲存庫」(例如，記憶體儲存庫230)。每一記憶體儲存庫包含一堆疊式晶粒塊組(例如，晶粒塊組208)、來自複數個堆疊式晶粒中之每一者之一個晶粒塊以及用於電互連晶粒塊組208之一組TWI。該儲存庫之每一晶粒塊包含一個或多個記憶體陣列(例如，記憶體陣列240)。雖然闡

述分割成個別儲存庫230，但亦可以若干個其他方式分割3D記憶體陣列200。其他實例性分割包含按晶粒、晶粒塊等分割。

於圖1中在於記憶體裝置100內之背景中圖解說明一記憶體儲存庫組102(其類似於來自圖2之記憶體儲存庫230)。記憶體裝置100亦包含複數個記憶體儲存庫控制器(MVC)104(例如，MVC 106)。每一MVC係以一對一關係以通信方式耦合至一對應記憶體儲存庫(例如，組102之記憶體儲存庫110)。因此，每一MVC能夠獨立於其他MVC與其各別記憶體儲存庫之間的通信而與一對應記憶體儲存庫通信。

記憶體裝置100亦包含複數個可組態串列化通信鏈路介面(SCLI)112。SCLI 112被劃分成一SCLI傳出群組113及一SCLI傳入群組115，其中「傳出」及「傳入」方向係從儲存器114之角度來界定。複數個SCLI 112中之每一SCLI能夠與其他SCLI同時運作。SCLI 112一起將複數個MVC 104以通信方式耦合至一個或多個處理器114。記憶體裝置100呈現至主機處理器114之一多鏈路高通量介面。

記憶體裝置100亦可包含一開關116。在某些實施例中，開關116可包括一矩陣開關，其亦可稱為一交叉連接開關。開關116以通信方式耦合至複數個SCLI 112及複數個MVC 104。開關116能夠將每一SCLI直接交叉連接至一選定MVC。因此，主機處理器114可跨越複數個SCLI 112以一大致同時方式存取複數個記憶體儲存庫102。此架構可

為現代處理器技術(包含多核心技術)提供高處理器至記憶體頻寬。

記憶體裝置100亦可包含耦合至開關116之一記憶體組構控制暫存器117。記憶體組構控制暫存器117接受來自一組態源之記憶體組構組態參數且組態記憶體裝置100之一個或多個組件以根據一可選擇模式運作。舉例而言，開關116及複數個記憶體儲存庫102以及複數個MVC 104中之每一者通常可經組態以回應於單獨記憶體請求而彼此獨立地運作。此一組態可因SCLI 112與記憶體儲存庫102之間的平行性而增強記憶體系統頻寬。

另一選擇為，記憶體裝置100可經由記憶體組構控制暫存器117重新組態，以致使複數個記憶體儲存庫102中之兩者或更多者之一子組及一對應MVC子組回應於一單個請求而同步運作。後一組態可用於存取比與一單個儲存庫相關聯之一資料字之寬度寬的一資料字。此一字在本文中稱為一寬資料字。此技術可降低延時。可藉由將一選定位元型樣載入至記憶體組構控制暫存器117中來達成其他組態。

在一項實例中，傳出SCLI 113可包含複數個傳出差異對串列路徑(DPSP)128。DPSP 128以通信方式耦合至主機處理器114且可共同地輸送一傳出封包。傳出SCLI 113亦可包含耦合至複數個傳出DPSP 128之一解串列化器130。傳出SCLI亦可包含以通信方式耦合至解串列化器130之一解多工器138。在一項實施例中，DSPS、解串列化器及解多工器之組態促進資料封包或資料子封包之高效傳送。類似

於傳出SLCI，在一項實施例中，傳入SCLI以及DSPS、串列化器及多工器之一類似組態促進資料封包或資料子封包之高效傳送。

圖3係根據各種實例性實施例之一MVC(例如，MVC 106)及相關聯模組之一方塊圖。MVC 106可包含一可程式化儲存庫控制邏輯(PVCL)組件310。PVCL 310將MVC 106介接至對應記憶體儲存庫(例如，記憶體儲存庫110)。PVCL 310產生與對應記憶體儲存庫110相關聯之一個或多個控制信號及/或定時信號。

PVCL 310可經組態以將MVC 106調適至一選定組態或一選定技術之一記憶體儲存庫110。因此，舉例而言，最初可使用當前可用DDR2 DRAM來組態記憶體裝置100。隨後，可藉由重新組態PVCL 310以包含DDR3庫控制及定時邏輯來調適記憶體裝置100以適應基於DDR3之記憶體儲存庫技術。

MVC 106包含以通信方式耦合至PVCL 310之一記憶體定序器314。記憶體定序器314基於用於實施相關聯記憶體儲存庫110之技術執行一組記憶體技術相依作業。舉例而言，記憶體定序器314可執行與對應記憶體儲存庫110相關聯之命令解碼作業、記憶體位址多工作業、記憶體位址解多工作業、記憶體再新作業、記憶體儲存庫訓練作業及/或記憶體儲存庫預取作業。在某些實施例中，記憶體定序器314可包括一DRAM定序器。在某些實施例中，記憶體再新作業可始發於一單獨再新控制器(未顯示)中。

記憶體定序器314可經組態以將記憶體裝置100調適至一選定組態或技術之一記憶體儲存庫110。舉例而言，記憶體定序器314可經組態以同與記憶體裝置100相關聯之其他記憶體定序器同步運作。此一組態可用於回應於一單個快取線請求而將一寬資料字自多個記憶體儲存庫遞送至與主機處理器114相關聯之一快取線(未顯示)。

MVC 106亦可包含一寫入緩衝器316。寫入緩衝器316可耦合至PVCL 310以緩衝自主機處理器114到達MVC 106之資料。MVC 106可進一步包含一讀取緩衝器317。讀取緩衝器317可耦合至PVCL 310以緩衝自對應記憶體儲存庫110到達MVC 106之資料。

MVC 106亦可包含一無序請求佇列318。無序請求佇列318建立對包含於記憶體儲存庫110中之複數個記憶體庫之讀取及/或寫入作業之一有序序列。該有序序列經挑選以避免對任一單個記憶體庫之連續作業以減少庫衝突且減少讀取至寫入周轉時間。

MVC 106亦可包含一記憶體修復邏輯(MRL)組件324。MRL 324管理若干個作業，例如使用TWI修復邏輯328之TWI修復作業或其他修復作業。

圖4圖解說明根據本發明之一實施例之一作業方法。在作業410中，選擇耦合至一主機之第一數目個第一鏈路。第一鏈路之一實例包含如上文所闡述之SCLI 112。每一第一鏈路具有一個別頻寬。當第一數目個第一鏈路經選擇以一起運作時，該等經組合第一鏈路之頻寬增加。

在作業420中，選擇耦合至該堆疊之複數個記憶體儲存庫中之各別記憶體儲存庫之第二數目個第二鏈路。第二鏈路之一實例包含如圖1中所圖解說明之鏈路120。在圖1實例中，第二鏈路120將MVC104中之各別MVC耦合至堆疊式晶粒3D記憶體陣列200中之每一相關聯記憶體儲存庫102。雖然記憶體儲存庫被敘述為堆疊式晶粒3D記憶體陣列200之部分，但其他部分(例如晶粒204、晶粒塊205等)亦係可能的。

在作業430中，選定之第一數目個第一鏈路及選定之第二數目個第二鏈路耦合於一起以提供記憶體晶粒堆疊與主機之間的一記憶體頻寬。再次使用圖1作為一實例，選定數目個第一鏈路112及選定數目個第二鏈路120經耦合以提供堆疊式晶粒3D記憶體陣列200與主機114之間的一記憶體頻寬。

實例性實施例包含將一個第一鏈路112耦合至多個第二鏈路120以平行地提供對多個儲存庫110之存取。另一實例性實施例包含將一個第二鏈路120耦合至多個第一鏈路112以自一單個給定儲存庫110提供比在僅一單個第一鏈路112之情形下可用的多的頻寬。其他實例包含多個第一鏈路112與第二鏈路120組合以提供關於多個儲存庫110與多個第一鏈路112兩者之若干個頻寬組合。

圖1中顯示一開關116，其用於將該數目個第一鏈路112耦合至該數目個第二鏈路120。在一項實例中，開關116係一動態鏈路控制器，其能夠在記憶體作業期間根據堆疊式

晶粒3D記憶體陣列200之部分改變記憶體頻寬。一動態鏈路控制器之一實例包含一縱橫開關，其將任何第一鏈路直接連接至任何第二鏈路。在另一實例中，該動態鏈路控制器包含一第一鏈路與一第二鏈路之間的一個本端直接連接，其中在一給定第一鏈路與其他遠端第二鏈路之間具有複數個緩衝連接。下文相對於圖5更詳細地闡述此實例性實施例。

在另一實例中，開關116係一靜態控制器，其在製造時或在裝置啟動時即根據堆疊式晶粒3D記憶體陣列200之部分設定記憶體頻寬。在一實例性靜態組態中，一鏈路組態暫存器(例如記憶體組構控制暫存器117)用於在製造時、在啟動或另一事件(例如裝置重設)時組態頻寬。

在一項實例中，一所需組態(例如上文所闡述之一靜態組態或一動態組態)係自主機114經由一路徑122發送至記憶體組構控制暫存器117。在一項實施例中，該所需組態係自一記憶體映射發送。在一記憶體映射組態中，記憶體位址空間之區域可經映射以由一個或多個儲存庫服務。在選定實例中，該記憶體映射可位於邏輯晶片202上、如上文所闡述之主機114中或記憶體裝置100外部之其他位置中。

上文所闡述之記憶體裝置及系統可經組態以使頻寬與各種類型之記憶體作業匹配。舉例而言，可組合多個鏈路以提供一個寬頻寬路徑，或可劃分鏈路以形成較大數目個較小頻寬路徑。在一個應用中，較小頻寬路徑用於節約電

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力，而在另一應用中，較寬頻寬路徑用於提供速度。

在一項實例中，組合多個鏈路以動態地提供不同於一讀取頻寬之一寫入頻寬。通常，在一記憶體系統中讀取作業花費與寫入作業不同之時間量。藉由組合鏈路以自一寫入作業至一讀取作業改變頻寬，一寫入作業之一速度可經調整以大致匹配一讀取作業之一速度。在一項實施例中，確定一給定記憶體裝置中之作業速度之一讀取對寫入比率。在一項實施例中，接著將該讀取對寫入比率儲存於一暫存器中，且在裝置作業期間，基於儲存於該暫存器中之該值而在讀取作業與寫入作業之間改變頻寬。在一項實例中，該暫存器位於記憶體裝置100上(例如以上實施例中所闡述之邏輯晶粒中)。用於記錄該讀取對寫入比率之其他方法亦係可能的，例如將該比率儲存於主機114內或一暫存器中之一不同位置處。

圖5顯示另一記憶體裝置500之一實例。顯示一主機514藉由若干第一鏈路512耦合至記憶體裝置500。顯示一堆疊式晶粒3D記憶體陣列501(類似於以上實施例)藉由若干第二鏈路520耦合至一邏輯晶粒502。在圖5之實施例中，每一第一鏈路512包含至堆疊式晶粒3D記憶體陣列501之一部分(例如一記憶體儲存庫)之一個直接連接。每一第一鏈路512亦可經由緩衝至遠端記憶體部分(例如儲存庫)之資訊交換之一動態鏈路控制器522選擇性地耦合至任一其他部分(例如一儲存庫)。顯示每一緩衝連接524耦合於動態鏈路控制器522與一本端開關(例如類似於上文所闡述述實施例之

一MVC 506)之間。

具有直接本端連接與緩衝遠端連接兩者之實施例提供快速本端存取，同時亦提供勝過例如一全縱橫鏈路控制器之實例之電力節省。由於對遠端儲存庫之緩衝作業或其他記憶體作業而促進電力節省。

各種實施例之設備及系統可用於除一高密度、多鏈路、高通量半導體記憶體子系統以外之應用中。因此，本發明之各種實施例並不受如此限制。對記憶體裝置100之圖解說明意欲提供對各種實施例之結構之一大體理解。該等圖解說明並非意欲用作對可使用本文中所闡述結構之設備及系統之所有元件及特徵之一完全說明。

如上文所論述，在本發明中闡述包含3D記憶體裝置及處理器之系統。此等系統之實例包含(但不限於)電視、蜂巢式電話、個人資料助理(PDA)、個人電腦(例如，膝上型電腦、桌上型電腦、手持式電腦、平板電腦等)、工作站、無線電、視訊播放器、音訊播放器(例如，MP3(動畫專家組、音訊層3)播放器)、車輛、醫療裝置(例如，心臟監視器、血壓監視器等)、視訊轉換器及其他裝置。

一個人電腦之一高階實例包含於圖6中以顯示本發明之一個可能較高階裝置應用。圖6係根據本發明之一實施例之併入至少一個記憶體裝置606之一資訊處置系統600之一方塊圖。

在此實例中，資訊處置系統600包括一資料處理系統，該資料處理系統包含一系統匯流排602以耦合該系統之各

種組件。系統匯流排602在資訊處置系統600之各種組件中提供通信鏈路且可實施為一單個匯流排、實施為一匯流排組合或以任一其他適合方式實施。

晶片總成604耦合至系統匯流排602。晶片總成604可包含任一電路或若干電路之運作上相容之組合。在一項實施例中，晶片總成604包含可係任一類型之一處理器608或多個處理器。如本文中所用，「處理器」意指任一類型之計算電路，例如，但不限於一微處理器、一微控制器、一圖形處理器、一數位信號處理器(DSP)或任一其他類型之處理器或處理電路。如本文中所用，「處理器」包含多個處理器或多個處理器核心。

在一項實施例中，一記憶體裝置606包含於晶片總成604中。一記憶體裝置(例如，一DRAM)係此一記憶體裝置606之一項實例。一DRAM裝置之一項實例包含具有如以上實施例中所闡述之一整合式邏輯晶片之一堆疊式記憶體晶片3D記憶體裝置。記憶體606亦可包含非揮發性記憶體(例如，快閃記憶體)。

資訊處置系統600亦可包含一外部記憶體611，該外部記憶體又可包含適於特定應用之一個或多個記憶體元件，例如，一個或多個硬驅動器612及/或處置可抽換媒體613(例如，快閃記憶體驅動器、光碟(CD)、數位視訊磁碟(DVD)及類似物)之一個或多個驅動器。

資訊處置系統600亦可包含一顯示器裝置509(例如，一監視器)、額外周邊組件610(例如，揚聲器等)及一鍵盤及/

或控制器614，其可包含一滑鼠、軌跡球、遊戲控制器、語音辨識裝置或准許一系統使用者將資訊輸入至資訊處置系統600中及自資訊處置系統600接收資訊之任一其他裝置。

雖然闡述了本發明之若干項實施例，但以上列表並非意欲為窮舉性。雖然本文中已圖解說明及闡述了具體實施例，但熟習此項技術者將瞭解，旨在達成相同目的之任何配置皆可替代所顯示之具體實施例。此申請案意欲涵蓋對本發明之任何修改或變型。應理解，以上說明意欲為說明性而非限制性。在審閱以上說明時，熟習此項技術者將明瞭以上實施例之組合及其他實施例。

【圖式簡單說明】

圖1顯示根據本發明之一實施例之一記憶體系統之一方塊圖。

圖2顯示根據本發明之一實施例之具有一邏輯晶粒之一堆疊式晶粒3D記憶體之一剖面概念視圖。

圖3顯示根據本發明之一實施例之一記憶體儲存庫控制器及相關聯模組之一方塊圖。

圖4顯示根據本發明之一實施例之操作一記憶體裝置之一方法。

圖5顯示根據本發明之一實施例之另一記憶體系統之一方塊圖。

圖6顯示根據本發明之一實施例之一資訊處置系統之一方塊圖。

【主要元件符號說明】

100	記憶體裝置
102	記憶體儲存庫
104	記憶體儲存庫控制器(MVC)
106	MVC
110	記憶體儲存庫
112	可組態串列化通信鏈路介面(SCLI)
113	SCLI傳出群組
114	主機處理器
115	SCLI傳入群組
116	開關
117	記憶體組構控制暫存器
120	鏈路
122	路徑
128	傳出差異對串列路徑(DPSP)
130	解串列化器
138	解多工器
200	堆疊式晶粒3D記憶體陣列
202	邏輯晶粒
203	記憶體陣列
204	晶粒
205A	晶粒塊
205B	晶粒塊
205C	晶粒塊

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208	晶粒塊組
212B	晶粒塊
212C	晶粒塊
212D	晶粒塊
224	傳導路徑
230	記憶體儲存庫
240	記憶體陣列
310	可程式化儲存庫控制邏輯(PVCL)組件
314	記憶體定序器
316	寫入緩衝器
317	讀取緩衝器
318	佇列
324	記憶體映射邏輯(MML)組件
328	TWI修復邏輯
500	記憶體裝置
501	堆疊式晶粒3D記憶體陣列
502	邏輯晶粒
506	MVC
512	第一鏈路
514	主機
520	第二鏈路
522	動態鏈路控制器
524	緩衝連接
600	資訊處置系統

602	系統匯流排
604	晶片總成
606	記憶體裝置
608	處理器
609	顯示器裝置
610	額外周邊組件
611	外部記憶體
612	硬驅動器
613	可抽換媒體
614	鍵盤/控制器

發明專利說明書

99年7月21日 修正補充

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※ 申請案號：99108537

※ 申請日：99.3.23　　※IPC 分類：~~G11C~~ G11C 11/34 (2006.01)

一、發明名稱：（中文/英文）

可組態頻寬記憶體裝置及方法

CONFIGURABLE BANDWIDTH MEMORY DEVICES AND METHODS

二、中文發明摘要：

本發明闡述記憶體裝置及方法，例如包含一記憶體晶粒堆疊及一所附接邏輯晶粒之記憶體裝置及方法。所闡述之方法及裝置達成組態針對一記憶體晶粒堆疊之選定部分之頻寬。本發明亦揭示額外裝置、系統及方法。

三、英文發明摘要：

Memory devices and methods are described, such as those that include a stack of memory dies and an attached logic die. Method and devices described provide for configuring bandwidth for selected portions of a stack of memory dies. Additional devices, systems, and methods are disclosed.

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七、申請專利範圍：

1. 一種記憶體裝置，其包括：

一記憶體晶粒堆疊，其包含該記憶體晶粒堆疊內之若干個記憶體部分；

一邏輯晶粒，其與該記憶體晶粒堆疊堆疊在一起，且包括：

該邏輯晶粒內之第一鏈路，其用以耦合至一始發及/或目的地裝置；

第二鏈路，其耦合至該等記憶體部分；及

一開關，其用以將選定數目個該等第一鏈路耦合至選定數目個該等第二鏈路，以改變該等記憶體部分與該始發及/或目的地裝置之間的頻寬。

2. 如請求項1之記憶體裝置，其中該開關包含一第一鏈路與一第二鏈路之間的一個本端直接連接，其中在一給定第一鏈路與其他遠端第二鏈路之間具有複數個緩衝連接。

3. 如請求項2之記憶體裝置，其進一步包含耦合至該若干個記憶體部分中之每一者之若干個儲存庫控制器，其中每一儲存庫控制器耦合至一個本端直接連接及一個緩衝連接。

4. 如請求項1之記憶體裝置，其中該記憶體晶粒堆疊內之該若干個記憶體部分包含若干個記憶體儲存庫。

5. 如請求項1之記憶體裝置，其中該開關經調適以在製造時組態該記憶體裝置中之頻寬。

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6. 如請求項1之記憶體裝置，其中該開關經調適以在該記憶體裝置之重設時組態該記憶體裝置中之頻寬。

7. 如請求項1之記憶體裝置，其中該開關經組態以在作業期間動態地組態該記憶體裝置中之頻寬。

8. 如請求項1之記憶體裝置，其中該開關包含位於該邏輯晶粒上用以組態該頻寬之一鏈路組態暫存器。

9. 如請求項8之記憶體裝置，其中該鏈路組態暫存器經組態以在啟動時設定該選定數目個該等第一鏈路至該選定數目個該等第二鏈路。

10. 如請求項8之記憶體裝置，其中該鏈路組態暫存器經組態以在裝置重設時設定該選定數目個該等第一鏈路至該選定數目個該等第二鏈路。

11. 一種記憶體裝置，其包括：

一記憶體晶粒堆疊；

一邏輯晶粒，其與該記憶體晶粒堆疊堆疊在一起，該邏輯晶粒包括耦合至該記憶體晶粒堆疊之部分之若干個鏈路；及

一開關，其用以選擇該記憶體晶粒堆疊之若干個部分以平行地運作。

12. 如請求項11之記憶體裝置，其中該開關位於該邏輯晶粒上。

13. 如請求項11之記憶體裝置，其中該開關位於該記憶體裝置外部。

14. 一種設定記憶體頻寬之方法，其包括：

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選擇耦合至一始發及/或目的地裝置之一定數目個第一鏈路；

選擇耦合至一記憶體晶粒堆疊中之複數個記憶體儲存庫中之各別記憶體儲存庫之第二數目個第二鏈路；及

將該選定數目個第一鏈路耦合至該選定數目個第二鏈路以提供該記憶體晶粒堆疊與該裝置之間的一記憶體頻寬。

15. 如請求項14之方法，其中在記憶體作業期間改變對該第一數目個第一鏈路及該數目個第二鏈路之選擇。

16. 如請求項14之方法，其中對該數目個第一鏈路及該數目個第二鏈路之選擇包含：選擇耦合至該記憶體堆疊之一第一部分之多個鏈路以提供至少一個寬頻寬路徑，且在該記憶體晶粒堆疊之一第二部分中，選擇一單個鏈路來形成至該第二部分之一窄頻寬路徑。

17. 如請求項14之方法，其進一步包括自一記憶體映射接收指令，其中至少部分地回應於該指令而執行該等選擇動作。

18. 如請求項17之方法，其中自一記憶體映射接收指令包含：自位於該記憶體裝置外部之一定位置中之一記憶體映射接收指令。

19. 如請求項17之方法，其中自一記憶體映射接收指令包含自位於與該記憶體晶粒堆疊堆疊在一起之一邏輯晶片上之一記憶體映射接收指令。

20. 如請求項17之方法，其中自一記憶體映射接收指令包含

自位於該始發及/或目的地裝置中之一記憶體映射接收指令。

21. 一種設定記憶體頻寬之方法，其包括：

選擇耦合至一始發及/或目的地裝置之一定數目個第一鏈路；

選擇耦合至一記憶體晶粒堆疊中之複數個記憶體儲存庫中之各別記憶體儲存庫之第二數目個第二鏈路；

將該選定數目個第一鏈路耦合至該選定數目個第二鏈路以提供該記憶體晶粒堆疊與該裝置之間的一寫入頻寬；及

在一讀取作業期間改變該選定數目個第一鏈路至該選定數目個第二鏈路以提供不同於該寫入頻寬之一讀取頻寬。

22. 如請求項21之方法，其中在一讀取作業期間改變該選定數目個第一鏈路至該選定數目個第二鏈路以提供一讀取頻寬包含提供用以使一讀取速度與一寫入速度大致匹配之一讀取頻寬。

23. 如請求項21之方法，其進一步將該記憶體裝置中之一暫存器設定成一選定讀取對寫入比率。

24. 如請求項23之方法，其中在裝置啟動時設定該暫存器。

25. 如請求項23之方法，其中在裝置重設時設定該暫存器。

八、圖式：

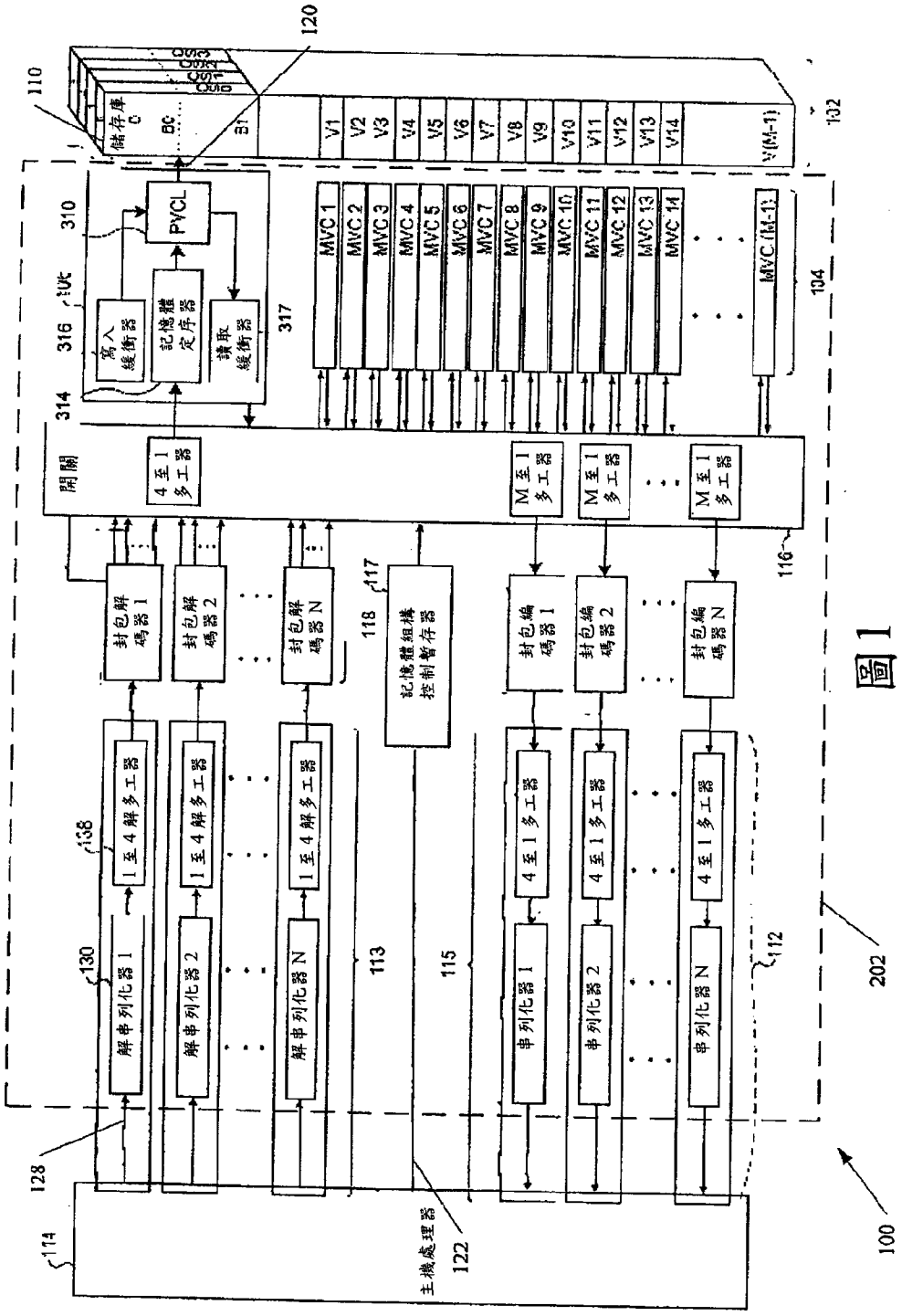


圖 1

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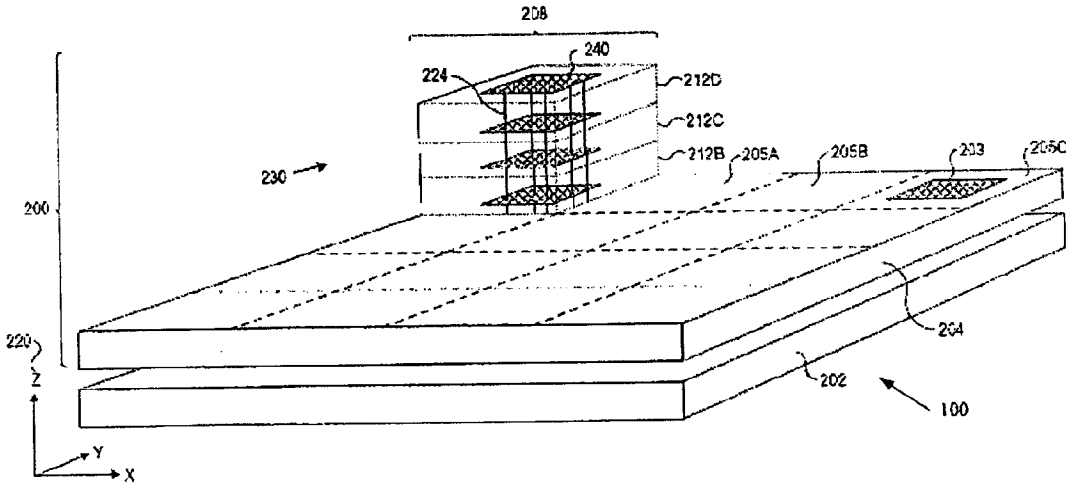

208
240
224
212D
212C
212B
205A
205B
203
205C
230
200
220
Z
Y
X
204
202
100

圖2

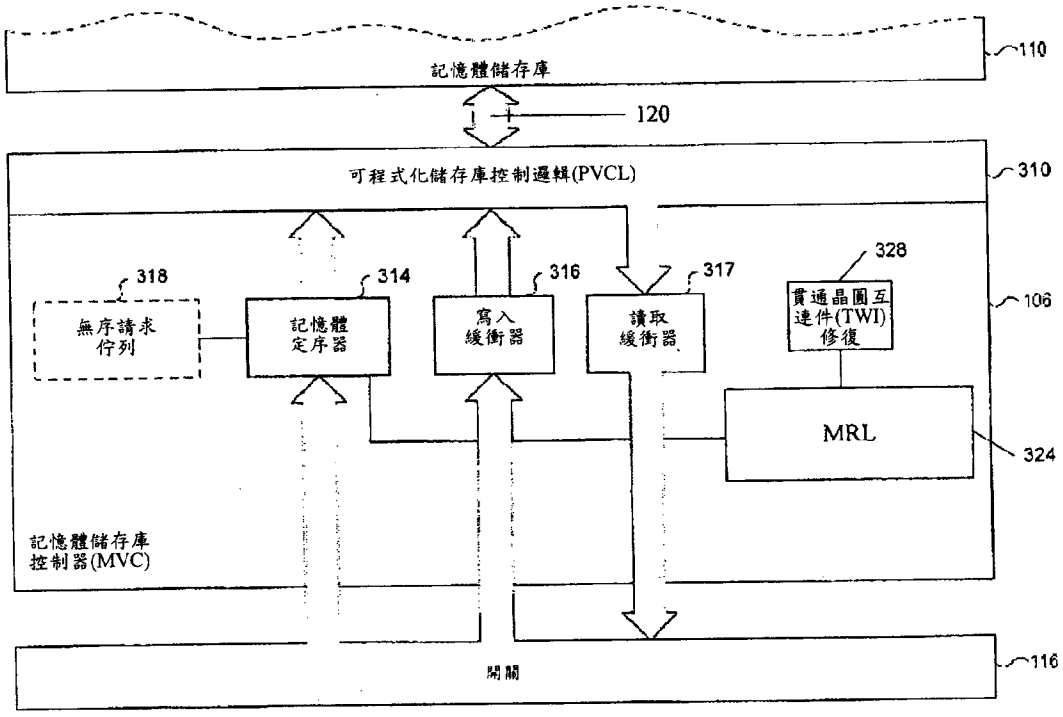

記憶體儲存庫
110
120
可程式化儲存庫控制邏輯(PVCL)
310
318
無序請求佇列
314
記憶體定序器
316
寫入緩衝器
317
讀取緩衝器
328
貫通晶圓互連件(TWI)修復
106
MRL
324
記憶體儲存庫控制器(MVC)
開關
116

圖3

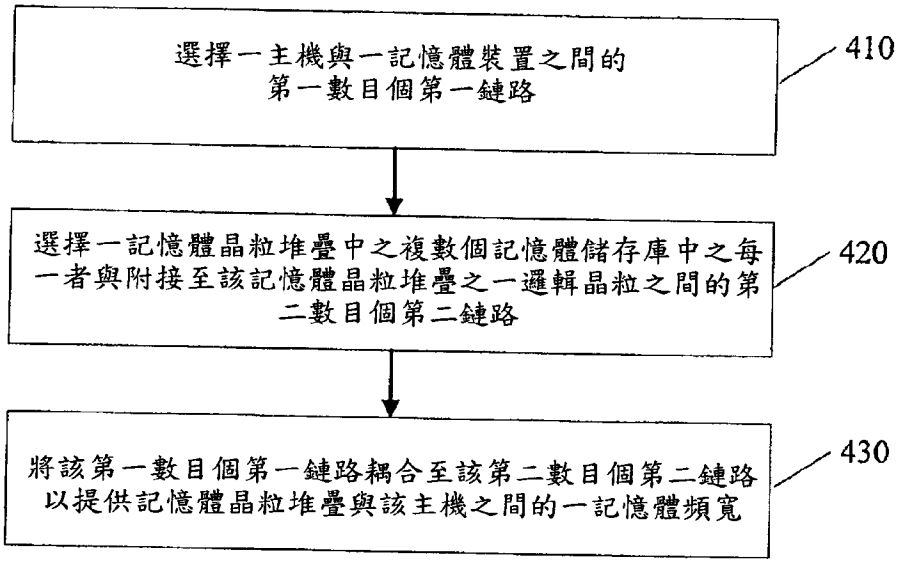


圖4

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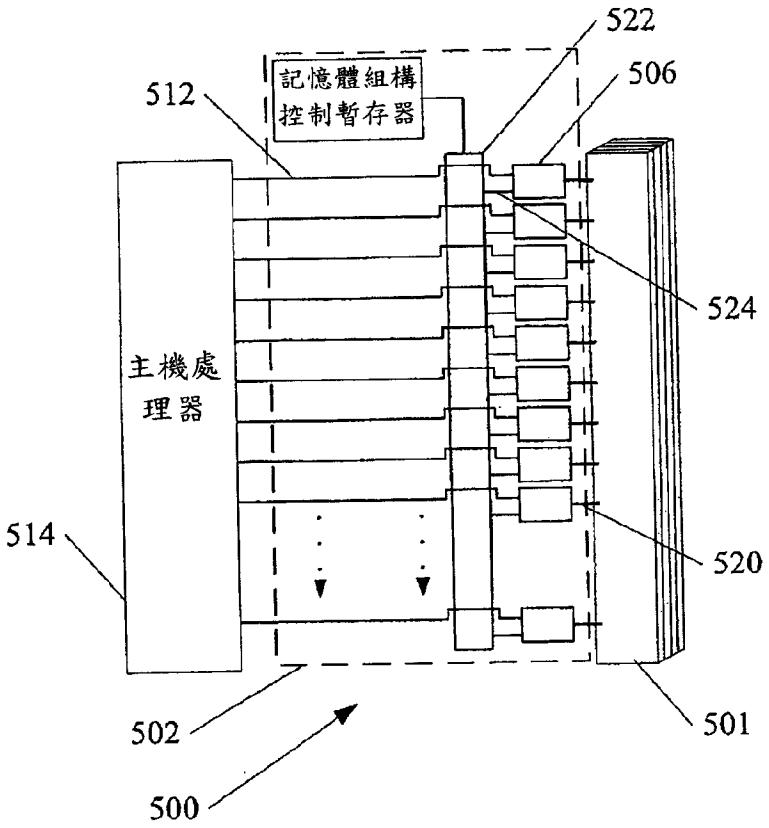


圖5

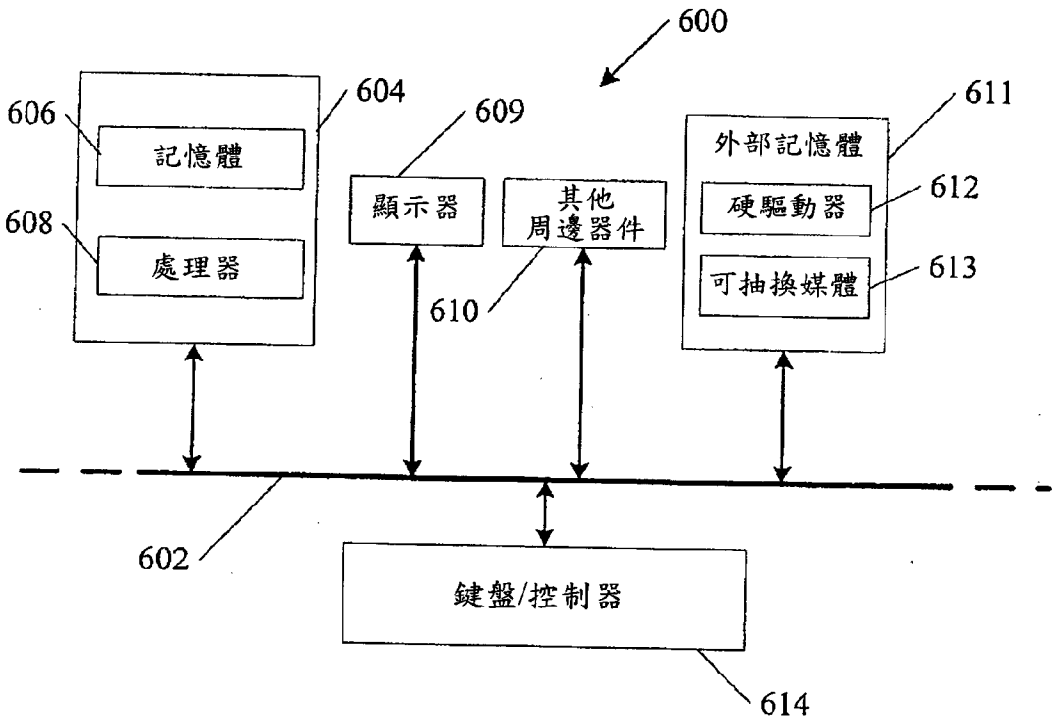

600
606
記憶體
608
處理器
604
609
顯示器
其他
周邊器件
610
611
外部記憶體
612
硬驅動器
613
可抽換媒體
602
鍵盤/控制器
614

圖6

四、指定代表圖：

(一)本案指定代表圖為：第（ 5 ）圖。

(二)本代表圖之元件符號簡單說明：

500	記憶體裝置
501	堆疊式晶粒3D記憶體陣列
502	邏輯晶粒
506	MVC
512	第一鏈路
514	主機
520	第二鏈路
522	動態鏈路控制器
524	緩衝連接

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

(無)

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Espacenet

Bibliographic data: TW201022923 (A) — 2010-06-16

Power management for multiple processor cores

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Applicant(s): INTEL CORP [US] ± (INTEL CORPORATION)

Classification: **- international:** *G06F1/26*
- cooperative: **G06F1/206**; **G06F1/26**; **G06F1/3203**; **G06F1/324**; **G06F1/3296**; Y02D10/126; Y02D10/16; Y02D10/172

Application number: TW20090136920 20091030

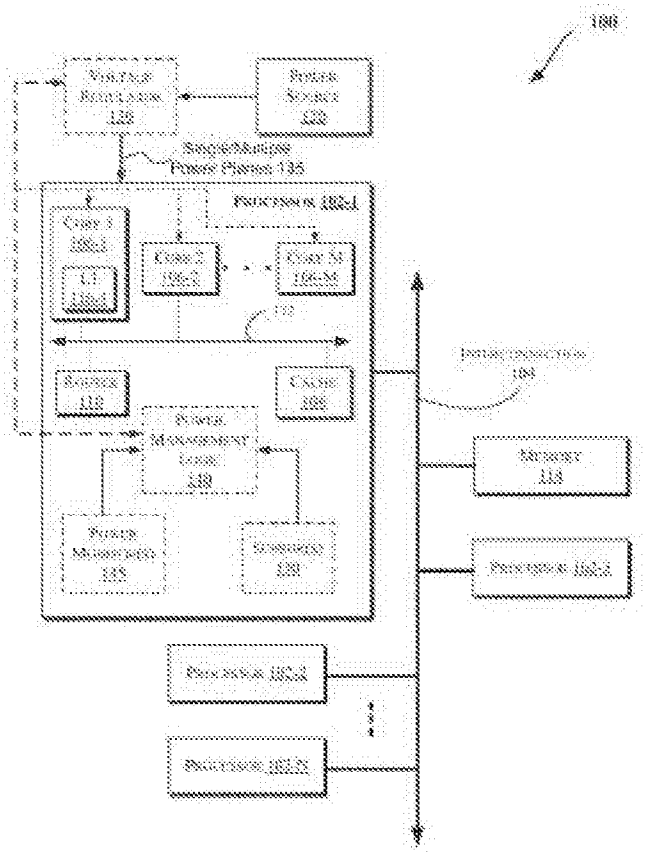
Priority number(s): US20080263421 20081031

Also published as: CN101923383 (A) CN101923383 (B) CN103440028 (A) CN103440028 (B) DE102009051387 (A1) TWI430079 (B) US2010115304 (A1) US2013219196 (A1) US8402290 (B2) less

Abstract of TW201022923 (A)

Methods and apparatus relating to power management for multiple processor cores are described. In one embodiment, one or more techniques may be utilized locally (e.g., on a per core basis) to manage power consumption in a processor. In another embodiment, power may be distributed among different power planes of a processor based on energy-based considerations. Other embodiments are also disclosed and claimed.

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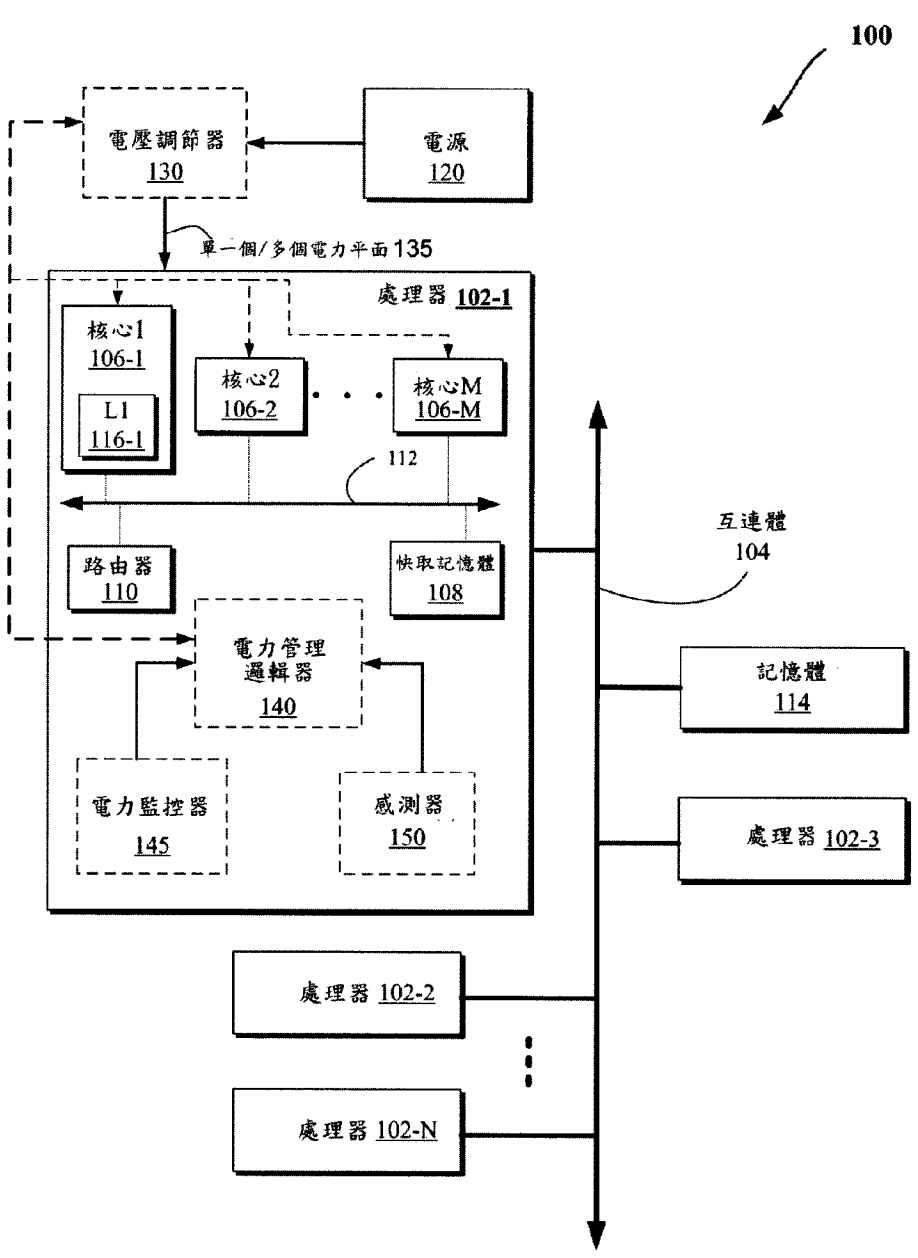
(54)名稱

用於多處理器核心之電力管理技術

POWER MANAGEMENT FOR MULTIPLE PROCESSOR CORES

(57)摘要

本文論述與用於多處理器核心之電力管理技術有關之方法與裝置。於一實施例中，可局部地（例如基於一種逐一核心的基礎）利用一或多種技術來管理一處理器中之電力消耗。於另一實施例中，可基於數種基於能量之考量，而將電力於一處理器的不同的電力平面間分配。本文亦揭露其他實施例，並加以請求專利。



100：系統
102：處理器
104：互連體/匯流排
106：核心
108：快取記憶體
110：路由器
112：互連體/匯流排
114：記憶體
120：電源
130：電壓調節器
135：電源平面
140：邏輯器
145：監控器
150：感測器

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本文論述與用於多處理器核心之電力管理技術有關之方法與裝置。於一實施例中，可局部地（例如基於一種逐一核心的基礎）利用一或多種技術來管理一處理器中之電力消耗。於另一實施例中，可基於數種基於能量之考量，而將電力於一處理器的不同的電力平面間分配。本文亦揭露其他實施例，並加以請求專利。

六、發明說明：

【發明所屬之技術領域】

發明領域

本發明一般係有關電子電路領域。更尤其是，本發明之一實施例係有關用於多處理器核心之電力管理。

【先前技術】

發明背景

隨著積體電路（IC）製作技術的進步，製造商也能夠將額外的功能整合進單一個矽基體上。然而，隨著這些功能數的增加，在單一個IC晶片上的元件數也隨之增加。額外的元件會增加額外的信號切換，進而產生更多熱能。而額外的熱能可能會由於例如熱膨脹而損害IC晶片。同樣的，額外的熱能也可能會限制含有此種晶片的運算裝置之使用位置及/或應用。例如，可攜式運算裝置可能僅依賴電池電力。因此，當可攜式運算裝置中整合進額外的功能時，減少電力消耗的需求就變得越來越重要，以，例如，在一段延長時間中維持電池電力。而不可攜式運算裝置在其IC元件使用更多電力並產生更多熱能時，亦會面臨冷卻及電力產生問題。

為了對來自於高溫危機的損害給予限制，其中一種途徑可能係利用動態電壓縮放（DVS）。例如，當溫度超越某一個臨界值的時候，頻率與電壓便下降到某個位準，之後再增加到另一個位準（不一定要是原先的那一個）。然而，在多核心處理器設計中，這樣的解決途徑會降低性能，因

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為無論是否所有的核心皆正導致高溫危機，它們全都會受到懲罰。另一種途徑可能係利用頻率節流（其可僅為DVS對頻域的一種投射）。然而，相對於電力減損來說，這種解決途徑的損失可能會是較為線性的。例如，由於藉由以x的因數來降低電壓而達成以相同因數來降低頻率，DVS技術之損失在某種程度上可能會是較少的，並使電力以x^3之因數減少。

【發明內容】

發明概要

依據本發明之一實施例，係特地提出一種裝置，其包含：具有多個處理器核心的一個處理器；單一個電力平面，用以對該等多個處理器核心中之一個以上核心提供電力；以及一個電力管理邏輯器，用以響應於下列狀況而致使對該等多個處理器核心中之至少一個處理器核心的一個操作特徵造成修改：於該至少一個處理器核心檢測到過度溫度；以及判定該等多個處理器核心中之其他處理器核心中的哪一個核心為作動並處於一溫度值。

依據本發明之另一實施例，係特地提出一種裝置，其包含：具有多個處理器核心的一個處理器；多個電力平面，用以對該等多個處理器核心提供電力；以及一個電力管理邏輯器，用以基於下列項目而針對該等多個電力平面中之各個電力平面來判定一個能量預算：該等多個電力平面中之一對應電力平面的一個能量餘數，該能量餘數指出於先前的一個時期中有多少能量仍未遭消耗；以及對應於該等

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多個電力平面中之各個電力平面的多個限制中之一或多個限制。

依據本發明之又一實施例，係特地提出一種方法，其包含下列步驟：判定是否要響應於下列狀況而修改多個處理器核心中之至少一個處理器核心的一個操作特徵：於該至少一個處理器核心檢測到過度溫度、以及判定出該等多個處理器核心中之其他處理器核心中的哪一個核心為作動並處於一溫度值；以及基於下列項目而針對耦接來對該等多個處理器核心提供電力的一或多個電力平面判定一個能量預算：該一或多個電力平面中之一對應電力平面的指出先前的一個時期中有多少能量仍未消耗的一個能量餘數、以及對應於該一或多個電力平面中之各個電力平面的一或多個限制。

依據本發明之再一實施例，係特地提出一種系統，其包含：具有多個處理器核心的一個處理器；一或多個電力平面，用以對該等多個處理器核心提供電力；一個電壓調節器，用以透過該一或多個電力平面而對該等多個處理器核心提供電力；以及一個電力管理邏輯器，用以：判定是否要響應於下列狀況而修改多個處理器核心中之至少一個處理器核心的一個操作特徵：於該至少一個處理器核心檢測到過度溫度、以及判定出該等多個處理器核心中之其他處理器核心中的哪一個核心為作動並處於一溫度值；以及基於下列項目而針對耦接來對該等多個處理器核心提供電力的一或多個電力平面判定一個能量預算：該一或多個電力

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平面中之一對應電力平面的指出先前的一個時期中有多少能量仍未消耗的一個能量餘數、以及對應於該一或多個電力平面中之各個電力平面的一或多個限制。

圖式簡單說明

參考隨附圖式提供詳細說明。在這些圖式中，參考號碼最左邊的（一或數個）位元顯示出此參考號碼首次出現的所在圖式。在不同圖式中使用相同參考號碼，標示出相似或是一模一樣的物品。

第1、6與7圖繪示運算系統之實施例的方塊圖，其可被運用來實施本文中所論述的多種實施例。

第2與4圖繪示依據一些實施例的圖表。

第3與5圖繪示依據一些實施例的流程圖。

【實施方式】

較佳實施例之詳細說明

在接下來的詳細說明中，為了提供對本發明的通盤了解而陳述許多具體細節。然而，本發明之多種實施例可在不具有這些特定細節的情況下實施。在其他情況中，為了不模糊本發明之特定實施例，已為人熟知的方法、程序、部件與電路並未予以詳細描述。此外，本發明之實施例的多種觀點可係利用多種工具來執行，諸如積體半導體電路（「硬體」）、組織在一或多個程式中的電腦可讀指令（「軟體」）或是硬體與軟體的一些組合等等。針對本揭露內容之議題，對「邏輯」之指涉應係指硬體、軟體或是其中的一些組合。

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本文中所論述的一些實施例可提供用於多處理核心的有效電力管理。如上文所述，倚賴DVS可能會減少性能，因為無論是否所有的核心皆正導致高溫危機，它們全都會受到懲罰。在一個實施例中，可對一或多個處理器核心（例如在一個多核心處理器中）局部地（例如在逐核基礎上）利用一或多個節流技術，例如，響應於檢測到熱事件（例如於一或多個核心檢測到過高溫度）的共享單一個電力平面者。同樣的，在具有多個電力平面的設計中，電力可在依據一實施例的基於能源之定義之下，分佈在不同的電力平面之間。此外，可將一些實施例應用於包括一或多個處理器（例如具有一或多個處理器核心者）的運算系統中，諸如參考第1-7圖所說明的那些實施例等等。

更具體地說，第1圖依據本發明的一個實施例，繪示一個運算系統100之方塊圖。系統100可包括一或多個處理器102-1至102-N（於此通常係以「數個處理器102」或「處理器102」來指稱）。處理器102可透過一個互連體或是匯流排104來通訊。各個處理器可包括多個元件，為求簡明，僅參考處理器102-1來論述其中的一些元件。相應地，各個剩餘處理器102-2至102-N亦可包括參考處理器102-1而論述的相同或相似的元件。

在一個實施例中，處理器102-1可包括一或多個處理器核心106-1至106-M（於此以「數個核心106」或「核心106」來指稱）、一個快取記憶體108及/或一個路由器110。可將處理器核心106實施於單一個積體電路（IC）晶片上。此外，

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此晶片可包括一或多個共享的及/或專有的快取記憶體（諸如快取記憶體108者）、匯流排或是互連體（諸如匯流排或是互連體112）、圖形及/或記憶體控制器（諸如參考第6-7所論述的那些）或是其他元件。

在一個實施例中，可利用路由器110來在處理器102-1及/或路由器110的多個元件之間通訊。此外，處理器102-1可包括一個以上的路由器110。此等眾多路由器110可處於通訊狀態，以使能夠在處理器102-1內部或外部的多個元件之間作資料路由。

快取記憶體108可儲存由處理器102-1的一或多個元件，諸如核心106等等，所運用的資料（例如，包括指令）。舉例來說，快取記憶體108可局部地快取儲存在一個記憶體114中的資料，以利處理器102之元件之較快存取（如使核心106較快地存取）。如於第1圖中所示，記憶體114可經由互連體104而與處理器102通訊。在一個實施例中，快取記憶體108（可為共享的）可為中階快取記憶體（MLC）、末階快取記憶體（LLC）等等。同樣的，各個核心106皆可包括一個第1階（L1）快取記憶體（116-1）（於本文中一般係以L1快取記憶體116來指稱）或是其他階的快取記憶體，諸如第2階（L2）等等。此外，處理器102-1的多個元件可直接與快取記憶體108通訊、透過匯流排（如匯流排112）及/或記憶體控制器或控制中樞來與快取記憶體108通訊。

系統100可亦包括一個電源120（例如直流（DC）電源或交流（AC）電源），以對系統100的一或多個元件提供電

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力。在一些實施例中，電源120可包括一或多個電池組。可透過一個電壓調節器（VR）130而將電源120與系統100之元件耦接。此外，雖然第1圖繪示的是一個電源120與一個電壓調節器130，但亦可運用額外的電源及/或電壓調節器。例如，各個處理器102可具有對應的（一或數個）電壓調節器及/或（一或數個）電源。同樣的，可將（一或數個）電壓調節器130耦接至單一個電源平面135（例如對所有的核心106提供電力者）或是耦接至多個電源平面135（例如各個電力平面可對不同的核心或核心群提供電力者）。

另外，雖然第1圖將電源120與電壓調節器130繪示為分離的元件，但亦可將電源120與電壓調節器130整合至系統100的其他元件中。例如，可將所有或是部份的VR 130整合進電源120及/或處理器102中。

如第1圖中所示，處理器102可更包括一個電力管理邏輯器140，以控制對處理器102之元件（例如核心106）的電力供給。邏輯器140可存取於此所論述的一或多個儲存裝置，以儲存與邏輯器140之操作有關的資訊，諸如與系統100之多個元件通訊的資訊，如於此所論述的。如圖所示，可將邏輯器140耦接至VR 130及/或系統100的其他元件（諸如核心106者）。例如，可將邏輯器140耦接來接收資訊（例如以一或多個位元或信號的形式者），來指出一或多個感測器150的狀態（其中可將感測器150設置在逼近系統100（或是於本文中所論述的其他運算系統，例如諸如參考包括第4與5圖的其他圖式所論述的那些系統）之元件，諸如核心106、

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互連體104或112等等，之處，以感測於溫度、操作頻率、操作電壓、電力消耗、核心間通訊活動等等中之變異）及/或來自於一或多個電力監控邏輯器145之資訊（例如可指出系統100之多個元件的運作狀態，諸如操作溫度、操作頻率、操作電壓、操作狀態（如作動的或非作動的）、電力消耗（立即的或經過一段時間的）等等，的資訊）。邏輯器140可指示VR 130、電源120及或系統100之個別元件（諸如核心106者）修改其操作。在一個實施例中，可以此種方式來感測變異，以查明相對於作動電力的漏電。例如，邏輯器140可請求核心106修正其操作頻率、電力消耗等。雖然將元件140、145與150示為包括在處理器102-1之內，但亦可於系統100中之他處提供這些元件。例如，可將電源管理邏輯器140提供於VR 130之中、於電源120之中、直接耦接至互連體104、在一或多個（或者是所有的）處理器102之內等等。

假設我們有一個具有n個處理器的系統，並具有單一個熱核心，其中此熱核心之電力係以一個β的因數來降低（即乘上可能係落在0與1之間的β），以預防侵擾的熱限制。我們以各個處理器的減速之加權總和來衡量系統的總減速。例如，若4個核心中的一個核心被減速20%，則可將有效頻率因數判定為（3+0.8）/4或是95%。

在一個實施例中，可如下式來判定對不同熱管理方法之減速（其中S_{dvs}指的是對DVS之減速，而S_{ft}指的是對頻率控制之減速）：

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$S_{dvs} = \sqrt[3]{\beta}$（例如在所有的核心皆受罰的情況）

$S_{ft} = \frac{n-1}{n} \times 1 + \frac{1}{n} \times \beta$（例如在有一個核心受罰的情況）

參考第2圖，其依據一個實施例而繪示純節流對上DVS之相對增益。當於此論述時，「純」節流指的是僅以下列其中一種節流來減少於一處理器中的電力消耗時的情況：頻率節流（其通常僅指DVS對頻域的投射）、時鐘閘控（例如包含停用正反器並不改變狀態的迴路部份者）、及/或微架構節流（例如由晶片上型熱單元監控一處理器的接面溫度，並動態地調整處理器操作電壓及/或頻率，以在變動的環境條件下提供最大性能者）。

更具體地說，純節流對上DVS之間的關係可以公式 $S_{ft}/S_{dvs}-1$ 來描述。如可由參考第2圖所見的，增益隨著核心數目之增加而增加。請注意，在一些實施例中，對於雙核心來說，DVS可由於合理的β值而仍為較有吸引力的。在一個實施例中，可選擇性地將DVS及/或節流應用在一個處理器上，如將於本文中，例如參考第3圖，而更做論述的。

在一些實施例中，可基於核心數而判定是否要使用一或多個DVS及/或節流。例如，可將此等技術應用在具有多於兩個核心的處理器中。然而，亦可將此種技術應用在具有少於三個核心的處理器中。

第3圖繪示將一或多個所選技術應用在處理器的多個核心上，以管理電力的一個方法300之一實施例之流程圖。於一實施例中，可利用參考第1-2圖與6-7圖所論述的多個元

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件來執行參考第3圖所論述的一或多個操作。

請再次參考第1-3圖，可於一個操作302判定在一個多核心處理器中的哪個/哪些（及/或多少）核心正導致高溫問題（諸如高溫壓力或過高操作溫度）。例如，邏輯器140可接收來自於逼近核心106之感測器150的資訊。或者是，此可藉由估計電力消耗來完成，例如透過結合熱感測器150讀數的電力監控器145。

可於一個操作304判定在一個處理器中的多少核心為作動並冷卻的（舉例來說，於溫度值低於，例如由感測器150所檢測到的，一個過高臨界溫度值時）。舉例來說，邏輯器140可考慮在核心106之操作狀態上的統計數字（例如由監控器145、感測器150及/或核心106自身所提供的）來判定哪些核心106為作動並冷卻的。可於一個操作306將操作302及/或304之資訊考慮在內（包括多種懲罰，諸如參考第2圖所論述者，包括例如針對DVS的電壓轉換懲罰等等），以及可能限制（例如，我們可能不會想要減少一個熱核心的頻率太多，以維持必要應用程式的平滑操作），以判定要使用哪個/哪些技術來管理在一個多核心處理器中的電力消耗。可於一個操作308應用所選技術來節流或修改一或多個核心106的一個操作特性（諸如一處理器核心106的操作電壓及/或操作頻率）。例如，邏輯器140可考慮DVS、純節流技術或是其中的一些組合，以控制處理器102的電力消耗。此外，在一個實施例中，操作308可在例如DVS將所有的核心降低至某個電力狀態（P狀態），且熱核心被藉由

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其中一個純節流技術來額外減速時，應用這些技術的一種組合。

在一個實施例中，可連續（或是於一種週期性基礎上）重複方法300之操作，例如，在操作308之後，可毫無延遲地（或是在例如由一個計時邏輯器所設定的一段時間過去之後）重新開始操作302。在一些實施例中，方法300可允許一個處理器在針對共享相同電力平面的多個核心的熱限制應用程式中，降低熱管理效能懲罰。

然而，對於具有多個電力平面的處理器來說，可能會出現額外的電力管理挑戰。例如，若在系統100中出現共享相同電源120的多個電力平面，可能會需要針對個別的各個電力平面之限制以及各個封包的通盤限制，來滿足電力管理。藉著這麼做，在處理器資源並未被完全利用時，便有可能共享一個共同的封包電力/能量預算，並允許例如在一個圖形效果（GFX）密集的工作負載中針對更多的GFX效能來利用未使用的處理器核心電力。然而，亦可將於此參考多個電力平面所論述的技術應用於可利用單一個電力平面的實作。

一些目前的基於電力的管理方案可能會忽略電力管理的時間面，因為其通常僅應付目前時間點。因此，在一些實施例中，可利用准許下列動作的各個電力平面之能量預算：（1）以將時間面考慮在內的一種方式來界定個別的元件（如個別的處理器核心）與共享的限制（如於多個元件或處理器核心間所共享的）；（2）表達對應於不同時間內容

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的有效限制；（3）於限制中處理線上改變的情況。在一個實施例中，可於不同的電力平面間並於基於能量的定義下管理電力分佈。

在一些實施例中，可依據一個目前預算來管理能量預算且/或做出電力設定（例如電壓及/或頻率改變）。可藉由控制如下式的迭代式定義的能量預算來執行基於能量的電力管理：

$$E_{n+1} = \alpha E_n + (TDP_n - P_n)\Delta t_n \qquad (1),$$

其中TDP_n為在步驟n上的熱設計電力（TDP）電力界限；P_n為在時間Δt_n中於步驟n上所花費的電力，而α為衰減成份。例如，使用$\alpha = 0.999$來對應以秒記的視窗大小，而使用$\alpha = 0.9$來對應更小得多的視窗大小。E_n之表示對應能量「餘數」，其為系統未消耗的能量。衰減成份之值係由時間視窗大小之要求而界定的。同樣的，在一些實施例中，可由一個軟體應用程式或使用者來提供TDP值。

這種能量預算相當於將一個指數罩強加在各個時刻的TDP與此時此刻所花費的電力間之差異上，也就是說：

$$E(t) = \int_0^t \alpha^{t-x}(TDP(x) - P(x))dx.$$

因此，系統（如邏輯器140）可將TDP限制分別設定在各個電力平面上，或/且將TDP限制設定在整個IC封包上。依據所強加的限制，可在一些實施例中維持多種預算，例如在個別限制的情況下對各個電力平面維持預算或是在共享限制的情況下對各個封包維持預算。此外，可維持各個

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視窗大小的不同預算電力（由α表示）及/或TDP限制。請注意，在一些實施例中，此種框架平滑地處理當TDP即時改變（例如軟體應用程式或使用者所做的）時的情況。在一個實施例中，可維持一組能量預算E_n^k，其中，例如，k對應於一個特定限制，而n對應於時間步驟。此種電力管理機制的一個目標係要在最大化效能時將能量預算保持為正。

在一個實施例中，可界定控制器預算（例如由邏輯器140來實施）。對於各個電力平面i，我們定義由$f^i(E)$來表示的一個控制器函數，其將能量預算映射到這組離散的電力狀態。在一個實施例中，被要求為一個非遞減函數的一個控制器將一個$[E_{low}^i, E_{high}^i]$的範圍映射到離散的$[P_n^i, P_0^i]$範圍，其中，P_0^i為針對此電力平面的最大渦輪狀態，而P_n^i為最大效率狀態。低於E_{low}^i的預算值被映射至P_n^i，而高於E_{high}^i的預算值被映射到P_0^i。其他需求可包括達到某些定錨點的要求——例如，將零預算對應於被稱為P_1的保證電力狀態：

$$f^i(E) = P_n^i, E \le E_{low}^i$$
$$f^i(0) = P_1^i$$
$$f^i(E) = P_0^i, E \ge E_{high}^i$$

依據一個實施例，於第4圖中示出一個控制器函數的範例。具體的控制器可將一個特定電力平面的需求納入考慮（此種在P狀態之間之轉換上的懲罰）。

至於那些限制，則假設存在m個控制器，而$f^i(E)$對應於不同的電力平面。針對限制k，可判定描述預算在電力平

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面E^k間如何分佈的使用者（或應用程式所界定的）性能。例如，可將此種資訊以長度m的向量W_k之形式提供為一個輸入，以使項目i對應於前往電力平面i的預算部份。針對個別的限制來說，單一個電力平面係可獲得整個預算，以使對應的權重向量為一個單位向量。在一般情況中，電力平面i可獲得此預算部份：

$$E^{k,i} = W_{ki}E^k \qquad (2)$$

在某些情況中，我們可針對一個電力平面i而使用此式，它的$W_{ki}E^k$部份夠高，足以提供最大渦輪（即，$W_{ki}E^k \geq E^i_{high}$）。在這種情況中，針對此電力平面的「未使用」預算，$W_{ki}E^k - E^i_{high}$，可能會在剩餘的電力平面間依據其權重而分佈。

讓我們$E^{k,i}_n$以來表示於步驟t_n接收電力平面i的預算部份E^k，那麼在這個步驟上，針對各個電力平面i的建議結果P狀態可寫為：

$$u^i_n = \min_k f^i(E^{k,i}_n) \qquad (3)$$

集合在所有的限制上的這些建議值，可提供各個電力平面的結果設定。請注意，此結果可為一種上限，且在一些實施例中，可更以其他演算法來作修改。此外，依據本發明的一個實施例，第5圖中示出基於能量的電力管理的一個流程圖之範例。

更具體地說，第5圖繪示一個方法500之一實施例的流程圖，此方法對一個處理器的多個核心施用一或多個所選技術電力管理操作。在一個實施例中，可利用參考第1-4與

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6-7圖所論述的多個元件來執行參考第5圖所論述的一或多個操作。

請參考第1-5圖，可於一個操作502判定各個限制E_n^k的能量預算餘數（如由邏輯器140依據上文之（1）式而為）。可於一個操作504判定各個電力平面$E_n^{k,i}$的能量預算餘數（如由邏輯器140依據上文之（2）式而為）。可於一個操作506判定各個電力平面u_n^i的控制器建議值（如由邏輯器140依據上文之（3）式而為）。可於一個操作508判定時間步驟（如由邏輯器140而為），例如，以針對各個電力平面判定在下一個時期中的未來值。

在一個實施例中，可連續（或是於一種週期性基礎上）重複方法300之操作，例如，於操作308之後，可毫無延遲地（或是在例如由一個計時邏輯器所設定的一段時間過去之後）重新開始操作302。

在一個實施例中，可連續（或是於一種週期性基礎上）重複方法500之操作，例如，於操作508之後，可毫無延遲地（或是在例如由一個計時邏輯器所設定的一段時間過去之後）重新開始操作502。在一個實施例中，可將參考第2-3圖所論述的技術與第4-5圖結合。例如，可將參考第2-3圖所論述的技術應用於多個電力平面處理器上。同樣的，亦可將參考第4-5圖所論述的技術應用於單一個電力平面處理器上。

第6圖繪示依據本發明之一實施例的一個運算系統600之方塊圖。運算系統600可包括一或多個中央處理單元

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（CPU）或處理器602-1到602-P（其於此可以「一個處理器602」或「數個處理器602」來指稱）。處理器602可透過一個互連網（或匯流排）604來通訊。處理器602可包括一般用途處理器、網路處理器（處理在一個電腦網路603上通訊的資料）、或其他類型的處理器（包括精簡指令集電腦（RISC）處理器或複雜指令集電腦（CISC））。此外，處理器602可具有單一個或多個的核心設計。具有多核心設計的處理器602可在相同的積體電路（IC）晶粒上整合不同類型的處理器核心。同樣的，可將具有多核心設計的處理器602實施為對稱的或不對稱的多處理器。在一個實施例中，處理器602中的一或多個處理器可為與第1圖之處理器102相同或相似的。在一些實施例中，處理器602中的一或多個處理器可包括第1圖之一或多個核心106、邏輯器140、感測器150及或電力監控器145。同樣的，可由系統600的一或多個元件來執行參考第1-5圖所論述之操作。例如，一個電壓調節器（諸如第1圖之VR 130者）可於邏輯器140之方向調節供應給第6圖之一或多個元件之電壓。

晶片組606可亦與互連網604通訊。晶片組606可包括一個圖形與記憶體控制中樞（GMCH）608。GMCH 608可包括與一個記憶體612通訊的一個記憶體控制器610。記憶體612可儲存資料，包括由處理器602或是包括在運算系統600中的任何其他裝置所執行的指令序列。在本發明的一個實施例中，記憶體612可包括一或多個依電性儲存體（或記憶體）裝置，諸如隨機取記憶體（RAM）、動態RAM（DRAM）、

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同步DRAM（SDRAM）、靜態RAM（SRAM）或其他類型的儲存裝置等等。亦可利用諸如硬碟等的非依電記憶體。額外裝置可透過互連網604來通訊，諸如多CPU及/或多系統記憶體。

GMCH 608可亦包括與一個圖形加速器616通訊的一個圖形介面614。於本發明的一個實施例中，圖形介面614可透過一個加速圖形埠（AGP）來與圖形加速器616通訊。於本發明的一個實施例中，一個顯示器（諸如平面顯示器、陰極射線管（CRT）、投影螢幕等等）可經由例如一個訊號轉換器來與圖形介面614通訊，此訊號轉換器將儲存在諸如影像記憶體或系統記憶體等等的一個儲存裝置中之影像之數位表示型態轉譯成由顯示器所解譯與顯示的顯示訊號。由顯示裝置所產生的顯示訊號在由顯示器解譯與隨後在顯示器上顯示之前，可傳遞通過多種控制裝置。

一個控制中樞介面618可允許GMCH 608與一個輸入/輸出控制中樞（ICH）620來通訊。ICH 620可提供與運算系統600通訊的一個介面I/O裝置。ICH 620可透過一個週邊橋接器（或控制器）624，諸如週邊元件互連（PCI）橋接器、通用串列匯流排（USB）控制器或其他類型的週邊橋接器或控制器等等，來與一個匯流排622通訊。橋接器624可提供於處理器602與週邊裝置之間的一個資料路徑。可利用其他類型的拓樸。同樣的，多個匯流排可與ICH 620通訊，例如透過多個橋接器或控制器。此外，在本發明之多種實施例中，與ICH 620通訊的其他週邊設備可包括整合驅動機電

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子電路（IDE）或小型電腦系統介面（SCSI）硬式驅動機、USB埠、鍵盤、滑鼠、並列埠、串列埠、軟碟驅動機、數位輸出支援（如數位影像介面（DVI））或其他裝置。

匯流排622可與一個音訊裝置626、一或多個碟片驅動機628與一或多個網路介面裝置630（其與電腦網路603通訊）通訊。其他裝置可透過匯流排622來通訊。同樣的，在本發明之一些實施例中，多種元件（諸如網路介面裝置630者）可與GMCH 608通訊。除此之外，可將處理器602與GMCH 608結合，以形成單一個晶片。此外，於本發明之其他實施例中，可將圖形加速器616包括在GMCH 608中。

此外，運算系統600可包括依電性及/或非依電性記憶體（或儲存體）。例如，非依電性記憶體可包括一或多個下列項目：唯讀記憶體（ROM）、可規劃ROM（PROM）、可抹除PROM（EPROM）、電氣式EPROM（EEPROM）、碟片驅動機（如628）、軟碟、光碟ROM（CD-ROM）、數位多功能光碟（DVD）、快閃記憶體、磁光碟或可儲存電子資料（如，包括指令）的其他類型的非依電性機器可讀媒體。在一個實施例中，可以一種點對點（PtP）組態來安排系統600之元件。例如，可以多個點對點介面來將處理器、記憶體及/或輸入/輸出裝置互連。

第7圖依據本發明之一實施，繪示以一種點對點（PtP）組態來安排的一個運算系統700。具體說來，第7圖示出以多個點對點介面來互連處理器、記憶體與輸入/輸出裝置的一個系統。可由系統700之一或多個元件來執行參考第1-6

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圖所論述的操作。例如，一個電壓調節器（諸如第1圖之VR 130者）可調節供應給第7圖之一或多個元件之電壓。

如於第7圖中所繪示的，系統700可包括數個處理器，其中只有兩個，處理器702與704，為求簡明而示出。處理器702與704可各包括一個本地記憶體控制器中樞（MCH）706與708，以致能與記憶體710及712之通訊。記憶體710及/或712可儲存多種資料，諸如參考第6圖之記憶體612所論述的那些。同樣的，處理器702與704可包括第1圖之一或多個核心106、邏輯器140、感測器150及/或電力監控器145。

在一個實施例中，處理器702與704可為參考第6圖之記憶體612所論述的處理器602之一。處理器702與704可分別透過利用PtP介面電路716與718的一個點對點（PtP）介面714來交換資料。同樣的，處理器702及704各可透過個別的利用點對點介面電路726、728、730及732的PtP介面722及724來與晶片組720交換資料。晶片組720可更透過一個高效能圖形介面736來與一個高效能圖形電路734交換資料，例如利用一個PtP介面電路737。

在至少一個實施例中，可由處理器702或704及/或系統700的其他元件，諸如透過一個匯流排740來通訊的那些，來執行參考第1-6圖所論述的一或多個操作。然而，本發明之其他實施例係可存在於第7圖之其他電路、邏輯單元或系統700中之裝置中。此外，本發明之一些實施例係可散佈於數個電路、邏輯單元或於第7圖中所繪示的裝置中。

晶片組720可利用一個PtP介面電路741來與匯流排740

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通訊。匯流排740可具有與其通訊的一或多個裝置，諸如匯流排橋接器742與I/O裝置743。透過匯流排744，匯流排橋接器742可與諸如鍵盤/滑鼠745、通訊裝置746（諸如數據機、網路介面裝置或其他可與電腦網路603通訊之通訊裝置）、音訊I/O裝置及/或資料儲存裝置748等等的其他裝置通訊。資料儲存體裝置748可儲存可由處理器702及/或704來執行的程式碼749。

於本發明之多種實施例中，於此所論述的操作，例如參考第1-7圖者，可被實施為硬體（如邏輯迴路）、軟體、韌體或其中之組合，其可以電腦程式產品來提供，例如包括具有儲存有用以規劃電腦以執行於此所論述之處理的指令（或軟體程序）的機器可讀媒體或電腦可讀媒體。此種機器可讀媒體可包括諸如針對第1-7圖所論述的儲存體裝置。此外，可將此種電腦可讀媒體作為一個電腦程式產品而下載，其中，可藉由以載波或其他傳播媒體透過通訊鏈結（例如匯流排、數據機或網路連接）而提供的資料信號，而將程式從一個遠端電腦（如伺服器）傳送給一個請求電腦（如客戶端）。

貫穿本說明書之對於「一實施例」或「一個實施例」之指涉，意指關於此實施例所說明的一個特定的特色、結構或特徵係被包括在本發明之至少一個實施例中。因此，貫穿本說明中，多處出現之「在一實施例中」或「在一個實施例中」等詞語不需全都指涉相同的實施例。同時，於說明書與申請專利範圍中，可使用「耦接」與「連接」等

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詞語及其衍生詞。於本發明之一些實施例中，「連接」可係用來指出二或更多個元件為直接在實體上或電氣上彼此接觸。「耦接」可意指二或更多個元件為直接在實體上或電氣上接觸。然而，「耦接」可亦指二或多個元件可為不直接彼此接觸，但可仍彼此協作或互動。

因此，雖然本發明之實施例業已以特定於結構特徵及/或方法論行為之方式來論述，但應瞭解，所請求之標的可不受所論述之特定特徵或行為之限制。反之，此等特定特徵與行為係作為實施所請求之標的的樣本形式而論述。

【圖式簡單說明】

第1圖繪示運算系統之實施例的方塊圖，其可運用來實施本文中所論述的多種實施例。

第2圖繪示依據一些實施例的圖表。

第3圖繪示依據一些實施例的流程圖。

第4圖繪示依據一些實施例的圖表。

第5圖繪示依據一些實施例的流程圖。

第6圖繪示運算系統之實施例的方塊圖，其可運用來實施本文中所論述的多種實施例。

第7圖繪示運算系統之實施例的方塊圖，其可運用來實施本文中所論述的多種實施例。

【主要元件符號說明】

100、600、700...系統

102、602、602-1～602-P、702、704...處理器

104、112...互連體/匯流排

106...核心

108、116...快取記憶體

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110...路由器

114、612、710、712...記憶體

120...電源

130...電壓調節器

135...電源平面

140...邏輯器

145...監控器

150...感測器

300、500...方法

302～308、502～508...操作

603...電腦網路

604...互連網/匯流排

606、720...晶片組

608...圖形與記憶體控制中樞（GMCH）

610...記憶體控制器

614...圖形介面

616...圖形加速器

618...控制中樞介面

620...輸入/輸出控制中樞（ICH）

622、740、744...匯流排

624...週邊橋接器/控制器

626...音訊裝置

628...碟片驅動機

630...網路介面裝置

706、708...記憶體控制器中樞（MCH）

714、722、724...點對點（PtP）介面

716、718、726、728、730、732、737、741...PtP介面電路

734...高效能圖形電路

736...高效能圖形介面

742...匯流排橋接器

743...I/O裝置

745...鍵盤/滑鼠

746...通訊裝置

748...資料儲存體裝置

749...程式碼

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201022923

發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※申請案號：98136920

※申請日：98.10.30　　※IPC 分類：G06F 15/16 (2006.01)

一、發明名稱：（中文/英文）

用於多處理器核心之電力管理技術

POWER MANAGEMENT FOR MULTIPLE PROCESSOR CORES

二、中文發明摘要：

本文論述與用於多處理器核心之電力管理技術有關之方法與裝置。於一實施例中，可局部地（例如基於一種逐一核心的基礎）利用一或多種技術來管理一處理器中之電力消耗。於另一實施例中，可基於數種基於能量之考量，而將電力於一處理器的不同的電力平面間分配。本文亦揭露其他實施例，並加以請求專利。

三、英文發明摘要：

Methods and apparatus relating to power management for multiple processor cores are described. In one embodiment, one or more techniques may be utilized locally (e.g., on a per core basis) to manage power consumption in a processor. In another embodiment, power may be distributed among different power planes of a processor based on energy-based considerations. Other embodiments are also disclosed and claimed.

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七、申請專利範圍：

1. 一種裝置，其包含：

具有多個處理器核心的一個處理器；

單一個電力平面，用以對該等多個處理器核心中之一個以上核心提供電力；以及

一個電力管理邏輯器，用以響應於下列狀況而致使對該等多個處理器核心中之至少一個處理器核心的一個操作特徵造成修改：

於該至少一個處理器核心檢測到過度溫度；以及

判定該等多個處理器核心中之其他處理器核心中的哪一個核心為作動並處於一溫度值。

2. 如申請專利範圍第1項之裝置，其中該溫度值低於一個過度臨界溫度值。

3. 如申請專利範圍第1項之裝置，其中該電力管理邏輯器係用以致使：減少提供給該處理器之一個以上核心之電壓以及減少該至少一個處理器核心之該操作特徵。

4. 如申請專利範圍第1項之裝置，其中該至少一個處理器核心之該操作特徵包含下列項目中之一或多項：操作電壓以及操作頻率。

5. 如申請專利範圍第1項之裝置，其更包含一或多個感測器，用以對應於該等多個處理器核心中之一或多個核心檢測下列項目中之一或多項的變異：溫度、操作頻率、操作電壓與電力消耗。

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6. 如申請專利範圍第1項之裝置，其更包含一個電壓調節器，用以透過該單一個電力平面而對該處理器的一個以上核心提供電力。

7. 如申請專利範圍第1項之裝置，其中該等多個處理器核心本質上係由三或更多個處理器核心所組成。

8. 如申請專利範圍第1項之裝置，其中該處理器與該電力管理邏輯器係位於單一個積體電路上。

9. 如申請專利範圍第1項之裝置，其中該電力管理邏輯器係用以基於下列項目而針對多個電力平面中之各個電力平面來判定一個能量預算：

多個電力平面中之一對應電力平面的一個能量餘數，該能量餘數指出於先前的一個時期中有多少能量仍未遭消耗；以及

對應於該等多個電力平面中之各個電力平面的多個限制中之一或多個限制。

10. 一種裝置，其包含：

具有多個處理器核心的一個處理器；

多個電力平面，用以對該等多個處理器核心提供電力；以及

一個電力管理邏輯器，用以基於下列項目而針對該等多個電力平面中之各個電力平面來判定一個能量預算：

該等多個電力平面中之一對應電力平面的一個能量餘數，該能量餘數指出於先前的一個時期中

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有多少能量仍未遭消耗；以及

對應於該等多個電力平面中之各個電力平面的多個限制中之一或多個限制。

11. 如申請專利範圍第10項之裝置，其中該電力管理邏輯器係用以基於該時期中的一個熱設計電力（TDP）界限來判定該能量餘數。

12. 如申請專利範圍第10項之裝置，其中該電力管理邏輯器係用以基於該時期內所耗費的電力量來判定該能量餘數。

13. 如申請專利範圍第10項之裝置，其中該電力管理邏輯器係用以基於一個衰減成份來判定該能量餘數。

14. 如申請專利範圍第10項之裝置，其中該電力管理邏輯器係用以基於所有該等多個限制來針對該等多個電力平面中之各個電力平面而判定一個能量預算。

15. 如申請專利範圍第10項之裝置，其更包含一或多個感測器，用以對應於該等多個處理器核心中之一或多個核心檢測下列項目中之一或多項的變異：溫度、操作頻率、操作電壓與電力消耗。

16. 如申請專利範圍第10項之裝置，其更包含一個電壓調節器，用以透過該等多個電力平面而對該處理器提供電力。

17. 如申請專利範圍第10項之裝置，其中該電力管理邏輯器係用以響應於下列狀況而致使對該等多個處理器核心中之至少一個處理器核心的一個操作特徵造成修改：

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於該至少一個處理器核心檢測到過度溫度；以及

判定該等多個處理器核心中之其他處理器核心中的哪一個核心為作動並處於一溫度值。

18. 如申請專利範圍第17項之裝置，其中該溫度值低於一個過度臨界溫度值。

19. 如申請專利範圍第17項之裝置，其中該電力管理邏輯器係用以致使：減少提供給該處理器之一個以上核心的電壓以及減少該至少一個處理器核心之該操作特徵。

20. 一種方法，其包含下列步驟：

判定是否要響應於下列狀況而修改多個處理器核心中之至少一個處理器核心的一個操作特徵：於該至少一個處理器核心檢測到過度溫度、以及判定出該等多個處理器核心中之其他處理器核心中的哪一個核心為作動並處於一溫度值；以及

基於下列項目而針對耦接來對該等多個處理器核心提供電力的一或多個電力平面判定一個能量預算：該一或多個電力平面中之一對應電力平面的指出先前的一個時期中有多少能量仍未消耗的一個能量餘數、以及對應於該一或多個電力平面中之各個電力平面的一或多個限制。

21. 如申請專利範圍第20項之方法，其中該溫度值低於一個過度臨界溫度值。

22. 如申請專利範圍第20項之方法，其中該至少一個處理器

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核心之該操作特徵包含下列項目中之一或多項：操作電壓以及操作頻率。

23. 如申請專利範圍第20項之方法，其更包含檢測下列項目中之一或多項上對應於該等多個處理器核心中之一或多個處理器核心的變異：溫度、操作頻率、操作電壓與電力消耗。

24. 如申請專利範圍第20項之方法，其中針對一或多個電力平面判定該能量預算之步驟，係基於下列項目中之一或多項而執行：

於該時期中的一個熱設計電力（TDP）界限；

在該時期內所耗費的電力量；以及

一個衰減成份。

25. 一種系統，其包含：

具有多個處理器核心的一個處理器；

一或多個電力平面，用以對該等多個處理器核心提供電力；

一個電壓調節器，用以透過該一或多個電力平面而對該等多個處理器核心提供電力；以及

一個電力管理邏輯器，用以：

判定是否要響應於下列狀況而修改多個處理器核心中之至少一個處理器核心的一個操作特徵：於該至少一個處理器核心檢測到過度溫度、以及判定出該等多個處理器核心中之其他處理器核心中的哪一個核心為作動並處於一溫度值；以及

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基於下列項目而針對耦接來對該等多個處理器核心提供電力的一或多個電力平面判定一個能量預算：該一或多個電力平面中之一對應電力平面的指出先前的一個時期中有多少能量仍未消耗的一個能量餘數、以及對應於該一或多個電力平面中之各個電力平面的一或多個限制。

26. 如申請專利範圍第25項之系統，其更包含一或多個感測器，用以對應於該等多個處理器核心中之一或多個核心，檢測下列項目中之一或多項的變異：溫度、操作頻率、操作電壓與電力消耗。

27. 如申請專利範圍第25項之系統，其中該溫度值低於一個過度臨界溫度值。

28. 如申請專利範圍第25項之系統，其中該電力管理邏輯器係用以致使：減少提供給該處理器之一個以上核心的電壓、以及減少該至少一個處理器核心之該操作特徵。

29. 如申請專利範圍第25項之系統，其中該電力管理邏輯器係用以基於下列項目中之一或多項而判定該能量餘數：

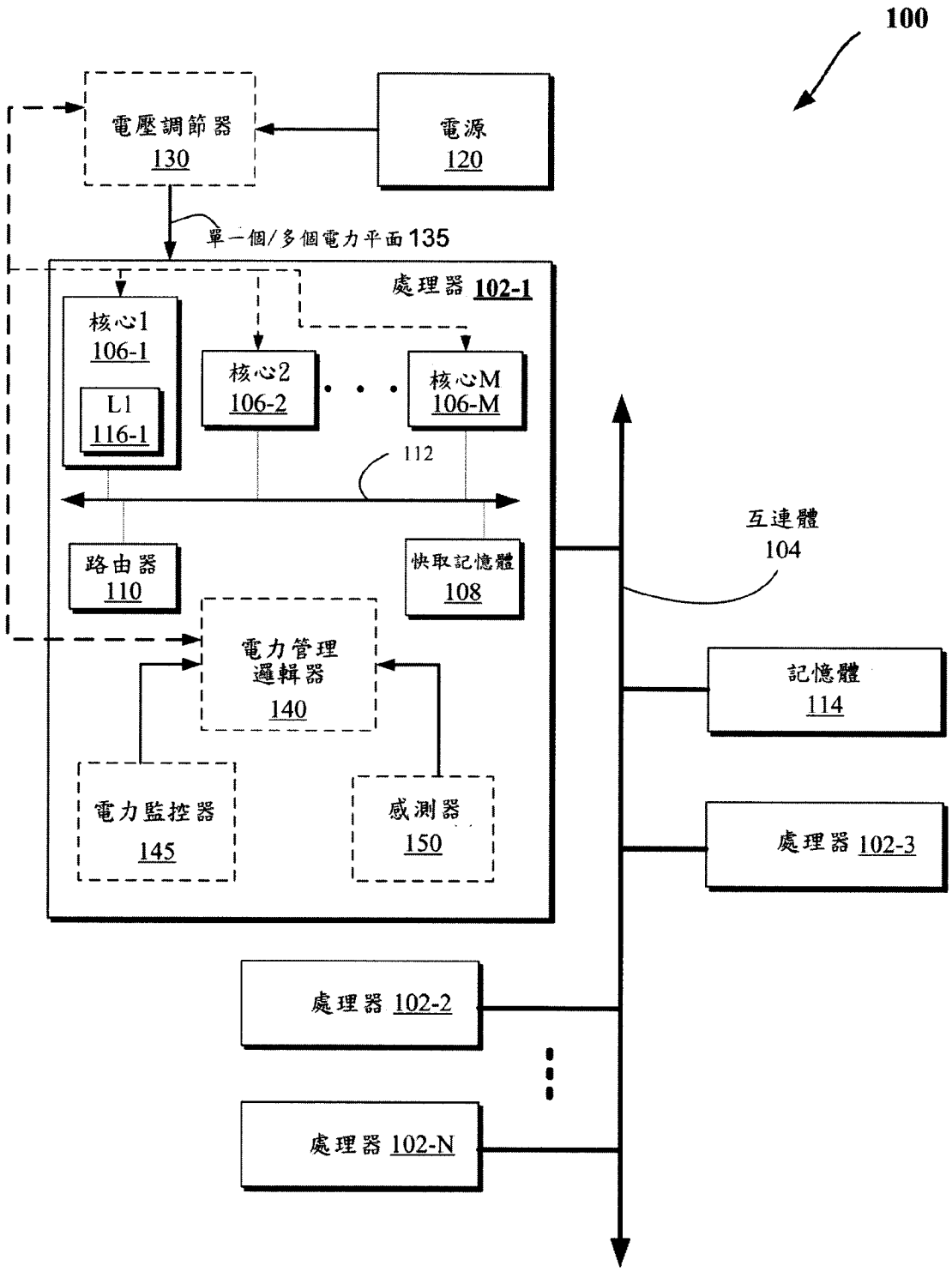
於該時期中的一個熱設計電力（TDP）界限；

在該時期內所耗費的電力量；以及

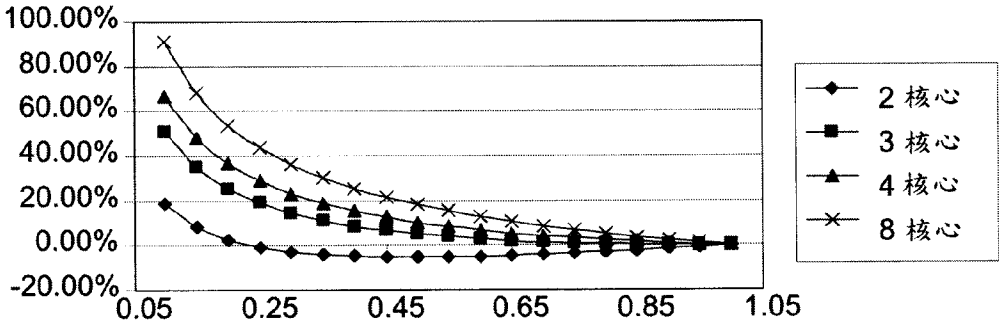
一個衰減成份。

30. 如申請專利範圍第25項之系統，其更包含一個音訊裝置。

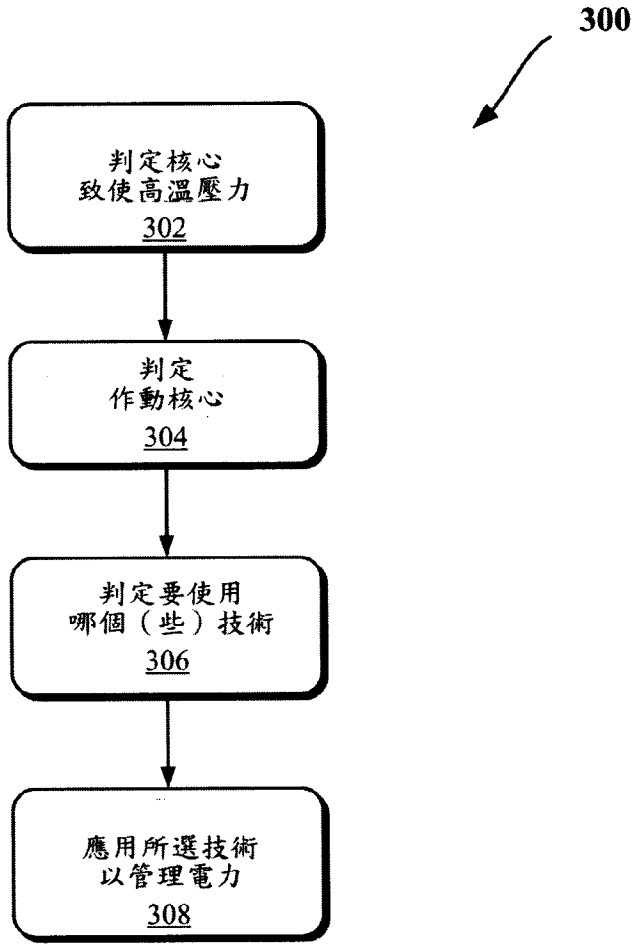
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100
電壓調節器
130
電源
120
單一個/多個電力平面135
處理器 102-1
核心1
106-1
L1
116-1
核心2
106-2
核心M
106-M
112
路由器
110
快取記憶體
108
電力管理
邏輯器
140
電力監控器
145
感測器
150
互連體
104
記憶體
114
處理器 102-3
處理器 102-2
處理器 102-N

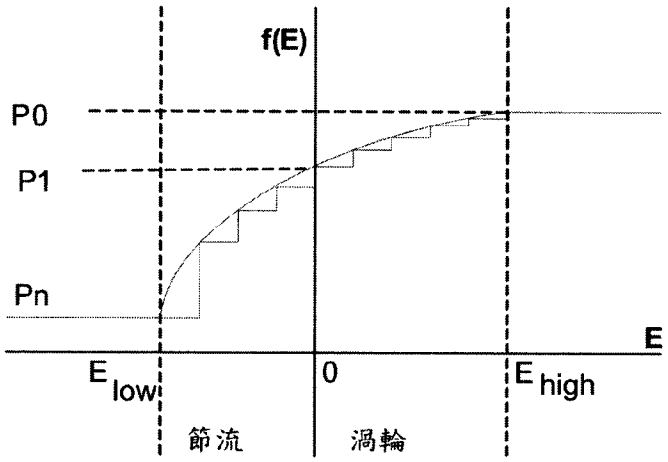
第1圖


100.00%
80.00%
60.00%
40.00%
20.00%
0.00%
-20.00%
0.05
0.25
0.45
0.65
0.85
1.05
2 核心
3 核心
4 核心
8 核心

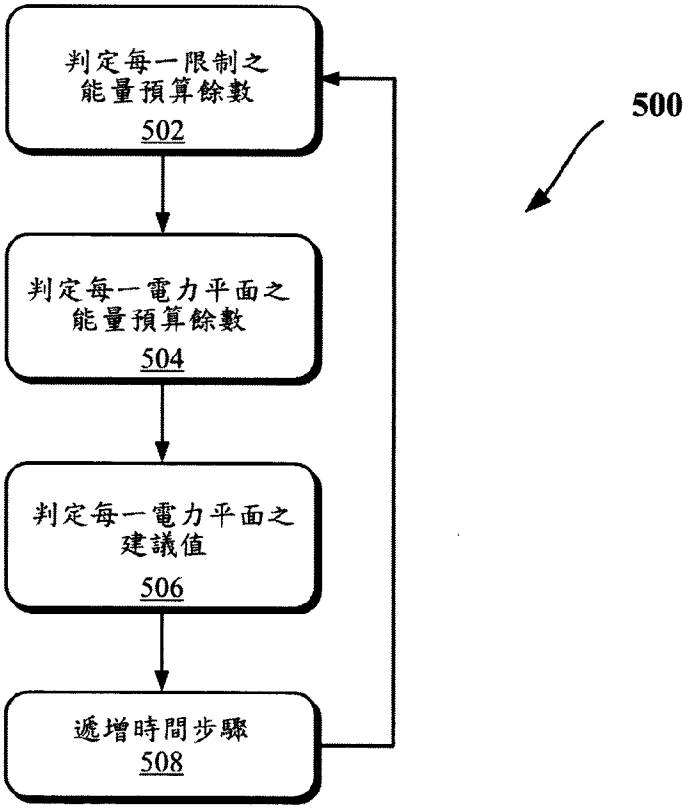
第2圖


300
判定核心
致使高溫壓力
302
判定
作動核心
304
判定要使用
哪個（些）技術
306
應用所選技術
以管理電力
308

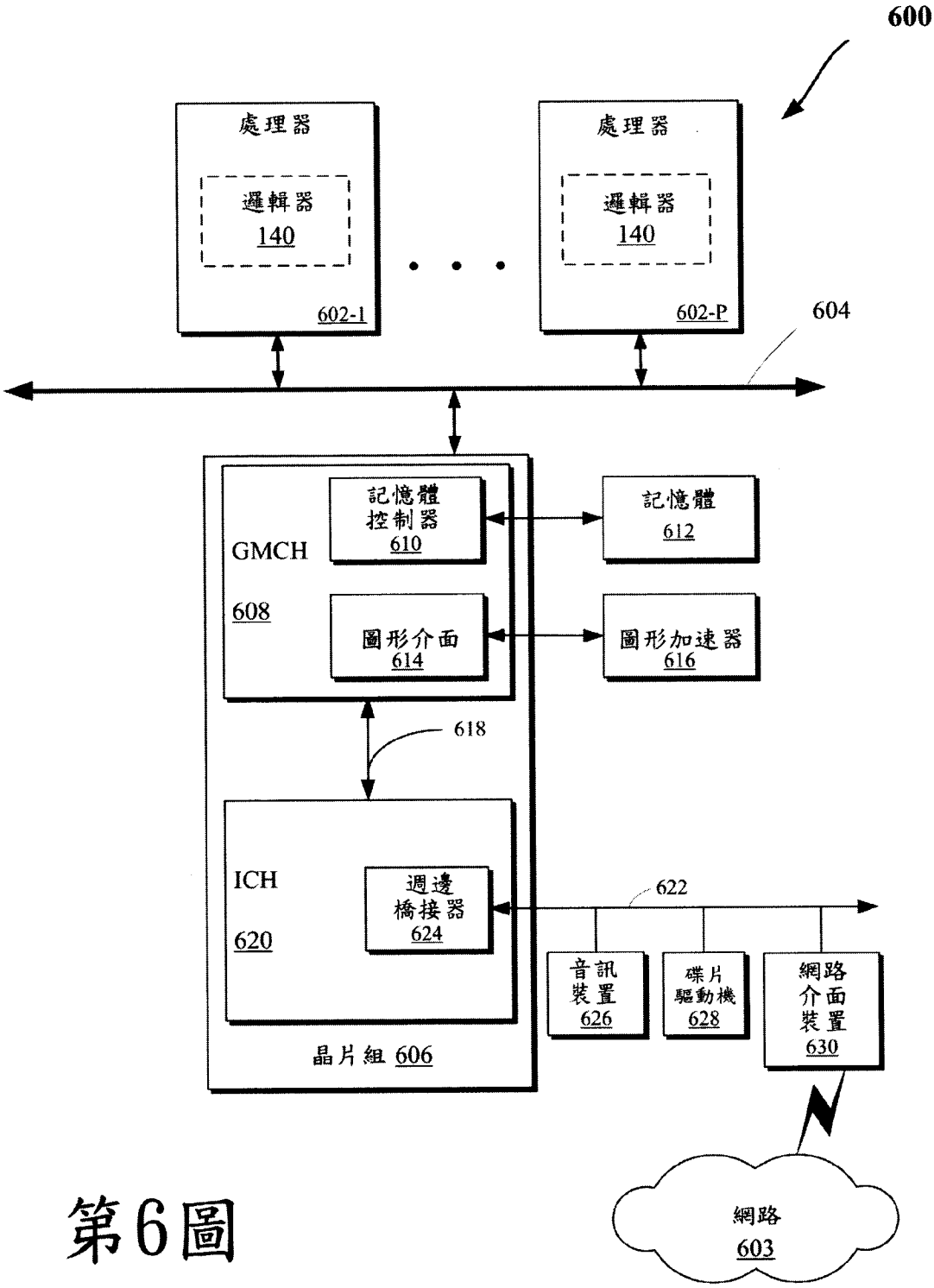
第3圖


f(E)
P0
P1
Pn
E
E low
0
E high
節流
渦輪

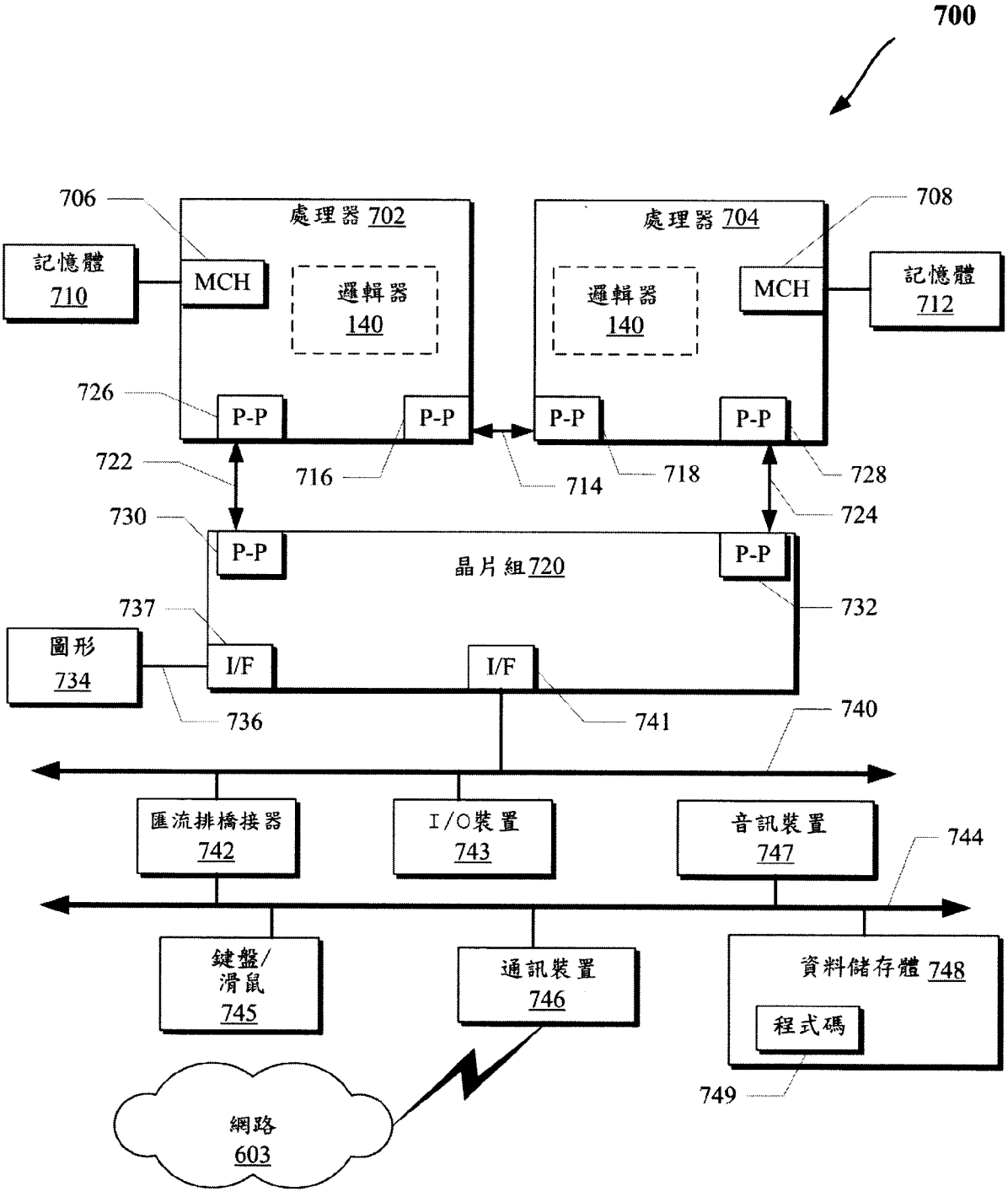
第4圖


判定每一限制之
能量預算餘數
502
判定每一電力平面之
能量預算餘數
504
判定每一電力平面之
建議值
506
遞增時間步驟
508
500

第5圖


600
處理器
邏輯器
140
602-1
處理器
邏輯器
140
602-P
604
GMCH
608
記憶體
控制器
610
記憶體
612
圖形介面
614
圖形加速器
616
618
ICH
620
週邊
橋接器
624
622
音訊
裝置
626
碟片
驅動機
628
網路
介面
裝置
630
晶片組 606
網路
603

第6圖


700
706
處理器 702
708
處理器 704
記憶體 710
MCH
邏輯器 140
邏輯器 140
MCH
記憶體 712
726
P-P
P-P
P-P
P-P
722
716
714
718
728
724
730
P-P
晶片組 720
P-P
737
732
圖形 734
I/F
I/F
736
741
740
匯流排橋接器 742
I/O裝置 743
音訊裝置 747
744
鍵盤/滑鼠 745
通訊裝置 746
資料儲存體 748
程式碼
749
網路 603

第7圖

四、指定代表圖：

(一)本案指定代表圖為：第（ 1 ）圖。

(二)本代表圖之元件符號簡單說明：

100...系統
102...處理器
104、112...互連體/匯流排
106...核心
108...快取記憶體
110...路由器
114...記憶體
120...電源
130...電壓調節器
135...電源平面
140...邏輯器
145...監控器
150...感測器

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

Petitioner Mercedes Ex-1009, 0136

Electronic Acknowledgement Receipt

EFS ID:	31614107
Application Number:	15138505
International Application Number:	
Confirmation Number:	3621
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/David Hopper
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2492C2US (P38407C2)
Receipt Date:	26-JAN-2018
Filing Date:	26-APR-2016
Time Stamp:	11:12:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ITL2492C2US_TW-D3_IDS.pdf	1035292 c9d46c52bacb8ea5de4eb7b3320032f822a76665	no	4

Warnings:

Petitioner Mercedes Ex-1009, 0137

Information:					
2	Foreign Reference	FR_1.pdf	2639944 7830ad64ef0afb27953635c29a2e1f8044333954	no	31
Warnings:					
Information:					
3	Foreign Reference	FR_2.pdf	3771358 7f2bc0bcceedc89af5c3f5f280d05ffca917020e	no	40
Warnings:					
Information:					
4	Other Reference-Patent/App/Search documents	TW-OA.pdf	567401 b088cac239b39f6ad53ddbb09662cd683f2c28d8	no	7
Warnings:					
Information:					
		Total Files Size (in bytes):	8013995		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
		§		
Serial No.:	15/138,505	§		
		§	Examiner:	Raymond Ngan Phan
Filed:	April 26, 2016	§		
		§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth In A Processor (As Amended)	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO OFFICE ACTION MAILED OCTOBER 5, 2017

Sir:

In response to the Office Action mailed October 5, 2017, please amend the above-referenced patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Petitioner Mercedes Ex-1009, 0139

Amendments to the Specification:

Please replace the title with the following amended title:

Enabling A Non-Core Domain To Control Memory Bandwidth In A Processor

Petitioner Mercedes Ex-1009, 0140

REMARKS/ARGUMENTS

Applicant gratefully acknowledges the indication that claims 22-31 and 39-41 are allowed.

The title has been amended, and thus it is respectfully submitted that the objection to the title is overcome.

Provided herewith is an e-Terminal Disclaimer and thus it is respectfully submitted that the obviousness-type double patenting rejection is overcome as to claim 32. As such, it is respectfully submitted that all claims are now in condition for allowance.

In view of the above amendment, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

Date: January 4, 2018

/Mark J. Rozman/

Mark J. Rozman
Registration No. 42,117
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, Texas 77057-2631
(512) 418-9944 [Phone]
(713) 468-8883 [Fax]
Customer No.: 47795

Petitioner Mercedes Ex-1009, 0141

Electronic Acknowledgement Receipt

EFS ID:	31404347
Application Number:	15138505
International Application Number:	
Confirmation Number:	3621
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2492C2US (P38407C2)
Receipt Date:	04-JAN-2018
Filing Date:	26-APR-2016
Time Stamp:	13:05:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	ITL2492C2USROA10-5-17.pdf	77199 b88b432521381a11547583fee9f9c5f9f9bb49b7	no	3

Warnings:

Petitioner Mercedes Ex-1009, 0142

Information:	
Total Files Size (in bytes):	77199

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	15138505
Filing Date	26-Apr-2016
First Named Inventor	Avinash Ananthakrishnan
Attorney Docket Number	ITL.2492C2US (P38407C2)
Title of Invention	Enabling A Non-Core Domain To Control Memory Bandwidth

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Intel Corporation	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

9354692

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.
Applicant claims the following fee status: ○ Small Entity ○ Micro Entity ◉ Regular Undiscounted I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number 42117 ○ A sole inventor ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ○ A joint inventor; all of whom are signing this request

Signature	/Mark J. Rozman/
Name	Mark J. Rozman

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	15138505
Filing Date:	26-Apr-2016
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Stephanie Petreas
Attorney Docket Number:	ITL.2492C2US (P38407C2)

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15138505

Filing Date: 26-Apr-2016

Applicant/Patent under Reexamination: Ananthakrishnan

Electronic Terminal Disclaimer filed on January 4, 2018

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	31395444
Application Number:	15138505
International Application Number:	
Confirmation Number:	3621
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2492C2US (P38407C2)
Receipt Date:	04-JAN-2018
Filing Date:	26-APR-2016
Time Stamp:	13:06:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$160
RAM confirmation Number	010418INTEFSW00013060201504
Deposit Account	201504
Authorized User	Stephanie Petreas

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33365 75d246d5cf7d33e8ed7be16960ad22d64c11c1c8	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30888 62aa73f929a1ba0a51a34b33880778a84ff2b558	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64253		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/138,505	04/26/2016	Avinash N. Ananthakrishnan	ITL.2492C2US (P38407C2)	3621

47795 7590 10/05/2017

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
10/05/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tphpto@tphm.com
Inteldocs_docketing@cpaglobal.com

Office Action Summary	Application No. 15/138,505	Applicant(s) ANANTHAKRISHNAN ET AL.	
	Examiner RAYMOND PHAN	Art Unit 2185	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *April 26, 2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *22-41* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *22-31 and 39-41* is/are allowed.

7)☒ Claim(s) *32-38* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *070816*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Petitioner Mercedes Ex-1009, 0152

Part III DETAILED ACTION

Notice to Applicant(s)

1. The present application is being examined under the pre-AIA first to invent provisions.

2. This application has been examined. Claims 22-41 are pending. Claims 1-21 are cancelled.

3. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2185.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on

nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

6. Claim 32 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 respectively of U.S. Patent No. 9,354,692. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of the US Patent No. 9,354,692 are similar in scope to claim 32 of the present application with only obvious wording variations.

In re Karlson, 136 USPQ 189 (ccPA 1963).

Allowable Subject Matter

7. Claims 22-31 and 39-41 are allowable over the prior of records.

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 22 and 39 are allowable over the prior art of record because the prior arts, cited in its entirety, or in combination, do not teach an interconnect of the processor to couple the first core of the plurality of cores, the

second core of the plurality of cores and the graphics unit to a memory external to the processor; and a power controller to control a frequency of the interconnect based at least in part on a frequency of the graphics unit, wherein the graphics unit is operable at a first plurality of frequencies and the interconnect is operable at a second plurality of frequencies, and the power controller is to update the frequency of the interconnect to another one of the second plurality of frequencies based at least in part on the frequency of the graphics unit (claim 22); an interconnect means for coupling the first core means, the second core means and the graphics means to a memory external to the apparatus; and a power control means for controlling a frequency of the interconnect means based at least in part on a frequency of the graphics means, wherein the graphics means is operable at a first plurality of frequencies and the interconnect means is operable at a second plurality of frequencies, and the power control means for updating the frequency of the interconnect means to another one of the second plurality of frequencies based at least in part on the frequency of the graphics means (claim 39).

Conclusion

9. Claim 32 is rejected. Claims 22-31 and 39-41 are allowed.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM. The Group Fax No. (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more

information about the PAIR system, see hop://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

/RAYMOND N PHAN/

Primary Examiner, Art Unit 2185

Notice of References Cited	Application/Control No. 15/138,505	Applicant(s)/Patent Under Reexamination ANANTHAKRISHNAN ET AL.	
	Examiner RAYMOND PHAN	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9,354,692 B2	05-2016	Ananthakrishnan; Avinash N.	G06F1/324	1/1
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

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	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	Art Unit
	RAYMOND PHAN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/29/2017								
	1	-								
	2	-								
	3	-								
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	23	=								
	24	=								
	25	=								
	26	=								
	27	=								
	28	=								
	29	=								
	30	=								
	31	=								
	32	✓								
	33	✓								
	34	✓								
	35	✓								
	36	✓								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	Art Unit
	RAYMOND PHAN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/29/2017								
	37	✓								
	38	✓								
	39	=								
	40	=								
	41	=								

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
Serial No.:	15/138,505	§		
		§	Examiner:	Unassigned
Filed:	April 26, 2016	§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Under 35 U.S.C. §120, this application relies on the earlier filing date of application serial number 14/451,807, filed August 5, 2014, which is a continuation of U.S. Patent Application Serial No. 13/282,896, filed October 27, 2011, now U.S. Patent No. 8,832,478, issued September 9, 2014. To the extent that any following foreign patent or non-patent literature references were submitted to and/or cited by the Office in the prior application, they are not provided in this application (pursuant to 37 C.F.R. §1.98(d) and M.P.E.P. §609.02(A)(2)).

Please apply any charges or credits to Deposit Account No. 50-4238.

Respectfully submitted,

Date: July 8, 2016

/Mark J. Rozman/
Mark J. Rozman
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Customer No.: 47795

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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(Not for submission under 37 CFR 1.99)

Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8832478		2014-09-09	Ananthakrishnan, et al.	

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	1							☐

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Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2 (P38407C2)

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	5	5621250		1997-04-15	Kim	
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	7	5163153		1992-11-10	Cole, et al.	
	8	5590341		1996-12-31	Matter	

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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(2)(P38407(2)

	9	5931950		1999-08-03	Hsu	
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Petitioner Mercedes Ex-1009, 0163

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	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	20	7437270		2008-10-14	Song, et al.	
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	23	6996728		2006-02-07	Singh	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Petitioner Mercedes Ex-1009, 0164

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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(Q)/P38407(2)

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	3	7146514		2006-12-05	Kaushik, et al.	
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	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

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	1	7603577		2009-10-13	Yamaji, et al.	
	2	7624215		2009-11-24	Axford, et al.	
	3	7752467		2010-07-06	Tokue	
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	1	20120096288		2012-04-19	Bates, et al.	
	2	20080136397		2008-06-12	Gunther, et al.	
	3	20080307240		2008-12-11	Dahan, et al.	

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Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2(P3840C2)

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	1	7624215		2009-11-24	Axford, et al.	
	2	7752467		2010-07-06	Tokue	
	3	7146514		2006-12-05	Kaushik, et al.	

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Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2JS (P38407C2)

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	3	8407319		2013-03-26	Chiu, et al.	
	4	6983389		2006-01-03	Filippo	
	5	7263457		2007-08-28	White, et al.	

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	1	20060053326		2006-03-09	Naveh, et al.	

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Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Ananthakrishnan, et al.
Art Unit	
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	2	8601288		2013-12-03	Brinks, et al.	
	3	7596464		2009-09-29	Hermerding, et al.	

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	1	20090271646		2009-10-29	Talwar, et al.	
	2	20070101174		2007-05-03	Tsukimori, et al.	
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First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2(P38407C2)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5287292		1994-02-15	Kenny, et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050288886		2005-12-29	Therien, et al.	
	2	20070106428		2007-05-10	Omizo, et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C3US (P38407C2)

	4	20100058078		2010-03-04	Branover, et al.	
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	8	20100250856		2010-09-03	Owen, et al.	

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	1	I342498	TW		2011-05-21	Asustek Comp Inc.		☒
	2	I344793	TW		2011-07-01	IND TECH RES INST		☒

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	Examiner Name	
	Attorney Docket Number	ITL.2492(2)P38407(2)

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	8	20060053326		2006-03-09	Naveh	
	9	20070005995		2007-01-04	Kardach, et al.	
	10	20040098560		2004-05-02	Storvik, et al.	
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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

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	Examiner Name	
	Attorney Docket Number	ITL.2492(P38407)

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	35	20090172375		2009-07-02	Rotem, et al.	
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Application Number	11513850S
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2184
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Attorney Docket Number	ITL.2492C2US (P38407C2)

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	1	20090292935		2009-11-26	Hallnor, et al.	
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	1	201009567	TW		2010-03-01	Hallnor, et al.		X

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	Attorney Docket Number	ITL.2492C2US (P38407C2)

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	3	200839497	TW		2008-10-01	Berry, et al.		☒

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	1	20090313489		2009-12-17	Gunther, et al.	
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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492CQUS (P38407CQ)

	2	20080005603		2008-01-03	Buch, et al.	

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	Attorney Docket Number	ITL.2492C2(P38407C2)

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	15	20130246825		2013-09-19	Shannon	

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	1	101403944	CN	A	2009-04-08	Gunther, et al.		☒
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	1	201120628	TW		2011-06-16	Hansquine, et al.		☒
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	Attorney Docket Number	ITL.2492C2 (P38407C2)

	1	KR 10-2006-012846	KR		2006-12-14	LG Electronics Inc.		☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	7	GRIGORIOS MAGKLIS, et al., "Profile-Based Dynamic Voltage and Frequency Scalling for a Multiple Clock Domain Microprocessor," 2003, pages 1-12.	☐
	8	GREG SEMERARO, et al., "Dynamic Frequency and Voltage Control for a Multiple Clock Domain Architecture," 2002, pages 1-12.	☐
	9	GREG SEMERARO, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," 2002, pages 29-40.	☐
	10	DIANA MARCULESCU, "Application Adaptive Energy Efficient Clustered Architectures," 2004, pages 344-349.	☐
	11	L. BENINI, et al., "System-Level Dynamic Power Management," 1999, pages 23-31.	☐
	12	RAVINDRA JEJURIKAR, et al., "Leakage Aware Dynamic Voltage Scaling For Real-Time Embedded Systems," 2004, pages 275-280.	☐
	13	RAVINDRA JEJURIKAR, et al., "Dynamic Slack Reclamation With Procrastination Scheduling In Real-Time Embedded Systems," 2005, pages 13-17.	☐
	14	R. TODLING, et al., "Some Strategies For Kalman Filtering and Smoothing," 1996, pages 1-21.	☐
	15	R.E. KALMAN, "A New Approach To Linear Filtering and Prediction Problems," 1960, pages 1-12.	☐
	16	INTEL TECHNOLOGY JOURNAL, "Power and Thermal Management in the Intel Core Duo Processor," May 15, 2006, pages 109-122.	☐
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	AVINASH N. ANANTHAKRISHNAN, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	1	U.S. Patent Application Serial No. 13/285,414, filed October 31, 2011, entitled "CONTROLLING A TURBO MODE FREQUENCY OF A PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2494)	☐
	2	U.S. Patent Application Serial No. 13/225,677, filed September 6, 2011, entitled "DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2495)	☐
	3	U.S. Patent Application Serial No. 13/247,580, filed September 28, 2011, entitled "CONTROLLING TEMPERATURE OF MULTIPLE DOMAINS OF A MULTI-DOMAIN PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2496)	☐
	4	U.S. Patent Application Serial No. 13/285,465, filed October 31, 2011, entitled "DYNAMICALLY CONTROLLING CACHE SIZE TO MAXIMIZE ENERGY EFFICIENCY," by AVINASH N. ANANTHAKRISHNAN, et al. (2497)	☐
	5	U.S. Patent Application Serial No. 13/282,947, filed October 27, 2011, entitled "CONTROLLING OPERATING FREQUENCY OF A CORE DOMAIN VIA A NON-CORE DOMAIN OF A MULTI-DOMAIN PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2493)	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C3US (P38407C3)

	1	U.S. Patent and Trademark Office, Office Action mailed July 31, 2014, in U.S. application no. 13/247,564. (2491)	☐
	2	U.S. Patent and Trademark Office, Office Action mailed January 16, 2014, with Reply filed April 9, 2014, in U.S. application no. 13/247,564. (2491)	☐
	3	U.S. Patent and Trademark Office, Office Action mailed June 6, 2014, with Reply filed September 4, 2014, in U.S. application no. 13/282,947. (2493)	☐
	4	U.S. Patent and Trademark Office, Office Action mailed May 16, 2014, with Reply filed August 12, 2014, in U.S. application no. 13/285,414. (2494)	☐
	5	U.S. Patent and Trademark Office, Final Office Action mailed May 14, 2014, with Request for Continued Examination filed August 13, 2014, in U.S. application no. 13/247,580. (2496)	☐
	6	U.S. Patent and Trademark Office, Office Action mailed August 18, 2014, in U.S. application no. 13/285,465. (2497)	☐

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	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2US (P38407C2)

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Taiwan Patent Office, Office action mailed August 21, 2014, in Taiwan application no.101135884.	☐
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	Attorney Docket Number	ITL.2492C2(P38407C2)

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	DAVID L. HILL, et al., "The Uncore: A Modular Approach To Feeding The High-Performance Cores," Intel Technology Journal, 2010, Vol 14, Issue 3, pages 30-49.	☐
	2	INTERNATIONAL SEARCHING AUTHORITY, "Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority," mailed March 28, 2013, in International application no. PCT/US2012/057655.	☐

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	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2492C2US (P38407C2)

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2016-07-08
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	75	core same entr$3 same map$4 same frequen$3	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:30
S2	4	"710"/$.ccls. and S1	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:30
S3	38	core same entr$3 same map$4 same bandwidth	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:32
S4	1	(non adj2 core) same map$4 same bandwidth	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:34
S5	122	(non adj2 core) same map$4	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:34
S6	4	"710"/$.ccls. and S5	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:34
S7	7	(non adj2 core) same map$4 same frequen$3	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:34
S8	8	(non adj2 core) same map$4 same frequen$4	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:35
S9	57	(non adj2 core) same bandwidth	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:36
S10	1	"20110022865"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:39
S11	2	"20080005603"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:39

EAST Search History (Prior Art)

S12	2	"20090070605"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:41
S13	27	un-core same core	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:43
S14	1	"7949887".pn. and frequency	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:47
S15	0	"7949887".pn. and (entr$3 or map$4)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:47
S16	1	"7949887".pn. and (entr$3 or map$4 or table)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:47
S17	1	"20090313489".PN.	US-PGPUB	OR	ON	2013/10/06 22:50
S18	1	"20080229128".PN.	US-PGPUB	OR	ON	2013/10/06 22:50
S19	1	"20070033425".PN.	US-PGPUB	OR	ON	2013/10/06 22:50
S20	1	"20060053326".PN.	US-PGPUB	OR	ON	2013/10/06 22:51
S21	1	"20050162188".PN.	US-PGPUB	OR	ON	2013/10/06 22:51
S22	1	"20050162188".PN.	US-PGPUB	OR	ON	2013/10/06 22:51
S23	1	"20050289365".PN.	US-PGPUB	OR	ON	2013/10/06 22:51
S24	1	"20050154931".PN.	US-PGPUB	OR	ON	2013/10/06 22:52
S25	1	"20040117678".PN.	US-PGPUB	OR	ON	2013/10/06 22:52
S26	1	"20030135768".PN.	US-PGPUB	OR	ON	2013/10/06 22:52
S27	1	"20030122429".PN.	US-PGPUB	OR	ON	2013/10/06 22:52
S28	1	"20030122429".PN.	US-PGPUB	OR	ON	2013/10/06 22:52
S29	1	"7664971".PN.	USPAT; USOCR	OR	ON	2013/10/06 22:53
S30	1	"7536597".PN.	USPAT; USOCR	OR	ON	2013/10/06 22:53
S31	1	"6983389".PN.	USPAT; USOCR	OR	ON	2013/10/06 22:53
S32	1	"7263457".PN.	USPAT; USOCR	OR	ON	2013/10/06 22:54
S33	0	un-core same map$4 same entr$3	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:55

EAST Search History (Prior Art)

S34	1	un-core and (map$4 same entr$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/06 22:55
S35	0	un-core same (frequenc$3 or clock$3) same (adjust$3 or compensat$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:40
S36	9	un-core same (frequenc$3 or clock$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:40
S37	16643	core same (frequenc$3 or clock$3) same (adjust$3 or compensat$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:41
S38	49	(non adj2 core) same (frequenc$3 or clock$3) same (adjust$3 or compensat$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:41
S39	159	"710"/$.ccls. and S37	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:42
S40	290	core same (frequenc$3 or clock$3) same (adjust$3 or compensat$3) same map$4	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:44
S41	11	"710"/$.ccls. and S40	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:44
S42	353	(frequenc$3 or clock$3) same map$4 same (switch$3 or interconnect$3) same minimum	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:46
S43	9	"710"/$.ccls. and S42	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 07:46
S44	790	"713"/$.ccls. and S37	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 08:07
S45	11	"713"/$.ccls. and S40	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2013/10/07 08:08

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CONFIRMATION NO. 3621

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/138,505	04/26/2016	713	2185	ITL.2492C2US (P38407C2)

APPLICANTS

Intel Corporation, Santa Clara, CA;

INVENTORS

Avinash N. Ananthakrishnan, Portland, OR;
Inder M. Sodhi, Folsom, CA;
Efraim Rotem, Haifa, ISRAEL;
Doron Rajwan, Rishon Le-Zion, ISRAEL;
Eliezer Weissmann, Haifa, ISRAEL;
Ryan Wells, Folsom, CA;

**** CONTINUING DATA ***************************

This application is a CON of 14/451,807 08/05/2014 PAT 9354692
which is a CON of 13/282,896 10/27/2011 PAT 8832478

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

05/09/2016

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /RAYMOND NGAN PHAN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		OR	5	1	1

ADDRESS

TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631
UNITED STATES

TITLE

Enabling A Non-Core Domain To Control Memory Bandwidth

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15138505	ANANTHAKRISHNAN ET AL.
	Examiner	Art Unit
	RAYMOND PHAN	2185

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 1/26; 1/30	09/25/17	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
G06F 1/3203	09/25/17	RP

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300-340	09/25/17	RP

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST SEARCHES	09/25/17	RP
CHECK PALM FOR DOUBLE PATENTING	09/25/17	RP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/RAYMOND PHAN/ Primary Examiner.Art Unit 2185

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
		§		
Serial No.:	15/138,505	§		
		§	Examiner:	Unassigned
Filed:	April 26, 2016	§		
		§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)
		§		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-referenced patent application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Petitioner Mercedes Ex-1009, 0199

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancelled)

Claims 2-21 (cancelled)

Claim 22 (new): A processor comprising:

a plurality of cores of the processor, a first core of the plurality of cores to operate at a first voltage and a second core of the plurality of cores to operate at a second voltage, the second voltage independent of the first voltage;

the first core of the plurality of cores to be associated with a first frequency and the second core of the plurality of cores to be associated with a second frequency, wherein the first and second frequencies may be different from each other;

a graphics unit of the processor, wherein a driver of the graphics unit is to control execution on the graphics unit;

an interconnect of the processor to couple the first core of the plurality of cores, the second core of the plurality of cores and the graphics unit to a memory external to the processor; and

a power controller to

control a frequency of the interconnect based at least in part on a frequency of the graphics unit,

wherein the graphics unit is operable at a first plurality of frequencies and the interconnect is operable at a second plurality of frequencies, and

the power controller is to update the frequency of the interconnect to another one of the second plurality of frequencies based at least in part on the frequency of the graphics unit.

Claim 23 (new): The processor of claim 22, wherein the power controller is to set the frequency of the interconnect to the another one of the second plurality of frequencies and

Petitioner Mercedes Ex-1009, 0200

set the frequency of the graphics unit to another one of the first plurality of frequencies, the another one of the second plurality of frequencies greater than the another one of the first plurality of frequencies.

Claim 24 (new): The processor of claim 22, wherein the driver of the graphics unit is to request the power controller to update the frequency of the interconnect based on a memory boundedness of a workload executed on the graphics unit.

Claim 25 (new): The processor of claim 24, wherein the driver of the graphics unit is to determine the memory boundedness based on statistics collected during execution of the workload on the graphics unit.

Claim 26 (new): The processor of claim 22, wherein the power controller is to control the frequency of the interconnect to be a maximum of a frequency requested by the driver of the graphics unit and a requested frequency requested by an operating system, and to reduce the frequency of the interconnect to the requested frequency when the graphics unit is to enter a low power mode.

Claim 27 (new): The processor of claim 22, wherein the interconnect comprises a ring interconnect.

Claim 28 (new): The processor of claim 22, further comprising a mailbox interface to enable the driver of the graphics unit to communicate with the power controller.

Claim 29 (new): The processor of claim 22, wherein the power controller includes a mapping table to map a frequency of the graphics unit to a minimum interconnect frequency.

Claim 30 (new): The processor of claim 29, wherein the power controller is to use the frequency of the graphics unit as an index to the mapping table.

Claim 31 (new): The processor of claim 29, wherein the driver of the graphics unit

Petitioner Mercedes Ex-1009, 0201

is to provide a first set of entries for the mapping table when the processor is enabled, and update at least some of the first set of entries based on a change to a workload.

Claim 32 (new): A processor comprising:

a plurality of cores of the processor, the plurality of cores including a first core operable at a first voltage and at a first frequency, and a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

a graphics unit of the processor, the graphics unit operable at a first variable frequency; and

an interconnect of the processor to couple the first core, the second core and the graphics unit to a memory external to the processor, the interconnect operable at a second variable frequency, the second variable frequency based at least in part on a value of the first variable frequency.

Claim 33 (new): The processor of claim 32, wherein the processor further comprises media processing circuitry.

Claim 34 (new): The processor of claim 32, wherein the graphics unit is to execute a 3D workload.

Claim 35 (new): The processor of claim 32, wherein the graphics unit is to execute a gaming workload.

Claim 36 (new): The processor of claim 35, wherein the processor is to increase the second variable frequency when the graphics unit is to execute the gaming workload.

Claim 37 (new): The processor of claim 32, wherein the processor is to decrease the second variable frequency when the graphics unit is to perform video playback.

Claim 38 (new): The processor of claim 32, further comprising a shared cache memory, wherein at least some of the plurality of cores are to share the shared cache memory.

Petitioner Mercedes Ex-1009, 0202

Claim 39 (new): An apparatus comprising:

a plurality of core means, a first core means of the plurality of core means for operating at a first voltage and a second core means of the plurality of core means for operating at a second voltage, the second voltage independent of the first voltage;

the first core means of the plurality of core means to be associated with a first frequency and the second core means of the plurality of core means to be associated with a second frequency, wherein the first and second frequencies may be different from each other;

a graphics means, wherein a driver means of the graphics means for controlling execution on the graphics means;

an interconnect means for coupling the first core means, the second core means and the graphics means to a memory external to the apparatus; and

a power control means for controlling a frequency of the interconnect means based at least in part on a frequency of the graphics means, wherein the graphics means is operable at a first plurality of frequencies and the interconnect means is operable at a second plurality of frequencies, and the power control means for updating the frequency of the interconnect means to another one of the second plurality of frequencies based at least in part on the frequency of the graphics means.

Claim 40 (new): The apparatus of claim 39, wherein the power control means is to set the frequency of the interconnect means to the another one of the second plurality of frequencies and set the frequency of the graphics means to another one of the first plurality of frequencies, the another one of the second plurality of frequencies greater than the another one of the first plurality of frequencies.

Claim 41 (new): The apparatus of claim 39, wherein the power control means is to increase the frequency of the interconnect means when the graphics means is to execute a gaming workload.

Petitioner Mercedes Ex-1009, 0203

REMARKS/ARGUMENTS

In view of the above amendment, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-4238.

Respectfully submitted,

Date: December 8, 2016

/Mark J. Rozman/

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Petitioner Mercedes Ex-1009, 0204

Electronic Acknowledgement Receipt

EFS ID:	27733493
Application Number:	15138505
International Application Number:	
Confirmation Number:	3621
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2492C2US (P38407C2)
Receipt Date:	08-DEC-2016
Filing Date:	26-APR-2016
Time Stamp:	12:40:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	ITL2492C2USSuppPreliminaryAmendment.pdf	83428 d5e5088a8bd2bb93c74f0724c31187891980637e	no	6

Warnings:

Petitioner Mercedes Ex-1009, 0205

Information:	
Total Files Size (in bytes):	83428

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/138,505	Filing Date 04/26/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **12/08/2016**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/POLIN ANG/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/138,505	04/26/2016	Avinash N. Ananthakrishnan	ITL.2492C2US (P38407C2)

CONFIRMATION NO. 3621

PUBLICATION NOTICE

47795
TROP, PRUNER & HU, P.C.
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

OC000000086798298

Title: Enabling A Non-Core Domain To Control Memory Bandwidth

Publication No.US-2016-0313778-A1
Publication Date:10/27/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Petitioner Mercedes Ex-1009, 0208

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
		§		
Serial No.:	15/138,505	§		
		§	Examiner:	Unassigned
Filed:	April 26, 2016	§		
		§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)
		§		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-referenced patent application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Petitioner Mercedes Ex-1009, 0209

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancelled)

Claim 2 (new): A processor comprising:

a first domain including a plurality of cores, at least some of the plurality of cores to operate at an independent voltage and frequency;

a second domain including at least one graphics unit to execute instructions, wherein a driver of the second domain is to control execution on the second domain;

an interconnect to couple the first domain and the second domain to a memory coupled to the processor; and

a power controller to control a frequency of the interconnect based at least in part on a frequency of the second domain.

Claim 3 (new): The processor of claim 2, wherein the power controller is to set the frequency of the interconnect to a first frequency and set the frequency of the second domain to a second frequency, the first frequency greater than the second frequency.

Claim 4 (new): The processor of claim 2, wherein the driver of the second domain is to request the power controller to update the frequency of the interconnect based on a memory boundedness of a workload executed on the second domain.

Claim 5 (new): The processor of claim 4, wherein the driver of the second domain is to determine the memory boundedness based on statistics collected during execution of the workload on the second domain.

Claim 6 (new): The processor of claim 4, wherein the first domain comprises the interconnect, and the power controller is to update a frequency of the first domain responsive to the second domain driver request.

Petitioner Mercedes Ex-1009, 0210

Claim 7 (new): The processor of claim 2, wherein the power controller is to control the frequency of the interconnect to be a maximum of a frequency requested by the driver of the second domain and a first domain frequency requested by an operating system, and to reduce the frequency of the interconnect to the first domain frequency when the second domain is to enter a low power mode.

Claim 8 (new): The processor of claim 2, wherein the interconnect comprises a ring interconnect.

Claim 9 (new): The processor of claim 2, further comprising a mailbox interface to enable the driver of the second domain to communicate with the power controller.

Claim 10 (new): The processor of claim 2, wherein the power controller includes a mapping table to map a frequency of the second domain to a minimum interconnect frequency.

Claim 11 (new): The processor of claim 10, wherein the power controller is to use the frequency of the second domain as an index to the mapping table.

Claim 12 (new): The processor of claim 10, wherein the driver of the second domain is to provide a first set of entries for the mapping table when the processor is enabled, and update at least some of the first set of entries based on a change to a workload.

Claim 13 (new): The processor of claim 2, wherein the power controller is to control the first domain and the second domain to operate at different voltage levels.

Claim 14 (new): The processor of claim 13, further comprising a third domain including the power controller, wherein the third domain is to operate at a fixed frequency.

Claim 15 (new): The processor of claim 2, wherein the power controller is to control at least one of the first domain and the second domain to dynamically enter into and exit

Petitioner Mercedes Ex-1009, 0211

one or more low power states.

Claim 16 (new): A method comprising:

receiving a message from a first domain of a processor, in a power controller of the processor via an interface, the message including a request to configure a mapping table to store a mapping between a frequency of the first domain and a minimum frequency of an interconnect that couples the first domain to a cache memory of the processor;

writing a plurality of entries of the mapping table, each entry including a mapping between a first domain frequency and a minimum interconnect frequency; and

controlling a frequency of the interconnect using the mapping table based at least in part on a frequency at which the first domain is operating.

Claim 17 (new): The method of claim 16, further comprising writing the plurality of entries including a ratio between a first domain frequency and an interconnect frequency.

Claim 18 (new): The method of claim 16, further comprising limiting the frequency of the interconnect to less than the minimum interconnect frequency for a corresponding frequency at which the first domain is operating when a second domain of the processor is thermally or power limited.

Claim 19 (new): A system comprising:

a multi-domain processor including an interconnect, a first domain having at least one core, a second domain including at least one graphics execution unit and a third domain including a power controller, the power controller to access a mapping table to map a frequency of the second domain to a minimum frequency of the interconnect, wherein the second domain is to send a request to the third domain to cause an update to a frequency of the interconnect based at least in part on a workload executed on the second domain and data in an entry of the mapping table; and

a dynamic random access memory (DRAM) coupled to the multi-domain processor.

Claim 20 (new): The system of claim 19, wherein a driver of the second domain is

Petitioner Mercedes Ex-1009, 0212

to write an indicator and an address into a first register of a mailbox interface and write data into a second register of the mailbox interface, and responsive to the indicator the third domain is to write the data into the entry of the mapping table addressed by the address in the first register.

Claim 21 (new): The system of claim 20, wherein the third domain is to control the frequency of the interconnect to be a maximum of a frequency requested by the driver of the second domain and a first domain frequency requested by an operating system.

Petitioner Mercedes Ex-1009, 0213

REMARKS/ARGUMENTS

In view of the above amendment, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-4238.

Respectfully submitted,

Date: August 12, 2016

/Mark J. Rozman/

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Petitioner Mercedes Ex-1009, 0214

Electronic Acknowledgement Receipt

EFS ID:	26627971
Application Number:	15138505
International Application Number:	
Confirmation Number:	3621
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2492C2US (P38407C2)
Receipt Date:	12-AUG-2016
Filing Date:	26-APR-2016
Time Stamp:	14:24:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	ITL2492C2USPreliminaryAmendment.pdf	82482 e5bc86ff94baf07db12fe836bc70be3b8f2e5f96	no	6

Warnings:

Petitioner Mercedes Ex-1009, 0215

Information:	
Total Files Size (in bytes):	82482

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
		§		
Serial No.:	15/138,505	§		
		§	Examiner:	Unassigned
Filed:	April 26, 2016	§		
		§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)
		§		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-referenced patent application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Petitioner Mercedes Ex-1009, 0217

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancelled)

Claim 2 (new): A processor comprising:

a first domain including a plurality of cores, at least some of the plurality of cores to operate at an independent voltage and frequency;

a second domain including at least one graphics unit to execute instructions, wherein a driver of the second domain is to control execution on the second domain;

an interconnect to couple the first domain and the second domain to a memory coupled to the processor; and

a power controller to control a frequency of the interconnect based at least in part on a frequency of the second domain.

Claim 3 (new): The processor of claim 2, wherein the power controller is to set the frequency of the interconnect to a first frequency and set the frequency of the second domain to a second frequency, the first frequency greater than the second frequency.

Claim 4 (new): The processor of claim 2, wherein the driver of the second domain is to request the power controller to update the frequency of the interconnect based on a memory boundedness of a workload executed on the second domain.

Claim 5 (new): The processor of claim 4, wherein the driver of the second domain is to determine the memory boundedness based on statistics collected during execution of the workload on the second domain.

Claim 6 (new): The processor of claim 4, wherein the first domain comprises the interconnect, and the power controller is to update a frequency of the first domain responsive to the second domain driver request.

Petitioner Mercedes Ex-1009, 0218

Claim 7 (new): The processor of claim 2, wherein the power controller is to control the frequency of the interconnect to be a maximum of a frequency requested by the driver of the second domain and a first domain frequency requested by an operating system, and to reduce the frequency of the interconnect to the first domain frequency when the second domain is to enter a low power mode.

Claim 8 (new): The processor of claim 2, wherein the interconnect comprises a ring interconnect.

Claim 9 (new): The processor of claim 2, further comprising a mailbox interface to enable the driver of the second domain to communicate with the power controller.

Claim 10 (new): The processor of claim 2, wherein the power controller includes a mapping table to map a frequency of the second domain to a minimum interconnect frequency.

Claim 11 (new): The processor of claim 10, wherein the power controller is to use the frequency of the second domain as an index to the mapping table.

Claim 12 (new): The processor of claim 10, wherein the driver of the second domain is to provide a first set of entries for the mapping table when the processor is enabled, and update at least some of the first set of entries based on a change to a workload.

Claim 13 (new): The processor of claim 2, wherein the power controller is to control the first domain and the second domain to operate at different voltage levels.

Claim 14 (new): The processor of claim 13, further comprising a third domain including the power controller, wherein the third domain is to operate at a fixed frequency.

Claim 15 (new): The processor of claim 2, wherein the power controller is to control at least one of the first domain and the second domain to dynamically enter into and exit

Petitioner Mercedes Ex-1009, 0219

one or more low power states.

Claim 16 (new): A method comprising:

receiving a message from a first domain of a processor, in a power controller of the processor via an interface, the message including a request to configure a mapping table to store a mapping between a frequency of the first domain and a minimum frequency of an interconnect that couples the first domain to a cache memory of the processor;

writing a plurality of entries of the mapping table, each entry including a mapping between a first domain frequency and a minimum interconnect frequency; and

controlling a frequency of the interconnect using the mapping table based at least in part on a frequency at which the first domain is operating.

Claim 17 (new): The method of claim 16, further comprising writing the plurality of entries including a ratio between a first domain frequency and an interconnect frequency.

Claim 18 (new): The method of claim 16, further comprising limiting the frequency of the interconnect to less than the minimum interconnect frequency for a corresponding frequency at which the first domain is operating when a second domain of the processor is thermally or power limited.

Claim 19 (new): A system comprising:

a multi-domain processor including an interconnect, a first domain having at least one core, a second domain including at least one graphics execution unit and a third domain including a power controller, the power controller to access a mapping table to map a frequency of the second domain to a minimum frequency of the interconnect, wherein the second domain is to send a request to the third domain to cause an update to a frequency of the interconnect based at least in part on a workload executed on the second domain and data in an entry of the mapping table; and

a dynamic random access memory (DRAM) coupled to the multi-domain processor.

Claim 20 (new): The system of claim 19, wherein a driver of the second domain is

Petitioner Mercedes Ex-1009, 0220

to write an indicator and an address into a first register of a mailbox interface and write data into a second register of the mailbox interface, and responsive to the indicator the third domain is to write the data into the entry of the mapping table addressed by the address in the first register.

Claim 21 (new): The system of claim 20, wherein the third domain is to control the frequency of the interconnect to be a maximum of a frequency requested by the driver of the second domain and a first domain frequency requested by an operating system.

Petitioner Mercedes Ex-1009, 0221

REMARKS/ARGUMENTS

In view of the above amendment, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-4238.

Respectfully submitted,

Date: August 12, 2016

/Mark J. Rozman/

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Customer No.: 47795

Petitioner Mercedes Ex-1009, 0222

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
		§		
Serial No.:	15/138,505	§		
		§	Examiner:	Unassigned
Filed:	April 26, 2016	§		
		§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)
		§		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-referenced patent application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Petitioner Mercedes Ex-1009, 0223

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancelled)

Claim 2 (new): A processor comprising:

a first domain including a plurality of cores, at least some of the plurality of cores to operate at an independent voltage and frequency;

a second domain including at least one graphics unit to execute instructions, wherein a driver of the second domain is to control execution on the second domain;

an interconnect to couple the first domain and the second domain to a memory coupled to the processor; and

a power controller to control a frequency of the interconnect based at least in part on a frequency of the second domain.

Claim 3 (new): The processor of claim 2, wherein the power controller is to set the frequency of the interconnect to a first frequency and set the frequency of the second domain to a second frequency, the first frequency greater than the second frequency.

Claim 4 (new): The processor of claim 2, wherein the driver of the second domain is to request the power controller to update the frequency of the interconnect based on a memory boundedness of a workload executed on the second domain.

Claim 5 (new): The processor of claim 4, wherein the driver of the second domain is to determine the memory boundedness based on statistics collected during execution of the workload on the second domain.

Claim 6 (new): The processor of claim 4, wherein the first domain comprises the interconnect, and the power controller is to update a frequency of the first domain responsive to the second domain driver request.

Petitioner Mercedes Ex-1009, 0224

Claim 7 (new): The processor of claim 2, wherein the power controller is to control the frequency of the interconnect to be a maximum of a frequency requested by the driver of the second domain and a first domain frequency requested by an operating system, and to reduce the frequency of the interconnect to the first domain frequency when the second domain is to enter a low power mode.

Claim 8 (new): The processor of claim 2, wherein the interconnect comprises a ring interconnect.

Claim 9 (new): The processor of claim 2, further comprising a mailbox interface to enable the driver of the second domain to communicate with the power controller.

Claim 10 (new): The processor of claim 2, wherein the power controller includes a mapping table to map a frequency of the second domain to a minimum interconnect frequency.

Claim 11 (new): The processor of claim 10, wherein the power controller is to use the frequency of the second domain as an index to the mapping table.

Claim 12 (new): The processor of claim 10, wherein the driver of the second domain is to provide a first set of entries for the mapping table when the processor is enabled, and update at least some of the first set of entries based on a change to a workload.

Claim 13 (new): The processor of claim 2, wherein the power controller is to control the first domain and the second domain to operate at different voltage levels.

Claim 14 (new): The processor of claim 13, further comprising a third domain including the power controller, wherein the third domain is to operate at a fixed frequency.

Claim 15 (new): The processor of claim 2, wherein the power controller is to control at least one of the first domain and the second domain to dynamically enter into and exit

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one or more low power states.

Claim 16 (new): A method comprising:

receiving a message from a first domain of a processor, in a power controller of the processor via an interface, the message including a request to configure a mapping table to store a mapping between a frequency of the first domain and a minimum frequency of an interconnect that couples the first domain to a cache memory of the processor;

writing a plurality of entries of the mapping table, each entry including a mapping between a first domain frequency and a minimum interconnect frequency; and

controlling a frequency of the interconnect using the mapping table based at least in part on a frequency at which the first domain is operating.

Claim 17 (new): The method of claim 16, further comprising writing the plurality of entries including a ratio between a first domain frequency and an interconnect frequency.

Claim 18 (new): The method of claim 16, further comprising limiting the frequency of the interconnect to less than the minimum interconnect frequency for a corresponding frequency at which the first domain is operating when a second domain of the processor is thermally or power limited.

Claim 19 (new): A system comprising:

a multi-domain processor including an interconnect, a first domain having at least one core, a second domain including at least one graphics execution unit and a third domain including a power controller, the power controller to access a mapping table to map a frequency of the second domain to a minimum frequency of the interconnect, wherein the second domain is to send a request to the third domain to cause an update to a frequency of the interconnect based at least in part on a workload executed on the second domain and data in an entry of the mapping table; and

a dynamic random access memory (DRAM) coupled to the multi-domain processor.

Claim 20 (new): The system of claim 19, wherein a driver of the second domain is

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to write an indicator and an address into a first register of a mailbox interface and write data into a second register of the mailbox interface, and responsive to the indicator the third domain is to write the data into the entry of the mapping table addressed by the address in the first register.

Claim 21 (new): The system of claim 20, wherein the third domain is to control the frequency of the interconnect to be a maximum of a frequency requested by the driver of the second domain and a first domain frequency requested by an operating system.

Petitioner Mercedes Ex-1009, 0227

REMARKS/ARGUMENTS

In view of the above amendment, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-4238.

Respectfully submitted,

Date: August 12, 2016

/Mark J. Rozman/

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Customer No.: 47795

Petitioner Mercedes Ex-1009, 0228

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/138,505	Filing Date 04/26/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **08/12/2016**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LDRC
ADRIANE WINSTON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/138,505	04/26/2016	2184	1740	ITL.2492C2US (P38407C2)	1	1

CONFIRMATION NO. 3621

UPDATED FILING RECEIPT

47795
TROP, PRUNER & HU, P.C.
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

OC000000084477819

Date Mailed: 07/20/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Avinash N. Ananthakrishnan, Portland, OR;
Inder M. Sodhi, Folsom, CA;
Efraim Rotem, Haifa, ISRAEL;
Doron Rajwan, Rishon Le-Zion, ISRAEL;
Eliezer Weissmann, Haifa, ISRAEL;
Ryan Wells, Folsom, CA;

Applicant(s)

Intel Corporation, Santa Clara, CA;

Power of Attorney: The patent practitioners associated with Customer Number 47795

Domestic Priority data as claimed by applicant

This application is a CON of 14/451,807 08/05/2014 PAT 9354692
which is a CON of 13/282,896 10/27/2011 PAT 8832478

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Petitioner Mercedes Ex-1009, 0230

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/09/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/138,505**

Projected Publication Date: 10/27/2016

Non-Publication Request: No

Early Publication Request: No

Title

Enabling A Non-Core Domain To Control Memory Bandwidth

Preliminary Class

710

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/138,505

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
		§		
Serial No.:	15/138,505	§		
		§	Examiner:	Unassigned
Filed:	April 26, 2016	§		
		§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)
		§		

Mail Stop **Missing Parts**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO NOTICE MAILED MAY 11, 2016

Sir:

In response to the Notice to File Missing Parts of Nonprovisional Application mailed May 11, 2016, please find attached:

(1) the basic filing fee, surcharge, search fee and examination fee.

The Commissioner is authorized to charge the requisite fee of $1740.00, along with any additional fees required, or credit any over payment to Deposit Account No. 50-4238.

Respectfully submitted,

Date: July 8, 2016

/Mark J. Rozman/

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(713) 468-8883 [Fax]
Customer No.: 47795

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Avinash N. Ananthakrishnan, et al.	§	Group Art Unit:	2184
Serial No.:	15/138,505	§		
		§	Examiner:	Unassigned
Filed:	April 26, 2016	§		
For:	Enabling A Non-Core Domain To Control Memory Bandwidth	§	Atty. Dkt. No.:	ITL.2492C2US (P38407C2)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Under 35 U.S.C. §120, this application relies on the earlier filing date of application serial number 14/451,807, filed August 5, 2014, which is a continuation of U.S. Patent Application Serial No. 13/282,896, filed October 27, 2011, now U.S. Patent No. 8,832,478, issued September 9, 2014. To the extent that any following foreign patent or non-patent literature references were submitted to and/or cited by the Office in the prior application, they are not provided in this application (pursuant to 37 C.F.R. §1.98(d) and M.P.E.P. §609.02(A)(2)).

Please apply any charges or credits to Deposit Account No. 50-4238.

Respectfully submitted,

Date: July 8, 2016

/Mark J. Rozman/
Mark J. Rozman
Registration No. 42,117
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, Texas 77057-2631
(512) 418-9944 [Phone]
(713) 468-8883 [Fax]
Customer No.: 47795

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8832478		2014-09-09	Ananthakrishnan, et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2 (P38407C2)

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7434073		2008-10-07	Magklis	
	2	6792392		2004-09-14	Knight	
	3	7194643		2007-03-20	Gonzalez, et al.	
	4	7010708		2006-03-07	Ma	
	5	5621250		1997-04-15	Kim	
	6	7412615		2008-08-12	Yokota, et al.	
	7	5163153		1992-11-10	Cole, et al.	
	8	5590341		1996-12-31	Matter	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(2)(P38407(2)

	9	5931950		1999-08-03	Hsu	
	10	7454632		2008-11-18	Kardach, et al.	
	11	5522087		1996-05-28	Hsiang	
	12	7272730		2007-09-18	Acquaviva, et al.	
	13	7529956		2009-05-05	Stufflebeam	
	14	7730340		2010-06-01	Hu, et al.	
	15	7539885		2009-05-26	Ma	
	16	6748546		2004-06-08	Mirov, et al.	
	17	6829713		2004-12-07	Cooper, et al.	
	18	71111179		2006-09-19	Girson, et al.	
	19	6823516		2004-11-23	Cooper	

Petitioner Mercedes Ex-1009, 0239

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	20	7437270		2008-10-14	Song, et al.	
	21	7093147		2006-08-15	Farkas, et al.	
	22	7043649		2006-05-09	Terrell	
	23	6996728		2006-02-07	Singh	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090150695		2009-06-11	Song, et al.	
	2	20090150696		2009-06-11	Song, et al.	
	3	20110154090		2011-06-23	Dixon, et al.	
	4	20070214342		2007-09-13	Newburn	
	5	20070079294		2007-04-05	Knight	

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Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492(2)/P38407(2)

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6908227		2005-06-21	Fusu, et al.	
	2	7797512		2010-09-14	Cheng, et al.	
	3	7146514		2006-12-05	Kaushik, et al.	
	4	8015427		2011-09-06	Miller, et al.	
	5	7966511		2011-06-21	Naveh, et al.	
	6	7434073		2008-10-07	Magklis, et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear

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	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
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	Attorney Docket Number	ITL.2492C2(P38407C2)

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7603577		2009-10-13	Yamaji, et al.	
	2	7624215		2009-11-24	Axford, et al.	
	3	7752467		2010-07-06	Tokue	
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20120096288		2012-04-19	Bates, et al.	
	2	20080136397		2008-06-12	Gunther, et al.	
	3	20080307240		2008-12-11	Dahan, et al.	

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Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan, et al.
Art Unit	2184
Examiner Name	
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	1	7624215		2009-11-24	Axford, et al.	
	2	7752467		2010-07-06	Tokue	
	3	7146514		2006-12-05	Kaushik, et al.	

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	1	20080136397		2008-06-12	Gunther, et al.	
	2	20080307240		2008-12-11	Dahan, et al.	
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First Named Inventor	Avinash N. Ananthakrishnan, et al.
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Attorney Docket Number	ITL.2492C2US (P38407C2)

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	1	7949887		2011-05-24	Gunther, et al.	
	2	8370551		2013-02-05	Ohmacht, et al.	
	3	8407319		2013-03-26	Chiu, et al.	
	4	6983389		2006-01-03	Filippo	
	5	7263457		2007-08-28	White, et al.	

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	1	20060053326		2006-03-09	Naveh, et al.	

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First Named Inventor	Ananthakrishnan, et al.
Art Unit	
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

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	1	7574321		2009-08-11	Kernahan, et al.	
	2	8601288		2013-12-03	Brinks, et al.	
	3	7596464		2009-09-29	Hermerding, et al.	

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	1	20090271646		2009-10-29	Talwar, et al.	
	2	20070101174		2007-05-03	Tsukimori, et al.	
	3	20080307240		2008-12-11	Dahan, et al.	

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	1	5287292		1994-02-15	Kenny, et al.	
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	1	20050288886		2005-12-29	Therien, et al.	
	2	20070106428		2007-05-10	Omizo, et al.	
	3	20080077282		2008-03-27	Hartman, et al.	
	4	20040030940		2004-02-12	Espinoza-Ibarra, et al.	
	5	20120114010		2012-05-10	Branch	

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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2US (P38407C2)

	4	20100058078		2010-03-04	Branover, et al.	
	5	20110093733		2011-04-21	Kruglick	
	6	20070168151		2007-07-19	Kernahan, et al.	
	7	20060006166		2006-01-12	Chen, et al.	
	8	20100250856		2010-09-03	Owen, et al.	

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	1	I342498	TW		2011-05-21	Asustek Comp Inc.		☒
	2	I344793	TW		2011-07-01	IND TECH RES INST		☒

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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(2)P38407(2)

	6	20060117202		2006-06-11	Magklis, et al.	
	7	20070016817		2007-01-18	Albonesi, et al.	
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	10	20040098560		2004-05-02	Storvik, et al.	
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	14	20070106827		2007-05-10	Boatright, et al.	
	15	20080028240		2008-01-31	Arai, et al.	
	16	20090158061		2009-06-18	Schmitz, et al.	

Petitioner Mercedes Ex-1009, 0248

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	17	20010044909		2001-11-22	Oh, et al.	
	18	20050022038		2005-01-27	Kaushik, et al.	
	19	20070156992		2007-07-05	Jahagirdar	
	20	20050033881		2005-02-10	Yao	
	21	20040064752		2004-04-01	Kazachinsky, et al.	
	22	20040139356		2007-07-15	Ma	
	23	20070239398		2007-10-11	Song, et al.	
	24	20060069936		2006-03-30	Lint, et al.	
	25	20020194509		2002-12-19	Plante, et al.	
	26	20050132238		2005-06-16	Nanja	
	27	20070245163		2007-10-18	Lu, et al.	

Petitioner Mercedes Ex-1009, 0249

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492CQ(P38407CQ)

	28	20040268166		2004-12-30	Farkas, et al.	
	29	20090006871		2009-01-01	Liu, et al.	
	30	20100115309		2010-05-06	Carvalho, et al.	
	31	20100191997		2010-07-29	Dodeja, et al.	
	32	20100146513		2010-06-10	Song	
	33	20090235105		2009-09-17	Branover, et al.	
	34	20090172428		2009-07-02	Lee	
	35	20090172375		2009-07-02	Rotem, et al.	
	36	20090158067		2009-06-18	Bodas, et al.	
	37	20080250260		2008-10-09	Tomita	
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Petitioner Mercedes Ex-1009, 0250

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Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

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	1	20090292935		2009-11-26	Hallnor, et al.	
	2	20080316950		2008-12-25	Damnjanovic	
	3	20080168287		2008-07-10	Berry, et al.	

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	1	201009567	TW		2010-03-01	Hallnor, et al.		X

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2US (P38407C2)

	2	200917694	TW		2009-04-16	Damnjanovic		☒
	3	200839497	TW		2008-10-01	Berry, et al.		☒

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	1	Taiwan Intellectual Property Office, Office Action mailed November 2, 2015 in Taiwan Patent Application no. 103146274.	X

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	1	20110022865		2011-01-27	Gunther, et al.	
	2	20080005603		2008-01-03	Deep, et al.	
	3	20090070605		2009-03-12	Nijhawan, et al.	
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	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	4	20120116599		2012-05-10	Arndt, et al.	

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Petitioner Mercedes Ex-1009, 0254

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	Application Number	15138505
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	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492(C2)P38407(C2)

	1	20090313489		2009-12-17	Gunther, et al.	
	2	20100332927		2010-12-30	Kurts, et al.	
	3	20070234083		2007-10-04	Lee	
	4					
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	8	20050046400		2005-03-03	Rotem	
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	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
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	Examiner Name	
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	6	20070260895		2007-11-08	Aguilar, et al.	
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	Examiner Name	
	Attorney Docket Number	ITL.2492CQUS (P38407C2)

	2	20080005603		2008-01-03	Buch, et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407US2)

	4	20090271141		2009-10-29	Coskun, et al.	
	5	20080028778		2008-02-07	Millet	
	6	20120053897		2012-03-01	Naffziger	
	7	20050223258		2005-10-06	Watts	
	8	20050046400		2005-03-03	Rotem	
	9	20120110352		2012-05-03	Branover, et al.	
	10	20090235108		2009-09-17	Gold, et al.	
	11	20120066535		2012-03-15	Naffziger	
	12	20080077813		2008-03-27	Keller, et al.	
	13	20110283124		2011-11-17	Branover, et al.	
	14	20120173907		2012-07-05	Moses, et al.	

Petitioner Mercedes Ex-1009, 0258

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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	15	20130246825		2013-09-19	Shannon	

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Petitioner Mercedes Ex-1009, 0259

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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Application Number	15138505
Filing Date	2016-04-26
First Named Inventor	Avinash N. Ananthakrishnan
Art Unit	2184
Examiner Name	
Attorney Docket Number	ITL.2492C2US (P38407C2)

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	1	101403944	CN	A	2009-04-08	Gunther, et al.		☒
	2	101351759	CN	A	2009-01-21	ADVANCED MICRO DEVICES INC		☒
	3	101010655	CN	B	2010-05-26	INTEL CORP		☒

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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	1	201120628	TW		2011-06-16	Hansquine, et al.		☒
	2	201040701	TW		2010-11-16	Pedersen, et al.		☒

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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
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	1	EP 1 282 030	EP	A1	2003-05-02	Mitsubishi Kenki Kabushiki Kaisha		☐

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	1	U.S. Patent Application No. 12/889,121, "Providing Per Core Voltage and Frequency Control," filed September 23, 2010, by Pakaj Kumar.	☐
	2	SPEC-Power and Performance, Design Overview V1.10, Standard Performance Information Corp., October 21, 2008, 6 pages.	☐
	3	U.S. Patent Application No. 13/070,700, "Obtaining Power Profile Information With Low Overhead," filed March 24, 2011, by Robert Knight.	☐
	4	ANOOP IYER, et al., "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors," 2002, pages 1-11.	☐
	5	GREG SEMERARO, et al., "Hiding Synchronization Delays In A GALS Processor Microarchitecture," 2004, pages 1-13.	☐
	6	JOAN-MANUEL PARCERISA, et al., "Efficient Interconnects for Clustered Microarchitectures," 2002, pages 1-10.	☐

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	Application Number	15 138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	1	KR 10-2006-012846	KR		2006-12-14	LG Electronics Inc.		☐

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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Avinash N. Ananthakrishnan, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407(2))

	7	GRIGORIOS MAGKLIS, et al., "Profile-Based Dynamic Voltage and Frequency Scalling for a Multiple Clock Domain Microprocessor," 2003, pages 1-12.	☐
	8	GREG SEMERARO, et al., "Dynamic Frequency and Voltage Control for a Multiple Clock Domain Architecture," 2002, pages 1-12.	☐
	9	GREG SEMERARO, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," 2002, pages 29-40.	☐
	10	DIANA MARCULESCU, "Application Adaptive Energy Efficient Clustered Architectures," 2004, pages 344-349.	☐
	11	L. BENINI, et al., "System-Level Dynamic Power Management," 1999, pages 23-31.	☐
	12	RAVINDRA JEJURIKAR, et al., "Leakage Aware Dynamic Voltage Scaling For Real-Time Embedded Systems," 2004, pages 275-280.	☐
	13	RAVINDRA JEJURIKAR, et al., "Dynamic Slack Reclamation With Procrastination Scheduling In Real-Time Embedded Systems," 2005, pages 13-17.	☐
	14	R. TODLING, et al., "Some Strategies For Kalman Filtering and Smoothing," 1996, pages 1-21.	☐
	15	R.E. KALMAN, "A New Approach To Linear Filtering and Prediction Problems," 1960, pages 1-12.	☐
	16	INTEL TECHNOLOGY JOURNAL, "Power and Thermal Management in the Intel Core Duo Processor," May 15, 2006, pages 109-122.	☐
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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	AVINASH N. ANANTHAKRISHNAN, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2(P38407C2)

	1	U.S. Patent Application Serial No. 13/285,414, filed October 31, 2011, entitled "CONTROLLING A TURBO MODE FREQUENCY OF A PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2494)	☐
	2	U.S. Patent Application Serial No. 13/225,677, filed September 6, 2011, entitled "DYNAMICALLY ALLOCATING A POWER BUDGET OVER MULTIPLE DOMAINS OF A PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2495)	☐
	3	U.S. Patent Application Serial No. 13/247,580, filed September 28, 2011, entitled "CONTROLLING TEMPERATURE OF MULTIPLE DOMAINS OF A MULTI-DOMAIN PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2496)	☐
	4	U.S. Patent Application Serial No. 13/285,465, filed October 31, 2011, entitled "DYNAMICALLY CONTROLLING CACHE SIZE TO MAXIMIZE ENERGY EFFICIENCY," by AVINASH N. ANANTHAKRISHNAN, et al. (2497)	☐
	5	U.S. Patent Application Serial No. 13/282,947, filed October 27, 2011, entitled "CONTROLLING OPERATING FREQUENCY OF A CORE DOMAIN VIA A NON-CORE DOMAIN OF A MULTI-DOMAIN PROCESSOR," by AVINASH N. ANANTHAKRISHNAN, et al. (2493)	☐

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	Application Number	15138505
	Filing Date	2016-04-26
	First Named Inventor	Ananthakrishnan, et al.
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	ITL.2492C2US (P38407C2)

	1	U.S. Patent and Trademark Office, Office Action mailed July 31, 2014, in U.S. application no. 13/247,564. (2491)	☐
	2	U.S. Patent and Trademark Office, Office Action mailed January 16, 2014, with Reply filed April 9, 2014, in U.S. application no. 13/247,564. (2491)	☐
	3	U.S. Patent and Trademark Office, Office Action mailed June 6, 2014, with Reply filed September 4, 2014, in U.S. application no. 13/282,947. (2493)	☐
	4	U.S. Patent and Trademark Office, Office Action mailed May 16, 2014, with Reply filed August 12, 2014, in U.S. application no. 13/285,414. (2494)	☐
	5	U.S. Patent and Trademark Office, Final Office Action mailed May 14, 2014, with Request for Continued Examination filed August 13, 2014, in U.S. application no. 13/247,580. (2496)	☐
	6	U.S. Patent and Trademark Office, Office Action mailed August 18, 2014, in U.S. application no. 13/285,465. (2497)	☐

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	1	Taiwan Patent Office, Office action mailed August 21, 2014, in Taiwan application no.101135884.	☐
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	1	DAVID L. HILL, et al., "The Uncore: A Modular Approach To Feeding The High-Performance Cores," Intel Technology Journal, 2010, Vol 14, Issue 3, pages 30-49.	☐
	2	INTERNATIONAL SEARCHING AUTHORITY, "Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority," mailed March 28, 2013, in International application no. PCT/US2012/057655.	☐

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	First Named Inventor	Avinash N. Ananthakrishnan
	Art Unit	
	Examiner Name	
	Attorney Docket Number	ITL.2492C2US (P38407C2)

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2016-07-08
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Application Number:	15138505
Filing Date:	26-Apr-2016
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Filer:	Mark J. Rozman/Stephanie Petreas
Attorney Docket Number:	ITL.2492C2US (P38407C2)

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Utility Examination Fee	1311	1	720	720
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Claims:				
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EFS ID:	26291508
Application Number:	15138505
International Application Number:	
Confirmation Number:	3621
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
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Attorney Docket Number:	ITL.2492C2US (P38407C2)
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Application Type:	Utility under 35 USC 111(a)

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Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	ITL2492C1USIDSToFile.pdf	3473990 17228b74061c1337056fa1ae755620ee99c89ea8	no	34
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Fee Worksheet (SB06)	fee-info.pdf	37472 1ba4e93603fc9b37f7ec5e34900a3ad5c53378c7	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3579650		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/138,505	04/26/2016	Avinash N. Ananthakrishnan	ITL.2492C2US (P38407C2)

CONFIRMATION NO. 3621

47795
TROP, PRUNER & HU, P.C.
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

FORMALITIES LETTER

OC000000082790450

Date Mailed: 05/11/2016

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **280** basic filing fee.
- $ **140** surcharge.
- $ **600** search fee.
- $ **720** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1740** TOTAL FEE BALANCE DUE.

Petitioner Mercedes Ex-1009, 0274

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/esalfonso/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/138,505

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/138,505	04/26/2016	2184	0.00	ITL.2492C2US (P38407C2)	1	1

CONFIRMATION NO. 3621

FILING RECEIPT

47795
TROP, PRUNER & HU, P.C.
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

OC000000082790449

Date Mailed: 05/11/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Avinash N. Ananthakrishnan, Portland, OR;
Inder M. Sodhi, Folsom, CA;
Efraim Rotem, Haifa, ISRAEL;
Doron Rajwan, Rishon Le-Zion, ISRAEL;
Eliezer Weissmann, Haifa, ISRAEL;
Ryan Wells, Folsom, CA;

Applicant(s)

Intel Corporation, Santa Clara, CA;

Power of Attorney: The patent practitioners associated with Customer Number 47795

Domestic Priority data as claimed by applicant

This application is a CON of 14/451,807 08/05/2014
which is a CON of 13/282,896 10/27/2011 PAT 8832478

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Petitioner Mercedes Ex-1009, 0277

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/09/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/138,505**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Enabling A Non-Core Domain To Control Memory Bandwidth

Preliminary Class

710

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Petitioner Mercedes Ex-1009, 0280

PTO/AIA/15 (07-12)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	ITL.2492C2US (P38407C2)
First Inventor	Avinash N. Ananthakrishnan, et al.
Title	
Express Mail Label No.	Filed Via EFS

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form.** (PTO/SB/17 or equivalent)
2. ☐ **Applicant claims small entity status.** See 37 CFR 1.27.
3. ☑ **Specification.** [*Total Pages* 16] Both the claims and abstract must start on a new page *(For information on the preferred arrangement, see MPEP § 608.01(a))*
4. ☑ **Drawing(s).** (*35 U.S.C. 113*) [*Total Sheets* 5]
5. **Inventor's Oath or Declaration.** [*Total Sheets* 6] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☐ Newly executed (original or copy)
   b. ☑ A copy from a prior application (37 CFR 1.63(d))
6. ☑ **Application Data Sheet.** **See Note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
7. ☐ **CD-ROM or CD-R.** in duplicate, large table or Computer Program *(Appendix)*
   ☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission.** *(if applicable, items a. – c. are required)*
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents**
P.O. Box 1450
Alexandria VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers.** (cover sheet & document(s))
   Name of Assignee_____
10. ☑ **37 CFR 3.73(c) Statement.** ☑ **Power of Attorney.** *(when there is an assignee)*
11. ☐ **English Translation Document.** *(if applicable)*
12. ☐ **Information Disclosure Statement.** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
13. ☐ **Preliminary Amendment.**
14. ☐ **Return Receipt Postcard.** *(MPEP § 503) (Should be specifically itemized)*
15. ☐ **Certified Copy of Priority Document(s).** *(if foreign priority is claimed)*
16. ☐ **Nonpublication Request.** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
17. ☐ **Other:**_____

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

18. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 47795 ***OR*** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Mark J. Rozman/	Date	2016-04-26
Name (Print/Type)	Mark J. Rozman	Registration No. (Attorney/Agent)	42,117

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ITL.2492C2US (P38407C2)
	Application Number	
Title of Invention	Enabling A Non-Core Domain To Control Memory Bandwidth	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Avinash	N.	Ananthakrishnan	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Portland	OR	US

Mailing Address of Inventor:

Address 1	8545 NW Ryan Street
Address 2	
City	Portland
State/Province	OR
Postal Code	97229
Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Inder	M.	Sodhi	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Folsom	CA	US

Mailing Address of Inventor:

Address 1	963 Sterling Circle
Address 2	
City	Folsom
State/Province	CA
Postal Code	95630
Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Efraim		Rotem	

Residence Information (Select One) ○ US Residency ● Non US Residency Active US Military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ITL.2492C2US (P38407C2)
	Application Number	
Title of Invention	Enabling A Non-Core Domain To Control Memory Bandwidth	

City	Haifa	Country of Residence [i]	IL

Mailing Address of Inventor:

Address 1	8 Vizo Street		
Address 2			
City	Haifa	State/Province	HA
Postal Code	34400	Country [i]	IL

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Doron		Rajwan	

Residence Information (Select One) ○ US Residency ◉ Non US Residency Active US Military Service

City	Rishon Le-Zion	Country of Residence [i]	IL

Mailing Address of Inventor:

Address 1	13 Odem Street		
Address 2			
City	Rishon Le-Zion	State/Province	M
Postal Code	00000	Country [i]	IL

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Eliezer		Weissmann	

Residence Information (Select One) ○ US Residency ◉ Non US Residency Active US Military Service

City	Haifa	Country of Residence [i]	IL

Mailing Address of Inventor:

Address 1	Albert Switcher 10		
Address 2			
City	Haifa	State/Province	HA
Postal Code	34995	Country [i]	US

Inventor 6 Remove

Legal Name

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ITL.2492C2US (P38407C2)
	Application Number	
Title of Invention	Enabling A Non-Core Domain To Control Memory Bandwidth	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ryan		Wells	

Residence Information (Select One) (•) US Residency ( ) Non US Residency Active US Military Service

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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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Application Information:

Title of the Invention	Enabling A Non-Core Domain To Control Memory Bandwidth		
Attorney Docket Number	ITL.2492C2US (P38407C2)	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	47795		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	14451807	2014-08-05

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14451807	Continuation of	13282896	2011-10-27	8832478	2014-09-09

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Foreign Priority Information:

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This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

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The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

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Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

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Country	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			

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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

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This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Mark J. Rozman/			Date (YYYY-MM-DD)	2016-04-26
First Name	Mark	Last Name	Rozman	Registration Number	42117

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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: **ENABLING A NON-CORE DOMAIN TO CONTROL MEMORY BANDWIDTH**

INVENTORS: **AVINASH N. ANANTHAKRISHNAN; INDER M. SODHI; EFRAIM ROTEM; DORON RAJWAN; ELIEZER WEISSMANN; RYAN WELLS**

Filed Via EFS

Date: April 26, 2016

Prepared by: Trop, Pruner & Hu, P.C., Mark J. Rozman
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ENABLING A NON-CORE DOMAIN TO CONTROL MEMORY BANDWIDTH

[0001] This application is a continuation of United States Patent Application Serial No. 14/451,807, filed August 5, 2014, which is a continuation of U.S. Patent Application Serial No. 13/282,896, filed October 27, 2011, now U.S. Patent No. 8,832,478, issued September 9, 2014, the content of which is hereby incorporated by reference.

Background

[0002] As technology advances in the semiconductor field, devices such as processors incorporate ever-increasing amounts of circuitry. Over time, processor designs have evolved from a collection of independent integrated circuits (ICs), to a single integrated circuit, to multicore processors that include multiple processor cores within a single IC package. As time goes on, ever greater numbers of cores and related circuitry are being incorporated into processors and other semiconductors.

[0003] Multicore processors are being extended to include additional functionality by incorporation of other functional units within the processor. One issue that arises is that the different circuitry can have differing needs with regard to frequency of operation based on their workloads. However, suitable mechanisms to ensure that these different units operate at an appropriate frequency are not available. Further, the different units can have a shared interface to access a shared cache or system memory. Typically, this interface to the cache and system memory is either operated at a constant fixed frequency or is tied to the frequency of the processor cores.

Brief Description of the Drawings

[0004] FIG. 1 is high level flow diagram of a method in accordance with an embodiment of the present invention.

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[0005] FIG. 2 is a flow diagram of a method for updating a mapping table in accordance with an embodiment of the present invention.

[0006] FIG. 3 is a block diagram of a processor in accordance with an embodiment of the present invention.

[0007] FIG. 4 is a block diagram of a multi-domain processor in accordance with another embodiment of the present invention.

[0008] FIG. 5 is a block diagram of a system in accordance with one embodiment of the present invention.

Detailed Description

[0009] A multi-domain processor including multiple domains such as a core domain, a non-core domain and a system agent domain can enable the non-core domain to control memory bandwidth available to it. As will be described herein, in various embodiments this memory bandwidth can be realized by an interconnect structure, namely a ring interconnect that is part of the core domain. However, although described herein as being part of the core domain, understand that in other implementations a multi-domain processor can include an independent interconnect domain. By allowing a non-core domain to have control over an interconnect frequency and thus bandwidth, memory bandwidth used by non-core domain can be more efficient.

[0010] As will be discussed further below, in a multi-domain processor, a non-core domain can be coupled to a shared memory such as a last level cache and system main memory via an interconnect structure. By default, the interconnect frequency can be at the maximum frequency of all active cores of the core domain. If however the processor is power and/or thermally limited, the interconnect frequency drops along with the cores' frequency. Since the interconnect frequency impacts the effective memory bandwidth available to the non-core domain, the interconnect frequency has a significant impact on non-core domain performance.

However, higher interconnect frequency comes at a cost of higher power consumption in the core domain. Embodiments may use a mailbox interface to dynamically optimize power/performance for a workload executing on a non-core domain.

[0011] In the particular implementation described herein, the non-core domain can be a graphics domain that includes one or more graphics engines. By enabling this domain to control its memory bandwidth via an interconnect to a memory hierarchy, performance of this domain can be improved, since particularly for a graphics workload performance is a strong function of bandwidth available to it. Although different manners of providing this control to the graphics domain are possible, embodiments described herein enable this ability by a mechanism that maps non-core domain frequency to a corresponding interconnect frequency. This mapping can be maintained in a table, which may be located in a power controller of the processor such as a power control unit (PCU). As will be described herein, this table can be configured during initialization by the non-core domain and furthermore, the table can be dynamically updated based on a workload being executed by the non-core domain. In this way, a close association between the workload being handled in the non-core domain and the bandwidth of the path to the memory subsystem can be achieved.

[0012] Referring now to FIG. 1, shown is high level flow diagram of a method in accordance with an embodiment of the present invention. As shown in FIG 1, method 100 can be performed by logic of the PCU, which can be the owner of the mapping table that associates non-core domain operating frequencies and corresponding interconnect operating frequencies. Namely, the table can map non-core domain frequency to a minimum interconnect frequency. However, the table data and initiation of table configuration and updates may be from another entity, such as a driver for the non-core domain. As seen, method 100 begins by receiving a configuration message from the non-core domain to configure a mapping table (block 110). This message may be received from a core of the core domain, as this driver may execute on a core. The receipt of information can be by way of a mailbox interface. This interface thus

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provides a mechanism for the driver to exchange parameters with the PCU. In one embodiment, a dedicated bus can be provided for communication between the driver and the PCU. In turn, the PCU can include a temporary storage area to store the incoming communications, and provide an interface to a mapping table in accordance with an embodiment of the present invention. In one embodiment this mailbox interface may enable the communication of table entries in serial fashion to thus populate the mapping table, which can be stored in a lookup table such as present in a memory of the PCU, e.g., random access memory (RAM). Next, at block 120 the mapping table can be configured using the mapping information received from the non-core domain. At this point the table entries have been written, and the PCU is now in position to control interconnect frequency based on the frequency at which the non-core domain is operating.

[0013] Accordingly, during normal operation control passes to block 130 where the interconnect frequency can be controlled using the mapping table. More specifically, responsive to the non-core domain operating frequency, which the PCU itself configures, a corresponding interconnect frequency is also configured. For example, when a graphics frequency changes, the PCU can use the updated graphics frequency value as an index into the table to access a table entry that includes a corresponding interconnect frequency for that graphics domain frequency. Accordingly, the PCU can take appropriate action to cause that interconnect frequency to be provided. As an example, the interconnect frequency can be changed by the same mechanism used to change core domain frequency, namely requesting core and non-core domains to pause generating cache bound or memory bound requests, draining the interconnect domain of all outstanding requests, effecting a frequency change and enabling the core and non-core domains to resume generating cache or memory traffic.

[0014] In the particular implementation described herein, note that the interconnect structure can be within the core domain and thus the core domain frequency itself is controlled. Note also that the frequency thus read from the table is a minimum frequency at which the

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interconnect is to operate and accordingly if the core domain is operating at a higher frequency than this value, the update to the interconnect frequency does not occur. And, when the processor is power/thermally limited, this frequency is not guaranteed. Further understand that in embodiments in which the interconnect frequency is also the operating frequency of the core domain, the PCU may select a maximum of the interconnect frequency from the appropriate mapping table entry and the core operating frequency requested by the operating system. Although shown at this high level in the embodiment of FIG. 1, understand the scope of the present invention is not limited in this regard.

[0015] As discussed above, the actual values stored in the mapping table can originate with the driver for the non-core domain. In one embodiment, this driver may include different tables, each associated with a particular type of workload to be executed on the non-core domain. These tables may include a base table that can be written to the mapping table in the PCU upon system initialization. However, due to changes in the workload, the table can be updated dynamically. This update may be to one or more values the table, or a complete update of the table to a new set of values can occur. Note that these different table configurations can be stored in connection with the driver, and each can be based on characterization testing of different workloads executing on the non-core domain. In a graphics domain example, different workload types can be different graphics resolution modes, 3D mode, multiple monitor configurations, and so forth. Also, different table entries may be provided depending on whether a gaming workload is performed (e.g., increasing interconnect frequency) or whether video playback on a portable device is executing (e.g., decreasing interconnect frequency) to reduce battery consumption.

[0016] Referring now to FIG. 2, shown is a flow diagram of a method for updating a mapping table in accordance with an embodiment of the present invention. This method can be performed at least in part by a non-core domain driver or other software/firmware/logic that can be used to cause a mapping table to be set up for use in connection with interconnect frequency

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control. In the implementation described herein where the non-core domain is a graphics domain, the driver for the graphics domain may operate on a core of the core domain. As shown in FIG. 2, more generally method 200 may be performed by a driver for the non-core domain, along with logic of the PCU. In general, the flow of method 200 can be performing at a predetermined interval, e.g., approximately every 10 to 500 milliseconds (ms).

[0017] As seen, method 200 begins by determining whether a characteristic of a workload executing on the non-core domain has changed (diamond 210). If not, the remainder of the flow does not proceed for this iteration. Note that the analysis of the workload change may be based on a video mode being executed, e.g., video resolution, the presence of multiple monitors, a 3D mode, a type of media being played back, or so forth.

[0018] If instead it is determined at diamond 210 that the workload characteristic has changed, control passes to block 220. There, a determination may be made as to the memory boundedness of the workload (block 220). Although the scope of the present invention is not limited in this regard, in one embodiment the determination of memory boundedness can be based on statistics gathered for a given time interval as to the status of certain operations of the workload. For example, in one embodiment memory boundedness can be determined based on a number of misses from low level caches (e.g., of the non-core domain) that require access to a last level cache (LLC) or system memory. In other implementations, memory boundedness can be determined as a ratio with regard to the residency of outstanding loads from memory of instructions in an order buffer such as a memory order buffer (MOB) as compared to time spent in an active (e.g., a C0) state. Or the boundedness can be determined by a ratio of non-core domain read and write transactions on the memory interconnect to the total transactions. Memory boundedness can also be inferred by analyzing the number of memory read/write or commands being sent out to each of the memory modules.

[0019] This determination of memory boundedness can thus take some amount of time to obtain. Upon its completion, the driver can send an update for the mapping table to the PCU

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(block 230). In one embodiment, the driver can use the mailbox interface to update the mapping table. As discussed, this update can be to one or more (up to all) entries of the mapping table. For example, assume that the workload is memory bounded, the driver can cause updated values to be sent to the PCU to thus enable the table to be updated with increased interconnect frequency values for the same corresponding non-core domain frequency values. Accordingly, control passes to block 240, where the PCU can then use this updated mapping table to select an appropriate interconnect frequency for the corresponding non-core domain frequency. While described with this particular implementation in the embodiment of FIG. 2, understand the scope of the present invention is not limited in this regard.

[0020] As seen in the example of Table 1, the mapping table can include a plurality of entries each having two parameters namely non-core domain frequency and corresponding minimum interconnect frequency, which in the Table 1 embodiment may be in terms of megahertz (MHz). However in other embodiments the table can store entries that associate frequencies by ratios, offsets or so forth. In an embodiment, the non-core domain driver during run time can use the mailbox interface to set up this table in PCU memory. This configuration may be via specification of pairwise entries to identify a target interconnect frequency for a corresponding non-core domain frequency. Then after configuration, the PCU can access the table based on a frequency at which the non-core domain is operating to obtain the corresponding target interconnect frequency, and in turn control the core domain to operate at this frequency (assuming it is higher than the current operating frequency of the core domain). Note that when the core domain is operating at an increased frequency due to the non-core domain control, and the non-core domain thereafter enters into a sleep state, the PCU can update the core domain frequency to a lower, OS-requested level to reduce power consumption.

Table 1

Table Entry	Non-Core Frequency	Minimum Interconnect Frequency

Petitioner Mercedes Ex-1009, 0300

1	300	800
2	350	800
3	400	800
4	450	800
5	500	800
6	550	800
7	600	800
8	650	1500
9	700	1500
11	750	1500
12	800	1500
13	850	1500
14	900	1800
15	950	1900
16	1000	2000
17	1050	2100
18	1100	2200
19	1150	2300
20	1200	2400
21	1250	2500
22	1300	2600

[0021] Referring now to FIG. 3, shown is a block diagram of a processor in accordance with an embodiment of the present invention. As shown in FIG. 3, processor 300 may be a multicore processor including a plurality of cores $310_a - 310_n$. In one embodiment, each such

Petitioner Mercedes Ex-1009, 0301

core may be of an independent power domain and can be configured to operate at an independent voltage and/or frequency, and to enter turbo mode when available headroom exists. The various cores may be coupled via an interconnect 315 to a system agent or uncore 320 that includes various components. As seen, the uncore 320 may include a shared cache 330 which may be a last level cache. In addition, the uncore may include an integrated memory controller 340, various interfaces 350 and a power control unit 355.

[0022] In various embodiments, power control unit 355 may include a frequency control logic 359, which may be a logic to perform dynamic control of interconnect frequency responsive to a request of a given domain (which can be one of the core domains or a non-core domain). In the embodiment of FIG. 3, assuming that each core is of an independent power domain, logic 359 can control an interconnect frequency (where the interconnect can be of one of core domains) responsive to a request of a given domain, e.g., with reference to a mapping table 357. In some embodiments, each domain can have at least one mapping table with entries to associate a given domain frequency and a corresponding minimum interconnect frequency. In turn, each such domain can write its mapping table to mapping table 357, which may thus include multiple tables each associated with a given domain. Although shown at this location in the embodiment of FIG. 3, understand that the scope of the present invention is not limited in this regard and the storage of this information can be in other locations, such as configuration registers, non-volatile storage or the like.

[0023] With further reference to FIG. 3, processor 300 may communicate with a system memory 360, e.g., via a memory bus. In addition, by interfaces 350, connection can be made to various off-chip components such as peripheral devices, mass storage and so forth. While shown with this particular implementation in the embodiment of FIG. 3, the scope of the present invention is not limited in this regard.

[0024] Referring now to FIG. 4, shown is a block diagram of a multi-domain processor in accordance with another embodiment of the present invention. As shown in the embodiment of

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FIG. 4, processor 400 includes multiple domains. Specifically, a core domain 410 can include a plurality of cores 410_0–410n, a graphics domain 420 can include one or more graphics engines, and a system agent domain 450 may further be present. In various embodiments, system agent domain 450 may execute at a fixed frequency and may remain powered on at all times to handle power control events and power management such that domains 410 and 420 can be controlled to dynamically enter into and exit low power states. Each of domains 410 and 420 may operate at different voltage and/or power.

[0025] Note that while only shown with three domains, understand the scope of the present invention is not limited in this regard and additional domains can be present in other embodiments. For example, multiple core domains may be present each including at least one core.

[0026] In general, each core 410 may further include low level caches in addition to various execution units and additional processing elements. In turn, the various cores may be coupled to each other and to a shared cache memory formed of a plurality of units of a last level cache (LLC) 440_0 – 440_n. In various embodiments, LLC 450 may be shared amongst the cores and the graphics engine, as well as various media processing circuitry. As seen, a ring interconnect 430 thus couples the cores together, and provides interconnection between the cores, graphics domain 420 and system agent circuitry 450. In one embodiment, interconnect 430 can be part of the core domain. However in other embodiments the ring interconnect can be of its own domain. In any event, the interconnect frequency can be controlled via system agent circuitry as described herein.

[0027] In the embodiment of FIG. 4, system agent domain 450 may include display controller 452 which may provide control of and an interface to an associated display. As further seen, system agent domain 450 may include a power control unit 455 which can include a frequency control logic 459 in accordance with an embodiment of the present invention to dynamically update the frequency of interconnect 430. In various embodiments, this logic may

Petitioner Mercedes Ex-1009, 0303

execute at least part of the algorithms shown in FIGS. 1 and 2 to dynamically control interconnect frequency. To this end, PCU 455 can be coupled to a mapping table 457, which may be a table configured as above to provide for association between a domain's frequency and a corresponding minimum interconnect frequency. Although the above embodiment of Table 1 shows table entries associating non-core domain frequency and minimum interconnect frequency, understand that multiple mapping tables may be present, each associated with a given domain of the processor and a corresponding minimum interconnect frequency.

[0028] To enable configuration of such table, which can be in a RAM of system agent domain 450, a mailbox interface 456 can be present. In general, interface 456 can include a first register 456a and a second register 456b. Such registers provide an interface for handshake-based communications between the PCU and other domains. In one embodiment, first register 456a can include a flag field to store a flag, a command field to store a command, and an address field to store an address, e.g., of an entry within mapping table 457. Second register 456b may be a data storage register. In one embodiment, graphics domain 420 can write an entry into a corresponding location within mapping table 457 by setting the flag field of first register 456a high, providing a write command for the command field, and providing an address corresponding to the entry in the table to be written to the address field, and further providing the data to be written to second register 456b. In turn, responsive to the active flag field, PCU 455 can thus write the data to the corresponding entry and reset the flag field to indicate to the graphics domain that it can write the next entry. While described with this particular protocol in the embodiment of FIG. 4, understand the scope of the present invention is not limited in this regard.

[0029] As further seen in FIG. 4, processor 400 can further include an integrated memory controller (IMC) 470 that can provide for an interface to a system memory, such as a dynamic random access memory (DRAM). Multiple interfaces 480_0 – 480_n may be present to enable interconnection between the processor and other circuitry. For example, in one embodiment at

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least one direct media interface (DMI) interface may be provided as well as one or more Peripheral Component Interconnect Express (PCI Express™ (PCIe™)) interfaces. Still further, to provide for communications between other agents such as additional processors or other circuitry, one or more interfaces in accordance with an Intel® Quick Path Interconnect (QPI) protocol may also be provided. Although shown at this high level in the embodiment of FIG. 4, understand the scope of the present invention is not limited in this regard.

[0030] Embodiments may be implemented in many different system types. Referring now to FIG. 5, shown is a block diagram of a system in accordance with an embodiment of the present invention. As shown in FIG. 5, multiprocessor system 500 is a point-to-point interconnect system, and includes a first processor 570 and a second processor 580 coupled via a point-to-point interconnect 550. As shown in FIG. 5, each of processors 570 and 580 may be multicore processors, including first and second processor cores (i.e., processor cores 574a and 574b and processor cores 584a and 584b), although potentially many more cores may be present in the processors. Each of the processors can include a PCU or other logic to perform dynamic control of an on-chip memory interconnect based on a non-core domain request, as described herein.

[0031] Still referring to FIG. 5, first processor 570 further includes a memory controller hub (MCH) 572 and point-to-point (P-P) interfaces 576 and 578. Similarly, second processor 580 includes a MCH 582 and P-P interfaces 586 and 588. As shown in FIG. 5, MCH's 572 and 582 couple the processors to respective memories, namely a memory 532 and a memory 534, which may be portions of system memory (e.g., DRAM) locally attached to the respective processors. First processor 570 and second processor 580 may be coupled to a chipset 590 via P-P interconnects 552 and 554, respectively. As shown in FIG. 5, chipset 590 includes P-P interfaces 594 and 598.

[0032] Furthermore, chipset 590 includes an interface 592 to couple chipset 590 with a high performance graphics engine 538, by a P-P interconnect 539. In turn, chipset 590 may be

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coupled to a first bus 516 via an interface 596. As shown in FIG. 5, various input/output (I/O) devices 514 may be coupled to first bus 516, along with a bus bridge 518 which couples first bus 516 to a second bus 520. Various devices may be coupled to second bus 520 including, for example, a keyboard/mouse 522, communication devices 526 and a data storage unit 528 such as a disk drive or other mass storage device which may include code 530, in one embodiment. Further, an audio I/O 524 may be coupled to second bus 520. Embodiments can be incorporated into other types of systems including mobile devices such as a smart cellular telephone, tablet computer, netbook, ultrabook, or so forth.

[0033] Embodiments may be implemented in code and may be stored on a non-transitory storage medium having stored thereon instructions which can be used to program a system to perform the instructions. The storage medium may include, but is not limited to, any type of disk including floppy disks, optical disks, solid state drives (SSDs), compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[0034] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

Petitioner Mercedes Ex-1009, 0306

What is claimed is:

1. A processor comprising:

a first domain including at least one core to execute instructions;

a second domain including at least one execution unit to execute instructions transparent to an operating system (OS), wherein a driver of the second domain is to control execution on the second domain;

an interconnect to interconnect the first domain and the second domain to a memory coupled to the processor; and

a power controller to control a frequency of the interconnect based on memory boundedness of a workload executed on the second domain.

Petitioner Mercedes Ex-1009, 0307

Abstract of the Disclosure

In one embodiment, the present invention includes a processor having multiple domains including at least a core domain and a non-core domain that is transparent to an operating system (OS). The non-core domain can be controlled by a driver. In turn, the processor further includes a memory interconnect to interconnect the core domain and the non-core domain to a memory coupled to the processor. Still further, a power controller, which may be within the processor, can control a frequency of the memory interconnect based on memory boundedness of a workload being executed on the non-core domain. Other embodiments are described and claimed.

Petitioner Mercedes Ex-1009, 0308

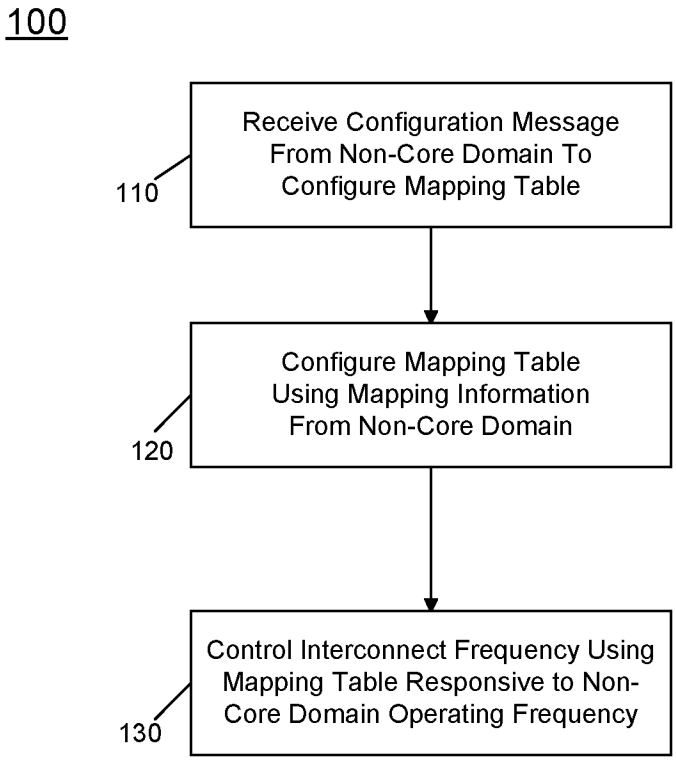

100
Receive Configuration Message From Non-Core Domain To Configure Mapping Table
110
Configure Mapping Table Using Mapping Information From Non-Core Domain
120
Control Interconnect Frequency Using Mapping Table Responsive to Non-Core Domain Operating Frequency
130

FIG. 1

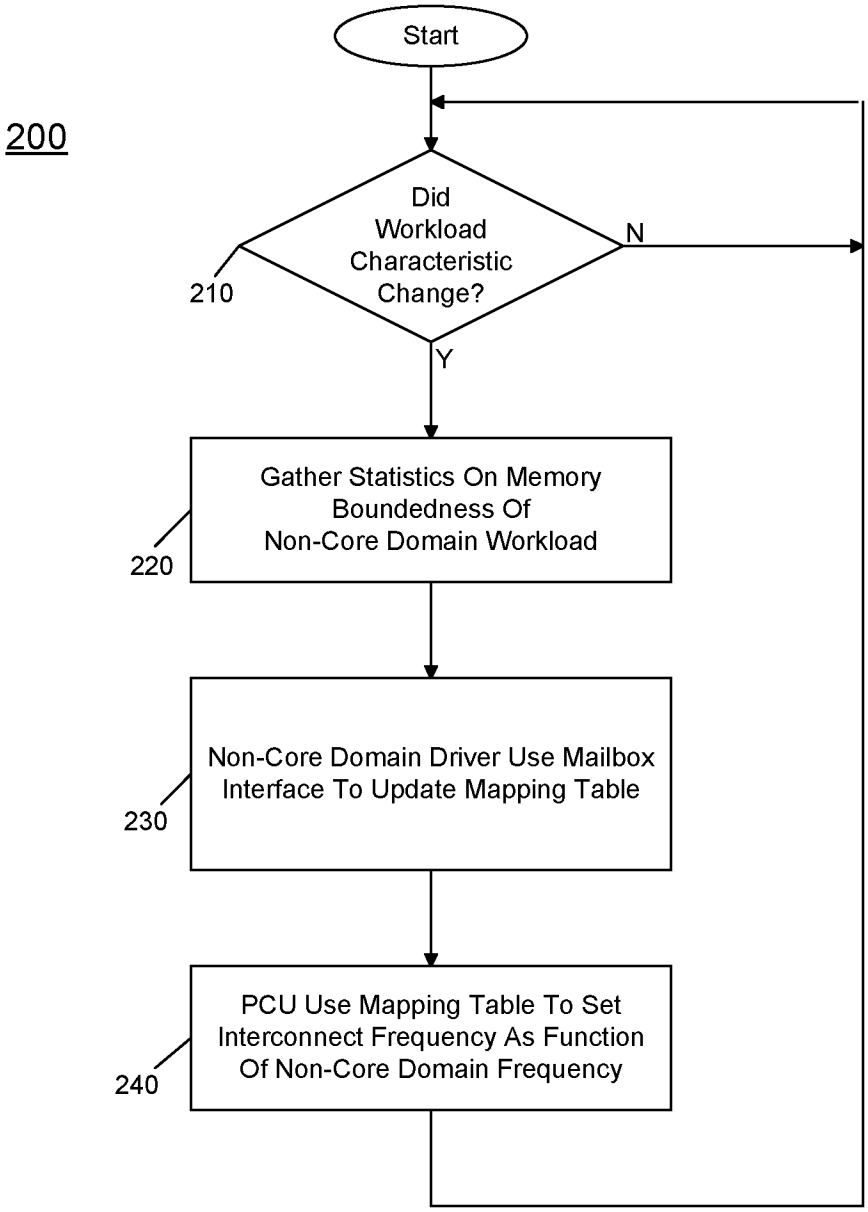

200
Start
Did Workload Characteristic Change?
210
N
Y
Gather Statistics On Memory Boundedness Of Non-Core Domain Workload
220
Non-Core Domain Driver Use Mailbox Interface To Update Mapping Table
230
PCU Use Mapping Table To Set Interconnect Frequency As Function Of Non-Core Domain Frequency
240

FIG. 2

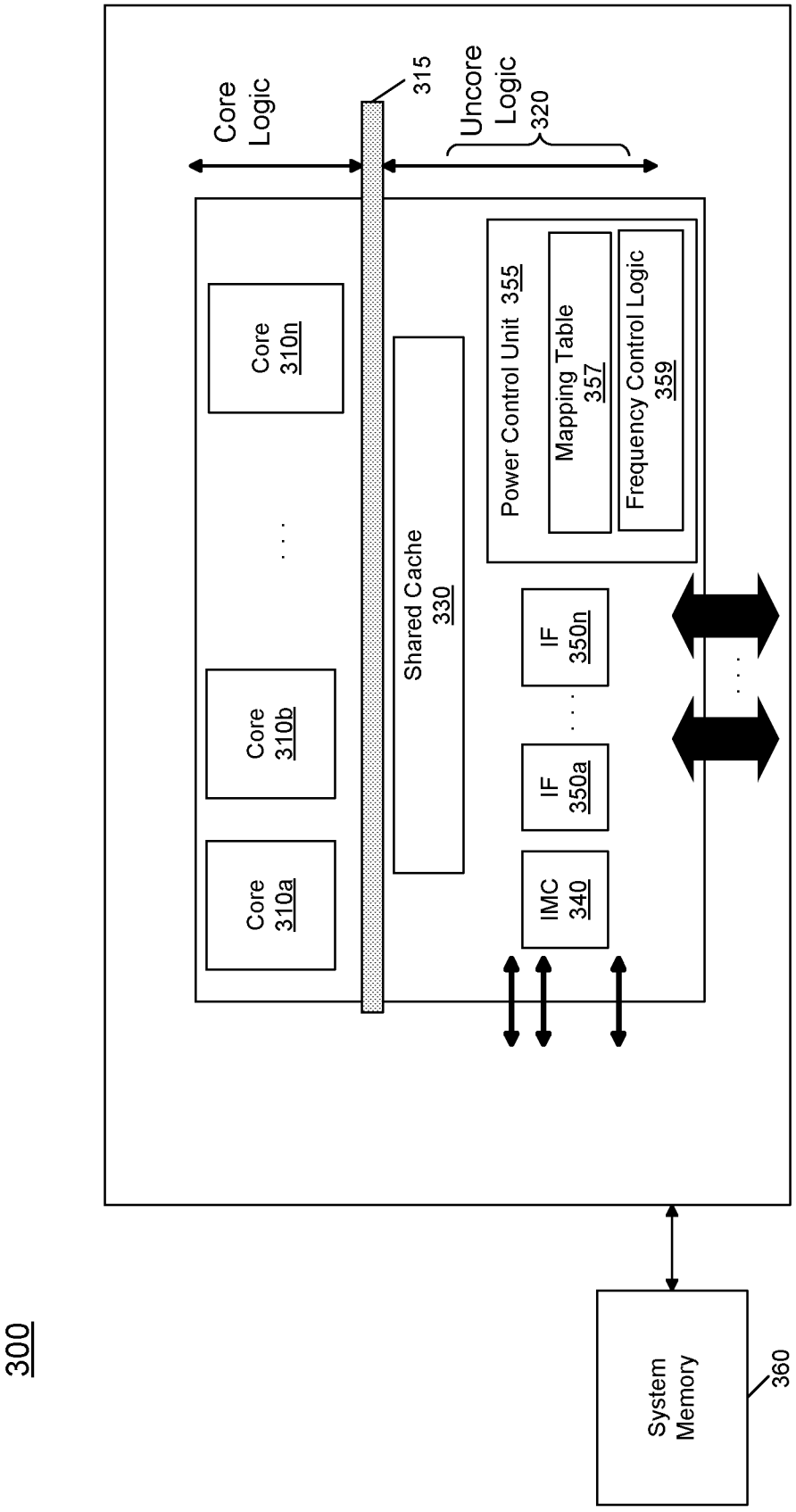

300
Core Logic
315
Uncore Logic 320
Core 310n
Core 310b
Core 310a
Shared Cache 330
Power Control Unit 355
Mapping Table 357
Frequency Control Logic 359
IF 350n
IF 350a
IMC 340
System Memory
360

FIG. 3

400

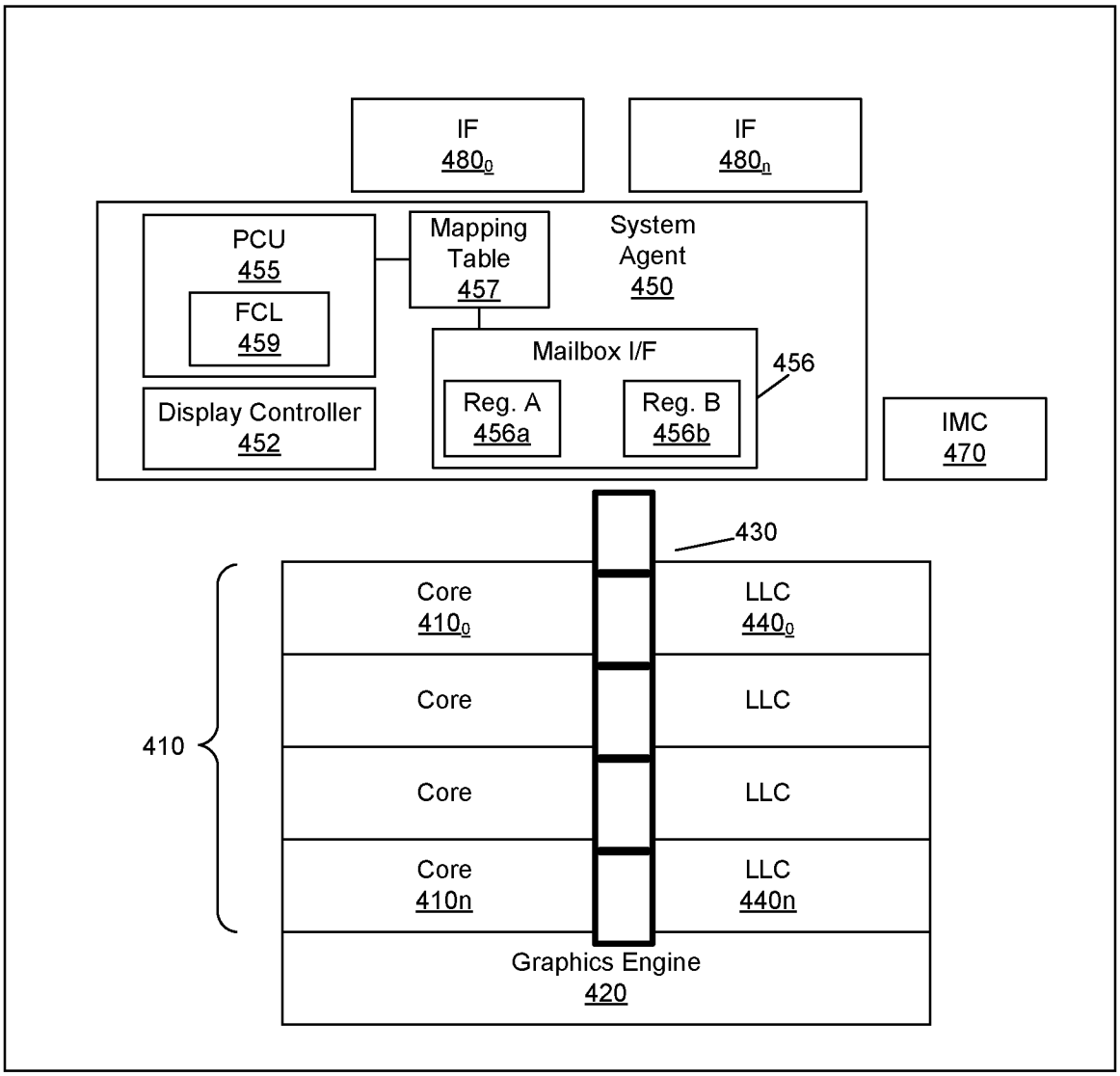

IF
480$_0$
IF
480$_n$
PCU
455
FCL
459
Mapping
Table
457
System
Agent
450
Mailbox I/F
456
Reg. A
456a
Reg. B
456b
Display Controller
452
IMC
470
430
Core
410$_0$
LLC
440$_0$
Core
LLC
Core
LLC
Core
410n
LLC
440n
410
Graphics Engine
420

FIG. 4

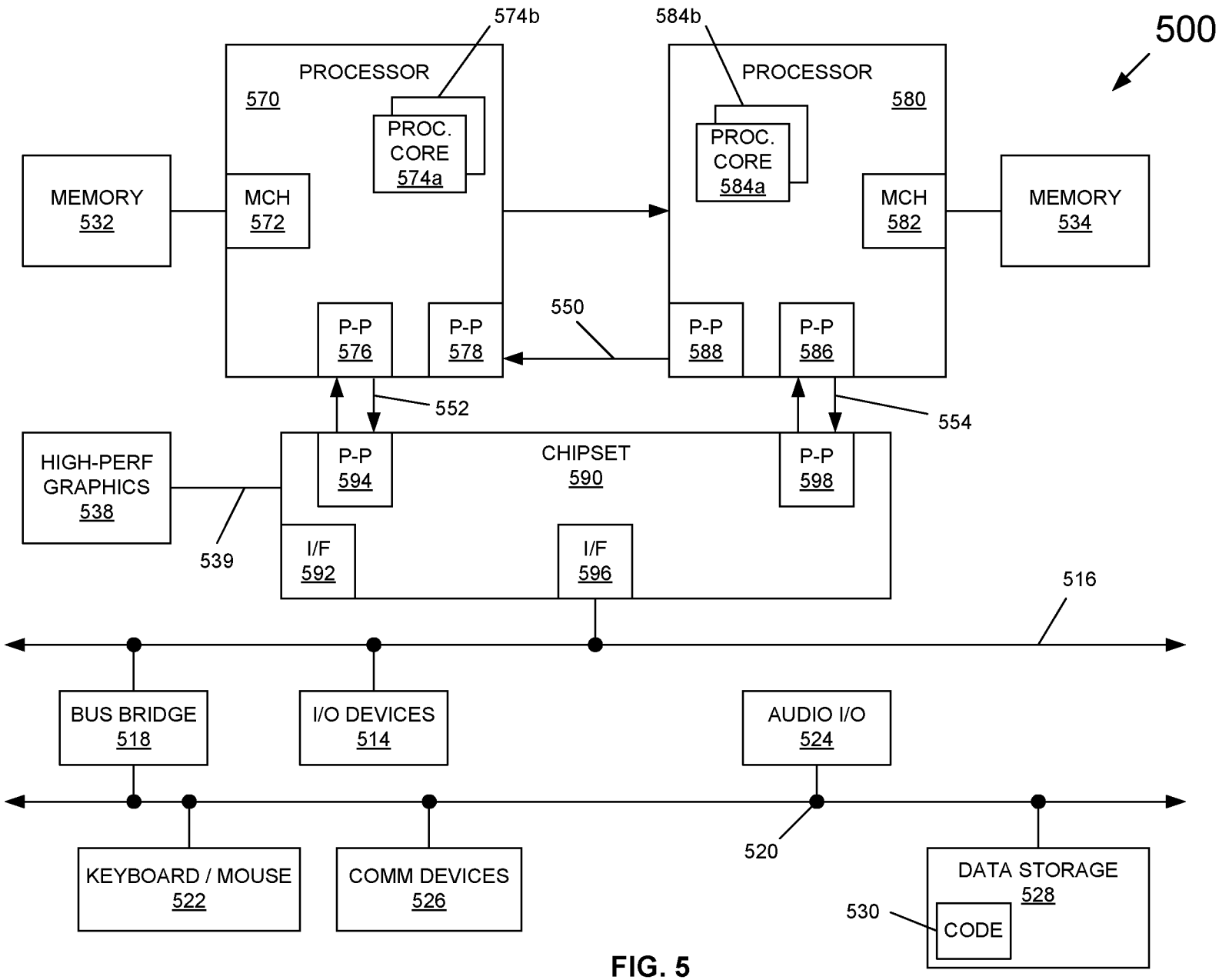


FIG. 5

Petitioner Mercedes Ex-1009, 0313

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	ENABLING A NON-CORE DOMAIN TO CONTROL MEMORY BANDWIDTH

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 14/451,807 filed on August 5, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: AVINASH N. ANANTHAKRISHNAN Date (Optional): 14-Aug-2014

Signature: Avinash

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LEGAL NAME OF INVENTOR

Inventor: INDER M. SODHI Date (Optional) :

Signature: Inder Sodhi

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LEGAL NAME OF INVENTOR

Inventor: EFRAIM ROTEM Date (Optional): 6/8/2014

Signature: _____

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LEGAL NAME OF INVENTOR

Inventor: DORON RAJWAN Date (Optional): 11/8/2014

Signature: _____

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I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: ELIEZER WEISSMANN Date (Optional) 2/6/2015

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	ENABLING A NON-CORE DOMAIN TO CONTROL MEMORY BANDWIDTH

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 14/451,807 filed on August 5, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: RYAN WELLS Date (Optional) :

Signature: Ryan Wells

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/AIA/80 (07-12)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

■ Practitioners associated with Customer Number: 47795

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

■ The address associated with Customer Number: 47795

OR

☐	Firm or Individual Name			
	Address			
	City		State	Zip
	Country			
	Telephone		Email	

Assignee Name and Address: Intel Corporation
2200 Mission College Boulevard
Santa Clara, CA 95054

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	/Heather Adamson/	Date	03/21/2014
Name	Heather Adamson	Telephone	503-712-5273
Title	Administrator of Patents		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

November 11, 2014

Re: Delegation of Signature Authority

To Whom It May Concern:

I, Allon Stabinsky, Vice President for Intel Corporation, hereby delegate authority to sign Powers of Attorney in patent matters before any patent office, Revocations of Power of Attorney in patent matters before any patent office, Patent Assignments, and other patent-related documents to: Jeff Draeger as Director, Intel Patent Group, Intel Corporation; Libby Hope, Sharon Wong and Kerry Tweet as Assistant Directors, Intel Patent Group, Intel Corporation; and Paul Steiner as Patent Procedures Manager, Intel Patent Group, Intel Corporation.

I hereby further delegate authority to sign Powers of Attorney in patent matters before any patent office and Revocations of Power of Attorney in patent matters before any patent office to Heather Adamson, Lisa Hopkinson, and Janice Boulden as Administrators of Patents, Intel Patent Group, Intel Corporation.

Thank you for your cooperation in this matter.

Sincerely,

Allon Stabinsky
Vice President
Litigation, Licensing, and Patents
Intel Corporation

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Intel Corporation

Application No./Patent No.: Filing Concurrently Filed/Issue Date: April 26, 2016

Titled: Enabling A Non-Core Domain To Control Memory Bandwidth In A Processor

Intel Corporation, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 037838, Frame 0285, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Mark J. Rozman/	2016-04-26
Signature	Date
Mark J. Rozman	42,117
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	25598280
Application Number:	15138505
International Application Number:	
Confirmation Number:	3621
Title of Invention:	Enabling A Non-Core Domain To Control Memory Bandwidth
First Named Inventor/Applicant Name:	Avinash N. Ananthakrishnan
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.2492C2US (P38407C2)
Receipt Date:	26-APR-2016
Filing Date:	
Time Stamp:	13:37:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	ITL2492C2USPatentApplicationTrans.pdf	139059 86732bcb8e4fb360e785582548709c928be2c447	no	2

Warnings:	
Information:	

Petitioner Mercedes Ex-1009, 0325

2	Application Data Sheet	ITL2492C2USADS.pdf	1823682 c381246c5c67b853b1a06456d2f011d961e27c16	no	10
Warnings:					
Information:					
3		ITL2492C2USPatentApplication.pdf	162065 013c27fb43de8d79998ee0a76454928ce7442a00	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	14
	Claims	15	15
	Abstract	16	16

Warnings:					
Information:					
4	Drawings-only black and white line drawings	ITL2492USDRAWINGS.pdf	47300 4e419906a7ce770078a7f9a8f2f4107311fc169e	no	5
Warnings:					
Information:					
5	Oath or Declaration filed	ITL2492USExDecs.pdf	982517 4d2d666632ae3c3bf9c806d7980ae38ebd42130b	no	6
Warnings:					
Information:					
6	Power of Attorney	INTEL_POST_AIA_POA_US.pdf	785022 cfb6b31c4228b28ef3de107bebbe2bac1a4570fe	no	2
Warnings:					
Information:					
7	Assignee showing of ownership per 37 CFR 3.73	ITL2492C2US373ToFile.pdf	82219 1453733bddfd844f07091fd25fab19b6e7c4b5de	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	4021864		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.