

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-01345
Patent 10,705,588 B2

Before WILLIAM V. SAINDON, JUSTIN T. ARBES, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Petitioner Mercedes-Benz USA, LLC filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–20 of U.S. Patent No. 10,705,588 B2 (Ex. 1001, “the ’588 patent”) pursuant to 35 U.S.C. § 311(a). Patent Owner Daedalus Prime LLC waived its right to file a preliminary response. See Paper 6; 37 C.F.R. § 42.107(b).

Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” *See* 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”). For the reasons that follow, we institute an *inter partes* review as to claims 1–20 of the ’588 patent on all grounds of unpatentability asserted in the Petition.

B. Related Matters

A different petitioner filed a petition in Case IPR2023-00547 (“the -547 case”) challenging claims 1–20 of the ’588 patent; the proceeding was terminated due to settlement after institution. *See* IPR2023-00547, Papers 1, 13 (“-547 Dec. on Inst.”). The parties also identify the following non-Board proceedings as related matters involving the ’588 patent:

(1) *Daedalus Prime LLC v. Arrow Electronics, Inc.*, No. 1:22-cv-01107 (D. Del.) (terminated); (2) *Daedalus Prime LLC v. Mazda Motor Corp.*, No. 1:22-cv-01108 (D. Del.) (terminated); (3) *Daedalus Prime LLC v. Mazda Motor Corp.*, No. 1:22-cv-01109 (D. Del.) (pending); (4) *Daedalus Prime LLC v. Samsung Electronics Co.*, No. 2:22-cv-00352 (E.D. Tex.) (pending; terminated as to the ’588 patent); (5) *In the Matter of Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, U.S. International Trade Commission (“ITC”) Inv. No. 337-TA-1335 (pending); and (6) *In the Matter of Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, ITC Inv. No. 337-TA-1332 (terminated). *See* Pet. 2–4; Paper 3, 2.

C. The '588 Patent

The '588 patent, titled “Enabling a Non-Core Domain to Control Memory Bandwidth in a Processor,” relates to a “multi-domain processor including multiple domains such as a core domain, a non-core domain and a system agent domain” that “enable[s] the non-core domain to control memory bandwidth available to it.” Ex. 1001, code (54), col. 1, ll. 57–60. The '588 patent states that “[b]y allowing a non-core domain to have control over an interconnect frequency and thus bandwidth, memory bandwidth used by [the] non-core domain can be more efficient” than in the processors of the prior art. *Id.* at col. 1, l. 67–col. 2, l. 2.

Figure 3 of the '588 patent is reproduced below.

300

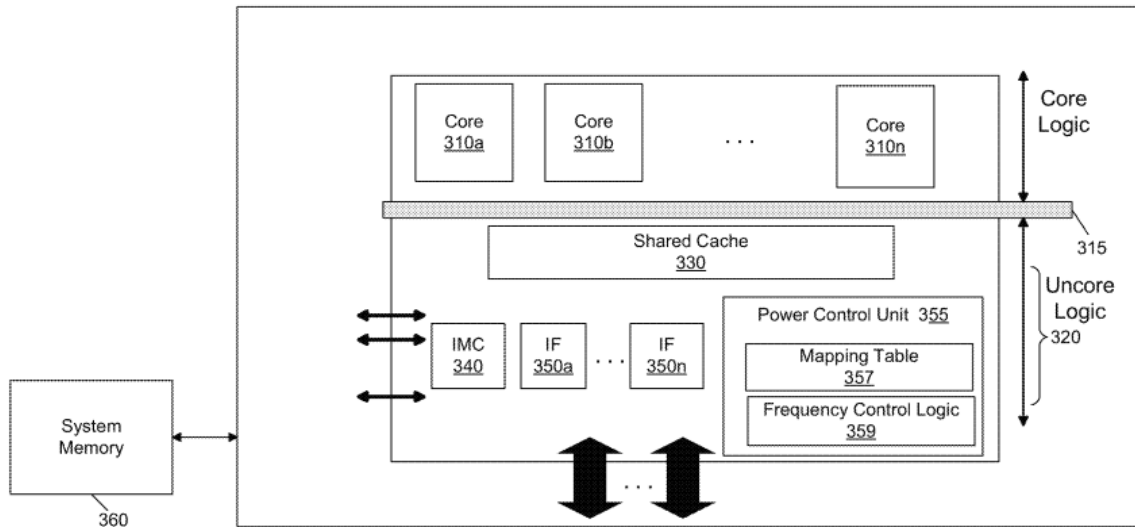


FIG. 3

Figure 3 is a block diagram of one embodiment of a processor according to the '588 patent. *Id.* at col. 1, ll. 47–48. As shown, processor 300 includes: (1) a plurality of cores 310a–310n having independent power domains and operating at independent voltages and/or frequencies; (2) a system agent or

“uncore” 320 having shared cache 330, integrated memory controller (IMC) 340, various interfaces (IF) 350 a –350 n , and power control unit (PCU) 355; (3) interconnect 315 that couples cores 310 a –310 n to uncore 320; and (4) system memory 360. *Id.* at col. 5, ll. 37–50, col. 6, ll. 4–6. Processor 300 communicates with system memory 360 via a memory bus and with various off-chip components (e.g., peripheral devices and mass storage) via interfaces 350. *Id.* at col. 6, ll. 4–8.

The ’588 patent states that, in some embodiments, PCU 355 includes mapping table 357 and frequency control logic 359, whereby each domain (e.g., each core) has a respective mapping table/entries that associate a given domain frequency to a corresponding minimum interconnect frequency. *Id.* at col. 5, ll. 51–66. Frequency control logic 359 dynamically controls the interconnect frequency responsive to a request of a given domain (e.g., of a core) by reference to matching entries of mapping table 357. *Id.*

Figure 4 of the '588 patent is reproduced below.

400

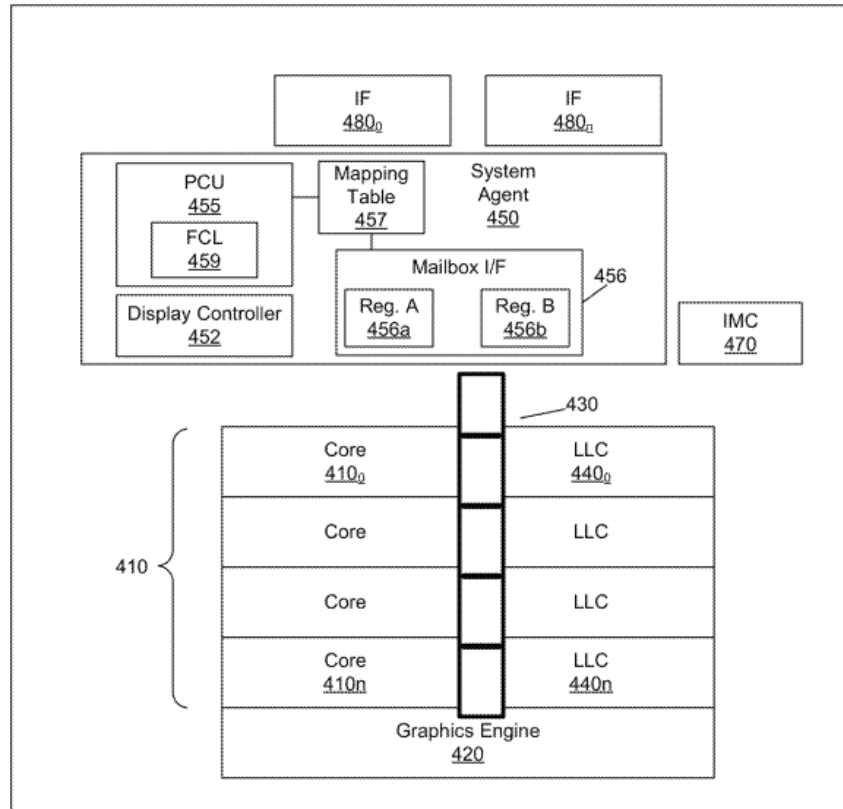


FIG. 4

Figure 4 is a block diagram of another embodiment of a processor according to the '588 patent. *Id.* at col. 1, ll. 49–51. As shown, processor 400 includes: (1) core domain 410 having a plurality of cores 410₀–410_n; (2) last level caches (LLC) 440₀–440_n associated with each core; (3) graphics domain 420 having one or more graphics engines; and (4) system agent domain 450. *Id.* at col. 6, ll. 11–18, 32–34. Ring interconnect 430 couples cores 410₀–410_n and their respective LLCs 440₀–440_n, and further interconnects core 410, graphics domain 420, and system agent domain 450. *Id.* at col. 6, ll. 32–40.

System agent domain 450 includes display controller 452 that provides a user interface, and PCU 455 having frequency control logic 459 that dynamically updates the frequency of interconnect 430 by referencing coupled mapping table 457 (associating a domain's frequency and a corresponding minimum interconnect frequency, as described above). *Id.* at col. 6, ll. 45–58. System agent domain 450 “may execute at a fixed frequency and may remain powered on at all times to handle power control events and power management such that domains 410 and 420 can be controlled to dynamically enter into and exit low power states.” *Id.* at col. 6, ll. 18–23.

The '588 patent states that mailbox interface 456 is used to configure mapping table 457. *Id.* at col. 6, ll. 64–66. Mailbox interface 456 includes first register 456*a* and second register 456*b* providing an interface for handshake-based communications between the PCU and other domains. *Id.* at col. 6, l. 64–col. 7, l. 2. Graphics domain 420 can write to mapping table 457 by providing, to first register 456*a*, a write command, an entry address of the table, and data to be written. *Id.* at col. 7, ll. 7–13. The data is written to second register 456*b*. *Id.* PCU 455 then writes the data to the entry address of the table. *Id.* at col. 7, ll. 13–16.

D. Illustrative Claim

Challenged claims 1, 8, and 20 of the '588 patent are independent. Claims 2–7 depend, directly or indirectly, from claim 1, and claims 9–19 depend, directly or indirectly, from claim 8. Claim 1 recites (with letter designations used in the Petition to refer to the various limitations):

1. [p] A processor comprising:

[A] a plurality of cores including a first core operable at a first voltage and at a first frequency, and [B] a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

[C] graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and

[D] an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first, second, and third frequencies.

E. Evidence

Petitioner relies on the following prior art:

U.S. Patent No. 7,392,411 B2, issued June 24, 2008 (Ex. 1006, “Shakkarwar”);

U.S. Patent No. 7,263,457 B2, issued Aug. 28, 2007 (Ex. 1005, “White”); and

U.S. Patent Application Publication No. 2011/0022356 A1, published Jan. 27, 2011 (Ex. 1007, “Nussbaum”).

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–20 of the ’588 patent are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–4, 7–11, 14–20	102 ¹	White

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102 and 103. Because the challenged claims of the ’588 patent have an effective filing date before the

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–4, 7–11, 14–20	103(a)	White
5, 6, 12, 13	103(a)	White, Shakkarwar
1–4, 7–11, 14–20	102	Nussbaum
1–4, 7–11, 14–20	103(a)	Nussbaum
5, 6, 12, 13	103(a)	Nussbaum, Shakkarwar

II. ANALYSIS

A. Legal Standards

“Anticipation requires that every limitation of the claim in issue be disclosed, either expressly or under principles of inherency, in a single prior art reference,” *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1255–56 (Fed. Cir. 1989), and that the claim limitations be “arranged or combined in the same way as recited in the claim,” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). However, “the reference need not satisfy an *ipsissimis verbis* test.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009). “In an anticipation analysis, the dispositive question is whether a skilled artisan would ‘reasonably understand or infer’ from a prior art reference that every claim limitation is disclosed in that single reference.” *Acoustic Tech., Inc. v. Itron Networked Solutions, Inc.*, 949 F.3d 1366, 1373 (Fed. Cir. 2020) (citation omitted). Whether a reference anticipates is assessed from the perspective of an

effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103. *See* Pet. 14, 59; Ex. 1001, codes (22), (63). Petitioner also challenges certain claims as “anticipated or obvious” over each of White and Nussbaum. Pet. 6–7, 19, 61. We view these as two separate grounds for each reference. *See* 37 C.F.R. § 42.104(b)(2).

ordinarily skilled artisan. *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1336 (Fed. Cir. 2008) (“[T]he meaning of a prior art reference requires analysis of the understanding of an artisan of ordinary skill.”).

A claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a) (2006)). The question of obviousness is resolved on the basis of underlying factual determinations, including “the scope and content of the prior art”; “differences between the prior art and the claims at issue”; and “the level of ordinary skill in the pertinent art.” *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Additionally, secondary considerations, such as “commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy.” *Id.*

A patent claim “is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418. An obviousness determination requires finding “both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016). Also, “[t]hough less common, in appropriate circumstances, a patent can be obvious in light of a single prior art reference if it would have been obvious to modify that reference to arrive at the

patented invention.” *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner argues that at the time of the earliest possible priority date of the ’588 patent (October 2011), a person of ordinary skill in the art would have had

a bachelor’s degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and additional experience substituting for formal education.

Pet. 11, 13–14 (citing Ex. 1003 ¶¶ 26–30). Based on the record presented, including our review of the ’588 patent and the types of problems and solutions described in the ’588 patent and cited prior art, we agree with Petitioner’s proposed definition of the level of ordinary skill in the art and apply it for purposes of this Decision. The same level of ordinary skill in the art was adopted in the -547 case. *See* -547 Dec. on Inst. 22–23.

C. Claim Interpretation

We interpret each challenged claim

using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b). Petitioner proposes interpretations for three terms that appear only in claim 20. Pet. 11–13. As in the -547 case, we conclude that no express interpretation of any claim term is necessary to determine whether to institute an *inter partes* review in this proceeding. See -547 Dec. on Inst. 23–24; *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“Because we need only construe terms ‘that are in controversy, and *only to the extent necessary* to resolve the controversy,’ we need not construe [a particular claim limitation] where the construction is not ‘material to the . . . dispute.’” (citation omitted) (emphasis added)).

D. Asserted Grounds Based on White (Claims 1–4, 7–11, and 14–20)

Petitioner contends that claims 1–4, 7–11, and 14–20 are anticipated by, and unpatentable as obvious over, White, citing the testimony of Robert W. Horst, Ph.D., as support. Pet. 14–49 (citing Ex. 1003). Patent Owner did not file a preliminary response. We are persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted grounds based on White as to claim 1.

1. White

White discloses a processor or other integrated circuit with multiple logic cores that are configured to operate at independent frequencies and voltages and may be connected to other sub-systems, components, or peripherals external to the integrated circuit, such as memory or communications busses. Ex. 1005, col. 2, ll. 15–22, 45–67, col. 6, ll. 23–40.

Figure 1 of White is reproduced below.

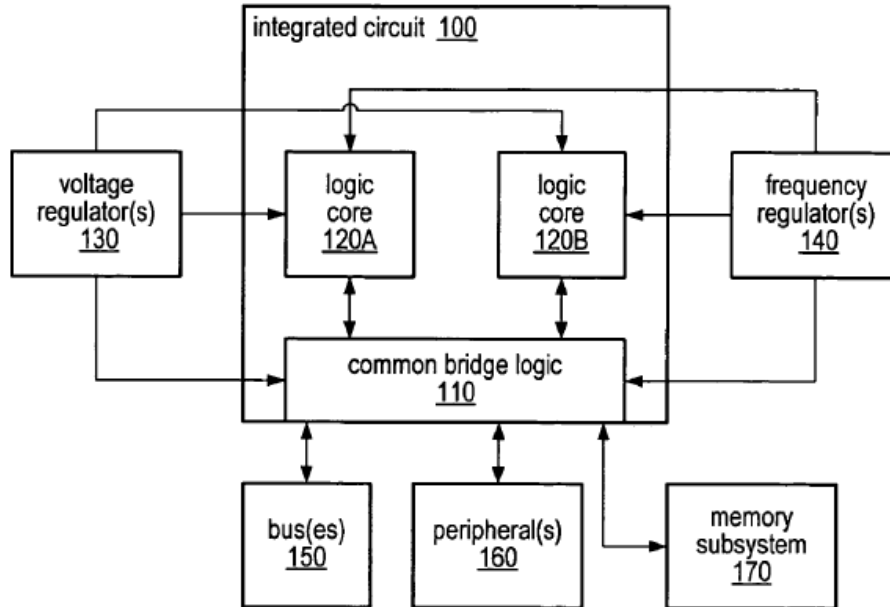


FIG. 1

Figure 1 is “a block diagram illustrating an integrated circuit including multiple logic cores configured to operate at independent voltages and/or frequencies.” *Id.* at col. 5, ll. 28–31. Figure 1 depicts integrated circuit 100 with logic cores 120A and 120B, voltage regulator(s) 130, frequency regulator(s) 140, and common bridge logic 110 “configured to communicate with the logic cores as well as with other elements or peripherals either internal or external to integrated circuit 100, such as bus 150, peripheral 160 and/or memory subsystem 170.” *Id.* at col. 6, l. 41–col. 7, l. 7.

Figure 2B of White is reproduced below.

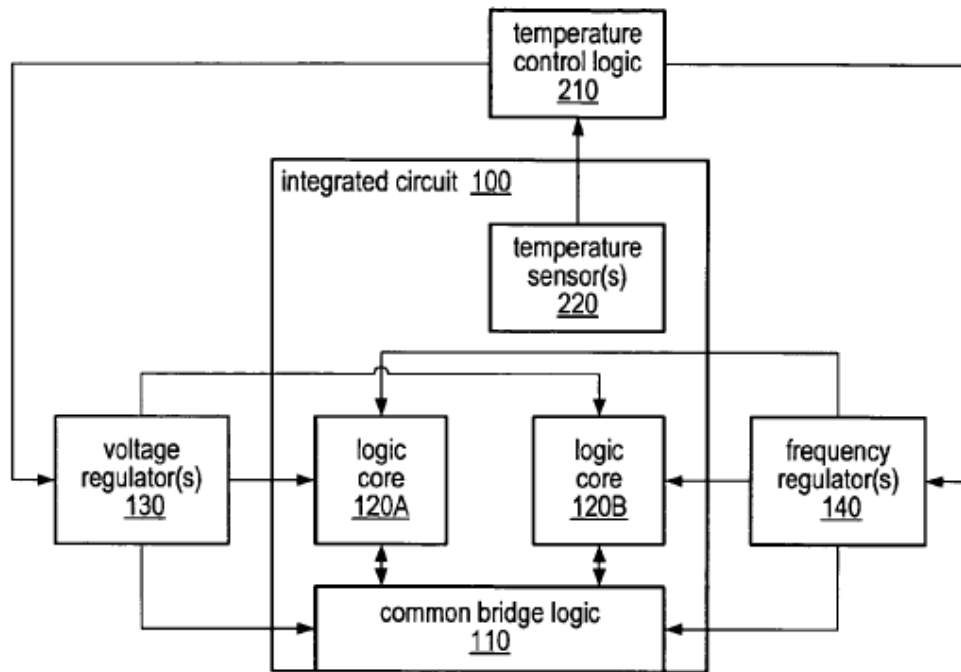


FIG. 2B

Figure 2B shows an “embodiment of a multi-core integrated circuit for which the operating characteristics (i.e. operating voltage and frequency) for each of multiple logic cores may be controlled by temperature control logic.” *Id.* at col. 11, ll. 61–64. Integrated circuit 100 includes temperature sensor(s) 220 that measure the “overall operating temperature of the entire integrated circuit 100” or “a local operating temperature for logic core 120A or logic core 120B.” *Id.* at col. 12, ll. 16–22. If the sensor(s) detect that the temperature is too high, the operating frequency or voltage of components, such as logic core 120A or logic core 120B, may be decreased by temperature control logic 210. *Id.* at col. 12, l. 59–col. 14, l. 20.

Figure 8 of White is reproduced below.

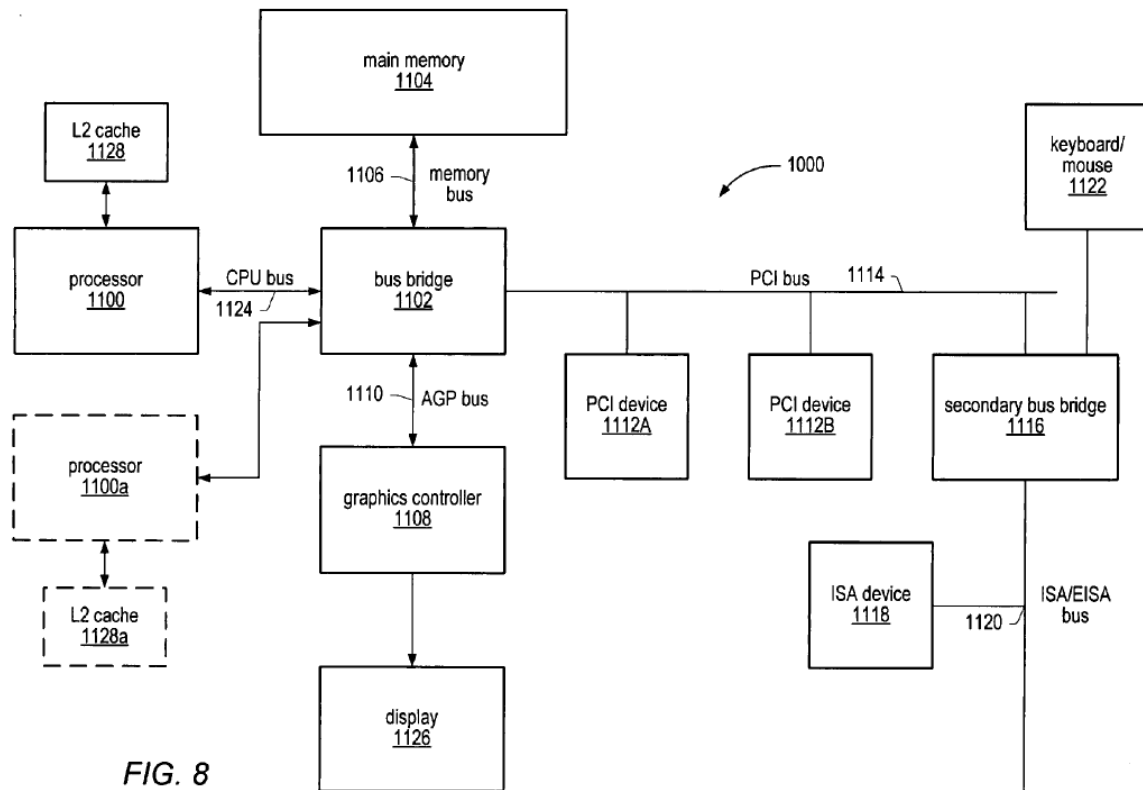


FIG. 8

Figure 8 depicts “computer system 1000 that includes a microprocessor 1100 coupled to a variety of system components through a Bus Bridge [1102].” *Id.* at col. 24, ll. 30–33. “Microprocessor 1100 may include multiple logic cores each of which may be configured to operate at voltages and/or frequencies independent of the voltages and/or frequencies at which others of the cores may operate,” and may include the temperature control components described with reference to Figure 2B above. *Id.* at col. 24, ll. 33–46. Also, graphics controller 1108 for “control[ing] the rendering of text and images on” display 1126, connected to Bus Bridge 1102 by Accelerated Graphics Port (AGP) bus 1110, “may include one or more multi-core integrated circuits and each logic core within such an integrated circuit may be configured to operate at independent frequencies and/or voltages.” *Id.* at col. 24, ll. 47–54, col. 25, ll. 64–65. “Bus Bridge 1102 may

provide an interface between microprocessor 1100, main memory 1104, graphics controller 1108, and devices attached to PCI bus 1114.” *Id.* at col. 25, ll. 21–23. “When an operation is received from one of the devices connected to Bus Bridge 1102, Bus Bridge 1102 identifies the target of the operation” and “routes the operation to the targeted device,” “translat[ing] an operation from the protocol used by the source device or bus to the protocol used by the target device or bus.” *Id.* at col. 25, ll. 23–31. Main memory 1104 (e.g., Dynamic Random Access Memory (DRAM)) “may be a memory in which application programs are stored and from which microprocessor 1100 primarily executes.” *Id.* at col. 25, ll. 50–53.

2. Claim 1

Petitioner argues that White discloses all of the limitations of claim 1. Pet. 14–32 (citing Ex. 1003 ¶¶ 59–92). Petitioner contends that the device shown in Figure 8 above, comprising multiple logic cores, a graphics controller, and an interconnected memory device, is a “processor.”² *Id.* at 19–22.

With respect to limitations 1[A] and 1[B], Petitioner argues that microprocessor 1100 contains integrated circuit 100 with a plurality of logic cores including a “first core” (i.e., logic core 120A shown in Figure 2B) “operable at a first voltage and at a first frequency” and a “second core” (i.e., logic core 120B) “operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency.” *Id.* at

² Petitioner does not take a position on whether the preambles to the claims are limiting. At this stage of the proceeding, we accept Petitioner’s showing that the preamble of claim 1 is taught by the prior art, without deciding whether the preamble is limiting.

20–27 (citing Ex. 1005, col. 24, ll. 33–46). Among other disclosures, Petitioner points to White’s statements that (1) each logic core “may be configured to operate at a particular voltage and frequency *regardless of whether* other logic cores in the processor are also operating at the same voltage and/or frequency”; (2) logic core 120A can be “configured to operate at an *independent* voltage and frequency” and “each logic core may operate at a voltage and/or frequency *independently* from the voltage and/or frequency at which other logic cores, such as logic core 120B, may operate”; and (3) each logic core can “us[e] a *different* voltage level and/or clock frequency.” *Id.* (quoting Ex. 1005, col. 2, ll. 15–22, 55–57, col. 6, ll. 43–49) (emphasis added).

With respect to limitation 1[C], Petitioner argues that White discloses “graphics processing circuitry” (i.e., graphics controller 1108) “coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency.” *Id.* at 27–29. Petitioner explains that graphics controller 1108 performs graphic processing for display 1126 and is coupled to the logic cores in microprocessor 1100 “through CPU bus 1124, bus bridge 1102, and AGP bus 1110,” as shown in Figure 8. *Id.* Also, as Petitioner points out, White discloses, after discussing the independent voltages and frequencies of the logic cores, that

other components of system 1000 may include multiple logic cores that may be configured to operate at *independent* frequencies and/or voltages. For example, graphics controller 1108 may include one or more multi-core integrated circuits and each logic core within such an integrated circuit may be configured to operate at *independent* frequencies and/or voltages, as described herein.

Ex. 1005, col. 24, ll. 47–54 (emphasis added); *see* Pet. 29 (citing Ex. 1005, col. 6, ll. 42–46, col. 24, ll. 47–54).

With respect to limitation 1[D], Petitioner argues that White teaches an “interconnect” (i.e., either AGP bus 1110, bus bridge 1102, and memory bus 1106 shown in Figure 8, or common bridge logic 110 shown in Figure 1) to couple graphics controller 1108 to a “memory device” (i.e., either main memory 1104 shown in Figure 8, or memory subsystem 170 shown in Figure 1), where “the interconnect [is] operable at a fourth frequency different from the first, second, and third frequencies.” Pet. 29–32 (citing Ex. 1005, col. 7, ll. 1–11 (describing the connection from integrated circuit 100 with common bridge logic 110 to memory subsystem 170 shown in Figure 1), col. 25, ll. 1–23 (describing the connection from graphics controller 1108 to main memory 1104 shown in Figure 8)). Regarding White’s common bridge logic, Petitioner points out that it can be a “Northbridge,” which is a “common component of many processors and may include separate interfaces to communicate with and route communication from multiple logic cores of an integrated circuit to other sub-systems, components or peripherals external to the integrated circuit.” *Id.* at 31–32 (quoting Ex. 1005, col. 2, ll. 48–53). Petitioner further relies on White’s disclosure that the common bridge logic can “operate at a frequency and voltage *different* from any particular voltage or frequency at which the individual logic cores may be currently operating,” and argues that a person of ordinary skill in the art would know that AGP bus 1110 “operates at a frequency *independent* of the frequency of the cores within processors 1100 and graphics controller 1108.” *Id.* at 32 (quoting Ex. 1005, col. 2, ll. 64–67; citing Ex. 1003 ¶¶ 90–92) (emphasis added).

Petitioner has made a sufficient showing, based on the current record, that White discloses all of the limitations of claim 1. *See* Pet. 14–32. Accordingly, Petitioner has shown a reasonable likelihood of prevailing on its assertion that claim 1 is anticipated by, and also unpatentable as obvious over, White. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (“[I]t is well settled that a disclosure that anticipates under § 102 also renders the claim invalid under § 103, for anticipation is the epitome of obviousness.” (citations and internal quotation marks omitted)). We institute review “on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” *See* 37 C.F.R. § 42.108(a).

3. *Claims 2–4, 7–11, and 14–20*

On this record, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertion that claim 1 is anticipated by, and unpatentable as obvious over, White, and need not determine at this time whether Petitioner also has shown a reasonable likelihood of prevailing as to any of the challenged dependent claims. *See* 37 C.F.R. § 42.108(a).

E. Additional Asserted Grounds Based on White, Nussbaum, and Shakkarwar (Claims 1–20)

Petitioner contends that claims 5, 6, 12, and 13 are unpatentable over White and Shakkarwar under 35 U.S.C. § 103(a); claims 1–4, 7–11, and 14–20 are anticipated by Nussbaum under 35 U.S.C. § 102; claims 1–4, 7–11, and 14–20 are unpatentable over Nussbaum under 35 U.S.C. § 103(a); and claims 5, 6, 12, and 13 are unpatentable over Nussbaum and Shakkarwar under 35 U.S.C. § 103(a). Pet. 49–94. On this record, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertion

that claim 1 is anticipated by, and unpatentable as obvious over, White, and need not determine at this time whether Petitioner also has shown a reasonable likelihood of prevailing as to any other challenged claims or asserted grounds. *See* 37 C.F.R. § 42.108(a).

III. CONCLUSION

Based on the arguments presented in the Petition, we conclude that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the '588 patent challenged in the Petition. Accordingly, we institute a trial on all claims and all grounds asserted in the Petition. The Board has not made a final determination under 35 U.S.C. § 318(a) with respect to the patentability of the challenged claims.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–20 of the '588 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '588 patent shall commence on the entry date of this Decision, and notice is hereby given of the institution of a trial.

IPR2023-01345
Patent 10,705,588 B2

FOR PETITIONER:

Celine Crowson
Joe Raffetto
Scott Hughes
Ryan Stephenson
Nicholas Rotz
Helen Y. Trac
HOGAN LOVELLS US LLP
celine.crowson@hoganlovells.com
joseph.raffetto@hoganlovells.com
scott.hughes@hoganlovells.com
ryan.stephenson@hoganlovells.com
nicholas.rotz@hoganlovells.com
helen.trac@hoganlovells.com

FOR PATENT OWNER:

Tarek Fahmi
Jonathan Tsao
ASCENDA LAW GROUP, PC
tarek.fahmi@ascendalaw.com
jonathan.tsao@ascendalaw.com