

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,

Petitioner,

v.

DAEDALUS PRIME LLC,

Patent Owner.

Case No.: IPR2023-01345

U.S. Patent No. 10,705,588

PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION AND SUMMARY OF ARGUMENTS..	1
II.	BACKGROUND, THE '588 PATENT, AND CLAIM CONSTRUCTION	2
A.	Background	2
B.	The '588 Patent	3
C.	Claim Construction and the Level of Ordinary Skill in the Art	6
1.	Selectable frequencies of the graphics processing circuitry and of the interconnect	9
D.	The IPR Petition.....	9
III.	THE PETITION FAILS TO DEMONSTRATE THAT CLAIMS 5, 6, 12, and 13 ARE UNPATENTABLE	10
A.	White-Shakkarwar Fails to Teach or Suggest the Invention Recited in Claims 5 and 12	12
1.	Overview of White	13
2.	Overview of Shakkarwar	17
3.	The petition fails to show that White-Shakkarwar teaches or suggests a mapping of selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect, as claimed.....	19
B.	Claims 6 and 13 Are Not Obvious in View of White-Shakkarwar	23
C.	Nussbaum-Shakkarwar Fails to Teach or Suggest the Invention Recited in Claims 5 and 12	23
1.	Overview of Nussbaum	23

2.	The petition fails to show that Nussbaum-Shakkarwar teaches or suggests a mapping of selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect, as claimed	26
D.	Claims 6 and 13 Are Not Obvious in View of Nussbaum-Shakkarwar	29
IV.	CONCLUSION	29

TABLE OF AUTHORITIES

CASES

<i>ACTV, Inc. v. Walt Disney Co.</i> , 346 F.3d 1082 (Fed. Cir. 2003).....	7
<i>Arendi S.A.R.L. v. Apple Inc.</i> , 832 F.3d 1355 (Fed. Cir. 2016).....	19
<i>CFMT, Inc. v. Yieldup Intern. Corp.</i> , 349 F.3d 1333 (Fed. Cir. 2003).....	22, 29
<i>Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.</i> , 800 F.3d 1375 (Fed. Cir. 2015).....	30
<i>Harmonic Inc. v. Avid Tech., Inc.</i> , 815 F.3d 1356 (Fed. Cir. 2016).....	29
<i>Hartness Int’l. Inc. v. Simplimatic Engineering Co.</i> , 819 F.2d 1100 (Fed. Cir. 1987).....	23, 29
<i>In re Gordon</i> , 733 F.2d 900 (Fed. Cir. 1984).....	11
<i>In re Magnum Oil Tools Int’l, Ltd.</i> , 829 F.3d 1364 (Fed. Cir. 2016).....	30
<i>In re Peterson</i> , 315 F.3d 1325 (Fed. Cir. 2003).....	11
<i>In re Ratti</i> , 270 F.2d 810 (CCPA 1959)	11
<i>In re Warner</i> , 379 F.2d 1011 (CCPA 1967)	11
<i>Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.</i> , 821 F.3d 1359 (Fed. Cir. 2016).....	11

<i>KSR Int’l v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	11, 12, 19
<i>Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.</i> , 868 F.3d 1013 (Fed. Cir. 2017).....	7
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005).....	7
<i>SAS Inst. Inc. v. Iancu</i> , 138 S. Ct. 1348 (2018).....	10
<i>Takeda Chem. Indus., Ltd. v. Alphapharm Pty, Ltd.</i> , 492 F.3d 1350 (Fed. Cir. 2007).....	19
<i>Vitronics Corp. v. Conceptronic, Inc.</i> , 90 F.3d 1576 (Fed. Cir. 1996).....	7

REGULATIONS

37 C.F.R. § 42.104(b)(4)	22, 29
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EXHIBIT LIST

EXHIBIT NO.	DESCRIPTION
2001	Transcript of Deposition of Dr. Horst
2002	Declaration of Michael C. Brogioli, Ph.D.

I. INTRODUCTION AND SUMMARY OF ARGUMENTS

Mercedes-Benz USA, LLC's ("MB USA" or "Petitioner") challenges to claims 5, 6, 12, and 13 of U.S. Patent No. 10,705,588 (the "'588 patent") fail to demonstrate that these challenged claims are unpatentable.

Insofar as claims 5 and 12 are concerned, the petition alleges that these claims are obvious in view of White-Shakkarwar and/or Nussbaum Shakkarwar because a person of ordinary skill in the art would have employed a look-up table that specifies clock speeds and/or voltages required to process information for specific devices in a power control unit of system such as that described by White and/or Nussbaum. However, even if such a combination were made, the result would not be a mapping of selectable frequencies of a graphics processing circuitry to selectable frequencies of an interconnect, as recited in these claims.

Importantly, Shakkarwar does not associate, by way of a look-up table or otherwise, particular graphics processing circuitry frequencies with particular interconnect frequencies. Instead, Shakkarwar describes a look-up table that reports clock speeds and/or voltage levels as required by software to process information by specific devices. There is no teaching or suggestion that such a table includes any mapping of frequencies of the kind specified, or, indeed, any *mappings* at all. Indeed, Dr. Brogioli explains that

no such mappings are needed because when it comes to hardware bandwidth requirements, Shakkarwar relies on empirical calculations.

Thus, because Shakkarwar does not associate any particular graphics processing circuitry frequencies with particular interconnect frequencies; and, in particular, does not disclose or suggest a mapping of same as required by claims 5 and 12, even if a person of ordinary skill in the art were to combine the teachings of Shakkarwar with those of White and/or Nussbaum as suggested by Petitioner, the result would not be the invention recited in claims 5 and 12 of the '588 patent. Hence, these claims, and their respective dependent claims 6 and 14, have not been shown to be unpatentable.

II. BACKGROUND, THE '588 PATENT, AND CLAIM CONSTRUCTION

A. Background

Modern computing devices make use of processors that combine previously-independent components within a single integrated circuit package. Ex. 1001 at 1:20-26. Consequently, multicore processors have become available and even these processors have been extended to include additional functionalities. *Id.* at 1:27-29. With this increase in functionality, however, complications arise. One such complication is the need to address

the different operational needs of individual components based on their respective workloads. *Id.* at 1:29-38.

One such operational need is the operating frequency of different components of a processor. *Id.* at 1:29-31. In the past, “suitable mechanisms to ensure that these different units operate at an appropriate frequency [were] not available.” *Id.* at 1:32-33.

B. The '588 Patent

The '588 patent describes a multicore processor in which different components can operate at different, independent voltages and/or frequencies. Such components can include individual CPU cores, graphics processing circuitry, and an interconnect. *See, e.g.*, Ex. 1001 at 1:57-2:39. Figure 4 depicts an exemplary embodiment of a multicore processor 400 that includes multiple cores 410a through 410n. *Id.* at 6:11-16. Processor 400 also includes graphics engine 420 and interconnect 430. *Id.* at 6:16-17, 6:37-41. And, processor 400 includes power control unit 455 and frequency control logic 459 to dynamically update the frequency of interconnect 430 based on a frequency of the graphics engine 420. *Id.* at 6:47-63.

400

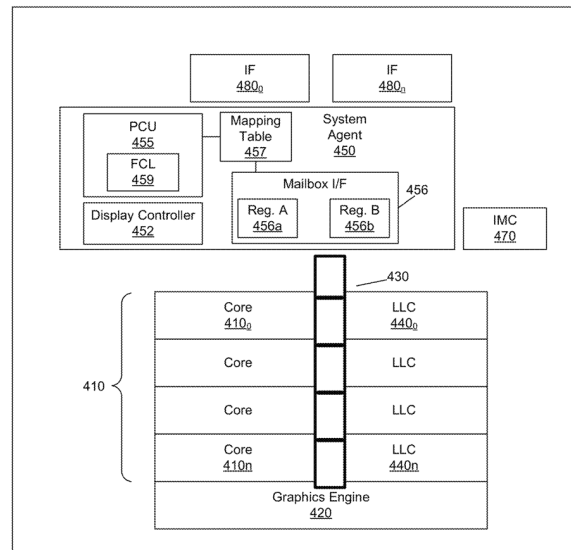


FIG. 4

Of importance to this Patent Owner Response, the '588 patent describes an embodiment of a multicore processor in which a graphics engine, such as graphics engine 420 shown in Fig. 4, can control its own memory bandwidth. *Id.* at 2:19 *et seq.* By allowing this functionality, performance of the graphics engine is improved over that which it might otherwise be, particularly since, for a graphics engine, workload performance is a strong function of the bandwidth available to it. *Id.* at 2:21-25. In the described embodiment, this ability is provided by a mechanism that maps the graphics engine frequency to a corresponding interconnect frequency. “This mapping can be maintained in a table, which may be located in a power controller of the processor such as a power control unit

(PCU).” *Id.* at 2:26-32. The table is configured during initialization, and can be dynamically updated based on a workload being executed by the graphics engine. In this way, a close association between the workload being handled in graphics engine and the bandwidth of the path to the memory subsystem can be achieved. *Id.* at 2:32-39.

Claims 5 and 12 of the ’588 patent recite the “mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.” *Id.* at 8:62-65; 9:37 – 10:2. An example of such a mapping is provided in Table 1 of the specification:

TABLE 1

Table Entry	Non-Core Frequency	Minimum Interconnect Frequency
1	300	800
2	350	800
3	400	800
4	450	800
5	500	800
6	550	800
7	600	800
8	650	1500
9	700	1500
11	750	1500
12	800	1500
13	850	1500
14	900	1800
15	950	1900
16	1000	2000
17	1050	2100
18	1100	2200
19	1150	2300
20	1200	2400
21	1250	2500
22	1300	2600

Id. at 5:13-35. In this example, the mapping table includes a plurality of entries each having two parameters, namely graphics engine (or “non-core domain”) frequency and corresponding minimum interconnect frequency, e.g., specified in MHz. *Id.* at 4:57-61. The specification explains that the graphics engine can set up this table in PCU memory, e.g., by specifying pairwise entries to identify a target interconnect frequency for a corresponding graphics engine frequency. Then, after configuration, the PCU can access the table based on a frequency at which the graphics engine is operating to obtain the corresponding target interconnect frequency. *Id.* at 4:63 – 5:1.

C. Claim Construction and the Level of Ordinary Skill in the Art

In *inter partes* reviews such as this one, the Board applies the same claim construction standard used to construe a claim in a civil action under 35 U.S.C. § 282(b). *Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51,340 (Oct. 11, 2018). Accordingly, the claims should be construed consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art as considered in the context in which the terms of the claims are used. *Phillips v. AWH Corp.*, 415 F.3d 1303,

1312-17 (Fed. Cir. 2005); *Vitronics Corp. v. Conceptronics, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *see also ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) (“the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms”). “The ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Phillips*, 415 F.3d at 1313. Furthermore, constructions are needed only to the extent necessary to resolve any asserted ground in the petition. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (only “terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” need be construed) (quoting *Vivid Techs., Inc. c. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

In its Institution Decision, the Board accepted MB USA’s proposed level of ordinary skill in the art:

[A] bachelor’s degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for

experience and additional experience substituting for formal education.

Paper 7 at 10 (citing Pet. at 11, 13-14). However, because the proposed level of ordinary skill in the art encompasses persons with much more than ordinary skill, the Board should not have accepted this definition.

The proposed level of ordinary skill encompasses persons with “at least two years of experience” in specified fields. Pet. at 13. Such a definition takes in people with more, potentially much more, than ordinary skill in the art—that is, by encompassing people with “at least” two years of experience in the designated field, it includes persons with far greater levels of experience and, therefore, is not limited to just persons of *ordinary skill* in the art. Patent Owner therefore uses the proffered definition of a person of ordinary skill in the art, but limits such individuals to those with two years of experience in the designated field in the analysis below. *See* Ex. 2002 at ¶ 25.

Although the Board did not make any claim constructions as part of its Institution Decision, *see* Paper 7 at 11, certain terms of the claims will be important for understanding distinctions from the prior art cited by Petitioner:

1. Selectable frequencies of the graphics processing circuitry and of the interconnect

Claims 5 and 12 each recite, “a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.” Ex. 1001 at 8:63-65; 9:38 – 10:2. As discussed above, the specification explains such a mapping and includes an example of a table that includes same. Dr. Horst testified that this phrase would be understood by a person of ordinary skill in the art as requiring “a set of possible frequencies that can be selected.” Ex. 2001 at 21:15 – 22:11. Dr. Brogioli agrees. Ex. 2022 at ¶ 33. Accordingly, the Board should construe claims 5 and 12 as requiring a mapping of a set of possible frequencies of the graphics processing circuitry that can be selected to a set of possible frequencies of the interconnect that can be selected.

D. The IPR Petition

In its petition, MB USA presents multiple grounds for the alleged unpatentability of the claims of the ’588 patent. Pet. at 6-7. This Patent Owner Response focuses on the challenges to claims 5, 6, 12, and 13:

Claims Challenged	35 U.S.C. §	References
5, 6, 12,13	103	White ¹ in view of Shakkarwar ²
5, 6, 12,13	103	Nussbaum ³ in view of Shakkarwar

Id.

III. THE PETITION FAILS TO DEMONSTRATE THAT CLAIMS 5, 6, 12, AND 13 ARE UNPATENTABLE

A petition must be judged as it is written. The Board may not overlook flaws in the petition or reformulate its challenges to enhance their suitability. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (“[I]t’s the petitioner, not the Director, who gets to define the contours of the proceeding.”); *see also id.* (“[T]he petitioner is master of its complaint . . .”); *see also id.* at 1353 (forbidding the Board from “curat[ing]” the petition). Furthermore, because all of the challenges in the petition rely on conclusions of obviousness, the analyses set forth in the petition must include “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR Int’l v. Teleflex Inc.*, 550 U.S. 398, 418

¹ US Patent 7,263,457 (Ex. 1005).

² US Patent 7,392,411 (Ex. 1006).

³ US PGPUB 2011/0022356 (Ex. 1007).

(2007) (*quoting In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). The challenger must supply the factual basis for the challenge and “may not resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis.” *In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967). Additionally, in cases such as the present, where the obviousness challenges involve a modification or combination of teachings, the Petitioner must also establish that one skilled in the art would have had a reasonable expectation of success to make the modification or combination. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367-68 (Fed. Cir. 2016). The modification or combination must not “require a substantial reconstruction and redesign of the elements” in a reference or “a change in the basic principles under which [a reference] was designed to operate.” *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959). Nor can the modification or combination render a reference unsatisfactory or “inoperable for its intended purpose.” *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984).

Also, the prior art must be considered for all that it teaches, and a *prima facie* case of obviousness may be rebutted “by showing that prior art teaches away from claimed invention in any material respect.” *In re Peterson*, 315 F.3d 1325, 1331 (Fed. Cir. 2003).

Last but not least, obviousness cannot be established by hindsight combination to produce the claimed invention, as the Supreme Court has emphasized:

A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning. *See Graham [v. John Deere Co.]*, 383 U.S. [1,] 36, 86 S. Ct. 684, 15 L. Ed. 2d 545 [(1966)] (warning against a “temptation to read into the prior art the teachings of the invention in issue” and instructing courts to “guard against slipping into use of hindsight” (quoting *Monroe Auto Equip. Co. v. Heckethorn Mfg. & Supply Co.*, 332 F.2d 406, 412 (6th Cir. 1964))).

KSR, 550 U.S. at 421.

As explained below, the petition’s challenge fails to demonstrate that any challenged claim is unpatentable.

A. White-Shakkarwar Fails to Teach or Suggest the Invention Recited in Claims 5 and 12

MB USA’s first set of challenges to claims 5 and 12 are based on the teachings of White and Shakkarwar. Pet. at 49 *et seq.* In particular, the petition alleges that “White in view of Shakkarwar [] teaches that [] power management circuitry can include a mapping of selectable frequencies of the

graphics processing circuitry to selectable frequencies of the interconnect.”
Id. at 49. The petition relies on Shakkarwar for allegedly teaching the use of
 look-up table to map selectable frequencies of graphics processing circuitry
 to selectable frequencies of an interconnect. *Id.* at 50-51.

1. Overview of White

White describes, “A processor or other integrated circuit [that] may
 include multiple logic cores, each of which may be configured to operate at
 frequencies and voltages independently of other logic cores.” Ex. 1006 at

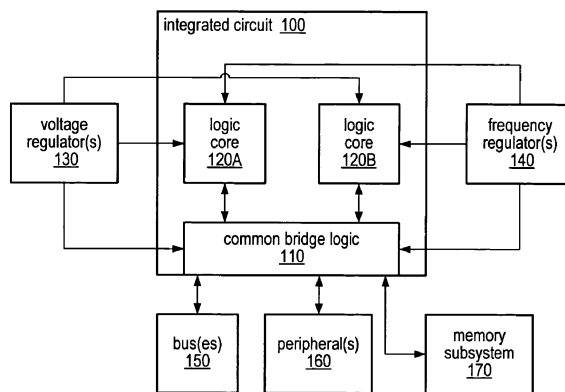


FIG. 1

2:15-18. White’s FIG. 1,
 reproduced here, depicts “a block
 diagram illustrating an integrated
 circuit including multiple logic
 cores configured to operate at
 independent voltages and/or
 frequencies.” *Id.* at 5:18–31; 6:43–

46. The common bridge logic 110, is “configured to communicate with the
 logic cores as well as with other elements or peripherals either internal or
 external to integrated circuit 100, such as bus 150, peripheral 160 and/or
 memory subsystem 170[, and] may be configured to operate at a voltage or

frequency different from, and independent of, the voltages or frequencies at which the logic cores 120A and 120B are operating.” *Id.* at 7:3-11.

According to White, the operating voltage and/or operating frequency of the various logic cores of integrated circuit 100 may be controlled by power management logic 200, as illustrated in FIG. 2A, reproduced here. *Id.* at 8:61-

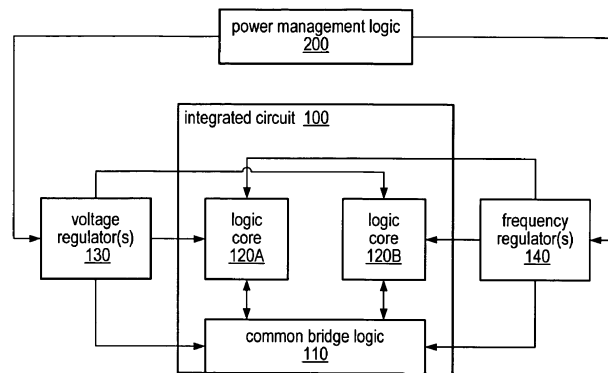


FIG. 2A

65. In this way, overall power consumption for the integrated circuit may be adjusted. *Id.* at 9:1-6. For example, the voltage and/or frequency of the cores 120A, 120B may be lowered when the system is operating on battery power, and raised in other cases. *Id.* at 9:6-12. Similarly, the voltage and/or frequencies supplied to the common bridge logic 110 may be adjusted by the power management logic 200, for example, to reduce potential bottlenecking of the common bridge logic. *Id.* at 9:30-53.

White explains a method for independent power management of the logic cores with reference to FIGs. 4 and 5, reproduced below.⁴ When a need to change an operating characteristic, e.g., frequency (FIG. 4) or voltage (FIG. 5), of a logic core is detected (400, 500), power management logic 200 determines a new operating voltage/frequency for the core (410, 510). *Id.* at 15:42 – 16:62; 18:20 – 19:42. New frequencies may be determined based on a “standard algorithm” or “from a look-up table.” *Id.* at 16:58-63. New

⁴ An additional approach is described with respect to FIG. 6 and involves reducing the operating characteristics for one or more logic cores in steps or stages. *Id.* at 20:58 *et seq.*

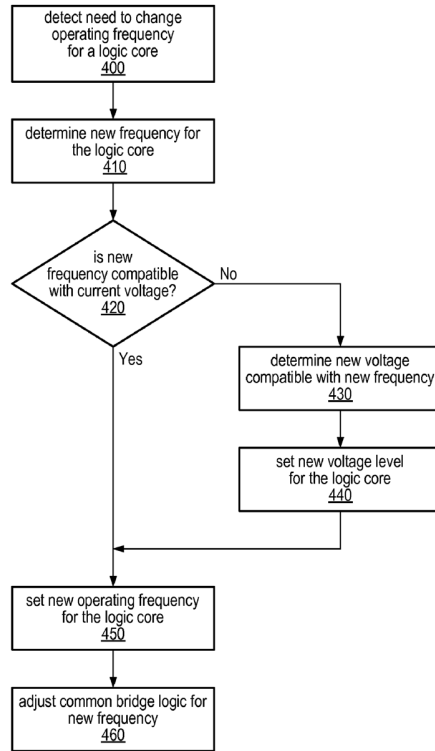


FIG. 4

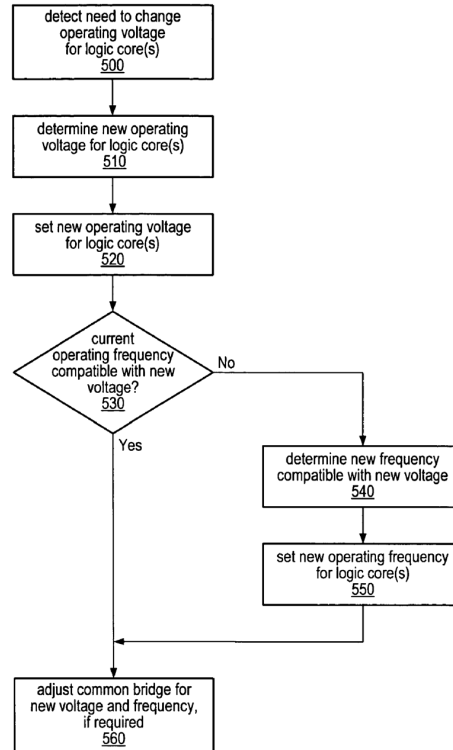


FIG. 5

voltages may be determined via a voltage determining algorithm . . . based upon current operating conditions for the system, such as current operating temperature, current power availability or current power consumption, or may be determined based upon a fixed table of operating voltages. *Id.* at 19:30-38.

Assuming the new frequency is compatible with the operating voltage of the core (420), or after making adjustments therefor (430, 440), the power management logic sets the new operating frequency for the core (450), *id.* at 16:63 – 17:28, and thereafter, adjusts the operating conditions for the

common bridge logic to be compatible with the new operating frequency of the core. (460). *Id.* at 17:29 – 18:8.

In the case of a new operating voltage for a core, after determining that new operating voltage the power management logic sets the new voltage as the operating voltage for the core (520), *id.* at 19:43-47, determines whether the operating frequency of the core is compatible with the new voltage (530), *id.* at 19:53-57, and makes adjustments to the operating frequency as necessary (540, 550). *Id.* at 19:57-65; 20:19-23. Thereafter, the power management logic adjusts the operating conditions for the common bridge logic to be compatible with the new operating voltage and/or frequency of the core. (560). *Id.* at 20:39-57.

2. Overview of Shakkarwar

Shakkarwar is directed to a software-based process for determining an ideal bandwidth for a bus, for example, based on analysis of software being executed by a processor, or based on detecting that certain components connected to the bus are idle or otherwise unused. *See, e.g.*, Ex. 1006 at 5:53 – 7:26. Shakkarwar’s goal is “reduced power consumption attributed to operating a communication bus and/or one or more electronic components and/or electronic devices at lower clock speed(s) and voltage level(s) based

on required bandwidth for processing information ... with minimal effect on overall processing bandwidth.” *Id.* at 8:50-56. Thus, Shakkarwar is concerned solely with adjusting bus data rates, and not the frequencies of the components using the bus.

For example, when the system disclosed in Shakkarwar detects that no software applications are using a GPU, the system can decide to reduce the data rate (i.e., reduce the bandwidth) over the bus to save power. *See id.* at 6:8-16. Similarly, when the system detects that an application was opened that is likely to require the GPU, the system will increase the data rate between the data controller and the graphics controller to support the functionality of the application, but does not disclose or suggest any changes to the data controller or graphics controller components. *See id.* at 6:49-58. Rather, Shakkarwar aims to determine when reducing the data rate of a bus can result in power savings “without sacrificing performance or powering down electronic devices, processors, components, etc.” *See id.* at 4:14-18.

Shakkarwar determines a frequency to change the bus to by using “a look-up table [that] may include a list of clock speeds ... required to process information for specific devices and/or groups of devices.” *Id.* at 7:7-10.

3. The petition fails to show that White-Shakkarwar teaches or suggests a mapping of selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect, as claimed

To find a claim unpatentable for obviousness, it is necessary to show that “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.” *Takeda Chem. Indus., Ltd. v. Alphapharm Pty, Ltd.*, 492 F.3d 1350, 1354-1355 (Fed. Cir. 2007) (quoting 35 U.S.C. §103(a)). This necessarily requires, among other things, determining the scope and content of the prior art. *KSR*, 550 U.S. at 406-407. And, while the obviousness analysis is flexible, what is not flexible is the need to consider all of the limitation of a claim and find, based on a reasoned analysis, they are present, before concluding the claim is obvious. *See, e.g., Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016) (“[R]eferences to ‘common sense’—whether to supply a motivation to combine or a missing limitation—cannot be used as a wholesale substitute for reasoned analysis and evidentiary support, especially when dealing with a limitation missing from the prior art references specified.”).

In the present case, however, MB USA fails to demonstrate that White-Shakkarwar teaches or suggests a mapping of selectable frequencies

of graphics processing circuitry to selectable frequencies of an interconnect, as recited in claims 5 and 12. Ex. 2002 at ¶¶ 42-45. The petition alleges that such a mapping can be found in Shakkarwar, Pet. at 50-51, particularly, the look-up table disclosed at 7:5-10. *Id.* According to the petition, a person of ordinary skill in the art would have understood Shakkarwar teaches such a mapping using the look-up table, because Shakkarwar determines an appropriate bandwidth for a data connection utilizing the look-up table that includes a list of appropriate clock speeds while also considering other active components and their clock speeds. *Id.* at 52-53. The petition concludes that a person of ordinary skill in the art would have employed such a look-up table in a system such as that described by White, as part of the power management logic or temperature control logic. *Id.* at 53. Even if such a combination were made, however, the result would not be the subject matter recited in claims 5 and 12. Ex. 2002 at ¶ 43.

To begin, Shakkarwar does not associate, by way of a look-up table or otherwise, particular GPU frequencies with particular bus frequencies. *Id.* Recall that even petitioner's declarant agreed that claims 5 and 12 require a mapping of a set of possible frequencies of the graphics processing circuitry that can be selected to a set of possible frequencies of the interconnect that can be selected. *See* Ex. 2001 at 21:19 – 22:11. Shakkarwar, on the other

hand, monitors bandwidth for a component (not frequency), and consults a table that includes clock speeds and/or voltage levels required to process information for specific devices. Ex. 2002 at ¶ 43 (citing Shakkarwar at 7:7-10); Ex. 2001 at 24:9 – 25:2. There is no teaching or suggestion that this table, which simply includes clock speeds required to process information for specific devices, has any *mapping* of frequencies, let alone frequencies that can be selected, of the kind specified. Indeed, such a table need only specify what is disclosed: the required clock speed of the affected device, for that is all that is needed to determine the necessary bandwidth of the associated data connection. Ex. 2022 at ¶ 43.

Moreover, Dr. Brogioli notes that, “insofar as Shakkarwar describes detecting ‘a change in processing condition[s],’” those changed processing conditions are not the *frequency* of any components, but rather the anticipated data needs of software. *Id.* at ¶ 44 (citing Shakkarwar at 6:8-16, 49 *et seq.*); Ex. 2001 at 25:3 – 26:3. He continues, “Shakkarwar specifies the look-up table reports clock speeds, etc. ***required to process information*** for specific devices. By highlighting information processing needs, Shakkarwar is indicating that the clock speeds are tied to particular data needs of software. Considerations of the hardware are handled through empirical calculation, by knowing the requested data bandwidth of each device.” *Id.*

(citing Shakkarwar at 7:7-17) (emphasis added); *and see* Ex. 2001 at 26:15 – 29:18. This further exemplifies why the look-up table does not provide any mapping of GPU frequencies to interconnect frequencies, and instead merely reports the device clock speeds (and/or voltages). Ex. 2002 at ¶ 44.

Thus, Shakkarwar does not associate any particular GPU frequencies with particular bus frequencies; and, in particular, disclose or suggest a mapping of selectable frequencies of a GPU to selectable frequencies of an interconnect, as required by claims 5 and 12. Therefore, even if a person of ordinary skill in the art were to combine the teachings of Shakkarwar with those of White, e.g., as suggested by Petitioner through the use of Shakkarwar’s look-up table in as part of the power management logic or temperature control logic in a system such as that described by White, the result would not be the invention recited in claims 5 and 12 of the ’588 patent. *Id.* at ¶ 45. Hence, the petition fails to set forth a prima facie case of obviousness of claims 5 and 12 in view of White-Shakkarwar, *CFMT, Inc. v. Yieldup Intern. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003), and likewise fails to satisfy its obligation to “specify where each element of the claim is found in the prior art.” 37 C.F.R. § 42.104(b)(4).

B. Claims 6 and 13 Are Not Obvious in View of White-Shakkarwar

Challenged claim 6 depends from claim 5 and claim 13 depends from claim 12. Each respective dependent claim is not unpatentable in view of White-Shakkarwar for at least the same reasons as claims 5 and 12, above. *See Hartness Int’l. Inc. v. Simplimatic Engineering Co.*, 819 F.2d 1100 (Fed. Cir. 1987).

C. Nussbaum-Shakkarwar Fails to Teach or Suggest the Invention Recited in Claims 5 and 12

MB USA’s challenges to claims 5 and 12 based on Nussbaum-Shakkarwar are similar to those addressed above based on White-Shakkarwar. Once again, the petition relies on Shakkarwar’s teachings concerning the use of a look-up table that stores clock speeds and/or voltage levels required to process information for specific devices. Pet. at 85-89. And, once again, the petition fails to demonstrate that any of claims 5, 6, 12, and 13 are unpatentable based on the teachings of Nussbaum and Shakkarwar.

1. Overview of Nussbaum

Nussbaum describes an “analysis of workload executed on computational units to help identify those computational units that are more

performance sensitive to a change in performance capability caused by, e.g., a frequency change.” Ex. 1007 at [0005]. Nussbaum explains that “[s]electively distributing power among the active cores or other computational units based on [such] frequency sensitivity allows for greater overall system throughput on heterogeneous workloads or multi-threaded workloads with heterogeneous threads.” *Id.* at [0019]. Nussbaum is therefore directed to determining the frequency sensitivity of computational units to make use of sensitivity-based power allocation. As Nussbaum states, “[t]he rationale for that is to not waste power by boosting cores whose performance will not be increased.” *Id.* at [0040].

Nussbaum describes its approach to calculating the performance sensitivity:

[T]he computational units are operated at a first performance level, and respective first utilization metrics are determined. The computational units are then operated at a second performance level and respective second utilization metrics are determined. The sensitivity to performance capability change, e.g., a frequency change, is determined.

Id. at Abst.; [0006]. As mentioned, power distribution is then based on these measured frequency sensitivities. *Id.* at [0019].

Nussbaum distinguishes this approach from changing power consumption of CPU cores collectively. For example, Nussbaum identifies approaches that “opportunistically raise the performance level (e.g., raise the frequency) of CPU cores on multi-core processors, when the processor integrated circuit is running below its thermal design point (TDP):”

Such approaches allow the operating frequency of the CPU cores to be raised together when there is estimated power, current or thermal headroom in order to improve performance under a given TDP, and decreased when the operation is exceeding those limits. Such approaches have assumed all active CPU cores operate in their maximum performance state when their frequency is raised in a coordinated fashion.

Id. at [0017]. Nussbaum then distinguishes those approaches from its own, explaining that its approach not only differs, but “allows for greater overall system throughput:”

The above approaches for homogenously increasing power to all cores or to one or more cores based on performance states of the cores, allow for power to be reallocated from idle computational units, such as the CPU or graphical processing unit (GPU), but treat all active units homogeneously when dithering frequency or boosting steady state frequency. However, some active cores or other computational units may be gaining little

or no performance increase from a higher core frequency, while other cores or computational units may be running workloads with a higher sensitivity to an increase in core frequency. Selectively distributing power among the active cores or other computational units based on frequency sensitivity allows for greater overall system throughput on heterogeneous workloads or multi-threaded workloads with heterogeneous threads. That requires an effective approach to identify workload sensitivity to changes in core frequency.

Ex. 1007, [0019]. Nussbaum is therefore directed to a different approach than those that allocate power collectively for example.

2. The petition fails to show that Nussbaum-Shakkarwar teaches or suggests a mapping of selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect, as claimed

The petition alleges that Nussbaum-Shakkarwar teaches or suggests a mapping of selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect, as recited in claims 5 and 12, Pet. at 85-89, particularly, that a person of ordinary skill in the art would have understood Shakkarwar teaches such a mapping in the form of a look-up table. *Id.* at 88-89 (“a POSITA would have understood that Shakkarwar teaches to map selectable frequencies of the graphics processing circuitry to

selectable frequencies of the interconnect using look-up tables”). The petition concludes that a person of ordinary skill in the art would have employed such a look-up table in a system such as that described by Nussbaum, as part of Nussbaum’s power allocation controller. *Id.* at 89. Even if such a combination were made, however, the result would not be the subject matter recited in claims 5 and 12. Ex. 2002 at ¶¶ 49-51, *and see id.* at ¶¶ 43-44.

As noted above, Shakkarwar does not associate, by way of a look-up table or otherwise, particular GPU frequencies with particular bus frequencies. *Id.* at ¶ 50. Instead, Shakkarwar monitors bandwidth for a component, not frequency, and consults a table that includes clock speeds and/or voltage levels required to process information for specific devices. *Id.* at ¶ 43; Ex. 1006 at 7:7-10. That is in contrast to the claims, which require a “**mapping** of selectable frequencies of the graphics processing circuitry to selectable frequencies of an interconnect.” There is no teaching or suggestion that a table that includes clock speeds required to process information for specific devices has any mapping of frequencies of the kind specified. Indeed, such a table need only specify what is disclosed: the required clock speed of the affected device, for that is all that is needed to

determine the necessary bandwidth of the associated data connection. *Id.* at ¶ 50.

Moreover, as Dr. Brogioli explains, “insofar as Shakkarwar describes detecting ‘a change in processing condition[s],’ those changed processing conditions are not the *frequency* of any components, but rather the anticipated data needs of software.” *Id.* at ¶ 43 (citing Shakkarwar at 6:8-16, 49 *et seq.*) (emphasis added). Note that Shakkarwar specifies the look-up table reports clock speeds, etc. *required to process information* for specific devices. Ex. 1006 at 7:7-10. By highlighting information processing needs, Shakkarwar is indicating that the clock speeds are tied to particular data needs of software. Ex. 2022 at ¶ 44. Considerations of the hardware are handled through empirical calculation, by knowing the requested data bandwidth of each device. *Id.*; Ex. 1006 at 7:10-17. This further exemplifies why the look-up table does not provide any mapping of GPU frequencies to interconnect frequencies, and instead merely reports the device clock speeds (and/or voltages). Ex. 2002 at ¶ 44.

Thus, Shakkarwar does not associate any particular GPU frequencies with particular bus frequencies; and, in particular, disclose or suggest a mapping of selectable frequencies of a GPU to selectable frequencies of an interconnect, as required by claims 5 and 12. Therefore, even if a person of

ordinary skill in the art were to combine the teachings of Shakkarwar with those of Nussbaum, e.g., as suggested by Petitioner through the use of Shakkarwar's look-up table in as part of a power allocation controller in a system such as that described by Nussbaum, the result would not be the invention recited in claims 5 and 12 of the '588 patent. *Id.* at ¶ 51. Hence, the petition fails to set forth a prima facie case of obviousness of claims 5 and 12 in view of Nussbaum-Shakkarwar, *CFMT, Inc.*, 349 F.3d at 1342, and likewise fails to satisfy its obligation to "specify where each element of the claim is found in the prior art." 37 C.F.R. § 42.104(b)(4).

D. Claims 6 and 13 Are Not Obvious in View of Nussbaum-Shakkarwar

Challenged claim 6 depends from claim 5 and claim 13 depends from claim 12. Each respective dependent claim is not unpatentable in view of Nussbaum-Shakkarwar for at least the same reasons as claims 5 and 12, above. *See Hartness Int'l. Inc.*, 819 F.2d 1100.

IV. CONCLUSION

For at least the foregoing reasons, the Board should find that Petition has failed to prove the unpatentability of any of claims 5, 6, 12, and 13.

Harmonic Inc. v. Avid Tech., Inc., 815 F.3d 1356, 1363 (Fed. Cir. 2016) ("In

an [inter partes review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.”) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (the burden of persuasion never shifts to the Patent Owner); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (a petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements”).

Dated: May 24, 2024

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WORD-COUNT CERTIFICATE

I certify that the foregoing document complies with the type-volume limitation of 37 C.F.R. § 42.24(a) and (b) and contains 5,569 words (including words in drawings created by the Patent Owner or as annotations added by the Patent Owner to images reproduced in this document) based on the word count indicated by Microsoft® Word for Mac v. 16.84, excluding those portions exempted by the rule.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing:

PATENT OWNER'S RESPONSE

and its accompanying exhibits were served on May 24, 2024, by filing this document through the P-TACTS System as well as by delivering a copy via email directed to the attorneys of record for the Petitioner at the following addresses:

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