

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

Case IPR2023-01345
U.S. Patent No. 10,705,588

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

Filed on behalf of Petitioner:

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PETITIONER'S EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 10,705,588 (the "'588")
1002	The '588 Prosecution History
1003	Declaration of Robert W. Horst, Ph.D. ("Horst Decl.")
1004	Curriculum Vitae of Robert W. Horst, Ph.D.
1005	U.S. Patent No. 7,263,457 to White et al. ("White")
1006	U.S. Patent No. 7,392,411 to Shakkarwar ("Shakkarwar")
1007	U.S. Patent Pub. No. 2011/0022356 to Nussbaum et al. ("Nussbaum")
1008	U.S. Patent No. 10,037,067 (the "'067")
1009	The '067 Prosecution History
1010	U.S. Patent No. 9,354,692 (the "'692")
1011	Chetana Keltcher, et al., <i>AMD Athlon Northbridge with 4x AGP and Next Generation Memory Subsystem</i> (1999)
1012	U.S. Patent Pub. No. 2010/0115304 to Finkelstein et al. ("Finkelstein")
1013	Deposition Transcript of Dr. Michael Brogioli taken August 23, 2024 in Case No. IPR2023-01345 ("Brogioli Tr.")

I. Introduction

In response to Petitioner's challenge to claims 1-20 of the '588, **Patent Owner concedes that claims 1-4, 7-11, and 14-20 are invalid** and that their elements were well-known as of the '588's priority date.¹ Patent Owner disputes only whether the prior art renders obvious a single element of challenged claims 5 and 12 (and claims 6 and 13 that depend therefrom): "a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect." (*See generally* Patent Owner's Response ("POR"), Paper 10.)

Yet this dispute is simply a rehashing of Patent Owner's unpersuasive argument from IPR2023-00547. *See* Patent Owner's Preliminary Response, *Qualcomm Inc. v. Daedalus Prime LLC*, No. IPR2023-00547, Paper 12 at 24-25, 2023 WL 4566657 (P.T.A.B. July 17, 2023). The Board was unconvinced by this argument there and should reject it again in this proceeding. *See Qualcomm Inc. v.*

¹ *See* Paper 8 at 9 ("Patent Owner is cautioned that any arguments not raised in the response may be deemed waived."). *See also In re Nuvasive, Inc.*, 842 F.3d 1376, 1380-81 (Fed. Cir. 2016) (holding that a patent owner waives an argument by failing to present it in its Response in the Board); *Hum Indus. Tech., Inc. v. Amsted Rail Co., Inc.*, No. IPR2023-00540, Paper 43 at 46-47, 63 (P.T.A.B. Aug. 6, 2024) (same, with respect to limitations not disputed in the patent owner's Response).

Daedalus Prime LLC, No. IPR2023-00547, Paper 13 at 36-38 (P.T.A.B. Sept. 19, 2023).

Shakkarwar is undisputedly combinable with White and Nussbaum, and Patent Owner does not contend otherwise. And the resulting White-Shakkarwar and Nussbaum-Shakkarwar combinations render claims 5, 6, 12, and 13 obvious because they disclose look-up tables (*i.e.*, a mapping) that correlate selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect.

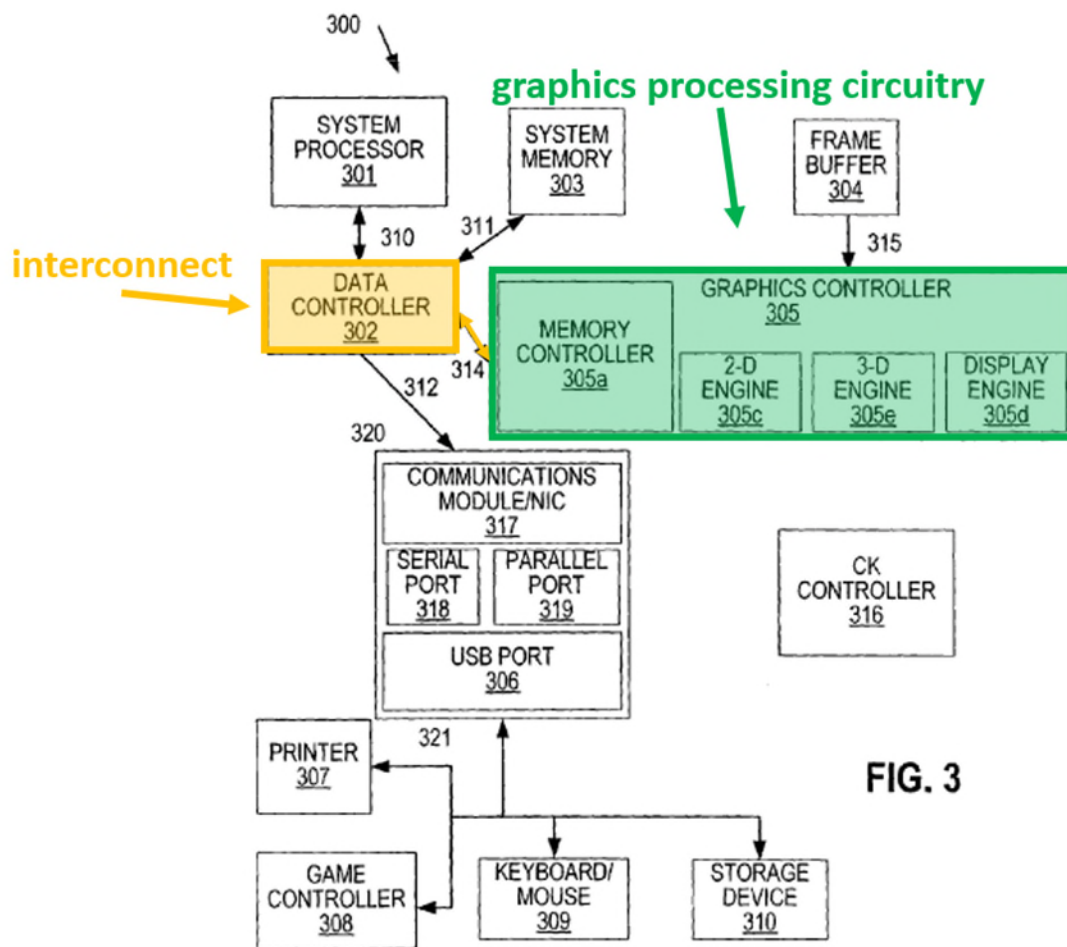
Each claim of the '588 is therefore anticipated and/or obvious over the prior art, as explained herein and in the Petition. Petitioner accordingly respectfully requests cancellation of claims 1-20 of the '588.

II. Shakkarwar Discloses the Claimed “Mapping,” So Dependent Claims 5 And 12 Are Obvious Over White Or Nussbaum In View Of Shakkarwar

The parties' sole dispute in this proceeding is whether combining White or Nussbaum with Shakkarwar renders obvious “a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.” It does, because Shakkarwar discloses this element and is undisputedly combinable with White and Nussbaum.

Shakkarwar discloses a power management system and method for efficiently operating a computing system by dynamically adjusting the voltages

and frequencies of constituent computing devices. (See, e.g., Shakkarwar, Abstract, 4:40-60.) Shakkarwar's dynamic power management system includes a **graphics controller 305** connected to system memory 303 through **data controller 302** (and **data connection 314**), as illustrated in Figure 3:



(Shakkarwar, Figure 3 (annotated).) As described in the Petition and Dr. Horst's declaration, and not disputed by Patent Owner or its expert, data controller 302 is (along with data connection bus 314) an "interconnect" and the "graphics controller 305" is "graphics processing circuitry." (See Paper 2 at 49-53, 85-89;

Horst Decl. ¶¶137, 215.)

In the '588, the claimed “mapping” can be accomplished by “associat[ing] the [graphics processing circuitry] operating frequencies and corresponding interconnect operating frequencies.” ('588, 2:44-46.) The '588 illustrates an exemplary mapping in Table 1, between a “non-core domain frequency and corresponding minimum interconnect frequency.” (*Id.*, 4:57-61, 5:5-35 (Table 1).) “Non-Core Frequency” refers to the frequency of the graphics processing circuitry. (*Id.*, 4:1-4; Brogioli Tr. 35:22-36:17.) And the “Minimum Interconnect Frequency” is the “target” frequency necessary to provide the graphics processing circuitry with enough bandwidth for its workload. ('588., 2:19-39 (explaining how “graphics workload performance is a strong function of bandwidth”); 4:57-5:13).

In other words, the interconnect frequencies listed in exemplary Table 1 of the '588 are those required to avoid bottlenecking the graphics processing circuitry when it operates at its corresponding frequencies. (See Brogioli Tr. 39:15-40:6, 44:16-45:9 (describing this as the “processor-to-memory bottleneck”).) Accordingly, “when a graphics frequency changes, the [system's processor] can use the updated graphics frequency value as an index into the table to access a table entry that includes a corresponding interconnect frequency for that graphics domain frequency.” ('588, 3:10-14; *see also* Brogioli Tr. 39:15-40:17.)

Like the '588, Shakkarwar “maps” selectable frequencies of its graphics

processing circuitry to those of its interconnect. (Horst Decl. ¶138; Shakkarwar, 7:5-10.) Shakkarwar describes monitoring components' bandwidth, including that of its interconnect and its graphics controller, and determining if the interconnect's bus rate (*i.e.*, frequency) is high enough to support the graphics controller's required bandwidth. (Shakkarwar, 6:49-52; Horst Decl. ¶138.) This bandwidth (*i.e.*, throughput) is a function of frequency for a fixed connection. (See Horst Decl. ¶140 n.4.; *see also* Brogioli Tr. 29:25-30:14.) So Shakkarwar's process of monitoring-and-determining bus frequency based on graphics bandwidth requirements before and after opening a 3-D graphics application is a "mapping" of selectable interconnect and graphics processing circuitry frequencies. (Horst Decl. ¶138; Shakkarwar, 6:49-52.) Stated differently, before opening "an application that is known to use 3-D graphics," the bus and graphics processing circuitry were each operating at their respective baseline frequencies. (Shakkarwar, 6:49-52.) But after opening the application, the graphics circuitry's bandwidth requirements increase (*i.e.*, because it is operating at a higher frequency) and the bus frequency also increases to accommodate the higher graphics bandwidth requirement. (*Id.*) This association between corresponding frequencies is a "mapping."

Shakkarwar also specifically describes determining bandwidth requirements for a data connection (*i.e.*, a bus or interconnect) based on the components that are

active at any given time. (See Shakkarwar 6:63-7:7; Horst Decl. ¶139.) A “look-up table... includ[ing] a list of clock speeds [*i.e.*, frequencies²]” is then used to determine the interconnect frequency required to meet the system's bandwidth requirements. (See Horst Decl. ¶139.) These bandwidth requirements can depend on whether the graphics processing circuitry is being used (*i.e.*, having a nonzero bandwidth and frequency) or inactive (*i.e.*, having an effective frequency of zero and needing no bandwidth). (See Shakkarwar, 6:59-62; *see also id.*, 5:47-52 (describing the same in the context of whether a USB module is being used or not being used).)

As such, Shakkarwar discloses mapping idle selectable frequencies of the interconnect to the graphics processing circuitry when no bandwidth is required (*i.e.*, both frequencies are effectively zero) and discloses mapping nonzero selectable frequencies when both components are active. *Id.* In short, the Shakkarwar correlates and maps frequencies of the graphics processing circuitry (graphics controller 305) and interconnect (data controller 302 / bus 314) that may be selected to accommodate a system's given bandwidth requirements, as claimed.

² The parties agree that “clock speed” is synonymous with frequency. (Horst Decl. ¶140 & n.1; *see also* Horst Decl. ¶¶91, 138; Shakkarwar at 2:51-58; Brogioli Tr. 28:17-29:24 (same); Brogioli Decl. ¶41.)

Patent Owner's arguments in response to the Petition are confusing and difficult to parse but seem to focus on pointing out purported differences between the overall Shakkarwar system and language used in the '588, focusing on facial differences in terminology and wording. Patent Owner argues that "mapping" requires "a look-up table or otherwise"³ to "associate" GPU with bus frequencies, (POR, 1, 20, 27), but fails to specify precisely what "mapping" requires and what aspect Shakkarwar lacks. Instead, Patent Owner largely rehashes the positions it took against the *inter partes* review petitioner in Case No. IPR2023-00547, which focused on the operation of Shakkarwar's software and discussions of bandwidth. See Patent Owner's Preliminary Response, *Qualcomm Inc. v. Daedalus Prime LLC*, No. IPR2023-00547, Paper 12 at 24-25, 2023 WL 4566657 (P.T.A.B. July 17, 2023). The Board rejected Patent Owner's arguments there, concluding that Shakkarwar discloses "mapping" in part because "[it] expressly teaches that the look-up table may include a list of *clock speeds*." *Qualcomm Inc. v. Daedalus Prime LLC*, No. IPR2023-00547, Paper 13 at 37 (P.T.A.B. Sept. 19, 2023). The Board found the petitioner more persuasive in arguing that Shakkarwar's look-up table "contain[s] a list of clock speeds to determine the appropriate bandwidth for a

³ Patent Owner's expert refused to define "look-up table" or even admit that Table 1 of the '588 qualified as one. (Brogioli Tr. 23:10-27:7, 57:3-58:9.)

component (e.g., a graphics controller)” and that Shakkarwar takes into consideration the clock speeds of other active components, such as data controller (or ‘interconnect’). *Id.* at 36-37. The Board should reach the same conclusion here.

Further, the Patent Owner's expert's admissions show that Shakkarwar discloses the claimed “mapping.” Dr. Brogioli states in his declaration that “Shakkarwar determines a frequency to change the bus [*i.e.*, the interconnect] to by using “a look-up table [that] may include a list of clock speeds . . . required to process information for specific devices and/or groups of devices.” (Ex. 2002 ¶41 (quoting Shakkarwar, 7:7-10); *see* Brogioli Tr. 51:1-9.) In his view, the look-up table thus contains selectable frequencies of the interconnect that are indexed for retrieval based on information-processing requirements. And in his deposition, Dr. Brogioli went on to explain that the look-up table contains the “clock speeds and voltage levels for processing information” for “computational components,” which would include graphics processing circuitry. (Brogioli Tr. 52:15-53:14.) Taking his testimony together, Dr. Brogioli therefore interprets Shakkarwar's look-up table as containing selectable frequencies of its graphics processing circuitry and corresponding frequencies to change the interconnect to, which is analogous to the '588's Table 1 and satisfies the claimed “mapping” recited in claims 5 and 12.

III. Patent Owner Does Not Substantively Dispute Dependent Claims 6 And 13 And Rationales To Combine White Or Nussbaum With Shakkarwar

Patent Owner does not dispute Petitioner's arguments in Grounds 2 or 4 that for Claims 6 and 13 are obvious and that it is obvious to combine White's / Nussbaum's teachings with those of Shakkarwar. (Petition, 53-59, 89-94.) Patent Owner's only argument for the patentability of Claims 6 and 13 is that they are "not unpatentable in view of [White / Nussbaum]-Shakkarwar for at least the same reasons as claims 5 and 12." (See POR at 23, 29.) Patent Owner is mistaken for the reasons in the Petition and provided above and has waived any new arguments. See *supra* Section I n.1 (discussing waiver), Section II.

IV. Conclusion

For these reasons and those in the Petition, the Board should cancel claims 1-20 of U.S. Patent No. 10,705,588 as anticipated or obvious over the prior art.

Date: September 6, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned hereby certifies that the foregoing **Reply to Patent Owner's Response** contains 1,706 words, excluding those portions identified in 37 C.F.R. § 42.24(a)(1), as measured by the word-processing system used to prepare this paper.

/s/ Joseph J. Raffetto
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*One of the attorneys for Petitioner
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CERTIFICATION OF SERVICE

The undersigned certifies that in accordance with 37 C.F.R. § 42.6(e), the foregoing Petitioner's Reply To Patent Owner's Response was served on September 6, 2024 upon the following via electronic mail:

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