

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,

Petitioner,

v.

DAEDALUS PRIME LLC,

Patent Owner.

Case No.: IPR2023-01345

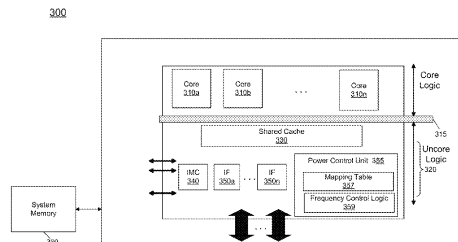
U.S. Patent No. 10,705,588

Patent Owner's Demonstrative Exhibits

'588 Patent

(12) United States Patent Ananthakrishnan et al.	(10) Patent No.: US 10,705,588 B2 (45) Date of Patent: *Jul. 7, 2020
(54) ENABLING A NON-CORE DOMAIN TO CONTROL MEMORY BANDWIDTH IN A PROCESSOR	(58) Field of Classification Search CPC combination set(s) only. See application file for complete search history.
(71) Applicant: Intel Corporation , Santa Clara, CA (US)	(56) References Cited
(72) Inventors: Avinash N. Ananthakrishnan , Portland, OR (US); Inder M. Sodhi , Folsom, CA (US); Efraim Rotem , Haifa (IL); Doron Rajwan , Rishon Le-Zion (IL); Eliezer Weissmann , Haifa (IL); Ryan Wells , Folsom, CA (US)	U.S. PATENT DOCUMENTS 5,163,153 A 11/1992 Cole et al. 5,287,292 A 2/1994 Kenny et al. (Continued)
(73) Assignee: Intel Corporation , Santa Clara, CA (US)	FOREIGN PATENT DOCUMENTS CN 101351759 A 1/2009 CN 101403944 A 4/2009 (Continued)
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days. This patent is subject to a terminal disclaimer.	OTHER PUBLICATIONS Taiwan Intellectual Property Office, Office Action dated Nov. 2, 2015 in Taiwan Patent Application No. 103146274. (Continued)
(21) Appl. No.: 16/249,103	Primary Examiner — Raymond N Phan
(22) Filed: Jan. 16, 2019	(74) Attorney, Agent, or Firm — Trop, Pruner & Hu, P.C.
(65) Prior Publication Data US 2019/0212801 A1 Jul. 11, 2019	(57) ABSTRACT
Related U.S. Application Data (63) Continuation of application No. 15/381,241, filed on Dec. 16, 2016, now Pat. No. 10,248,181, which is a (Continued)	In one embodiment, the present invention includes a processor having multiple domains including at least a core domain and a non-core domain that is transparent to an operating system (OS). The non-core domain can be controlled by a driver. In turn, the processor further includes a memory interconnect to interconnect the core domain and the non-core domain to a memory coupled to the processor. Still further, a power controller, which may be within the processor, can control a frequency of the memory interconnect based on memory boundedness of a workload being executed on the non-core domain. Other embodiments are described and claimed.
(51) Int. Cl. G06F 1/324 (2019.01) G06F 1/3293 (2019.01) (Continued)	
(52) U.S. Cl. CPC G06F 1/324 (2013.01); G06F 1/3203 (2013.01); G06F 1/3293 (2013.01); (Continued)	

20 Claims, 5 Drawing Sheets



The '588 patent describes a multicore processor in which different components (individual CPU cores, graphics processing circuitry, and an interconnect) can operate at different, independent voltages and/or frequencies. Such components can include.

The processor includes a power control unit and frequency control logic to dynamically update the frequency of interconnect based on a frequency of the graphics engine.

The graphics engine can control its own memory bandwidth. Thus, performance of the graphics engine is improved over that which it might otherwise be, particularly since, for a graphics engine, workload performance is a strong function of the bandwidth available to it.

Ex. 1001 1:57-2:39; 6:47-63
POR, 3-4

'588 Patent

Control of the memory bandwidth is provided by a mechanism that maps the graphics engine frequency to a corresponding interconnect frequency. “This mapping can be maintained in a table, which may be located in a power controller of the processor such as a power control unit (PCU).” The mapping table includes a plurality of entries each having two parameters, namely graphics engine (or “non-core domain”) frequency and corresponding minimum interconnect frequency, e.g., specified in MHz.

The table is configured during initialization (e.g., the graphics engine can set up this table in PCU memory by specifying pairwise entries to identify a target interconnect frequency for a corresponding graphics engine frequency) and can be dynamically updated based on a workload being executed by the graphics engine. After configuration, the PCU can access the table based on a frequency at which the graphics engine is operating to obtain the corresponding target interconnect frequency. In this way, a close association between the workload being handled in graphics engine and the bandwidth of the path to the memory subsystem can be achieved.

Claims 5 and 12 of the '588 patent recite the “mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.”

TABLE 1

Table Entry	Non-Core Frequency	Minimum Interconnect Frequency
1	300	800
2	350	800
3	400	800
4	450	800
5	500	800
6	550	800
7	600	800
8	650	1500
9	700	1500
11	750	1500
12	800	1500
13	850	1500
14	900	1800
15	950	1900
16	1000	2000
17	1050	2100
18	1100	2200
19	1150	2300
20	1200	2400
21	1250	2500
22	1300	2600

Ex. 1001 2:19 *et seq.*; 4:57 – 5:1; 8:62-65; 9:37 – 10:2.
POR, 4-6

'588 Claim Construction

Claims 5 and 12 each require a mapping of a set of possible frequencies of the graphics processing circuitry that can be selected to a set of possible frequencies of the interconnect that can be selected.

Horst Deposition 23:1-11

5. The processor of claim 4, wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.

12. The system of claim 11, wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.

1 So I interpret that to mean that there are a
2 set of possible frequencies that can be selected.
3 BY MR. FAHMI:
4 Q And if we look at claim 12, which begins at
5 the bottom of column 9 and carries over to the top of
6 column 10, it also recites the mapping of selectable
7 frequencies.
8 Would that have the same meaning in claim 12
9 as it does in claim 5?
10 A Yes. Claims 5 and 12, again, I analyzed
11 together with similar limitations.

Brogioli Dec. at ¶ 33;
POR, 9.

'588 Challenges

Claims Challenged	35 U.S.C. §	References
5, 6, 12, 13	103	White in view of Shakkarwar
5, 6, 12,13	103	Nussbaum in view of Shakkarwar

White

A processor or other integrated circuit may include multiple logic cores, each of which may be configured to operate at frequencies and voltages independently of the other logic cores, according to one embodiment of the present invention.

White, 2:15-18.

(12) **United States Patent**
White et al.

(54) **SYSTEM AND METHOD FOR OPERATING COMPONENTS OF AN INTEGRATED CIRCUIT AT INDEPENDENT FREQUENCIES AND/OR VOLTAGES**

(75) Inventors: **Scott A. White**, Austin, TX (US);
William A. Hughes, San Jose, CA (US); **Philip E. Madrid**, Round Rock, TX (US)

(73) Assignor: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 156(b) by 0 days.

(21) Appl. No.: **11/925,054**

(22) Filed: **Jan. 3, 2006**

(65) **Prior Publication Data**
US 2007/0156370 A1 Jul. 5, 2007

(51) Int. Cl. **G01K 1/08** (2006.01)

(52) U.S. CL. **702/132**

(58) **Field of Classification Search** **702/132**
See application file for complete search history.

(10) **Patent No.: US 7,263,457 B2**

(45) **Date of Patent: Aug. 28, 2007**

(56) **References Cited**
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6,991,303 B2 * 5/2005 Larson et al. 700/108
7,228,242 B2 * 6/2007 Read et al. 702/57
2003/0115013 A1 * 6/2003 Dendinger 702/132
2006/0161375 A1 * 7/2006 Dabirian et al. 702/132
* cited by examiner
Primary Examiner—John Barlow
Assistant Examiner—Jonathan Moffat
(74) *Attorney, Agent, or Firm*—Robert C. Kowert; Meyerson, Hood, Kiwin, Kowert & Goetzel, P.C.

(57) **ABSTRACT**
Multiple logic cores of integrated circuits and processors may be configured to operate at frequencies and voltages independently of each other. Additionally, other components, such as a common bridge configured to interface with the logic cores, may operate at a voltage and frequency independent of the voltage and frequency at which the logic cores are operating. The operating frequency and/or voltage of a logic core may be independently adjusted for various reasons, including power management and temperature control. Logic circuitry at an interface between the controller and the logic cores may translate logic signals from one voltage and/or frequency to another to enable communication between the bridge and the logic core when the two are operating at different voltages and/or frequencies.

32 Claims, 9 Drawing Sheets

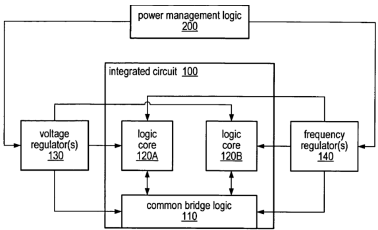
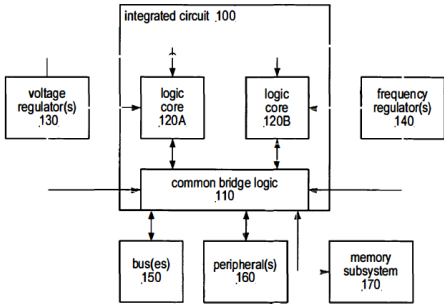


FIG. 2A

FIG. 2A illustrates a block diagram representing one embodiment of a system including multi-core integrated circuit 100. In the embodiment illustrated by FIG. 2A, power management logic 200 may be configured to control the operating characteristics, such as the operating voltage and/or operating frequency, of each of multiple logic cores 120 of integrated circuit 110.

White 8:61-65.

White

When a need to change an operating characteristic, e.g., frequency (FIG. 4) or voltage (FIG. 5), of a logic core is detected (400, 500), power management logic 200 determines a new operating voltage/frequency for the core (410, 510). New frequencies may be determined based on a “standard algorithm” or “from a look-up table.” New voltages may be determined via a voltage determining algorithm based upon current operating conditions for the system or a fixed table of operating voltages.

Assuming the new frequency is compatible with the operating voltage of the core (420), or after making adjustments therefor (430, 440), the power management logic sets the new operating frequency for the core (450 and then adjusts the operating conditions for the common bridge logic to be compatible with the new operating frequency (460).

In the case of a new operating voltage, the power management logic sets the new voltage (520), determines whether the operating frequency of the core is compatible with the new voltage (530), and adjusts the operating frequency as necessary (540, 550).

Thereafter, the power management logic adjusts the operating conditions for the common bridge logic to be compatible with the new operating voltage and/or frequency of the core (560).

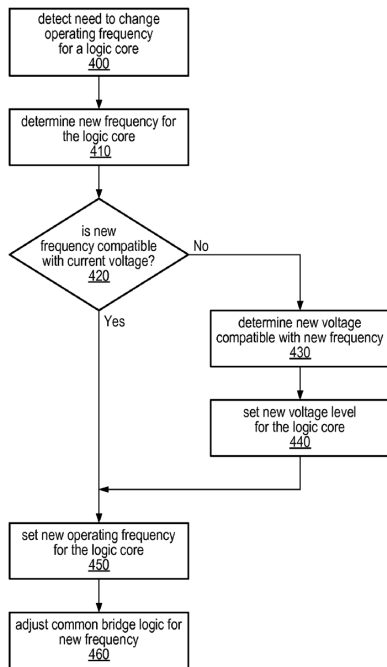


FIG. 4

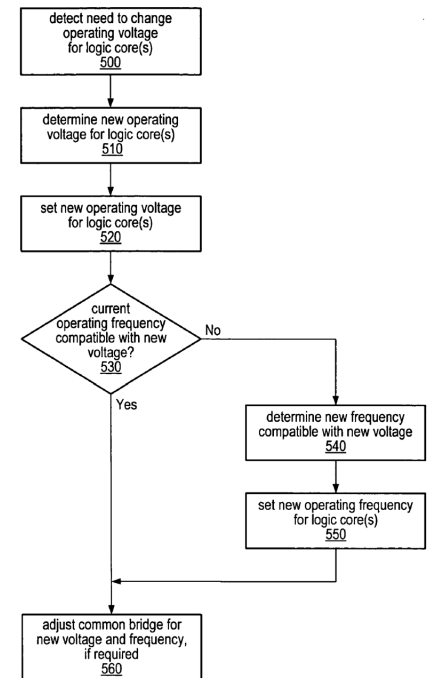


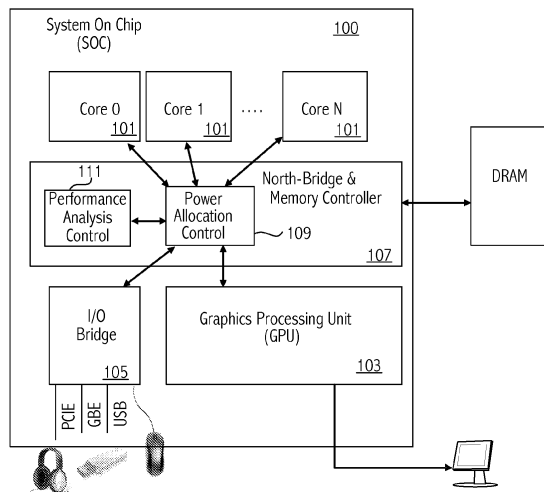
FIG. 5

Nussbaum

- (19) **United States**
- (12) **Patent Application Publication** (10) **Pub. No.: US 2011/0022356 A1**
Nussbaum et al. (43) **Pub. Date: Jan. 27, 2011**
- (54) **DETERMINING PERFORMANCE SENSITIVITIES OF COMPUTATIONAL UNITS** (52) **U.S. CL. 702/182**
- (76) **Inventors:** **Sebastien Nussbaum**, Lexington, MA (US); **Alexander Branover**, Chestnut Hill, MA (US); **John Kalamatianos**, Arlington, MA (US)
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- (21) **Appl. No.: 12/508,902**
- (22) **Filed: Jul. 24, 2009**
- Publication Classification**
- (51) **Int. Cl. G06F 15/00 (2006.01)**

(57) **ABSTRACT**

Performance sensitivities to a change in performance capabilities of computational units of a computer system are determined based on measured utilization metrics for each of the computational units. In order to determine the performance sensitivities, in one approach, the computational units are operated at a first performance level, and respective first utilization metrics are determined. The computational units are then operated at a second performance level and respective second utilization metrics are determined. The sensitivity to performance capability change, e.g., a frequency change, is determined based on the respective first and second utilization metrics. The performance sensitivities of the computational units to a change in performance capability are continually updated in response to, e.g., a process context change of a computational unit or in response to a predetermined period of time elapsing since the last sensitivity to a performance capability change was determined for a computational unit.



Nussbaum describes an “analysis of workload executed on computational units to help identify those computational units that are more performance sensitive to a change in performance capability caused by, e.g., a frequency change.”

The computational units are operated at a first performance level, and respective first utilization metrics are determined. The computational units are then operated at a second performance level and respective second utilization metrics are determined. The sensitivity to performance capability change, e.g., a frequency change, is determined.

Power distribution is then based on these measured frequency sensitivities.

Shakkarwar

(12) **United States Patent**
Shakkarwar

(10) **Patent No.:** **US 7,392,411 B2**
(45) **Date of Patent:** **Jun. 24, 2008**

(54) **SYSTEMS AND METHODS FOR DYNAMIC VOLTAGE SCALING OF COMMUNICATION BUS TO PROVIDE BANDWIDTH BASED ON WHETHER AN APPLICATION IS ACTIVE**

6,754,129 B2 * 6/2004 Khatri et al. 365/226
7,096,377 B2 * 8/2006 Kumar et al. 713/600
2002/0120878 A1 * 8/2002 Lapidus 713/300

OTHER PUBLICATIONS

(75) Inventor: **Rajesh G. Shakkarwar**, Cupertino, CA (US)

F. Worm, P. Jenne, P. Thiran, and G. De Micheli, "An adaptive low-power transmission scheme for on-chip networks," International Symposium on System Synthesis, pp. 92-100, 2002.*
L. Shang, I. Peh, and N. K. Jha, "Power-efficient interconnection networks: Dynamic voltage scaling with links," IEEE Computer Architecture Letters, vol. 1, No. 5, 2002.*
G.-Y. Wei, J. Kim, D. Liu, S. Sidiropoulos, and M. A. Horowitz, "A variable-frequency parallel I/O interface with adaptive power-supply regulation," IEEE Journal of Solid-State Circuits, vol. 35, No. 11, Nov. 2000.*

(73) Assignee: **ATI Technologies, Inc.**, Markham, Ontario (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 750 days.

(21) Appl. No.: **10/423,290**

* cited by examiner
Primary Examiner—Chun Cao
Assistant Examiner—Albert Wang

(22) Filed: **Apr. 25, 2003**

(65) **Prior Publication Data**
US 2004/0215986 A1 Oct. 28, 2004

(57) **ABSTRACT**

(51) **Int. Cl.**
G06F 1/32 (2006.01)

Systems and methods for dynamic power management of electronic devices are disclosed. In one form, a system employing dynamic power management for electronic devices includes a central processing unit operable to process information via a communication bus. The system includes a clock generator and a voltage generator coupled to the processing unit and operably associated with the communication bus having multiple operating voltage levels. The clock generator and communication bus are operated at variable clock rates and voltage levels to ensure bandwidth requirements are satisfied for communicating and processing information. In this manner, power consumption of the system may be dynamically managed while providing sufficient bandwidth for the system.

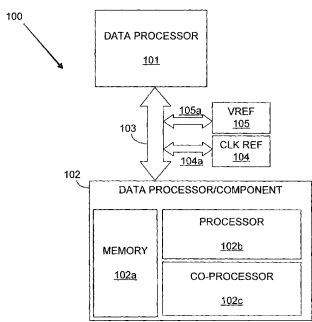
(52) **U.S. Cl.** 713/320; 710/104

(58) **Field of Classification Search** 710/104; 713/300, 320
See application file for complete search history.

(56) **References Cited**
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5,630,163 A * 5/1997 Fung et al. 710/307
6,072,334 A * 6/2000 Chang 326/82
6,453,374 B1 * 9/2002 Kovalan et al. 710/100
6,535,945 B1 * 3/2003 Tobin et al. 710/305

25 Claims, 5 Drawing Sheets



Shakkarwar is concerned with adjusting the data rate of a bus based on analysis of software being executed by a processor, or on detecting that certain components connected to the bus are idle or otherwise unused.

For example, when the system detects that no software applications are using a GPU, the system can decide to reduce the data rate (i.e., reduce the bandwidth) over the bus to save power. Similarly, when the system detects that an application was opened that is likely to require the GPU, the system will increase the data rate between the data controller and the graphics controller to support the functionality of the application.

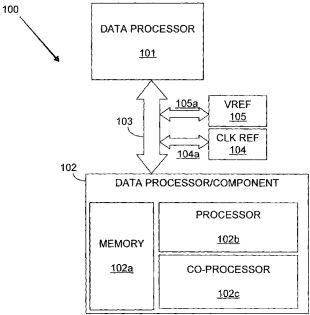
Shakkarwar determines a frequency to change the bus to by using “a look-up table [that] may include a list of clock speeds ... required to process information for specific devices and/or groups of devices.”

Shakkarwar, 5:53 – 7:26; 8:50-56;
POR, 17-18.

Shakkarwar

(12) United States Patent Shakkarwar	(10) Patent No.: US 7,392,411 B2 (45) Date of Patent: Jun. 24, 2008
(54) SYSTEMS AND METHODS FOR DYNAMIC VOLTAGE SCALING OF COMMUNICATION BUS TO PROVIDE BANDWIDTH BASED ON WHETHER AN APPLICATION IS ACTIVE	6,754,129 B2 * 6/2004 Khatri et al. 365/226 7,096,377 B2 * 8/2006 Kumar et al. 713/600 2002/0120878 A1 * 8/2002 Lapidus 713/300
(75) Inventor: Rajesh G. Shakkarwar , Cupertino, CA (US)	OTHER PUBLICATIONS F. Worm, P. Ienne, P. Thiran, and G. De Micheli, "An adaptive low-power transmission scheme for on-chip networks," International Symposium on System Synthesis, pp. 92-100, 2002.* L. Shang, L. Peh, and N. K. Jha, "Power-efficient interconnection networks: Dynamic voltage scaling with links," IEEE Computer Architecture Letters, vol. 1, No. 5, 2002.* G.-Y. Wei, J. Kim, D. Liu, S. Sidiropoulos, and M. A. Horowitz, "A variable-frequency parallel I/O interface with adaptive power-supply regulation," IEEE Journal of Solid-State Circuits, vol. 35, No. 11, Nov. 2000.*
(73) Assignee: ATI Technologies, Inc. , Markham, Ontario (CA)	* cited by examiner Primary Examiner—Chun Cao Assistant Examiner—Albert Wang
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 750 days.	
(21) Appl. No.: 10/423,290	
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(65) Prior Publication Data US 2004/0215986 A1 Oct. 28, 2004	(57) ABSTRACT Systems and methods for dynamic power management of electronic devices are disclosed. In one form, a system employing dynamic power management for electronic devices includes a central processing unit operable to process information via a communication bus. The system includes a clock generator and a voltage generator coupled to the processing unit and operably associated with the communication bus having multiple operating voltage levels. The clock generator and communication bus are operated at variable clock rates and voltage levels to ensure bandwidth requirements are satisfied for communicating and processing information. In this manner, power consumption of the system may be dynamically managed while providing sufficient bandwidth for the system.
(51) Int. Cl. G06F 1/32 (2006.01)	
(52) U.S. Cl. 713/320; 710/104	
(58) Field of Classification Search 710/104; 713/300, 320 See application file for complete search history.	
(56) References Cited U.S. PATENT DOCUMENTS 5,423,009 A * 6/1995 Zhu 710/307 5,630,163 A * 5/1997 Fung et al. 710/307 6,072,334 A * 6/2000 Chang 326/82 6,453,374 B1 * 9/2002 Kovalan et al. 710/100 6,535,945 B1 * 3/2003 Tobin et al. 710/305	

25 Claims, 5 Drawing Sheets



Upon detecting a change in processing, the method determines bandwidth 403 for an associated data connection based on the active components. For example, a look-up table may include a list of clock speeds, and/or voltage levels required to process information for specific devices and/or groups of devices.

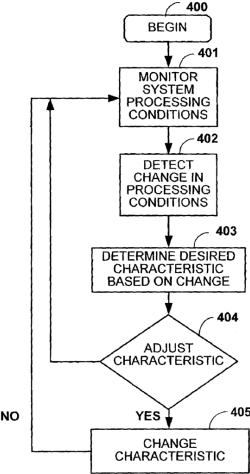


FIG. 4

Shakkarwar at 7:7-10
Fig. 4

Failings of White-Shakkarwar & Nussbaum-Shakkarwar

Petition Arguments

White-Shakkarwar / Nussbaum-Shakkarwar teaches or suggests a mapping of selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect, specifically the look-up table disclosed at 7:5-10 of Shakkarwar.

A POSITA would have understood Shakkarwar teaches such a mapping using the look-up table, because Shakkarwar determines an appropriate bandwidth for a data connection utilizing the look-up table that includes a list of appropriate clock speeds while also considering other active components and their clock speeds.

Pet. at 52-53, 88-89;
POR, 20-22, 27-28.

Flaws

Shakkarwar does not associate, by way of a look-up table or otherwise, particular GPU frequencies with particular bus frequencies.

Dr. Horst testified that claims 5 and 12 require a mapping of a set of possible frequencies of the graphics processing circuitry that can be selected to a set of possible frequencies of the interconnect that can be selected. *Horst Tr.* at 21:19 – 22:11.

Shakkarwar, on the other hand, monitors bandwidth for a component (not frequency), and consults a table that includes clock speeds and/or voltage levels required to process information for specific devices. *Brogioli Dec.* at ¶ 43 (citing *Shakkarwar* at 7:7-10); *Horst Tr.* at 24:9 – 25:2.

There is no teaching or suggestion that this table, which simply includes clock speeds required to process information for specific devices, has any *mapping* of frequencies, let alone frequencies that can be selected, of the kind specified. *Brogioli Dec.* at ¶¶ 43-44.

Failings of White-Shakkarwar & Nussbaum-Shakkarwar

Petition Arguments

White-Shakkarwar / Nussbaum-Shakkarwar teaches or suggests a mapping of selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect, specifically the look-up table disclosed at 7:5-10 of Shakkarwar.

A POSITA would have understood Shakkarwar teaches such a mapping using the look-up table, because Shakkarwar determines an appropriate bandwidth for a data connection utilizing the look-up table that includes a list of appropriate clock speeds while also considering other active components and their clock speeds.

Pet. at 52-53, 88-89;
POR, 20-22, 27-28.

Flaws

Insofar as Shakkarwar describes detecting “a change in processing condition[s],” Ex. 1006 at 6:49 *et seq.*, those changed processing conditions are the anticipated data needs of software, not the frequency of any devices..

Shakkarwar specifies the look-up table reports clock speeds, etc. required to process information for specific devices. Ex. 1006 at 7:7-10.

By highlighting information processing needs, Shakkarwar is indicating that the clock speeds are tied to particular data needs of the devices. Considerations of the hardware are addressed through empirical calculation, by knowing the requested data bandwidth of each device. Ex. 1006 at 7:10-17. This explains why the look-up table does not need to and does not provide any mapping of frequencies, and instead merely reports the device clock speeds (and/or voltages).

Brogioli Dec. at ¶ 44.

Conclusion

The Petition has failed to prove the unpatentability of any of the challenged claims.